

Optimization of Transition Edge Sensor Arrays for Cosmic Microwave Background Observations With the South Pole Telescope

Junjia Ding, P. A. R. Ade, A. J. Anderson, J. Avva, Z. Ahmed, K. Arnold, J. E. Austermann, A. N. Bender, B. A. Benson, L. E. Bleem, K. Byrum, J. E. Carlstrom, F. W. Carter, C. L. Chang, H. M. Cho, J. F. Cliche, A. Cukierman, D. Czaplewski, R. Divan, T. de Haan, M. A. Dobbs, D. Dutcher, W. Everett, A. Gilbert, R. Gannon, R. Guyser, N. W. Halverson, N. L. Harrington, K. Hattori, J. W. Henning, G. C. Hilton, W. L. Holzapfel, J. Hubmayr, N. Huang, K. D. Irwin, O. Jeong, T. Khaire, D. Kubik, C. L. Kuo, A. T. Lee, E. M. Leitch, S. S. Meyer, C. S. Miller, J. Montgomery, A. Nadolski, T. Natoli, H. Nguyen, V. Novosad, S. Padin, Z. Pan, J. Pearson, C. M. Posada, A. Rahlín, C. L. Reichardt, J. E. Ruhl, B. R. Saliwanchik, J. T. Sayre, J. A. Shariff, I. Shirley, E. Shirokoff, G. Smecher, J. Sobrin, L. Stan, A. A. Stark, K. Story, A. Suzuki, Q. Y. Tang, R. B. Thakur, K. L. Thompson, C. Tucker, K. Vanderlinde, J. D. Vieira, G. Wang, N. Whitehorn, W. L. K. Wu, V. Yefremenko, and K. W. Yoon

Abstract—In this paper, we describe the optimization of transition-edge-sensor (TES) detector arrays for the third-generation camera for the South Pole Telescope. The camera, which contains $\sim 16\,000$ detectors, will make high-angular-resolution maps of the temperature and polarization of the cosmic microwave background. Our key results are scatter in the transition temperature of Ti/Au TESs is reduced by fabricating the TESs on a thin Ti(5 nm)/Au(5 nm) buffer layer and the thermal conductivity of the legs that support our detector islands is dominated by the SiO_x dielectric in the microstrip transmission lines that run along

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J. Ding, R. Gannon, T. Khaire, V. Novosad, J. Pearson, and C. M. Posada are with the Argonne National Laboratory, Material Science Division, Argonne, IL 60439 USA (e-mail: dingj@anl.gov).

P. A. R. Ade and C. Tucker are with the Cardiff University, Cardiff CF24 3YB, U.K.

A. J. Anderson is with the Fermi National Accelerator Laboratory, Batavia, IL 60510 USA, and also with the Kavli Institute for Cosmological Physics, University of Chicago, Chicago, IL 60637 USA.

J. Avva, A. Cukierman, T. de Haan, N. L. Harrington, W. L. Holzapfel, N. Huang, O. Jeong, I. Shirley, A. Suzuki, N. Whitehorn, and W. L. K. Wu are with the Department of Physics, University of California, Berkeley, CA 94720 USA.

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Z. Ahmed, K. D. Irwin, C. L. Kuo, K. L. Thompson, and K. W. Yoon are with the Kavli Institute for Particle Astrophysics and Cosmology and the Department of Physics, Stanford University, Stanford, CA 94305 USA, and also with the SLAC National Accelerator Laboratory, Menlo Park, CA 94025 USA.

K. Arnold is with the Department of Physics, University of Wisconsin, Madison, WI 53706 USA.

J. E. Austermann, G. C. Hilton, and J. Hubmayr are with the NIST Quantum Devices Group, Boulder, CO 80305 USA.

A. N. Bender, L. E. Bleem, and F. W. Carter are with Argonne National Laboratory, High-Energy Physics Division, Argonne, IL 60439 USA, and also with the Kavli Institute for Cosmological Physics, University of Chicago, Chicago, IL 60637 USA.

B. A. Benson is with the Fermi National Accelerator Laboratory, Batavia, IL 60510 USA, and also with the Kavli Institute for Cosmological Physics and the Department of Astronomy and Astrophysics, University of Chicago, Chicago, IL 60637 USA.

K. Byrum, G. Wang, and V. Yefremenko are with the Argonne National Laboratory, High-Energy Physics Division, Argonne, IL 60439 USA.

J. E. Carlstrom is with the Kavli Institute for Cosmological Physics, the Enrico Fermi Institute, the Department of Physics, and the Department of Astronomy and Astrophysics, University of Chicago, Chicago, IL 60637 USA, and also with the Argonne National Laboratory, High-Energy Physics Division, Argonne, IL 60439 USA.

C. L. Chang and S. Padin are with the Argonne National Laboratory, High-Energy Physics Division, Argonne, IL 60439 USA, and also with the Kavli Institute for Cosmological Physics, the Department of Astronomy and Astrophysics, University of Chicago, Chicago, IL 60637 USA.

H. M. Cho is with the SLAC National Accelerator Laboratory, Menlo Park, CA 94025 USA.

J. F. Cliché, A. Gilbert, and J. Montgomery are with the Department of Physics, McGill University, Montreal, QC H3A 2T8, Canada.

E. M. Leitch, E. Shirokoff, and Q. Y. Tang are with the Kavli Institute for Cosmological Physics and also with the Department of Astronomy and Astrophysics, University of Chicago, Chicago, IL 60637 USA.

D. Czaplewski, R. Divan, C. S. Miller, and L. Stan are with the Argonne National Laboratory, Center for Nanoscale Materials, Argonne, IL 60439 USA.

M. A. Dobbs is with the Department of Physics, McGill University, Montreal, QC H3A 2T8, Canada, and also with the Canadian Institute for Advanced Research, CIFAR Program in Cosmology and Gravity, Toronto, ON M5G 1Z8, Canada.

D. Dutcher, Z. Pan, and J. Sobrin are with the Kavli Institute for Cosmological Physics and also with the Department of Physics, University of Chicago, Chicago, IL 60637 USA.

W. Everett and J. T. Sayre are with the CASA, Department of Astrophysical and Planetary Sciences, University of Colorado, Boulder, CO 80309 USA.

I. INTRODUCTION

CURRENT cosmic microwave background (CMB) [1], [2] experiments aim to precisely measure the CMB polarization, especially the parity-violating B-mode polarization [3], with the goal of measuring the energy scale of inflation, the number of neutrino species, and the sum of masses of neutrinos [4], [5]. The measurements require exquisite sensitivity, which means large-format cameras with many bands for removing foreground signals [6]. One such camera, which is being built for the next-generation experiment on the South Pole Telescope (SPT-3G) [7], has 2690 pixels, each with 6 transition-edge sensor (TES) detectors [8], [9] measuring 2 linear polarizations in 3 bands, and will be deployed at the end of 2016.

In this paper, we describe the optimization of the TES detector arrays for SPT-3G. The TES critical temperature (T_c) distributions of wafers prepared by two different detector fabrication processes and two different TES film structures have been systematically investigated. The result shows that the TES performance becomes more controllable if the TES is prepared on an unetched surface with a thin Ti(5 nm)/Au(5 nm) buffer layer. It worth to mention that the main target of this work is the T_c scattering over the wafer rather the absolute values. The thermal link, a LSN (low-stress silicon nitride)/Nb/SiO_x/Nb quadruple layer structure, is another critical component for the detector array. Two test wafers were fabricated to investigate the detailed thermal link properties as functions of the film structure and the leg dimensions. We found that the thermal conductance is approximately linearly dependent on the leg width-to-length ratio

R. Guyser and A. Nadolski are with the Astronomy Department, University of Illinois, Urbana, IL 61801 USA.

N. W. Halverson is with the CASA, Department of Astrophysical and Planetary Sciences and also with the Department of Physics, University of Colorado, Boulder, CO 80309 USA.

K. Hattori is with the High Energy Accelerator Research Organization, Tsukuba 305-0801, Japan.

J. W. Henning and R. B. Thakur are with the Kavli Institute for Cosmological Physics, University of Chicago, Chicago, IL 60637 USA.

D. Kubik, H. Nguyen, and A. Rahlin are with the Fermi National Accelerator Laboratory, Batavia, IL 60510 USA.

A. T. Lee is with the University of California, Berkeley, CA 94720 USA, and also with the Physics Division, Lawrence Berkeley National Laboratory, Berkeley, CA 94720 USA.

S. S. Meyer is with the Kavli Institute for Cosmological Physics, the Enrico Fermi Institute, the Department of Physics, and also with the Department of Astronomy and Astrophysics, University of Chicago, Chicago, IL 60637 USA.

T. Natoli is with the Dunlap Institute for Astronomy and Astrophysics, University of Toronto, Toronto, ON M5S 3H4, Canada.

C. L. Reichardt is with the School of Physics, University of Melbourne, Parkville, VIC 3010, Australia.

J. E. Ruhl, B. R. Saliwanchik, and J. A. Shariff are with the Physics Department, Case Western Reserve University, Cleveland, OH 44106 USA.

G. Smecher is with the Three-Speed Logic, Inc., Vancouver, BC V6A 2J8, Canada.

A. A. Stark is with the Harvard-Smithsonian Center for Astrophysics, Cambridge, MA 02138 USA.

K. Story is with the Kavli Institute for Particle Astrophysics and Cosmology, and also with the Department of Physics, Stanford University, Stanford, CA 94305 USA.

K. Vanderlinde is with the Dunlap Institute for Astronomy and Astrophysics, and also with the Department of Astronomy and Astrophysics, University of Toronto, Toronto, ON M5S 3H4, Canada.

J. D. Vieira is with the Astronomy Department, and also with the Department of Physics,, University of Illinois, Urbana, IL 61801 USA.

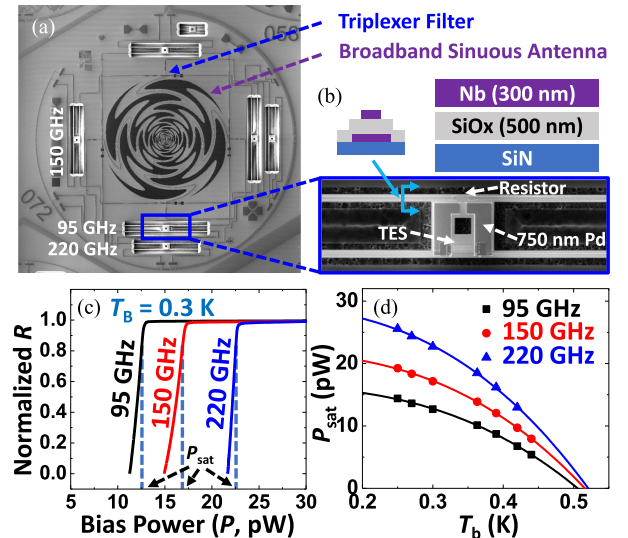


Fig. 1. (a) SEM image of a pixel. (b) Detail around the island. All TESs are with a dimension of $15 \mu\text{m} \times 80 \mu\text{m}$ in this paper. The sketch shows the cross-section of a leg. The LSN layer was $1 \mu\text{m}$ before processing and it will be thinner in the final devices. (c) TES resistance as a function of the P_{tot} for different bands. (d) P_{sat} as a function of the bath temperature T_b : measurements (points) and predicted trend (solid curves).

in our detector arrays, and the LSN contributes approximately 30% of the total thermal conductance of the whole leg. These results provide important information for improving the overall sensitivity of the detector array.

The paper is organized as follows: Section II gives an overview of the detector fabrication and characterization, Section III describes the TES performance with different substrate surfaces and film structures, and Section IV describes an investigation of the thermal link properties.

II. DETECTOR DESIGN AND CHARACTERIZATION

A. Design

The SPT-3G camera has 10 hexagonal detector arrays, each containing 269 pixels. Fig. 1(a) shows the details of a pixel. The millimeter-wavelength signal is received by a self-complementary, log-periodic, broadband, sinuous antenna [10], [11]. Three-pole, quasi-lumped-element filters [12]–[14] split the signal into three bands centered around 95, 150 and 220 GHz. Superconducting, 10Ω , Nb, microstrip, transmission lines [15] distribute the balanced signal for each band to the appropriate detector island, where it is absorbed by a 20Ω Ti/Au load resistor. The change in temperature of the island is then sensed by a Ti/Au TES. A 750 nm thick layer of Pd is deposited on the island to increase the heat capacity and stabilize the detector [16]. The thermal link of the TES detector is a set of four LSN legs that support the island. The leg length and width is designed to provide a detector saturation power (P_{sat}) roughly 2.5 times the expected loading (P_{load}) from the sky, telescope, and cold optics. Detailed information about the island and the leg are shown in Fig. 1(b). Fabrication details for the SPT-3G detector arrays are given in Posada *et al.* [17], [18].

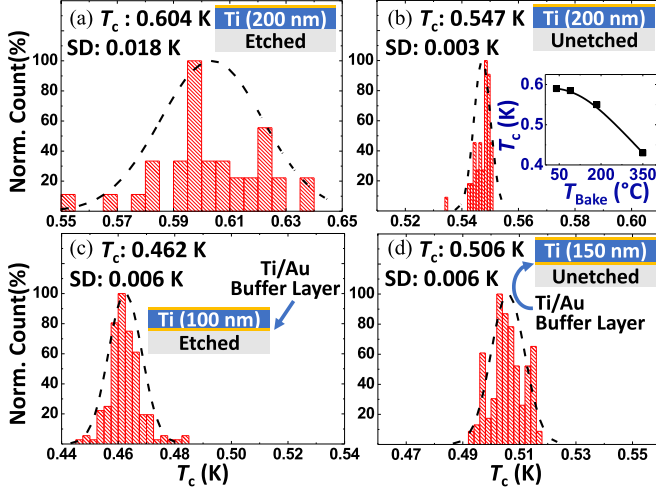


Fig. 2. T_c distribution for TESs (a) on etched SiOx, (b) on unetched SiOx, (c) with Ti(5 nm)/Au(5 nm) buffer layer on etched SiOx, (d) with Ti(5 nm)/Au(5 nm) buffer layer on unetched SiOx. TES T_c change as a function of the baking temperature (T_{Bake}) is shown in the insert of (b). The average T_c and standard deviation (SD) are labeled in each figure. All TESs are covered by 20 nm Au in this paper.

B. Characterization

A digital, frequency-domain, multiplexing scheme [19] has been developed to read out groups of 64 detectors using a single pair of wires [20], making it possible to quickly evaluate the performance of large numbers of detectors.

For this work, the detector performance was investigated using measurements of the resistance, (R), versus bias power P for different bath (i.e., wafer or wafer holder) temperatures (T_b) as shown in Fig. 1(c). $P_{\text{sat}}(T_b)$ is indicated by the dashed lines in Fig. 1(c). Values of $P_{\text{sat}}(T_b)$ from Fig. 1(c) can be plotted, as in Fig. 1(d), and fitted to [21]–[23]:

$$P_{\text{sat}} = K \times (T_c^n - T_b^n) \quad (1)$$

where the constant $K = NkA/l$, N is the number of legs, A is the leg cross section, l is the leg length, k is the thermal conductivity of the leg material, and, n is the index for thermal conductivity. The fit yields values of the parameters and the thermal conduction ratio $G(T_c) = dP_{\text{sat}}/dT = nKT_c^{n-1}$. Since the phonon noise equivalent power (NEP) [24] is directly related to G and T_c , it is important to keep P_{sat} within a reasonable range.

Currently in SPT-3G project, the target T_c is 510 mK and the target P_{sat} is 10.6 pW, 16.0 pW and 21.0 pW for 95 GHz, 150 GHz and 220 GHz bands, respectively. These values are equal to twice the expected optical loading during normal operation, assuming an overall optical efficiency of 85%. They may be varied depending on the measured optical efficiency.

III. TES PERFORMANCE

In some SPT-3G arrays, the TESs are fabricated on an etched SiOx surface [17], while in others, the TESs are fabricated on an unetched surface [18]. The unetched surface gives much lower scatter in T_c , as shown in Figs. 2(a) and (b). It is possible that residual by-products and increased roughness, due to etching SiOx during fabrication of the Nb microstrip, may

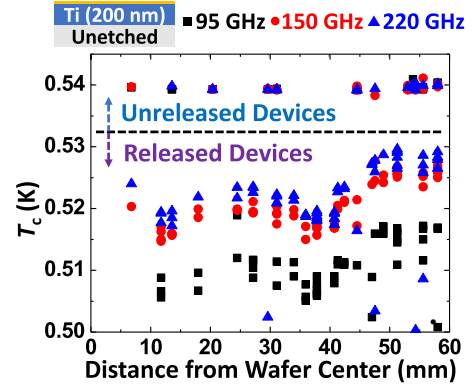


Fig. 3. TES T_c as a function of the distance from the wafer center for unreleased detectors (top panel) and released detectors (bottom panel, the detector legs and islands are released from the Si wafer). Every 4th row of pixels on this wafer was left unreleased.

cause the large scatter shown in Fig. 2(a). The TESs on etched SiOx have slightly higher T_c than those on unetched SiOx, due to the fact that the latter are prepared at a much earlier stage, so they encounter more fabrication processing. Heating during processing reduces the TES T_c , as shown in the inset in Fig. 2(b).

We have also investigated adding a Ti(5 nm)/Au(5 nm) buffer layer under the TES to isolate the TES from the substrate. The buffer layer results in lower T_c , and lower scatter in T_c , for both etched and unetched SiOx, as shown in Figs. 2(c) and 2(d). In Figs. 2(c) and 2(d) the combination of the buffer layer and thinner Ti (100 nm for Fig. 2(c) and 150 nm for Fig. 2(d)) gives T_c in the range 450–510 mK, cf. 550–600 mK for the thicker TESs without buffer layer in Figs. 2(a) and 2(b).

The small scatter in T_c in Fig. 2(b) may be due to a smaller number of detectors for this measurement (~ 50 for Figs. 2(a) and 2(b), cf. ~ 150 for Figs. 2(c) and 2(d)) or variations in the etch that releases the detector legs and islands from the Si wafer (releasing process). Releasing decreases T_c , probably due to heating of the TESs, and increases the scatter in T_c , as shown in Fig. 3. Fig. 3 also shows a larger variation in T_c with radius and band. Since these effects are only observed in released devices, they could be due to (i) excess, band-dependent, optical loading in the measurement setup, or (ii) heating of the TESs during release (or during final oxygen plasma cleaning to remove photoresist), which may depend on band because detectors for different bands have different leg lengths with different thermal conductivities. Further investigations are still on going. One plan to further reduce the T_c scattering is to optimize the island releasing process to achieve a more uniform releasing across the wafer.

IV. PROPERTIES OF THE THERMAL LINK

We have fabricated two test wafers to investigate the effects of different film structures (Fig. 4(a-c)) and different leg widths and lengths (Fig. 4(d-f)), respectively. Fig. 4(a-c) shows results for detectors with (a) legs that have only LSN and Nb leads for reading out the TESs (black squares), (b) legs with LSN, the 500 nm SiOx dielectric for microstrip transmission line and Nb

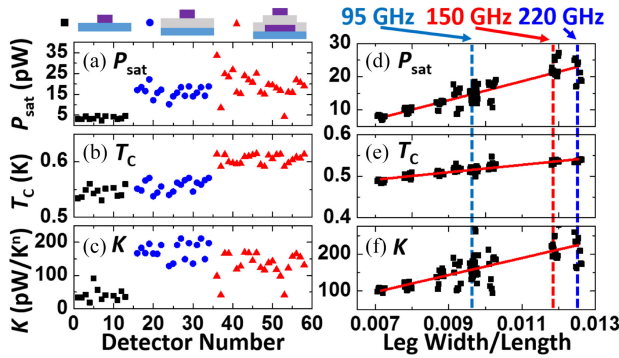


Fig. 4. Detector parameters for different leg film configurations (a)–(c), and different leg widths and lengths (d)–(f). For these measurements, $T_b = 300$ mK. The detectors in (a)–(c) are dark (no load resistors on the islands).

leads (blue dots), and (c) legs that have LSN and a complete microstrip transmission line (red triangles). K for detectors with only LSN and Nb leads is 3 times smaller than for the other configurations, and the microstrip Nb ground layer has little effect on K , as expected for a superconductor, so the thermal conductivity of the legs must be dominated by the SiOx layer, with the LSN contributing only $\sim 30\%$.

Since the SiOx layer thickness is constrained by the filter design, and the LSN layer on the legs must be thick enough to support the island without breaking, changes to the leg thermal conductivity may require a different leg width or length. Fig. 4(d-f) shows measurements of detectors from a wafer on which $\frac{1}{4}$ of the detectors have 23% longer legs and $\frac{1}{4}$ have 26% narrower legs. A complete discussion of these results is outside the scope of this paper (more discussion about thermal link can be found in [25], [26]) and the origin of the scattering of K in our results is still under investigation. However, it is clear that K is approximately proportional to the ratio of leg width to leg length (W/L), as expected for long legs. The scaling of K with W/L also suggests that the islands and legs are fully released, i.e., the legs are the only thermal link between island and the substrate. A touch between island and the substrate would give a higher K for long and narrow legs than the observed results.

V. CONCLUSION

In summary, we have shown that adding a thin Ti(5 nm)/Au(5 nm) buffer layer under a Ti/Au TES significantly decreases the scatter in transition temperature. We have demonstrated that the thermal conductivity of the legs that support the SPT-3G detector islands is dominated by the SiOx microstrip dielectric layer, and that the thermal conductivity scales as expected with leg width/length. These results will be used to optimize the performance of the TES detector arrays for the new SPT-3G camera.

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