Thermal Regulation and Balancing in Modular Multilevel Converters

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Contents

Abstract

Modular multilevel converters (MMCs) are envisaged as the key power electronic converter topology to enable a multi-terminal pan-European high voltage direct current (HVDC) Supergrid for the interconnection of offshore wind farms and exchange of energy between different countries.

A key feature of MMCs in the large number of semiconductor devices employed in each converter station, distributed over a stack of series-connected sub-modules (SMs). These semiconductors possess strict thermal limits, which can constrain the operating range on the converter by limiting its capability of providing enhanced functionalities to the AC grid such as short-term power overloads. Furthermore, due to different loading conditions and ageing, significant temperature differences can exist between SMs which can lead to a very different lifetime expectancies for the semiconductor modules.

This thesis proposes active thermal control methodologies to act of two distinct converter levels. Firstly, two novel dynamic rating strategies are proposed to define the converter current injection limit as a response to the maximum semiconductor temperature feedback. This enables the exploitation of the semiconductors thermal headroom to provide short-term power overloads, which can be used for the improvement of the frequency support of a power-distressed AC grid. Secondly, a SM-level temperature regulation and balancing algorithm is proposed, aiming at the equalisation of the maximum semiconductor die temperature in all the SMs of an MMC arm.

The proposed methods are validated in a detailed and combined electro-thermal simulation model with 3 and 10 SMs per arm developed in MATLAB®/Simulink® using PLECS® Blockset. An experimental platform has been designed and utilised to verify the effectiveness of the dynamic rating strategies and the SM temperature regulation and balancing strategy.

Acknowledgements

In the first place, I would like to thank my supervisors, Dr. Daniel James Rogers and Professor Jun Liang, for their guidance, support, trust and patience!

I would also like to thank European Union for funding MEDOW Project, a Marie Curie Initial Training Network, through the Seventh Framework Programme. This project enable me to expand the scope of my research by undertaking two four months-long secondments at China Electric Power Research Institute (CEPRI) in Beijing, China and at the CITCEA Group of the Technical University of Catalonia (UPC BarcelonaTech) in Barcelona, Spain, and an eight months-long secondment at the Energy and Power Group of the University of Oxford in Oxford, UK . A work of appreciation to all the colleagues I have worked with and all the friends I have made during these (ad)ventures.

Last but not least, I want to thank my girlfriend, Jingli Guo, and my family, mother Alice, father Manuel and brother Manuel António, for their unconditional support before and during my move to the UK to work as an Early State Researcher in the MEDOW Project and as a PhD student at Cardiff University and also for the support during this journey. This work is dedicated to them.

Abbreviations

AAC	**A**lternate **A**rm **C**onverter
AC	**A**lternating **C**urrent
CTL	**C**ascaded **T**wo-**L**evel
CVB	**C**apacitor **V**oltage **B**alancing
DC	**D**irect **C**urrent
FPGA	**F**ield-**P**rogrammable **G**ate **A**rray
HVDC	**H**igh **V**oltage **D**irect **C**urrent
EtherCAT	Ethernet for **C**ontrol **A**utomation **T**echnology
IGBT	**I**nsulated **G**ate **B**ipolar **T**ransistor
LCC	**L**ine **C**ommutated **C**onverter
MMC	**M**odular **M**ultilevel **C**onverter
MTDC	**M**ulti **T**erminal High Voltage **D**irect **C**urrent
OWF	**O**ffshore **W**ind **F**arm
PI	**P**roportional-**I**ntegral (controller)
PLL	**P**hase-**L**ocked **L**oop
PWM	**P**ulse-**W**idth **M**odulation
SM	**S**ub-**M**odule
SOA	**S**afe **O**perating **A**rea
SOH	**S**tate **O**f **H**ealth
TOEn	**T**ransient **O**verload **En**ergy
TOE	**T**ransient **O**perational **E**nvelope
TSO	**T**ransmission **S**ystem **O**perator
VHDL	**V**HSIC (Very High Speed Integrated Circuit) **H**ardware **D**escription **L**anguage
VSC	**V**oltage **S**ource **C**onverter

Symbols

C	Capacitance	F
C_{th}	Thermal Capacitance	J/°C
D	Load Damping Constant	W/Hz
f	Electrical Frequency	Hz
H_s	Inertia Constant	s
I	Current	A
L	Inductance	H
P	Active Power	W
R_{th}	Thermal Resistance	°C/W
Q	Reactive Power	var
R	Permanent Droop	Hz/W
T	Temperature	°C
V	Voltage	V
Z_{th}	Thermal Impedance	°C/W
ω	angular frequency	rad·s^{-1}

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Chapter 1

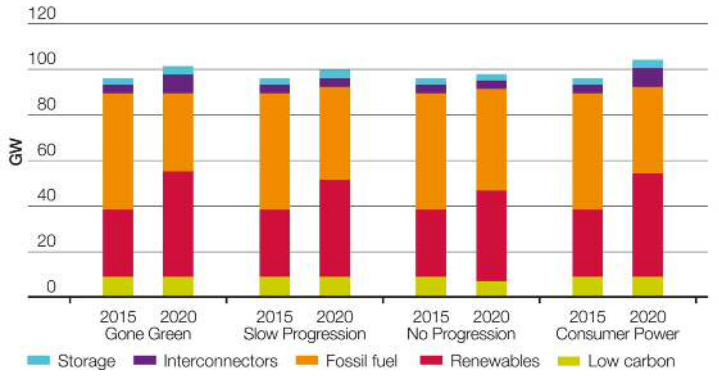
Introduction

1.1 Background

The consequences of global warming and the need for CO_2 emissions reduction lead the push to a low carbon power system and the shift from fossil fuels towards renewable energy based generation [14–16]. Ambitious targets to the decarbonisation of the electricity sector have been set by the European Union (EU) [17]. In the UK these policies mandate that 15 % of the total generation must come from renewable energy resources by 2020 [18], aiming at achieving a greenhouse gas emissions reduction of 80 % by 2050. This has lead to an increasing market penetration of renewable energy resources such as wind and solar [19–21].

Achieving these targets requires a significant shift in the paradigm by which power generation and transmission presently occurs. For all the different scenarios analysed by National Grid, the UK Transmission System Operator (TSO) for Gas and Electricity, by which these targets can be met, only the 'Gone Green' scenario embodies a balanced and realistic strategy. This scenario combines the power generation, transport and heat. It can be observed in Figure 1.1 (a) that between 2015 and 2020 the installation of renewable generation is the main contributor to the reduction in the fossil fuel in the power generation mix, as aged and inefficient coal based power plants are decommissioned [22].

Much of the new generation is led by renewables, with a strong deployment of offshore wind [1], as presented in Figure 1.1 (b), with both onshore and offshore wind being



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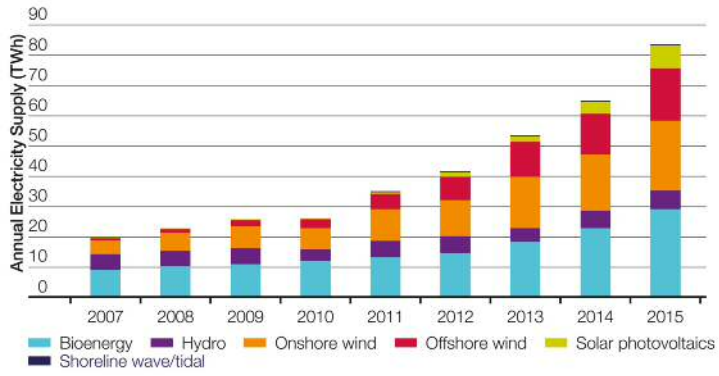


(B)

FIGURE 1.1: Electricity generation in the UK: (a) - Amount installed by type 2015-2020 and (b) - Renewable generation history [1].

regarded as the key to the EU's long term decarbonisation, energy security and competitiveness objectives [23]. In the UK, the offshore installed capacity is expected to reach 17 GW by 2020, with the Crown Estate having already issued three rounds of offshore wind farm licenses, which will potentially lead to a total capacity of over 40 GW. It is expected that over £15 billion will be spent to connect the offshore projects of the three rounds [24].

During 2016 13.9 GW of wind power were installed across Europe, from which 12.5 GW were installed in the EU. Of the capacity installed in the EU, 10.923 MW was onshore, which represents a 11 % increased compared to 2015, and 1.567 MW offshore [2]. In total, 24.5 GW of new gross power generation capacity were installed in the EU in 2016, with wind power being the dominant energy technology (51 %) of all new installations. The market shares of the total installed capacity for the different EU countries are shown in Figure 1.2, where it can be observed that the UK has the 4^{th} largest share in the total installed capacity, with 736 MW, showcasing its commitment to a future low carbon power system.

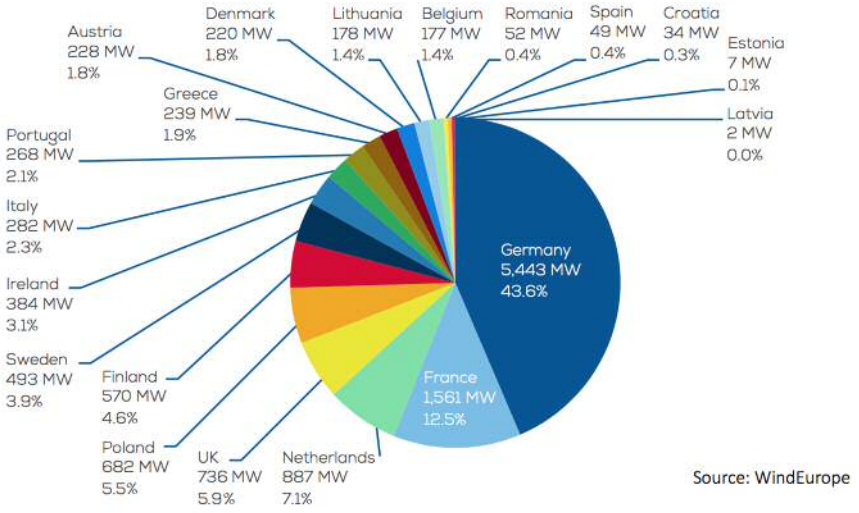


FIGURE 1.2: Market shares for new wind energy capacity installed in Europe during 2016 [2].

Overall, the wind sector represents over 300,000 jobs and generates €72 billion in annual turnover in Europe, and is expected to contribute to ambitious post-2020 renewables policies, enabling the generation of net benefits for the EU economy of €13 billion, boosting the job count to 688,000 [23].

1.2 Drivers of HVDC Transmission Systems

Higher and more constant wind speeds away from shore result in a more efficient energy generation at a lower cost. Conventional High Voltage Alternating Current (HVAC) transmission cables generate excessive charging currents that limit the useful capacity for current flow and require compensation by shunt reactors. In contrast, High Voltage Direct Current (HVDC) transmission does not have oscillatory charging currents and requires a smaller number of cables. Although a conversion step is introduced in the connection to shore, additional flexibility is introduced for power and voltage control and this option is expected to be the default solution for long distance offshore transmission.

HVDC transmission systems employ either Line Commutated Converters (LCCs) or Voltage Source Converters (VSCs), with the former being the preferred solution for long distance bulk power transmission, mainly due to being a mature technology with low losses and capable of achieving higher ratings [25]. These converters, however, possess several disadvantages such as substantial reactive power and filtering requirements, large

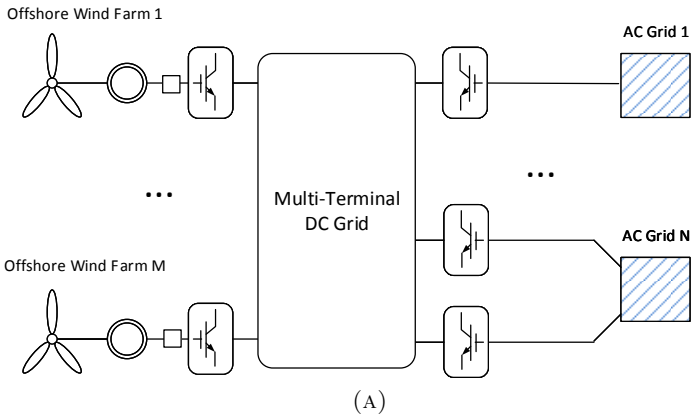
footprint, sensitivity to commutation failures and power flow reversal by reversing the DC voltage polarity [26]. This leads to the preference of VSC based HVDC systems for the connection of offshore wind farms. VSCs are immune to commutation failures and possess minimal filtering requirements, specially for recent Modular Multilevel Converter (MMC) topologies [27], which results in a small offshore platform footprint. Besides independent active and reactive power control [28], the power flow can be reversed by changing the current direction, which makes VSCs the preferred solution for recent long distance offshore wind generation, e.g. Borwin and Sylwin projects [29].

Present VSC-HVDC projects in Europe for the connection of offshore wind farms are essentially Point-to-Point (P2P) located in the North Sea, and are still affected by the wind intermittency. Given the geographical dispersion of dominant renewable energy sources such as wind and hydro in the north and solar power in the south, the interconnection between several countries can overcome the intermittency of any single resource. The construction of a pan-European Multi-Terminal HVDC (MTDC) transmission network widely known as a Supergrid [30], as demonstrated in Figure 1.3 (a), has received widespread attention as an effective solution for the integration of renewable energy resources.

Several studies [31, 32] have demonstrated that compared to several P2P systems, an MTDC grid provides an increase in the inter-country connected capacity and operational reliability while having a reduced number of converter stations. It also results in a lower cost, lower conversion losses and shorter cable lengths. Although there is some accummulated experience of the operation and control of P2P connections, the implementation of an MTDC grid is, however, not starightforward. Despite the vision to create a North Sea hub in Europe connecting multiple countries, as shown in Figure 1.3 (b), presently only two MTDC projects in the world have been commissioned: the 3-terminal Nan'ao grid [33] and the 5-terminal Zhoushan grid [34], both located in China.

1.3 Technical Challenges

Significant efforts are needed to overcome the challenges towards the establishment of HVDC grids. Although there are some operational obstacles to be addressed, such as DC



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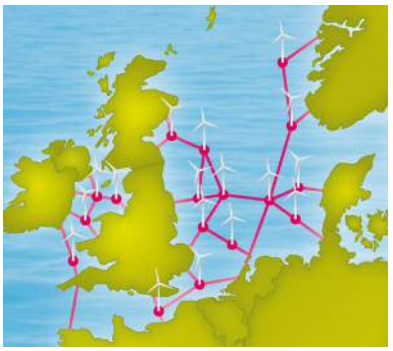


(B)

FIGURE 1.3: MTDC supergrid for offshore wind: (a) - General structure and (b) - North Sea vision [3].

grid voltage standardisation, technical hurdles are critical and have received widespread research efforts.

Ongoing research on HVDC grids aims to overcome key challenges including the decrease in the system inertia. Functionalities such as frequency support from other grids and offshore wind farms [35] are being increasingly discussed as wind energy can provide grid support services, contributing to the secure and cost-effective management of the power system [23]. These features, however, may present a challenge if power electronic converters operate close to their full transmission capacity. The provision of such functionality may result in a limited benefit given the limited rating of the semicondutor switches, as well as the need to assure limited ratings to enable temperature management strategies.

Similarly to AC Grid Code requirements, the power electronic converters of HVDC grids may be requested to provide additional functionalities such as power overload or temporary emergency rating conditions [36]. These operating conditions have significant implications in the design of the converters and in the limited rating of the semiconductor

switches. Furthermore, varying operating conditions for the converters result in more demanding and varying operations conditions for the semiconductor devices, with severe influence on their lifetime, power conversion capability and converter reliability. In is therefore of utmost importance to analyse and understand the implications of switching device-level thermal stresses and its influence on the system-level performance of power electronic converters. This will ensure the converters can operate safely in demanding conditions while being able to provide additional and critical functionalities to system operators.

1.4 Research Objectives

The aim of this thesis is to investigate temperature management strategies of semiconductor devices to enable an enhanced operation of Modular Multilevel Converters (MMCs) in HVDC applications. The detailed research objectives and contributions of this thesis are outlined as:

- To **develop active thermal control strategies suitable for MMCs**. Two dynamic rating strategies using estimated junction temperature feedback for current limit regulation were developed.
- To **investigate and assess the short-term overload capability of semiconductors and its effect on the enhancement of the current injection capability of MMCs**. The transient overload capability of semiconductor devices was quantified through a new figure of merit and explored during the operation of an MMC when subjected to a cooling system failure and current overload commands. The effect on the frequency support of a power distressed grid was also investigated.
- To **design a control strategy to manage semiconductor temperature differences between Sub-Modules in an MMC**. A per arm Sub-Module temperature regulation and balancing method was proposed, where temperature equalisation is achieved through the control of capacitor voltages.

- To **develop an experimental MMC test platform** for further development and validation of the proposed dynamic rating and Sub-Module temperature regulation and balancing strategies. Experimental results were compared to the results obtained in simulation studies and show good agreement.

1.5 Thesis Structure

This thesis consists of six chapters.

- **Chapter 2**

  Presents a literature review of AC-DC converter topologies for HVDC applications, with a particular focus on the MMC. The Electrical model of an MMC, as well as different configurations of the SMs are presented and the different control loops necessary for the operation of this converter are detailed and analysed. The operational requirements and challenges of semiconductors temperature control and the management of SMs redundancy and state of health monitoring in MMCs are introduced and discussed.

- **Chapter 3**

  Presents an overview of the electro-thermal dynamics of semiconductor devices and details a loss calculation process particularly suitable for MMCs. A literature review on different junction temperature estimation methods is presented, including an analysis of the requirements of each method, as well as the challenges of their practical implementation.

- **Chapter 4**

  Presents two dynamic rating strategies to extend the power transmission capability of an MMC, while keeping the temperature of semiconductor switches within safe limits. The chapter starts with the review of the limitations of conventional thermal control strategies in regulating semiconductors temperature in MMCs, followed by the proposal of an additional control loop that enables the current limit in the converter control to be sensitive to semiconductors temperature. A choice of suitable control parameters for the rating strategies is made through an

eigenvalue analysis to avoid temperature overshoots; an analytical method is proposed to quantify the effect of different parameter values on the transient overload capability of the semiconductors. The proposed dynamic rating strategies and the influence of their parameter values are explored for two scenarios: cooling system failure and converter overload. The ability of the MMC to operate in an overload mode to improve the inertial response of a power distress grid is investigated. Studies in this chapter also explore the heat sink design as a control variable to enable an extend the duration of the semiconductors transient current overload, as well as its effect on the improvement of the frequency support.

- **Chapter 5**

  Describes a SM capacitor voltage control strategy to regulate and balance the maximum die temperature between the SMs of an arm. This strategy complements the dynamic rating strategies proposed in Chapter 4, which only respond to the maximum calculated temperature in the semiconductors, irrespective of being a generalised or localised temperature increase. The effectiveness of the proposed method is validated via case studies with different amplitudes for the thermal disturbances and its dependency on the number of SMs available to participate in the regulation process is investigated.

- **Chapter 6**

  Describes a reduced-order setup capable of replicating the electrical and thermal operating conditions of the SMs in a compete MMC. The operation and control of this test setup are discussed and its implementation on an experimental test rig is presented in detail. The effectiveness of the dynamic rating strategies presented in Chapter 4 and of the SM temperature regulation and balancing method proposed in Chapter 5 are validated in the test rig. Comparisons are drawn between the experimental results and the results obtained from simulation using MATLAB®/Simulink® and the PLECS® Blockset toolbox.

- **Chapter 7**

  Summarises the conclusions from the work presented in the thesis and discusses some recommendations for future research.

1.6 Publications by the Author

The following publications were written based on work done during the Ph.D. study period.

1.6.1 Journal Publications

- **Gonçalves, J.**, Rogers, D. J., and Liang, J., "Sub-Module Temperature Regulation and Balancing in Modular Multilevel Converters". IEEE Transactions on Industrial Electronics (accepted)
- Guo, J., Wang, X., Liang, J., Pang, H. and **Gonçalves, J.**, "Reliability Modelling and Evaluation of MMCs under Different Redundancy Schemes". IEEE Transactions on Power Delivery (in press). DOI: 10.1109/TPWRD.2017.2715664

1.6.2 Conference Publications

- **Goncalves, J.**, Rogers, D. J., and Liang, J., "Extension of Power Transmission Capacity in MMC-based HVDC Systems through Dynamic Temperature-Dependent Current Limits". 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), Geneva, Switzerland, 2015

1.6.3 Research Workshops

- **Goncalves, J.**, Rogers, D. J., and Liang, J., "Operation of MMCs with Dynamic Temperature-Dependent Current Limits", 3^{rd} Manchester Electrical Energy and Power Systems (MEEPS) workshop, Manchester, UK, 2014
- **Goncalves, J.**, Rogers, D. J., and Liang, J., "Dynamic Current Limits to Manage IGBT Temperature in Modular Multilevel Converters for HVDC Applications", EPSRC-Power Electronics UK meeting, Nottingham, UK, 2015
- **Goncalves, J.**, Rogers, D. J., and Liang, J., "Enhanced Control and Operation of Modular Multilevel Converters", special MEDOW session at IEEE International Energy Conference (ENERGYCON) 2016, Leuven, Belgium, 2016

- **Goncalves, J.**, Rogers, D. J., and Liang, J., "A Reduced-Order Setup for the Investigation of Electrical and Thermal Effects in Modular Multilevel Converter", 7^{th} HVDC Colloquium, Porto, Portugal, 2016

Other presentations of the research outcomes were made to research peers, industry professionals (Alstom Grid - currently GE Grid Solutions, National Grid, Scottish Power Energy Networks and Smart Grid Research Institute (SGRI) - currently Global Energy Interconnection Research Institute (GEIRI)) and during the update meetings of the MEDOW project.

MEDOW (Multi-tErminal Dc grid for Offshore Wind) is a Marie Curie Initial Training Network (ITN) consisting of 11 partners (5 universities and 6 industrial organisations) with collective expertise on the manufacturing, design, operation, and control of multi-terminal DC grids and has received funding from the Seventh Framework Programme of the European Union (http://sites.cardiff.ac.uk/medow/).

Chapter 2

Power Electronic Converters for HVDC Grids

2.1 Introduction

HVDC transmission is a field where significant technological progress has been made since the first project was commissioned in 1954 [37]. This chapter reviews the literature on High Voltage Power Electronic Converters for DC Grids, focusing on the current state of the art MMC topology, including its operation and control. The main challenges and operational requirements of these converters are also presented and discussed.

2.2 AC-DC Conversion

2.2.1 Line Commutated Converters

LCCs are a cost-effective technology for bulk DC power transmission. Thyristor valves are employed to perform the energy conversion between the AC and DC sides, typically in a 12- or 24-pulse arrangement in which 6-pulse bridges are connected in series on the DC side, as illustrated in Figure 2.1. The thyristors firing pulses are determined by the converter control.

The transformers have a star-star-delta three-winding configuration to eliminate some of the common harmonics generated by the 6-pulse bridges and ease the filtering requirements on the AC side [4, 26]. Since the current flow is unidirectional due to the physical limit of the thyristors, the power flow reversal can only occur by reversing the DC voltage polarity [25], which limits the application of LCCs in multi-terminal or meshed configurations.

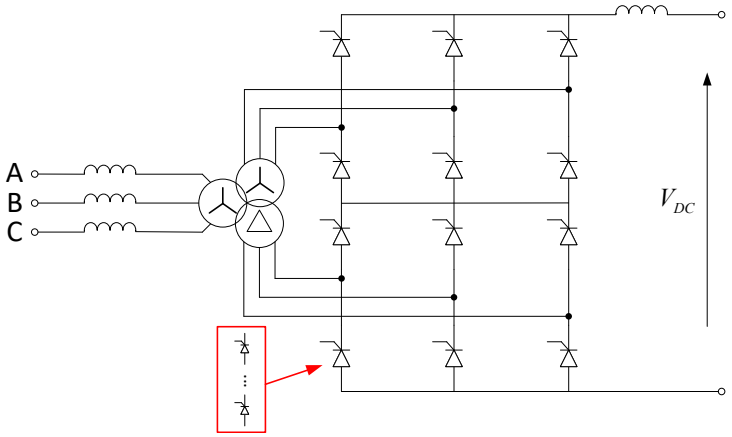
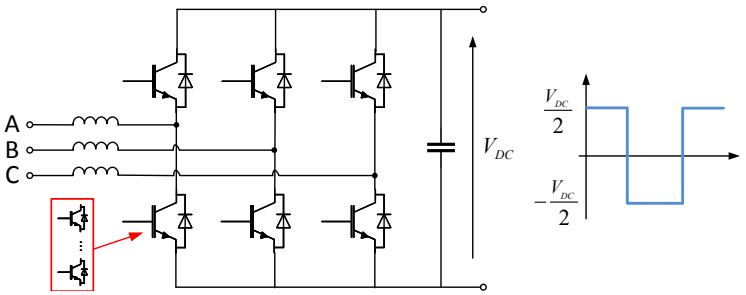


FIGURE 2.1: Typical configuration of a 12-pulse LCC [4].

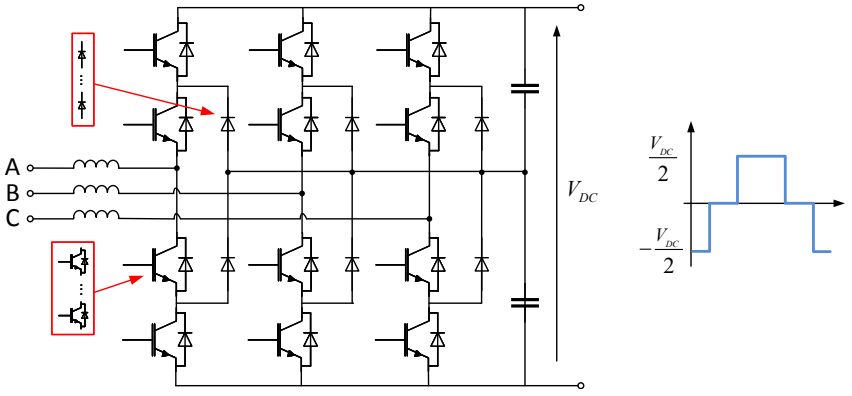
2.2.2 2- and 3-Level Voltage Source Converters

Several VSCs have been proposed and thoroughly investigated, particularly the 2-level and 3-level topologies. These designations correspond to the number of levels of the produced output voltage at the converter's AC terminals, as presented in Figure 2.2. These topologies require large DC-side capacitors to provide intermediary energy storage from the conversion between AC and DC sides, and to aid the regulation of the DC voltage [38].

Both 2-level and 3-level VSCs typically employ Insulated-Gate Bipolar Transistors (IGBTs) with anti-parallel diodes, connected in series to match the rated DC voltage. The IGBTs are fully controllable, i.e. they can be turned ON and OFF when desired, and are switched simultaneously. The switching actions depend on the gate signals, typically generated by the comparison between a reference sinusoidal waveform at the desired grid frequency and a high frequency triangular carrier. The carrier waveform typically has a frequency in the range $1 - 2\,\text{kHz}$, which originates a Pulse-Width Modulated (PWM) signal [28].



(a) - 2-level converter (left) and output voltage waveform (right)



(b) - 3-level converter (left) and output voltage waveform (right)

FIGURE 2.2: Reduced-level VSC topologies.

The output voltage waveforms have a rich harmonic content, as shown on the right of Figure 2.2. Due to the small resemblance with a sinusoidal voltage waveform, extensive filtering is necessary to extract the sinusoidal fundamental frequency component [25], although in a much smaller extension than in an LCC converter station. Large phase reactors are also employed for the filtering of line currents.

2.2.3 Modular Multilevel Converters

Comparing with the 2-level VSC, both the size of voltage steps and the related voltage gradients can be reduced or minimized if the AC voltage generated by the converter can be selected in smaller increments than two (or even three) levels only. The finer this gradation, the smaller is the proportion of harmonics. Converters with that capability are called multi-level converters [38]. The switching frequency of individual semiconductor devices can also be reduced, effectively reducing converter losses.

In the past, different multi-level topologies such as diode clamped-based or converters with so called flying capacitors have been thoroughly discussed [39, 40]. The main

problem of these early multi-level topologies is related with the difficulty of keeping acceptable values for capacitor voltage drifts, as well as the necessity of having separate DC sources. Furthermore, the lack of modularity resulted in difficulties for design expansion and maintenance. This makes them unsuitable for HVDC transmission, particularly under unbalanced and transient conditions, but perfectly suited for energy storage applications [41].

Taking these limitations into account, together with the inconvenient of having a large DC-side capacitor feeding a DC fault, a new approach, the MMC, was proposed in [42]. This family of converters, whose general structure is depicted in Figure 2.3, is composed of two arms in each phase, with the midpoint of the two arms connected to the AC side through two identical arm inductors L. Each arm has a distributed energy storage in the form of series-connected SMs, which are inserted or bypassed according to a control scheme to generate both AC and DC voltages.

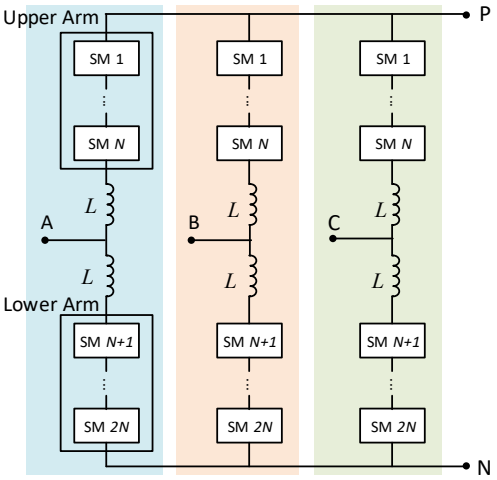


FIGURE 2.3: MMC topology.

Compared with 2- and 3-level converters, some of the main differences are [38, 42–47]:

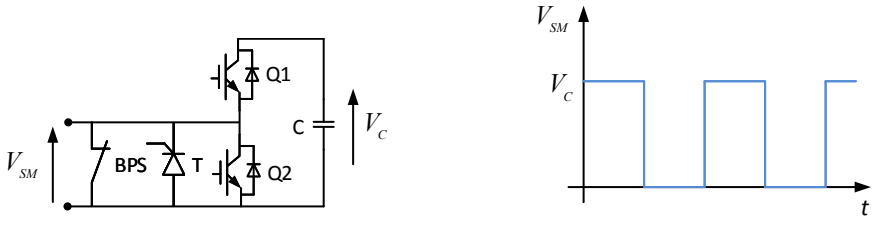
- Smaller voltage steps;
- Distributed energy storage;
- Absence of a large pole-to-pole DC side capacitor;
- No simultaneous commutation of series-connected IGBTs;
- Modular structure;

- Low Total Harmonic Distortion (THD) on the output voltage;
- Minimal or even unnecessary filtering requirements;
- Lower switching frequency;
- Lower losses.

MMCs are the current state of the art topology for VSC-based HVDC transmission systems due to the technical possibilities and advantages offered, and their operation and control will be discussed here. The modular structure allows additional flexibility since different configurations can be chosen for the SMs [43, 44]. Although several configurations have been proposed [48–52], only the Half-Bridge(HB) and Full Bridge (FB) SMs have found commercial application.

2.2.3.1 Half-Bridge MMC

The structure of the HB SM or cell is illustrated in Figure 2.4, where the switching is performed by two IGBTs (Q1 and Q2) with anti-parallel diodes. A high-speed bypass switch "BPS" is used to increase the reliability and safety of the MMC in case of a SM failure [53]. A protective thyristor "T" is also included, and used to protect the semiconductor devices and cables from high fault currents. This is especially important during DC side faults due to the current infeed from the AC side through the free-wheeling diodes. Since these devices possess a low surge current capability, the protective thyristor is fired during the fault, carrying most of the high fault current.



(A) Configuration (B) Voltage Output

FIGURE 2.4: HB SM.

According to the state of IGBTs Q1 and Q2, three different states define the operation of the SM [42, 46, 47]:

- Both IGBTs are switched OFF: this is the condition of every SMs' capacitors after charging and can be compared to a "blocked" condition as in the 2-level VSC. In the event of a serious failure, all SMs are placed in this state, which is not used during normal operation;
- IGBT Q1 is ON and IGBT Q2 is OFF: the SM output voltage corresponds to the capacitor voltage. Depending on the direction of flow, the current either flows through the diode in parallel with IGBT Q1 and charges the capacitor, or through IGBT Q1 and thereby discharges the capacitor;
- IGBT Q2 is ON and IGBT Q1 is OFF: the current either flows through IGBT Q2 or its respective anti-parallel diode, depending on the current direction, ensuring that zero voltage is applied to the terminals of the SM, and the capacitor voltage remains unchanged.

This SM configuration was used by Siemens [38, 46, 47] and ABB [54] HVDC technologies, although in different manners. Siemens followed the initial concept, where each SM is rated in the range of a few kilovolts. Therefore, for HVDC applications hundreds of HB SMs [33, 55, 56] are connected in each of the arms of the converter shown in Figure 2.3.

The main limitation of the SM rating is associated with the voltage rating of the IGBTs. Currently, 6.5 kV IGBT modules are already available, allowing a bigger rating for the SMs while decreasing the number of switching devices, and the subsequent cost of the converter. Based on this, ABB proposed the cascaded two-level converter (CTL) [54], illustrated in Figure 2.5. Conceptually, a CTL has a topology similar to that of a MMC [54]: it consists of several smaller two-level building blocks, also called cells, enabling the creation of a nearly sinusoidal output voltage. The reason for the use of a different name relies on the fact that typical press-pack IGBTs are connected in series in the SMs, thus extending the technology that was used in 2-level VSCs through cascaded connections, while allowing a higher rating for the SMs. As in an HB MMC, each phase leg of the converter is divided in two arms, connecting the positive and negative poles of the DC bus to the converter AC bus and each arm is composed by the cascaded connection of N 2-level cells.

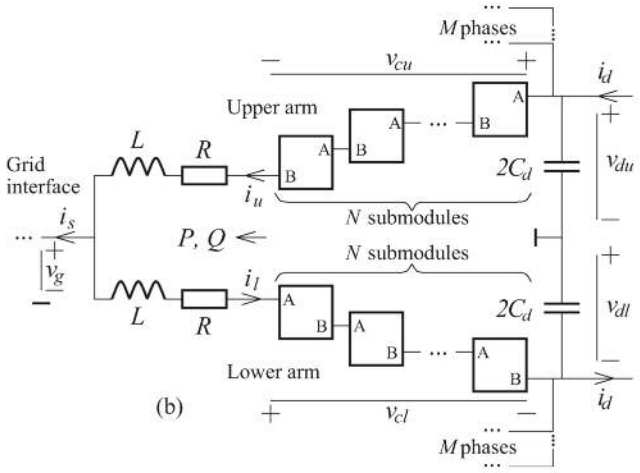
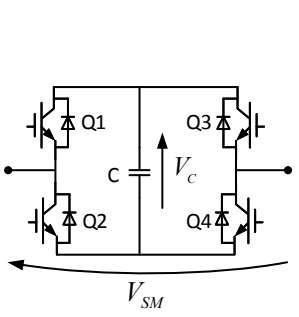


FIGURE 2.5: CTL structure [5].

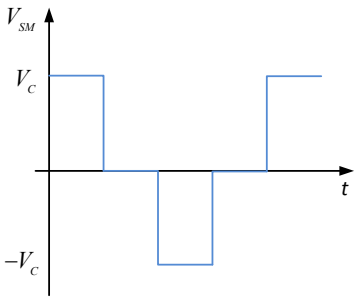
2.2.3.2 Full-Bridge MMC

The FB configuration of a SM, also called H-bridge cell, as well as its possible output voltages are depicted in Figure 2.6. The IGBTs can be controlled to produce a positive, zero, or negative output voltage, according to the control patterns. With Q1 and Q4 conducting, the output voltage V_{SM} is equal to the capacitor voltage V_c, and when Q2 and Q3 are ON, the output voltage equals $-V_c$. If Q1 and Q3 or Q2 and Q4 conduct, V_{SM} is zero.

In every moment two IGBTs are conducting while only one was in the ON state at each moment in the HB configuration. This implies that the conduction losses will be higher for FB-based MMC [57], which is the main reason for the preference of the HB configuration. However, and like the 2-level topology, HB SMs are not immune to DC-side faults like their FB counterparts; they are incapable of producing a negative voltage



(A) Configuration



(B) Voltage Output

FIGURE 2.6: FB SM .

to regulate the current in the converter and avoid infeed from the AC side. This leads to the conduction of the anti-parallel diodes connected to the IGBTs and creates an uncontrollable current path in the case of a DC short-circuit [45, 58]. Although losses are a significant operational issue, in some applications like in an MTDC grid, having DC side fault management capability may be an advantageous feature, especially when the DC grid connects different countries/Control Areas.

2.3 Operation and Control of Modular Multilevel Converters

The general control structure for a MMC has a high-level VSC (or vector) Control that addresses the dynamics between the converter and the external AC grid and an "MMC Control" comprising a set of dedicated control loops to regulate the inner dynamics in the MMC.

2.3.1 Model

The analysis of the MMC is performed for a single phase only for simplicity, represented in Figure 2.7, where HB SMs are considered. The analysis can be directly extended to the other phases.

Regarding the internal quantities of the MMC, one can define i_U and i_L as the upper and lower arm currents, respectively, and i_g and V_g as the current flowing into the AC grid and the phase-to-ground AC voltage on the point of connection of the converter. V_{arm}^U and V_{arm}^L are the upper and lower arm voltages, respectively, and V_{DC}^U and V_{DC}^L are the per pole DC voltages with respect to the fictitious DC side mid-point.

The current i_g can be defined as a function of the upper and lower arm current as:

$$i_g = i_U - i_L \tag{2.1}$$

Additionally, a parasitic circulating current i_C appears as a result of the unbalances between the sum of arm voltages and the DC voltage. This current flows between the converter arms, but not to the AC or DC sides, and can be expressed as:

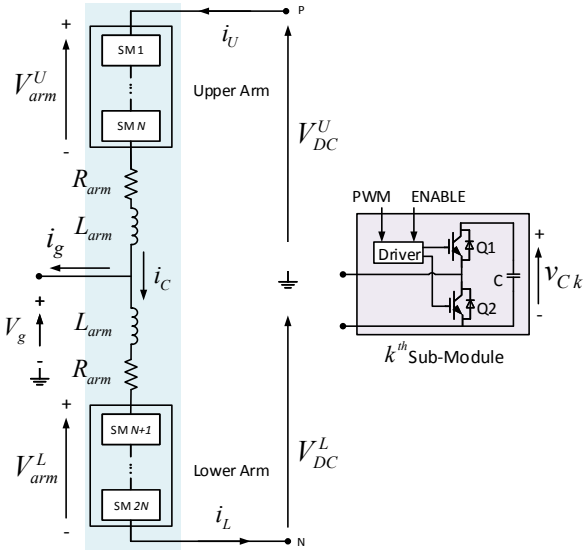


FIGURE 2.7: Single-phase MMC configuration with HB SMs.

$$i_C = \frac{i_U + i_L}{2} \tag{2.2}$$

Regarding the voltage drops on the converter arms, the following relationships apply to the upper and lower arms:

$$V_g = V^U_{DC} - V^U_{arm} - R_{arm} i_U - L_{arm} \frac{d i_U}{dt} \tag{2.3}$$

$$V_g = -V^L_{DC} + V^L_{arm} + R_{arm} i_L + L_{arm} \frac{d i_L}{dt} \tag{2.4}$$

Defining V^{Δ}_{DC} as the imbalanced DC voltage:

$$V^{\Delta}_{DC} = V^U_{DC} - V^L_{DC} \tag{2.5}$$

and adding (2.3) and (2.4) yields:

$$2V_g = V^{\Delta}_{DC} + V^L_{arm} - V^U_{arm} - R_{arm} \left(i_U - i_L\right) - L_{arm} \frac{d \left(i_U - i_L\right)}{dt} \tag{2.6}$$

Defining V_s as the output voltage driving i_g:

$$V_s = \frac{V_{DC}^{\Delta} + V_{arm}^{L} - V_{arm}^{U}}{2} \tag{2.7}$$

and recalling (2.1), (2.6) can be rearranged as:

$$V_g = V_s - \frac{R_{arm}}{2} i_g - \frac{L_{arm}}{2} \frac{d i_g}{dt} \tag{2.8}$$

This equation describes the MMC outer dynamics.

Defining V_{DC} as the total pole-to-pole DC voltage, i.e.:

$$V_{DC} = V_{DC}^{U} + V_{DC}^{L} \tag{2.9}$$

and subtracting (2.3) and (2.4) results in:

$$V_{DC} - V_{arm}^{U} - V_{arm}^{L} = R_{arm} \left(i_U + i_L \right) + L_{arm} \frac{d \left(i_U + i_L \right)}{dt} \tag{2.10}$$

If V_c is defined as the internal voltage driving i_C:

$$V_c = \frac{V_{DC} - V_{arm}^{U} - V_{arm}^{L}}{2} \tag{2.11}$$

and recalling (2.2), (2.10) can be rearranged as:

$$V_c = R_{arm} i_C - L_{arm} \frac{d i_C}{dt} \tag{2.12}$$

This equation describes the MMC inner dynamics.

Replacing (2.7) into (2.8) and expanding, yields:

$$V_g = \frac{V_{DC}^{\Delta} + V_{arm}^{L} - V_{arm}^{U}}{2} - \frac{R_{arm}}{2} i_g - \frac{L_{arm}}{2} \frac{d i_g}{dt} \tag{2.13}$$

The arm resistance represents the lumped resistive losses in the SMs connection and is very small, therefore the voltage drop across this element is normally neglected. The

voltage drop in the arm inductors is also very small, compared with the arm voltages, and therefore (2.13) can be simplified as:

$$V_g = \frac{V_{DC}^{\Delta} + V_{arm}^{L} - V_{arm}^{U}}{2} \tag{2.14}$$

The insertion of the SMs is controlled by the reference voltage waveform so that both V_{arm}^{U} and V_{arm}^{L} are regulated (and the SMs inserted) to sustain the intended DC bus voltage. If the arm voltages are regulated at V_{arm}^{C}, i.e.

$$V_{arm}^{L} + V_{arm}^{U} = V_{arm}^{C} \tag{2.15}$$

then (2.11) can be rewritten as:

$$V_c = \frac{V_{DC} - V_{arm}^{C}}{2} \tag{2.16}$$

The imbalance between the DC voltage V_{DC} and V_{arm}^{C} creates the internal voltage V_c in (2.12), which drives i_C and justifies the analysis presented above.

As it will presented shortly, the circulating current can be controlled to a constant value, irrespective of the number of phases. Hence, it is always possible to maintain a constant pole-to-pole DC voltage. For the single-phase case, MMCs are different from 2-level VSCs in this respect. For the latter, pulsations of twice the fundamental frequency appear on the dc bus. For an MMC, these pulsations instead appear as capacitor voltage ripple [5]. On the other hand, if the output currents do not sum up to zero, there will be a fundamental-frequency ripple on the DC bus voltage. For three-phase converters, this is in general not a problem as normally there is no zero-sequence current component. The removal of the DC bus midpoint grounding (cf. Figure 2.7) ensures $V_{DC}^{\Delta} = 0$ and creates a high zero-sequence impedance seen from the grid interface [5]. For single-phase converters on the other hand, this imbalance is unavoidable. It will be henceforth assumed that $V_{DC}^{\Delta} = 0$, which allows (2.14) to be further simplified as:

$$V_g = \frac{V_{arm}^{L} - V_{arm}^{U}}{2} \tag{2.17}$$

Expressing the output voltage as:

$$V_g = \frac{1}{2} m V_{arm}^C sin(\omega t) \tag{2.18}$$

where m is the modulation index and ω is the AC system fundamental frequency, allows (2.17) to be to rewritten as:

$$V_{arm}^L - V_{arm}^U = m V_{arm}^C sin(\omega t) \tag{2.19}$$

Combining (2.15) and (2.19), the voltages across the upper and lower arms are:

$$V_{arm}^U = \frac{1}{2} V_{arm}^C (1 - msin(\omega t)) \tag{2.20}$$

$$V_{arm}^L = \frac{1}{2} V_{arm}^C (1 + msin(\omega t)) \tag{2.21}$$

The peak AC voltage $\hat{V_g}$ can be expressed as:

$$\hat{V_g} = \frac{1}{2} V_{arm}^C \tag{2.22}$$

Assuming all the capacitor voltages have an average value of v_C (which is assured by a dedicated Capacitor Voltage Balancing (CVB) algorithm in the MMC Control), and that, in each moment, N sub-modules are inserted, the DC voltage that is produced by the modulation of N sub-modules is:

$$V_{DC} = N v_C \tag{2.23}$$

Given that N sub-modules are on the ON state in each moment,

$$\hat{V_g} = \frac{1}{2} N v_C = \frac{1}{2} V_{DC} \tag{2.24}$$

2.3.2 Vector Control

Vector Control has been widely accepted as a standard method for the current control of VSCs. The control is based on two cascaded control loops, as shown in Figure 2.8: a fast inner control loop that controls the current on the AC side of the VSC, with reference current values provided by controllers in the outer loop.

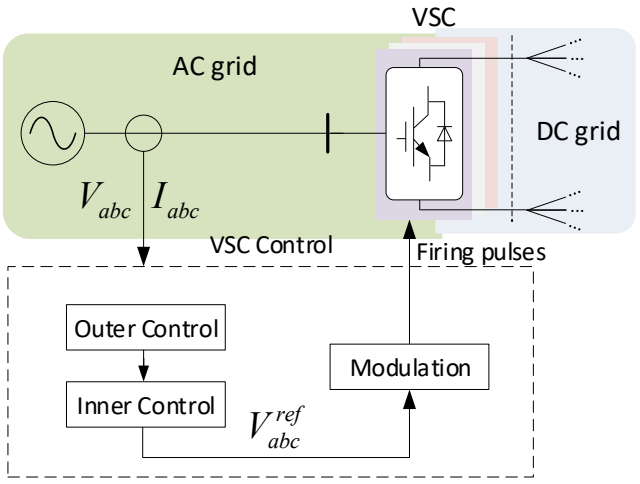


FIGURE 2.8: General control structure of a VSC.

The outer loop of a VSC comprises a set of control function whose choice depends on the application. Typical control variables are the active (P) and reactive (Q) powers and the AC (V_{AC}) and DC (V_{DC}) voltages. Two variables are chosen to be regulated at any moment and each of the variables is compared with its respective reference value and regulated through simple Proportional-Integral (PI) controllers. The output of these controllers generates either an active (I_d^{ref}) or reactive (I_q^{ref}) current component reference, sent to the inner control loop as presented in Figure 2.9.

In Vector Control, system quantities suffer an axis transformation, from the three-phase reference frame to a synchronous one, also known as Park's or d-q Reference Frame. One of the main advantages of this method is that three-phase voltage and current vectors are constant in steady-state, therefore the errors in the control loops can be eliminated through PI controllers, as in the outer loop, and shown in Figure 2.9. A Phase-Locked Loop (PLL) synchronises a local oscillator with one of the phases of the AC grid voltage in the connection point and provides the transformation angle θ for Park's transformation and inverse transformation.

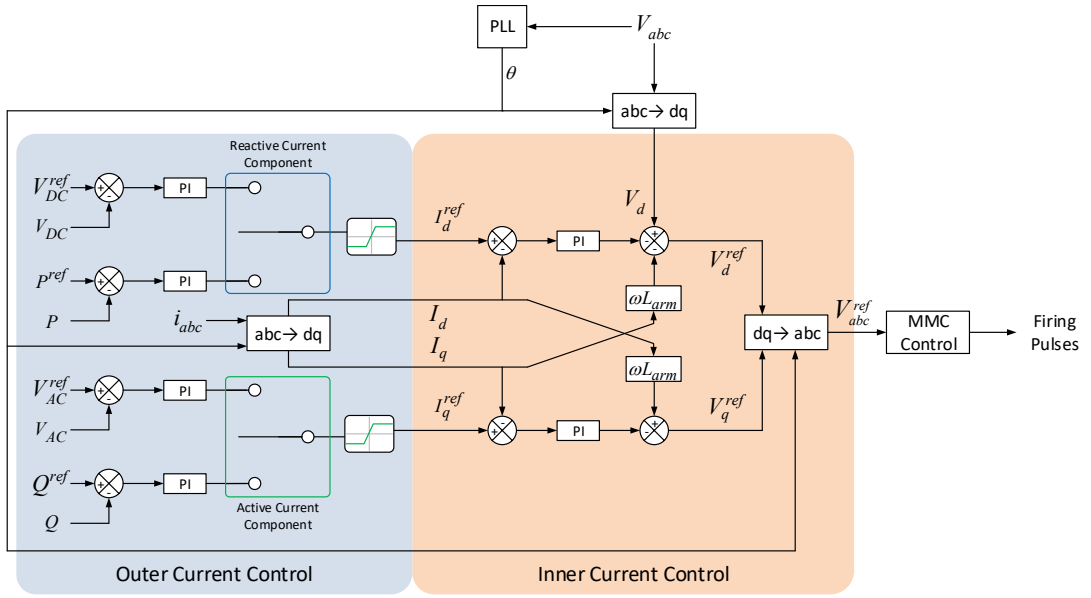


FIGURE 2.9: Outer and inner current control loops of VSCs.

The active (I_d) and reactive (I_q) currents, also called direct and quadrature components of the AC current, are regulated to their respective reference values provided by the outer control. The independent control of the components is achieved through feed-forward compensation of the cross terms [28], generating the voltage reference components V_d^{ref} and V_q^{ref}. These voltages are transformed back to three-phase quantities through the generation of three sinusoidal waveforms V_{abc}^{ref}, corresponding to the desired voltage output of the converter at its AC terminals. These reference sinusoidal waves are then provided to the "MMC Control" which, after a series of control loops specific to MMCs, generate the firing pulses of the IGBTs in the SMs. Saturation blocks are typically included between the outer and inner current loops to constrain the magnitude of I_d^{ref} and I_q^{ref} to values within the physical limits of the converter [59].

2.3.3 Modular Multilevel Converter Control

At a given moment, the AC voltage reference waveform that is supposed to be "followed" by the converter output voltage is provided by the VSC control structure shown in Figure 2.8. This voltage can be built using the distributed energy stored in the SM capacitors, through appropriate insertion and bypass of the SMs. Simultaneously, the arm voltages must be regulated so that the converter can match the DC voltage and is capable of providing the power transfer between the AC and DC sides. Accordingly, the converter operation can be summarised in the following sequence of steps:

1. Determine the necessary output voltage magnitude, given by the AC reference voltage waveform;
2. Determine the number of SMs in each phase and in each arm that need to be turned ON/OFF;
3. Determine which SMs will be switched ON/OFF;
4. Ensure the capacitor voltages in the SMs are kept within reasonable limits, i.e. they do not drift severely from a pre-defined reference value and from each other. In other words, they are balanced;
5. Produce the firing pulses for the IGBTs of the SMs that need to be turned ON/OFF.

This is significantly more complex than previous 2- and 3-level converter topologies and imposes the need of additional controllers to stabilise the operation of the converter [56, 60, 61]. The global view of the classic control strategy of an MMC is shown in Figure 2.10. The MMC Control block regulates the inner dynamics of the converter and is composed of three main dedicated control loops: Modulation, CVB and Circulating Current Suppression.

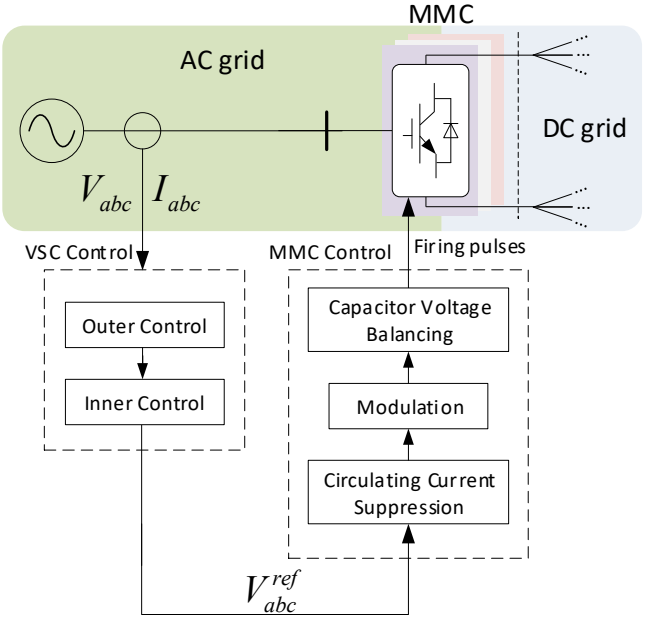


FIGURE 2.10: Control structure of a MMC.

2.3.3.1 Modulation

The modulation step determines the number of SMs that need to be turned ON/OFF at a given moment in a given arm, in order to generate the AC side voltage waveform. As shown by (2.20) and (2.21), the sinusoidal reference is phase-shifted by 180 ° between the arms of a phase, ensuring a complementary number of the SMs, from each arm, that are requested to build the desired voltage waveform.

Initial Modulation schemes were drawn from the control of VSCs. The voltage reference waveform is compared with a number of high frequency triangular waveforms, originating a series of pulses with varying width and naming this process PWM. Since multiple carriers are used, the term "multi-carrier PWM techniques" is frequently employed [62] and the arrangement and phase shift between the carriers determines the particular type of scheme used. Further modulation techniques have been proposed and can be classified into the following categories:

- Multi-Carrier Techniques:
  - Carrier-Disposition;
  - Phase-Shifted (PS) Carriers;
- Selective Harmonic Elimination (SHE);
- Nearest Level of Control (NLC).

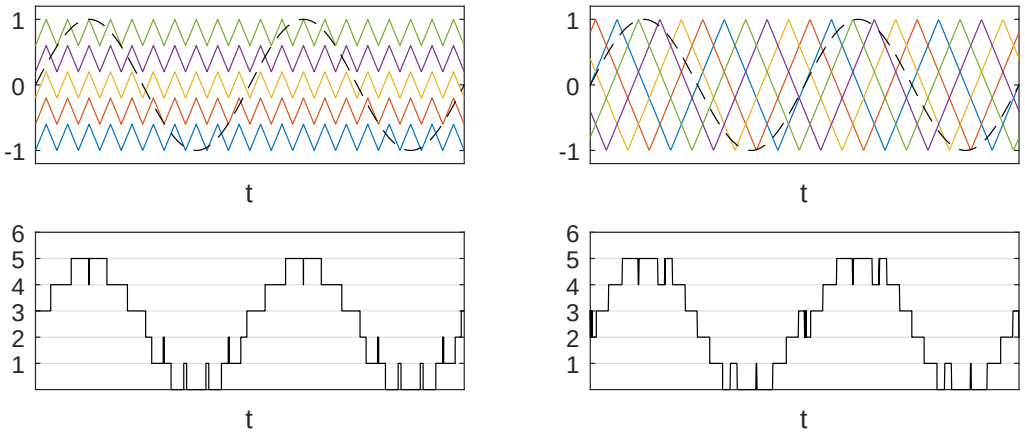
Carrier-Disposition PWM

In these techniques, N carrier waveforms with the same frequency and amplitude are displaced contiguously and symmetrically with respect to the zero axis [62, 63]. Each carrier is typically associated with a specific SM, resulting in a line-to-neutral output voltage waveform with $N + 1$ levels. The number of SMs to be inserted in an arm is determined by the number of carrier signals that are below the reference voltage. This is exemplified in Figure 2.11 (a) for a system with five carriers, where the bottom figure shows the resulting number of SMs n_{on} to be inserted in one arm; the other arm contributes with $(5 - n_{on})$ SMs.

Particular PWM methods are obtained according to the phase-shift between the carriers, with the basic Phase Disposition (PD) method being shown in Figure 2.11 (a).

Alternatively, in the Phase-Opposition-Disposition (POD) method, half the carriers are phase-shifted by 180° with respect to the other half, but the carriers in both halves remain in phase. For the Alternate Phase-Opposition-Disposition (APOD) approach, alternating carriers are phase-shifted by 180° with respect to the preceding carrier [62].

The major disadvantages of these techniques are related with the large magnitude of the resulting circulating currents, as well as a high THD in the output voltage [51], which can be mitigated by a carrier rotation mechanism [62, 64, 65]. Further improvements have been reported [61, 66] when the carriers in the PD-PWM method are not assigned to specific SMs. Instead, the sum of the pulses produces an $(N+1)$-level waveform that determines the number of SMs to be inserted in the upper and lower arms, and the gate signals for insertion and bypass are provided by a dedicated Capacitor Voltage Balancing Algorithm. An improved method has also been proposed in [67] where the Modulation scheme is greatly simplified by using only a single carrier per arm. The switching pulses are distributed alternately among the SMs of an arm, overcoming the need of a dedicated sorting algorithm.



(A) PD (B) PS

FIGURE 2.11: Typical carriers used in PWM schemes.

Phase-Shifted PWM

The carriers in the PS-PWM scheme are placed consecutively with a phase-shift angle $\theta = \frac{360^\circ}{N}$, as illustrated in Figure 2.11 (b). At any moment, the number of SMs to be inserted in an arm is determined by the number of carrier signals that are below the reference voltage. Each SM is associated with a specific carrier and the insertion and bypass commands are controlled independently based on the singular relationship of the SM carrier of the voltage reference [68]. The resulting switching patterns provide equal conduction times for all the SMs [62], overcoming the need for a dedicated Capacitor Voltage Balancing algorithm, due to the interesting self-balancing properties [69–71] exhibited by this technique. The carriers can also be interleaved and distributed alternatively between the upper and the lower arms, yielding an average SM switching frequency similar to the one resulting from a PD-PWM scheme [72].

A key feature of this method is that odd- and even-order harmonics can be separated between the AC and DC sides, respectively, through an appropriate choice of the switching frequency value [73]. Although this yields balanced operating conditions in the upper and lower arms [74], the choice of a particular value needs to be performed carefully as it can lead to diverging capacitor voltages [73].

The implementation effort of this method increases significantly with the number of SMs and instability may occur under certain operating conditions [75]. This can be overcome by the inclusion of additional compensation and feedback loops to modify the individual voltage reference waveform driving the capacitor voltages towards the reference value [76]. An additional mechanism for improved stability has been proposed in [77], based on the swap of the switching pattern in order to achieve a more even distribution among the SMs of an arm. Another possible solution is to promote a phase-shift rotation of each carrier [78].

Sawtooth carriers can also be used, under the designation of "Sub-Harmonic PWM" scheme [62]. The carriers are phase-shifted by an angle $\theta = \frac{360^\circ}{N-1}$, generating an output waveform with N levels. This, however, produces a higher distortion on the AC side voltages than an equivalent PD-PWM scheme [79, 80].

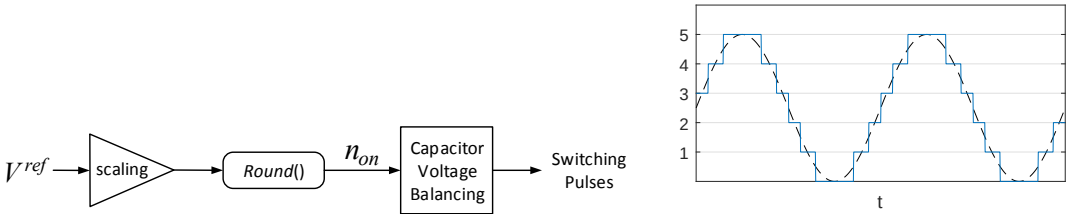
Selective Harmonic Elimination

In addition to these methods, SHE-PWM methods have also been reported in literature. In these approaches, either the switching patterns [81–83] or the firing angles [84, 85] of the IGBTs are pre-determined for various modulation indices and output voltage phase angles. The results are stored in a set of look-up tables and used to eliminate low-order harmonics in the output voltage waveform [86–90].

Nearest Level of Control

PWM-based and SHE Modulation strategies become problematic as the number of SMs increases to dozens or even hundreds, found in commercial projects [53]. PWM-based methods are less attractive due to typically high switching frequencies necessary for a reduced capacitor voltage variation span and low THD values in the output voltage. For SHE strategies, the major drawback lies on the complexity of managing and processing multi-dimensional tables of fire angles for multiple operating points.

Staircase-type methods such as NLC, initially proposed in [91], aim to overcome these limitations. In the NLC Modulation process presented in Figure 2.12 (a), the reference voltage waveform V^{ref} is scaled in the range $[0 - V_{DC}]$, sampled and divided by the average SM capacitor voltage v_C. The result is then rounded, producing the integer number n_{on} of SMs to be inserted in order to generate the desired output voltage; an example for a system with five SMs is shown in Figure 2.12 (b). Compared to the PWM-based and SHE methods, the NLC technique is easy to implement, more efficient, requires a smaller computational effort and yields a lower switching frequency [51]. It is, therefore, the preferred Modulation strategy for systems with a high number of SMs [53].



(A) Block diagram (B) SMs insertion waveform

FIGURE 2.12: NLC modulation.

Although the overall switching frequency is smaller than PWM-based methods, NLC modulation can lead to higher circulating current magnitudes, larger capacitor voltage ripples and increased THD of the output voltage [92]. The approach in [6] analysed the impact of the sampling frequency on the distortion of the output voltage waveform and derived a critical range where significant reductions in the THD can be achieved. A level-increased nearest level modulation has been proposed in [93], which attempts to build a staircase-like waveform without the typical switching harmonics introduced by the previous PWM methods and a particle swarm optimisation-based staircase modulation strategy has also been reported [94].

A Simplified NLC method coupled with a traditional sorting algorithm in the CVB process has also been proposed in [95], which simplifies and eliminates some of the stages of the balancing algorithm; it also eases the hardware implementation requirements. However, and compared with the basic NLC method, these advantages tend to be less significant as the number of SMs increases.

2.3.3.2 Capacitor Voltage Balancing

One of the main operational challenges of MMCs is the need to keep the individual capacitor voltages in each arm and phase leg balanced as the SMs are inserted and bypassed to generate the AC side voltage waveform. Capacitor voltage drifting is a well-known problem in early multilevel flying capacitor topologies [27, 39, 96] and a dedicated CVB method is usually employed in MMCs [60]. CVB algorithms are typically implemented on an arm basis where N capacitors share the total DC voltage V_{DC} and are balanced around an implicit reference average value of V_{DC}/N. Although approaches proposing an independent control of each SM capacitor voltage within an arm have also been proposed [97], the converter output current cannot be fully controlled to its exact reference using this method.

The most straightforward method is to use all the operating SM capacitor voltages in order to sort them before selecting the upper and lower arms' SMs to be switched ON. The selection can be made according to the highest or lowest capacitor voltages. For a specified number of SM's that need to be on the ON state in the upper and lower arms, determined in the modulation step of the MMC control, several switching combinations are possible. One of the approaches is the algorithm proposed in [61], where the capacitor

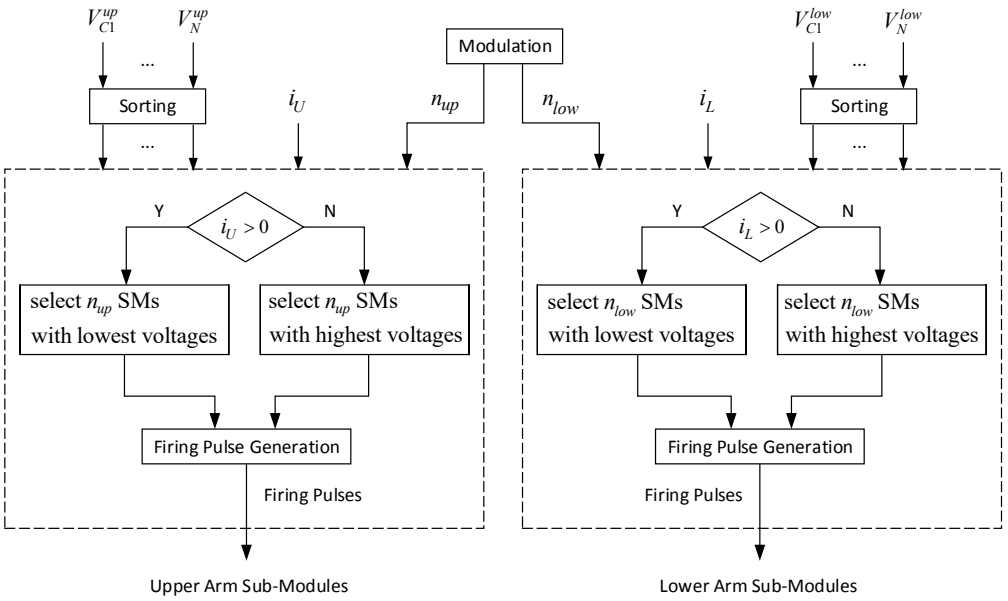


FIGURE 2.13: CVB in a Phase of a MMC.

voltage values and also the direction of the arm currents are used to select the SMs that should be switched ON and OFF, as shown in Figure 2.13.

Let n_{up} and n_{low} be the number of SMs that need to be turned ON in the upper and lower arms, respectively, of a phase, and where $n_{up} + n_{low} = N$. The HB SM configuration in Figure 2.4 is considered and this algorithm is implemented independently for each arm of each phase. To carry out the capacitor voltage balancing task of the SMs in each arm, during each period of the modulation the SM capacitor voltages of each arm are measured and sorted in descending order. If the upper (lower) arm current is positive, in each corresponding arm n_{up} (n_{low}) SMs with the lowest voltages are selected and switched ON. Consequently, the corresponding SM capacitors are charged and their voltages increase. If the upper (lower) arm current is negative, in each corresponding arm, n_{up} (n_{low}) SMs with the highest voltages are selected and switched ON. Consequently, the SM capacitors are discharged and their voltages decrease.

Even though this method can be easily implemented, the requirement of all the individual capacitor voltages and arm currents comprises a significant number of measurements that need to be acquired, processed and made available on the control level. This entails a significant computational burden [98, 99] as the number of SMs increases and values as high as 400 SMs per arm are used in commercial projects [53].

Several methods have been proposed, aiming to solve particular problems with the classic CVB method, either by trying to simplify the sorting and balancing methods or by reducing the number of necessary measurements. Alternative and less computationally-intensive voltage balance algorithms have been proposed at the expense of additional signal processing on the control level [100, 101]. Another approach [102] has presented the concept of a tolerance band to allow the capacitor voltages to variate more widely within a given balancing margin around their average value. This method enables the SMs' switching frequency to be as low as 70 Hz, although at the expense of significantly divergent capacitor voltages.

The amplitude of the capacitor voltage ripple is inversely proportional to the switching frequency and also depends on the Modulation scheme itself. Based on this, some approaches frequently promote some sort of modification of the Modulation method used in order to excel a particular aspect of the CVB algorithm. This typically occurs when PWM-based methods are used.

An improved PD-PWM method was proposed in [66], where the bias of the carrier wave is changed according to the balance situation of the system. In this method, only the capacitors with the highest or lower voltages are acted upon in order to decrease unnecessary switching actions, although some additional switching still exists. A discontinuous modulation strategy based on the injection of a zero sequence signal in the reference voltage has been proposed in [103] to minimize the switching losses and achieve a significant reduction in the capacitor voltage ripples. In this method modified modulation signals are provided by the circulating current control to define the SM insertion periods. This strategy is particularly suited for MMCs interfacing motors operating with low modulation indices, i.e. low frequencies/speeds. The method proposed in [104] relies on a modified PS-PWM method and does not require the measurement of arm currents, reducing the number of necessary sensors. Nonetheless, it relies of a high-frequency component related with the switching frequency, which may not be possible to use as the number of SMs increases to industrial levels.

An improved PS-PWM based method has also been reported [105], aimed at mitigating the capacitor voltages variation. The major drawback of this approach is the large variation of the output voltage THD according to the loading conditions, with values that may exceed the Grid Code requirements [106]. Since only the relative voltages of

the SMs in an arm are considered for the balancing algorithm, unnecessary switching actions occur for the previous methods, which can be avoided by employing the improved PD-PWM method proposed in [67]. However, the voltage balancing in achieved in a closed-loop fashion, which still requires the feedback of all individual capacitor voltages, similarly to the fast SM selection and balancing method proposed in [107]. This is also valid for the predictive sorting algorithm proposed in [108] that minimises the capacitor voltage deviations at low switching frequency. The same drawback is also present in the adaptive voltage balancing method in [109] that proposes a trade-off between the switching losses and the capacitor voltage balancing margin.

The arm current flow through the SMs will impose a fundamental frequency ripple on the average value of the capacitor voltages [42]. In order to further avoid unnecessary switching actions due to high switching frequencies, methods where switching instants occur at fundamental frequency have also been reported. However, these methods either introduce low-frequency ripples [110] or significant harmonic components [111] in the capacitor voltages, or require complex combination of pulse patterns based on pre-defined operating conditions [112].

Alternative approaches have also been proposed to avoid the feedback of all SM capacitor voltages and arm currents to the control level for the voltage balancing. This eliminates the need of large amount of measurements and the processing requirements on the control cabinets [98]. An open-loop control scheme where the capacitor voltages are not measured but the total arm energy estimated and used to derive the reference voltage for each SM was proposed in [99]. However, this method does not ensure the voltage balancing under all operating conditions. Another method with reduced computational requirements for the voltage balancing has also been proposed in [113], but additional hardware needs to be included in each SM to enable the self-power supply of capacitor voltages. An alternative approach has been proposed in [114], where an adaptive state observer was employed to estimate individual capacitor voltages while taking into account uncertainties related with unknown circuit parameters. Nevertheless, the convergence rate for the parameters estimation and capacitor voltages are quite subjective, as they depend on the observer and adaptation gains.

A space-vector (SV) modulation strategy has also been proposed in [42, 115], which eliminates the external controller for arm voltage balancing and reduces the required

number of current sensors by 50 %. A "divide and conquer" approach has also been explored in [116] using voltage mapping and categorization of the SMs in different regions. The objective is the reduction of the amplitude of the voltage fluctuation in the low-frequency region. This is achieved through the injection of zero-sequence voltage to change the frequency of the converter power fluctuation. The proposed strategy cannot, however, be applied to high modulation indices, constraining the operational range of the converter.

The previous methods have essentially tried to solve separately the reduction of the computational requirements for the voltage balancing and the need of all the capacitor voltages and arm currents measurements. It is worth noting that some of the benefits of the previous algorithms only materialise for specific power applications or operating conditions. Alternatively, generic and simple methods such as the one shown in Figure 2.13 can be used when the detailed representation of the semiconductor devices is used and when the dimension of the system does not exceed 10-20 SMs. This ensures that simulation times compatible with the representation of semiconductor switching events are kept within acceptable ranges.

Although some modulation techniques presented in subsection 2.3.3.1 can render the need for a CVB invalid, their application might not be always generalised. SM capacitor voltages can remain tightly regulated around their nominal value with minimal variation span if the switching frequency of the system is high. However, this leads to unnecessary switching losses, driving the need for some of the reduced switching frequency methods presented here, such as the NLC, usually coupled with a bespoke CVB algorithm.

2.3.3.3 Circulating Current Suppression

Due to the modulation process, since the SMs that are turned ON at any given instant are different in each phase of the converter, small imbalances between the sum of upper and lower arm voltages and the DC voltage will exist. This leads to the appearance of circulating currents in the arms of the converter, at twice the AC system fundamental frequency [117]. These currents do not flow to either AC or DC sides but circulate between the converter arms and increase the ripple of SM capacitor voltages [56, 60].

As the switching frequency is low, semiconductor conduction losses are dominant and essentially a function of the arm current [118]. Therefore, circulating currents contribute directly to converter losses by distorting and increasing the peak and rms values of the arm currents. Different methods for suppressing circulating currents have been proposed. These include the proper design of the arm inductors [119], the use of a physical filter [54] and several "suppression-by-control" approaches, implemented in the form of an additional control loop.

Different circulating current injection and suppression strategies have been analysed and compared in [120], including the proposal of a closed-loop method where the regulation of the capacitor voltages is achieved with low ripple. Further approaches have essentially developed dedicated control loops to mitigate the magnitude of the circulating currents, frequently aiming at simultaneously reducing the capacitor voltage variation span. These approaches have essentially used proportional-resonant controllers [121, 122], repetitive controllers [123, 124] or even feed-forward compensation [125] and moving average filters [85] to eliminate the parasitic harmonic component.

A simple and popular scheme to suppress these currents was proposed in [126] and further investigated in [127]. The suppression controller follows the principle of vector control and is presented in Figure 2.14. Following this principle, the inner difference current i^j_{diff} for each phase ($j = a, b, c$) is calculated by adding the respective upper (i_{pj}) and lower (i^j_n) arm currents. They are then transformed to the double line-frequency, negative-sequence rotational frame, originating i_{2fd} and i_{2fq}. With both reference values of i_{2fd_ref} and i_{2fq_ref} set to zero to minimize the circulating currents magnitudes, the control signals are obtained through PI controllers with cross-coupling compensation. The three-phase inner unbalanced voltage u_{diffj_ref} is obtained by applying the inverse Park transformation and then added and subtracted to the lower and upper arm reference voltages, respectively. This voltage difference leads to a slight increase or decrease in the arm voltages, compensating the difference of the sum of arms voltages to the DC voltage and therefore eliminating the arm current component at twice the AC system fundamental frequency.

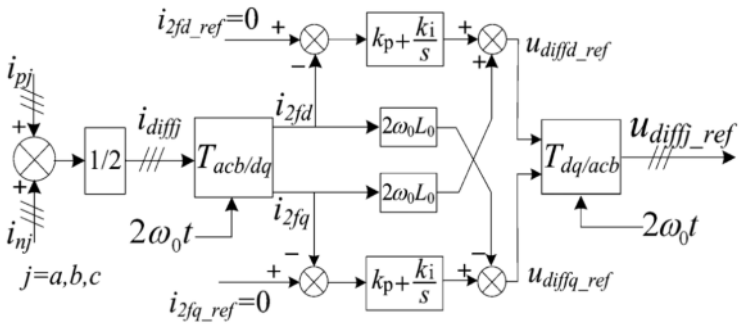


FIGURE 2.14: Circulating current suppression controller [6].

2.3.3.4 Alternative MMC Control Strategies

Alternative control strategies have also been proposed, where the different control functions of the converter are not associated with dedicated and explicit control loops. Two of these strategies are presented here.

Averaging and Balancing Control

This control strategy, proposed in [68], is implemented per phase and is presented in Figure 2.15. The CVB function is divided in two control loops: averaging control and balancing control. The averaging control is implemented per phase leg and used to enforce an average capacitor voltage $v^*_{SM\,nom}$ across all SMs in a phase. This control loop is also responsible for the mitigation of the circulating in the respective phase. The balancing control is implemented for each SM, e.g. SM k, and responsible for forcing each capacitor voltage $v_{C\,k}$ to follow an individual reference $v^*_{SM\,nom}$.

The AC voltage command V_{ref} is provided by the high-level VSC control of the converter and both the DC voltage v_{DC} and SM capacitor voltages v_C are included as feed-forward controlled variables. The carrier waveforms of the PWM scheme are phase-shifted by $(360/N)^\circ$ for each SM to improve current control and reduce harmonic content. Consequently, the arm will produce a multilevel voltage waveform with $N+1$ levels.

This control structure proposes a distributed per-SM CVB strategy that eliminates the need for an external sorting and selection method and has demonstrated a good dynamic performance in experimental tests.

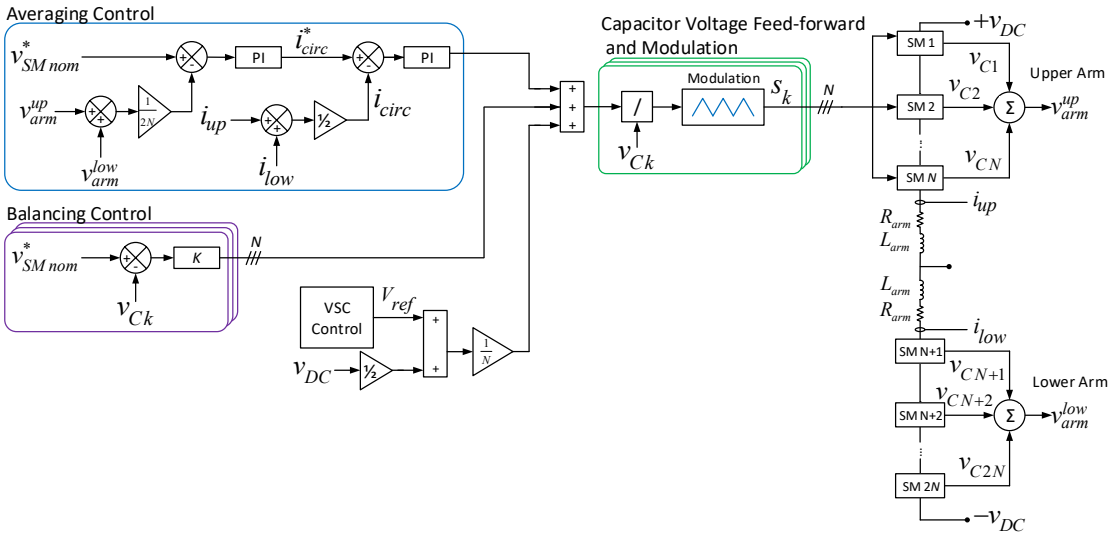


FIGURE 2.15: Averaging and balancing control-based CVB in a MMC.

Model Predictive Control

The different control functions regulating the internal MMC dynamics and shown in Figure 2.10 and Figure 2.15 were treated explicitly through dedicated loops. Alternatively, the control of an MMC can be based on a Model Predictive Control (MPC) framework. An optimisation method is employed for the selection of the best switching state that results in the minimum value for a defined cost function associated with the control objective of a system [128–131].

A MPC strategy is a promising control method to control power electronic converters due to its fast dynamic response, flexibility to include constrains and non-linearities of the system, and ease in implementation [132–135]. The main disadvantage of this approach lies on the large computational requirements, which rise exponentially with the number of switching states [136].

For MMCs, the objective consists on the control of AC side currents, regulation and balancing of SM capacitor voltages and circulating currents suppression. For converters with a large number of SMs, and given the high number of switching possibilities resulting from different combinations of SMs insertion and bypass states, the control performance becomes compromised and this method is impractical. Nonetheless, experimental test have validated the use of MPC as a valid control strategy for MMCs with a small number of SMs [136–139].

2.4 Operational Requirements and Challenges

Research into MMCs has essentially focused on the investigation of system-level control function such as loss minimisation, CVB algorithms and circulating current elimination methods. Other important control and operational requirements concern the methods put in practice to ensure a safe and reliable operation, as well as the electrical and thermal design of the system, with a particular focus on the semiconductor devices.

2.4.1 Semiconductors Temperature Control

In the classic VSC-type control, depicted in Figure 2.9, the outer controllers provide the I_d^{ref} and I_q^{ref} components of current to the inner current loop. The operating point of the converter is below its maximum electrical rating, due to safety and reliability reasons, therefore the above mentioned current reference components are subjected to limits, as shown. The way these limits are defined follows a rather conservative approach, being defined as 1.2-1.5 per unit of the rated load [59], and only consider the electrical limits of the most sensitive components in the converter station, the semiconductor devices. The derating of the converter can ensure the thermal limits are respected, at least for steady state operation, but leads to a very poor operation from both technical and economic points of view.

Even under worst-case conditions such as faults, the operating point of the semiconductors must be kept inside the Safe Operating Area (SOA) specified in the devices data-sheets. The SOA is an operating range defined as a function of maximum allowed collector current I_C and collector-emitter voltage V_{CE} values, as presented in Figure 2.16, for which the device can operate without damage. It consists in a graphical representation of the device power handling capability under various conditions and combines the maximum junction temperature, bond wires current carrying capability and internal power dissipation limits [7].

For IGBTs, the turn-off transient is of special importance due to effects such as minority carrier storage time and capacitance [7]. For these devices, the Reverse Bias Safe Operating Area (RBSOA) is the SOA typically specified in data sheets and corresponds to the limitations during the device turn-off. As long as the collector voltage and collector current stay within the RBSOA during the entire turn-off, the IGBT is safe. Since

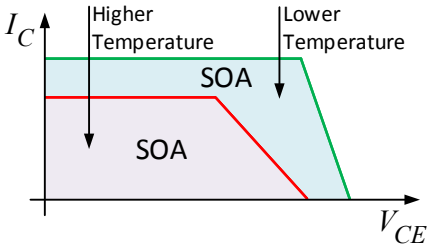


FIGURE 2.16: SOA of a semiconductor module [7].

the RBSOA is associated with the very brief turn-off process, it does not constrain the continuous power dissipation limit.

For MMC applications the key main factors driving the operational limits of the semiconductor devices are the SM capacitor voltages and the arm currents flowing through the dies. These parameters must be regulated to obey the SOA and RBSOA limits, but also the more stringent temperature limits. With the exception of the small ripple due to the voltage balancing span, the capacitor voltages are essentially regulated for a constant value. The low switching frequency that can be achieved in the modulation step translates into dominant conduction losses in an MMC, which is a key difference from 2- and 3-level predecessor topologies. Accordingly, the control of semiconductor devices temperature in MMCs, and its implications on the converter rating, can be essentially performed by acting on the current (VSC) control layer of the complete converter control. Specifically, on the current control limits shown in Figure 2.9.

Although the current limits can be re-defined, the junction temperature must be kept within a safe limit. Given the widespread adoption of MMCs in HVDC systems, especially for the connection of offshore wind farms, current overload capability might be required. This is foreseeable in the near future as features such as inertia and frequency support are frequently reported [35] as being potentially used for the provision of power support to AC grids due to unbalances between load and generation. The use of fixed limits as a conservative approach for semiconductors temperature control undermines the possibility to, at least temporarily, provide some overload capability.

2.4.2 Management of Sub-Modules Redundancy and State of Health Monitoring

Benefiting from its modularity, the reliability of a MMC can be easily ensured by integrating a certain additional components accounting for redundancy, so that upon the failure of a component, a healthy spare part will replace the faulty one. In HVDC applications, this translates into a non-interruptible power transmission until the next programmed maintenance [140, 141], typically every 1-2 years [54]. Although the MMC topology is often featured with its robustness for component failures, different topologies arrangements lead to distinct redundancy implementation and management approaches.

For the CTL shown in Figure 2.5, its similarity to low-level VSC topologies requires high-voltage switching devices where several semiconductors are connected in series and work simultaneously to attain the desired voltage blocking capability [54, 140]. The redundancy for fail-safe operation is achieved through the appropriate choice of the SMs and IGBTs rating. In this converter, the semiconductor modules are designed to fail in a short-circuit mode [54]. The failure of an IGBT means that the remaining operational semiconductors will withstand the necessary blocking voltage to ensure the post-fault operation of the SM and the converter station.

In the straightforward HB-MMC implementation illustrated in Figure 2.3, the low rating of the IGBTs used in the SMs leads to the addition of redundant SMs in the converter station. The fail-safe functionality can be easily implemented simply by bypassing the faulty SM using its bypass switch [142] and replacing it by a healthy spare one. Unlike traditional medium-voltage multilevel converters, the redundant SMs are always bypassed and do not operate the same way as the ordinary SMs [140]. Due to the high number of SMs per arm in MMC-based HVDC transmission projects, (e.g., 200 SMs in the TransBay Cable Project [55], 220 in the Nan'ao Project [33] and 400 SMs in the INELFE Project [53]), the output voltage waveform is almost perfectly sinusoidal. Therefore the activation of redundant SMs is not practical in real applications and will have little impact in the voltage waveform quality [140].

The management of the SMs redundancy requires a high-level control to account not only or possible impacts on the global converter operation but also for the control of the SMs safety and integrity. Besides addressing the system-level impact of the SMs

redundancy, a proper management system must be responsible for a fast and accurate detection of abnormal operation conditions of the SMs, i.e. must monitor the SMs state of health (SOH). Previous work have analysed the design and control of a MMC for non-interruptible energy transfer [141], as well as the effect of the use of redundant SMs to improve the converter operation. Some examples are the reduction of the harmonic amplitude in the circulating current and reduced utilization of the SMs [143], and the improvement of the fault ride-through performance of the converter [144]. The effect of inserting spare SMs (cold reserve) to replace faulty ones has also been analysed in [140]. Nonetheless, the crucial part of the management system, the diagnosis algorithm, responsible for the detection and signalling of abnormal or degraded SMs' SOH, has been poorly addressed, in favor of approaches focusing only on fault detection.

Earlier fault detection approaches on multilevel topologies have focused on cascaded H-Bridge (CHB) converters, structurally similar to MMCs. A detection approach was presented in [145], based on the magnitude of the switching frequency component of the output phase voltage, which becomes significantly larger after the occurrence of a fault. However, the method is complex to implement and very prone to provide an erroneous diagnosis during transient operating conditions. An artificial intelligence-based fault detection algorithm has been proposed in [146], which besides presenting a low accuracy for some cases, also requires a long training time for the circuit and all the fault scenarios.

With respect to particularly suited methods for MMCs, a detection algorithm has been proposed in [147]. The method is based on a sliding mode observer and requires the input of converter arm currents and individual SM capacitor voltages, allowing the detection of faulty semiconductors in the SMs. Although the detection is achieved in a windows of 100 ms, the accuracy is very sensitive to measurement errors. A control strategy to enable a fault-tolerant operation of MMCs has been proposed in [77], where the fault detection is achieved by comparing the measured capacitor voltages and circulating currents with their reference values. However, for MMCs with a large number of SMs, such as in industrial applications, the sampling frequency of the proposed algorithm has to be decreased to reduce the calculation burden and to avoid over-provisioning. A fault detection and localization method has also been proposed in [148], based on the comparison of measured and estimated state variables from a Kalman Filter. Besides only being applicable for the detection of one kind of fault, the algorithm must be

executed with a very small time step, leading to a high computational burden. This becomes unacceptable for systems with a large number of SMs.

Further methods reported in the literature have essentially proposed SM fault detection methods and immediate control actions utilising the redundant SMs to resume operation of the converter [149–151] or explored different SM redundancy strategies [152, 153]. If redundant SMs are not available, a possible solution is the utilisation of the approach proposed in [154], where a faulty SM is bypassed and the number of operating SMs in both arms is decreased. As a result, the quality of the output voltage waveform is degraded and its THD increases. Nonetheless, the nonexistence of redundant SMs leads to low reliability metrics [153, 155, 156] that can trigger the shut-down of the converter station. Given the very high amounts of power typically flowing through the DC link, this is a highly undesirable event and underlines the need of SM-level SOH monitoring strategies that can act upon the detection of non-ideal operating conditions. Presently, limited work has been reported in this area.

2.5 Summary

This chapter introduced the power electronic converters used in HVDC grids. The topologies and operation principles of LCCs and 2- and 3-level VSCs are described and the review highlighted MMCs, the current state of the art topology due to several technical advantages and capabilities.

The control and operation of MMCs is more complex than previous VSC topologies and its cascaded control layers have been discussed in detail. The general VSC control enables the MMC to control system-level quantities such as active or reactive power and AC or DC voltages, generating a reference AC voltage waveform to be used by the MMC control. The MMC control comprises three dedicated but strongly related control loops: modulation, CVB and circulating current suppression. The modulation process uses the reference voltage waveform provided by the VSC control to determine the number of SMs to be inserted and bypassed in each arm. This can be done recurring to a multitude of PWM- or NLC-based methods, typically operating at low switching frequency. Although several simplified methods have been proposed, the CVB algorithm typically requires all the SM capacitor voltages and arm currents feedback, and employs

a sorting algorithm to select the SMs to be effectively inserted and bypassed. The circulating current suppression step mitigates parasitic harmonic current components in the arm currents at twice the AC system fundamental frequency, responsible for increased SM capacitor voltage ripple and losses. The MMC Control provides the final gate signals for the IGBTs in the SMs. Alternative control strategies have also been presented and discussed.

Other important operational requirements and challenges in MMCs have also been identified and discussed. These concern the methods put in practice to achieve a safe and reliable operation, as well as the electrical and thermal design of the system to ensure a safe operating environment for the semiconductor devices. Reliability in MMC is typically achieved through the inclusion of redundant SMs: in case of an internal problem, the faulty SM is bypassed and replaced by a spare one. Several identification strategies of abnormal conditions and converter control methods have been identified and discussed.

The operational limits of the converter are defined in the VSC Control, where the fixed maximum permissible value of the current is typically defined. The current limit has been identified as the key parameter to enable the semiconductors operation within its safe operating range, as well as permitting the temperature to remain under strict limits, especially under transient conditions like faults. The widespread adoption of MMCs for the connection of large renewable generation projects and different countries with varying loads foresees the need of enabling additional control functionalities such as current overload capability. This possibility is undermined by the conservative approach of using fixed current limits in the control level as a mean for semiconductors temperature control.

Chapter 3

Junction Temperature Estimation in Power Electronic Modules

3.1 Introduction

The key to an improved operation of power electronic converters and better utilisation of the semiconductors thermal capacity is to consider semiconductors' junction temperature, which is also critical for condition monitoring [157] of the devices reliability. Measurements from easily accessible locations such as the heat sink or coolant temperature do not provide the necessary time-critical information and dedicated temperature estimation methods need to be employed. This chapter presents an overview of the electro-thermal dynamics of semiconductor devices and details a loss calculation process particularly suitable for MMCs. A literature review on different methods for junction temperature estimation is presented, including an analysis of the requirements and challenges of their practical implementation.

3.2 Semiconductors Electro-Thermal Dynamics

3.2.1 Thermal Model

Semiconductor devices in power electronic modules operate as switches and phenomena such as resistive heating, potential barrier drops and carrier recombination result in

losses in the dies in the form of heat, leading to a temperature increase in the junction. Semiconductor losses are generally divided in conduction and switching losses, which are aggregated into a single power loss value. Although losses occur in localised regions in the die structure, it is assumed they are produced evenly throughout the die due to its size, thickness and thermal conductivity, and therefore a uniform die temperature is presumed.

In electronic applications using semiconductor transistors and diodes, the junction temperature generally must be kept below a certain maximum temperature. For Silicon (Si) based devices, this is typically $110 - 180\,^{\circ}\mathrm{C}$ [158], while for wide-bandgap (WBG) devices such as Gallium Nitride (GaN) and Silicon Carbide (SiC), temperatures in excess of $300\,^{\circ}\mathrm{C}$ are permitted [159]. This tolerance for higher operating temperature results in better overall system reliability and enables smaller, lighter and more efficient systems. However, their power rating is yet to match the values of currently available Si-based high-power semiconductor devices.

The concept of "junction temperature" is a simplified approach in that it assumes the surface temperature of a die is uniform and ignores three-dimensional thermal gradients resulting from high power conditions or when a single die has multiple heat sources [7]. Heat conduction process in electronics is usually achieved through conduction from the heat source, the die, to the surrounding ambient through a series of different layers. Although this is a complicated three-dimensional process governed by differential equations, a one-dimensional heat flow is assumed for the sake of simplification. This is valid when the heat inducing area is larger than the material cross-section, so that a "heat spreading" effect does not occur. This applies as long as the heat propagation is not obstructed by subsequent layers with low conductivity (heat accumulation effect). Furthermore, the size of every volume element in which heat is produced must be determined exactly because its thermal capacitance has a decisive influence on the thermal impedance of the system when power dissipation pulses occur with a very short duration [160].

As a result, the heat conduction process can be modelled by an equivalent electric circuit diagram consisting of lumped RC elements and voltage sources, which can be used to predict and evaluate the thermal performance of semiconductor devices. This is illustrated in Figure 3.1 considering the thermal interface with a heat sink and where P_L

represents the power dissipation (heat flow occurring in the chip in the thermal equivalent network), T_J is the junction temperature and T_a is the ambient air temperature.

Each layer is characterised by a thermal resistance, defined as a function of its thickness, area and thermal conductivity, and by a thermal capacitance which depends on the layer volume, specific heat and material density. Although parameters such as the thermal resistance $R_{th\,CHS}$ between the module case and the heat sink are provided as lumped values, they comprise multiple parameters, e.g. the contact resistances $R_{th\,contact}$ between the case and heat sink and the thermal grease or thermal interface material (TIM), and the TIM layer resistance $R_{th\,TIM}$ itself.

The power generated within the die increases the device temperature according to the thermal capacitances and resistances of the layers involved, from the die to the module case or from the die to the heat sink, as presented in Figure 3.2.

The transient thermal behaviour can be determined by an equivalent mathematical thermal impedance Z_{th} that embodies the response of the die temperature to dynamic conditions as a series of exponential terms determined by a curve-fitting method [7]:

$$Z_{th}(t) = \sum_{i=1}^{m} R_{th\,i}\left(1 - e^{-\frac{t}{\tau_i}}\right) \tag{3.1}$$

where, for each layer, $\tau_i = R_{th\,i}C_{th\,i}$. The thermal network corresponding to the impedance parameters can be represented [7] by the series connection of parallel $R_{th}C_{th}$ elements in a Foster representation, or by the Cauer form shown in Figure 3.2. Using the electrical-thermal system analogy, the junction temperature can be determined as:

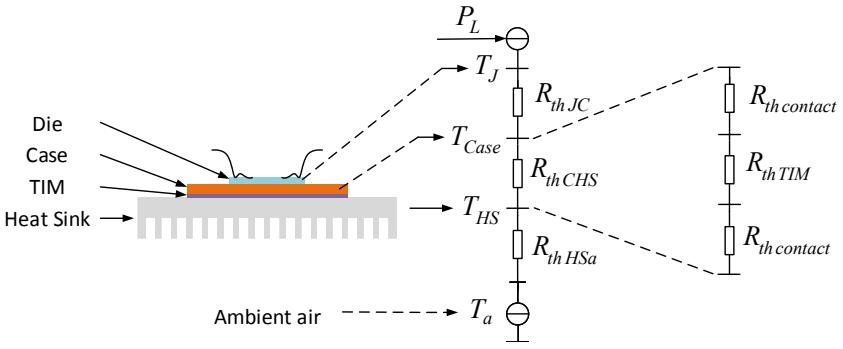


FIGURE 3.1: Equivalent thermal model of a semiconductor module considering the thermal interface with a heat sink.

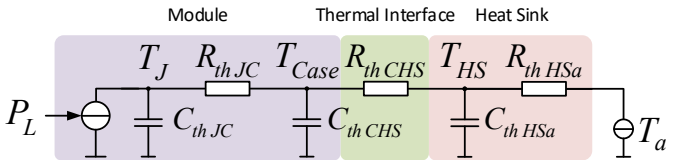


FIGURE 3.2: Equivalent thermal model of a semiconductor module for the estimation of junction temperature.

$$\mathrm{T}_J(t) = P_L(t) * Z_{th}(t) + T_a \tag{3.2}$$

3.2.2 Semiconductors Cooling

Due to the large amounts of heat generated during their operation, semiconductors for high-power applications such as HVDC are liquid cooled, which allows their temperature to be controlled within reasonable values for a wide range of operating scenarios. A simple water cooling system is shown in Figure 3.3 and the main components and respective functions are [8]:

- Object to be cooled: semiconductor valves for HVDC applications, converters and rectifiers;
- Pump: pumps the water through the system. Normally a redundant system with double pumps and motors is implemented for additional reliability;
- By pass: to by pass warm water in order to keep the cooling water at the desired temperature, if required;
- Heat exchanger: equipment where the temperature of the cooling water is decreased by means of raw water supply, dry liquid cooling (free cooling, fans), chillers or evaporate cooling units. They can be made of different material such as aluminium, copper, stainless steel or titanium depending on the quality of the cooling water or the environment where the coolers are placed;

- Make up water: possibility to add water when necessary. Can be manual or automatic;
- Ion exchanger: responsible for the de-ionization of water to a defined level, typically through polystyrene bottles containing a chemical resin;
- Filter: filtering of the water to avoid small particles to circulate in the system;
- Strainer: mechanical filtering of the main cooling water;
- Expansion vessel: handles the volume variations of the cooling water caused by temperature variations.

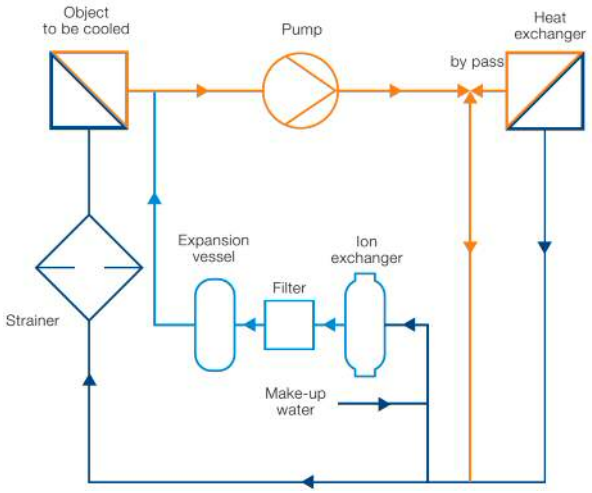


FIGURE 3.3: Flow diagram of a water cooling system [8].

Essentially, a water cooling system has a main loop cooling the object, with water transferring the heat to water-to-water or water-to-air heat exchangers. From the main loop a small part of the flow passes through a water-treatment circuit, where the water is filtered mechanically and is also continuously purified from ions and oxygen. The conductivity of the cooling water at 25 °C can hence be maintained as low as $< 0.1\,\mu S/\text{cm}$.

For the cooling of semiconductors in applications such as HVDC converters and drives, low conductivity is essential, hence pure water is used. When the ambient temperature is below 0 °C or when there is risk of freezing, a Glycol-water mixture is utilised instead.

The results of an industrial survey reported in [36] have shown that cooling system faults are the leading cause of power electronic converter failures, underlining the necessity of providing a reliable cooling plant, as well as the need of effective thermal management

strategies. This is especially crucial since an outage in this system may result in serious damage to the semiconductors. Usually redundant components are employed [161].

3.2.3 Losses and Temperature Calculation

Online junction temperature estimation requires the calculation of device-specific conduction and switching losses, which can be approximated by the specifications of the semiconductor module provided by the manufacturer. The characteristic curves for conduction and switching loss calculations can typically be accurately approximated with an exponential [118] or a 2^{nd} order polynomial curve [162, 163] using a least-squares curve fitting method applied to the semiconductor module datasheet information.

3.2.3.1 Conduction Losses

The relationship between the voltage drop V_{CE} and the collector current I_C of an IGBT, or forward voltage V_F and current I_F for a diode is provided by the manufacturer's datasheet. Assuming that the IGBTs and diodes can be modelled as a constant voltage drop V_0 and a series resistance R_0, losses can be calculated considering the average (I_{avg}) and rms (I_{rms}) values of the arm current:

$$P_C\left(I_{avg}, I_{rms}\right) = V_0 I_{avg} + R_0 I_{rms}^2 \tag{3.3}$$

The parameters in (3.3) can be determined graphically, as demonstrated in Figure 3.4 for the IGBT die in the HB module FF75R12YT3 from Infineon [9]. The voltage drop V_0 can be read directly from the datasheet and the series resistance R_0 can be calculated from the voltage and current measurements at 25 °C and 125 °C, $\{V_{D\,25}, I_{25}\}$ and $\{V_{D\,125}, I_{125}\}$, respectively :

$$R_{0\,25/125} = \frac{V_{D\,25/125}}{I_{25/125}} \tag{3.4}$$

Including a first-order approximation [162] for temperature (T) dependency on the curve-fitting coefficients V_Q, R_Q, V_D and R_D, conduction losses for the IGBT (Q) and diode (D) dies are calculated as:

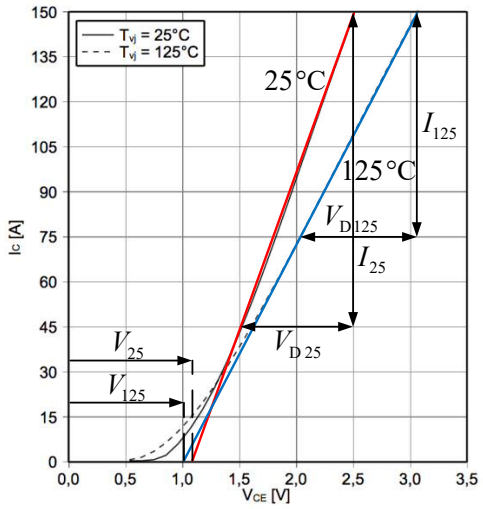


FIGURE 3.4: Typical output characteristic of IGBT die [9].

$$P_C\left(I_{avg}, I_{rms}, T\right) = \left(V_0 + V_1 T\right) I_{avg} + \left(R_0 + R_1 T\right) I_{rms}^2 \tag{3.5}$$

Since there is one pair of $\{V_0, R_0\}$ coefficients that can be determined for each datasheet temperature, typically 25 °C and 125 °C ($\{V_{25}, R_{0\,25}\}$ and $\{V_{125}, R_{0\,125}\}$, respectively, as shown in Figure 3.4), the coefficients in (3.5) can be determined as:

$$V_0 = \frac{V_{25} \times 125 - V_{125} \times 25}{125 - 25} \tag{3.6}$$

$$V_1 = \frac{V_{125} - V_{25}}{125 - 25} \tag{3.7}$$

$$R_0 = \frac{R_{0\,25} \times 125 - R_{0\,125} \times 25}{125 - 25} \tag{3.8}$$

$$R_1 = \frac{R_{0\,125} - R_{0\,25}}{125 - 25} \tag{3.9}$$

3.2.3.2 Switching Losses

Switching losses depend of several operating conditions of the device, namely blocking voltage, gate resistor value, gate supply voltage and temperature, and the dependency on the current is provided in the datasheet for a well-defined set of these parameters. The construction of detailed semiconductor physics-based models [164, 165] to provide an accurate representation of the switching events requires very small time steps, leading

to extremely large simulation times, therefore being unsuitable for online loss calculation. Alternatively, switching losses can be calculated analytically based on the switches on-times, when the modulation scheme is well defined [166]. However, the analytical calculations are frequently difficult to perform.

Other alternatives suitable for an online implementation rely on a loss look-up table, defined as a function of the device operating parameters such as current and blocking voltage [167]. The accuracy can be further improved by counting the switching losses and weighting them with the loss energy data in a table [168]. Alternatively, the counting of the switching actions can be used to calculate switching losses through an equation that assumes a direct dependency between the current being switched and the switching loss energy [169, 170]. This approach will be used in this work and is demonstrated in Figure 3.5 for the IGBT die in the half-bridge module FF75R12YT3 from Infineon [9].

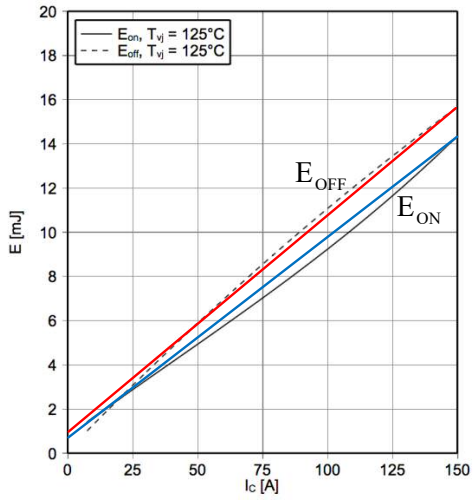


FIGURE 3.5: Typical switching energy losses of IGBT die [9].

At every switching instant the total switching-loss energies E_{total} (turn-on and turn-off losses for IGBTs and turn-off losses for diodes) are accounted at the beginning and end, respectively, of each switching period. The switching instants are then considered in accordance with the device switching frequency.

Switching losses P_{sw} can be determined using the rms value of the arm current and be scaled by the ratio of the SM capacitor voltage v_C to the reference voltage V_{CE}^{ref} specified in the datasheet:

$$P_{sw}\left(I_{rms}, v_C, f_{sw}\right) = E_{Total}\left(I_{rms}\right) \frac{v_C}{v_{CE}^{ref}} f_{sw} \tag{3.10}$$

If the switching-loss energy values are provided for more than one operating temperature value (usually only for 125 °C, as shown in Figure 3.5), temperature dependency can be included in the curve fitting coefficients, as shown in (3.6) - (3.9).

The total losses P_L in the IGBT and diode dies are calculated as the sum of conduction and switching losses:

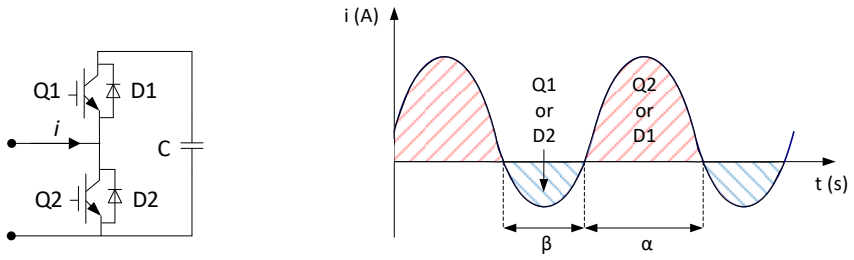
$$P_L = P_C\left(I_{avg}, I_{rms}, T\right) + P_{sw}\left(I_{rms}, v_C, f_{sw}\right) \tag{3.11}$$

3.2.3.3 Losses Distribution

During the operation of the semiconductors, losses depend not only on the current through and the voltage imposed on the individual chips, but also on their individual conduction periods. Consequently, there may be significant differences between the temperatures of IGBTs and diodes in the same SM [118] and their individual temperatures must be determined.

Considering a HB SM, as illustrated in Figure 3.6 (a), IGBTs Q1 and Q2 will conduct in a complementary fashion, i.e. Q1 will conduct with a duty cycle D and Q2 with duty cucle of (1-D). According to the current polarity, *i.e.* positive or negative, different elements will be in the current path, and therefore subject to losses. Taking the arm current shown in Figure 3.6 (b) as an example, when the current is positive it will flow though Q2 or D1. When it is negative, it will flow through Q1 or D2. As the arm current has an offset, considered to be positive in Figure 3.7 and Figure 3.6 (b), the conduction periods will not be the same for all the chips. As can be seen on Figure 3.6 (b), Q1 or D2 will conduct for a duration β and Q2 or D1 will conduct for a duration α, where the overall duration $\alpha + \beta$ corresponds to the fundamental period of the AC-side current imposed on the arm.

As presented in subsection 2.3.3.3, the parasitic circulating component in the arm current can be eliminated through appropriate methods. Accordingly, the arm currents, whose typical waveforms are illustrated in Figure 3.7, will have a fundamental frequency component with angular frequency ω, imposed by the AC-side current (I_{ac}), and a dc offset (I_{dc}) responsible for active power transfer between the AC and DC sides:



(A) (B)

FIGURE 3.6: HB IGBT SM: (a) - Configuration and (b) - Typical waveform for the arm current in an MMC.

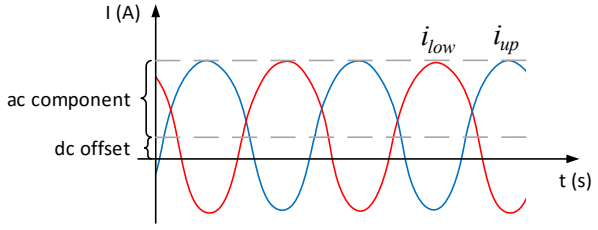


FIGURE 3.7: Typical waveforms for the arm currents in an MMC.

$$i_{arm} = I_{ac} \sin(\omega t) + i_{dc} \tag{3.12}$$

The conduction periods $\{\alpha, \beta\}$ can be determined by finding the zeros of the trigonometric equation (3.12):

$$t = \frac{2\pi n - \arcsin\left(\frac{I_{dc}}{I_{ac}}\right)}{\omega} \quad \wedge \quad t = \frac{2\pi n + \pi + \arcsin\left(\frac{I_{dc}}{I_{ac}}\right)}{\omega}, \quad n \in \mathbb{N} \tag{3.13}$$

The solution can be found by considering the two first set of solutions, *i.e.* $n = 0$ and $n = 1$. The first solution for $n = 0$ will result in an inadmissible negative value while the second solution and the first solution for $n = 1$ will result in admissible values. As $\alpha + \beta$ corresponds to the fundamental period $T = \frac{2\pi}{\omega}$ of the arm current, only two calculations are needed to determine both α and β:

$$\beta = \frac{2\pi - \arcsin\left(\frac{I_{dc}}{I_{ac}}\right)}{\omega} - \frac{\pi + \arcsin\left(\frac{I_{dc}}{I_{ac}}\right)}{\omega} = \frac{\pi - 2\arcsin\left(\frac{I_{dc}}{I_{ac}}\right)}{\omega} \tag{3.14}$$

$$\alpha = \frac{2\pi}{\omega} - \frac{\pi - 2\arcsin\left(\frac{I_{dc}}{I_{ac}}\right)}{\omega} = \frac{\pi + 2\arcsin\left(\frac{I_{dc}}{I_{ac}}\right)}{\omega} \tag{3.15}$$

The duty cycle D of the IGBTs and the conduction times α and β affect differently the value of the average (I_{avg}) and rms (I_{rms}) currents responsible for the losses in the dies. As the arm current is a sinusoidal waveform with an offset, its average and rms values can also be determined as a function of its components:

$$I_{avg} = I_{dc} \tag{3.16}$$

$$I_{rms} = \sqrt{I_{dc}^2 + \frac{I_{ac}^2}{2}} \tag{3.17}$$

Considering the individual chip temperatures in a HB SM, as shown in Figure 3.6 (a), the average and rms values of the current in each IGBT and Diode k can be determined as:

$$I_{avg/rms\,k} = \delta I_{avg/rms} \tag{3.18}$$

Where

$$\delta = \begin{cases} D\beta, & k = Q1 \\ (1-D)\,\alpha, & k = Q2 \\ D\alpha, & k = D1 \\ (1-D)\,\beta, & k = D2 \end{cases} \tag{3.19}$$

3.2.3.4 Temperature Calculation

The die temperatures in a HB SM, as presented in Figure 3.6 (a), can be calculated using (3.2.1), considering the losses for the IGBT and diode dies and their individual average and rms currents given by (3.18) and (3.19).

The loss calculation equation in (3.11) can be expanded considering the expressions for conduction (3.5) and switching (3.10) losses for an IGBT or diode die k:

$$\begin{aligned} P_{L\,k} &= \left(V_{0\,k} + V_{1\,k}T\right) I_{avg\,k} + \left(R_{0\,k} + R_{1\,k}T\right) I_{rms\,k}^2 \\ &\quad + E_{Total\,k}\left(I_{rms\,k}\right) \frac{v_C}{V_{CE}^{ref}} f_{sw} \end{aligned} \tag{3.20}$$

Replacing (3.16) - (3.18) into (3.20) and (3.2.1) and rearranging the resulting equation as a function of the temperature yields a direct expression for the calculation of the die temperature:

$$\begin{aligned} T_{J\,k} &= \frac{R_{th\,k}\delta_k \left(V_{0\,k} i_{dc} + R_{0\,k}\left(i_{dc}^2 + \frac{i_{ac}^2}{2}\right)\delta_k\right)}{1 - R_{th\,k}\delta_k \left(V_{1\,k} i_{dc} + R_{1\,k}\left(i_{dc}^2 + \frac{i_{ac}^2}{2}\right)\delta_k\right)} \\ &\quad + \frac{R_{th\,k}\delta_k \left(\left(E_{0\,k} i_{dc} + E_{1\,k}\left(i_{dc}^2 + \frac{i_{ac}^2}{2}\right)\delta_k\right)\frac{v_C}{V_{CE}^{ref}} f_{sw}\right) + T_a}{1 - R_{th\,k}\delta_k \left(V_{1\,k} i_{dc} + R_{1\,k}\left(i_{dc}^2 + \frac{i_{ac}^2}{2}\right)\delta_k\right)} \end{aligned} \tag{3.21}$$

Where the time index is omitted for clarity and the thermal impedance is represented by the steady-state value of the thermal resistance. The individual temperatures for Q1, Q2, D1 and D2 can be obtained by replacing (3.19) into (3.21).

The ambient temperature T_a is the reference point to which the junction temperature T_J is calculated, as the result of the semiconductor die losses P_L flowing through the total thermal resistance R_{th} between the junction and the ambient. Equation (3.21) can therefore be applied for the calculation of a die temperature from a temperature measurement T_a located in the thermal path, and to which R_{th} is referred to, e.g. heat sink.

3.3 Junction Temperature Acquisition and Estimation

3.3.1 Challenges and Requirements

A key challenge in the realisation of active thermal control and condition monitoring systems is the accurate measurement of junction temperature [171]. Sensing junction temperature during converter operation is not trivial and the selection of an estimation method must be made with careful consideration. The main challenges in the selection or design of a temperature measurement system are [172, 173]:

- Temperature point or distribution, i.e. single location or ability to detect non-uniform temperature distribution in a die and between different power dies;
- Access/modification of the device, as direct access to dies is prevented by the dielectric gel and the module packaging;
- Noises and environmental disturbances, e.g. adverse electromagnetic interference (EMI) environment;
- Performance degradation, if the measurement system introduces degradation in converter performance;
- Sampling rate and resolution, i.e. data sampling every millisecond or once per day.

The identification of the constraints and requirements of the temperature measurement system will lead to a choice that falls within one of the following families of methods [12, 174, 175]: Optical Methods, Physical Contact Sensors, Thermal Model-based Methods and Thermo-Sensitive Electric Parameters (TSEPs).

3.3.2 Junction Temperature Estimation

3.3.2.1 Optical Methods

These methods rely on the temperature-dependent optical properties of semiconductors and many indicators can be found, such as luminescence, Raman effect, refraction index [174], reflectance [176], or laser deflection [177–179]. Frequently, infrared (IR) radiation

variation with temperature is employed, e.g. local IR sensors [180–184], IR microscope [185, 186] and IR cameras [180, 187–191].

The main advantage of the IR camera and the thermo-reflectance techniques is the possibility of obtaining a temperature distribution of the power device [12]. This is demonstrated in Figure 3.8 for the surface temperature measurement of an IGBT, where the non-uniform temperature distribution inside a semiconductor module is clearly observable.

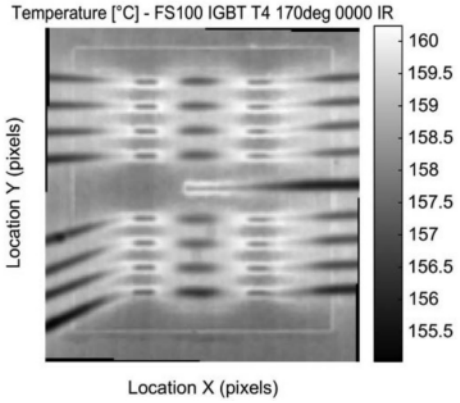


FIGURE 3.8: IR temperature measurement of an IGBT module [10].

The IR microscope [185] and the 2-D radiometry [181, 182] also allow for thermal mapping of the semiconductor device and the laser deflection technique [177–179] can be used to measure the temperature gradients directly inside the power semiconductor.

The measurement time when these methods are employed is generally not higher than a few milliseconds due to the electronic processing [173]. However, modification of the power module is required as the chip has to be seen by the optical system and the polymer package and the dielectric gel have to be removed [12]. This not only excludes their application from high-voltage systems but also makes them impractical for online monitoring

3.3.2.2 Physical Contact Sensors

Temperature measurements can also be obtained by making direct contact with the chip with a thermo-sensitive material such as solutions using liquid crystals or thermographic phosphors [174]. The main methods are optical (thermal) fibres, thermocouples and thermistors

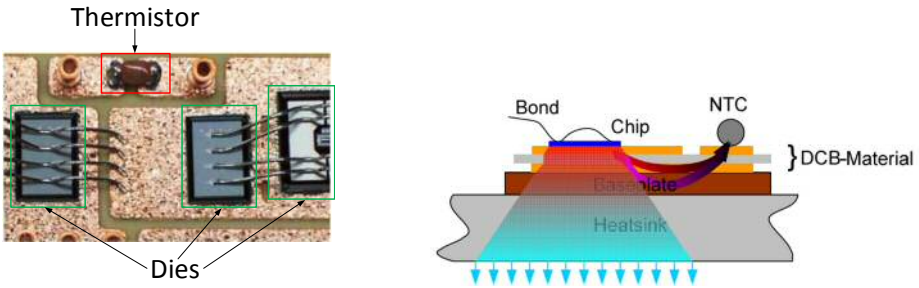
Temperature measurements by optical fibers in direct contact with the power chip [192, 193] only provide a local measurement but allow these components to be employed without the need to remove the dielectric gel. Typically, less accurate thermocouples with external diameters of hundreds of micrometers are glued or soldered onto the chip surface [184, 194–196]. These methods have the advantage of requiring limited modification to device and are suitable for long term online monitoring. They possess a low cost and the flexibility of providing a measurement of not only junction temperature but the temperature of any point of the device on which they are installed. However, they possess a relatively slow response time (thermocouple: s, thermal fibre: ms) and are rather sensitive to noise and EMI [172]. More accurate methods use small size microprobes [197], which lead to a low thermal capacitance and allow fast measurements without heat transfer disturbances.

Direct access to semiconductors junction temperature is not possible without complex methods requiring sensors mounted on the chip, e.g. soldering the gate-resistor directly onto an IGBT chip and using the temperature dependence of its resistance to evaluate the semiconductor temperature [184], or even being part of it, reducing the active area that contributes to the die's current carrying capabilities [198]. This limits the application of the chosen temperature measurement method to a more convenient point, such as the semiconductor module case or heat sink.

A common approach followed by some manufacturers is the inclusion of temperature sensors, typically thermistors, in the close proximity of the silicon die [9, 199], as illustrated in Figure 3.9 (a). The thermistor, also known as negative temperature coefficient (NTC) resistor is a resistive element whose resistance value depends on its temperature: by knowing its characteristic curve, the resistance value can be converter to an equivalent temperature. The measured value typically reflects the Case temperature and allows the elimination of the low-pass filtering action of the thermal network between the silicon and any other accessible points outside the module such as the heat sink or the coolant temperature. Nonetheless, as it is a single point measurement and does not correspond the required junction temperature, a calculation process, e.g. by employing (3.21), must be implemented in order to obtain a value for the junction temperature.

As shown in Figure 3.9 (b), the majority of heat generated in the chip flows directly to the heat sink, and only part of it flows towards the thermistor position. As this

does not flow instantaneously, the thermistor is only suitable to represent the baseplate temperature in static points of operation [11] and transient phenomena such as short circuit conditions can not be monitored or detected as the associated time constants are far too small. Nonetheless, they provide a simple and easy access to temperature information inside a semiconductor module.



(A) Location (B) Heat Flow

FIGURE 3.9: Thermistor-based temperature measurement in a semiconductor module [11].

3.3.2.3 Thermal Model-based Methods

Semiconductors junction temperature can be estimated based on the power losses [200, 201], detailed in subsection 3.2.3, and the device thermal model [163]. The combination of these two systems can underpin the construction of a state observer (SO) for on-line junction temperature estimation, without the need for additional hardware. A SO is a well-known process and has been used for several decades in state estimation problems. In the scope of temperature estimation, its flexibility enables its application in a broad range of areas, from supercapacitor strings [202] and lithium ion batteries [203] to induction hobs [204], heat exchangers [205] and motor stator windings [206]. In semiconductor power module applications, the literature has demonstrated the effectiveness of a SO in the study of thermoelectric ageing of power modules [207], as well as reduced thermal cycling in power electronic cooling [208] and overload monitoring in high power, high frequency converters [209].

The flexibility of a SO allows it to be used for unstable process plants and provide an accurate estimation when some of the measurements are missing. However, it relies on the premise that the parameters of the thermal network are known accurately, and the state matrix can be perfectly built to represent the system under study. When this information is not available, the SO can still be employed, but not until the process it

will be applied to is perfectly characterised, typically though the test and measurement of a large number of samples [204].

The generic structure of a SO is presented in Figure 3.10. If the device voltage v or current measurements i and duty cycle d are not measured directly, reference (i_{ref}) and estimated values ($\hat{v}$) can be used for loss calculation and the SO is said to be an open-loop SO. The application of this method to different topologies [163, 210] in experimental conditions [188, 200] have reported a T_J estimation error as low as 2 °C. However, since temperature feedback is not used (dashed T_f red line in Figure 3.10), the accuracy of temperature estimation can be affected by disturbances in the plant.

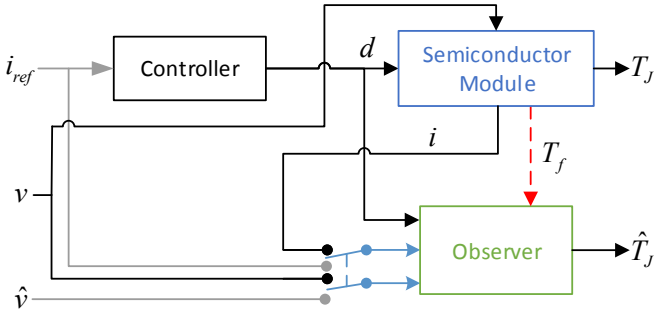


FIGURE 3.10: SO-based junction temperature estimation in a semiconductor module [11].

To overcome this, a closed-loop SO can consider feedback information from the semiconductor power module, e.g. temperature T_f in Figure 3.10, corresponding to the module baseplate temperature [211], which can be used to update the device thermal model. The disturbance rejection bandwidth of this method is limited by the bandwidth of the feedback temperature signal [212], which can be obtained from various types of sensors, such as the ones presented in subsections 3.3.2.1 and 3.3.2.2.

The variation of the loss model as the semiconductor module ages has been demonstrated in [213] to result in erroneous junction temperature estimations. However, since temperature feedback is used for a closed-loop SO, this problem is only important if an open-loop SO is employed. This also means that junction temperature estimation methods based on power dissipation models become less accurate as the package and the semiconductor die age, although monitoring solutions to overcome this limitation have also been proposed [214, 215].

Alternatively, a Kalman filter can also be used. The Kalman filter [216] is a model-based approach that also relies on the thermal and power loss models of a semiconductor

module to provide a junction temperature estimation. Based on available voltage and current measurements, power losses are calculated and used as an input to the filter.

The adaptive property of a Kalman filter allows accurate estimates of junction temperature to be obtained in the presence of ageing effects and variable cooling conditions [217]. In addition, the quality of the estimate can be assessed through the examination of the model residual error, which provides a mechanism for detecting changes in the thermal path. This enables the method to be immune to semiconductor's ageing effects, allowing it to also be used in condition monitoring of power semiconductor devices [215].

3.3.2.4 Thermo-Sensitive Electric Parameters (TSEPs)

Recent semiconductor devices temperature evaluation techniques rely on electrical methods to overcome the need of visual or mechanical access to the die, required by the aforementioned methods. As electrical properties of the dies are used to determine the temperature, the dies are, in a way, the temperature sensor themselves, and the temperature can therefore be evaluated using only voltage and current measurements on packaged devices [12].

Various classifications of existing TSEP-based methods have been proposed [12, 172, 174, 212], each of them using different and not unanimous criteria and the general classification proposed in [172] is followed and improved in this thesis. Although typically IGBTs and diodes are employed in VSC-HVDC applications, temperature estimation methods for other devices such as metal–oxide–semiconductor field-effect transistor (MOSFETs) and bipolar junction transistors (BJTs) are also included. This is because particularly suited methods for these devices share the same principles used in the junction temperature measurement of IGBT and diode dies.

TSEP-based methods for junction temperature measurement can be classified as belonging to one of the following categories:

- Classic TSEPs:
  - Voltage drop at low current;
  - Saturation current;
  - Short-circuit current;

- Static characteristic-based TSEPs;
- Dynamic characteristic-based TSEPs:
  - Measurement at device turn-on or turn-off;
  - Measurement of duration.

Classic TSEPs

- Voltage drop at low current

This family of methods refers to commonly used TSEPs for temperature measurement. One of these methods is the voltage drop at low current. This method enables junction temperature to be measured by establishing a relationship between this parameter and the device voltage, e.g. collect-emitter voltage (V_{CE}) of an IGBT, when the device output current is close to zero [213, 218]. Typically values up to hundreds of milliamps are used [12], which takes advantage of the linear dependency of silicon-based devices with temperature [219]. This approach is frequently used in power electronic applications because almost all devices have a p-n junction in their structure [213, 218, 220–222]). It can therefore be used in forward-biased diodes [222–226], MOSFETs in the OFF-state [227], base-emitter junction of BJTs [228] and IGBTs [187, 225, 229–232]. A typical set of resulting relationships from the application of this method is shown in Figure 3.11.

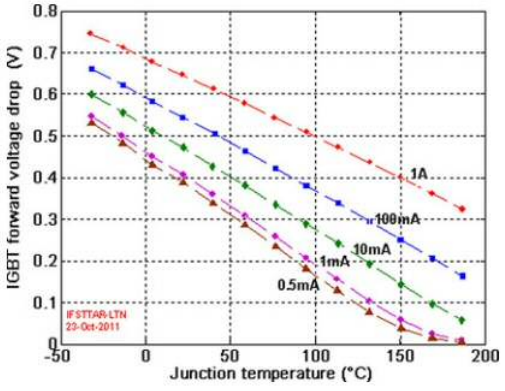


FIGURE 3.11: IGBT forward voltage drop as a function of the device temperature for different measured currents [12].

A key consideration in the implementation of this method is the choice of an appropriate measurement current, whose magnitude can vary greatly according to the rating of the device, and can influence severely the quality of the temperature measurement [223].

For power converters with a high number of semiconductors, high-resolution voltage sensing and high-voltage isolation for each switching semiconductor are required, which can significantly increase the volume of the converter [212]. This is due to the need of the voltage sensing circuit to have galvanic connection to the power terminals of the device (collector and emitter for IGBT, drain and source for MOSFET). As a result, challenging conditions arise for accurate temperature measurement due to thermal and EMI issues.

This method has simple computational requirements and since the frequency of the converter load current is much slower than the converter switching frequency, high-bandwidth current measurement is not required. The voltage sensing bandwidth will determine the temperature measurement bandwidth, which is generally higher than 100 kHz [233].

- Saturation current

For IGBTs (MOSFETs), it is possible to use the saturation current under a given gate-emitter (gate-source) and a given collector-emitter (drain-source) voltages [187, 222, 234]. This approach relies on the temperature dependence of electron mobility and threshold voltage of the device and not on its voltage [235]. The main requirement of this method is the need of a current sensor able to measure a low current level in order to have accurate temperature measurements [236].

- Short-circuit current

The possibility to induce a hard switching fault to create a short-circuit and its relation with temperature has also been studied in [237]. The main drawback of this method is the resulting high thermal dissipation during the short circuit, which can lead to the thermal runaway of the device, as well as premature device degradation. Furthermore, additional components are necessary for the implementation of this method, although its validity has been demonstrated in multiple semiconductor applications [237].

Static characteristic-based TSEPs

A straightforward way to estimate the junction temperature of a device is to consider simultaneously the static relationship between the temperature, its forward voltage and

the current crossing it. In this method, a high current is injected into the power device and the evaluating parameter is either the ON-state drain–source voltage for MOSFETs [233, 238, 239], the ON-state V_{CE} for IGBTs [191, 240–243] or the forward voltage V_f for diodes [241, 244, 245]. The measured voltage is largely dependent on the current value and a calibration step is often carried out to obtain the static current–voltage characteristic of the semiconductor device as a function of temperature [12].

The sensitivity of this method depends largely on the current magnitude and appears to be especially suited for online temperature measurement [238, 240, 241]. A floating-voltage sensor with good resolution and enough voltage stress rating is necessary for the voltage measurement. The measuring circuit has to allow for accurate measurements at low voltage (when the device if ON) and has to be protected against high system voltages (when the device is OFF), which is typically achieved through the use of specific circuits [238, 240].

The accuracy of the temperature measurement can be affected by the noise generated by the power converter due to a low sensitivity of the voltage variation with temperature [212]. It can also be aggravated by magnetic components in the power converter and parasitic resistances that lead to additional voltage drops on the bond wires [246, 247]. Although the latter can be corrected by evaluating the packaging geometry and the location of the semiconductor chip [247], the degradation and the failure of the bond wires can make the correction inaccurate as the devices age [10].

Dynamic characteristic-based TSEPs

This family of methods provides temperature estimation by measuring dynamic parameters of the power devices.

- Measurement at device turn-on or turn-off

The turn-on delay of the gate-emitter voltage V_{GE} has also been reported as being temperature-dependent [248–250]. This delay increases linearly with the temperature and a sensitivity of 2 ns/°C was reported in [249]. This is a delicate measurement because of the very short time span [12] and an increase in the gate resistance value in order to increase the switching time when a temperature measurement is required has been

suggested in [248]. The turn-on delay measurement is a very interesting TSEP as it not influenced by the current value but it is greatly affected by parasitic elements.

The turn-off delay can also be used as a thermo-sensitive parameter [249–251], with a similar sensitivity to that obtained with the turn-ON delay and the collector current slope variation with temperature during the turn-on has also been reported [249, 250, 252]. However, these methods are less interesting because the measured time depends greatly on the collector current before switching and on the voltage [249].

This family of methods is constrained by the need for very fast current sensors due to the temperature sensitivity being on the range of nanoseconds or even picoseconds, per degree [172]. One possible solution to overcome this problem is to observe changes in these electrical parameters indirectly, e.g. through the monitoring of harmonics in the output current that indicate changes in the IGBT turn-off mechanism due to its relationship with temperature [224].

The interaction between the switching semiconductor and its gate drive system has also been explored as a method for temperature measurement [212]. The dependency of the gate drive turn-on output transient current peak value, as well as its integral [253], on the temperature has been applied on both MOSFETs [254] and IGBTs [253, 255]. Only access to the semiconductor gate and power terminals (MOSFET drain and source or IGBT collector and emitter) is required and a sensitivity of 2.4 mA/°C was reported in [254]. It has also been shown that the sensitivity value depends on the gate drive topology used [256].

- Measurement of duration

Temperature estimation based on measurements during switching is underpinned by three different principles: Miller plateau, turn-off delay time and switching time duration.

It was shown in [257] that the Miller plateau width of the gate-emitter voltage V_{GE} during the IGBT turn-off is temperature-sensitive. For different IGBT modules, a temperature variation of 1 °C can cause a Miller plateau duration change in the order of 0.8 ns to 3.4 ns [257], which requires accurate time counters for appropriate online temperature measurement.

Also during an IGBT turn-off transient, the induced voltage between the Kelvin emitter and the power emitter (V_{eE}) has two spikes. The delay time between the these spikes ("V_{eE} delay time") has also been reported [258, 259] to be temperature-dependent, with a sensitivity of 8 ns/ °C. When this method is applied to parallel-connected power semiconductor dies, unbalanced circuit layouts in the power module can cause an unbalanced current sharing during the turn-off transient and distort the total V_{eE} waveform [187] and the resulting temperature measurement.

IGBT switching times have been shown to be temperature dependent [260, 261] and the turn-off time has been analysed in [262, 263] for online temperature estimation. The temperature-dependency of an IGBT V_{CE} during the turn-off transient has been examined in [262, 263] and it was shown that larger turn-off times and smaller dV_{CE}/dt values are observed for higher temperatures. This relationship has a sensitivity of 3 to 4 $\mu s/°$C and is independent from the voltage or load current magnitudes.

Temperature estimation methods based on measurements during switching require high-bandwidth voltage comparators and high-resolution time counters [212]. Consider that the voltage measurements in [257, 259, 263] use the IGBT emitter as voltage reference, the temperature measurement circuit and the device gate drive system can share the same isolated power supply [212]. The method based on the Miller plateau [257] relies on the measurement of V_{GE}, allowing the measurement circuit to be integrated into the IGBT gate drive. The method based on the turn-off delay time [258, 259] needs to have access to both Kelvin emitter and power emitter, and the method based on the switching time duration [263] requires galvanic connection to the IGBT collector and emitter. Thus, the measurement circuits are likely to be embedded inside of or be placed very close to the power module and will, therefore, be sensitive to switching noise and EMI.

3.4 Summary

This chapter presented an overview of the electro-thermal dynamics of semiconductor devices and detailed a loss calculation process particularly suitable for MMCs. A literature review on different junction temperature estimation methods is presented, including an

analysis of the requirements of each method, as well as the challenges of their practical implementation.

TSEPs are presently regarded as the most promising methods for temperature estimation during the operation of a power electronic converter as they can be implemented using only voltage and current measurements on packaged devices. However, complex measurement circuitry that requires the modification of the structure or operation of the converter is often required, together with calibration and compensation procedures. This makes TSEPs less attractive than "off-the-shelf" solutions such as thermistors, although improvements on die temperature estimation using TSEPs are expected to be obtained in the future.

For applications employing hundreds or thousands of switching semiconductor devices such as MMCs, the feedback of some or all devices temperatures to the control cabinets for monitoring purposes can appear daunting. This is especially important where the dies are subjected to asymmetric operating conditions and are, therefore, expected to have different temperature distributions within an arm and a phase leg. However, in industrial applications the status of each semiconductor device is passed to the control level for monitoring and protection reasons [264]. Thus, the feedback of a large number of individual semiconductors temperatures to the converter control is not expected to pose a problem, even for systems employing a large number of semiconductor devices such as MMCs.

Chapter 4

Operation of Modular Multilevel Converters with Dynamic Rating Strategies

4.1 Introduction

Unlike other power system components such as large synchronous generators, lines or transformers, semiconductor switches utilised in MMCs possess a very short thermal time constant and therefore have a very limited overload capability. To avoid over-temperature stresses, a fixed current limit is normally implemented in the converter control system. This can be regarded as a conservative choice in that it sets the maximum power contribution from the converter, without the possibility to temporarily provide an overload capability.

In order to extend the power transmission capacity but keep the temperature of semiconductor switches within safe limits, an additional control loop is presented in this chapter. In the control loop, the current limit is dynamically set in response to the measured semiconductors temperature according to two different rating strategies. The proposed control scheme exploits the available semiconductors thermal headroom to enforce a current magnitude limit that ensures the electrical and thermal limits are kept within safe bounds. Eigenvalue analysis is performed to analyse the stability of the proposed strategies and the thermal headroom is explored to enhance the performance

of a MMC under two critical operational scenarios: cooling system failure and current overload. The current overload capability is explored to improve the frequency response from a power distressed AC grid and simulation results for the rating strategies are presented and compared for an MMC with 3 SMs per arm.

4.2 Temperature Control Strategies

4.2.1 Semiconductor Limitations

The limiting factor in providing current overload capability is the possible over-temperature damage to semiconductors. Although converter overload needs to take into consideration other components in the system, such as bushings and cables, line rating systems are normally implemented and provide real-time feedback about the power transmission limit of the system [265–267].

The short thermal time constant of semiconductor devices limits their capacity to operate in an overload mode. This is especially critical for IGBT-based VSCs, notoriously less robust against fault and overload currents than thyristor-based LCCs. To avoid IGBT over-temperature stresses a fixed current limit is normally implemented in the converter control system, as shown in Figure 2.9. The use of a conventional fixed (nominal) current limit I_{nom} restrains the maximum current that can flow through the semiconductor dies, defining an operational area, for a given semiconductor operating voltage, as shown in Figure 4.1. This limit is set low enough that the nominal operating junction temperature $T_{J(nom)}$ of the semiconductor dies in the IGBT modules is never violated, even under worst-case operating conditions (e.g. high system voltage and high ambient temperature). However, during other operating conditions (e.g. nominal system voltage and low ambient temperature), the limits prevent the full capability of the converter from being used, e.g. to support a power distressed grid [35]. An example is the Storebælt HVDC interconnection (LCC-based), which, with redundant cooling in operation, is designed for [36]:

- Continuous operation at 105 % rated load;
- Operation at 110 % rated overload for 2 hours;

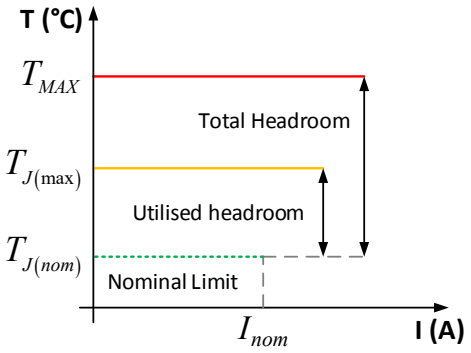


FIGURE 4.1: Influence of the maximum operating temperature on the semiconductor thermal headroom.

- 3 second overload capability of 135 % rated load.

These values are quite modest, even for robust overload and fault-tolerant devices such as thyristors.

4.2.2 Conventional Control Strategies

The aim of active thermal control strategies is to regulate semiconductors' junction temperature by modulating one or more control signals. For the thermal control of 2- and 3-level VSCs, the frequency of the PWM scheme is normally changed in order to limit the maximum junction temperature [268–271] and reduce thermal cycling [211]. Further approaches aiming at loss reduction for temperature control have addressed changes between continuous and discontinuous PWM schemes in [272, 273], but their general application needs to be carefully considered due to the large impact in the current ripple.

These approaches adopt a system-level control of the switching frequency with inherent processing delays, generally in the order of a few milliseconds [274]. More advanced applications benefited from the smallest accessible time constants by employing direct gate driver control [273, 275–277], with the potential to reduce the thermal cycling by increasing the power losses also being explored.

Although providing effective alternatives for the active thermal control of 2- and 3-level topologies, the previous approaches are inappropriate for MMC applications for two fundamental but closely related operating reasons. The first concerns the very low switching

frequency of the PWM scheme, in the order of a few hundred Hertz, with little room for further reduction. This low switching frequency is one of the advantages of MMCs over previous 2- and 3-level VSC topologies, typically operating in the kilohertz range [271]. Furthermore, very low switching frequency [54] or even fundamental frequency switching schemes have been proposed [110–112, 278], invalidating the above-mentioned control approaches. The second reason is related to the modulation scheme itself. As the number of SMs increases, PWM-based schemes become cumbersome and more efficient approaches, such as the NLC method [95, 126] are more attractive. This method results in a low switching frequency for each SM, close to the reference waveform fundamental frequency. In other words, low switching frequencies make switching losses small [6, 118], hence in a MMC the temperature rise is almost entirely due to conduction losses. Subsequently, any active thermal control approach suitable for MMCs needs to, first and foremost, act on conduction losses in order to perform temperature control.

4.2.3 Proposed Active Thermal Control Concept

An enhanced operation can be achieved by exploiting the available thermal headroom between the nominal temperature limit $T_{J(nom)}$ and the maximum temperature T_{MAX} of the semiconductor devices, as shown in Figure 4.1. By allowing the converter to operate temporarily beyond its nominal limits, improved performance can be achieved by enabling advanced functionalities such as cooling system failure ride-through and temporary current overloads. Although additional operating limits could be attained by de-rating the converter with a (more) conservative current limit, this would also degrade performance. Since the electrical and thermal limits must be satisfied even under worst-case conditions, a more practical implementation is the control of the current limit, and a more robust operation can be achieved if the current limits are sensitive to semiconductors' junction temperature.

Considering a junction temperature $T_{J(0)}$ resulting from a given current I_0 flowing through the hottest semiconductor die in the converter, as shown in Figure 4.2, the utilisation of a fixed limit would limit the overload current set-point I_1 to the nominal value I_{nom}. By enabling the current limit I_{lim} to be defined as a function of the temperature, the new current set-point I_1 request at $t = t_0$ is initially met, leading to an increase in the value of the junction temperature. As the temperature increases and

approaches $T_{J(max)}$, the current limit is decreased accordingly, regulating the value of the overload magnitude I_1 to the nominal value I_{nom}, until an equilibrium is reached at $t = t_{ov}$. The duration $t = t_{ov} - t_0$ (shaded are in the top graph of Figure 4.2) corresponds to the operation of the converter in an overload mode.

The current limit for a basic dynamic rating strategy can be defined as:

$$I_{\text{lim}}\left(T_J\right) = I_{nom} + k\left(T_{J(nom)} - T_J\right) \tag{4.1}$$

Where T_J is the maximum estimated temperature of all the dies is all the SMs; I_{nom} is the nominal current limit, i.e. the design current of the system. $T_{J\,(nom)}$ is the nominal (threshold) operating temperature of the IGBT and is chosen in order to take into account the long term reliability of the semiconductors. k, defined in [A/°C], is the temperature-current droop constant, which determines the decrease in the current limit per unit increase in junction temperature. k is defined so that the current limit is zero when the maximum temperature $T_{J\,(max)}$ (the upper limit of the thermal headroom) is reached, i.e. $I_{\text{lim}}\left(T_{J\,(max)}\right) = 0$. Thus

$$k = \frac{I_{nom}}{T_{J\,(max)} - T_{J\,(nom)}} \tag{4.2}$$

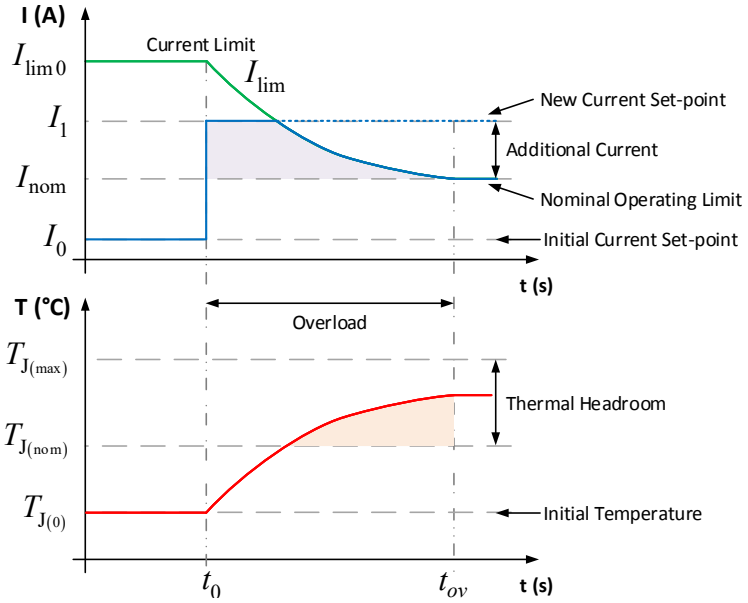


FIGURE 4.2: System response to a current order step with fixed and dynamic current limit with junction temperature feedback.

The nominal point corresponds to the maximum continuous operation point of the converter, which typically corresponds to 1.05-1.2 pu of the rated load [36]. This value is defined so that the resulting operating (nominal) temperature is below the maximum possible operating temperature of the semiconductors in order to guarantee a safety margin for transients such as SM bypass and faults.

The current limit variation as a function of the temperature, defined by (4.1), is shown in Figure 4.3, where the nominal current limit I_{nom} is bound to the nominal temperature $T_{J\,(nom)}$. Since the current limit should not be restricted at this operating point, the slope of the current limitation, i.e. k, is defined by the maximum temperature $T_{J\,(max)}$, as shown by the dashed lines in Figure 4.3. The lower the maximum temperature, the faster the current limit decreases (increases) for temperatures higher (lower) than $T_{J\,(nom)}$.

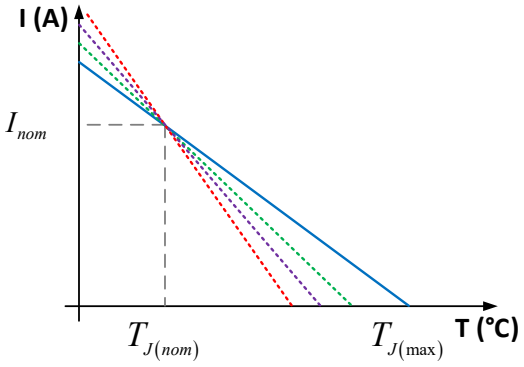


FIGURE 4.3: Influence of the maximum allowed temperature on the dynamic current limit.

In practice, the association of a particular $T_{J\,(nom)}$ with I_{nom} is unrealistic since the temperature at a given current depends on other factors such as ambient and coolant temperatures and thermal resistance of the semiconductor modules. These factors change as the modules ages, e.g. due to the formation of thermal voids in the solder layer of the module [214]. These parameters are not directly included in (4.1) and affect the value of the temperature even if the current through the dies does not change.

The current limit defined by (4.1) will try to keep the converter operating closely to $\left(I_{nom}, T_{J\,(nom)}\right)$, for any other operating conditions exceeding these values. This means that excursions from this operating point are limited and the provision of overload capability is reduced, both in duration and magnitude, as shown in [279]. Furthermore, for a given increase in the current order above the nominal value or an external temperature

disturbance leading to a current reduction, the upper limit of the operational headroom cannot be directly controlled using the current limit defined by (4.1). This violates a key aspect of the proposed active thermal control concept that only part of the total headroom is utilised as under normal operating conditions a certain headroom must be respected to enable semiconductors to survive phenomena such as voltage and current surges resulting from SM bypass and fault ride-through [145, 148].

4.2.4 Dynamic Rating Strategy A: Proportional Current Control

A proportional-type control strategy is shown in Figure 4.4, where the current limit I_{lim}^{A} is defined as:

$$I_{\text{lim}}^{A}\left(T_J\right) = k_p\left(T_{J(max)} - T_J\right) \tag{4.3}$$

k_p is the temperature-current droop constant and $T_{J\,(max)}$ is the upper limit of the utilised thermal headroom. Unlike the control law (4.1), proposed in [279] and illustrated by the solid line in Figure 4.4, the new control law in (4.3) is more flexible since it only responds to the difference between the input maximum die temperature and its maximum permitted value, i.e. it is not bound to a specific $\left(I_{nom}, T_{J\,(nom)}\right)$ operating point.

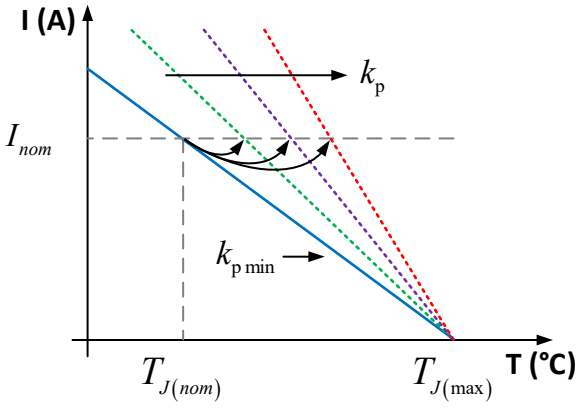


FIGURE 4.4: Shift of the maximum operating temperature at nominal current with increasing proportional gain.

To avoid current limitation at a given nominal point, the gain k_p should be set for a minimum value

$$k_{p\,min} = \frac{I_{nom}}{T_{J\,(max)} - T_{J\,(nom)}} \tag{4.4}$$

which is the same as the droop value determined by (4.2). Since the objective is to not exceed $T_{J\,(max)}$, k_p can be increased, allowing not only for the maximum temperature to not be reached, but also shifting to higher values the temperature at which current limitation occurs, i.e. $I^A_{lim} \leq I_{nom}$, as shown in Figure 4.4, allowing the converter to operate in a permanent current overload mode within the utilised thermal headroom region.

Since I_{nom} and $T_{J\,(nom)}$ are no longer coupled for $k_p \geq k_{p\,min}$, the current limit is more flexible and the temperature can vary by greater amounts than when (4.1) is utilised, without having the current limited, i.e. it allows a more generous current to be injected for a given nominal temperature. Accordingly, for any $k_p > k_{p\,min}$, the current limit will always be higher than I_{nom}, and higher current overloads will be permitted. The full utilisation of the thermal headroom (enabling higher overloads) becomes, therefore, dependent on the choice of a high gain k_p, which also increases the sensitivity of the current limit to measurement errors and noise.

4.2.5 Dynamic Rating Strategy B: PI-based Current Control

This strategy aims to overcome the limitations of having to employ a high gain for a better utilisation of the thermal headroom by regulating the current limit with temperature feedback through a PI controller. The control law is now given by:

$$\begin{aligned} I^B_{\text{lim}}\left(T_J\right) = K_P\left(T_{J(max)} - T_J\right) + \\ K_I \int \left(T_{J(max)} - T_J\right)\, dt \end{aligned} \tag{4.5}$$

where K_P and K_I are the proportional and integral gains, respectively, of the PI controller. The utilisation of the upper limit $T_{J(max)}$ of the headroom as a reference temperature allows the maximisation of the current limit, thus enabling current limitation to occur only when the temperature approaches $T_{J(max)}$ very closely. Hence, and unlike

Strategy A, a better utilisation of the headroom, i.e. permitting higher current magnitudes to flow through the semiconductors and ensuring the respect of the thermal limit, does not necessarily require a very high proportional gain.

4.3 Enhanced Current Control Loop with Temperature Feedback

The control strategies defined by (4.3) and (4.5) enable the current limit to be defined as a function of the temperature. However, this limit corresponds to the absolute value, i.e.

$$I_{lim} = \sqrt{I_{d\,lim}^{ref^2} + I_{q\,lim}^{ref^2}} \tag{4.6}$$

The individual limits for I_d^{ref} and I_q^{ref}, $I_{d\,lim}^{ref}$ and $I_{q\,lim}^{ref}$, respectively, depend on the high-level control set-points. These individual limits can independently share the new and temporary current limit provided by the rating strategies, which can be observed in Figure 4.5.

Considering two junction temperatures $T_{J\,A}$ and $T_{J\,B}$, where $T_{J\,A} < T_{J\,B}$, the absolute current limit is larger for $T_{J\,A}$, enabling a higher power transmission capability. However,

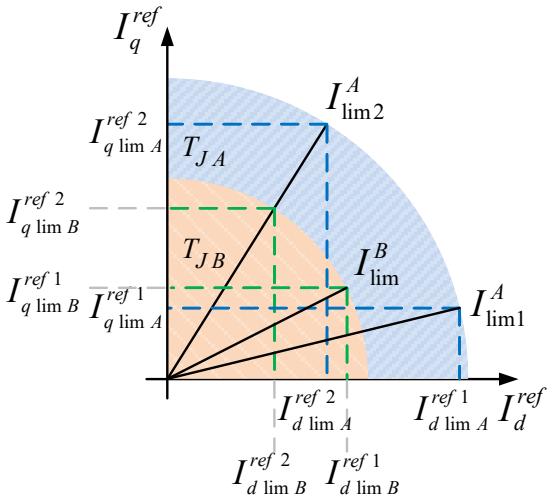


FIGURE 4.5: Extended current limit diagram with flexible limits for the current references ($T_j^A < T_J^B$).

for the same current limit, either $I^{A}_{lim\,1}$ or $I^{A}_{lim\,2}$ [1], the relative limits for I^{ref}_{d} and I^{ref}_{q} can also be extended and defined (e.g. sub-points "1" or "2"), according to the desired performance for the converter.

The active and reactive powers are regulated through the control of the active I^{ref}_{d} and reactive I^{ref}_{q} current components, respectively. For sub-point "1" ($I^{A}_{lim\,1}$), $I^{ref\,1}_{d\,lim\,A}$ can be prioritised over $I^{ref\,1}_{q\,lim\,A}$ for an offshore wind farm-side converter, in order to maximise the transmitted active power and keep the reactive power at the minimum value required to regulate the AC voltage on the offshore hub. Alternatively, the reference currents for the active $I^{ref}_{d\,lim}$ and reactive $I^{ref}_{q\,lim}$ current components can be scaled proportionally to their original set-point values for sub-point "2" ($I^{A}_{lim\,2}$), i.e. the additional operational envelope is shared by both components, now being defined as:

$$\begin{cases} I^{ref}_{d\,lim} &= I^{ref\,2}_{d\,lim\,A} = \epsilon I^{ref\,2}_{d\,lim\,B} \\ I^{ref}_{q\,lim} &= I^{ref\,2}_{q\,lim\,A} = \epsilon I^{ref\,2}_{q\,lim\,B} \end{cases} \tag{4.7}$$

where

$$\epsilon = \frac{I^{A}_{lim\,2}}{\sqrt{I^{ref\,2^2}_{d\,lim\,B} + I^{ref\,2^2}_{q\,lim\,B}}} \tag{4.8}$$

The proposed control structure of the MMC, with the current limits being dynamically set as a function of the junction temperature, is presented in Figure 4.6. The active ($I^{ref}_{d\,lim}$) and reactive ($I^{sp}_{q\,lim}$) current component limits are applied to the set-point limits $I^{sp}_{d\,lim}$ and $I^{sp}_{q\,lim}$ from the high-level control of the converter, defining the final limits for the active $I^{ref}_{d\,1}$ and reactive $I^{ref}_{d\,1}$ reference currents. The remaining control blocks shown in Figure 2.9 remain unaltered.

Back-calculation anti wind-up method [280] is included in the active and reactive current PI controllers to avoid 'winding-up' when the dynamic limits are applied.

[1] The designation of the variables associated with temperatures "A" or "B" is independent from the designation utilised to differentiate the dynamic rating strategies defined by (4.3) and (4.5), respectively.

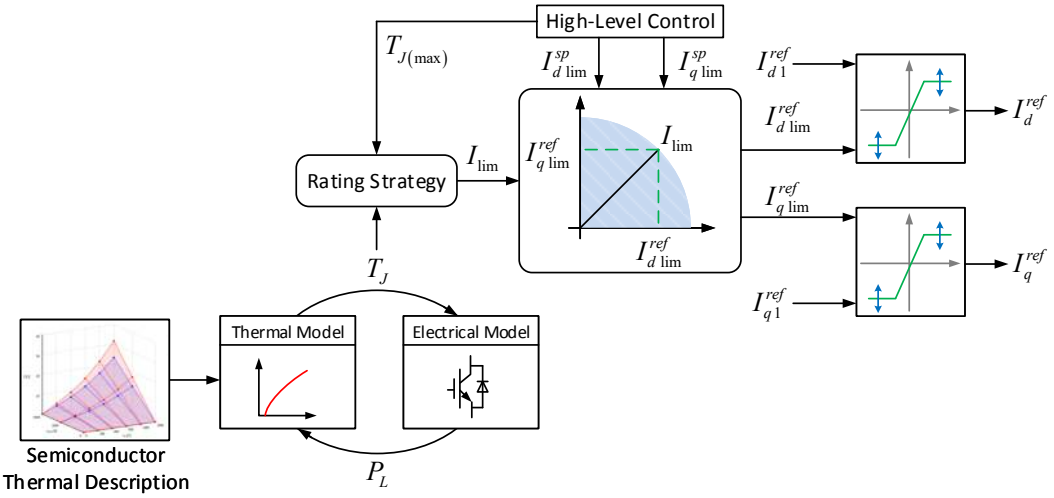


FIGURE 4.6: Current control structure of an MMC with dynamic current limits.

4.4 Transient Overload Capability of Semiconductors

The current overload enabled by the dynamic rating strategies can be explored to enhance the operation of converter This can be observed in Figure 4.7, where the nominal current limit I_{nom} defines the maximum (fixed) currents limit for the active $I^{ref}_{d\,lim\,1}$ and reactive $I^{ref}_{q\,lim\,1}$ current components. Assuming the reactive current component limit $I^{ref}_{q\,lim\,1}$ remains unchanged, the additional current injection capability provided by the new (and temporary) current limit I_{lim} can be utilised to increase the active current component limit from $I^{ref}_{d\,lim\,1}$ to $I^{ref}_{d\,lim\,2}$. In other words, the headroom can be used to temporarily increase the active current (power) injection of the converter; as the temperature starts to increase, $I^{ref}_{d\,lim\,2}$ is decreased back towards $I^{ref}_{d\,lim\,1}$.

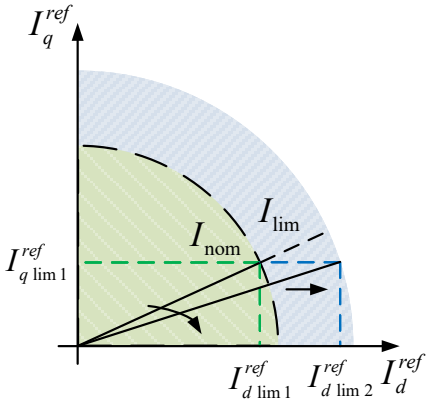


FIGURE 4.7: Maximisation of active current component with dynamic current limits.

Considering the operation in an overload mode, shown in Figure 4.8, it can be observed that the overload current command I_1 can have an arbitrary magnitude in the range between the nominal current limit I_{nom} and the initial current limit $I_{lim\,0}$ given by either (4.3) or (4.5). The shaded area corresponds to the transient overload capability of the converter, i.e. the temporary increase in current injection capability, enabled by the exploitation of the thermal headroom between $T_{J(nom)}$ and $T_{J(max)}$.

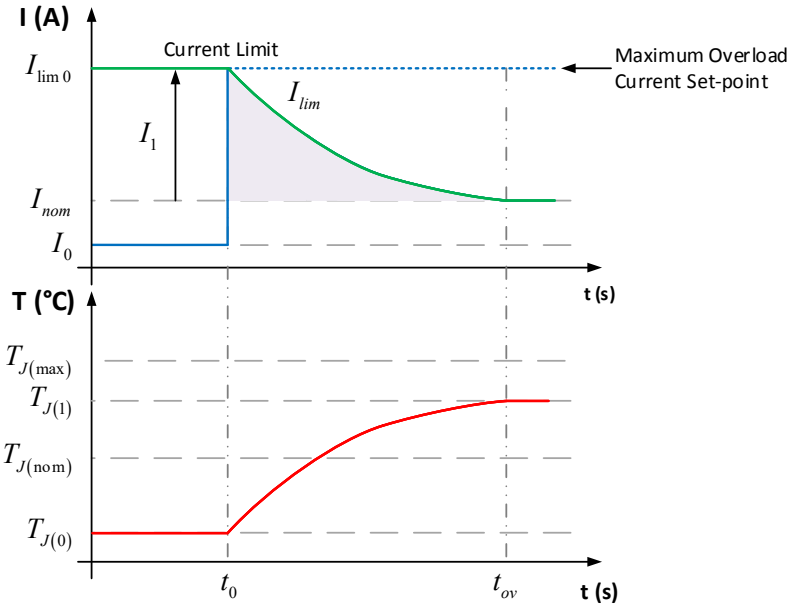


FIGURE 4.8: Transient current overload capability of semiconductors.

It can also be observed that the duration of an overload will depend on the magnitude of the associated overload current command and that lower current overload magnitudes lead to a slower temperature increase, hence longer overload durations.

The current limitation will act on the peak value of the 'ac' component of the arm current. Hence, the average 'dc' (i_{avg}) component is assumed to remain unchanged but not the rms value (i_{rms}), the calculation of which by (3.17) is now a function of either (4.3) or (4.5). The temperature variation over time will be introduced by the time constants in the impedance of the thermal network, according to (3.1), defining the time constant of the temperature increase. Combining (3.2.1) and (3.1) yields:

$$T_J\left(I_{lim}^{A/B}\right) = \sum_{i=1}^{m} R_{th\,i}\left(1 - e^{-\frac{t}{\tau_i}}\right) P_L\left(I_{rms}, T_J\left(I_{lim}^{A/B}\right)\right) + T_a \tag{4.9}$$

where T_J is the maximum estimated temperature of all the dies is all the SMs and the remaining variables necessary for its determination were omitted for clarity. Simultaneously, the temperature variation will define the current limit, either by (4.3) or (4.5). As shown in Figure 4.8, the equilibrium temperature $T_{J(1)}$ is reached at $t = t_{ov}$, when the current flowing through the semiconductors has been reduced to the nominal value I_{nom}:

$$I_{lim}^{A/B}\left(T_J\right) = I_{nom} \quad \wedge \quad T_J = T_{J(1)}^{A/B} \tag{4.10}$$

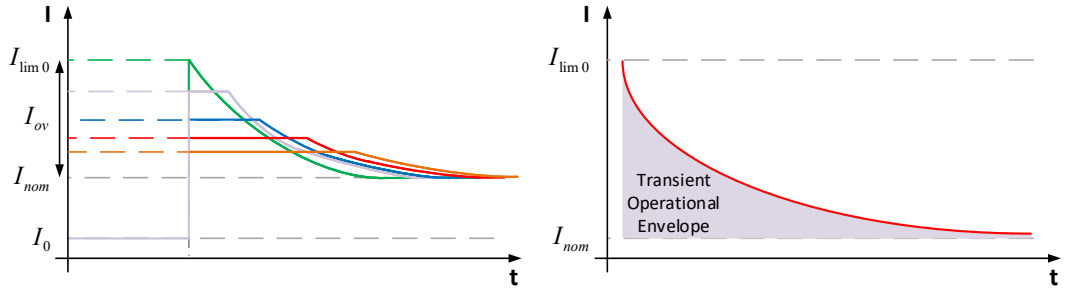
Eq. (4.10) can be rewritten as a function of the current limit at the equilibrium point and substituted in (4.9), yielding:

$$\sum_{i=1}^{m} R_{th\,i}\left(1 - e^{-\frac{t}{\tau_i}}\right) = \frac{T_{J(1)}^{A/B} - T_a}{P_L\left(I_{rms}, T_J\left(I_{lim}^{A/B}\right)\right)} \tag{4.11}$$

where $t = t_{ov}$. Eq. (4.11) allows the determination of the overload time for an arbitrary current overload limited by employing either A or B thermal control strategies. Given the interaction of the temporal variation of thermal impedances in the thermal network and the current regulation by the thermal control strategies, it is difficult to write (4.11) in a closed formulation for the calculation of the overload time, especially for strategy B, which includes an integral term. The overload time can, however, be determined numerically.

Using (4.11), all the possible overload magnitudes and their respective durations (I_{ov}, t_{ov}) can be mapped, as shown in Figure 4.9 (a), completely defining the transient operational envelope (TOE) of the converter, illustrated by the shaded area in Figure 4.9 (b). This area can be used to aid in the determination of the overload current set-points of the converter.

The TOE is defined by not only the semiconductor parameters, namely thermal resistances and time constants, but also the current overload capability and the parameters of the dynamic rating strategies, as defined in (4.11). It is, therefore, specific for a converter



(A) (B)

FIGURE 4.9: Transient current overload capability of semiconductors: (a) - Mapping of overload current magnitude (y-axis) for different overload times (x-axis) and (b) - TOE.

with a given nominal current employing specific semiconductor devices. The concept of let-through energy or "I^2t" value from fuses can be utilised to uniquely quantify the TOE and provide a transient overload energy (TOEn) figure of merit. The TOEn is defined as the extra thermal energy that the semiconductor switches can absorb during a current overload and can be used for the evaluation of different parameters utilised in the dynamic rating strategies.

Designating I_{ov} as the overload current magnitude (I_1 in the top graph in Figure 4.8), the overload current will have an exponential-like decay, which can be defined as:

$$I_{ov}(t) = I_{ov\,0} e^{-\frac{t}{\tau_{ov}}} \tag{4.12}$$

where $I_{ov\,0}$ is the initial overload current command and τ_{ov} is the overload time constant. Defining the time of the overload command request $t_0 = 0$ s and the overload time duration t_{ov}, the TOEn can be defined as:

$$TOEn = \int_0^{t_{ov}} I_{ov}^2(t)\, dt = \int_0^{t_{ov}} \left(I_{ov\,0} e^{-\frac{t}{\tau_{ov}}}\right)^2 dt = \frac{\tau_{ov} I_{ov\,0}^2}{2} \left(1 - e^{-\frac{2}{\tau_{ov}} t_{ov}}\right) \tag{4.13}$$

For $t_{ov} > \tau_{ov}$,

$$TOEn \approx \frac{\tau_{ov} I_{ov\,0}^2}{2} \tag{4.14}$$

From (4.13) and (4.14) it can also be observed that the TOEn will suffer a much smaller increase for an increase in the overload time constant than an increase in the overload current magnitude. The TOE can be exploited for system level benefits, such as the possibility of an extended power support to the system, e.g. improving the inertial response from the converter and the HVDC system, as seen from the AC grid.

For a given parametrisation of the dynamic rating strategies, the peak overload magnitude is essentially dependent on the specific properties of the semiconductors, namely their thermal resistances, as shown by (4.11). The overall current injection variation as a function of the overload duration, presented in Figure 4.9, is provided by the time constants of each section of the thermal network and its effect can be observed more clearly in Figure 4.10, where the TOEs for two systems, system A and system B, are shown.

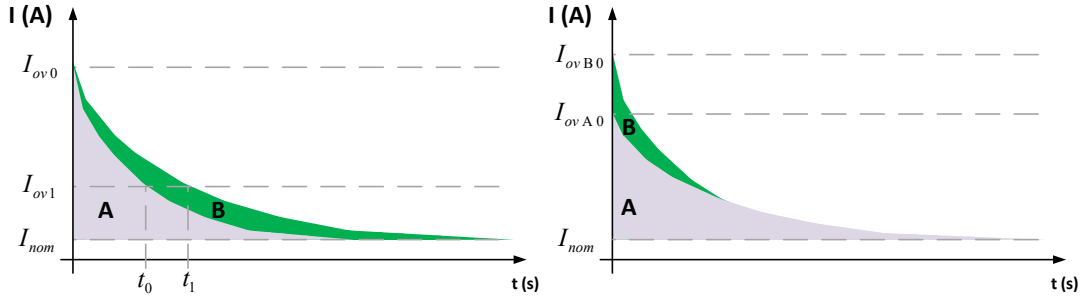


FIGURE 4.10: Influence of the system time constant on the transient current overload capability of semiconductors: (a) - Equal peak overload current magnitudes and (b) - Different peak overload current magnitudes.

Considering an overload current command $I_{ov\,1}$, as shown in Figure 4.10 (a), the duration of the current magnitude will be t_0 for system A and t_1 for system B. Recalling (4.12), the following relationship exists:

$$I_{ov\,1} = I_{ov\,0} e^{-\frac{t_0}{\tau_{ov\,A}}}|_{t=t_0} = I_{ov\,0} e^{-\frac{t_1}{\tau_{ov\,B}}}|_{t=t_1} \tag{4.15}$$

Eliminating common terms and rearranging results in:

$$\frac{t_0}{\tau_{ov\,A}} = \frac{t_1}{\tau_{ov\,B}} \tag{4.16}$$

which can be simply written as:

$$t_1 = t_0 \frac{\tau_{ov\,B}}{\tau_{ov\,A}} \tag{4.17}$$

From which it can be concluded that the TOE of a system can be effectively extended by increasing its time constant, which is mainly defined by the dominant (largest) time constant of a semiconductor thermal network. The benefit of possessing a large thermal time constant is clearly evident from (4.14), where it can be observed that the TOEn is directly proportional to the overload time constant.

The effect of the overload time constant can also be observed in Figure 4.10 (b), where systems A and B have different peak overload magnitudes of $I_{ov\,A\,0}$ and $I_{ov\,B\,0}$, respectively, but also different overload time constants.

Calculating the TOEn using (4.14) results in:

$$\begin{cases} TOEn\,A & \approx \frac{\tau_{ov\,A} I_{ov\,A\,0}^2}{2} \\ TOEn\,B & \approx \frac{\tau_{ov\,B} I_{ov\,B\,0}^2}{2} \end{cases} \tag{4.18}$$

Considering the higher peak overload magnitude for system B, the effect of the overload time constant can be explored to ensure $TOEn\,A > TOEn\,B$. For this, it is required that:

$$\tau_{ov\,A} I_{ov\,A\,0}^2 > \tau_{ov\,B} I_{ov\,B\,0}^2 \tag{4.19}$$

Defining $I_{ov\,B\,0} = \rho I_{ov\,A\,0}$ yields:

$$\tau_{ov\,A} > \rho^2 \tau_{ov\,B} \tag{4.20}$$

From (4.17) and (4.20) it can be concluded that larger time constants contribute directly to an improved semiconductors transient overload capability. Consequently, if semiconductors transient overload capability requirements are included at the design stage, the largest time constant of the system can be regarded as a design parameter. This can be controlled, for example, by employing large copper or aluminium heat sinks,

which possess a longer time constant compared to the temperature rise inside the power devices.

4.5 Stability Analysis

The exploitation of the semiconductors thermal headroom to extend the operational envelope of the converter depends on the choice of suitable control parameters, namely a high gain for Strategy A and proportional and integral gains selection for Strategy B. This choice must also ensure that undesirable phenomena such as temperature overshoot or unstable oscillations do not occur.

The rating strategies given by (4.3) and (4.5) establish a simple junction temperature feedback system, shown in Figure 4.11, combining the thermal model of semiconductors and the current limit regulation by the proposed dynamic rating strategies.

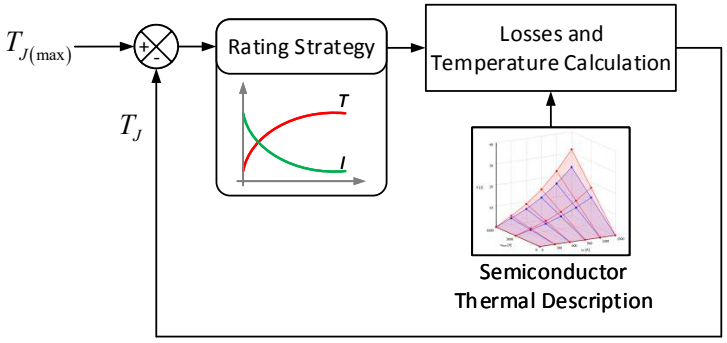


FIGURE 4.11: Simple closed-loop system for current limit regulation with semiconductors temperature feedback.

4.5.1 Thermal Model

Each SM semiconductor module is placed on a liquid-cooled heat sink with a regulated coolant temperature, as in practical applications, and the converter operates as an inverter. Considering the HB semiconductor module FF75R12YT3 from Infineon [9], the corresponding thermal network is illustrated in Figure 4.12, where the parameters are shown in Table 4.1. The datasheet parameters are provided in a Foster-type format, which have been converted to a Cauer-type representation [281].

Simulation studies have identified IGBT Q2 (cf. Figure 2.4 (a)) as the hottest die in the semiconductor modules, dictating the maximum temperature utilised to determine the

current limit, according to (4.3) and (4.5). Regarding the thermal network in Figure 4.12, that characterizes the semiconductor module considered in this work, and considering the heat flow energy balance from one thermal section to the other, the following equations apply for the thermal network associated with Q2 and highlighted in Figure 4.12:

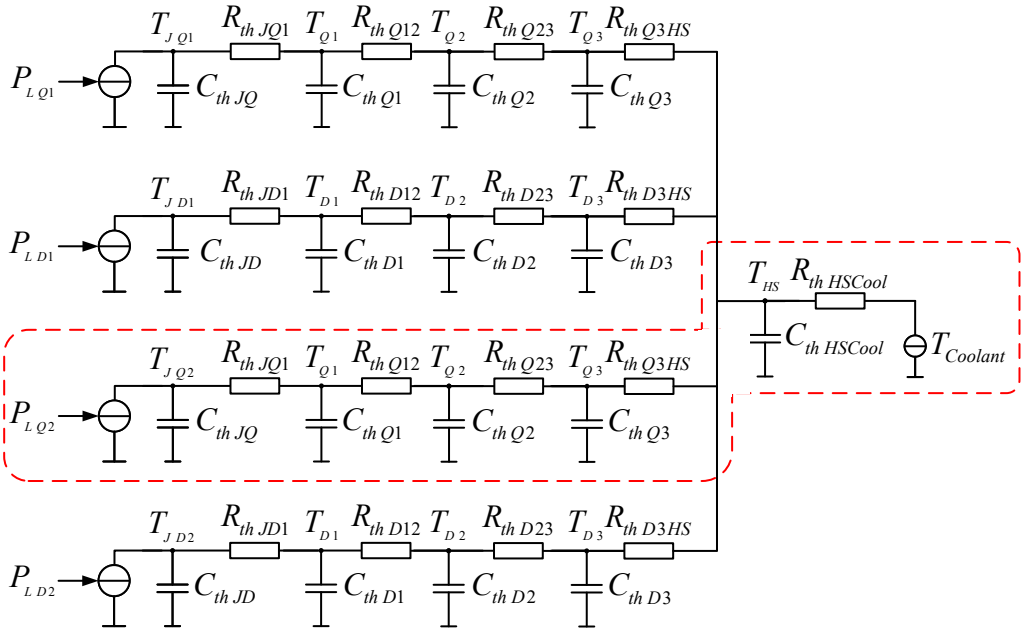


FIGURE 4.12: Cauer-type thermal network for HB semiconductor module Infineon FF75R12YT3 [9] mounted on a liquid-cooled Seat-Sink.

TABLE 4.1: Thermal network parameters for IGBT module Infineon FF75R12YT3 [9]

Section		1	2	3	4	5	Heat Sink	
Foster	R_{th} (°C/W)	0.01696	0.03021	0.16059	0.32224	$R_{th\,HS\,Cool}$ (°C/W)	0.45
	τ_{th} (s)	0.0005	0.005	0.05	0.2	$\tau_{HS\,Cool}$ (s)	5
Cauer	R_{th} (°C/W)	0.02896	0.0871	0.2647	0.1491		
	C_{th} (J/°C)	0.02239	0.08141	0.1429	0.9635		

$$\dot{T}_{J\,Q2} = -\frac{T_{J\,Q2}}{R_{th\ JQ1}C_{th\ JQ}} + \frac{T_{Q1}}{R_{th\ JQ1}C_{th\ JQ}} + \frac{P_{L\,Q2}}{C_{th\ JQ}} \tag{4.21}$$

$$\dot{T}_{Q1} = \frac{T_{J\,Q2}}{R_{th\ JQ1}C_{th\ Q1}} - \left(\frac{1}{R_{th\ JQ1}} + \frac{1}{R_{th\ Q12}}\right)\frac{T_{Q1}}{C_{th\ Q1}} + \frac{T_{Q2}}{R_{th\ Q12}C_{th\ Q1}} \tag{4.22}$$

$$\dot{T}_{Q2} = \frac{T_{Q1}}{R_{th\ Q12}C_{th\ Q2}} - \left(\frac{1}{R_{th\ Q12}} + \frac{1}{R_{th\ Q23}}\right)\frac{T_{Q2}}{C_{th\ Q2}} + \frac{T_3}{R_{th\ Q23}C_{th\ Q2}} \tag{4.23}$$

$$\dot{T}_{Q3} = \frac{T_{Q2}}{R_{th\ Q23}C_{th\ Q3}} - \left(\frac{1}{R_{th\ Q23}} + \frac{1}{R_{th\ Q3HS}}\right)\frac{T_{Q3}}{C_{th\ Q3}} + \frac{T_{HS}}{R_{th\ Q3HS}C_{th\ Q3}} \tag{4.24}$$

$$\dot{T}_{HS} = \frac{T_{Q3}}{R_{th\ Q3HS}C_{th\ HS\,Cool}} - \left(\frac{1}{R_{th\ Q3HS}} + \frac{1}{R_{th\ HS\,Cool}}\right)\frac{T_{HS}}{C_{th\ HS\,Cool}} + \frac{T_{Coolant}}{C_{th\ HS\,Cool}} \tag{4.25}$$

In order to diminish the influence of short-term variations in the junction temperature on the current limit, a low-pass filter is included to smooth the temperature measurement. This low-pass filter also approximates the placement of a temperature sensor a short distance away from the silicon die internal to the IGBT module. A filter cut-off frequency of 10 Hz was used to remove the temperature fluctuations due to IGBT switching actions but leave the longer-term temperature rises intact. This creates another state variable T_J^F, corresponding to the filtered value of $T_{J\,Q2}$. Using a first order low pass filter with a time constant τ gives:

$$\dot{T}_J^F = \frac{T_{J\,Q2}}{\tau} - \frac{T_J^F}{\tau} \tag{4.26}$$

4.5.2 Current Limit

The inclusion of the dynamic rating strategies in the feedback control system is based on two fundamental assumptions:

1. The rating strategies control the peak value of the ac components of the arm current. Hence, the average 'dc' (i_{avg}) component is assumed to remain unchanged but the rms value (i_{rms}) is not;

2. The dynamics of the high-level control can be neglected due to the higher bandwidth of the current loop and the bandwidth separation principle between the inner current loop and the outer loops.

4.5.2.1 Strategy A

The current limit control via temperature feedback according to (4.3) results in the control of the losses P_L in (4.21), according to (3.20), which is a non-linear function. Linearising (3.20) around $T_{J(max)}$ results in:

$$P_L = \gamma^A + \psi^A T_{J\,Q2} + \phi^A T_J^F \tag{4.27}$$

where

$$\begin{cases} \gamma^A &= V_0\delta i_{dc} + R_0\delta^2 i_{dc}^2 + \delta i_{dc}\frac{v_{SM}}{v_{CE}^{ref}} f_{sw}\left(E_0 + E_1\delta i_{dc}\right) - \\ &\quad T_{J(max)}^2\left(E_1\delta\frac{v_{SM}}{v_{CE}^{ref}} f_{sw}\left(1-k_p^2\right)\right) - T_{J(max)}^3\left(k_pR_1\delta^2 - k_p^2R_1\delta^2\right) \\ \psi^A &= V_1\delta i_{dc} + R_1\delta i_{dc}^2 + T_{J(max)}^2\left(\frac{k_pR_1\delta^2}{2} - k_p^2R_1\delta^2\right) \\ \phi^A &= T_{J(max)}\left(k_p^2E_1\delta\frac{v_{SM}}{v_{CE}^{ref}} f_{sw}\left(1+\delta\right) - k_p^2R_0\delta^2 + k_p\delta^2R_0\right) + \\ &\quad T_{J(max)}^2\left(k_pR_1\delta^2 - k_p^2R_1\delta^2\right) \end{cases} \tag{4.28}$$

Updating (4.21) and rearranging results in:

$$\dot{T}_{J\,Q2} = \left(\psi^A - \frac{1}{R_{th\ JQ1}}\right)\frac{T_{J\,Q2}}{C_{th\ JQ}} + \frac{T_1}{R_{th\ JQ1}C_{th\ JQ}} + \frac{\phi^A T_J^F}{C_{th\ JQ}} + \frac{\gamma^A}{C_{th\ JQ}} \tag{4.29}$$

Defining the filtered junction temperature T_J^F as the output and γ^A and $T_{Coolant}$ as the inputs, the state-space representation of the closed-loop system for current limit regulation with temperature feedback using Strategy A is defined as:

$$\begin{aligned} \begin{bmatrix} \dot{T}_J^F \\ \dot{T}_{J\,Q2} \\ \dot{T}_1 \\ \dot{T}_2 \\ \dot{T}_3 \\ \dot{T}_{HS} \end{bmatrix} &= \mathbf{A} \begin{bmatrix} T_J^F \\ T_{J\,Q2} \\ T_1 \\ T_2 \\ T_3 \\ T_{HS} \end{bmatrix} + \mathbf{B} \begin{bmatrix} \gamma^A \\ T_{coolant} \end{bmatrix} \\ \begin{bmatrix} T_J^F \end{bmatrix} &= \mathbf{C} \begin{bmatrix} T_J \\ T_{J\,Q2} \\ T_1 \\ T_2 \\ T_3 \\ T_{HS} \end{bmatrix} + \mathbf{D} \begin{bmatrix} \gamma^A \\ T_{coolant} \end{bmatrix} \end{aligned} \tag{4.30}$$

Where the state **A**, input **B**, output **C** and feed-forward **D** matrices are defined as:

$$\mathbf{A} = \begin{bmatrix} -\frac{1}{\tau} & \frac{1}{\tau} & 0 & 0 & 0 & 0 \\ \frac{\phi^A}{C_{th\ JQ}} & \frac{1}{C_{th\ JQ}}\left(\psi^A - \frac{1}{R_{th\ JQ1}}\right) & \frac{1}{R_{th\ JQ1}C_{th\ JQ}} & 0 & 0 & 0 \\ 0 & \frac{1}{R_{th\ JQ1}C_{th\ Q1}} & -\frac{1}{C_{th\ Q1}}\left(\frac{1}{R_{th\ JQ1}} + \frac{1}{R_{th\ Q12}}\right) & \frac{1}{R_{th\ Q12}C_{th\ Q1}} & 0 & 0 \\ 0 & 0 & \frac{1}{R_{th\ Q12}C_{th\ Q2}} & -\frac{1}{C_{th\ Q2}}\left(\frac{1}{R_{th\ Q12}} + \frac{1}{R_{th\ Q23}}\right) & \frac{1}{R_{th\ Q23}C_{th\ Q1}} & 0 \\ 0 & 0 & 0 & \frac{1}{R_{th\ Q23}C_{th\ Q3}} & -\frac{1}{C_{th\ Q3}}\left(\frac{1}{R_{th\ Q23}} + \frac{1}{R_{th\ Q3HS}}\right) & \frac{1}{R_{th\ Q3HS}C_{th\ Q2}} \\ 0 & 0 & 0 & 0 & \frac{1}{R_{th\ Q3HS}C_{th\ HSCool}} & -\frac{1}{C_{th\ HSCool}}\left(\frac{1}{R_{th\ Q3HS}} + \frac{1}{R_{th\ HSCool}}\right) \end{bmatrix} \tag{4.31}$$

$$\mathbf{B} = \begin{bmatrix} 0 & 0 \\ \frac{1}{C_{th\ J}} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{1}{R_{th\ HSCool}} \\ 0 & 0 \end{bmatrix} \tag{4.32}$$

$$\mathbf{C} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{4.33}$$

$$\mathbf{D} = \begin{bmatrix} 0 & 0 \end{bmatrix} \tag{4.34}$$

4.5.2.2 Strategy B

Compared with Strategy A, the integrator in (4.5) creates an additional state m_1:

$$\begin{cases} I^B_{\text{lim}}\left(T_J\right) & = K_P\left(T_{J(max)} - T_J\right) + m_1 \\ \dot{m_1} & = K_I\left(T_{J(max)} - T_J\right) \end{cases} \tag{4.35}$$

The current limit control via temperature feedback according to (4.5) results in the control of the losses P_L in (4.21), according to (3.20). Linearising the latter equation around $T_{J(max)}$ results in:

$$P_L = \gamma^B + \psi^B T_{JQ2} + \phi^B T_J^F + \eta^B m_1 \tag{4.36}$$

where

$$
\begin{cases}
\gamma^B &= \Big(V_0\delta i_{dc} + R_0\delta^2 i_{dc}^2 + \delta i_{dc}\frac{v_{SM}}{v_{CE}^{ref}} f_{sw}\left(E_0 + E_1\delta i_{dc}\right) - \\
&\quad T_{J(max)}^2\left(E_1\delta\frac{v_{SM}}{v_{CE}^{ref}} f_{sw}\left(1-K_P^2\right)\right) - T_{J(max)}^3\left(K_P R_1\delta^2 - K_P^2 R_1\delta^2\right)\Big) + \\
&\quad m_1^0\left[T_{J(max)}\left(E_1\delta\frac{v_{SM}}{v_{CE}^{ref}} f_{sw}\left(\delta K_P - \delta - K_P\right) - 3R_0\delta^2\right) - \right. \\
&\quad \left. T_{J(max)}^2\left(K_P R_1\delta^2\left(1+\frac{T_{J(max)}^2}{2}\right)\right)\right] + \\
&\quad m_1^{0^2}\left[-\frac{R_0\delta^2}{2}E_1\delta^2\frac{v_{SM}}{v_{CE}^{ref}} f_{sw} - T_{J(max)}R_1\delta^2\right] \\
\psi^B &= \left(V_1\delta i_{dc} + R_1\delta i_{dc}^2 + T_{J(max)}^2\left(\frac{K_P R_1\delta^2}{2} - K_P^2 R_1\delta^2\right)\right) + \\
&\quad m_1^0\left[T_{J(max)}\left(K_P R_1\delta^2\left(1+\frac{T_{J(max)}^2}{2}\right)\right) - R_1\delta^2\right] + m_1^{0^2}\left[\frac{R_1\delta^2}{2}\right] \\
\phi^B &= -m_1^0\left[R_0\delta^2 + E_1\delta^2\frac{v_{SM}}{v_{CE}^{ref}} f_{sw} + T_{J(max)}R_1\delta^2\right] + \\
&\quad \left(T_{J(max)}\left(K_P^2 E_1\delta\frac{v_{SM}}{v_{CE}^{ref}} f_{sw}\left(1+\delta\right) - K_P^2 R_0\delta^2 + K_P\delta^2 R_0\right) + \right. \\
&\quad \left. T_{J(max)}^2\left(K_P R_1\delta^2 - K_P^2 R_1\delta^2\right)\right) \\
\eta^B &= m_1^0\left[R_0\delta^2 + E_1\delta^2\frac{v_{SM}}{v_{CE}^{ref}} f_{sw} + T_{J(max)}R_1\delta^2\right] + \\
&\quad \left(T_{J(max)}\left(\delta^2 R_0\left(K_P - 1\right) + E_1\frac{v_{SM}}{v_{CE}^{ref}} f_{sw}\left(1 + K_P\delta^2\right)\right) + \right. \\
&\quad \left. T_{J(max)}^2\left(K_P R_1\delta^2\left(1+\frac{T_{J(max)}}{2}\right) - R_1\delta^2\right)\right)
\end{cases}
\tag{4.37}
$$

Updating (4.21) and rearranging results in:

$$
\dot{T}_{J\,Q2} = \left(\psi^B - \frac{1}{R_{th\;JQ1}}\right)\frac{T_{J\,Q2}}{C_{th\;JQ}} + \frac{T_1}{R_{th\;JQ1}C_{th\;JQ}} + \frac{\phi^B T_J^F}{C_{th\;JQ}} + \frac{\eta^B m_1}{C_{th\;JQ}} + \frac{\gamma^B}{C_{th\;JQ}} \tag{4.38}
$$

Defining the filtered junction temperature T_J^F as the output and γ^B, $T_{J(max)}$ and $T_{Coolant}$ as the inputs, the state-space representation of the system is defined as:

$$\begin{bmatrix} \dot{m}_1 \\ \dot{T}_J^F \\ \dot{T}_{J\,Q2} \\ \dot{T}_1 \\ \dot{T}_2 \\ \dot{T}_3 \\ \dot{T}_{HS} \end{bmatrix} = \mathbf{A} \begin{bmatrix} m_1 \\ T_J^F \\ T_{J\,Q2} \\ T_1 \\ T_2 \\ T_3 \\ T_{HS} \end{bmatrix} + \mathbf{B} \begin{bmatrix} T_{J(max)} \\ \gamma^B \\ T_{coolant} \end{bmatrix}$$
$$\begin{bmatrix} T_J^F \end{bmatrix} = \mathbf{C} \begin{bmatrix} m_1 \\ T_J \\ T_{J\,Q2} \\ T_1 \\ T_2 \\ T_3 \\ T_{HS} \end{bmatrix} + \mathbf{D} \begin{bmatrix} T_{J(max)} \\ \gamma^B \\ T_{coolant} \end{bmatrix} \tag{4.39}$$

where the state **A**, input **B**, output **C** and feed-forward **D** matrices are defined as:

$$\mathbf{A} = \begin{bmatrix} 0 & -K_I & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{\tau} & \frac{1}{\tau} & 0 & 0 & 0 & 0 & 0 \\ \frac{\eta^B}{C_{th\ JQ}} & \frac{\phi^B}{C_{th\ JQ}} & \frac{1}{C_{th\ JQ}}\left(\psi^B - \frac{1}{R_{th\ JQ1}}\right) & \frac{1}{R_{th\ JQ,1}C_{th\ JQ}} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{R_{th\ JQ1}C_{th\ 1}} & -\frac{1}{C_{th\ Q1}}\left(\frac{1}{R_{th\ JQ1}} + \frac{1}{R_{th\ Q12}}\right) & \frac{1}{R_{th\ Q12}C_{th\ Q1}} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{R_{th\ Q12}C_{th\ Q2}} & -\frac{1}{C_{th\ Q2}}\left(\frac{1}{R_{th\ Q12}} + \frac{1}{R_{th\ Q23}}\right) & \frac{1}{R_{th\ Q23}C_{th\ 3}} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{R_{th\ Q23}C_{th\ Q2}} & -\frac{1}{C_{th\ Q3}}\left(\frac{1}{R_{th\ Q23}} + \frac{1}{R_{th\ Q3HS}}\right) & \frac{1}{R_{th\ Q3HS}C_{th\ Q3}} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{R_{th\ Q3HS}C_{th\ HSCool}} & -\frac{1}{C_{th\ HSCool}}\left(\frac{1}{R_{th\ Q3HS}} + \frac{1}{R_{th\ HSCool}}\right) & 0 \end{bmatrix} \tag{4.40}$$

$$\mathbf{B} = \begin{bmatrix} K_I & 0 & 0 \\ 0 & \frac{1}{C_{th\ QJ}} & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{1}{R_{th\ HSCool}} \\ 0 & 0 & 0 \end{bmatrix} \tag{4.41}$$

$$\mathbf{C} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{4.42}$$

$$\mathbf{D} = \begin{bmatrix} 0 & 0 & 0 \end{bmatrix} \tag{4.43}$$

4.5.3 Eigenvalue Analysis

The state-space systems defined by (4.30) and (4.39) form a linear time-invariant (LTI) system, which is (asymptotically) stable if all the eigenvalues λ have negative real parts. The eigenvalues can be solved by solving the characteristic equation:

$$|s\mathbf{I} - \mathbf{A}| = 0 \tag{4.44}$$

Where $\mathbf{I}$ is the identity matrix of appropriate dimension. In other words, the values for s that satisfy (4.44), i.e. the poles of the transfer function, are the eigenvalues λ of $\mathbf{A}$. In the s domain, it is required that all the poles of the system are located in the left-half plane, and therefore all the eigenvalues must have negative real parts and also be over-damped to avoid temperature overshoot.

The verification of the analytical models defined by (4.30) and (4.31) is presented is Appendix B. The eigenvalues of the system are evaluated for different controller parameters of Strategies A and B. The system parameters [2] of Table 4.2 are considered and the loss calculating parameters are presented in Table 4.3. The loss calculation expression is linearised around $T_{J(max)} = 95\,^{\circ}\mathrm{C}$, which is the upper limit considered for the thermal headroom.

4.5.3.1 Strategy A

The eigenvalues of the system as a result of the variation of the temperature-current droop k_p are shown in Figure 4.13 (a). It can be observed that the eigenvalues only possess real part and although an increase in the value of k_p places the eigenvalues closer to the origin, they remain in the left-hand plane for the analysed range.

The variation of the maximum semiconductor temperature $T_{J(max)}$ in the eigenvalues of the system is shown in Figure 4.13 (b). An increase in the maximum limit of the

[2] The nominal operating voltage of the SMs is $V_{SM\,nom} = 50\,\mathrm{V}$, which is much smaller than the maximum rated collector-emitter voltage of the semiconductor module, $v_{CE\,max} = 1200\,\mathrm{V}$, and the collector-emitter voltage to which the datasheet loss value are referenced ($v_{CE} = 600\,\mathrm{V}$). This reduced ratio is due to the rating of the experimental setup and diminishes the effect of switching losses on the overall semiconductor losses. In order to compensate for this limitation, the frequency f_{sw} of the triangular carriers is set to 2.5 kHz. Although this value is significantly higher than the typical values used in the range of hundreds of hertz, it allows the $\frac{v_{SM}}{v_{CE}^{max}} f_{sw}$ ratio in (3.10) to approximate the operating electrical conditions of a commercial SM.

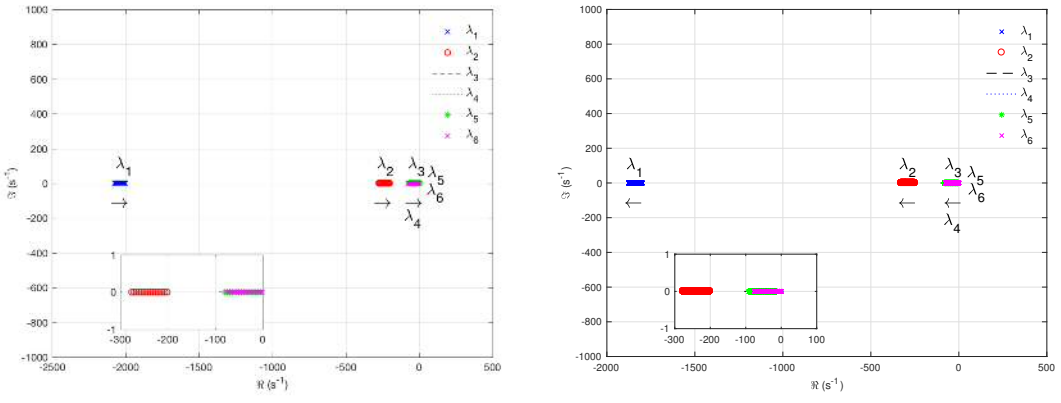
TABLE 4.2: MMC system parameters

Parameter	Value	Unit
Number of SMs per arm (N)	3	-
SM capacitance (C_{SM})	4.7	mF
Arm inductance (L_{arm})	3.3	mH
Nominal SM voltage ($v^*_{SM\,nom}$)	50	V
Nominal arm voltage ($v_{arm\,ref}$)	150	V
Line current (i_g)	30	A
Phase voltage (v_g)	75	V
Carrier frequency (f_{sw})	2.5	kHz
Fundamental frequency (f_0)	50	Hz
Nominal coolant temperature ($T_{Coolant}$)	50	°C

TABLE 4.3: Semiconductor specifications for IGBT module FF75R12YT3

IGBT			Diode		
Parameter	Value	Unit	Parameter	Value	Unit
$V_{0\,Q}$	0.65625	V	$V_{0\,D}$	0.62625	V
$V_{1\,Q}$	0.00175	V/°C	$V_{1\,D}$	0.00295	V/°C
$R_{0\,Q}$	0.0142	Ω	$R_{0\,D}$	0.004125	Ω
$R_{1\,Q}$	0.0001	Ω/°C	$R_{1\,D}$	0.000127	Ω/°C
$E_{0\,Q}$	0.2233	J/A	$E_{0\,D}$	0.1135	J/A
$E_{1\,Q}$	0.0002	J/A^2	$E_{1\,D}$	0.0004	J/A^2

headroom is beneficial also from a stability point of view as the eigenvalues are placed further into the left-hand plane. Similarly to the variation of the droop constant, eigenvalues $\lambda_{3,4,5,6}$ are located very close to the origin, but remain in the left-hand plane for the analysed range.



(a) (b)

FIGURE 4.13: Eigenvalues of the system for Strategy I: (a) - k_p variation from 0.1 A/°C to 100 A/°C in 0.1 A/°C steps ($T_{J(max)} = 95\,°C$) and (b) - $T_{J(max)}$ variation from 80 °C to 100 °C in 1 °C steps ($k_p = 5\,A/°C$). Arrows indicate growing parameter values.

Considering $k_p = 5\text{A}/^\circ\text{C}$ and $T_{J(max)} = 95\,^\circ\text{C}$, the eigenvalues of the system are shown in Table 4.4.

TABLE 4.4: Eigenvalues of the system for strategy A

Eigenvalues
$\lambda_1 = -2001.25$
$\lambda_2 = -225.23$
$\lambda_3 = -50.37$
$\lambda_4 = -30.41$
$\lambda_5 = -15.63$
$\lambda_6 = -21.22$

4.5.3.2 Strategy B

For this strategy, the eigenvalues of the system are evaluated for several values of the controller proportional gain K_P, integral gain K_I, and maximum temperature $T_{J(max)}$, and are shown in Figure 4.14 (a), (b) and (c), respectively. It can be observed in Figure 4.14 (a) that the system possesses a complex conjugate pair, $\lambda_{3,4}$, with both real and imaginary parts increasing as the proportional gain increases. For $K_P \geq 8\text{A}/^\circ\text{C}$, the eigenvalue pair becomes under-damped, leading the system to have an oscillatory behaviour. All the other eigenvalues have only real part, which moves close to the origin as the proportional gain increases without, however, moving to the right-hand plane.

A similar behaviour can be observed for the integral gain variation in Figure 4.14 (b). The complex pair $\lambda_{3,4}$ also dictates the stability of the system as high gain values ($K_I \geq 0.015\text{A}/^\circ\,(\text{C s})$) lead to under-damped poles as all the other eigenvalues remain in the left-hand plane for the analysed range. Unlike Strategy A, however, the increase in the upper limit of the thermal headroom contributes to a placement of the eigenvalues closer to the origin, as shown in Figure 4.14 (c). It also leads to the placement of the complex conjugate pair within the over-damped region of the imaginary place, thus aiding the improvement of the stability of the system. A minimum value $T_{J(max)} = 85\,^\circ\text{C}$ must be considered for a stable operation.

Considering $K_P = 5\text{A}/^\circ\text{C}$ and $T_{J(max)} = 95\,^\circ\text{C}$, as for Strategy A, and $K_I = 0.001\,\text{A}/(^\circ\text{C s})$, the eigenvalues of the system are shown in Table 4.5. Although the eigenvalues, including the complex conjugate pair, are located close to the origin, they are over-damped and remain on the left-hand plane.

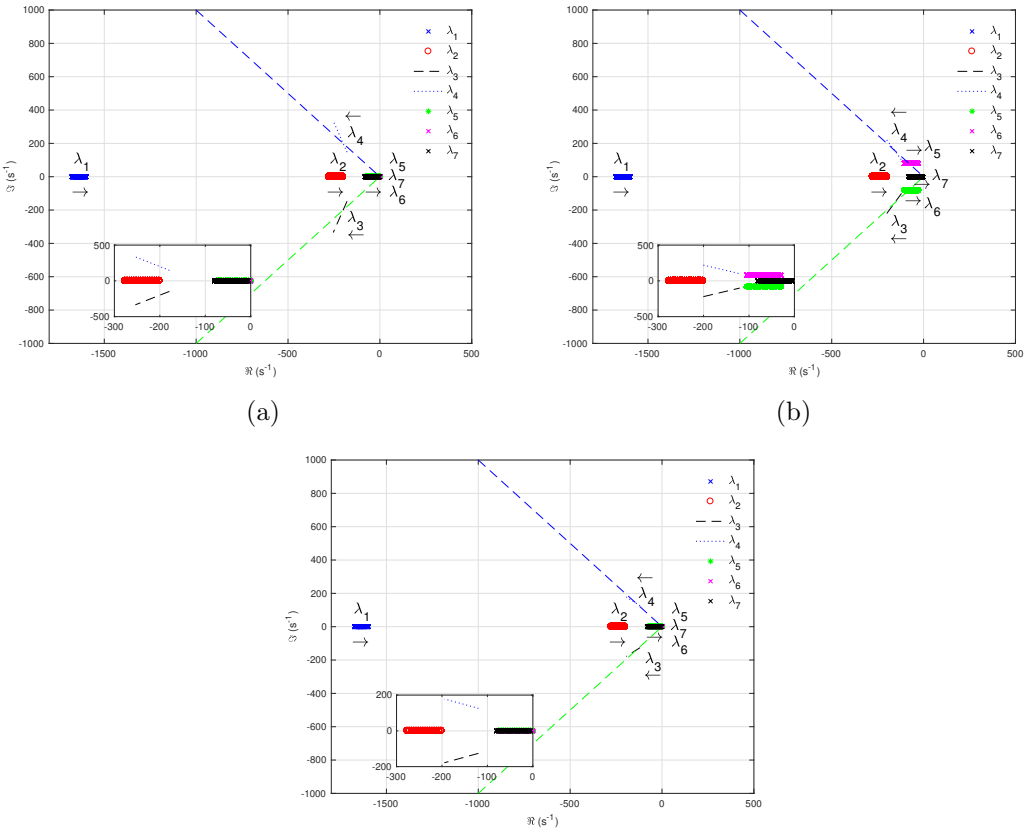


FIGURE 4.14: Eigenvalues of the system for Strategy I: (a) - K_P variation from 1 A/°C to 20 A/°C in 0.1 A/°C steps ($K_I = 0.001\text{A}/(°\text{C}\,\text{s})$ and $T_{J(max)} = 95\,°\text{C}$) ; (b) - K_I variation from 0.0001 A/(°C s) to 0.025 A/(°C s) in 0.0001 A/(°C s) steps ($K_P = 5\text{A}/°\text{C}$ and $T_{J(max)} = 95\,°\text{C}$) and (c) - $T_{J(max)}$ variation from 80 °C to 100 °C in 1 °C steps ($K_P = 5\text{A}/°\text{C}$ and $K_I = 0.001\text{A}/(°\text{C}\,\text{s})$). Arrows indicate growing parameter values.

TABLE 4.5: Eigenvalues of the system for strategy B

Eigenvalues
$\lambda_1 = -1598.67$
$\lambda_2 = -201.17$
$\lambda_{3,4} = -29.74 \pm j0.18$
$\lambda_{5,6} = -0.21$
$\lambda_7 = -5.03$

Results in Figure 4.13 and Figure 4.14 clearly show that the combined electro-thermal system for the proposed dynamic rating strategies is always stable and always over-damped and therefore can never cause the junction temperatures to overshoot $T_{J(max)}$.

4.6 Results

The proposed method is validated in MATLAB/Simulink using the PLECS Toolbox [282], with the parameters of the MMC presented in Table 4.2. SMs 1-3 and SMs 4-6 are located in the upper and lower arms, respectively, of each phase and the circulating current suppression method proposed in [126] was implemented. The converter operates in an inverter mode and the thermal network of Figure 4.12 is implemented using the datasheet parameters in Table 4.1.

4.6.1 Steady-State Operation

The steady-state quantities of phase A of the MMC test system are shown in Figure 4.15. The calculated steady-state temperatures on the dies of the semiconductor module of SM 3 are presented in Figure 4.15 (a) for a peak line current $i_g = 30\,\text{A}$, presented in Figure 4.15 (b). The temperatures are similar for the corresponding dies in different SMs, with the die of IGBT Q2 having the highest (nominal) temperature $T_{J(nom)} = 77.4\,^\circ\text{C}$ and therefore determining the value to be utilised for the rating strategies in (4.3) and (4.5). The reactive current component I_q is kept at zero and all the current limit and headroom is prioritised for the active current component I_d.

The SM capacitor voltages of the upper and lower arms are presented in Figure 4.15 (c), where the 50 Hz ripple due to the arm currents can be observed. The voltages are balanced around their nominal value $v^*_{SM\,nom} = 50\,\text{V}$, resulting in arm voltage waveform with four $(N+1)$ distinct levels, shown in Figure 4.15 (d), and a standard AC-side multilevel voltage, shown in Figure 4.15 (e). Due to the interleaved phase-shifted carriers in the PWM scheme, the phase voltage waveform possesses $2N+1 = 7$ levels [283].

Semiconductor losses in (3.11) are defined as a function of the arm currents. For the line current, the arm currents in Figure 4.15 (b) have a peak value of 23 A, which is used for the rating strategies in (4.3) and (4.5). Given the maximum virtual junction temperature $T_{vj\,max} = 150\,^\circ\text{C}$ for the semiconductor module used is this work, the upper limit of the thermal headroom is considered to be $T_{J(max)} = 95\,^\circ\text{C}$.

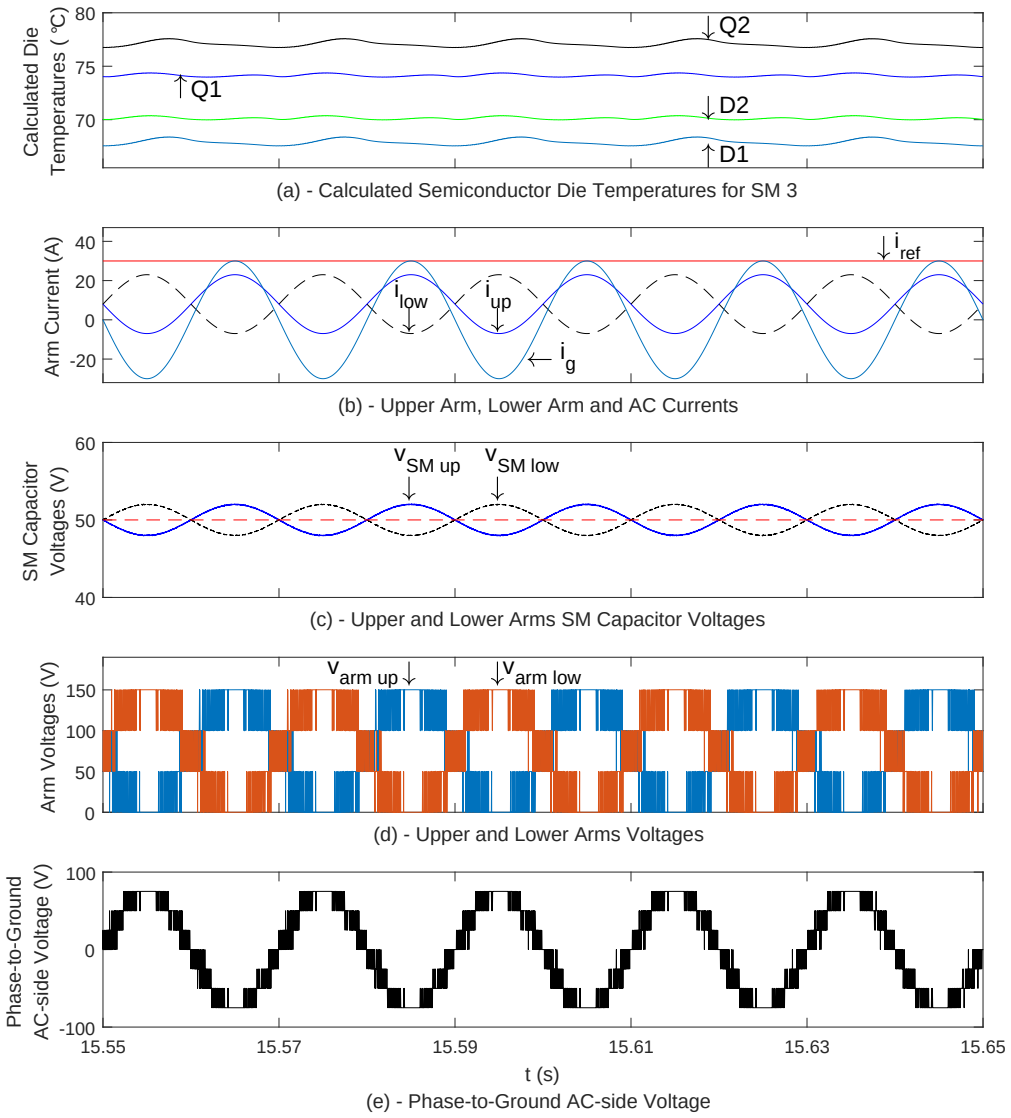


FIGURE 4.15: Steady-state quantities in phase A.

TABLE 4.6: Dynamic rating strategies case studies parameters

Rating Strategy	Case	Parameter	Value	Unit
Strategy A	I	k_p	1.3068	A/°C
	II	k_p	5	A/°C
	III	k_p	100	A/°C
Strategy B	IV	K_P	5	A/°C
		K_I	0.001	A/°Cs

The test cases in Table 4.6 are used to validate the performance of the proposed rating strategies in two key operational scenarios: response to a cooling system failure and converter current overload. For Case I, $k_p = k_{p\,min} = \frac{23}{95-77.4} = 1.3068$ A/°C, as in (4.4).

4.6.2 Cooling System Failure

The dynamic rating capability of the converter is verified with the utilisation of a coolant temperature profile shown in Figure 4.16, corresponding to a cooling system failure. The coolant temperature is controlled by the main pump via a closed-loop system, as shown in Figure 3.3, and is initially set to $T_0 = 50\,°\text{C}$. When a problem leading to a malfunction of the main cooling circuit occurs [264], e.g. obstruction of the hydraulic circuit or malfunction of the heat exchanger, the cooling effectiveness decreases and the coolant temperatures starts to increase. When the measured temperature reaches a threshold $T_{th} = 60\,°\text{C}$, deviating from the set-point of $50\,°\text{C}$, a reserve pump is activated and takes ownership of the cooling. Simultaneously, the coolant temperature continues to increase, as the large time constant of the coolant prevents an immediate temperature decrease. The temperature stabilizes at $T_1 = 70\,°\text{C}$ when a thermal equilibrium is reached and is further decreased until the initial desired coolant temperature of $50\,°\text{C}$ is attained.

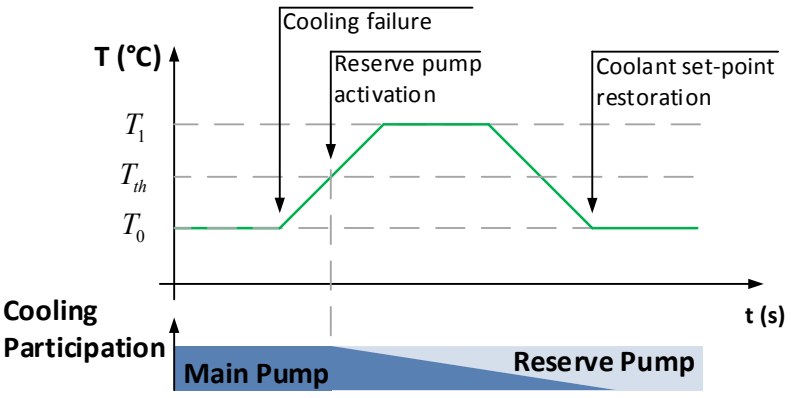


FIGURE 4.16: Coolant temperature profile for cooling system failure.

The durations corresponding to the temperature ramp-up, thermal equilibrium, and temperature ramp-down were considered the same and equal to 5 minutes (300 s) due to lack of information from commercial projects. The total duration of the cooling profile is therefore 900 s and the detection of the failure is assumed to be based on the measured temperature deviation from the initial set-point of $50\,°\text{C}$, although other methods reported in the literature such as [284, 285] can also be implemented.

The simulation results of the temperature regulation by the proposed rating strategies as a result of a cooling failure are shown in Figure 4.17 for a peak arm current $I_{ref} = 20\,\text{A}$. For the cooling profile in Figure 4.17 (a), it can be observed that without current limit

modulation the temperature in Figure 4.17 (b) will increase to a maximum of 103.7 °C, well above the maximum temperature $T_{J(max)} = 95\,°C$.

When the rating strategies are implemented, the current limit is decreased as the temperature increases, as shown in Figure 4.17 (c), leading to the curtailment of the output current as a means to control the temperature; for any of the cases, the temperature is controlled to be below the maximum value of 95 °C. It can be observed for Strategy A that an increase in the proportional gain from Case I to Case III leads to higher temperatures as the current limit is decreased by a smaller amount for the same temperature increase. Nonetheless, there is a very small difference between the resulting temperatures for Case II and Case III, despite the proportional gain being twenty times larger for the latter. This suggests that there is a saturation effect as significant increases in the proportional gain do not result in significant decreases in the curtailed current.

For Case IV, where Strategy B is employed, it can be observed that by utilising the same proportional gain as the proportional-type control considered for Case II, the addition of an integral term in the dynamic rating law results in a better performance: the current

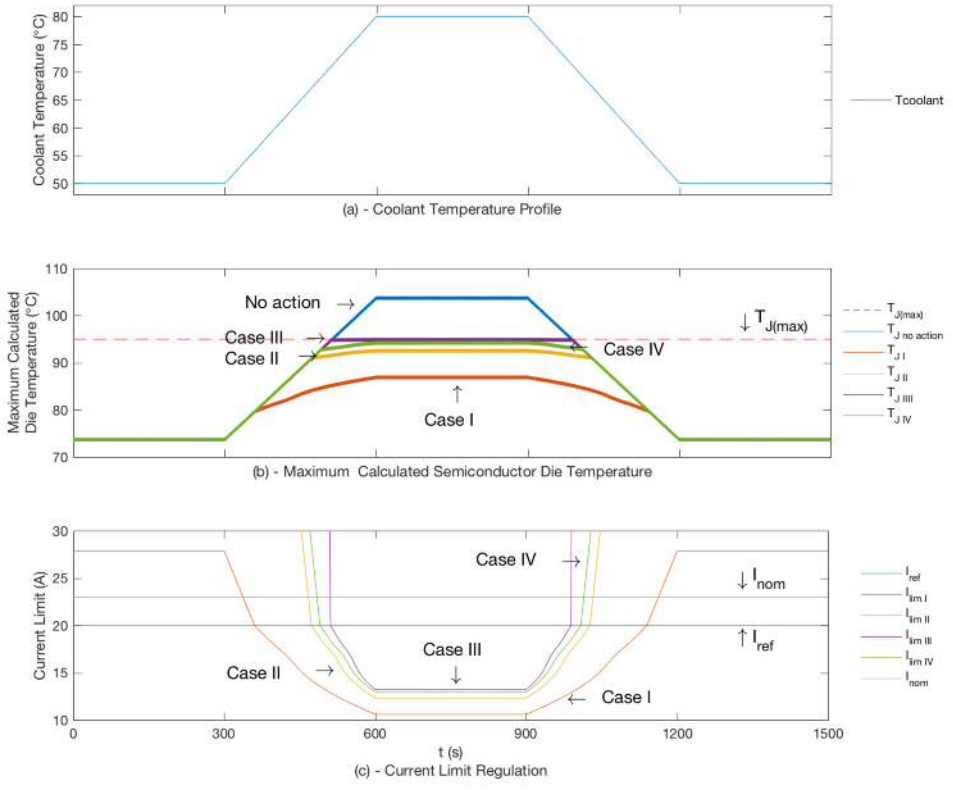


FIGURE 4.17: Temperature regulation during a cooling failure.

limit is much closer to the limit imposed by Strategy A for Case III than Case II, resulting in a higher maximum temperature, i.e. the thermal headroom is better utilised and the current reduction is smaller. The superiority of Strategy B can be observed more clearly in Figure 4.18, where results are also presented for $k_p = \{2, 10, 25, 50, 75\}$ A/°C.

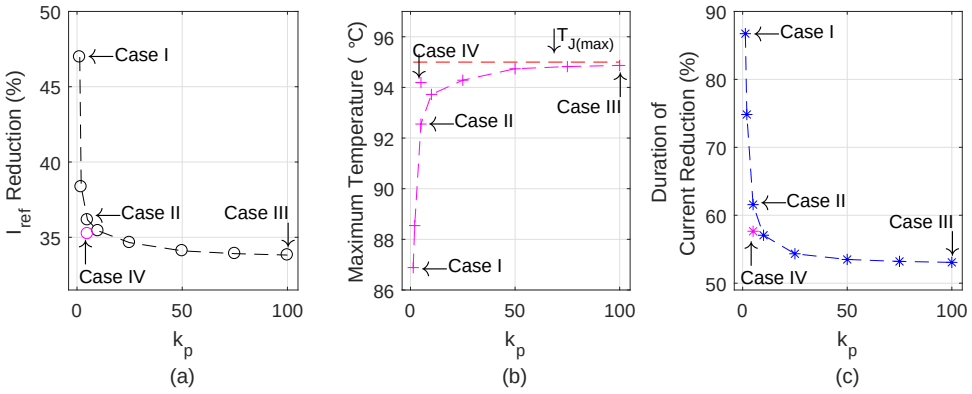


FIGURE 4.18: Simulation results of temperature regulation during a cooling failure as a function of the proportional gain: (a) - Maximum percent reduction in the reference current; (b) - Maximum calculated semiconductor die temperature and (c) - Percent duration of the current curtailment period with respect to the duration of the cooling profile.

The percent current reduction as a function of the proportional gain k_p (K_P for Case IV), is shown in Figure 4.18 (a), where it can be observed that the reduction is smaller for Case IV than for Case III, but also even lower than for $k_p = 10\,\text{A/°C}$, which is twice the value of K_P. Furthermore, for high k_p values the saturation effect suggested by the results in Figure 4.17 can be observed more clearly: large k_p values determine large current limits, which means that the reference current will only be curtailed when the temperature gets very close to 95 °C. For high values of the proportional gain, the curtailment will only occur at successively higher temperatures, resulting in smaller current reductions. Hence, very large increases in the proportional gain when employing Strategy A do not result in a generally better utilisation of the thermal headroom, nor specifically in a better performance during cooling failure ride-through.

The saturation phenomenon resulting from the temperature "clamping" is confirmed by the maximum temperature presented in Figure 4.18 (b), where it can be seen that successively higher temperatures are reached for higher k_p values, but always remain below 95 °C. For example, increasing k_p from 50 A/°C to 100 A/°C results in a change in the maximum temperature from 94.7 °C to 94.9 °C and a change in the minimum current limit from 13.2 A to 13.3 A. This difference has almost no impact in a practical

application as the temperature will very likely be masked by measurement noise, which can be further amplified by employing a large k_p value. The better performance of Case IV can also be observed in this graph, as the resulting maximum temperature is higher than the equivalent Case II and than the resulting temperature for $k_p = 10\,\mathrm{A/^{\circ}C}$.

As a result of the current only being curtailed for temperatures very close to the upper limit of the thermal headroom, the duration of the current reduction period is also smaller as the proportional gain increases, which can be observed in Figure 4.18 (c). For high-power applications such as HVDC, operating times during reduced current injection capability should be minimised, as well as the magnitude of current curtailed. These are two conflicting objectives, as clearly shown in Figure 4.18.

4.6.3 Converter Overload

The simulation results of the temperature regulation by the proposed rating strategies during a current overload command are shown in Figure 4.19 for Cases I-IV (first to last columns, respectively). It can be observed in Figure 4.19 (a)-(d) that similarly to Figure 4.17 and Figure 4.18, the use of a higher proportional gain leads to a better exploitation of the thermal headroom as the current is only limited when temperatures approach 95 °C very closely: the the maximum temperatures are $T_J = T_{J(nom)} = 77.4\,^{\circ}\mathrm{C}$ for Case I, 88.6 °C for Case II, 94.6 °C for Case III and 89.9 °C for Case IV. This permits higher overload current overload magnitudes, as shown in maximum Figure 4.19 (e)-(h), where successively higher magnitudes can be reached for higher gains.

Modest overloads are achieved for Case I as $k_p = k_{p\,min}$. For Case II and Case IV. the results are very similar, with the latter slightly outperforming the former, as also verified in the simulation results of the temperature regulation during a cooling failure. The shift of the maximum operating temperature at nominal current with increasing proportional gain was demonstrated graphically in Figure 4.4 and can be observed for Cases II-IV. This enables the converter to possess a 'new' fixed limit, above the nominal one, that can be sustained permanently, as a result of the utilisation of the thermal headroom, i.e. the effective power transmission capacity of the converter is increased. The new fixed limits for Cases II-IV are 32 A, 37.2 A and 33 A, respectively, which represents an increase of the effective converter rating from 1.15 pu to 1.6 pu, 1.86 pu and 1.65 pu, respectively.

Semiconductors overload magnitude and duration mapping is shown in Figure 4.19 (i)-(l), where the effect of permanent increase of the current limit can be clearly observed. Furthermore, it is also demonstrated that very large current magnitudes can flow through the semiconductors, even if only for short periods ($< 1\,\text{s}$). For the range shown in Figure 4.19 (i)-(l), maximum overloads of 85 A (4.25 pu) and 135 A (6.75 pu) can be attained for Cases II and IV and Case III, respectively.

The semiconductors TOE is shown in Figure 4.20. Results are similar for Cases II and IV (proportional-based and PI-based control, respectively, with $k_p = K_P = 5\,\text{A}/^{\circ}\text{C}$), although marginally higher for Case IV. Nonetheless, any of the Cases II-IV presents a significantly larger TOE than Case I, which is essentially negligible. The high proportional gain employed in Case IV enables a much larger TOE than the other cases, where a peak hypothetical overload of 500 A for an almost instantaneous duration could be achieved, at the expense of a maximum semiconductor temperature operation up to 94.6 °C. However, the maximum continuous collector current $I_{c\,max} = 75\,\text{A}$ [9] (3.75 pu) for the semiconductor module must be respected, therefore establishing the maximum overload magnitude. For this value, the overload duration increases from 690 ms for Case II, to 820 ms for Case IV and 2.09 s for Case III, which is three time the overload duration achieved for Case II. For lower current magnitudes, higher overload durations are permitted as a result of a slower temperature increase to the maximum value, down to the permanent extended current limits enabled by the dynamic rating strategies.

The results in Figure 4.19 and Figure 4.20 clearly demonstrate that the thermal headroom of semiconductor devices can be safely exploited though dynamic rating strategies, enabling an enhanced current injection capability from the converter.

The largest time constant of the thermal network is associated with the thermal capacitance $C_{th\,HSCool}$ of the heat sink mass, which dominates the dynamic response of the converter. This value depends not only on the material composition of the heat sink but also on the cooling technique employed. Typical time constants can range from values as low as 15 s for liquid cooling employing cold plates to values in the order of 150s for forced-air cooling and 500s when natural convection is chosen [286].

The influence of the time constant in the semiconductors overload capability is analysed for four different scenarios, where different cooling solutions are assumed to be employed:

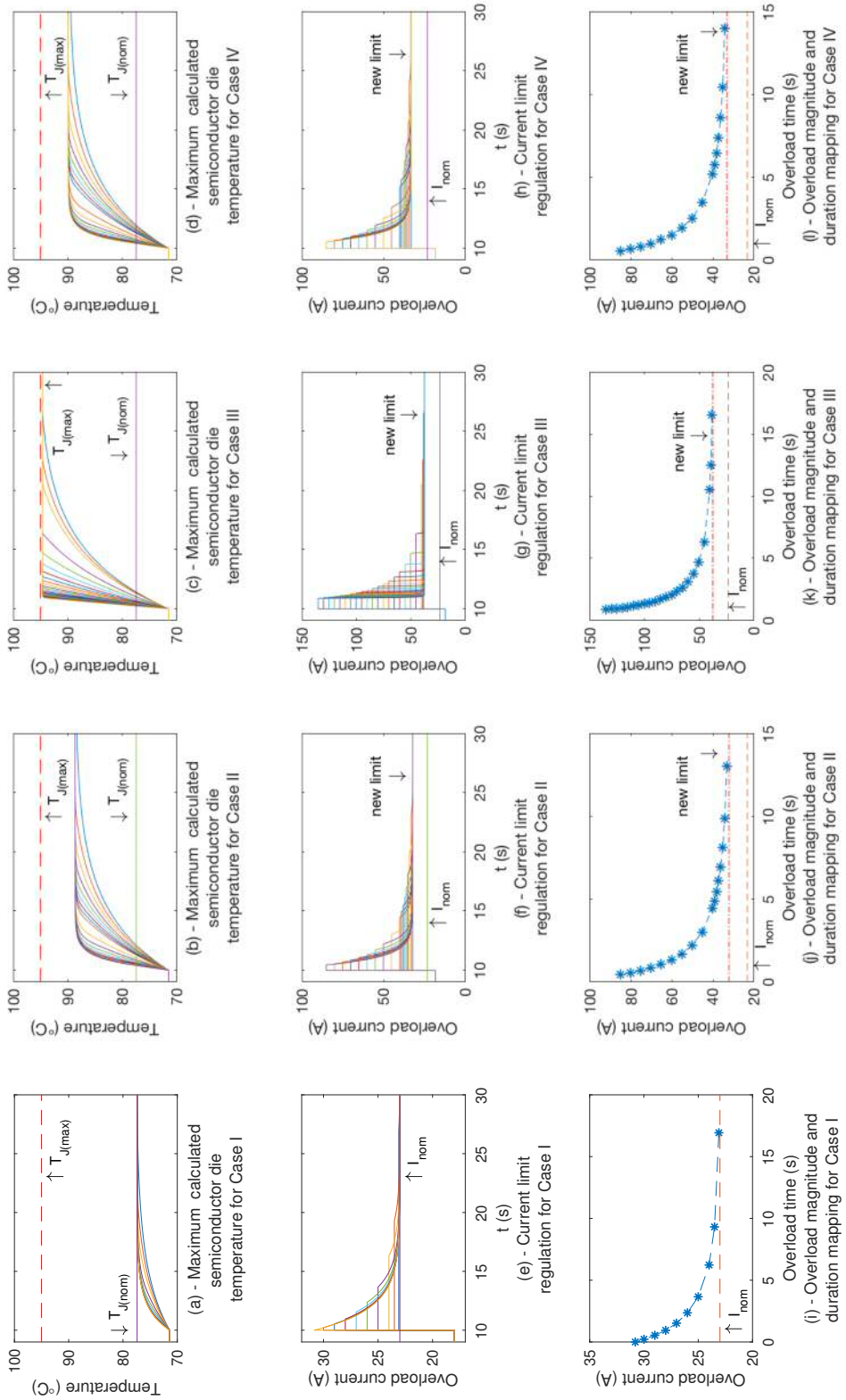


FIGURE 4.19: Temperature regulation during a current overload.

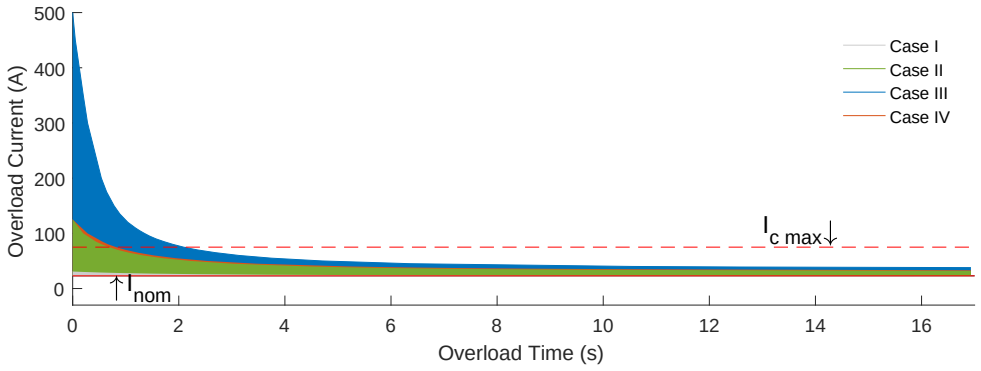


FIGURE 4.20: Semiconductors TOE.

- base scenario: system data as in Table 4.1;
- LC scenario: liquid cooling (LC) is utilised and $\tau_{HS\,Cool} = 50\,\text{s}$;
- FC scenario: forced-air cooling (FC) is utilised and $\tau_{HS\,Cool} = 100\,\text{s}$;
- NC scenario: natural convection (NC) is utilised and $\tau_{HS\,Cool} = 150\,\text{s}$.

Utilising (4.14), the TOEns for these four scenarios for each of the cases are shown in Table 4.7. It can be clearly observed that the TOEn suffers a greater increase for an increase in the peak overload magnitude for the different cases than an increase in the time constant for the different scenarios of a case, given the effect of the second-order dependency of the TOEn on the peak overload magnitude.

As shown in Figure 4.19 and Figure 4.20, it can be observed in Table 4.7 that Case IV outperforms Case II, which results mainly from the slightly higher initial peak overload magnitude since their respective TOEns do not differ significantly when the same time constant is considered, for all scenarios

The effect of the heat sink time constant on the semiconductors TOE is presented in Figure 4.21. For all Cases and respective scenarios, it is clear that larger time constants allow the overload current commands to be sustained for a longer duration, considerably improving the TOE, as expected from the TOEn results in Table 4.7. These longer durations also enable the improvement of the provision of power support and ancillary services to the AC grid.

Considering a peak overload current command of 25 A for Case I, 65 A for Cases II and IV and 180 A for Case III, the comparison between analytical calculation using (4.17)

TABLE 4.7: Semiconductors TOEn for different heat sink time constants (kA^2s).

Case	Scenario			
	base	LC	FC	NC
I	2.35	23.46	46.91	70.37
II	34.96	349.636	699.27	1048.91
III	593.14	5931.42	11862.83	17794.25
IV	36.29	362.95	725.89	1088.84

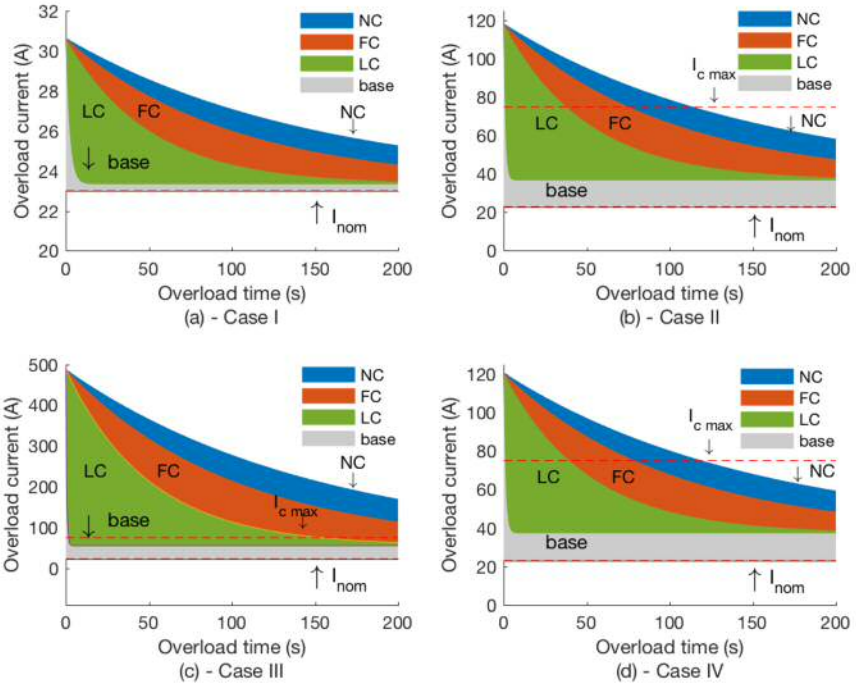


FIGURE 4.21: Variation of semiconductors TOE for different heat sink time constants.

and simulation results for the variation of overload durations for different Heat Sink time constants is shown in Table 4.8. The absolute maximum error ranges from 0.3 % to 4.5 %, which indicates a good level of agreement between analytical and calculated results, for all the cases and scenarios analysed. This level of agreement confirms the TOEn as a simple method for the evaluation and benchmark of heat sinking system solutions if the overload capability is included in the converter design stage.

4.6.4 Improvement of Frequency Support

'The Grid Code' [106] of National Grid, the Transmission System Operation in Great Britain, establishes that mandatory frequency response is an automatic change in active power output in response to a frequency change, in order to maintain the frequency

TABLE 4.8: Comparison between analytical and simulation results for the variation of overload durations for different heat sink time constants.

Case	Scenario	Overload Duration			
		Calculation (s)	Simulation (s)	Error	% Error
I	LC	73.5	73.7	0.2	0.3 %
	FC	147.1	147.6	0.5	0.3 %
	NC	220.6	221.1	0.5	0.2 %
II	LC	50.6	52.8	2.2	4.2 %
	FC	101.2	106	4.8	4.5 %
	NC	151.7	158.7	7	4.4 %
III	LC	60.67	62	1.3	2.1 %
	FC	121.3	124	2.7	2.2 %
	NC	182	186	4	2.2 %
IV	LC	56	54.8	-1.2	−2.2 %
	FC	112	109.6	-2.4	−2.2 %
	NC	168	164.5	-3.5	−2.1 %

within statutory (49.5Hz - 50.5Hz) and operational (49.8Hz - 50.2Hz) limits. This is achieved by using up to three response services, with progressive durations. Given the short-time overload of the semiconductors demonstrated in Figure 4.20, the first or primary response is of interest. Primary response consists in the provision of additional active power (or a decrease in demand) within 10 seconds after an event and can be sustained for a further 20 seconds. This can be triggered by the high-level control of the converter station upon the detection of measurements exceeding certain thresholds such as frequency deviation or frequency derivative. The additional power can be deployed within a relatively long time frame, resorting, or not [35], to using a remote communication infrastructure. From Figure 4.20, it can therefore be concluded that in order to comply with the Grid Code requirements, lower magnitudes are required given the power support duration requirement. Thus, the converter will operate mainly in the lower band of the thermal headroom, using modest overload current magnitudes compared to the maximum possible values of the TOE.

The single-line representation of the test system is shown in Figure 4.22 and it is assumed that the additional power utilised during the overload is provided by a remote source connected to the DC grid, e.g. inertia emulation from offshore wind farms [35], and is triggered by the high-level control of the converter station. The overload power can also be provided by controlled circulating currents [287].

A complete representation of the primary frequency regulation scheme for a synchronous machine-based power plant was considered for the AC grid, including a speed governor

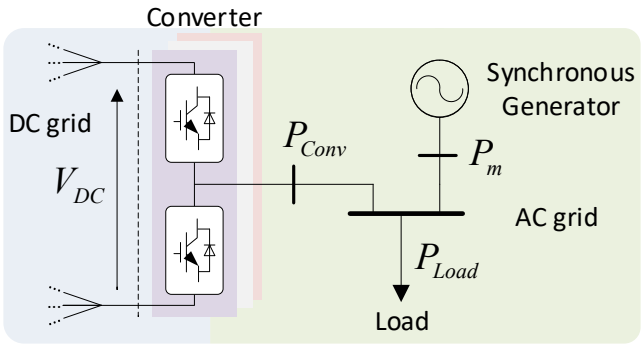


FIGURE 4.22: Single-line representation of the test system.

"Steam Gov 1" and a steam turbine "Steam Tur 1" [13, 288]. The automatic generator control was not included for the synchronous generator as its response is considerably slower than the inertial and primary frequency responses [289].

The frequency regulation of the grid is illustrated in Figure 4.23 and its parameters shown in Table 4.9. P_m, P_{Load} and P_{Conv} denote the prime mover power of the thermal plant, the active power consumption of the load and the power injected by the converter, respectively. Neglecting the small value of the damping coefficient D, the system frequency ω can be expressed as a function of system inertia H and the injected and absorbed powers as:

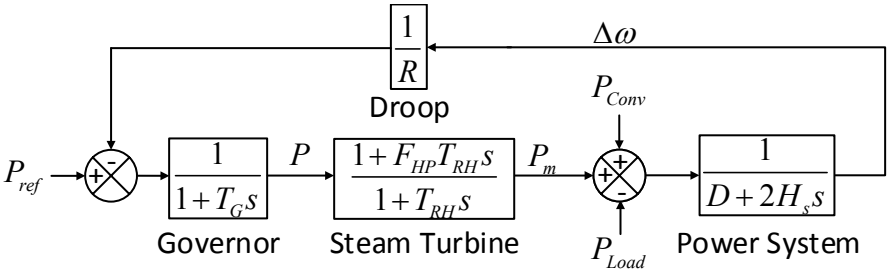


FIGURE 4.23: Primary frequency regulation of the AC grid, including speed governor and steam turbine.

$$2H_s \frac{d\omega}{dt} = P_m + P_{Conv} - P_{Load} \tag{4.45}$$

from where it can be observed that any changes in P_m or P_{Load} that can be offset by P_{Conv} will result in a smaller transient frequency shift during disturbances, while simultaneously enhancing the damping of the electromechanical swing mode [289].

Defining a peak arm current of 18 A as 1 pu, the rated power P_{Conv} of the converter is:

TABLE 4.9: Primary frequency regulation model parameters [13]

Parameter	Value	Unit
Governor Time Constant (T_G)	0.3	s
Re-heater Time Constant (T_{RH})	6	s
Fraction of power generated by the High-Pressure section (F_{HP})	0.33	-
Load Damping Constant (D)	2.5	W/Hz
Inertia Constant (H_s)	2.5	s
Permanent Droop (R)	0.05	Hz/W

$$P_{Conv} = \sqrt{3}\frac{75\sqrt{3}}{\sqrt{2}}\frac{18}{\sqrt{2}} = 2025\,\text{W} \tag{4.46}$$

For a synchronous generator (P_m) to converter (P_{Conv}) ratio or 2:1 [290], the load power P_{Load} in Figure 4.22 and Figure 4.23 under power balance conditions is:

$$P_{Load} = 3 \times 2025 = 6075\,\text{W} \tag{4.47}$$

The simulation results of the frequency regulation by the proposed rating strategies during a current overload command are shown in Figure 4.24 for Cases II-IV (first to last columns, respectively). Case I is not considered here given the impossibility to cope with the support duration requirement of the Grid Code and f_o and f_s correspond to the lower operational and statutory limits of 49.8 Hz and 49.5 Hz, respectively. A frequency deviation exceeding the operational limit is used as the triggering signal for the converter overload.

Given the different permanent overload capabilities enabled by the rating strategies, the load increase is defined separately for each Case. For Cases II-IV, and considering a base of 23 A, the maximum permanent overloads are 32 A, 37.2 A and 33 A, respectively, corresponding to maximum current and power overloads of 0.391 pu, 0.617 pu and 0.435 pu, respectively. These values are considered as the load increase in each Case to assess the effect of frequency regulation due to the full utilisation of the semiconductors overload capability. For each Case, four scenarios are considered:

- "Initial Set-point", where the initial current command of 18 A remains unchanged;

- "Fixed Limit", where the nominal current limit of the converter $I_{nom} = 23\,\text{A}$ defines the maximum current injection;
- "$I_{ov\,max}$" corresponds to the maximum permanent current contribution of the converter, i.e. the "new limit" shown in Figure 4.19 and resulting from the utilisation of the dynamic rating strategy;
- "$I_{ov\,temp}$" is an overload current command higher than $I_{ov\,max}$ and used to demonstrate the response of the frequency to an extreme power imbalance that cannot be completely corrected by the permanent overload capability of the converter.

Simulation results for these scenarios are presented in Figure 4.24 (g)-(i), where it can be observed that resorting to the nominal fixed limit of the converter results in smaller transient and steady-state frequency deviations than when the initial set-point remains unchanged after the power imbalance, as shown in Figure 4.24 (a)-(c). However, for all the Cases, both scenarios are unable to sustain the steady-state frequency above the lower statutory or operational limits. Although the same proportional gain is used for both Cases II and IV, the higher permanent overload magnitude for the latter results in a higher power imbalance (0.418 pu instead of 0.390 pu) and a higher frequency deviation, as shown in Figure 4.24 (g)-(i).

The maximum semiconductor die temperatures are shown in Figure 4.24 (d)-(f), where the progressive utilisation of the thermal headroom from Case II to Case IV and to Case III can be observed. The maximum equilibrium ("clamped") temperatures have the same value as previously observed in Figure 4.19. When the permanent overload current limit $I_{ov\,max}$ is utilised, it can be observed that for all Cases the power imbalance is completely corrected by the converter following the detection of the AC grid frequency exceeding 49.8 Hz. The overload magnitudes define the maximum load increase/loss of generation for which the converter can provide to support the primary frequency response of the AC grid and completely correct the power imbalance. Although the correction of the power imbalance is a function of the secondary frequency response [106], with a much larger time frame (30s - 30 min), results in Figure 4.24 (g)-(i) clearly demonstrate the flexibility introduced by the dynamic rating strategies in enabling the converter not only to cope with the primary frequency regulation but also to be able to provide ancillary (and paid) services to the grid, such as secondary frequency response.

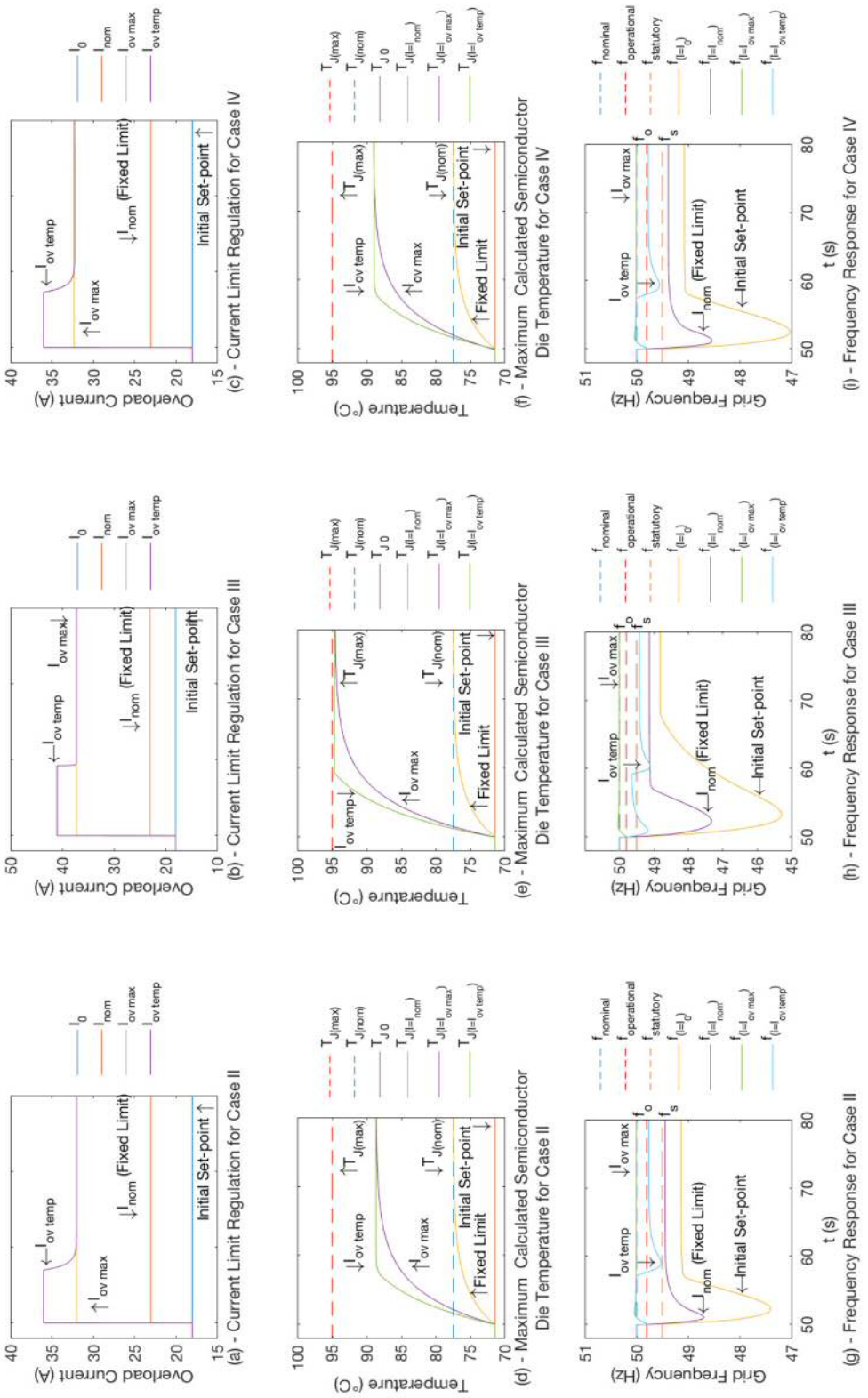


FIGURE 4.24: Frequency regulation during current overload as response to a load increase.

In an extreme scenario, the power imbalance can be such that it cannot be corrected by the permanent overload capability of the converter. Considering a base ov 23 A, this is explored for overloads of 0.565 pu for Cases II and IV and 0.783 pu for Case III. For these imbalances, overload commands of 36 A for Cases II and IV and 41 A for Case III are requested; these commands have a magnitude higher than the permanent overload magnitude and are within the semiconductors TOE shown in Figure 4.20. It can be observed in Figure 4.24 (a)-(c) that for Cases II and IV, the converter is initially able to provide the requested current command of 36 A, which can completely offset the power imbalance, regulating the frequency to its nominal value of 50 Hz, as shown in Figure 4.24 (g)-(i) This current is, however, temporary and decreases to the permanent overload value $I_{ov\,max}$ after approximately 8 s, leading to a second frequency drop because this current magnitude is unable to counteract the total power imbalance in the AC grid; the permanent overload current is, however, able to sustain the frequency to a value closer to the lower frequency operational limit of 49.8 Hz.

For Case III, the extreme power imbalance leads to the regulation of the frequency between the statutory and operational limits, as shown in Figure 4.24 (h). As the transient overload current is decreased from 41 A to its permanent value of 37.2 A, as presented in Figure 4.24 (b), the frequency undergoes a new transient, being regulated to a value slightly below the statutory limit of 48.5 Hz.

The response to this extreme scenario clearly demonstrated that the proposed dynamic rating strategies have a twofold benefit to the regulation of the AC grid frequency. Firstly, the additional (transient) current enables an enhanced operation of the converter by permitting an operation with a new fixed limit (permanent overload) to cope with the primary frequency regulation. Secondly, it can be utilised to counteract the initial frequency transient resulting from extreme power imbalances, allowing other sources to deploy the power in a timely manner in order to aid in the primary frequency regulation.

The "clamping" of the maximum semiconductors temperature to the equilibrium value of each Case can be observed in Figure 4.24 (d)-(f) and are in agreement with the values demonstrated in Figure 4.19 (a)-(d).

The improvement of semiconductors TOE resulting from an increase in the heat sink time constant is shown in Figure 4.25 for Cases II-IV (first to last columns, respectively). The same load increases as for the $I_{ov\,temp}$ scenario, i.e. current imbalances that cannot

be completely corrected by the permanent overload capability of the converter, are considered.

As shown by (4.17) and in Figure 4.21, only the overload duration for a given current overload command is affected when the dominant time constant of the thermal network changes for the different scenarios. Accordingly, the steady-state values of the peak temperatures, in Figure 4.25 (d)-(f) and of the frequency curve in Figure 4.25 (g)-(i) remain unchanged when compared to the corresponding results in Figure 4.24.

The longer overload durations enabled by larger time constants effectively extend the duration of the power support capability, as shown in Figure 4.25 (a)-(c). For Cases II and IV, and for the analysed range, this results in a power support capability that can compensate for the load imbalance for up to 200 s, without the need to deploy secondary frequency regulation responsive sources connected to the AC grid. When the equilibrium temperature is reached, only the maximum permanent current contribution $I_{ov\,max}$ of the converter can be injected, which is sufficient, however, to almost regulate the frequency to an acceptable value above the lower operational limit $f_0 = 49.8\,\mathrm{Hz}$.

Similarly to Cases II and IV, the maximum overload duration for Case III is achieved for the NC scenario, leading to a temporary current overload above the maximum permanent contribution with a duration of approximately 320 s. This results not only from the longer time constant of the heat sink but also from the higher equilibrium temperature reached as a result of the higher proportional gain ($k_p = 100\,\mathrm{A/^\circ C}$).

Results in Figure 4.21 and Figure 4.25 demonstrate the significant system-level benefit of utilising a system with a large time constant as a mean to the extend the semiconductors TOE. It is worth noting the TOE is also dependent on the upper limit of thermal headroom, which underpins the parametrisation of the rating strategy and fundamentally defines the initial overload current command and, consequently, the TOEn of the system. However, for a given system with a certain parametrization of the rating strategy and with a given time constant, it is possible to achieve a similar performance to another system with a higher overload current magnitude by designing its largest time constant properly, as shown by (4.20).

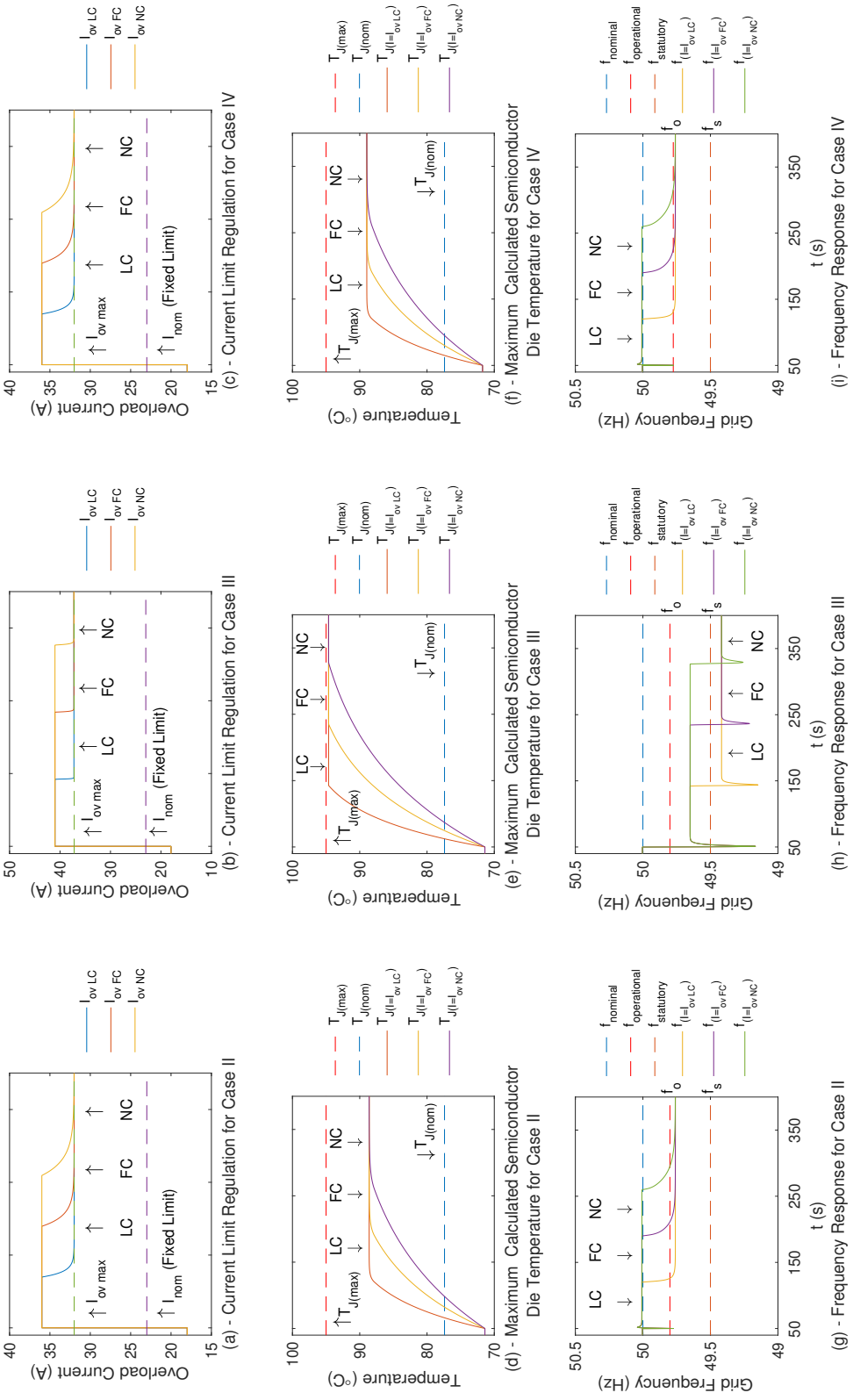


FIGURE 4.25: Frequency regulation during current overload as response to a load increase for different heat sink time constants.

4.7 Summary

This chapter has presented an additional control loop to extend the power transmission capability of a MMC by employing two different dynamic rating strategies, where the current limit is dynamically set in response to the measured semiconductors temperature. The proposed control scheme exploits the available semiconductors thermal headroom to enforce a current magnitude limit that ensures the junction temperature is kept in safe bounds.

The state-space model of the closed-loop system with semiconductor temperature feedback was derived and an eigenvalue analysis was performed to determine appropriate parameters for the dynamic rating strategies and analyse their influence in the stability of the system, with the objective of avoiding temperature overshoots.

Simulation results were presented and compared for an AC Grid-tied MMC with 3 SMs per arm, where the benefits of the rating strategies were analysed for two critical operation scenarios: Cooling System Failure and Current Overload. It was concluded that high proportional gains for Strategy A lead to smaller current curtailments during Cooling Failure and higher Overload Current magnitudes, while the use of an integral term for Strategy B outperforms Strategy A when the same proportional gain is employed is both strategies, for both operational scenarios. The use of high proportional gains, for both strategies, enables the converter to operate permanently in an overload mode, without exceeding the upper limit of the considered thermal headroom.

The TOE for the semiconductor modules was characterised, defining a complete current-time overload operating range. The capability of permanent and transient current overloads to aid in the frequency support of a power distressed AC grid was explored for different scenarios. It was concluded that the converter Current Overload enabled by the proposed dynamic rating strategies has a positive influence on the frequency regulation of the AC grid. Furthermore, depending on the parametrisation of the rating strategies, the converter can not only cope with the Primary Frequency Regulation requirements of the Grid Code, but also use the Current Overload to aid in the Secondary Frequency Response.

Analytical derivations supported by simulation were presented to investigate the effect of the heat sink time constant, the dominant time constant of the thermal network,

on the semiconductors' TOE. Results concluded that for a given configuration of a system, the semiconductors' transient overload capability can be meaningfully improved by employing heat sinks with a large mass. This improvement translates into longer durations of the transient power support capability of the converter, further improving the possibility of providing frequency support to a power-distressed grid.

Chapter 5

Sub-Module Temperature Regulation and Balancing

5.1 Introduction

The dynamic rating strategies proposed in the previous chapter respond to the maximum calculated temperature in the semiconductor dies. This temperature may result from an abnormal temperature increase in a single SM , leading to an unnecessary curtailment of the power transmission capacity of the converter. This chapter proposes a SM capacitor voltage control strategy to regulate and balance the maximum die temperature between the SMs of an arm while controlling the arm voltage to a reference value in order to maintain a particular DC-link voltage. Simulation results are presented to validate the effectiveness of the proposed method.

5.2 Thermal Imbalances in Sub-Modules of Modular Multilevel Converters

For the reliable operation of an MMC, the temperature of the semiconductor switches in the SMs should be limited in order to avoid damages resulting from over-temperature and thermal cycling [291]. Under abnormal conditions such as overload or system cooling malfunction [292], one or more SMs may suffer a large temperature increase. Previous

work [211, 269] has addressed system-level thermal control strategies for 2- and 3-level converters. Although some of this work has been extended for MMCs [279], thermal management strategies operating at the SM-level have not yet been proposed. It has also been shown that it is possible to achieve significantly different temperatures between the SMs of an arm during normal operation due to the load conditions [118], resulting in unequal current and losses distribution between the dies in the semiconductor modules. Recent work [293, 294] proposed the blending of semiconductor devices temperature information on the voltage balancing process. Besides being able to only correct small thermal imbalances, the results are dependent on a subjective weighting factor and a capacitor voltage variation cycling effect may occur.

Long-term operation of an MMC can be affected by capacitance ageing [295], semiconductor modules ageing [214], parameter mismatch between SMs or partial cooling failures [292] that can lead to significant temperature differences among SMs. This poses a significant threat to the normal operation of the MMC as the power semiconductor devices have been identified as the components that fail most often in power electronic converters [296]. Their lifetime is mainly defined by the amplitude of thermal cycles and the junction temperature value [291] and excessive values of either may lead to premature ageing and failure, which in turn affect maintenance strategies and the overall reliability of the converter station [153, 155].

5.3 Voltage-Temperature Regulation and Balancing

Temperature control in power converters may be achieved by the control of semiconductors losses, with the majority of these being conduction losses, as described in Chapter 3. Switching losses in MMCs are usually a small proportion of total losses as a result of a low switching frequency, which is typically a few hundred Hertz [110]. Conduction losses are dependent only on the magnitude of the arm current [118] and are equal in all SMs (each SM has one power device conducting at all times). Therefore, SM temperature can only be controlled independently by modifying switching losses through the modulation of its capacitor voltage. This poses a challenge as typical capacitor voltage algorithms are usually implemented per phase arm [97, 110] in order to regulate all capacitor voltages to a shared nominal value, independent of the load conditions, i.e. they do not allow for independent control of SM capacitor voltages.

5.3.1 Proposed Control Strategy for Individual Sub-Module Voltage Control

A key challenge in MMCs is the balancing of SM capacitor voltages and extensive work has been done in this area. The methods in [100, 104, 107, 110, 115] compare each SM capacitor voltage to an implicit reference of $\frac{v_{DC}}{N}$, i.e. the DC link voltage is shared equally by the operating SMs. A modification of the classic MMC capacitor voltage balancing scheme [60] is proposed here to allow independent regulation of $N-1$ SM voltages within an arm while maintaining the total arm voltage regulated at a reference value.

The modified SM capacitor voltage balancing strategy is based on that proposed in [68] and shown in Figure 2.15. However, unlike the original per-phase balancing strategy, the strategy proposed in this work is implemented per arm and enables direct SM capacitor voltage control while keeping the total arm voltage regulated to its reference value. This strategy is shown in Figure 5.1 for the upper arm of a MMC with N SMs and comprises two cascaded control levels:

1. Averaging Control, implemented per arm and used to enforce an average capacitor voltage of $v^*_{SM\,nom} = \frac{v^*_{arm}}{N}$ across all SMs in an arm, thus regulating the arm voltage to its reference v^*_{arm};

2. Balancing Control, implemented for each SM k and responsible for forcing each capacitor voltage $v_{C\,k}$ to follow an individual reference $v^*_{SM\,nom} + \Delta v_{SM\,k}$.

The additional control blocks of the MMC control remain unchanged, including the DC voltage feed-forward, the AC reference waveform V_{ref} from the higher level VSC control and the capacitor voltage feed-forward and modulation functions, as shown in Figure 2.15.

5.3.2 Proposed Control Strategy for Sub-Modules Temperature Regulation

A SM temperature equalisation method is proposed that compensates for thermal imbalances across the SMs by modulation of the capacitor voltages and thereby modulation

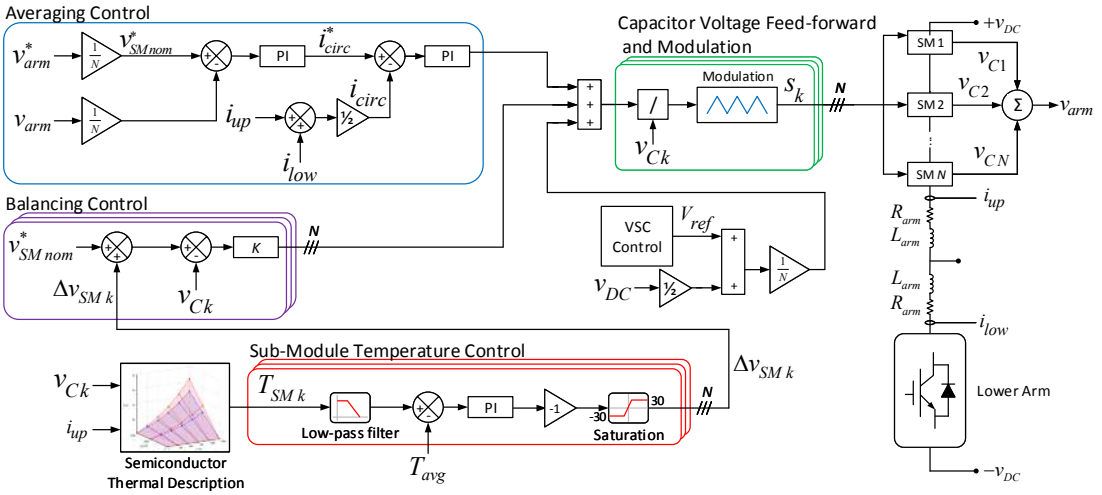


FIGURE 5.1: Proposed per-arm individual SM voltage control strategy with temperature regulation and balancing.

of switching losses. When a SM possesses a higher temperature than the others, its voltage is decreased and the available operating voltage margin in the remaining SMs is exploited in order to compensate for this decrease, ensuring the total arm voltage, and therefore the DC-link voltage, remains constant.

Temperature control is exerted using the voltage difference input Δv_{SM}: Δv_{SM} is responsible for modifying each SM voltage from a starting assumption of equal voltages. The voltage differences $\Delta v_{SM\,k}$ are set as a function of the temperature of SM k by a dedicated SM temperature control loop, as illustrated in the bottom of Figure 5.1. The SM temperature is set to the maximum value of the individual die temperatures in each SM k:

$$T_{SM\,k} = \max\{T_{Q1\,k}, T_{D1\,k}, T_{Q2\,k}, T_{D2\,k}\} \tag{5.1}$$

And compared with the average temperature T_{avg} in the arm:

$$T_{avg} = \frac{1}{N}\sum_{k=1}^{N} T_{SM\,k} \tag{5.2}$$

The difference is fed to a PI controller which will determine the voltage difference Δv_{SM} to be added to each individual SM voltage reference in the balancing control. A first-order low-pass filter is included to smooth the temperature measurement due to noise.

This scheme ensures that a single SM is not solely responsible for voltage balancing, i.e. there is no 'master' SM used to achieve thermal regulation: all available SMs participate equally in the voltage-temperature balancing process.

5.3.3 Considerations Regarding Capacitor Voltage Modulation

The use of the SM voltage as a mean for temperature control needs to be performed carefully. The arbitrary arm voltage sharing within the SMs aiming for the thermal regulation and balancing of the SM temperatures has to account for the maximum operating rating of each SM so that its maximum operating voltage is not exceeded.

Considering a semiconductor module with a maximum rated voltage v_{MAX} and a nominal SM operating voltage $v_{SM\,nom}$, its voltage limits and different operating areas are presented in Figure 5.2. The voltage balancing margin is here defined as the span of capacitor voltage balancing variation, where a value $\delta v_{SM\,nom} \pm 10$ % is typically considered [54] around the average capacitor voltage $v_{SM\,nom}$. The operational voltage margin available to be explored by the SM temperature control loop is, effectively, the exploitable voltage slack between the maximum nominal operating voltage plus half the voltage balancing margin $\delta v_{SM\,nom}$, and the voltage limit $v_{SM\,max}$ for the safe operation of the semiconductors. This ensures the necessary voltage margin to survive transients such as those resulting from SM bypass and fault ride-through. The forbidden operating area corresponds to the remaining possible voltage value up to the upper limit v_{MAX}, which is the maximum value between the rated capacitor voltage and the semiconductor SOA maximum voltage given the nominal current.

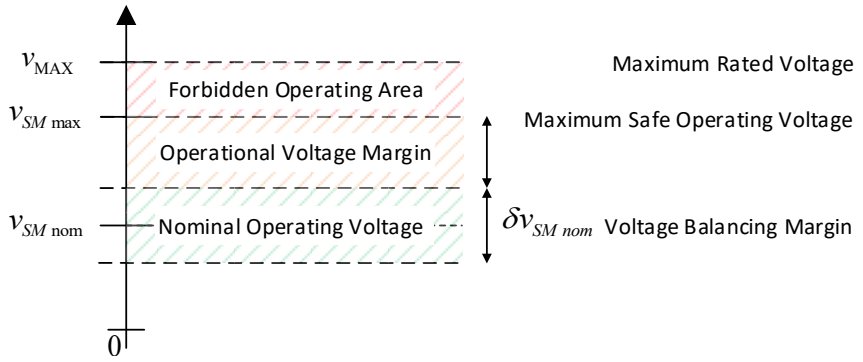


FIGURE 5.2: Operational voltage limits in a SM.

To ensure the capacitor voltage of each SM is properly regulated up to a maximum value of $v_{SM\,max}$, saturation blocks are included in the proposed SM temperature control loop, as shown in Figure 5.1, and the PI controllers have back-calculation anti-windup mechanism [280].

5.3.4 Stability of Sub-Module Temperature Regulation

The proposed SM temperature control loop regulates SM capacitor voltages to prevent SM temperature from reaching dangerous values and must therefore avoid temperature overshoots. Using the principle of bandwidth separation between the cascaded loops and neglecting constant disturbances, the open-loop transfer function $G_{OLT}(s)$ of the system can be defined as:

$$G_{OLT}(s) = K_{pT}\left(\frac{1+sT_{iT}}{sT_{iT}}\right)\left[K_c\left(\frac{1}{1+\tau}\right)\left(\frac{1}{1+sT_{eq}}\right)\right] \tag{5.3}$$

where the gain K_c is defined as:

$$K_c = \left(\frac{KR_{th\,JC\,I}E_{Total}\left(I_{rms}\right)f_{sw}}{3v_{CE}^{ref}}\right) \tag{5.4}$$

and K_{pT} and T_{iT} are the proportional gain and integral time constant, respectively, of the PI controller in the SM temperature control loop of Figure 5.1, τ is the low-pass filter time constant and $T_{eq} = 1/2f_{sw}$ corresponds to the delay of the control loop due to the PWM scheme.

The modulus optimum criterion [297] is utilised to tune the PI controller in the SM temperature control loop. The zero of the PI controller is selected to cancel the largest time constant, while the closed loop gain should be larger than unity for as high frequencies as possible. The PI controller parameters are defined as:

$$\begin{cases} K_{PT} &= \frac{\tau}{2T_{eq}K_c} \\ K_{IT} &= \tau \end{cases} \tag{5.5}$$

and the open-loop transfer function becomes:

$$G(s) = \frac{1}{2T_{eq}} \frac{1}{s(1 + sT_{eq})} \tag{5.6}$$

From which can be observed that the system possesses one pole at the origin and one real pole located at $\omega_n = -1/Teq = -5000\, s^{-1}$. The system is, therefore, stable and there will be no oscillations or overshoot in the temperature.

The Bode plot of the transfer function in (5.6) is shown in Figure 5.3, where it can be observed that the system possesses a generous phase margin of 65° and an infinite gain margin. Although this is, in practice, a finite value, it means that the system can robustly handle phase uncertainty and time delays, typically present in experimental systems.

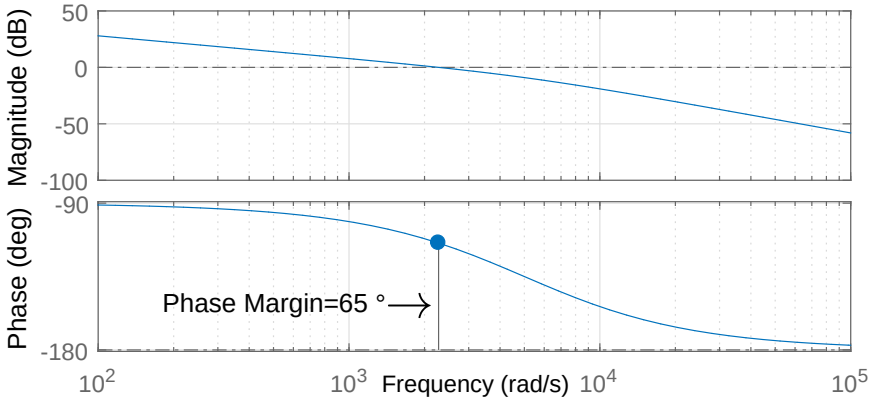


FIGURE 5.3: Bode Diagram of the SM temperature control open-loop transfer function.

5.3.5 Analysis and Limitations of the Thermal Regulation

Considering a SM operating with a capacitor voltage $v_{SM(0)}$, its initial (maximum SM) temperature of $T_{J(0)}$ is determined by:

$$T_{J(0)} = P_{Losses(0)} R_{th} + T_{m\,0} \tag{5.7}$$

When an external thermal disturbance ΔT is applied to the SM and temperature regulation does not occur, as presented in Figure 5.4, the temperature will rise to $T_{J(2)}$:

$$T_{J(2)} = P_{Losses(2)} R_{th} + T_{m\,0} + \Delta T \tag{5.8}$$

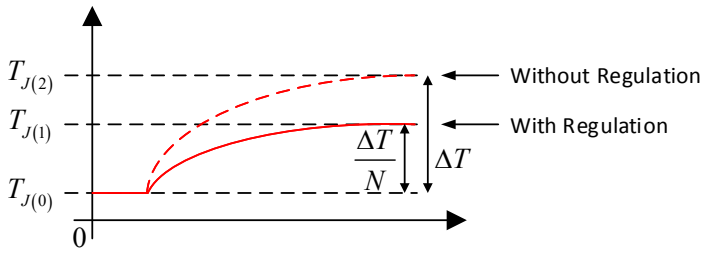


FIGURE 5.4: SM temperature profile with and without thermal regulation when subjected to a thermal disturbance.

The thermal disturbance can, for instance, be caused by an increase in the thermal resistance of the module due to ageing [214] or result from a partial cooling failure of the system [292], resulting in an increase of the measured temperature value T_m.

If the proposed thermal regulation process is implemented, and assuming $v_{SM\,max}$ has not been reached, i.e. there is an operational voltage margin in the SMs, each of the N available SMs will share an equal part $\frac{\Delta T}{N}$ of the total disturbance and the new SM voltage will be regulated to:

$$v_{SM\,1} = v_{SM\,0} + \Delta v_{SM} \tag{5.9}$$

And the new $T_{J(1)}$ temperature will be lower:

$$T_{J(1)} = T_{J(0)} + \frac{\Delta T}{N} = P_{Losses(1)} R_{th} + T_{m\,0} + \Delta T \tag{5.10}$$

Substituting (3.20) into (5.10) and expanding, yields:

$$\begin{aligned} T_{J(1)} &= \underbrace{\left[\left(V_0 + V_1 T_{J(0)}\right) I_{avg} + \left(R_0 + R_1 T_{J(0)}\right) I_{rms}^2 + \left(E_0 I_{rms} + E_1 I_{rms}^2\right) \frac{v_{SM\,(0)}}{V_{CE}^{ref}} f_{sw} \right]}_{P_{Losses(0)}} R_{th} \\ &\quad + T_{m\,0} + \Delta T + \left[\frac{\Delta T}{N} \left(V_1 I_{avg} + R_1 I_{rms}^2\right) + \left(E_0 I_{rms} + E_1 I_{rms}^2\right) \frac{\Delta v_{SM}}{V_{CE}^{ref}} f_{sw} \right] R_{th} \\ &= T_{J(0)} + \Delta T + \left[\frac{\Delta T}{N} \left(V_1 I_{avg} + R_1 I_{rms}^2\right) + \left(E_0 I_{rms} + E_1 I_{rms}^2\right) \frac{\Delta v_{SM}}{V_{CE}^{ref}} f_{sw} \right] R_{th} \end{aligned} \tag{5.11}$$

The average I_{avg} and rms I_{rms} currents refer to the respective values of the hottest die in the SM. Equating (5.10) and (5.11) results in:

$$\frac{\Delta T}{N} = \Delta T + \left[\frac{\Delta T}{N} \left(V_1 I_{avg} + R_1 I_{rms}^2 \right) + \left(E_0 I_{rms} + E_1 I_{rms}^2 \right) \frac{\Delta v_{SM}}{V_{CE}^{ref}} f_{sw} \right] R_{th} \tag{5.12}$$

Rearranging (5.12) as a function of the voltage difference Δv_{SM} yields:

$$\Delta v_{SM} = \frac{\Delta T \left(\frac{1}{N} \left(1 - R_{th} \left(V_1 I_{avg} + R_1 I_{rms}^2 \right) \right) - 1 \right)}{R_{th} \left(E_0 I_{rms} + E_1 I_{rms}^2 \right) \frac{f_{sw}}{V_{CE}^{ref}}} \tag{5.13}$$

The remaining SMs aiding in the thermal regulation, with an initial voltage $v_{SM\,0} = v_{SM\,nom}^{*}$, will suffer a voltage regulation to a new value $v_{SM\,\chi}$ given by (cf. Figure 5.1):

$$v_{SM\,\chi} = \frac{v_{arm}^{*} - v_{SM\,0} + \Delta v_{SM}}{N - 1} \tag{5.14}$$

It can be observed from (5.13) that the magnitude of the voltage difference Δv_{SM} is inversely proportional to the number of SMs N and directly proportional to the magnitude of the thermal disturbance ΔT. Accordingly, for a given thermal disturbance, the larger the number of SMs, the smaller the capacitor voltage variations become.

The proposed strategy leads to an even distribution of the thermal stress across the operating SMs at all times, without using redundant SMs typically included in MMCs [51]. The redundant SMs are therefore still available to be used as a failsafe functionality, e.g. if excessive temperatures destroy a semiconductor module or if further problems such as internal SM faults occur, ensuring the MMC can operate with a high reliability [155].

5.4 Results

The proposed method is validated using the parameters of the MMC shown in Table 4.2. The thermal network of Figure 4.12 is implemented for HB semiconductor modules using the datasheet parameters in Table 4.1; $\tau_{HS\,Cool}$ has been updated to 75 s to better

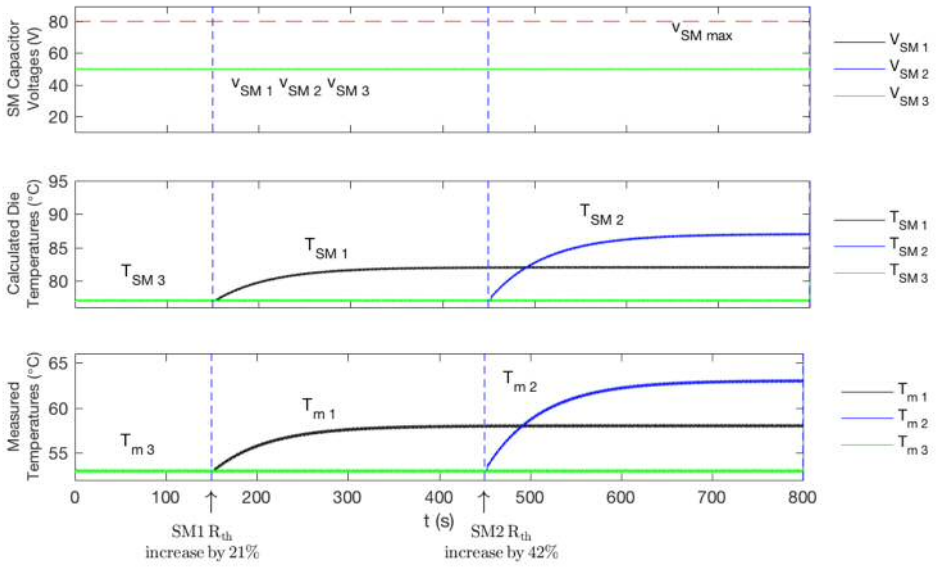
replicate the conditions of the experimental setup. A PS-PWM modulation scheme with interleaved carriers is considered and, as explained in subsection 4.5.3, the frequency f_{sw} of the triangular carriers is set to 2.5 kHz to allow the $\frac{v_{SM}}{v_{CE}^{max}} f_{sw}$ ratio in (3.10)-(3.10) to approximate the operating electrical conditions of a commercial SM. A maximum operating voltage of $v_{SM\,max} = 80$ V (60 % voltage increase) is considered.

A thermal disturbance is assumed to result from partial cooling system failures, resulting in temperature increases of 5 °C and 10 °C. This corresponds to an increase of 21 % and 42 %, respectively, in the thermal resistance to ambient of the semiconductor module. The MMC operates as an inverter and is composed of three SMs (SM 1-3); the disturbances are applied to SM 1 and SM 2, at 150 s and 450 s, respectively.

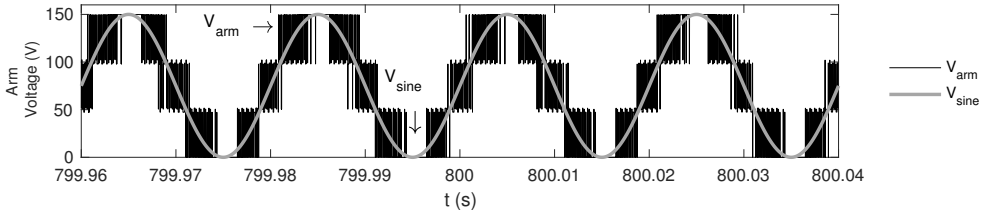
5.4.1 Scenario I: Thermal Disturbance without Voltage Regulation for a small number of SMs

The response of the SM voltages, maximum calculated die and measured temperatures are shown in Figure 5.5 (a), when the thermal balancing algorithm is not active, i.e. individual SM voltage control does not occur and the SMs voltages are balanced around their nominal value $v^*_{SM\,nom} = 50$ V. For a peak arm current of 23 A the maximum calculated die temperatures are the same in all SMs, with the lower IGBT Q2 (see Figure 4.15) in each module having the highest temperature (≈ 77 °C); this determines the T_{SM} temperature to be used for the voltage regulation process.

When the increase in the thermal resistance is applied to SM 1 and SM 2 at $t = 150$ s and $t = 450$ s, respectively, their measured and calculated junction temperatures start to increase with a time constant $\tau = RC = 0.45 \times 167 \approx 75$ s, imposed by the thermal resistance and the thermal capacitance of the heat sink and the coolant. When the temperatures reach steady-state, 5 °C and 10 °C temperature imbalances exist between SM 1 (82 °C) and SM 2 (87 °C), and SM 3 (77 °C), respectively, for both measured case temperatures and calculated die temperatures. Since the thermal balancing algorithm is not enabled, the SM capacitor voltages remain unchanged and generate a standard 4-level arm voltage waveform, regulated to its nominal peak value of 150 V as shown in Figure 5.5 (b). The waveform has a Total Harmonic Distortion (THD) value of 35.47 %.



(a) - SMs' voltages and temperatures



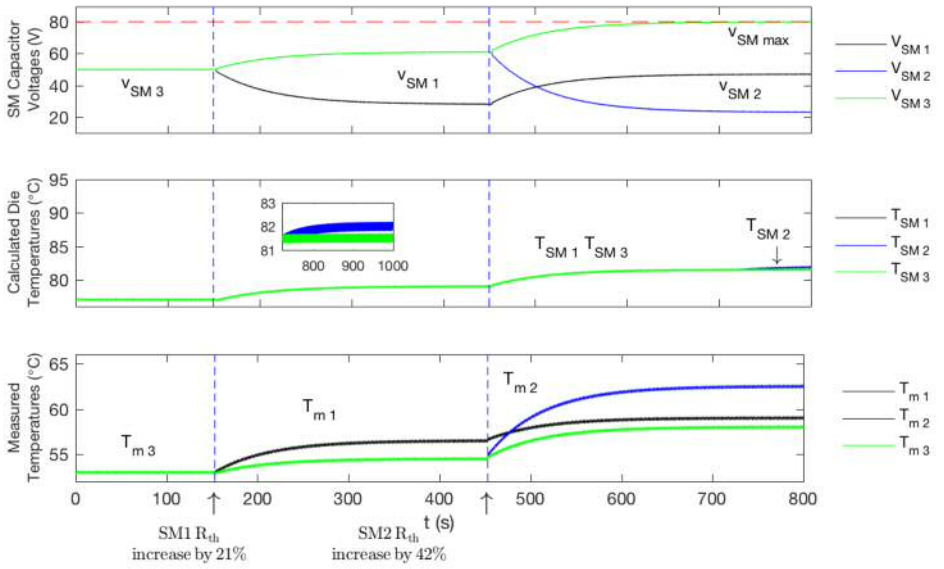
(b) - Multilevel arm voltage waveform

FIGURE 5.5: Simulation of response of SMs' voltages and temperatures to thermal imbalances without thermal regulation.

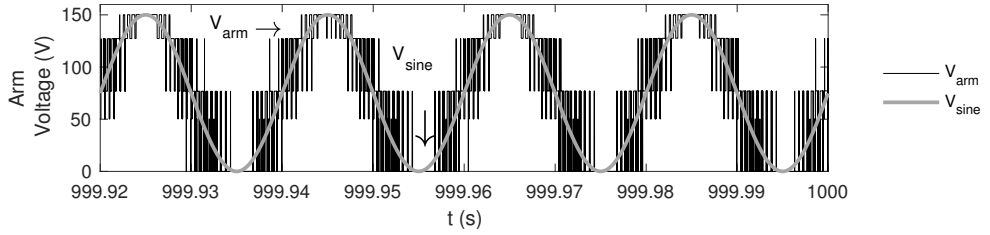
5.4.2 Scenario II: Thermal Disturbance with Voltage Regulation for a small number of SMs

The results with the proposed balancing control are shown in Figure 5.6 (a). When the thermal resistance of SM 1 increases at $t = 150\,\text{s}$ and its temperature starts to increase, its capacitor voltage is decreased to 28 V ($\Delta v_{SM} = 22\,\text{V}$); the difference to the nominal value is equally compensated by an increase in both SMs 2 and 3 capacitor voltages to $\frac{150-28}{2} = 61\,\text{V}$. This results in all the SM calculated die temperatures being equalised at approximately 78.5 °C (middle plot), despite the cases of the semiconductor modules operating at different temperatures (bottom plot). These results are in agreement with the expected capacitor variation of $\Delta v_{SM} = 22.07\,\text{V}$ obtained using (5.13) and $v_{SM\,\chi} = \frac{150-50+22.07}{3-1} = 61.04\,\text{V}$ using (5.14).

When the thermal resistance of SM 2 increases at $t = 450\,\text{s}$, its temperature will initially



(a) - SMs' voltages and temperatures



(b) - Multilevel arm voltage waveform as a result of unbalanced SM voltages

FIGURE 5.6: Simulation of SMs thermal regulation as a response to thermal imbalances.

increase faster as the result of a larger disturbance. Similarly to the initial disturbance applied to SM 1, SM 2 capacitor voltage is diminished as a means to regulate the maximum die temperature. The voltage difference to the nominal value of 50 V is compensated by an increase in the voltage of SM 3 and SM 1, whose voltage was decreased previously as a result of the first disturbance. At approximately $t = 720\,s$, SM 3 voltage reaches the maximum operating limit $v_{SM\,max} = 80\,\text{V}$ and since SM 1 voltage was regulated to 47 V to ensure a thermal equilibrium is reached, SM 2 voltage is further decreased to 23 V in order to ensure the arm voltage is set at 150 V. Although SM 1 and SM 3 reach a thermal equilibrium temperature of 81.5 °C, SM 2 temperature continues to increase, reaching a steady state value of approximately 82 °C.

While the total arm voltage v_{arm} remains regulated to 150 V, as shown in Figure 5.6 (b), the multilevel waveform appears distorted when compared to Figure 5.5 (b) as a result of unbalanced SM voltages, and its THD increases to 47.75 %. Nonetheless, the use of SM capacitor voltage feed-forward, shown in Figure 5.1 (b), enables the fundamental

component of the arm voltage (v_{sine}) to remain unchanged.

5.4.3 Scenario III: Thermal Disturbance with Voltage Regulation for a large number of SMs

The consideration of only three SMs in an arm limits to two the number of SMs available to assist in the thermal regulation of a 'hot' SM. Consequently, only small imbalances can be corrected, at the expense of quite divergent capacitor voltages, as shown in Figure 5.6 (a). In HVDC applications, where dozens or hundreds of SMs are used, temperature control can be achieved using smaller capacitor voltage variations from their nominal value, as demonstrated by (5.13), resulting in significantly lower multilevel voltage waveform distortion.

Considering an MMC with 10 SMs per arm, the system data from [279] and presented in Table 5.1 is used to analyse the scalability of the proposed method. ABB HiPak 5SNA 0650J450300 semiconductor modules [298] are employed and two cascaded disturbances of 10 °C are applied to two SMs (SM 1 and SM 2), with the results being shown in Figure 5.7 (a). It can be observed that the thermal disturbances lead to a final value of 3.17 kV (5.6% voltage variation) for all the SMs sharing the additional voltage, compared to a maximum variation of 30 V (60%) for SM 1 in the MMC with only 3 SMs; this means that higher thermal imbalances can be corrected with smaller relative capacitor voltage variations. The temperature increase in the SMs sharing the voltage burden is also smaller, $\approx 1\,^{\circ}$C per thermal disturbance per SM, given its division by the higher number of available SMs.

TABLE 5.1: Parameters of the MMC with 10 SMs per arm.

Parameter	Value	Unit
Number of SMs per arm (N)	10	-
SM capacitance (C_{SM})	5	mF
Arm inductance (L_{arm})	3	mH
Nominal SM voltage ($v^*_{SM\,nom}$)	3.0	kV
Nominal (reference) arm voltage (v^*_{arm})	30	kV
Carrier frequency (f_{sw})	500	Hz
Fundamental frequency (f_0)	50	Hz
Nominal coolant temperature ($T_{Coolant}$)	50	°C

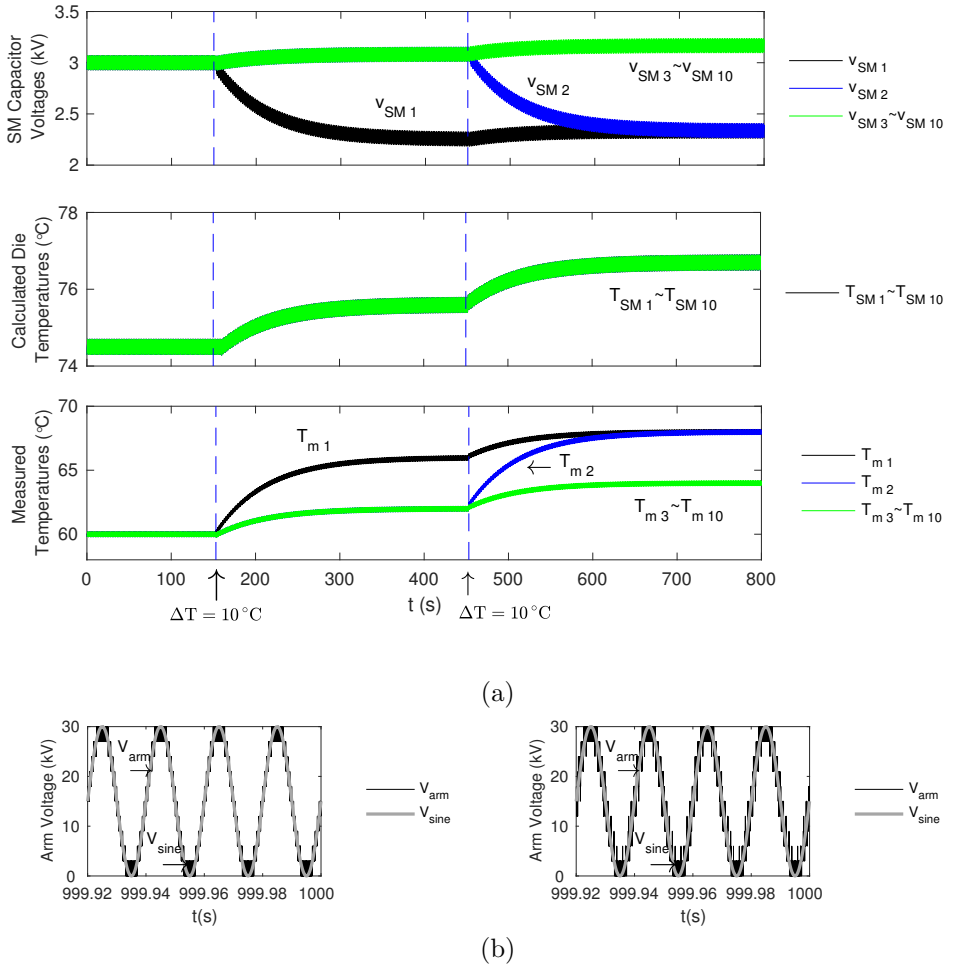


FIGURE 5.7: SMs thermal regulation for a thermal disturbance: (a) - Sub-Modules' voltages and temperatures and (b) - Multilevel arm voltage waveform without (left) and with (right) unbalanced SM voltages as a result of thermal regulation.

Thermal imbalances of 10 ° C lead to a voltage variation of 750 V in SM 1 and SM 2, which is in good agreement with $\Delta v_{SM} = 749.35\,\text{V}$ obtained using (5.13). After the first imbalance, the unaffected SM voltages are regulated to $v_{SM\,\chi} = \frac{30000-3000+749.35}{10-1} = 3083.26\,\text{V}$, which represents a 2.8 % voltage increase from their nominal value. A similar voltage regulation occurs after the second 10 ° C imbalance, resulting in final SM voltages of $v_{SM\,\chi} = \frac{30000-2250+749.35}{10-1} = 3166.59\,\text{V}$, also in good agreement with the value of 3.17 kV obtained in simulation.

The arm voltage waveform resulting from uneven SM voltages due to the thermal regulation is shown on the right in Figure 5.7 (b). It can be observed that there is a very little increase in distortion (THD = 11.61 %), compared to the waveform shown on the left in Figure 5.7 (b), where the proposed algorithm is not enabled and there is no SM voltage regulation (THD = 11.08 %). Although SM capacitor voltage feed-forward allows the

fundamental components of the arm voltage to remain unchanged, there is, effectively, a trade-off between SM thermal regulation and the quality of the output voltage waveform.

5.4.4 Influence of the Thermal Imbalance Amplitude and Number of SMs in the Thermal Regulation

For the MMC with 10 SMs per arm, the SM voltages that are regulated to correct thermal imbalances between the SMs in an arm are shown in Figure 5.8. Results are presented as a function of the number of SMs and for different thermal disturbances.

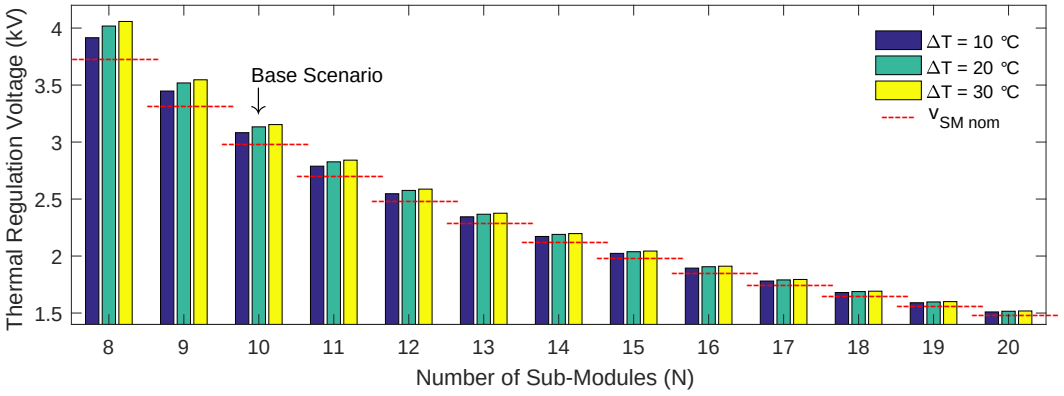


FIGURE 5.8: SMs thermal regulation voltages as a function of the number of SMs for different thermal imbalances.

It can be observed that for any number of SMs N, the larger the thermal imbalance, the higher the SM voltage variation from its nominal value. However, as the number of SMs increases, these variation differ very little in amplitude as they are shared by a higher number of SMs, in accordance with (5.14). This can observed more clearly in Figure 5.9, where the voltage variations are shown in terms of percent variation: as the number of SMs increases, and for the same reference arm voltage, the nominal SM capacitor voltage becomes smaller, which means that for the same thermal imbalance, smaller voltage variations are required in order to correct the temperature imbalance between SMs, as defined by (5.13).

In Figure 5.9 it can also be observed that, especially for the thermal imbalances of 20 °C and 30 °C, a higher number of SMs makes the required voltage variation necessary for thermal regulation of these imbalances almost identical. Thus, an increase in the number of SMs seems to result in a higher thermal disturbance management capability with minimal influence in the SM capacitor voltage variation, and very little utilisation

of the Operational Voltage Margin presented in Figure 5.2. This is confirmed by the results in Figure 5.10, where the THD of the arm voltage is presented as a function of the number of SMs and for different thermal imbalances.

It can be observed that the effect of the amplitude of the disturbance and the THD of the arm voltage waveform becomes less significant as the number of SMs increases, thus minimising the trade-off between SM thermal regulation capability and the quality of the output voltage waveform, clearly visible in Figure 5.6 for the system with only three SMs.

As the number of SMs increases to values commonly in HVDC systems, e.g. 400 [53], it can therefore be expected that significant thermal imbalances can be accommodated while simultaneously respecting the THD limit of 3% [106, 299] at the connection point with the AC grid of the Transmission System Operator. Thus, the proposed SM temperature regulation and balancing strategy allows the converter to operate with significant

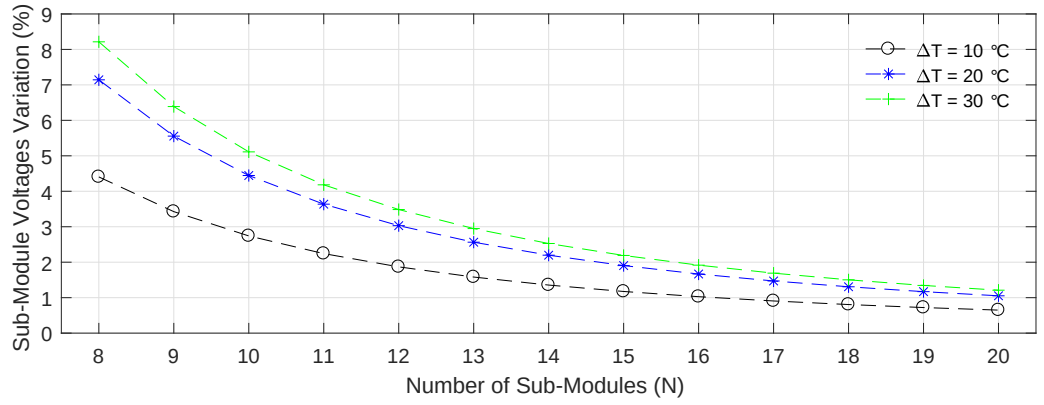


FIGURE 5.9: SM voltages variation as a function of the number of SMs for different thermal imbalances.

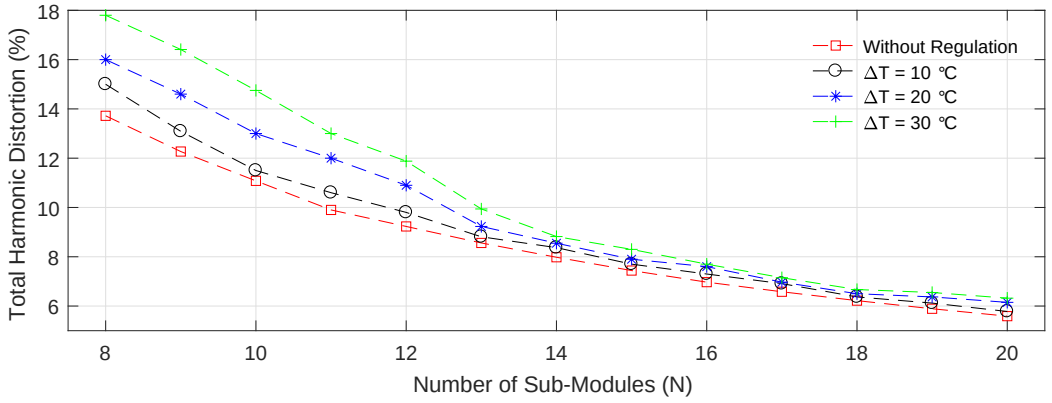


FIGURE 5.10: Arm voltage total harmonic distortion as a function of the number of SMs for different thermal imbalances.

thermal imbalances between the SMs without affecting the system-level functions of the converter or violating the power quality requirements.

5.5 Summary

This chapter presents a method that enables direct SM capacitor voltage control in MMC-based applications, while keeping the total arm voltage regulated to its reference value. Based on this method, a dedicated SM temperature control loop is proposed for each SM. In this control strategy, temperature control is exerted by controlling the capacitor voltage of each SM in order to equalise the estimated junction temperatures, ensuring similar thermal conditions for the semiconductor dies. This is expected to translate into a similar lifetime expectation for all the SMs [300], leading to an increased converter reliability [155] and more predictable lifetime behaviour when compared to strategies without thermal regulation and balancing.

The effectiveness of the proposed method has been demonstrated by simulation of two MMCs with 3 and 10 SMs per arm. For systems with a reduced number of SMs, a distorted multilevel arm voltage waveform is produced from unbalanced capacitor voltages, although its fundamental frequency component remains unchanged. As the number of SMs increases, higher thermal imbalances can be corrected with smaller capacitor voltage variations, which results in a negligible increase in the voltage waveform distortion.

The use of an estimation of the temperature in the dies eases the implementation of the proposed method. The temperature calculation procedure utilised in this chapter relies on accurate knowledge of the semiconductor module parameters such as turn-on and turn-off energies and thermal resistances, which were assumed to be constant over the lifetime of the converter. In practice, their values may change as the modules age, e.g. thermal resistances may increase due to the formation of thermal voids in the solder layer of the module, which can be addressed by employing online thermal resistance monitoring methods such as [215].

Chapter 6

Experimental Tests

6.1 Introduction

This chapter presents a scaled-down MMC-based experimental platform to validate the active thermal control strategies and the SM temperature regulation and balancing algorithm in the simulation work demonstrated in Chapter 4 and Chapter 5. A simplified reduced-order setup with dedicated control loops is proposed to validate and replicate the full-scale MMC operation and key results of the experimental system will be presented and discussed.

6.2 Reduced-Order Modular Multilevel Converter Setup

6.2.1 Rationale and Description

The research on MMC control and operation has mainly focused on system-level phenomenon such as CVB [61, 66, 92, 99, 100, 102, 104, 107, 108, 110, 114–116, 301] and circulating current suppression [120–122, 124, 126, 127]. Studies on the SM and sub-SM level are not common, especially the ones addressing electro-thermal performance and its impact on the operation of the converter. In addition to detailed and averaged simulation models [53, 60], experimental validation [99, 104, 114, 115, 140] is frequently envisaged to demonstrate the validity of the claims.

The construction of a 3-phase MMC, even with a reduced rating and only a few SMs per arm, is costly and time consuming. The use of synthetic tests circuits allows a detailed study of phenomena at the SM or valve level and provides an economic alternative for testing a representative part of an MMC valve [302–304]. Nonetheless, they require complex setups and extensive component requirements, and are not capable of including a DC component in the (arm) current flowing through the SMs with non-zero active power conversion.

The test of individual SMs proposed in [305] and improved in [306] overcomes the galvanic isolation problem of the previous approaches and allows a more in-depth understanding of electro-thermal and electro-magnetic phenomena of the SM and sub-SM level. However, it provides a narrow scope for the interpretation of the results as higher-level phenomena cannot be investigated. Furthermore, the international standard IEC 62501 [307] requires that an MMC valve consisting of several SMs should be tested to validate the converter operation and associated electrical circuits with respect to current, voltage and temperature stresses [304].

In order to understand detailed electro-thermal interactions on the sub-SM level but keeping the system-level phenomena at sight, a complete MMC arm with three SMs is considered in this work, as illustrated in Figure 6.1 (a). The objective is to allow a detailed study of the operation and control of MMCs, while reducing the complexity of an experimental platform of a complete three-phase of single-phase MMC. Recalling the complete single-phase MMC presented in Figure 2.7 and Figure 6.1 (a), and considering one of the arms, such as the lower one, the mathematical model of this system was defined by (2.4) in Subsection 2.3.1:

$$V_g = -V_{DC}^L + V_{arm}^L + R_{arm} i_L + L_{arm} \frac{di_L}{dt} \tag{6.1}$$

Moving the first term in the right-hand side of (6.1) to the left-hand side yields:

$$V_g + V_{DC}^L = V_{arm}^L + R_{arm} i_L + L_{arm} \frac{di_L}{dt} \tag{6.2}$$

Which simply shows that each arm, in this case the lower arm, can be seen as a two-port device. When applied a supply voltage waveform of "$V_g + V_{DC}^L$" and receiving

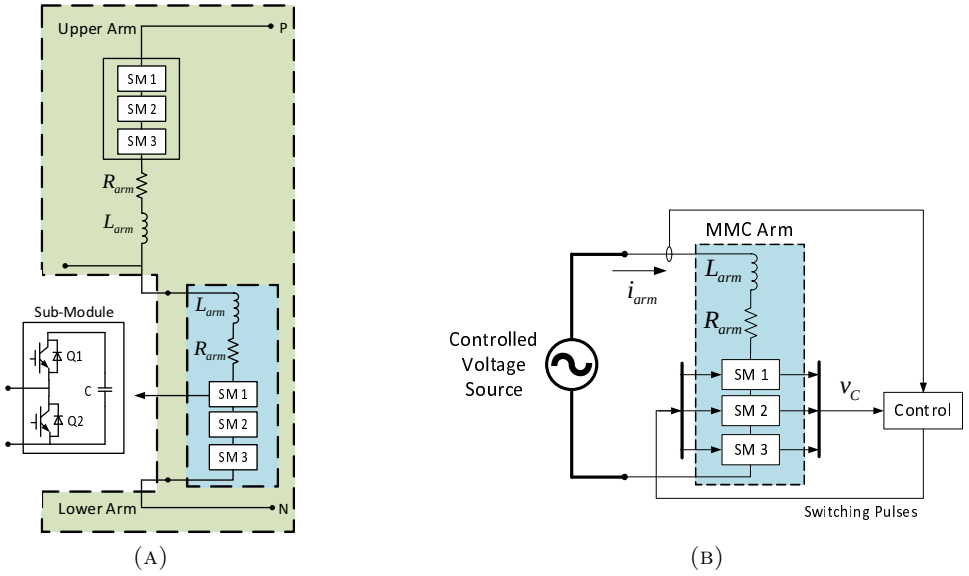


FIGURE 6.1: MMC setup: (a) - Complete phase leg and (b) - Reduced-order arm setup.

appropriate control signals, this two-port device will behave as it is operating in a full converter, as shown in Figure 6.1 (b). Designating the left-hand side term of (6.2) as the supply voltage V_{supply}, V_{arm}^{L} as the voltage V_{arm} and i_L as the arm current i_{arm}, the mathematical model of the MMC Arm can be represented as:

$$V_{supply} = V_{arm} + R_{arm} i_{arm} + L_{arm} \frac{di_{arm}}{dt} \tag{6.3}$$

From (6.3) it can be observed that equivalent supply voltage V_{supply} contains an alternating component, corresponding to the AC side grid voltage V_g, and a DC component V_{DC}^{L}, corresponding, under normal conditions, to half the value of the total pole-to-pole DC voltage. Recalling (2.18), (2.22) and (2.24), it can be observed that the peak value of V_g in (6.2) equals half the value of the total DC voltage, assuming the SMs are capable of generating the nominal arm voltage. Consequently, V_{supply} will be a fundamental frequency sinusoidal waveform with an offset that eliminates the negative half-cycle of the AC voltage, causing it to vary between 0 and the DC voltage in the full setup, as described by (2.21). Hence, a similar operation to the complete MMC can be obtained by using the MMC Arm setup shown in Figure 6.1 (b) and a controllable voltage source that can output V_{supply}.

6.2.2 Operation and Control

The reduced MMC arm setup aims to attain a simplified, yet sufficient electrical and thermal representation of the operation of a complete MMC. Consequently, in order for the setup to be faithful representation of the complete system, both high-level and device-level controls must be the same. Although this can be easily achieved for a single-SM setup and the application of pre-recorded signals [305], dynamic operational scenarios as a result of time-variant control signals are required. For a complete arm, besides current control and multilevel arm voltage waveform generation, this requires the control of individual SM voltages, replicating the features enabled by the control loops in Figure 5.1.

A new control strategy, based on the control proposed in Figure 5.1 is proposed for the single arm setup presented in Figure 6.1 (b) and is shown in Figure 6.2. The averaging and balancing control functions of the arm are now replaced by arm voltage and SM capacitor voltage control loops, respectively. The output $i^*_{arm\,dc}$ of the arm voltage control is an offset added to the arm current reference i^*_{arm} and used to decrease/increase the voltage signal before the PWM modulation and thereby simultaneously discharge/charge all capacitors. This mechanism is used to make the total arm voltage equal to its reference value.

The SM capacitor voltage control is implemented for each SM in the arm and is responsible for forcing the capacitor voltage of each SM to follow its reference, made of two parts:

1. A nominal reference set to $v^*_{SM\,nom} = \frac{v^*_{arm}}{N}$ that represents an equal sharing of the reference arm voltage v^*_{arm} by N SMs;
2. A voltage difference Δv_{SM}, responsible for modifying the voltage reference for each SM.

The voltage difference inputs Δv_{SM} remain determined according to the temperature of each SM, by the same SM temperature control loop. The measured voltages feedback to the Arm Voltage Controller ensures the arm voltage remains regulated at its reference, despite the possible differences in the SM voltages due to the voltage differences Δv_{SM}.

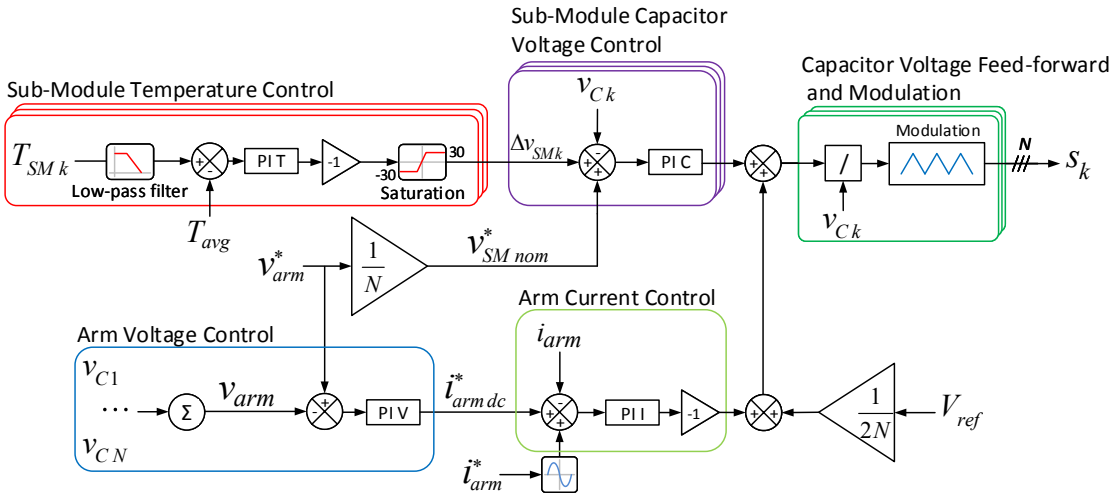


FIGURE 6.2: Control strategy of the reduced-order MMC converter arm.

For each SM the capacitor voltage is also included as a feed-forward term and phase-shifted carriers are used in the modulation step.

The arm current control is a typical current control loop where the measured arm current i_{arm}, common to all SMs, is controlled directly [120] to its reference i^*_{arm} (peak) value. This control scheme allows the different control functions in the arm (individual SM voltages, arm voltage and arm current) to replicate the conditions in a complete MMC.

The arm current reference i^*_{arm} is multiplied by a sine wave generator synchronised with the reference angle θ derived from the supply voltage V_{supply} via a PLL. Due to the circulating current control loop in Figure 5.1, this waveform only contains a fundamental frequency (50 Hz) component. If desired, harmonic components corresponding to the circulating current (at twice the fundamental frequency) or of higher order can be included.

6.2.3 Controller Design

The control strategy of the reduced-order MMC Arm shown in Figure 6.2 is a Multiple-Input Multiple-Output (MIMO) system. Considering a system with three SMs per arm, the arm voltage reference v^*_{arm}, arm current reference i^*_{arm} and the voltage differentials $\{\Delta v_{SM\,1}, \Delta v_{SM\,2}, \Delta v_{SM\,3}\}$ are the inputs to the system. The SM capacitor voltages $\{V_{C\,1}, V_{C\,2}, V_{C\,3}\}$, the arm voltage v_{arm} and the arm current i_{arm} are the outputs.

The tuning of controllers in MIMO systems is affected by the multiple loop interactions between the different input and output signals. However, the MIMO system can be decomposed in several SISO tuning problems using the bandwidth separation principle if there is no coupling between the plants. In the tuning process of PI controllers for VSC-HVDC applications, cascaded control requires the speed of response to increase towards the inner loop. Hence, the internal loop is designed to achieve fast response. On the other hand, the main goal of the outer loops is steady-state regulation.

From Figure 6.2, the SM capacitor voltage control function is the outmost loop control, followed by the arm voltage control and arm current control loops. This is due to the direct inclusion of the output of the arm voltage control's 'PI V' into the arm current control and because the total arm voltage must be regulated to its reference independently of the individual SM voltages. Thus this establishes the order for control speed.

In order to specify the parameters of the different PI controllers, the open loop transfer functions (TFs) of each control scheme must be determined. The TFs can be derived directly from the control diagram in Figure 6.2, where the Laplace transformed equivalent of the physical systems are considered and the converter is represented as a delay, as in (5.3). Neglecting the non-linearities and the disturbances, the open-loop TFs of the SM capacitor voltage control ($G_{OL\,SM}$), arm voltage control ($G_{OL\,AV}$) and arm current control ($G_{OL\,AC}$) of the reduced-order MMC arm control strategy are:

$$G_{OL\,SM}(s) = K_{pC}\left(\frac{1+sT_{iC}}{sT_{iC}}\right)\left(\frac{1}{1+sT_{eq}}\right) \tag{6.4}$$

$$G_{OL\,AV}(s) = K_{pV}\left(\frac{1+sT_{iV}}{sT_{iV}}\right)\left(\frac{1}{1+sT_{eq}}\right)\left(\frac{1}{sL_{arm}C}\right) \tag{6.5}$$

$$G_{OL\,AC}(s) = K_{pI}\left(\frac{1+sT_{iI}}{sT_{iI}}\right)\left(\frac{1}{1+sT_{eq}}\right)\left(\frac{1}{sL_{arm}}\right) \tag{6.6}$$

where $\{K_{pC}, K_{pV}, K_{pI}\}$ and $\{T_{iC}, T_{iV}, T_{iI}\}$ are the proportional and integral gains, respectively, of the PI controllers. C is the capacitance value in each SM, L_{arm} is the value of the arm inductance and $T_{eq} = 1/2f_{sw}$ is the average time delay corresponding to

one switching cycle. Since the arm current control is the innermost control loop, special attention is paid to the tuning of 'PI I'.

It can be observed that the open-loop transfer function of the arm current control in (6.6) has one of the poles is at the origin. The "symmetrical optimum" design criterion is employed here, which obtains a controller that forces the frequency response of the system as close as possible to that for low frequencies. The method has the advantage of maximizing the phase margin [308] for a given frequency, which means the system can tolerate more delays, typically found in practical experimental systems. This method optimizes the control system behaviour with respect to disturbance input [309, 310].

The tuning criteria according to the symmetrical optimum method is obtained using the Nyquist criteria [311] of stability:

$$\begin{cases} |G_{OL\,AC}(j\omega)| = 1 \\ \angle G_{OL\,AC}(j\omega) = -180^\circ + \Phi_m \end{cases} \tag{6.7}$$

where Φ_m is the phase margin. Differentiation of the angle criteria with respect to ω gives the condition for maximum phase margin:

$$\omega_d = \frac{1}{\sqrt{T_{i\,I} T_{eq}}} \tag{6.8}$$

This condition gives the tuning criteria for time constant of the controller as:

$$T_{i\,I} = T_{eq} \left(\frac{1 + \sin \Phi_m}{1 - \sin \Phi_m} \right) \tag{6.9}$$

The resulting open loop frequency characteristic will have a maximum phase Φ_M at the crossover frequency of ω_d, symmetric about $\frac{1}{T_{i\,I}}$ and $\frac{1}{T_{eq}}$. Then, by symmetric property, one can also write:

$$T_{i\,I} = a^2 T_{eq} \tag{6.10}$$

where a is the symmetrical distance between $\frac{1}{T_i}$ and $\frac{1}{T_{eq}}$ to ω_d. From the magnitude condition, the tuning for gain of the controller can be found as follows:

$$K_{pI} = \frac{L}{aT_{eq}} \tag{6.11}$$

Using the PI controller parameters, the open-loop transfer function of the arm current control loop becomes:

$$G_{OL\,AC}(s) = \frac{1}{s^2 a^3 T_{eq}^2}\left(\frac{1 + sa^2 T_{eq}}{1 + sT_{eq}}\right) \tag{6.12}$$

A higher value of a, typically constrained between 4 and 16 in the literature [312], increases the phase margin and improves the damping, although slowing the system response. Hence the choice of the controller parameters from a design point of view is a compromise between these performances. Using the bandwidth separation principle, the gains of the controllers in the SM capacitor voltage control and arm voltage control can be defined as:

$$\begin{cases} K_{pV} = \frac{K_{pI}}{5}, & T_{iV} = \frac{T_{iI}}{5} \\ K_{pC} = \frac{K_{pI}}{10}, & T_{iV} = \frac{T_{iI}}{10} \end{cases} \tag{6.13}$$

Defining $a = 10$ and using the system parameters of Table 4.2 the controllers are tuned with the parameters presented in Table 6.1. The parameters of 'PI T' in the SM temperature control loop are the same as determined by (5.5).

The continuous-time controllers in the different TFs are replaced by corresponding discrete-time controllers in the FPGA. Although several methods such as Euler's and Tustin's methods are frequently used [313], this transformation is performed automatically by LabVIEW in the FPGA control board through a 'design-by-emulation' process [314]. The LabVIEW design process ensures the performance of the resulting discrete-time controllers matches the 'ideal' controller design in continuous-time, and that the resulting closed-loop system is also stable. As a result, and also due to the presence of higher order modes in the experimental system that have not being modelled in the ideal TFs, the PI controller gains have to be adjusted and are also presented in Table 6.1.

TABLE 6.1: Reduced-order MMC arm controllers parameters

Controller	Parameter	Analytical Value	Experimental Value
PI T	K_{pT}	20	0.5
	T_{iT}	0.01	0.01
PI C	K_{pC}	0.165	0.62
	T_{iC}	0.002	0.12
PI V	K_{pV}	0.33	0.84
	T_{iV}	0.004	0.1
PI I	K_{pI}	1.65	5
	T_{iI}	0.02	0.012

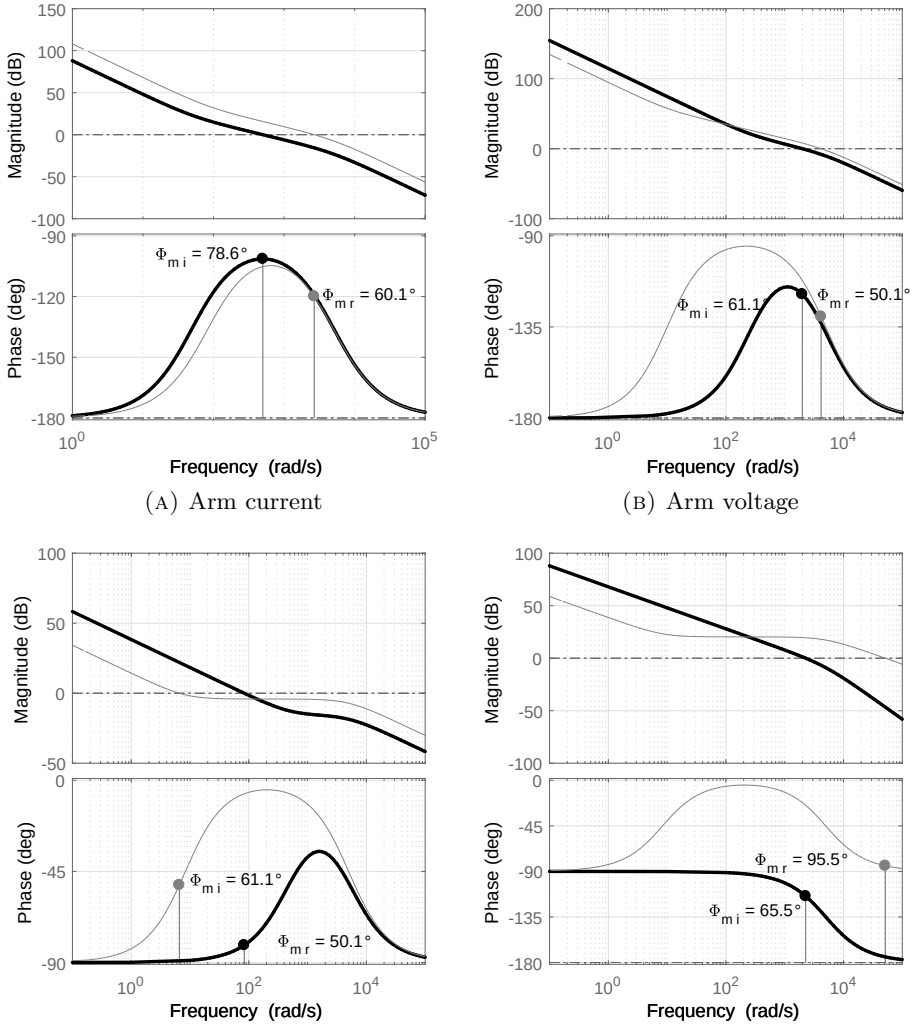
The Bode diagrams of the open-loop transfer functions of the different controllers are shown in Figure 6.3, when the analytical values (solid black curve) and experimental values (grey dashed curve) parameters are used in the PI controllers. For 'PI I', using the experimental parameters leads to a decrease in the phase margin from the ideal case $\Phi_{mi} = 78.6\,^\circ$ at $\omega_d = \frac{1}{\sqrt{0.02\times0.0002}} = 500\,\text{rad/s}$ to $\Phi_{mr} = 60.1\,^\circ$ at $\omega_c = 2674\,\text{rad/s}$. A similar behaviour is also observed for the arm voltage ('PI V') and SM temperature control ('PI T') in Figure 6.3 (b) and (d), respectively, where the reduction on the phase margin is accompanied by a shift in the crossover frequency to higher values.

The opposite behaviour can, however, be verified for the SM capacitor voltage control ('PI C'), where the utilisation of the experimental set of parameters results in an increase in the phase margin from $\Phi_{mi} = 50.1\,^\circ$ to $\Phi_{mr} = 61.1\,^\circ$, but also in a reduction in the crossover frequency from $\omega_c = 83.6\,\text{rad/s}$ to $\omega_c = 6.59\,\text{rad/s}$. Nonetheless, the closed-loop systems are stable and with a generous phase margin. Since the phase margin bode diagrams never cross $-180\,^\circ$, the gain margin will be infinite, which implies that the systems are inherently stable.

6.3 Experimental Platform

6.3.1 Overall System Structure

An experimental MMC arm test bench with three SMs shown in Figure 6.4 has been established to validate the proposed reduced-order MMC Setup operation and control, as well as the active thermal control and SM thermal regulation and balancing strategies discussed in Chapter 4 and Chapter 5, respectively.



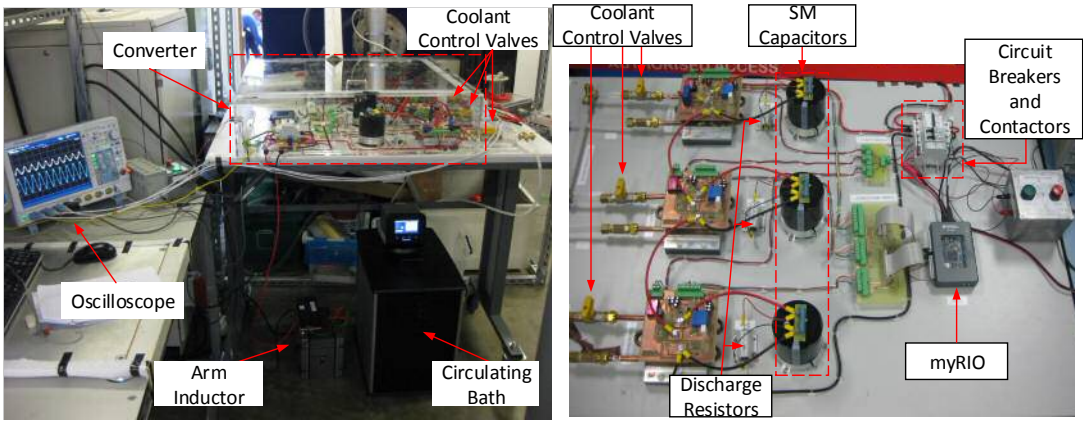
(A) Arm current (B) Arm voltage

(C) SM capacitor voltage (D) SM temperature

FIGURE 6.3: Open-loop transfer functions Bode diagrams for different controllers in the reduced-order MMC arm control strategy. Solid black and dashed grey curves represent the system with the ideal analytical and experimental PI controller's parameters, respectively.

The overall structure of the experimental platform is shown in Figure 6.5. A Triphase Power Module PM15F120 [315], controlled via MATLAB®/Simulink®, is utilised as a controllable voltage source to generate the supply voltage V_{supply}, providing the electrical interface for the MMC arm. The Wiring Diagram of the MMC setup can be consulted in Appendix A.

The control of the MMC arm is implemented in a National Instruments (NI) myRIO-1900 control board based on a dual-core ARM® Cortex™-A9 real-time processor and a Xilinx Zynq®-7010 FPGA with a 40 MHz Onboard clock. The model encompasses the complete control of the experimental MMC Arm, namely:



(A) Global setup (B) Detail of electrical system

FIGURE 6.4: Experimental MMC arm setup.

- Acquisition and scaling of capacitor voltages, arm current and semiconductors case temperature measurements;
- Implementation of the proposed control strategy shown in Figure 6.2;
- Generation of PWM outputs and driver Enable signals for each SM;
- Data logging and safety control, including shut-down due to abnormal conditions such as overvoltage, overcurrent or overtemperature.

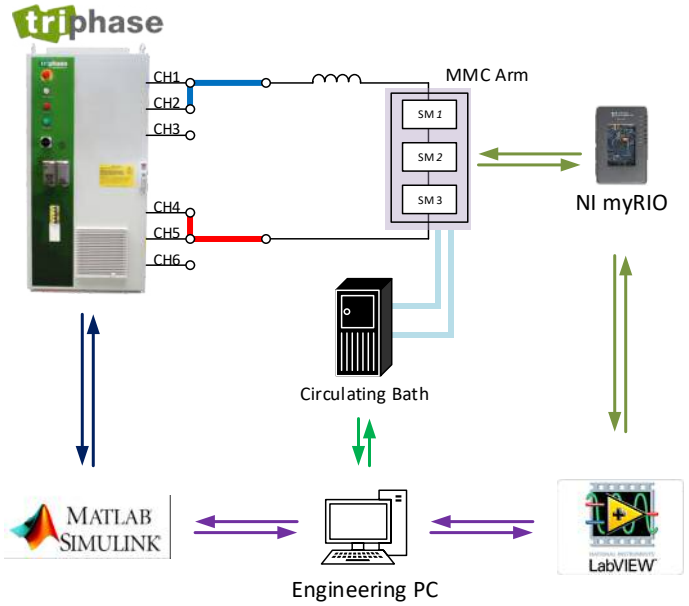


FIGURE 6.5: Overall connection and communication structure for the control of the experimental MMC arm setup.

The control strategy is implemented in the LabVIEW FPGA environment [316] and compiled to C code and VHDL (VHSIC (Very High Speed Integrated Circuits) Hardware Description Language) in order to be executed by the processor and the FPGA, respectively. A simple Graphical User Interface, shown in Figure 6.6, is also implemented in LabVIEW and runs on the Engineering PC, communicating with the control model in the myRIO.

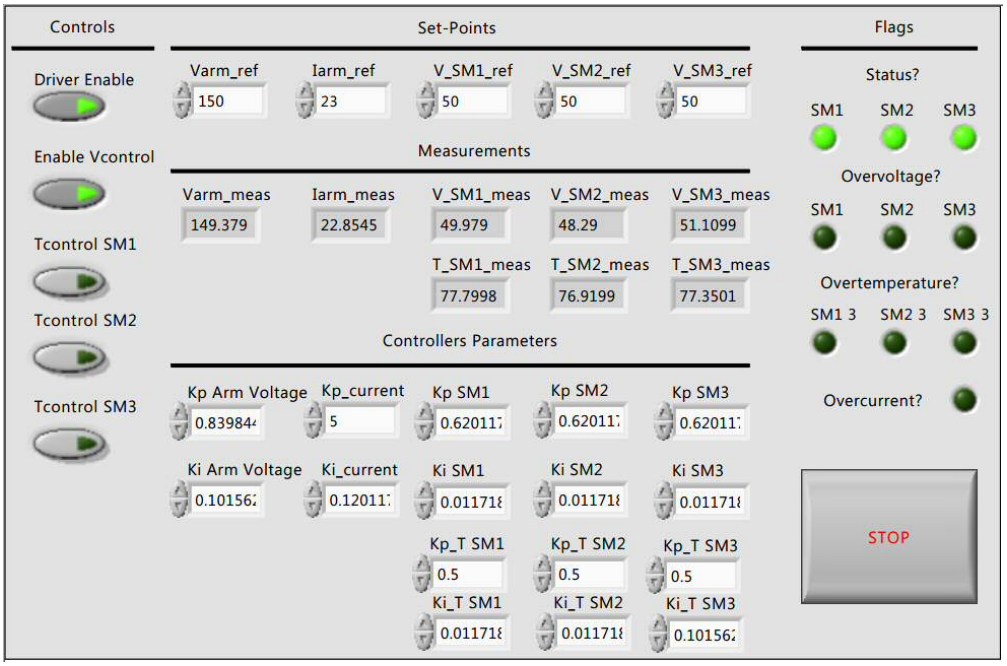


FIGURE 6.6: LabVIEW Graphical User Interface.

The coordination of tasks between the processor and the FPGA is shown in Figure 6.7. The fast electrical variables control functions are implemented in the FPGA, while the slower temperature calculation function, data logging and set-points are defined in the processor. These functions are implemented in several parallel loops running at different time steps in order to eliminate jitter, enabling the execution of high-speed deterministic code in a compact board like the myRIO.

The different controllers in the arm should be fast enough to track their references at any time, with minimum errors. For the inner-most (and faster) arm current controller, in particular, a significant error may exist between the desired current value and its actual value due to a limited sampling frequency.

The largest current error will occur when the current changes at its fastest rate. Neglecting the circulating component, the fastest rising speed of the current reference is when its rising magnitude crosses the 'DC' value [305]. At that instant, the slope equals

ωi_{ac}^{pk}, where ω is the grid frequency and i_{ac}^{pk} is the peak amplitude of the fundamental frequency 'ac' component of the arm current. Considering a sampling period t_s, the maximum current change Δi_{max} can be determined as:

$$\frac{\Delta i_{max}}{t_s} = \frac{V_{supply}}{L_{arm}} + \omega i_{ac}^{pk} \tag{6.14}$$

For a given maximum acceptable tracking error Δi_{max}, the minimum sampling time $t_{s\,min}$ can be calculated by:

$$t_{s\,min} = \frac{\Delta i_{max}}{\frac{V_{supply}}{L_{arm}} + \omega i_{ac}^{pk}} \tag{6.15}$$

Using the system parameters from Table 4.2, the arm current waveform from Figure 4.15 (b) and considering a maximum error of $\pm 10\,\%$, the minimum sampling time for the FPGA main loop is:

$$t_{s\,min} = \frac{0.1 \times 23}{\frac{150}{0.0033} + 2 \times 50 \times \pi \times 23} = 44\,\mu\text{s} \tag{6.16}$$

Which corresponds to a sampling frequency of 21.7 kHz. The internal clock of the FPGA operates at 40 MHz and can be derived for a desired frequency using an integer multiple of the base value. A frequency of 40 kHz corresponds to a sampling time of 25 μs,

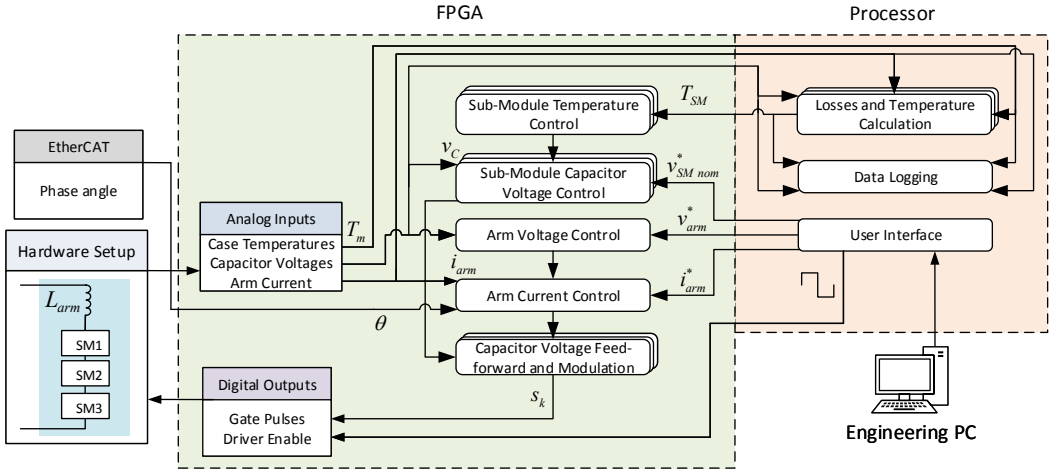


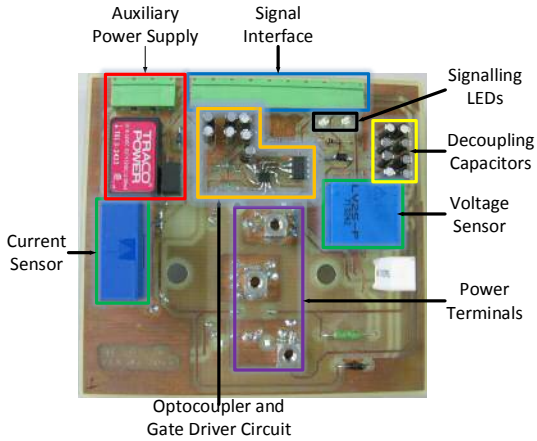
FIGURE 6.7: Task coordination between the processor and the FPGA in the myRIO board.

smaller than 44 μs, and therefore sufficient to ensure the arm current (fastest control loop) remains regulated within a maximum difference of $\pm 10\,\%$ of its reference value.

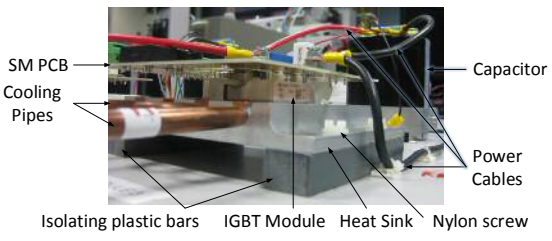
6.3.2 Sub-Module Structure

The configuration of each SM in the MMC arm is shown in Figure 6.8. Each SM is an independent block and has a dedicated printed circuit board (PCB) with a PWM and Driver Enable signal inputs. The outputs consist of the capacitor voltage, arm current and semiconductor module case temperature measurements, each of these from independent and dedicated circuits, as illustrated in Figure 6.8 (a). The semiconductors are Infineon's EasyDUAL 2 1200V dual HB IGBT module FF75R12YT3 [9] and are placed under the PCB, as shown in Figure 6.8 (b). Each SM also has an external discharge ('bleeding') resistor, not included in Figure 6.8 but presented in Figure 6.4 (b).

The baseplate of the IGBT module is in contact with a liquid cooled heat sink, via a thermal grease layer, where each SM has an individual control valve, used to regulate the coolant flow from a temperature-controlled circulating bath. The heat sink is thermally insulated from the assembly table through polyethylene bars using nylon screws, in order to ensure that the heat generated from the semiconductor losses will mainly flow through conduction from the silicon dies to the coolant. In this setup only water is used for semiconductors cooling, provided by a PolyScience PP15R-40-A12E Refrigerated Circulating Bath, which is remotely controlled by the Engineering PC.



(A) PCB layout

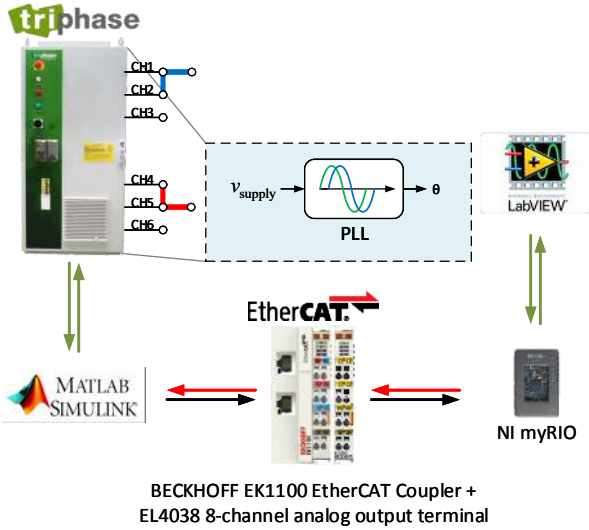


(B) Physical assembly

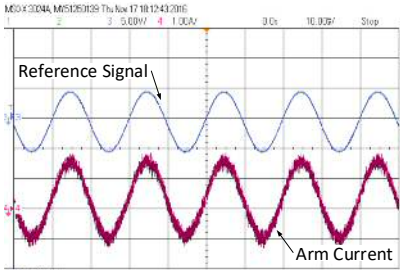
FIGURE 6.8: Experimental SM configuration.

6.3.3 Phase Synchronisation

The high-level VSC control scheme for a full-scale MMC shown in Figure 2.9 produces the reference output voltage waveform V_{ref}, synchronised with the grid voltage via a PLL. In the experimental setup, the arm voltage and the arm current in Figure 6.2 are synchronised with the phase of the supply voltage V_{supply} generated by the Triphase power module via a PLL, as shown in Figure 6.9 (a), where the single-phase PLL proposed in [317] was implemented. The phase information is communicated via a BECKHOFF EL1100 EtherCAT™Coupler and an EL4038 Analog Output terminal with a 12 bit resolution to the myRIO board via an Analog Input. The synchronisation is demonstrated in Figure 6.9 (b) for a test reference voltage signal defined in LabVIEW and sent to the Triphase control, and the arm current in the MMC setup.



(A) Phase angle communication

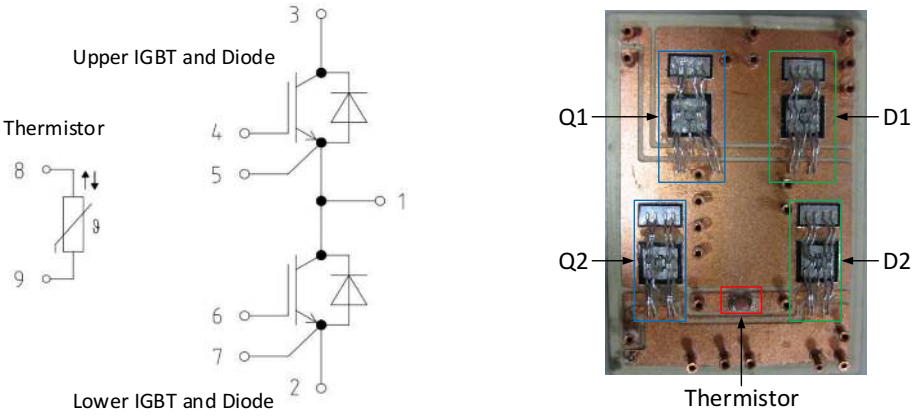


(B) Example of phase synchronisation

FIGURE 6.9: PLL-based synchronisation between MMC arm voltage and current and Triphase output.

6.3.4 Temperature Measurement and Calculation

Direct access to semiconductors junction temperature is not possible without complex methods requiring sensors mounted on the chip or even being part of it, as presented in Subsection 3.3. The chosen IGBT modules include an easily accessible embedded thermistor, also known as NTC [11], placed in a close location to the chips, as illustrated in Figure 6.10.



(A) (B)

FIGURE 6.10: Thermistor placement in Infineon HB IGBT module FF75R12YT3: (a) - Configuration [9] and (b) - Physical module with embedded thermistor.

An estimation of the junction temperatures can therefore be calculated by using the case temperature measurement as a known point to start from, and the thermal resistances of the semiconductor module, as specified in its datasheet [9]. The thermal network inside the semiconductor module is now purely resistive, as presented in Figure 6.11, with the parameters shown in Table 6.2 for the different semiconductor dies.

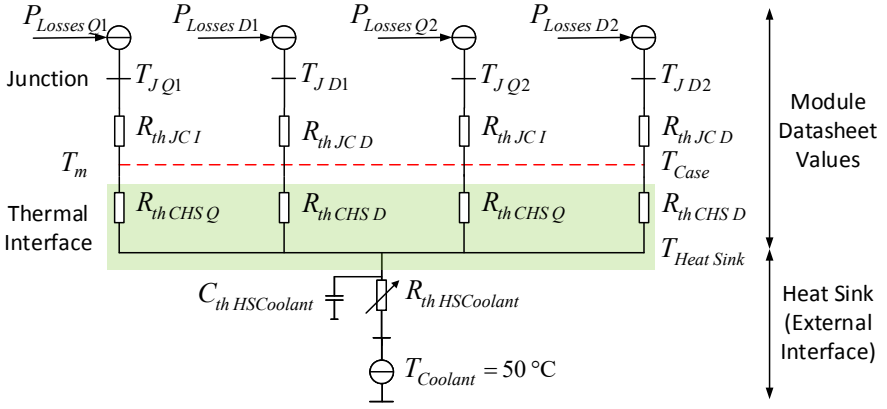


FIGURE 6.11: Thermal network of IGBT module Infineon FF75R12YT3 [9] considered in the experimental tests.

The thermistor mathematical representation is given by:

$$R(T) = R_1 e^{B\left(\frac{1}{T} - \frac{1}{T_1}\right)} \tag{6.17}$$

where $B = 3433\,\mathrm{K}$, $R_1 = 5\,\mathrm{k\Omega}$ is the reference thermistor value at $25\,°\mathrm{C}$ and $T_1 = 298.15\,\mathrm{K}$ is the reference temperature ($25\,°\mathrm{C}$) in degrees Kelvin.

TABLE 6.2: Experimental thermal network parameters for IGBT module Infineon FF75R12YT3 [9]

Parameter	Value	Unit
Thermal Resistance Junction to Case per IGBT ($R_{th\,JC\,Q}$)	0.36	°C/W
Thermal Resistance Case to Heat Sink per IGBT ($R_{th\,CHS\,Q}$)	0.20	°C/W
Thermal Resistance Junction to Case per Diode ($R_{th\,JC\,D}$)	0.60	°C/W
Thermal Resistance Case to Heat Sink per Diode ($R_{th\,CHS\,D}$)	0.25	°C/W
Thermal Resistance Heat Sink to Coolant ($R_{th\,HSCoolant}$)	0.45	°C/W
Thermal Capacitance of Heat Sink ($C_{th\,HSCoolant}$)	167	J/°C

Considering a simple voltage divider, as shown in Figure 6.12, where the supply voltage V_s is provided by the auxiliary power supply shown in Figure 6.8 (a), the thermistor voltage can be determined by:

$$V_T = V_s \frac{R(T)}{R_d + R(T)} \tag{6.18}$$

And its resistance value can be determined by:

$$R(T) = R_d \frac{V_T}{V_s - V_T} \tag{6.19}$$

Substituting (6.17) into (6.19), the case temperature of each SM in degrees Celsius can be can be computed though the following expression, easily implemented in LabVIEW:

$$T = \frac{1}{\frac{\ln\left(\frac{R_d V_T}{R_1 (V_s - V_T)}\right)}{B} + \frac{1}{T_1}} - 273.15 \tag{6.20}$$

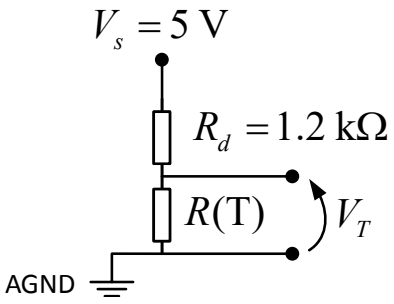


FIGURE 6.12: Thermistor resistance measurement circuit.

The resistor R_d in the voltage divider is selected to have a value of 1.2 kΩ so that a maximum 1 °C tolerance due to self-heating of the thermistor is considered [11]. The measured voltage value V_T will have a value in the range 0−5 V and is connected to one of the Analog Input channels of the FPGA. A digital low-pass filter with a cutoff frequency of 10 Hz is implemented in LabVIEW to remove some of the voltage measurement noise due to the proximity of the thermistor to the switching dies, as presented in Figure 6.10 (b).

The thermal resistances in Figure 6.11 allow the direct calculation of junction temperature under static conditions and the case temperature measurement captures the thermal time constant $\tau = R_{th\,HSCoolant} C_{th\,HSCoolant} \approx 75$ s. The much smaller thermal time constant associated with the die is neglected and as a result the calculation tends to produce transient under- and over-temperature values. This is demonstrated in Figure 6.13 for a peak current reference step from 17 A to 23 A. The temperature over-estimation is, however, a positive feature as it ensures an additional safety margin for the actual junction temperature value.

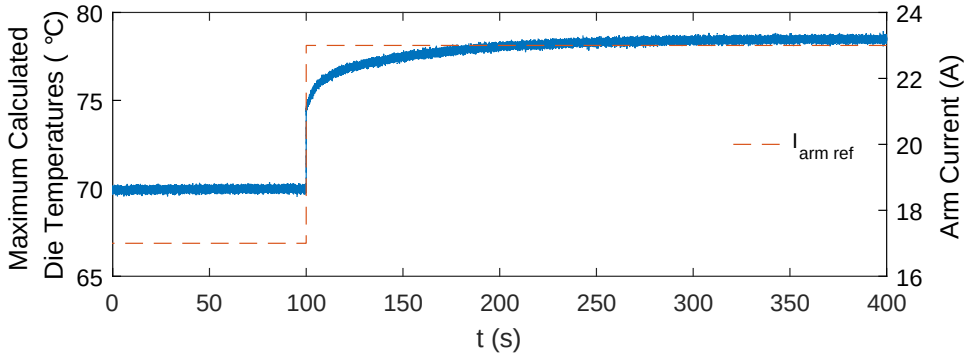


FIGURE 6.13: Maximum calculate die temperatures response to a step in the arm current reference.

6.4 Experimental Results and Discussion

Experimental results are presented initially to validate the dynamic performance of the MMC arm, followed by the results for the active thermal control strategies proposed in Chapter 4 and the SM temperature regulation and balancing algorithm discussed in Chapter 5.

The test cases in Table 4.6 are also considered for the experimental tests and replicated in Table 6.3. With the exception of the integral gain K_I for Case IV, which been adjusted to 0.01 A/°C s, the remaining proportional and integral gains are the same as in the simulation results for all cases. The parameters of the experimental setup are the same as the simulation model and are shown in Table 4.2 and the time constant of the heat sink has been determined to be $\tau_{th} = 75\,\text{s}$. Similarly to the simulation studies in Chapter 4 and Chapter 5, a PS-PWM modulation scheme with interleaved carriers is considered.

TABLE 6.3: Dynamic rating strategies case studies' parameters for experimental tests

Rating Strategy	Case	Parameter	Value	Unit
Strategy A	I	k_p	1.3068	A/°C
	II	k_p	5	A/°C
	III	k_p	100	A/°C
Strategy B	IV	K_P	5	A/°C
		K_I	0.01	A/°Cs

6.4.1 Dynamic Performance

The steady-state electrical quantities of the experimental MMC arm are shown in Figure 6.14. The average value of the three SM capacitor voltages in Figure 6.14 (a) is regulated to the reference $v^*_{SM\,nom} = 50\,\text{V}$ and the voltages remain balanced within a narrow band. This results in an arm voltage waveform with four distinct levels, shown in Figure 6.14 (c).

The peak value of the arm current in Figure 6.14 (b) is regulated to its reference of 23 A and, similarly to the SM capacitor voltages and arm voltage, is in good agreement with the simulation results of the complete MMC in Figure 4.15 (c).

The response of a step in the arm current peak value reference from 23 A to 28 A at $t = 10\,\text{s}$ is shown in Figure 6.15 (a). The current waveform follows the new reference promptly and without overshoot, and without affecting the SM capacitor voltages or the arm voltage control, as presented in Figure 6.15 (b). This result validates the good tuning of the different controllers in the MMC arm control strategy presented in Figure 6.2.

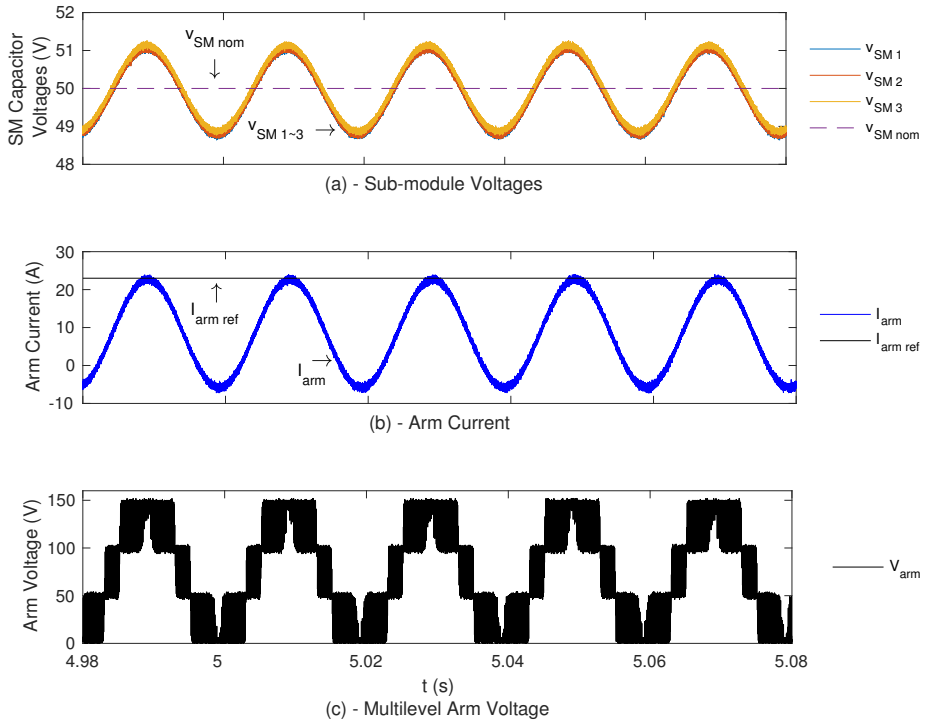


FIGURE 6.14: Experimental MMC arm results.

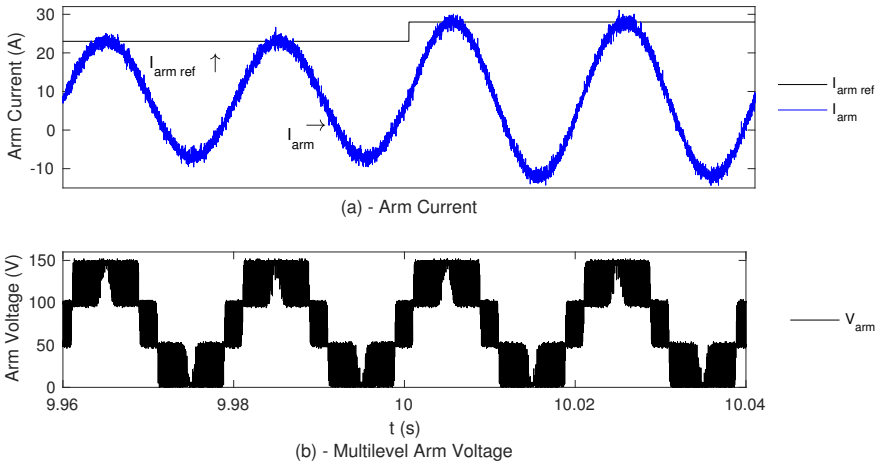


FIGURE 6.15: Experimental response to a step in the arm current reference.

6.4.2 Active Thermal Control

6.4.2.1 Cooling System Failure

The cooling profile presented in Figure 4.16 was programmed into the circulating bath. Although this equipment has internal PID controllers to enable responsiveness to a

desired coolant profile, a delay can be observed when the reference temperature suffers sudden changes, as illustrated in Figure 6.16 (a). Nonetheless, the desired profile is closely followed by the actual coolant temperature.

The results of the temperature regulation by the proposed rating strategies as a result of a cooling failure are shown in Figure 6.16 for a peak arm current $I_{ref} = 20\,\text{A}$. It can be observed in Figure 6.16 (b) that without current limit modulation the maximum calculated die temperature exceeds the upper limit $T_{J(max)} = 95\,^{\circ}\text{C}$ of the thermal headroom.

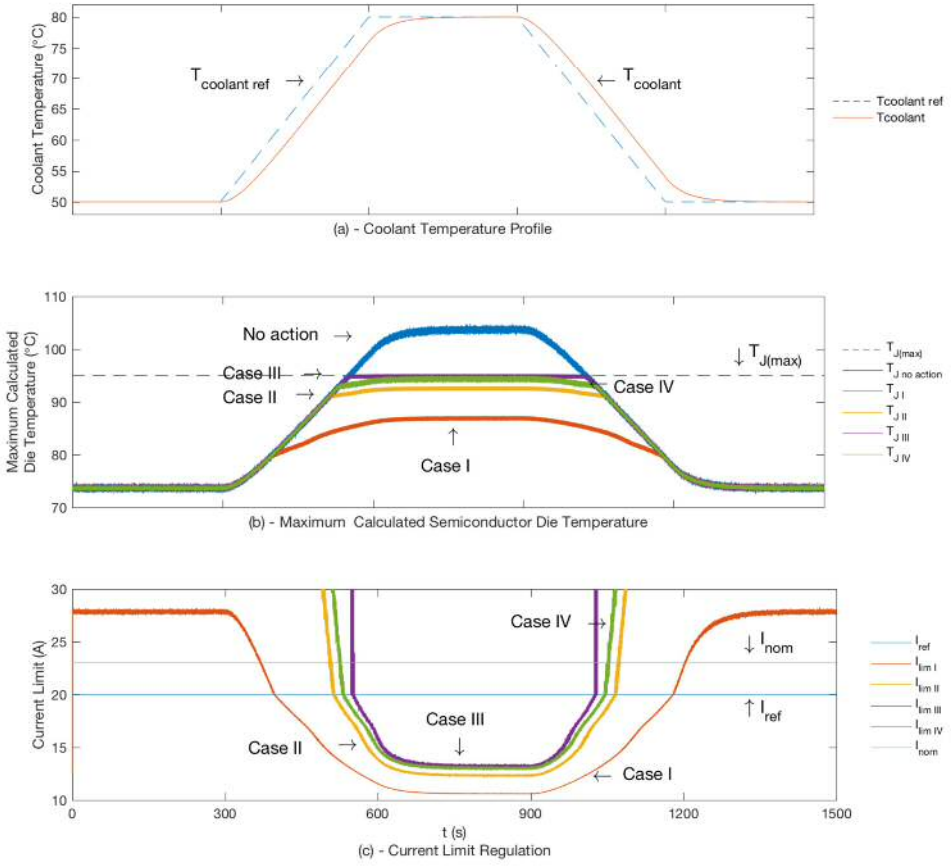


FIGURE 6.16: Experimental temperature regulation during a cooling failure.

When the rating strategies are implemented, the temperature is controlled to be below $T_{J(max)} = 95\,^{\circ}\text{C}$ for any of the cases, as a result of the curtailment of the output current. It can be observed for Strategy A that an increase in the proportional gain from Case I to Case III leads to smaller current curtailments as higher maximum temperatures are permitted. However, large increases do not result in significant reductions in the curtailed current. It can also be observed in Figure 6.16 that Case IV outperforms

Case II as it leads to a slightly smaller current curtailment due to a higher permitted temperature.

Due to the 'lag' effect caused by the temperature regulation by the circulating bath, the higher temperature values are only achieved briefly, at approximately 900 s. This corresponds to the end of the period of highest temperature of the coolant, whose temperature also starts to decrease around this moment. As a result, the current curtailments have a smaller magnitude, compared to the simulation results in Figure 4.17, for the ideal cooling profile. This can verified in Figure 6.17 (a), where for Cases II-IV, there is an approximate reduction of 5 % in the current curtailment magnitude than the corresponding simulation results.

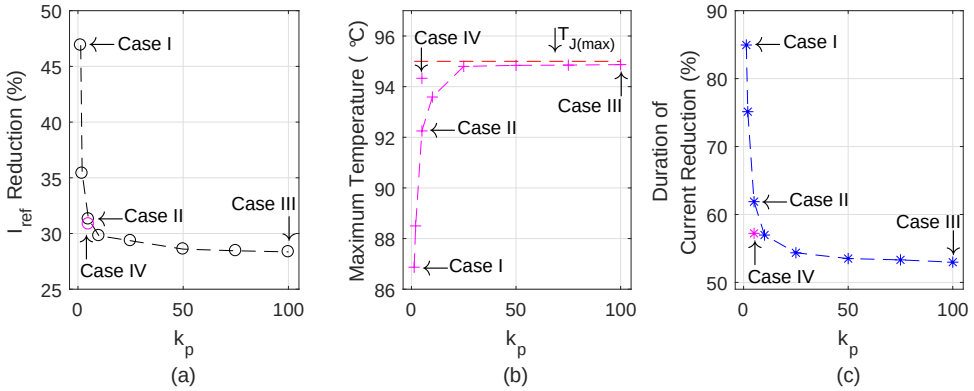


FIGURE 6.17: Experimental results of temperature regulation during a cooling failure as a function of the p roportional gain: (a) - Maximum percent reduction in the reference current; (b) - Maximum calculated semiconductor die temperature and (c) - Percent duration of the current curtailment period with respect to the duration of the cooling profile.

As a result of higher proportional gains from Case I to Case IV, higher permitted temperatures are clearly observable in Figure 6.17 (b), which lead to the smaller current curtailments observed in Figure 6.16 and in Figure 6.17 (a). Although the delay in the coolant temperature regulation allows for smaller current curtailments, the symmetry of the coolant profile leads to similar durations for the curtailment period, which are shown in Figure 6.17 (c). These results are also in good agreement with the corresponding simulation results.

6.4.2.2 Converter Overload

The experimental results of the temperature regulation by the proposed rating strategies during a current overload command are shown in Figure 6.18 for Cases I-IV (first to last

columns, respectively). The instantaneous variation of the calculated temperatures due to the purely resistive thermal network considered for the semiconductor module can be observed in Figure 6.18 (a)-(d); the maximum equilibrium temperatures have similar values to the simulation results presented in Chapter 4 that considered the complete thermal impedance of the individual dies. As a result of the proposed dynamic rating strategies, the new fixed limits for Cases II-IV in Figure 6.18 (e)-(h) are 31.7 A, 34.7 A and 32.6 A, respectively, while the simulation studies yielded 32 A, 37.2 A and 33 A, respectively. As expected, successively higher magnitudes can be reached for higher gains, from Case I to Case IV.

The instantaneous variation of the temperature when the overload command is requested leads to an immediate decrease in the current limit. This results in the reduction of the maximum initial peak value of the current overload magnitude that can flow through the semiconductor dies, which are presented in Figure 6.18 (i)-(l). It can be observed that the current and duration mapping for the different Cases, as well as the initial overload magnitudes, are significantly smaller than the corresponding results from the simulation studies in Figure 4.19. Nonetheless, a key distinction from the simulation results is that the effect of a large time constant of the heat sink is now clearly observable in Figure 6.18 (i)-(h), leading to a significant increase in the overload duration to dozens of seconds. This results in a trade-off in terms of a reduced peak overload magnitude that is compensated by a increase in the overload time constant.

Considering all the possible overload current magnitudes and durations, the experimental TOE is plotted in Figure 6.19. As expected, the TOE for Case I is negligible, comparing with the remaining Cases. Cases II and IV having similar TOEs, with the latter outperforming the former, and with both being dominated by Case III.

Given the maximum output current of 24 A of each phase of the Triphase Power Module [315], the programmable outputs have been connected in parallel, as shown in Figure 6.5. Although this configuration allows the realisation of the high current tests, experiments for peak current overloads higher than 50 A could not be performed for Case III because of the tripping of the breakers in the TriPhase cabinet due to overcurrent protection reasons. This is, therefore, the considered peak initial overload current for this Case, although experimental results seem to indicate higher magnitudes would be permitted.

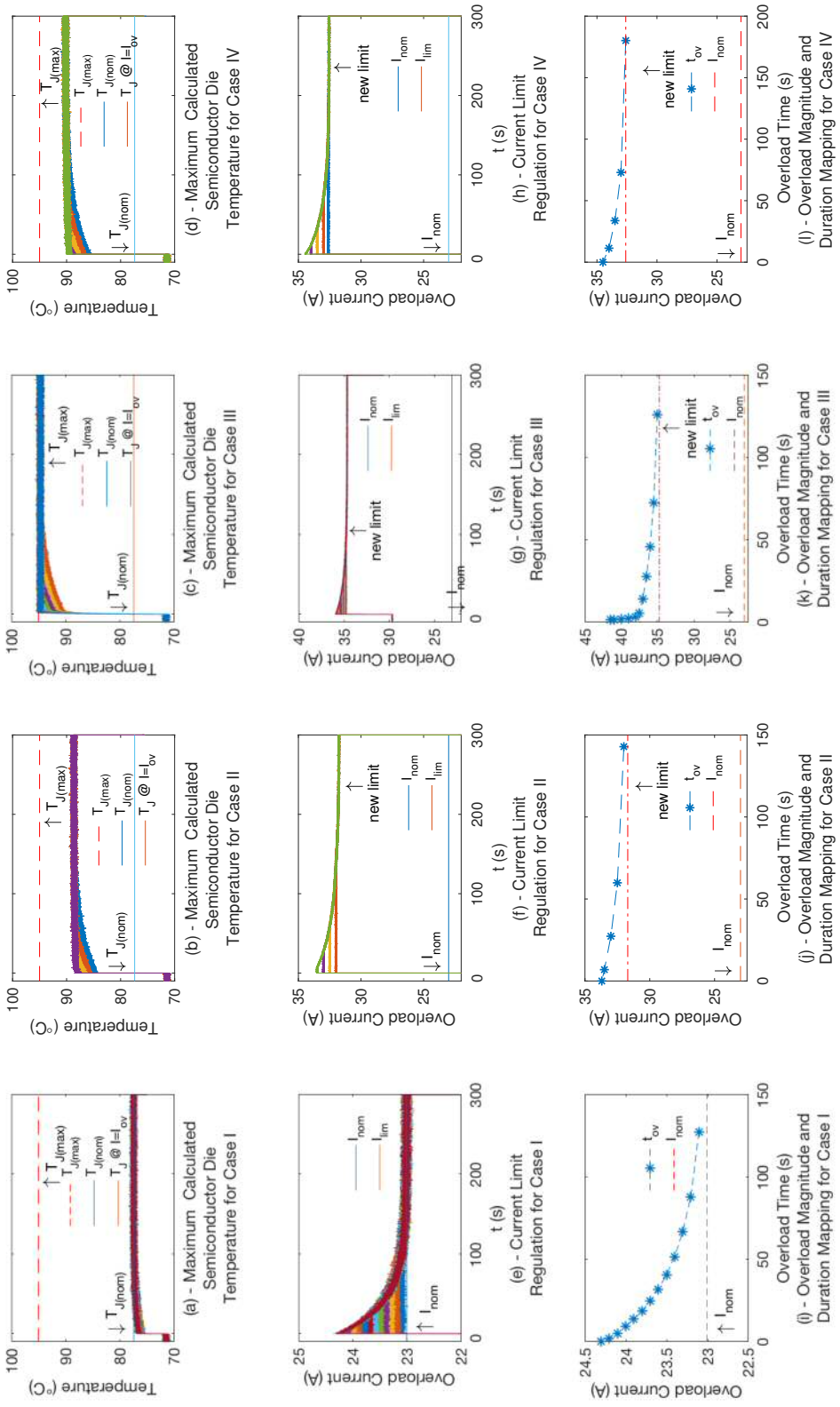


FIGURE 6.18: Experimental results of temperature regulation during a current overload.

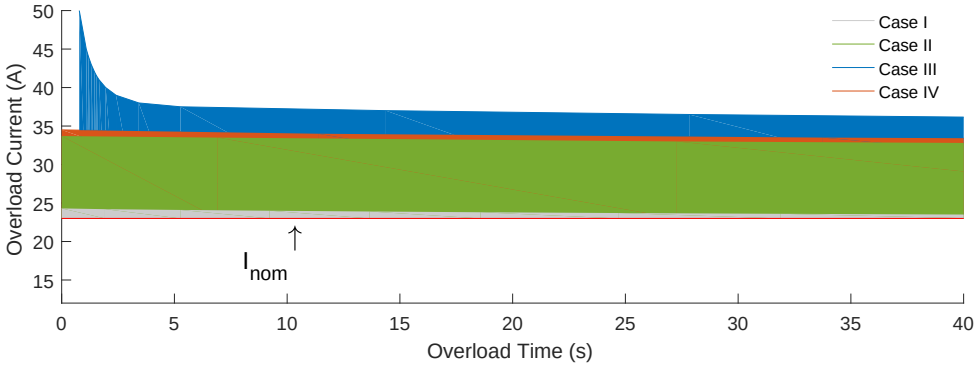


FIGURE 6.19: Semiconductors experimental TOE.

Table 6.4 presents the comparison of simulation and experimental results for the semiconductors TOEn. For the simulation results, the base scenario is considered. With the exception of Case I, all the experimental TOEn values are smaller than the corresponding simulation values. Case I is an exception due to large time constant of the heat sink that compensates the smaller difference between the initial overload magnitudes: 30.8 A in simulation against 24.3 A in the experiment.

TABLE 6.4: Comparison of simulation and experimental results for the semiconductors TOEn (kA^2s).

Case	TOEn		τ_{min} (s)
	Simulation	Experimental	
I	7.04	22.14	24.10
II	104.89	42.59	184.72
III	1779.43	93.75	1423.54
IV	108.88	44.63	182.96

For the remaining Cases, it can be observed that although the heat sink time constant in the experimental setup is much larger than the value considered in the simulation studies, the equivalent TOEns are significantly smaller for Cases II-IV. This is due to the second degree dependency of the TOEn expression on the initial overload current magnitude, which is significantly smaller for the experimental tests.

If the overload capability is included at the converter design stage, the simulation results for the TOEn can be matched by appropriate sizing of the heat sink. Applying (4.20), a minimal value τ_{min} of the heat sinking system can be determined, which is presented in the last column of Table 6.4. For Case I, the minimum value of the heat sink time constant is smaller than the actual value of the physical setup since the experimental

TOEn has a higher value than the corresponding TOEn from simulation. For Cases II-IV, however, the τ_{min} values are, as expected, significantly higher than the actual value of the experimental setup. These values can be achieved by the utilisation of larger heat sinks with higher masses and volumes which, if physically attainable, would lead to similar values of the TOEn.

6.4.2.3 Improvement of Frequency Support

This experimental work aims to validate the application of the semiconductors' transient overload capability enabled by the proposed dynamic rating strategies on the improvement of the inertial response of a power distressed AC grid. The same parameters as in Table 4.9 are considered for the AC grid, which was implemented in LabVIEW using the Control Design and Simulation Module [318]. Similarly to the simulation studies, only Cases II-IV are considered and a frequency deviation exceeding the lower operational limit of 49.8 Hz is used as the triggering signal for the converter overload.

The load increases are defined separately for each test case, given the different permanent overload capabilities ("$I_{ov\,max}$") enabled by the rating strategies and considering a base of 23 A: 31.7 A (0.378 pu) for Case II, 34.7 A (0.509 pu) for Case III and 32.6 A (0.417 pu) for Case IV. Besides the "Initial Set-point" and "Fixed limit" scenarios, with maximum injections of 18 A and 23 A, respectively, the temporary current overload commands ("$I_{ov\,temp}$") are the following: 33.5 A (0.432 pu) for Case II, 36.5 A (0.516 pu) for Case III and 32.6 A (0.432 pu) for Case IV. The results for these scenarios are shown in Figure 6.20 (g)-(i), confirming that resorting to the nominal fixed limit of the converter results in smaller transient and steady-state frequency deviations than when the initial set-point remains unchanged after the power imbalance, as shown in Figure 6.20 (a)-(c). Nonetheless, both scenarios are unable to sustain the steady-state frequency above the lower statutory or operational limits, for all cases.

Although the correction of the power imbalance is a function of the Secondary Frequency Response, the utilisation of the permanent overload current limit $I_{ov\,max}$ can completely correct the power imbalances and restore the frequency to its nominal value of 50 Hz in all the Cases, as shown in Figure 6.20 (g)-(i). This is supported by the longer duration of the power support introduced by the large time constant of the hear sink. Essentially, a large time constant postpones the need to deploy secondary frequency regulation responsive

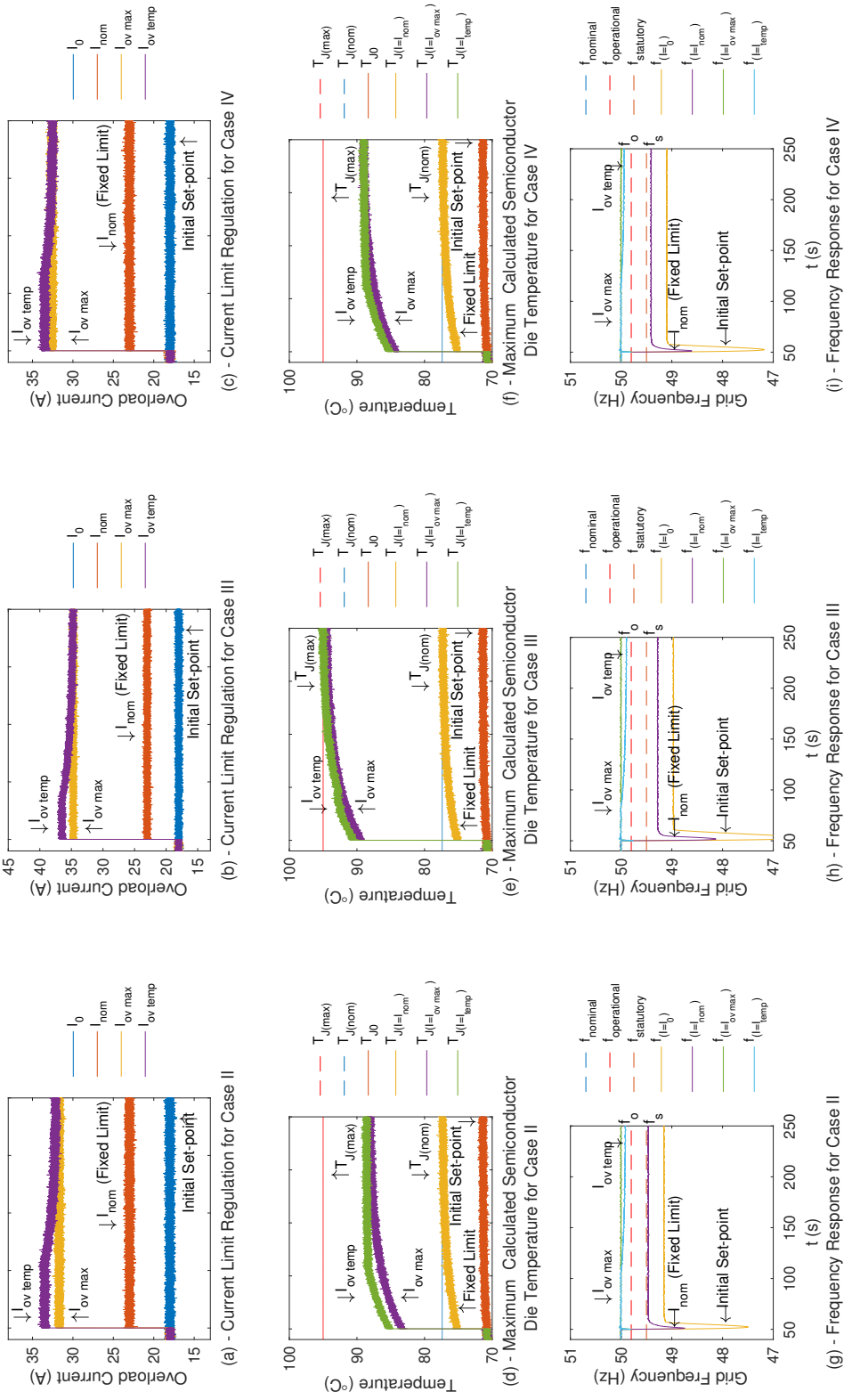


FIGURE 6.20: Experimental frequency regulation during current overload as response to a load increase.

sources connected to the AC grid, confirming the practical application of the simulation studies in Figure 4.25.

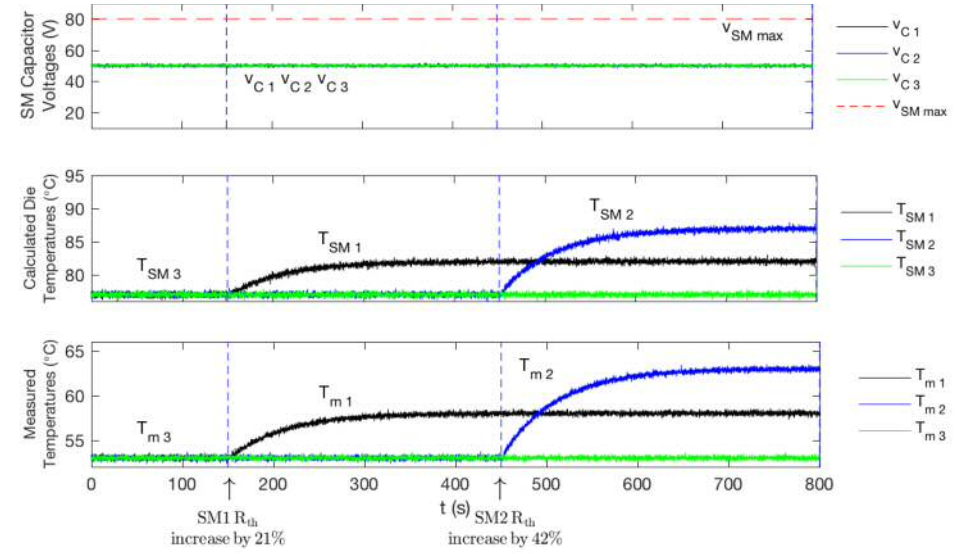
For the extreme scenario of a load imbalance that cannot be corrected by the permanent overload capability of the converter, the overload commands $I_{ov\,temp}$ are requested from the converter. It can be observed in Figure 6.20 (a)-(c) that the converter is initially able to provide the requested current command and completely offset the power imbalance, regulating the frequency to its nominal value, as shown in Figure 6.20 (g)-(i). However, in all cases the temporary nature of the current overload magnitude results is a decay to the new limit $I_{ov\,max}$, leading to a second frequency drop as this current magnitude is unable to counteract the total power imbalance in the AC grid. The permanent overload current is, however, able to sustain the frequency to a value above the lower frequency operational limit of 49.8 Hz.

6.4.3 Sub-Module Temperature Regulation and Balancing

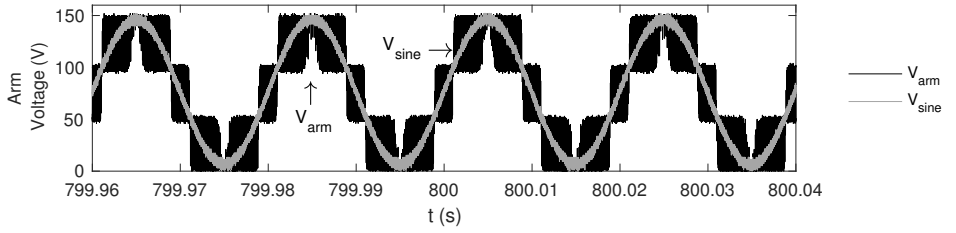
This experimental work aims to validate the effectiveness of the SM temperature regulation and balancing strategy proposed in Chapter 5, through the individual control of SM capacitor voltages. The thermal imbalances are caused by controlled partial cooling failures, applied to two SMs in a two-step procedure, at $t = 150\,\text{s}$ and $t = 450\,\text{s}$. Characterisation tests concluded that for specific valve positions (shown in Figure 6.4 (b)), approximately 1/3 and 2/3 of the fully open position, the desired temperature increases of 5 °C and 10 °C, respectively, are achieved.

6.4.3.1 Thermal Imbalances without Voltage Regulation

The effect of partial cooling failures of the individual temperatures of the SMs without regulation is shown in Figure 6.21 (a), when the proposed temperature regulation and balancing strategy is not enabled. It can be observed that without any SM capacitor voltage control action, all SM voltages are regulated to $v^{*}_{SM\,nom} = 50\,\text{V}$ and the SM (calculated die) temperatures differ significantly as a result of the imbalances. As a result, the arm voltage is regulated to its nominal value of $3 \times 50 = 150\,\text{V}$, as demonstrated in Figure 6.21 (b), where V_{sine} corresponds to the fundamental frequency component of the arm voltage waveform.



(a) - SMs' voltages and temperatures



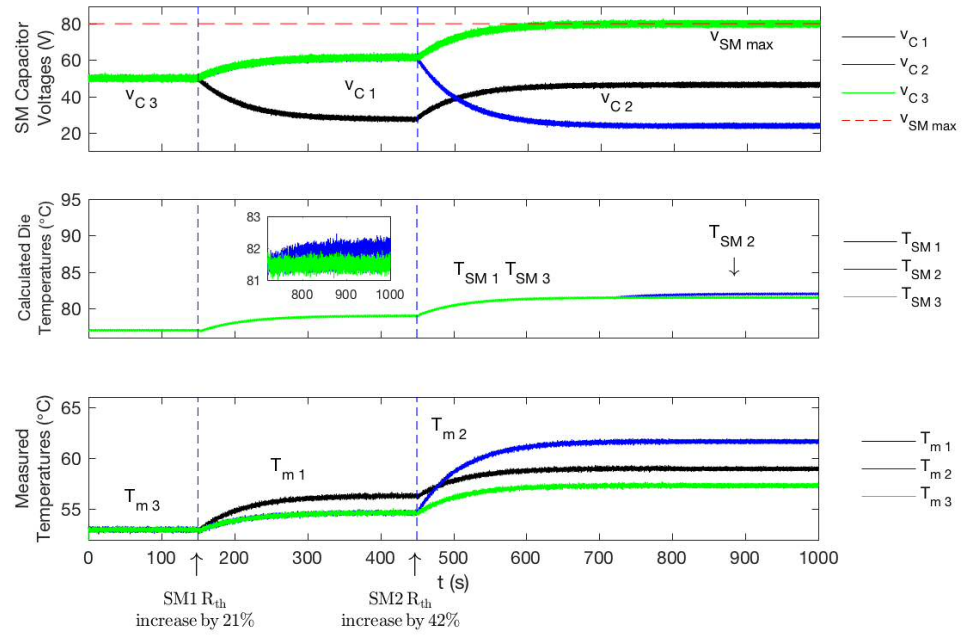
(b) - Multilevel arm voltage

FIGURE 6.21: Experimental response of SMs' voltages and temperatures to thermal imbalances without thermal regulation.

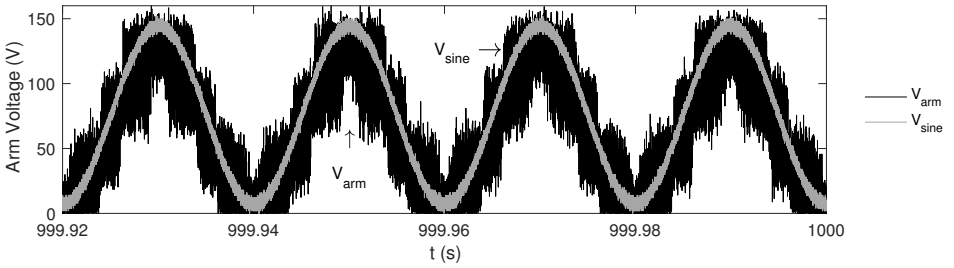
6.4.3.2 Thermal Imbalances with Voltage Regulation

Figure 6.22 (a) presents the results when the proposed balancing control is implemented. When the first thermal imbalance (5 °C) occurs at $t = 150\,\text{s}$ and $T_{SM\,1}$ starts to increase, $v_{C\,1}$ is decreased to 28 V to counteract the imbalance and $v_{C\,2}$ and $v_{C\,3}$ are increased to 61 V in order to achieve a thermal equilibrium while maintaining the arm voltage regulated to its reference value of 150 V.

The thermal imbalance of 10 °C applied to SM2 at $t = 450\,\text{s}$ leads to the reduction of $v_{C\,2}$, while SMs 1 and 3 have their capacitor voltages increased in order to regulate the arm voltage. $v_{C\,1}$, which was previously decreased to 28 V, is increased to 47 V, while $v_{C\,3}$ increases up to the maximum limit of 80 V, reached at approximately $t = 700\,\text{s}$. As a result of this saturation, $v_{C\,2}$ is decreased to 23 V in order to keep the arm voltage regulated at 150 V, leading to a very small (calculated die) temperature



(a) - SMs' voltages and temperatures



(b) - Multilevel arm voltage as a result of unbalanced SM voltages

FIGURE 6.22: Experimental SMs thermal regulation as a response to thermal imbalances.

difference between SM 2 and SMs 1 and 3, which reached a thermal equilibrium at approximately 82 °C.

From $t \approx 800\,\text{s}$ onwards, it can be observed that the converter can operate permanently with a total thermal imbalance of 15 °C. Both voltage and temperature values are in a very good agreement with the simulation results in Figure 5.6. It can also be seen that despite the distortion caused by the uneven voltage steps, the fundamental frequency component of the multilevel voltage waveform in Figure 6.22 (b) remains unchanged compared to the scenario in Figure 6.21 (b) where all SM voltages are regulated to $v^*_{SM\,nom} = 50\,\text{V}$.

6.5 Summary

This chapter presented both the concept of a reduced-order MMC arm setup to validate and replicate a full-scale MMC operation through appropriate control loops, and the development of a corresponding experimental test rig. The reduced-order MMC arm setup aims to overcome the need for the construction of a 3-phase MMC, while being able to replicate the electrical and thermal conditions observed by the semiconductor switches in a complete converter configuration. This is possible by the implementation of dedicated control loops for the key functions of a MMC arm: SM capacitor voltage control, arm voltage control and arm current control. Experimental results were in good agreement with the simulation studies.

Experiments have been performed to validate the performance of the proposed dynamic rating strategies in Chapter 4 and the SMs temperature regulation and balancing algorithm analysed in Chapter 5. Results from experimental tests confirmed the capability of the dynamic rating strategies in enabling the converter to operate in an overload mode without exceeding a given thermal headroom. The current overload capability was exploited to enhance the frequency support of a power distressed AC grid and it was shown that the grid frequency can safely be regulated within the statutory and operational limits when the dynamic rating strategies are enabled, following large power imbalances.

The effectiveness of the SM temperature regulation and balancing strategy through the individual control of capacitor voltages has also been experimentally validated, on a MMC arm with 3 SMs. Results show that significant temperature unbalances between SMs can be successfully distributed among the SM of an arm in order to equalise their maximum calculated die temperatures. As a result of the proposed method, a distorted multilevel arm voltage waveform is produced from unbalanced capacitor voltages, although its fundamental frequency component remains unchanged. Results from both simulations and experimental tests have shown a strong correlation.

The proposed control strategies require an estimation of semiconductors temperature and a simple method was used in this work, making use of a case temperature measurement provided by an embedded thermistor. The use of a purely resistive thermal

network for the calculation of the dies' temperatures leads to a limitation in the maximum possible overload currents, which are partially compensated by the large time constant of the heat sink. This provides some dynamics in the temperature variation but does not limit excessively the benefits of employing dynamic rating strategies to provide an enhanced operation of the converter. Furthermore, it presents no impact on the effectiveness of the SM temperature regulation and balancing strategy.

Due to the high proportional gain required by the proportional-type strategy (Strategy A) to fully exploit the thermal headroom, it was expected some noise amplification in the measured thermistor voltage. This was especially important for Case III given the high value of the gain multiplied by the temperature resulting from applying (6.20). In practice, results in Figure 6.16 and Figure 6.18 show that the 10 Hz cutoff bandwidth of the digital low-pass filter implemented in the FPGA is sufficient to eliminate most of the noise in the thermistor voltage measurement due to its close proximity to the switching dies, as presented in Figure 6.10.

Chapter 7

Conclusions and Recommendations for Future Research

7.1 Conclusions

7.1.1 Operation of Modular Multilevel Converters with Dynamic Rating Strategies

This thesis proposes an additional control loop to extend the power transmission capability of an MMC by employing two different dynamic rating strategies. In these strategies the current limit is dynamically set in response to temperature measurements of the power semiconductor devices. The proposed control scheme exploits the available semiconductor thermal headroom to enable higher output power for short periods. Eigenvalue analysis is performed to determine appropriate ranges for the parameters in the dynamic rating strategies.

The concept of TOE is proposed to characterise the temporary overloading capability of the semiconductors by mapping all the possible overload current durations and magnitudes. Based of this concept, a figure of merit named TOEn is also proposed as a means to evaluate and benchmark different parametrisations of the dynamic rating strategies and alternative heat sinking design solutions.

Simulation results were presented and compared for an AC Grid-tied MMC with 3 SMs per arm, where the benefits of the dynamic rating strategies were analysed for two critical operation scenarios: Cooling System Failure and Current Overload. The use of high proportional gains, for both strategies, leads to the minimisation of the current curtailment during a coolant failure, enabling the converter to keep operating in a derated mode. Furthermore, the converter is also able to operate for a long term in an overload mode, without exceeding the upper limit of the considered thermal headroom. By employing successively higher proportional gains, significant overload magnitudes can be reached, compared to the nominal current limit. The current overload capability was exploited to enhance the frequency support of a power distressed AC grid and it was shown that the grid frequency can safely be regulated within the statutory and operational limits when the dynamic rating strategies are enabled, following large power disturbances.

Analytical derivations supported by simulation results have concluded that for a given configuration of a system, the semiconductors' transient overload capability can be meaningfully improved by employing heat sinks with a large mass. This improvement translates into longer durations of the transient power support capability of the converter, further improving the possibility of providing frequency support to a power-distressed grid.

7.1.2 Sub-Module Temperature Regulation and Balancing

To avoid the unnecessary curtailment of the current limit in the converter, as described in Chapter 4, resulting from an abnormal temperature increase in a single SM, a SM temperature regulation and balancing strategy is incorporated in the converter control. In this method, discussed in Chapter 5, temperature control is exerted by controlling the capacitor voltage of each SM in order to equalise the estimated junction temperatures and ensure similar thermal conditions for the semiconductor dies. This is expected to translate into a similar lifetime expectation for all the SMs, leading to an increased converter reliability and more predictable lifetime behaviour when compared to strategies without temperature regulation and balancing.

The capacitor voltage regulation occurs within a given margin to avoid excessive voltage stresses in the semiconductor devices and capacitors, which limits the amplitude of the

thermal imbalances that can be corrected. As a result of the temperature regulation and balancing process, a distorted multilevel arm voltage waveform is produced from unbalanced capacitor voltages for a small number of SMs, although its fundamental frequency component remains unchanged. In agreement with theoretical derivations, the results also show that a higher number of available SMs to participate in the thermal regulation and balancing process has a higher impact in the correction of thermal imbalances than large voltage margins. As the additional voltage and thermal imbalances that need to be accommodated by each SM decrease substantially as the number of SMs increases, the resulting voltage waveform distortion becomes negligible.

7.1.3 Reduced-Order Experimental Modular Multilevel Converter Platform

A reduced-order experimental MMC arm setup was designed and built to attain a simplified, yet sufficient representation of the electrical and thermal operating conditions of the SMs in a full scale MMC. This faithful representation is achieved through dedicated control loops that regulate the key quantities in the MMC: SM capacitor voltages, arm current and arm voltage. Simulation results from the complete MMC model in PLECS and from the experimental platform are compared and show good agreement for the electrical quantities. A discrepancy occurs for the calculated temperatures under fast dynamic conditions due to the thermistor-based case temperature measurement utilised in the setup. As a result, under- or over-estimation of the calculated die temperatures occurs. Under steady-state and other operating conditions with much slower time constants than the ones of electrical variables, there is no observable difference between the calculated temperature values in simulation and in the experimental tests.

Two sets of experiments using different parameters have demonstrated the effectiveness of the dynamic rating strategies in the regulation of the current limit in the converter within a given thermal headroom. This results in a continuous current injection during a cooling system failure and the possibility for the converter to operate in an overload mode. The application of the overload current on the improvement of the frequency support to a power distressed grid has also been validated.

The experimental work also verifies the effectiveness of the SM temperature regulation and balancing strategy in achieving calculated die temperature equalisation under asymmetric thermal imbalances in the SMs. Although the experimental MMC arm consists of only three SMs, which serves as a basic design concept for the validation of the proposed strategies, it can easily be expanded to a larger system by increasing the number of SMs and updating the setup control implemented in LabVIEW.

7.2 Recommendations for Future Research

From the research outcomes of this thesis and building upon the work carried out, further progress on this line of research can be made. Future work might address some of the following research directions.

7.2.1 Improved Semiconductor Temperature Estimation Method

The major disadvantage of the simple thermistor-based junction temperature calculation method utilised in this work is the lack of access to the fast die time constant, which results in under- and over-temperature estimations under rapid dynamic conditions. Although this was not problematic for the SM temperature regulation and balancing, given the large time constant associated with the heat sink and the coolant, it limits the provision of overload current by the converter when the dynamic rating strategies are enabled.

Future work should employ some of the online junction temperature estimation methods identified in Chapter 3 to provide an estimation that reflects the complex thermal system, which includes multiple time constants. The access to some of the junction dynamics is expected to result in the provision of an improved power injection capability, in both duration and magnitude, and in an extended frequency support to a power distressed grid.

7.2.2 Alternative Dynamic Rating Strategies

The two dynamic rating strategies utilised in this work regulate the current limit through a simple proportional-type control law and a PI-based law. These strategies enable the

converter to operate in an overload mode by exploiting a given thermal headroom. However, and as demonstrated in Chapter 4, the performance of the converter is dependent on the appropriate choice of proportional and integral gains, and suitable ranges were determined by an eigenvalue analysis.

A direction for future development of this work could be the consideration of alternative dynamic rating strategies such as a proportional-derivative (PD) control law. The advantage of this new control law would be the provision of the speed at which the current temperature increases towards the $T_{J(max)}$ limit, adding a predictive element to the control. As a result, the settling time of the current limit increase to its limit and the stability of the system may be improved. The use of improved control schemes for the same rating strategies used in this thesis is also expected to translate into a better performance.

7.2.3 Inclusion of Semiconductors Lifetime Estimation in the Voltage Balancing and Load Sharing Algorithms

Excessive junction temperatures cause a reduction in the lifetime of semiconductors [300], leading to a short operating life and low reliability. This is an important feature for semiconductor-intensive applications such as MMCs, were the reliability of the overall converter station and transmission system is directly linked with appropriate maintenance strategies [153].

Future work should quantify and analyse semiconductors lifetime, e.g. through the application of the well-known Coffin-Manson law. Lifetime information can be used to improve the SM temperature regulation and balancing strategy proposed in Chapter 5, which is expected to result in the extension of semiconductors lifetime. Alternatively, lifetime calculation can be included in the classic CVB as a decision variable.

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[318] National Instruments. LabVIEW Control Design and Simulation Module, . URL http://www.ni.com/labview/cd-sim/.

Appendix A

Wiring Diagram of the Experimental Setup

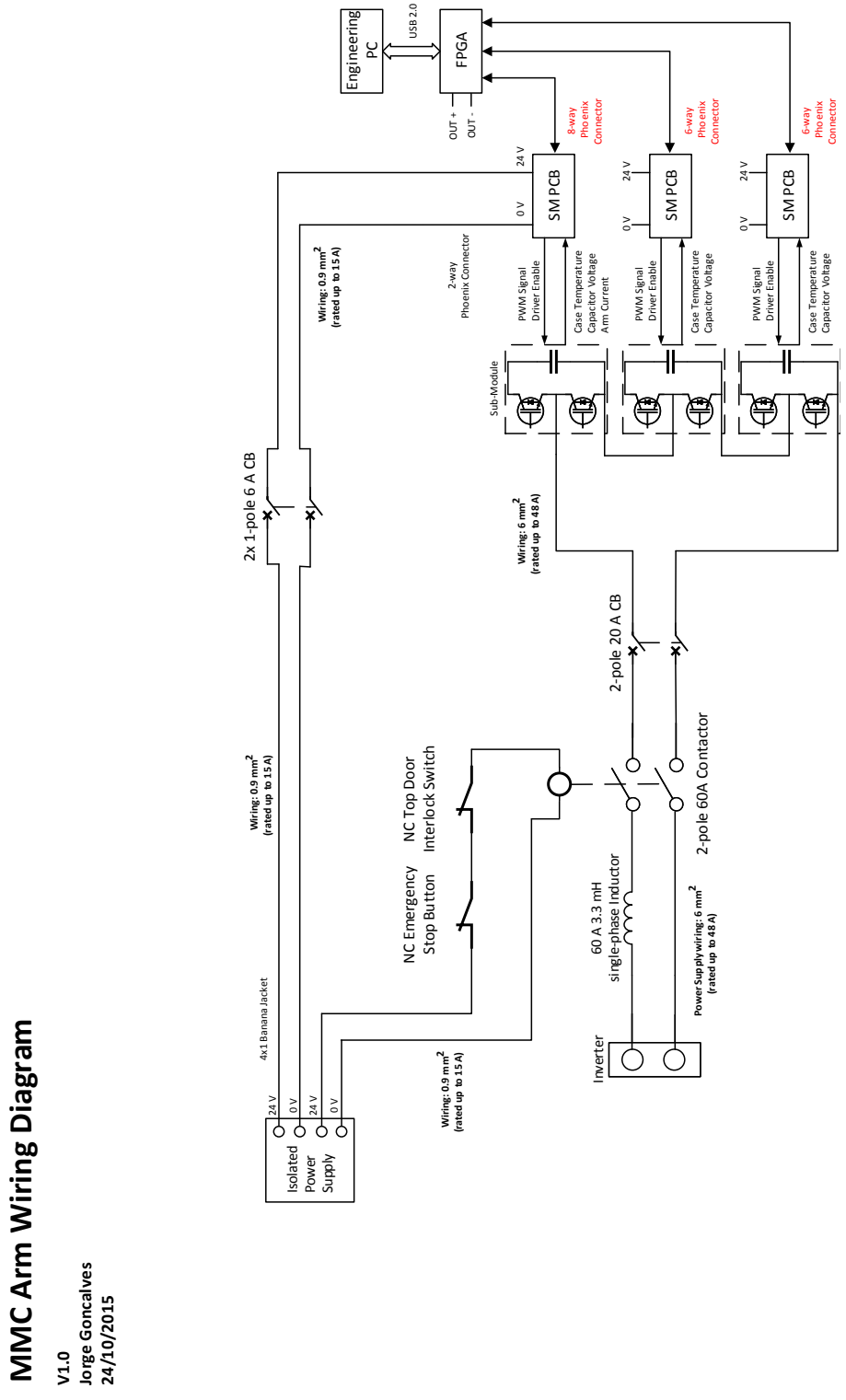

FIGURE A.1: Wiring diagram of the experimental MMC arm setup.

Appendix B

Validation of the Analytical Model of Dynamic Rating Strategies

The comparison between the analytical and simulation models for the dynamic rating strategies presented in sections 4.5.2.1 and 4.5.2.2 is shown in Figure B.1 and Figure B.2, respectively. Subscripts "sim" and "ana" refer to the variables from simulation and analytical model, respectively.

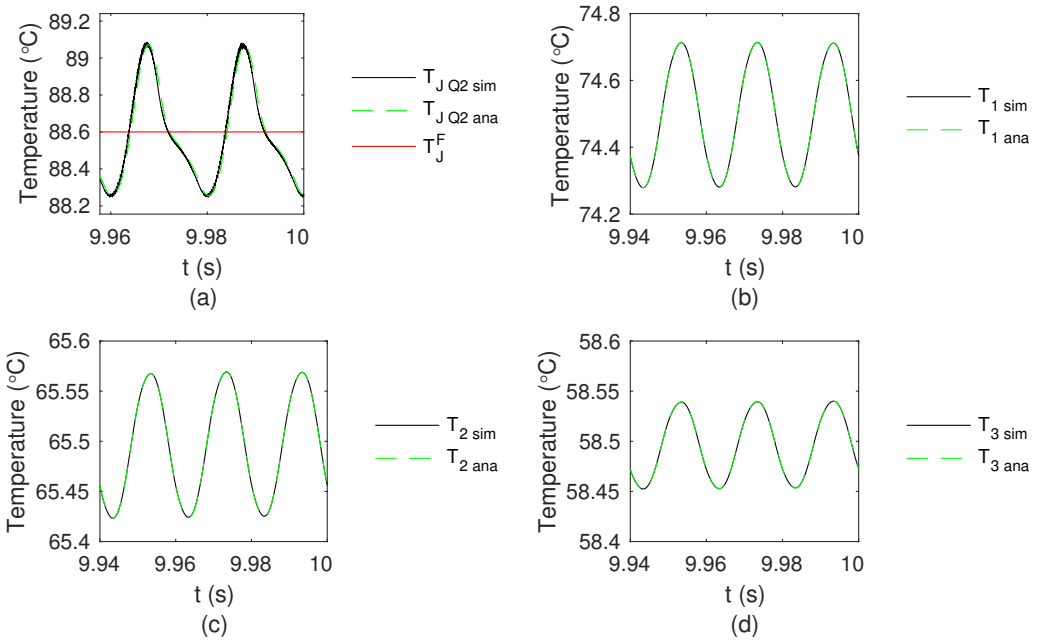

FIGURE B.1: Comparison between simulation and analytical model for dynamic rating strategy A, with $k_p = 5\text{A}/^\circ\text{C}$ and $T_{J(max)} = 95\,^\circ\text{C}$: (a) - T_{JQ2} and T_J^F; (b) - T_1; (c) - T_2 and (d) - T_3.

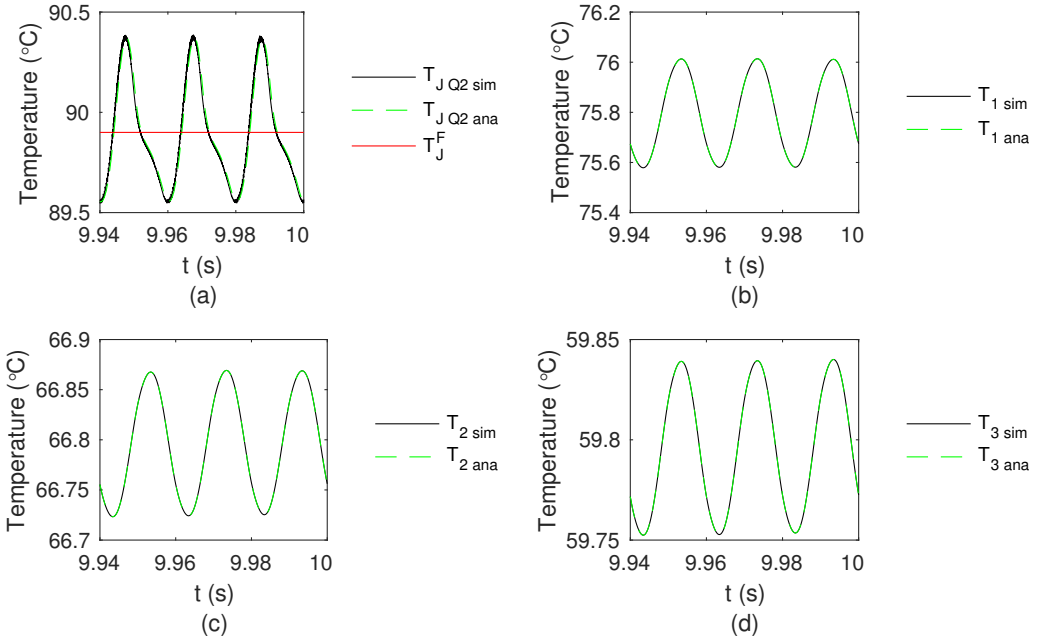

FIGURE B.2: Comparison between simulation and analytical model for dynamic rating strategy B, with $k_p = 5\text{A}/^\circ\text{C}$, $T_{J(max)} = 95\,^\circ\text{C}$ and $K_I = 0.001\,\text{A}/\,(^\circ\text{C}\,\text{s})$: (a) - T_{JQ2} and T_J^F; (b) - T_1; (c) - T_2 and (d) - T_3.