ANALYSIS AND PROTECTION OF HVDC SYSTEMS SUBJECT TO AC AND DC FAULTS

Thesis submitted to

CARDIFF UNIVERSITY

For the degree of

DOCTOR OF PHILOSOPHY

2017

GEN LI

SCHOOL OF ENGINEERING

To my family

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Contents

Acknowledgement

The completion of this research work would have not been possible without the guidance and assistance of many kind people.

First and foremost, I would like to express my sincere gratitude to my brilliant supervisor Prof. Jun Liang for his continuous technical guidance throughout my PhD study. I will also remember the valuable instructions I obtained from him beyond the research. I would also like to thank Dr. Carlos E. Ugalde-Loo for his wise advice and support.

I would like to thank my parents for their encouragement and unconditional support throughout my life.

I would like to thank Dr. Meng Cheng for the happy time in the past years and her kind assistance on revising the writing of my PhD thesis.

I would like to thank Dr. Senthooran and Tibin for their support and assistance in setting-up the experiment in the power electronic lab.

I would like to acknowledge Dr. Ziming Song from Toshiba International (Europe) for his assistance and discussions from the view of industry which made me develop and complete important parts of this thesis.

I would like to thank Dr. Lu Zhang, Avinash Aithal, Prof. Gangui Yan, Guanglu Wu, Dr. Qing Mu and Dr. Fan Ma for their collaborations and joint publications.

Thanks also to the supervisors during my industrial secondments: Dr. Xiaobo Hu and Dr. Yalou Li from China Electric Power Research Institute; Dr. Paul Coventry from National Grid and Dr. Johan Rimez from Elia.

I would also like to thank all my colleagues and friends at Cardiff University for all the motivation and inspiration I got from them. In particular, my special thanks to Dr. Yue Zhou, Qi Qi, Chenghua Zhang, Dr. Marc, Khadijat, Dr. Dantas, Sathsara and Dr. Jorge, with whom I spent most of my time during this journey.

Last but not least, I would like to acknowledge the financial support from the European Commission's Marie Curie ITN (MEDOW) project, which provided me the golden opportunity to explore and develop my career with valuable industry

training and a variety of activities. My thanks also go to other *MEDOWers* for the interesting and useful discussions we shared during this project and also to Cath for her patience dealing with our issues.

Summary

Voltage source converter-based (VSC) high-voltage direct-current (HVDC) system is emerging as an important technology for transmitting bulk power over long distances and integrating large-scale renewable energy. However, there are still a number of technical challenges. One of the critical aspects is the fault protection. This thesis focuses on the fault behaviours of the VSC HVDC systems and the connected ac systems when the HVDC system subject to ac or dc faults.

In relation to the dc side faults, the operating characteristics of dc circuit breakers (DCCBs) and the application of DCCBs in dc grids were studied. The factors, such as the current limiting reactor and the surge arrester, which affect the performance of a DCCB to interrupt dc fault currents were investigated through simulations. In order to test the effectiveness of utilising DCCBs to isolate dc faults, experimental validation was carried out by applying DCCB prototypes in a three-terminal VSC HVDC test-rig.

Different dc fault protection approaches were applied in a meshed dc grid which connects to an ac transmission system with two connection points. This aims to investigate the impact of different dc protection approaches on the stability of the integrated ac/dc system. The dynamic interactions between the ac and dc systems were studied further.

In terms of converter ac side fault, single-phase faults which occur in the area between the valve and the interface transformer were studied. The fault characteristics of the valve-side single-phase fault in three converter station configurations were analysed in detail. Fault protection strategies based on the theoretical analysis were proposed and validated through simulations.

The study of this research work is expected to contribute to the design of ac and dc fault protection of HVDC systems.

Abbreviations

AAC	Alternate arm converter
ACCB	Alternative current circuit breaker
CD	Clamp-double
DCCB	Direct current circuit breaker
FB	Full-bridge
HB	Half-bridge
HCB	Hybrid circuit breaker
HVDC	High voltage direct current
IGBT	Insulated-gate bipole transistor
LCC	Line commutated converter
LCS	Load commutation switch
MCB	Mechanical circuit breaker
MI	Mass-impregnated
MMC	Modular multilevel converter
MOSFET	Metal–oxide–semiconductor field-effect transistor
MTDC	Multi-terminal HVDC
NPC	Neutral-point-clamped
OHL	Overhead line
PCB	Printed circuit board
PCC	Point of common coupling
PPL	Paper polypropylene laminate
SCG	Short-circuit generator
SM	Sub-module
SPG	Single-phase-to-ground
SSCB	Solid-state circuit breaker
SSR	Subsynchronous resonance
STATCOM	Static synchronous compensator
UFS	Ultra-fast switch
VSC	Voltage source converter
XLPE	Extruded cross-linked polyethylene

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Chapter 1

Introduction

1.1 Background

Power generation plants, transmission grids and distribution networks are constantly expanding to cope with growing demand. At the same time, the environmental impact due to the burning of fossil fuels needs to be minimised. Renewable energy has a key role to play in this effort. High-voltage direct-current (HVDC), a technology which has been used more than 70 years [1], is suited to transport large amounts of power over long distances with minimum losses. Renewable energy sources, such as wind, solar and hydro, are often located great distances from the end-users. Deployment of HVDC is leading to an increasing number of point-to-point connections in different parts of the world. Fig. 1. 1 shows the existing and future HVDC links in North Europe [2]. Those HVDC links contribute to bringing power to the customers efficiently and in line with demand. This improves power supply security and mitigates the intermittence of renewable energy.

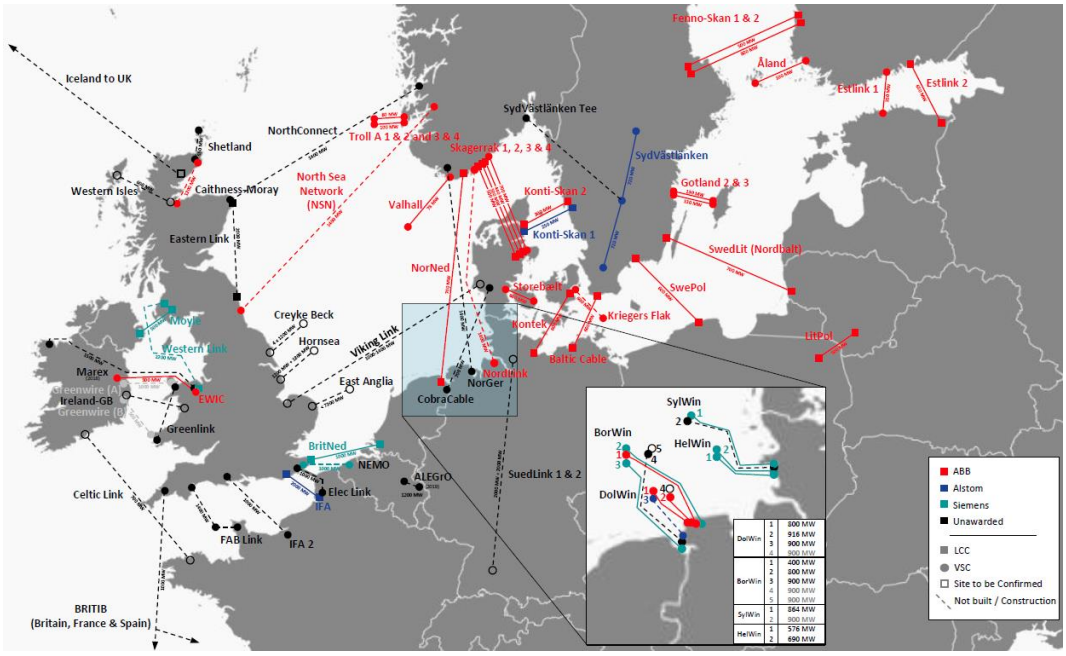


Fig. 1. 1. North Europe HVDC links [2].

The logical next step is to interconnect the links and improve the reliability of the network and balance the power loads. A multi-terminal HVDC (MTDC) grid may reduce the number of converter stations and transmission lines compared to point-to-point configurations. Additionally, the flexible controllability for

Fig. 1. 2. An European dc grid vision [3].

integrating multiple power sources and loads makes the MTDC grid a highly competitive solution to achieve transnational exchange of electricity. Fig. 1. 2 shows a European dc grid vision [3]. This dc grid brings solar power from the desert of Africa to Europe and connects the offshore wind power and hydro power in European countries. Such a large-scale dc grid will provide reliable and cost-effective power transmission services and optimise the value of existing ac infrastructures by utilising state-of-the-art technologies.

In HVDC systems, the voltage source converter (VSC) technology is becoming an attractive alternative to conventional line commutated converters (LCCs) for its features. These include: 1) compact and flexible station layouts, with low space requirements, and a scalable system design; 2) a high dynamic performance and stable operation with ac networks; 3) capability of supplying power to passive networks and black-start; 4) an independent control of active and reactive power; and 5) no voltage polarity reversal during power flow reversal [4]-[7]. Therefore, VSC-based HVDC is more suitable for large-scale renewable energy integration and the deployment of MTDC grids. In particular, modular multilevel converters (MMCs), a type of VSCs, have been implemented in many commercial HVDC projects (*e.g.* INELFE project, Nan'ao three-terminal project and Zhoushan five-

terminal project [9]-[11]) due to their excellent steady-state performance and fault tolerant operation [12].

Although VSC-based MTDC grids complement the existing ac grids by making them more functional and controllable, their large-scale development still faces a number of challenges. One of the major obstacles is the lack of fast and reliable dc grid protections. The absence of current zero-crossings in a dc system inherently makes dc current interrupting more difficult than in ac systems. Even though some manufacturers have produced several fast HVDC circuit-breakers, their high capital costs limit their applications [13]-[14]. The application issues associated with dc circuit-breakers (DCCBs) in dc grids need to be investigated. For instance, the impact of DCCB operation on the dc system and the dc system connected ac systems.

Compared to ac systems, due to the small inductance of the dc circuits, the rate-of-change of the dc voltage and current during a dc short-circuit event can be very high. A dc network is unable to prevent the voltage collapse that occurs in the event of a dc fault from propagating rapidly throughout the network. The converters are not capable to provide voltage support during a dc fault, as they might be blocked immediately to protect themselves from large dc fault currents. The currents from the ac side will keep infeeding to the dc fault if the faulted circuits cannot be isolated quickly and in a reliable manner. From the viewpoint of the dc grid connected ac grid, a fault within the dc grid can be seen as "multiple faults" on the ac system [15]. This may lead to instability of the overall ac/dc system. With the continuously increasing of the HVDC market, more attention is required to be paid to the transient behaviours of the ac and dc grids subject to a dc fault. In addition, the impact of different dc fault isolation and post-fault restoration approaches on the stability of ac/dc systems should be investigated as well.

Apart from dc faults, converter ac fault-tolerant operation is another important aspect of the operation of VSC HVDC systems. As asymmetrical faults are most common in ac systems, the control and operation of VSCs under unbalanced grid conditions has received a significant attention in the literature [16]-[23]. However, converter valve-side ac faults remain an under-researched topic.

Converter transformers are typically installed outside the halls housing the converters. The valve-side winding bushings of these transformers protrude through the hall wall to connect to converter ac buses [24]-[25]. Insulation failure and/or flashover of wall bushings may cause a station internal single-phase-to-ground (SPG) fault between the converter and the transformer [26]. The SPG faults may also occur on switchgears and converter grounding systems which are deployed in the area between the converter hall and the outside transformers. This area, which is in the overlapping protective zones of the converter and the transformer, needs high insulation and to withstand high voltages and large currents. A valve-side SPG fault in this area will lead to severe consequences, such as commutation failures in LCCs, dc voltage oscillations in symmetrical monopole MMCs, and non-zero-crossing fault currents in asymmetrical monopole and bipole MMCs [25]-[30]. The existing analysis of this type of faults in LCCs and two-level VSCs are not applicable to MMCs. Although the probability of the occurrence of station internal ac grounding faults is low, this type of faults is still conditions the future MMC stations have to cope with.

1.2 Research objectives

This thesis focuses on the analysis and protection approaches of VSC HVDC systems subject to ac and dc faults. The main research objectives of this work include:

- To investigate the voltage and current characteristics and response time of DCCBs.
- To validate the application of DCCBs on protecting a dc grid against dc faults through experiment.
- To investigate the impact of different dc grid protection approaches on the stability of integrated ac/dc systems subject to dc faults.
- To analyse the fault characteristics of symmetrical, asymmetrical and bipole MMC HVDC systems subject to valve-side SPG fault.
- To develop protection strategies for symmetrical, asymmetrical and bipole MMC HVDC systems subject to valve-side SPG fault.

1.3 Thesis structure

The structure of the thesis is as follows:

Chapter 2 – Literature Review

In this chapter, the state-of-the-art of the VSC HVDC technologies is overviewed. The challenges in achieving MTDC grids are discussed. Different dc fault handling devices and approaches for MTDC grids are summarised and critically reviewed. The existing research on analysing the stability of ac/dc grids subject to dc faults and converter ac side faults is presented. The problems caused by converter ac side faults, especially the valve-side single-phase faults, are described.

Chapter 3 – Application of DCCB in DC grid

In this chapter, the voltage and current characteristics and response time of DCCBs are firstly investigated in simulations. Then the operation and control of using DCCBs to protect dc grids are validated in a VSC HVDC test-rig.

Chapter 4 – Dynamic Interactions of AC and DC Grids Subject to DC Faults

In this chapter, using different dc fault protection approaches, the dynamic interactions of ac and dc grids under the same dc fault are investigated and assessed. Simulations are conducted in an integrated ac/dc transmission system which contains a 4-terminal meshed dc grid and a 4-machine two-area ac grid.

Chapter 5 – Symmetrical Monopole MMCs under Valve-side Single-phase Faults

This chapter presents the theoretical analysis of symmetrical monopole MMCs under valve-side SPG fault conditions, with a special focus on the investigation of its fault characteristics. The fault responses are broken down into individual contributions from different network components. The influence of key factors, such as converter grounding schemes, dc lines and fault resistance, on fault characteristics are illustrated. A protection strategy based on the theoretical analysis and fault characteristics has been proposed for a point-to-point MMC HVDC transmission system. The analysis and proposed protection strategy are validated through time domain simulations.

Chapter 6 – Asymmetrical Monopole and Bipole MMCs under Valve-side Single-phase Faults

This chapter analyses the characteristics of valve-side SPG faults in asymmetrical monopole and bipole MMCs. Upper arm overvoltage and ac side non-zero-crossing currents arising from SPG faults in the two MMC configurations are investigated. An *LR* parallel circuit is employed to create zero-crossing currents which will enable the operation of grid-side ac circuit breakers. Protection strategies based on the *LR* parallel circuit for asymmetrical monopole and bipole MMCs are proposed to relieve the aforementioned issues. The solutions are verified through time domain simulations.

Chapter 7 – Conclusions

This chapter concludes and summarises the thesis. Contributions of the research work and recommendations for future work are presented.

Chapter 2

Literature Review

2.1 Introduction

The world's first commercial voltage source converter-based (VSC) high-voltage direct-current (HVDC) project was put into operation in 1999 on the island of Gotland [31]. This project is based on the two-level VSC technology with a dc voltage of ± 80 kV and a power rating of 50 MW. Since then, the dc voltage, power rating and transmission distance of VSC HVDC technology have been continuously improving. By the end of 2017, there have been more than 30 system operational VSC HVDC projects worldwide [2]. The highest dc voltage of the modular multilevel converter (MMC) has been developed to ± 800 kV and its rating has been increased to 5000MW [32]. Moreover, there are a number of VSC HVDC projects under construction or being planned.

This chapter gives an overview of the VSC HVDC technology. The key components of VSC HVDC systems are described, including converters, dc circuit breakers (DCCBs), dc transmission lines and converter grounding schemes. DC grid protection approaches are summarised and discussed. The stability analysis of integrated ac/dc grids subject to ac and dc faults in the literature are reviewed. Finally, the converter ac side faults are described and discussed.

2.2 Overview of VSC HVDC technologies

VSC HVDC technology has experienced rapid development in the last two decades. This section aims to provide an overview of this technology and its worldwide development.

2.2.1 Converter topologies

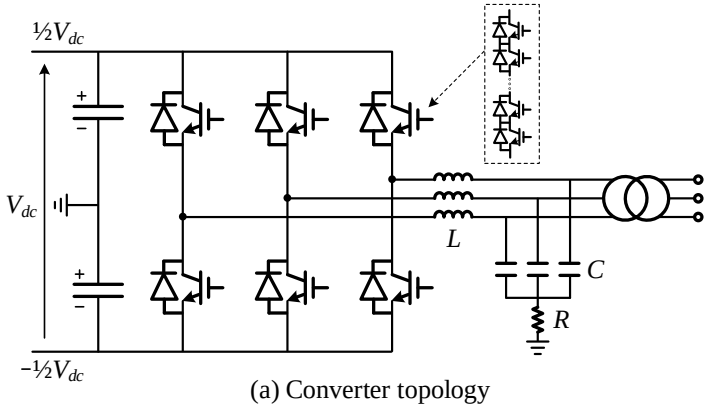
Converter is one of the core elements of HVDC systems, playing a key role in power conversion between ac and dc systems. The requirements of VSC design include converting power with minimum losses, low harmonic, compact dimension, flexible operation and control, high reliability, and fault-tolerant operation [4]-[6].

Three types of converter topologies have been utilised for VSC HVDC systems: two-level converter, three-level neutral-point-clamped (NPC) converter, and modular multilevel converter (MMC).

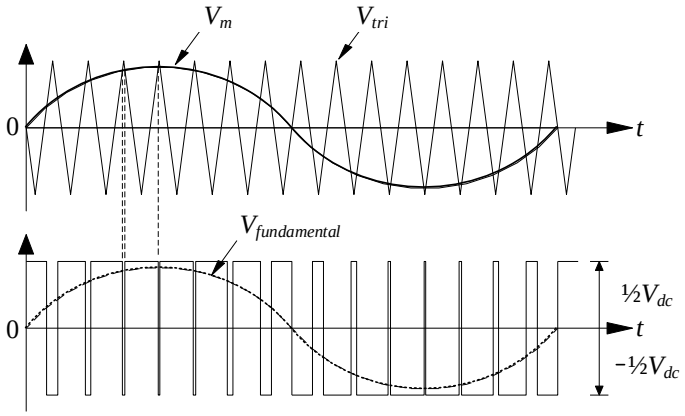
2.2.1.1 Two-level VSC

Two-level VSCs generate rectangular waveforms of high and steep voltage steps. The down and rise of the output voltages stress the components (e.g. converter transformer) and produce harmonics and noise. Extensive filtering and smoothing measurements need to be taken to obtain sinusoidal ac waveforms at the ac terminal. Although the switching frequency can be increased to obtain smoother output waveforms, the power losses will be increased at the same time.

Fig. 2. 1 shows the topology and pulse-width-modulation (PWM) of a two-level converter. The converter consists of six arms which use series connected insulated-gate bipole transistors (IGBTs) as the switching components. The comparison between the modulation signal (V_m) and the carrier (triangle) signal (V_{tri}) produces the PWM signals which are sent to the switches [5]. The output voltages alternate at high frequency between the positive and negative polarities of the charged dc capacitors. The output voltage has the same magnitude but different widths, as shown in Fig. 2. 1(b). A better sinusoidal waveform can be achieved by increasing



(a) Converter topology



(b) Modulation and output ac voltage.

Fig. 2. 1. Two-level VSC.

the switching frequency. Moreover, reactors and filters are needed to smooth the waveforms and reduce harmonics.

The PWM enables the independent control of the magnitude and phase angle of the output voltage which, therefore, achieves the independent control of the active and reactive power. However, there are some inherent disadvantages of this converter: difficulty in turning on/off all IGBTs in the same string simultaneously; high switching losses; large ac filters (note that the filters are still much smaller than LCC HVDC); high insulation requirements on converter transformer to withstand high output voltage stress and electromagnetic interference [5]-[7].

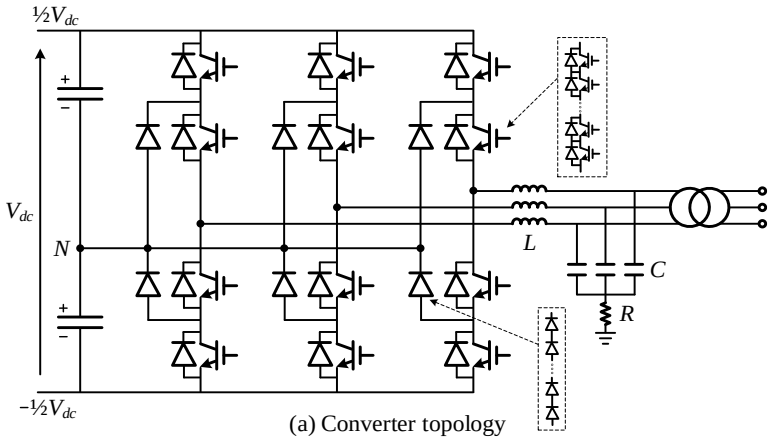
2.2.1.2 Three-level VSC

There are different types of three-level VSCs: NPC, T-type, active NPC and hybrid NPC [33]. Fig. 2. 2 shows the topology and PWM of a three-level NPC. Due to the NPC diodes, the three-level converter is able to generate three voltage levels: $½V_{dc}$, 0 and $-½V_{dc}$. Therefore, this converter reduces the harmonic distortion of the output voltages and lowers the switching frequency compared to the two-level converter. However, this type of converters increases the system complexity and capital costs by involving more power electronic devices. Moreover, large dc capacitors and capacitor voltage balancing controller are needed to avoid the fluctuation of the neutral-point voltage and to reduce the distortion of the output voltage [34]. These disadvantages limit the application of this type of converters in HVDC applications.

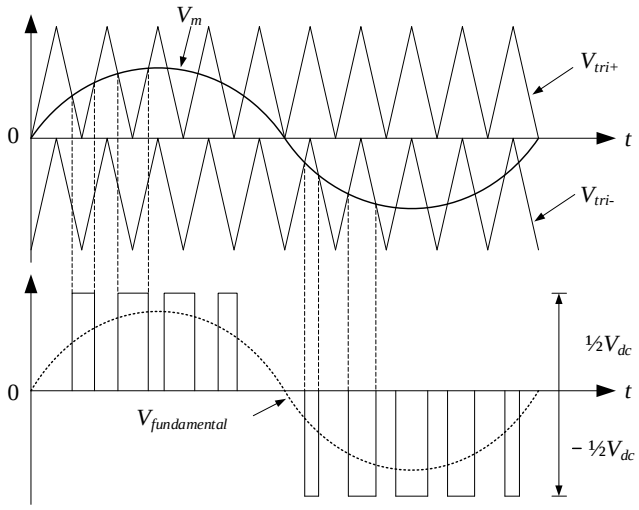
2.2.1.3 Modular multilevel converters

Modular multilevel converter (MMC) opens the prospect of significantly increased ratings of VSC HVDC technologies at acceptable losses/size and a number of new converter functions/roles in dc systems. MMC has lower switching frequency, reduced switching power losses, reduced harmonic components and occupies much smaller passive ac filters than the two-level and three-level VSCs [12].

MMC was firstly proposed by R. Marquardt and A. Lesnicar in 2003 [35]. Its first commercial application was in the Trans Bay Cable project in San Francisco



(a) Converter topology

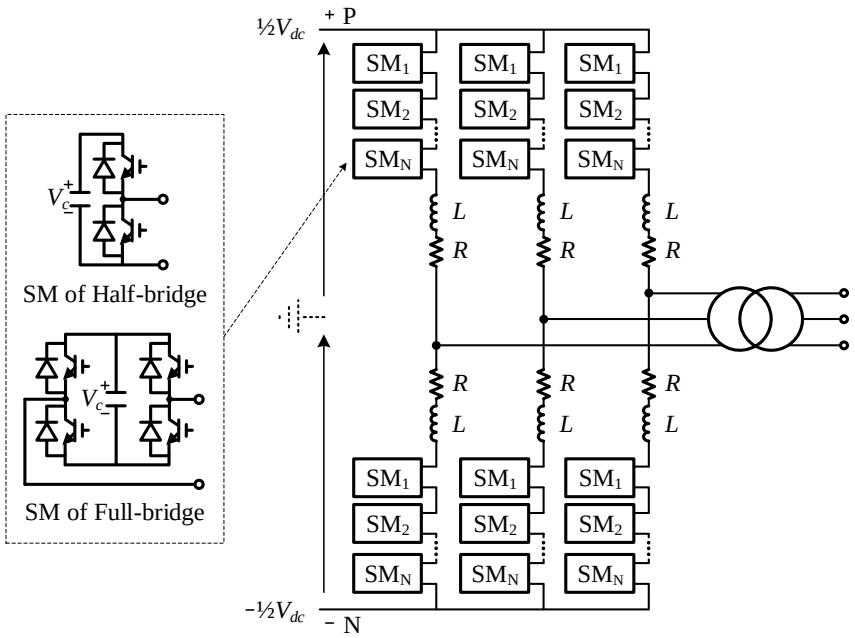


(b) Modulation and output ac voltage.

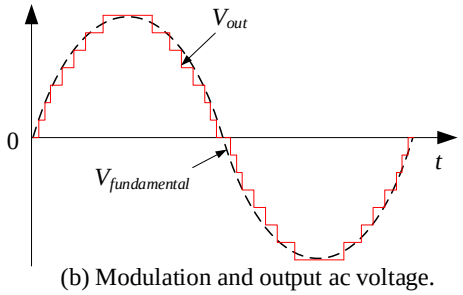
Fig. 2. 2. Three-level NPC.

[36]. Fig. 2. 3 shows the topology and modulation of an MMC. The converter consists of three-phase units. Each phase consists of one upper and one lower arm. Each arm has N series-connected sub-modules (SMs) and one inductor L. The equivalent circuit resistance is represented by resistor R. In steady-state operation, the voltage of each SM is V_{dc}/N. By switching on different numbers of SMs in each arm, a multi-level waveform can be achieved, as shown in Fig. 2. 3(b). There are redundant SMs to ensure the proper operation of the system in case of component failures.

The two main configurations of the SMs are half-bridge (HB) and full-bridge (FB). The HB SM contains two IGBTs as the switching elements, two anti-parallel diodes and a dc storage capacitor, as shown in Fig. 2. 3. The output voltage of the HB SM is either 0 or the dc capacitor voltage (V_c). As for the FB SM, there are four IGBTs and its output voltage can be $+V_c$, 0 and $-V_c$. During normal operation, its



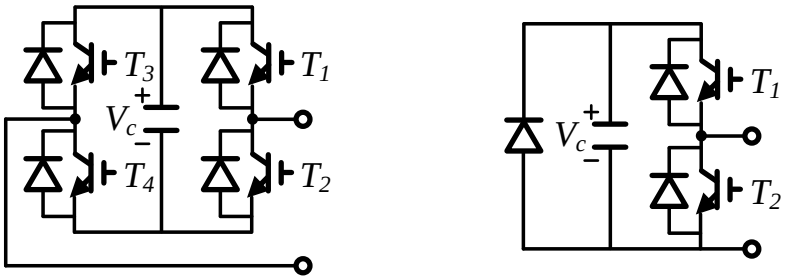
(a) Converter topology



(b) Modulation and output ac voltage.

Fig. 2. 3. Schematic diagram of an MMC.

operating states are the same with HB SM. As shown in Fig. 2. 4, T_3 is off and T_4 is on, the switching of T_1 and T_2 will produce the output voltage $+V_c$ and 0. Although the capital costs and power losses of an FB MMC are nearly twice of an HB MMC, the FB MMC has some important benefits compared to HB MMC: the capabilities of blocking dc fault currents and reversing dc terminal voltage [4].



(a) SM topology (b) Equivalent circuit during normal operation.

Fig. 2. 4. Schematic diagram of an FB SM.

2.2.1.4 Converters after being blocked

The performance of a converter under fault conditions is an important aspect in the stage of project planning and design. Fig. 2. 5 illustrates the equivalent circuits of three types of VSCs after being blocked due to dc faults. As shown in Fig. 2. 5(a), the two-level VSC becomes an uncontrollable bridge once it is blocked. The dc capacitors start to discharge firstly after the fault. Then, the currents from ac side start to infeed to the fault once the voltage on the dc side is lower than the valve-side line voltages.

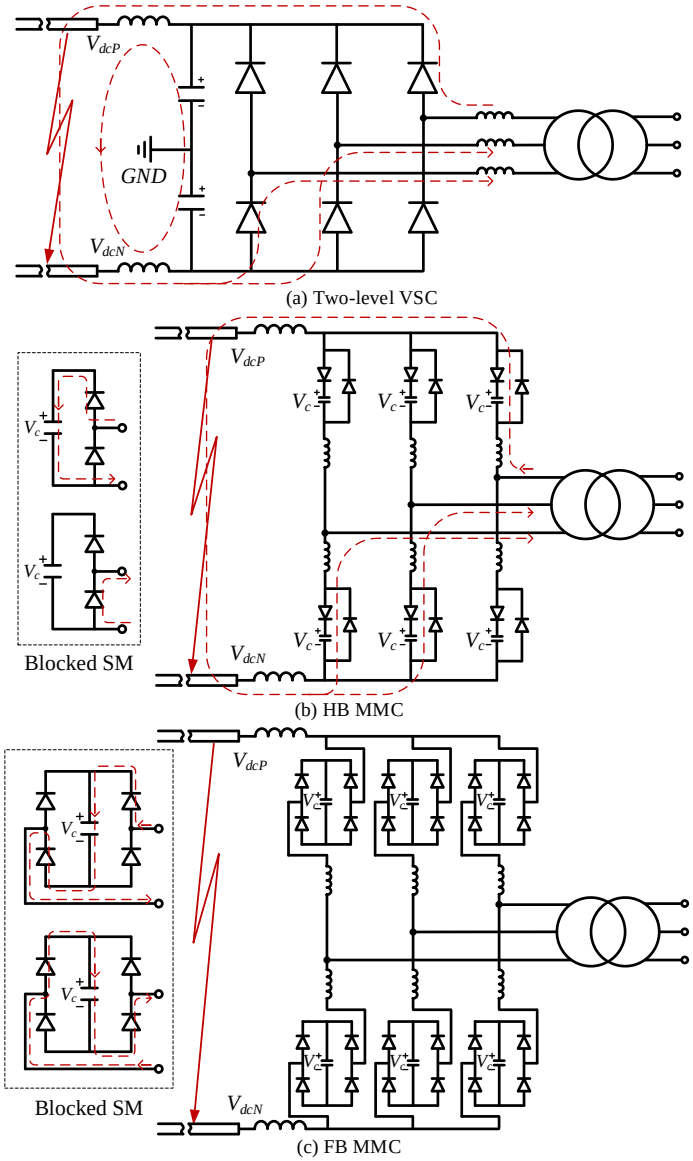


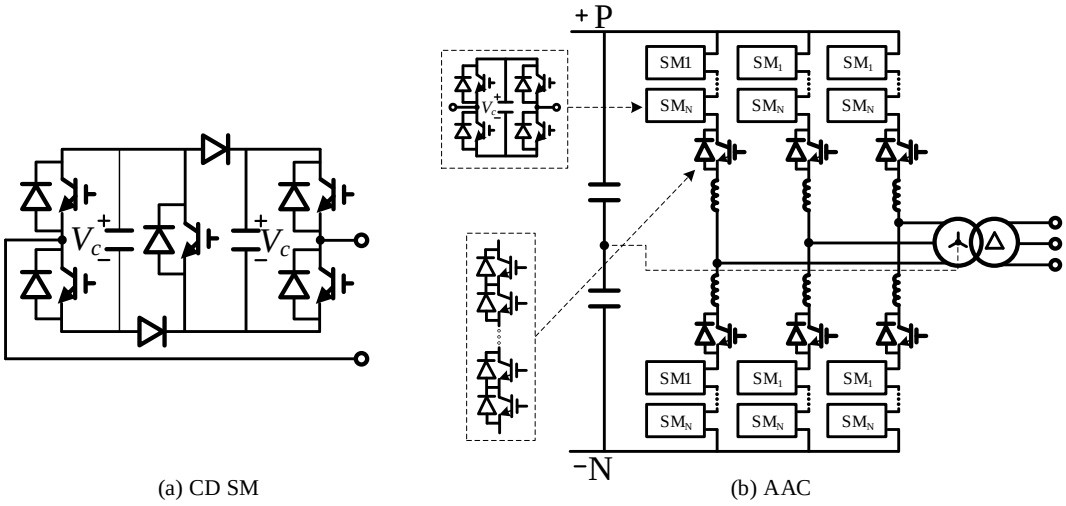
Fig. 2. 5. Equivalent circuits of the blocked converters.

As for the HB MMC shown in Fig. 2. 5(b), its SM capacitors stop discharging due to the upper diode in the SM. However, the capacitor can be charged through

the upper diode if the dc voltage experiences transient oscillations and is higher than the arm voltage. At the same time, the infeeding currents from converter ac side will keep flowing through the lower diode.

In comparison with two-level VSC and HB MMC, FB MMC has the capability of blocking ac side infeeding currents. Fig. 2. 5(c) illustrates current paths of a blocked FB SM. It can be seen that the SM capacitor will be charged regardless of the directions of arm currents. The ac infeeding currents will be blocked immediately once the sum voltage of all SM capacitors in the arms is higher than the valve-side line voltage.

In order to achieve the fault blocking capability and to reduce the power losses during normal operation, different topologies of MMCs have been proposed [1], [12] such as the clamp-double MMC (CD MMC) [37] and alternate arm converter (AAC) [38], as shown in Fig. 2. 6.



(a) CD SM (b) AAC

Fig. 2. 6. MMCs with dc fault blocking capability.

The SM of the CD MMC consists of two HBs connected in series through two diodes and one IGBT with its anti-parallel diode. The two capacitors in the CDSM will be in parallel and provide opposing voltage once all the IGBTs are blocked and therefore the fault current will be blocked. With the same number of voltage levels, the power losses of CD MMC are higher than HB MMC and lower than FB MMC. Moreover, additional design considerations are required to be considered to solve the problem that the two capacitors in the CD SM may have different voltages before they are connected in parallel [1].

The so-called AAC, as shown in Fig. 2. 6(b), combines FB SMs and series connected IGBTs to achieve fault blocking capability. In particular, the number of power electronic components are reduced and hence reduces the capital costs and overall power losses. However, the fixed ratio between direct and alternating voltages (an ideal operating condition) restricts the operation of the converter [4], [38]. Moreover, the AAC requires dc side filters to eliminate dc side harmonics.

More MMC topologies with dc fault blocking capability can be found in the literature [1], [4], [12].

2.2.2 Converter station configurations

The converter station is the place hosting the converter valve hall, transformers, converter grounding devices, switchgears and other equipment. Converter stations can be built with configurations according to the operating requirements, such as symmetrical monopole, asymmetrical monopole and bipole [5]-[7]. Fig. 2. 7 depicts possible configurations for VSC and hybrid LCC/VSC HVDC systems.

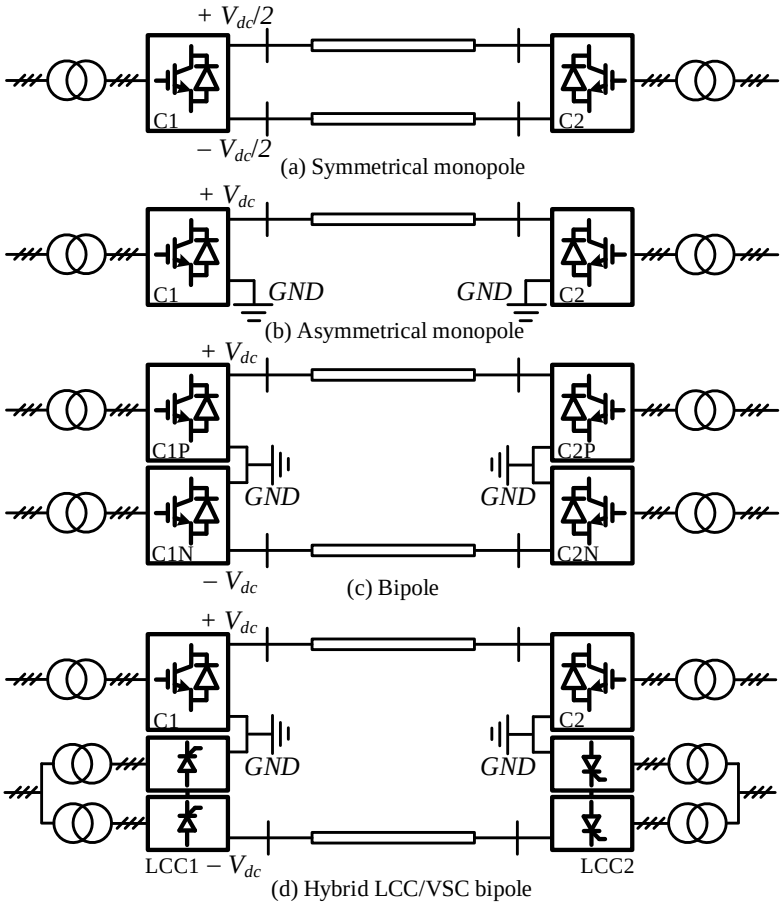


Fig. 2. 7. VSC and hybrid LCC/VSC HVDC systems.

A symmetrical monopole is shown Fig. 2. 7(a), which features two poles with opposite voltage potential. Both poles need to be fully insulated. Conversely, only one polarity is present in the asymmetrical monopole shown in Fig. 2. 7(b). The dc current returns through the ground or a metallic return path and thus low-voltage insulation is required for the metallic return line. The drawbacks of this configuration include a lack of redundancy during faults, corrosion on the metallic pipes in the ground and potential negative environmental effects [8].

A bipole VSC HVDC system is shown in Fig. 2. 7(c). The system consists of two independently controlled asymmetrical monopoles. This configuration offers a higher reliability and flexibility compared to monopole systems. For instance, the loss of any converter entails a 50% loss of the total transmission capacity only. A single asymmetrical monopole link can also be installed in parallel with an existing LCC link as a hybrid LCC-MMC bipole HVDC system, as shown in Fig. 2. 7(d). The VSCs in this topology can minimise the risk of commutation failures on the nearby LCC link and minimise the overvoltage when the LCC link is blocked [29]-[30].

2.2.3 HVDC circuit breakers

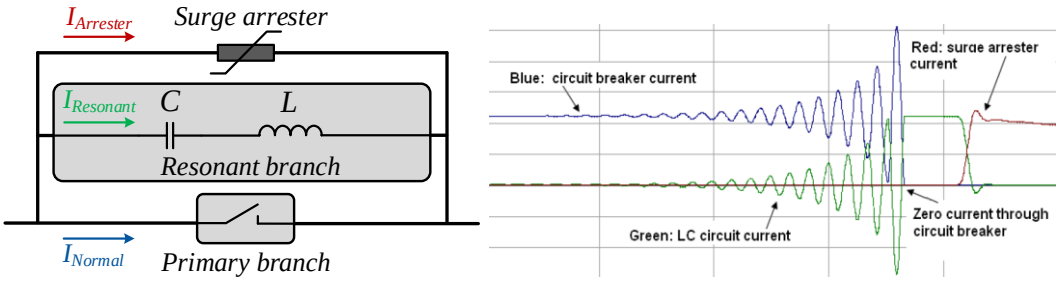
Fast and reliable DCCBs are considered by both the academia and the industry as key components to remove the obstacles in the development of large-scale dc systems [39]-[41]. DC fault current interruption is challenging due to the lack of natural current zero-crossings and the current's fast rate-of-change [40]-[41].

Research on DCCBs is a topic dating back to the 1970s. Since then a number of DCCB topologies have been proposed for different applications [42]-[45]. DCCBs are normally categorised into three main types: mechanical circuit breaker (MCB), solid-state circuit breaker (SSCB) and hybrid circuit breaker (HCB) [40]-[41].

2.2.3.1 Mechanical circuit breaker

Fig. 2. 8 illustrates the schematic diagram and current breaking process of an MCB. Normal operating current flows through the primary branch which consists of a mechanical breaker. Little power loss is produced in this branch due to the small resistance of the mechanical breaker. The mechanical breaker will start to open once a fault is detected. The fault current will be forced into the resonant

branch by the arc voltage between the two contactors of the mechanical breaker. Then, the current in the resonant branch starts to oscillate due to the *LC* circuit. The mechanical breaker will fully open once the first current zero-crossing occurs [41].



(a) Topology (b) Current breaking process [42]

Fig. 2. 8. A classical MCB.

In the early years, the operating time of MCBs was tens or even hundreds of milliseconds mainly due to the operating time of mechanical switches and the time to wait for current zero-crossings. In order to reduce the operating time, active resonant circuits [44]-[50] or electromagnetic force based fast mechanical switches [43], [51]-[53] have been developed recent years. For instance, the active resonant MCB proposed in [46] shown in Fig. 2.9 is able to interrupt a 16 kA dc fault current under 80 kV within 8 ms [47]. The world's first ± 160 kV active resonant MCB which can interrupt 9 kA within 3.5 ms has been deployed in the Nan'ao three-terminal HVDC network [48]-[49].

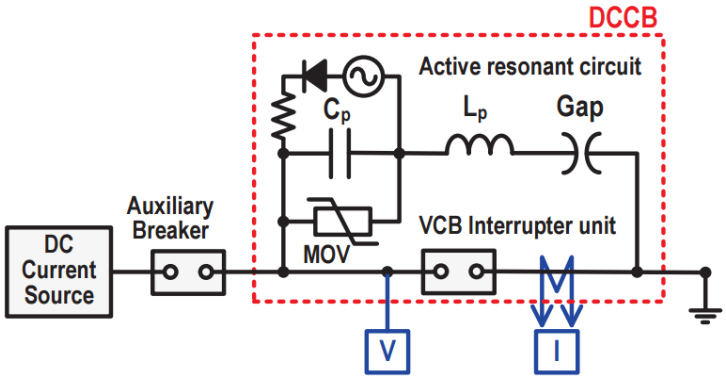
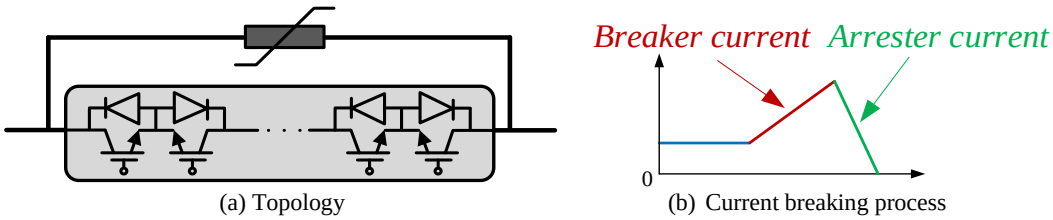


Fig. 2. 9. An active resonant mechanical circuit breaker [46].

2.2.3.2 Solid-state circuit breaker

SSCB, as shown in Fig. 2. 10, based on power electronic devices exhibits a faster response compared to MCBs and can interrupt dc fault currents in a few microseconds. However, the high on-state losses and capital costs are the main drawbacks of this technology. Moreover, a cooling system might be needed due to

the on-state heating, which increases the complexity and dimension of the system, and therefore increases the capital costs [39].

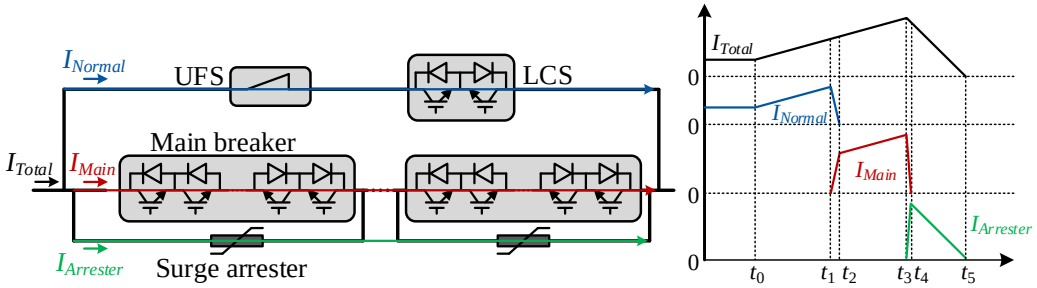


(a) Topology (b) Current breaking process

Fig. 2. 10. A classical SSCB.

2.2.3.3 Hybrid circuit breaker

The long operating time of MCBs and high losses of SSCBs cannot meet the requirements for building MTDC grids. However, a combination of these breaking devices and hence of their capabilities has resulted in the HCB [13], [54]-[55], which has become the most common DCCB design topology.



(a) Topology (b) Current breaking process

Fig. 2. 11. A classical HCB.

These devices normally have three branches as illustrated in Fig. 2. 11(a): a normal operation branch which contains a load commutation switch (LCS) and an ultra-fast switch (UFS); a main breaker branch which is formed by several power electronic switches (normally IGBTs); and an energy dissipation branch which consists of surge arresters.

The currents in different branches during the current breaking process are depicted in Fig. 2. 11(b). A fault occurs at t_0. The LCS turns off at t_1 once fault discrimination ends. At the same time, the main breaker turns on. The current starts to commutate into the main breaker due to the large resistance of the blocked LCS. The UFS starts to open at t_2 once the current totally commutates into the main breaker. The main breaker is turned off at t_3 once the UFS is fully opened. After t_4, the current is fully forced into the surge arresters where it will be totally dissipated at t_5.

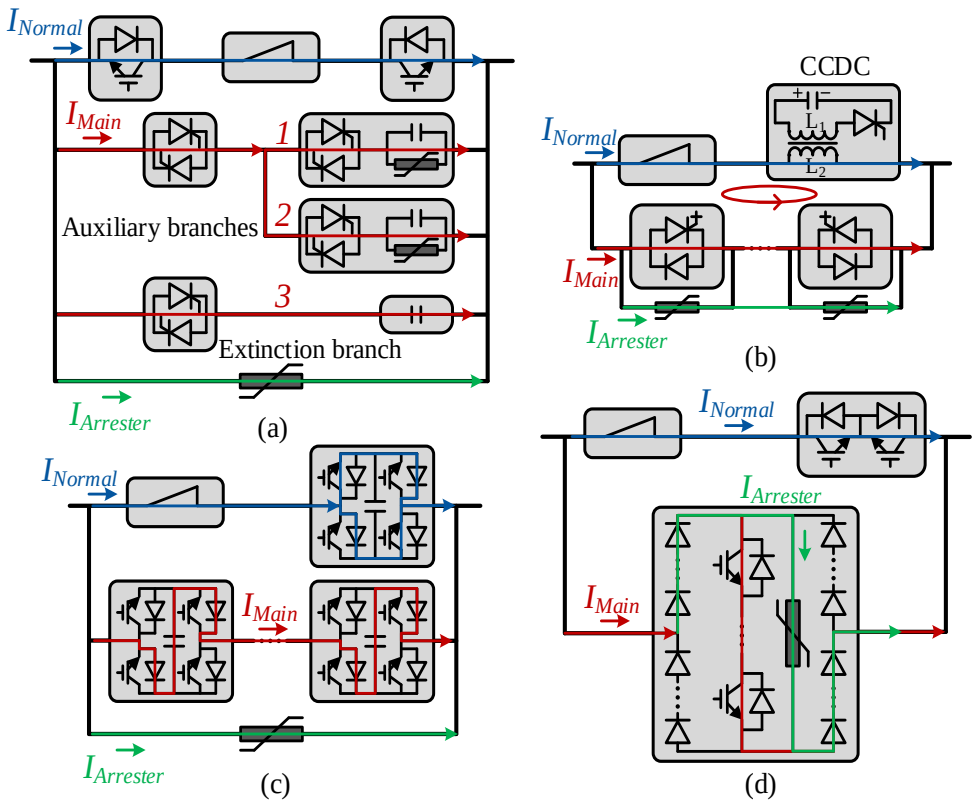


Fig. 2. 12. Schematic diagrams of modified HCBs.
(a) HCB with thyristor and capacitor based main breaker; (b) HCB with CCDC; (c) HCB with FB SMs; (d) HCB with diode-based H-bridge.

In recent years, HCBs have been extensively studied by both the industry and the academia [39], [55]-[60]. Fig. 2. 12 illustrates some of the latest proposed HCB topologies. A modified HCB, shown in Fig. 2. 12(a), has been proposed in [55] to avoid the dynamic voltage control of series-connected IGBTs and reduce the costs by using fewer IGBTs. The main breaker consists of multiple auxiliary branches and an extinction branch. There are anti-parallel thyristors and capacitors in the auxiliary branches. The capacitors start to be charged once the fault current commutates into these branches. The fault current will be interrupted in the extinction branch once the voltage on the capacitor exceeds the rated voltage of the arrester. Although this HCB topology reduces the number of semiconductor switches, more auxiliary branches are required to limit larger fault currents, which in turn may extend the commutation time and therefore, increase the magnitude of the fault current.

With the aim of reducing the commutation time and on-state power losses, a current commutation drive circuit (CCDC) has been proposed for HCBs [44]-[45].

Fig. 2. 12(b) depicts the circuit schematic for the CCDC. The thyristor within the CCDC will be turned on once fault discrimination ends. Then the pre-charged capacitor starts to discharge immediately which results in a loop current through L_2. The current in the normal operation branch will be quickly forced into the main breaker by the generated loop current. Compared to traditional LCSs, the CCDC exhibits low power losses, low costs and no need for a cooling system. However, the transient current produced in the CCDC during the commutation process is extremely high, which may burn the CCDC and/or other parts of the CB in extra HV applications.

The HCB shown in Fig. 2. 12(c) employs FB SMs to solve the dynamic voltage balancing issues of IGBTs [58]. The current interruption capability is also enhanced as the fault current passes through two switches in each SM. However, this topology needs additional capacitors and the number of power electronic devices is doubled compared to the HCB shown in Fig. 2. 11. Therefore, capital costs and power losses are more than doubled, which are the main drawbacks of this device. This HCB has been deployed in the Zhoushan five-terminal project [11].

A commutation-based HCB proposed in [61], shown in Fig. 2. 12(d), uses diode-based H-bridges as the extinction branch. Compared to the HCB in Fig. 2. 11, this design can theoretically reduce the number of IGBTs by half if a unidirectional module (the main breaker) is employed to interrupt bidirectional fault currents. Moreover, the decrease of IGBTs also increases system reliability. This topology uses multiple medium voltage modules to achieve a modular, compact and scalable design. As the H-bridge contains many series connected diodes, the stray inductance of the circuit may result in a long current commutation time, and further lead to a large fault current magnitude. The parameters of HCBs developed by the main technology manufacturers are shown in Table 2. 1.

Table 2. 1. Parameters of HBCs from typical manufacturers.

	NR [61]	**GEIRI** [58]	**GE** [55]	**ABB** [13]
Rated voltage	± 500 kV	± 200 kV	120 kV	320 kV
Rated current	3 kA	2 kA	2 kA	2 kA
Interruption current	25 kA	15 kA	5.2 kA	8.5 kA
Operating time	5 ms	5 ms	5.5 ms	5 ms

2.2.4 HVDC overhead lines and cables

Both dc overhead lines (OHLs) and cables are used in dc transmission. The choice is influenced by environmental constraints as well as an overall optimisation that considers total capital cost, performance, losses and transmission system reliability [6].

2.2.4.1 HVDC overhead lines

The power-carrying capability of HVDC OHL is substantially higher than ac systems. Gains of up to 80% in transmission capacity can be reached when converting existing ac transmission lines (double circuit) to dc operation [62]. In order to increase the power capacity of the existing ac transmission corridors, analysis and work have been carried out on converting ac lines into dc operation in [63]-[67].

When comparing ac and dc OHLs, dc lines are more susceptible to flashovers due to the dust on insulators and the constant polarisation of the air surrounding the wires [68]. Since OHLs are more vulnerable to lightning strikes and pollution, dc short-circuit occurs more in OHL-based dc systems than dc cable-based systems [69]. In addition, the protection of non-permanent faults in OHL-based MTDC grid is an important aspect that has to be solved [69]-[71].

2.2.4.2 HVDC cables

There are mainly three types of cables used for HVDC applications: mass-impregnated (MI), self-contained fluid-filled, and extruded [72]-[75]. Of these, the MI cable and the extruded cable are most commonly used.

A. Mass-impregnated cable

The MI cable has been in service for more than 40 years and has been proven as a highly reliable technology. Voltages up to 600 kV and current ratings of 1800 A are available, corresponding to a maximum pole rating of 1100 MW and bipole rating of 2200 MW. The insulation material is paper, impregnated with a high-viscosity compound.

The MI cable also has some specific disadvantages: the low operating temperature tolerance reduces the power capacity, and the cable is expensive and

heavy compared to polymeric extruded cables. The cable is also very difficult to install as the jointing process is difficult. There are some new developments of this kind of cable including the using of paper polypropylene laminate (PPL) [75].

B. Extruded cross-linked polyethylene cable

The extruded cross-linked polyethylene (XLPE) cable is not well suited for LCC HVDC as space charges in the insulation material might cause damage to the cable at power reversals. XLPE cables are mainly used for VSC HVDC as there is no voltage polarity reversal when reversing the power flow. This technology has been applied at voltages up to ± 200 kV (in service with a power capacity of 500 MW), with several larger projects at an advanced construction stage which use voltages of ± 320 kV and have power ratings between 800 MW and 1000 MW per converter [5]. Currently, higher XLPE cables (and accessories) at higher voltages (up to 500 kV) are being tested and expected in the near future [75].

Compared to MI cables, XLPE cables have some advantages: lighter weight, smaller bending radius and lower manufacturing costs. The installations of this type of cable are also faster and less expensive. Furthermore, a higher conductor temperature can be used, giving an overall more compact cable for the same power rating. Table 2. 2 gives the summary of the typical HVDC cables of MI and XLPE [75].

Table 2. 2. Summary of typical MI and XLPE cables.

Cable Technology	Maximum rated operating voltage	Maximum power (cable pair)	Maximum continuous conductor temperature
MI	600 kV MI-PPL (installation) 500 kV MI (installed)	2200 MW (installation) 1600 MW (installed)	70-80 °C (MI-PPL) 55-60 °C (MI)
XLPE	400 kV (awarded) 320 kV (installed)	1400 MW (installation) 1000 MW (installed)	70 °C

MI – Mass Impregnated; PPL- Paper Polypropylene Laminate
XLPE- Extruded Cross-Linked Polyethylene

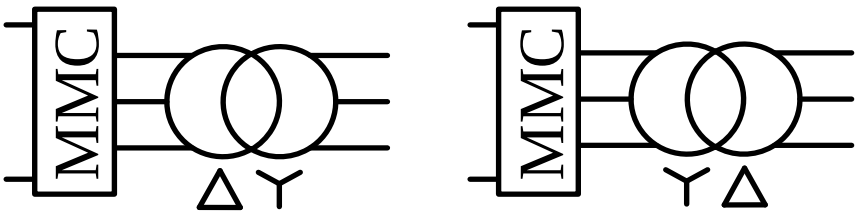
2.2.5 Converter grounding schemes

Converter grounding scheme is an important aspect in HVDC transmission systems. A grounding point provides a zero-potential reference for the control and

protection systems. It is the reference for calculating overvoltage and insulation coordination in converter stations as well. The groundings can be deployed either on the ac side or dc side and each grounding scheme has its merits and demerits. As the converter grounding systems of two-level and three-level have been widely studied in the literature [76]-[79], only the grounding schemes of MMCs are presented in this section.

2.2.5.1 Ungrounded

Fig. 2. 13 shows the cases MMCs are ungrounded either on the ac side or dc side. The windings of the transformers are connected in a delta/star (Δ/Y) and star/delta (Y/Δ) configuration which can filter harmonics and prevent zero-sequence components flowing between the converter and its ac grid [78]-[82]. The voltage potential reference can be provided by other converters. This ungrounded scheme can be applied for MMCs which are not used to start-up charging an MTDC network. This ungrounded scheme is also not applicable to the MMCs which need to run as a static synchronous compensator (STATCOM) [83]. Moreover, if an unbalanced voltage between the two dc poles occurs, for example, caused by MMC blocking, control system errors, and unbalanced ac faults [80], the unbalanced voltage will continually exist in an ungrounded system which is the drawback of this scheme.

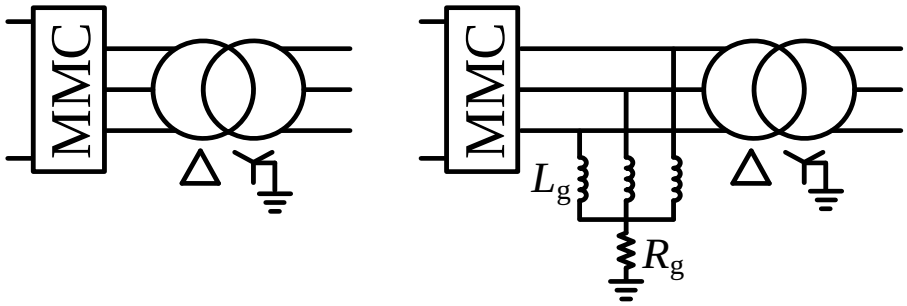


(a) Transformer Δ/Y (b) Transformer Y/Δ

Fig. 2. 13. Converters without grounding.

2.2.5.2 Delta/Star and Delta/Star with Star-point reactor

The delta/star (Δ/Y) grounding schemes shown in Fig. 2. 14 are widely used in VSC HVDC transmission systems. The grid-side Y connection is typically arranged with a solid neutral grounding. The dc side zero-potential reference of the MMCs using the scheme shown in Fig. 2. 14(a) can be provided by other MMCs. As for the scheme in Fig. 2. 14(b), the star-point reactors with a grounding resistor is



(a) Transformer Δ/Yg (b) Transformer Δ/Yg with the Star-point reactor

Fig. 2. 14. Delta/Star grounding schemes.

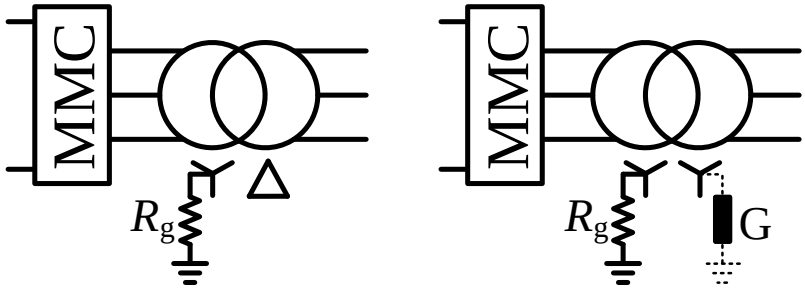
applied to provide zero-potential reference [84]. The grounding resistor is used to block zero-sequence current during both normal and fault conditions.

The parameters of the reactor and resistor are designed as a large impedance to reduce the consumption of reactive power. However, if the reactance is too large and/or the valve-side voltage is high, it will bring problems for manufacturing, insulation, transportation and increasing the footprint of the converter station, and therefore, increases capital costs [85]. The grounding resistor cannot be too large, otherwise, the system will be equivalent to ungrounded. Moreover, due to the reactive power consumption of the reactors, this scheme will affect the grid-side ac voltages during the start-up and converter blocking processes. Therefore, the scheme in Fig. 2. 14(b) is suitable for MMCs connecting to strong ac grids, which has been applied in Zhoushan station in the Zhoushan five-terminal project [11], the Trans Bay Cable project [86] and the INELFE project [87].

2.2.5.3 Star/Delta and Star/Star

Fig. 2. 15 shows transformer Y connections on converter valve-side. There is a high-resistance grounding at the neutral point of the Y connection. The grid-side connection of the transformer can be either Δ or Y connection which depends on the requirements of its connected ac system, transformer protection system and system insulation levels [10], [88]. The grid-side neutral point of Fig. 2. 15(b) can be grounded or ungrounded according to the requirements of the grid-side system.

Compared to the start-point reactor grounding scheme, this arrangement does not need reactors, therefore, this arrangement is more economical. This scheme will not consume reactive power during normal operation as well. However, in normal



(a) Transformer Yg/Δ (b)Transformer Yg/Y(g)

Fig. 2. 15. AC side high-resistor.

operation, small zero-sequence current will flow through the neutral point, and therefore produce power losses and might affect the operation of the transformer. During fault conditions, the dc components of fault currents will flow through the neural point which might induce dc magnetic bias on the transformer, and therefore affect its life expectancy [85]. In order to limit unbalanced currents in both normal and fault conditions, the grounding resistor is required to be high. However, at the same time, the grounding resistor cannot be too high, otherwise, the grounding system will be equivalent to ungrounded. The scheme in Fig. 2. 15(a) has been deployed in the Nan'ao three-terminal project [10] and the scheme in Fig. 2. 15(b) has also been deployed in the Yangshan station Zhoushan five-terminal project [11].

2.2.5.4 DC side high-resistance grounding

Fig. 2. 16 shows the grounding system using two large resistors with a neutral point to provide dc side zero-potential reference. This arrangement is economical and easy to install. The main function of the two large resistors is to clamp the positive and negative dc pole voltages and to make them symmetric.

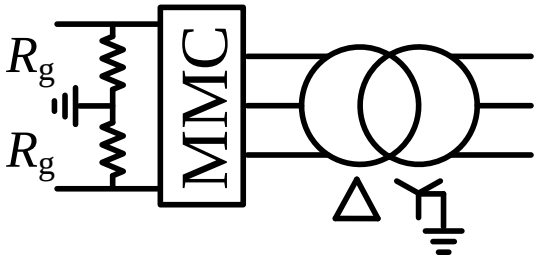


Fig. 2. 16. DC side high-resistance grounding.

The performance of this scheme is highly dependent on its resistance. A small resistance provides good performance on clamping the pole voltages and fast post-fault recovery. However, the power losses will be high if the resistance is small,

especially in the case of the dc voltage is quite high, and then the insulation, heat dissipation and manufacturing of the grounding resistors will be issues. If the resistance is too large, grounding system will be equivalent to ungrounded and will increase the footprint of the substations. Moreover, the resistance may affect the sensitivity of the dc protection systems [88]. This grounding scheme has been employed in the Nanhui offshore wind power connection project [89].

2.2.6 Multi-terminal VSC HVDC networks

The successful applications of point-to-point HVDC links worldwide indicate that greater economic and technical advantages might be achieved by MTDC systems [90]. There have been several MTDC networks based on the conventional LCC HVDC technology, such as the tree-terminal Sardinia-Corsica-Italy network, the three-terminal Hydro-Québec – New-England network and the three-terminal North-East Agra network [91]-[93].

Although the LCC HVDC technology is a well-proven technology that offers high power transmission capacity, it has limited active and reactive power control and the problem of reversing voltage polarity when changing power flow direction. VSC has independent active and reactive power control capability over LCC and its polarity remains unchanged when the directions of power flow change. Therefore, VSC becomes an attractive alternative to LCC for integrating renewable energy and flexible multi-terminal operation [5]-[7]. Some VSC MTDC networks have been constructed or under construction.

2.2.6.1 Nan'ao three-terminal network

The Nan'ao three-terminal HVDC network was the world's first multi-terminal network based on VSC HVDC technology. The project was successfully commissioned on 19th December 2013 [94]. The objective of this project is to incorporate the existing and future wind power generation on the Nan'ao island into the mainland power grid [10].

Fig. 2. 17 shows the system configuration of the Nan'ao project. Its rated dc voltage is ±160 kV and the rated power of the three converter stations is 200 MW (SC station)-100 MW(JN station)-50 MW(QA station). The converters used in this project are HB MMCs. In the next stage, the Tayu (TY) offshore wind farm will be

built and connected to the MTDC network as the fourth terminal [10]. DCCB is not employed in this project and the ac circuit breakers (ACCBs) installed at the ac side of the converters are used to protect dc side faults.

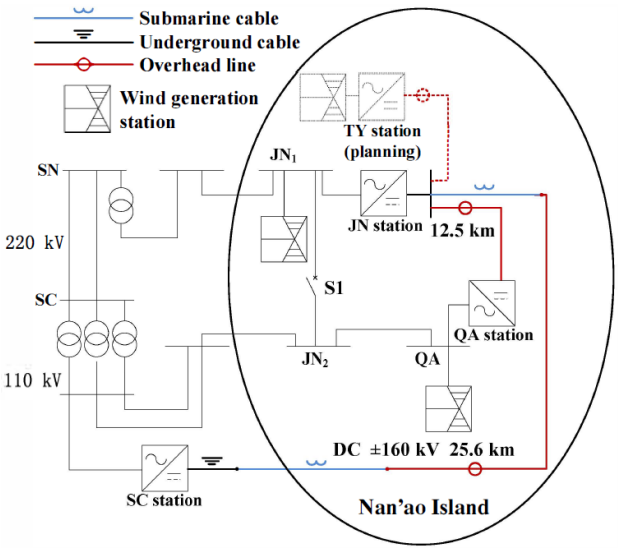


Fig. 2. 17. The configuration of the Nan'ao MTDC network [10].

2.2.6.2 Zhoushan five-terminal network

The world's second multi-terminal VSC MTDC system is the five-terminal Zhoushan network, which was commissioned on 4th July 2014 [95]. Fig. 2. 18 illustrates the system configuration of the Zhoushan project. This MTDC network connects different islands, enhances the strength of the grid structure and improves the reliability of power supply. Moreover, it also allows the integration of large-scale onshore and offshore wind power [11].

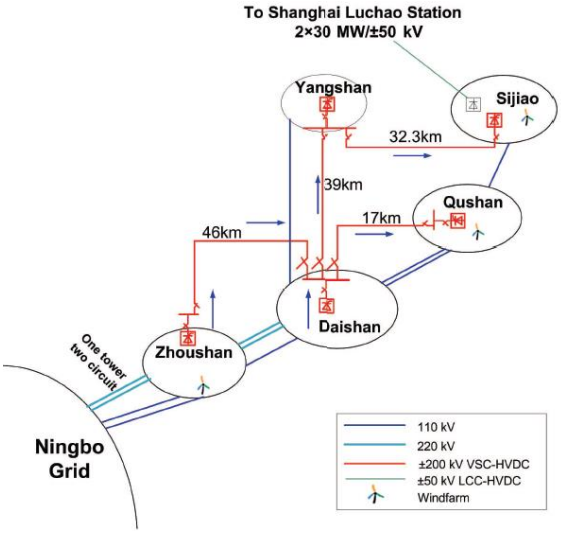


Fig. 2. 18. The configuration of the Zhoushan MTDC network [11].

The dc voltage is ± 200 kV. The rated power of the five converter stations is 400 MW (Zhoushan station)- 300 MW (Daishan station)- 100 MW (Yangshan station) -100 MW(Sijiao station) -100 MW(Qushan station). DCCBs based on FB SM, as shown in Fig. 2. 12(c), have been installed in this system on 29th December 2016 [95]. In the future, another dc line will be constructed between the Yangshan and Zhoushan stations to form a dc grid which will provide redundancy and reduce transmission losses [11].

2.2.6.3 Zhangbei MTDC grid

The Zhangbei project will be the first meshed MTDC grid in the world once completed in 2018. The project is designed to secure the power supply to Beijing from a variety of clean energy sources, including wind, solar and hydro power [97].

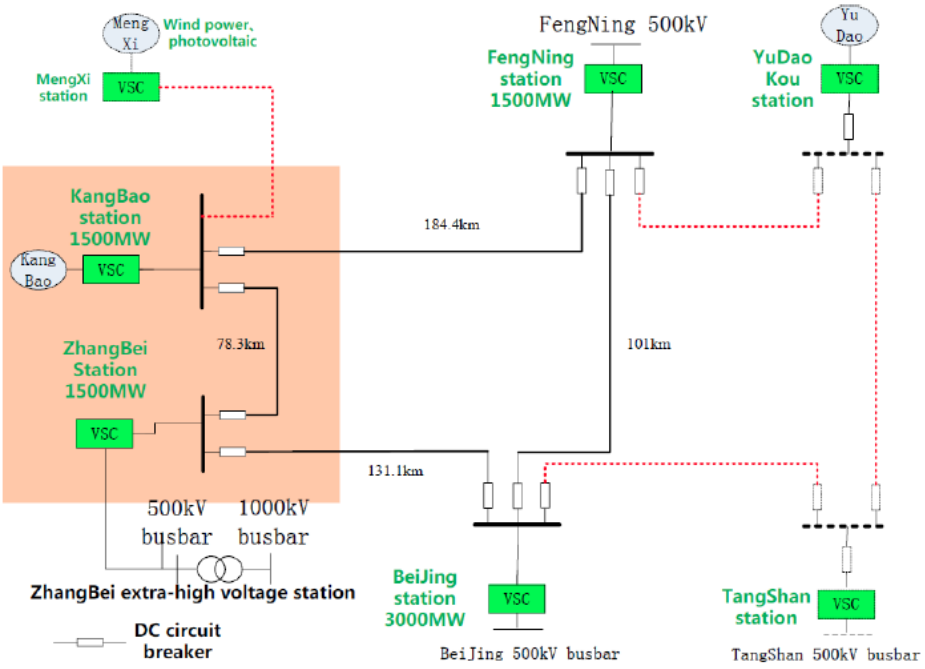


Fig. 2. 19. The configuration of the Zhanbei MTDC grid [90].

Fig. 2. 19 shows the system configuration of the Zhangbei project. The dc voltage is ± 500 kV. The dc transmission lines are OHLs. The DCCB shown in Fig. 2. 12(d) will be deployed in this project [98]. In the first phase, four stations will be built, including 3 sending terminals (1500 MW each) and one receiving terminal (3000 MW). Another two terminals have been planned for the second phase, with commissioning expected in 2021.

2.2.6.4 Other installations and projects

Apart from the above projects which are clearly MTDC systems, there are some installations and projects can be considered or may be used as multi-terminal systems.

A. Atlantic Wind Connection Project

The Atlantic Wind Connection Project is an offshore, undersea transmission line that spans the mid-Atlantic region. The VSC HVDC technology is used in this project. It consists of three links, as shown in Fig. 2. 20: the New Jersey Energy Link, the Delmarva Energy Link and the Bay Link [99].

Fig. 2. 20. The Atlantic Wind Connection Project [99].

The project is built in phases in coordination with the development of offshore wind projects. When complete, it will consist of 12 converter stations and converter platforms [90] and support the development of up to 6000 MW of offshore wind energy, which is enough to power over 2 million homes [99]. Subject to the receipt of permits and availability of materials, components, and equipment, the entire system is planned to be in operation by 2021 [100].

B. Tres Amigas Superstation project

The Tres Amigas Superstation utilises the HVDC technology to link the Eastern, Western, and Texas interconnections at a single location in New Mexico via a multi-node, multi-terminal interconnection [101]. The design concept of the project is illustrated in Fig. 2. 21.

Although the initial project called for the development of a three-terminal HVDC bus with the potential use of high-temperature superconductor cable and HVDC power circuit breaker systems, in 2010 the concept was revised, and the present plan is called for a traditional power transmission node [102]. The first phase of the project started from November 2015 [103]. The final project will have 3×750 MW VSCs and 3×920 MW LCCs. The project also has the opportunity to build a 20 MW or more battery energy storage park at its interconnection with East and West to provide power balancing for the intermittent generation from the renewable energy sources [104].

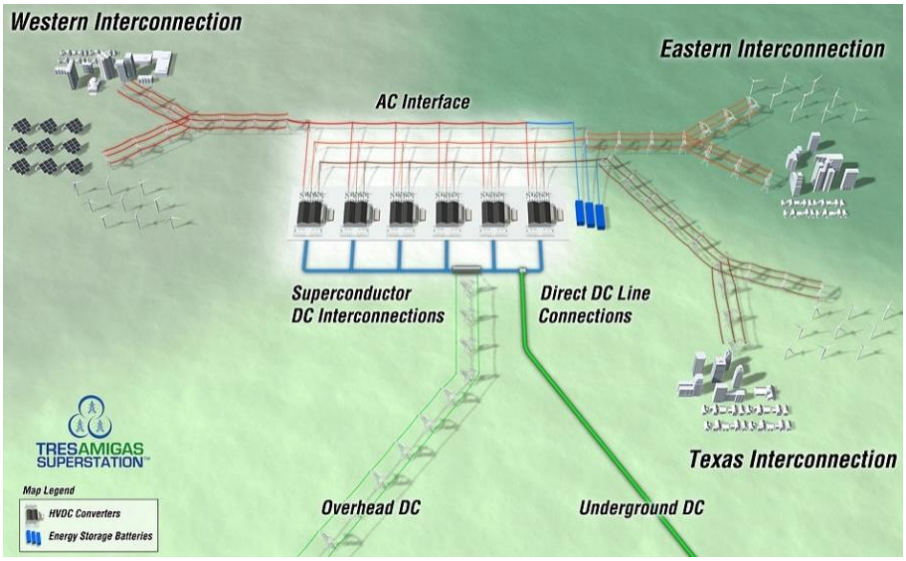


Fig. 2. 21. The Tres Amigas Project [101].

2.2.7 HVDC grid code

Whilst ac grid codes are well documented and are constantly being updated, HVDC grid codes are still being developed. The drafting of dc network codes of the European Commission relating to HVDC grid connection codes is with Agency for the Cooperation of Energy Regulators (ACER), European Network of Transmission System Operators for Electricity (ENTSO-E) and market participants.

The ENTSO-E represents 43 electricity transmission system operators (TSOs) from 36 countries across Europe. ENTSO-E members share the objective of setting up the internal energy market and ensuring its optimal functioning, and of supporting the ambitious European energy and climate agenda. One of the important issues on today's agenda is the integration of a high degree of Renewables in Europe's energy system, the development of consecutive flexibility, and a much more customer centric approach than in the past [105].

ENTSO-E has drafted a Network Code on HVDC connections aiming at setting out clear and objective requirements for HVDC system owners, dc connected power park module owners, network operators and national regulatory authorities in order to contribute to non-discrimination, effective competition and the efficient functioning of the internal electricity market and to ensure system security [106].

ENTSO-E Network Code is mainly concerning the influence of HVDC system on its connected ac system. The HVDC system needs to fulfil the requirements referring the frequency and voltage stability, be capable of giving active and reactive power support and have the capability of fault ride through. Moreover, the ENTSO-E Network Code does not make a distinction between LCC and VSC technologies and not address dc fault level management, dc protection and control. Therefore, more work needs to be conducted on the development of dc grid codes.

2.3 DC fault handling approaches in multi-terminal HVDC grids

Fast and economical dc protection is one of the main obstacles for deployment of VSC MTDC grids, although a number of VSC HVDC links and multi-terminal MTDC networks have been commissioned or in planning [11], [107]-[109]. Effective dc protection methods need to be applied to minimise the impact from dc faults and ensure the secure operation of MTDC systems. There are three possible solutions to clear dc faults within MTDC networks: using ACCBs; using DCCBs and using fault blocking converters.

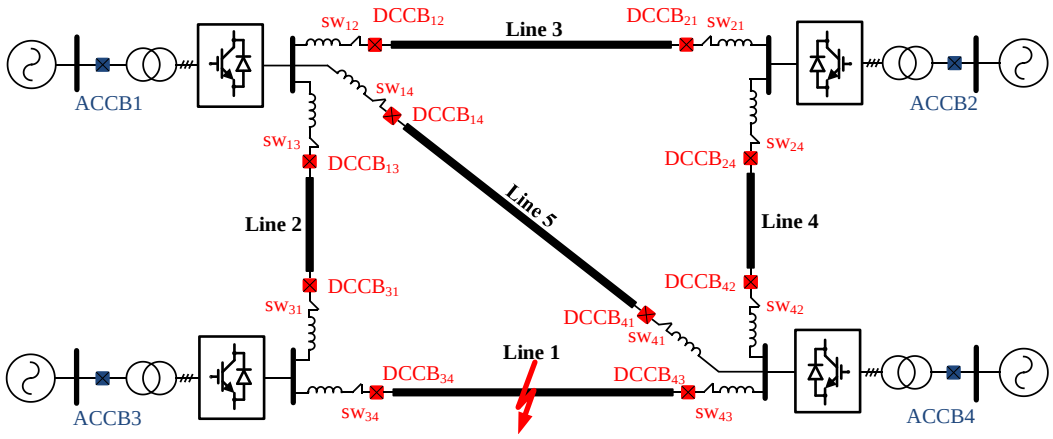


Fig. 2. 22. Schematic diagram of a 4-terminal dc grid equipped with ACCBs, DCCBs and fast dc switches.

2.3.1 Using ac circuit breakers

As illustrated in Fig. 2. 22, the high voltage ACCBs which are already equipped on the ac side of the converters can be one option to protect the dc grid. The so-called "Handshaking" method which employs ACCBs and fast dc switches has been proposed in [110]. In order to extinguish the dc fault currents, all converters need to be blocked once a dc fault is detected. Then ACCBs will be tripped. Fast dc switches are available at both ends of each line and are used to isolate the faulted line at zero current. The healthy circuits will be restored once the faulted line is isolated. A progressive fault isolation and grid restoration strategy using ACCBs are proposed in [111]. The strategy reduces the grid outage time through the progressive restoration of the dc grid.

The advantages of using ACCBs are that it is simple and economic. This greatly reduces the investment cost of building a large scale MTDC grid. However, the long fault isolation time (several hundred milliseconds) associated with this strategy will lead to the de-energisation of the entire dc grid [112]-[113]. This, in turn, may negatively impact the system operation.

2.3.2 Using dc circuit breakers

In a dc grid using DCCBs to provide fast clearance of a dc fault, two main solutions appear: one is to apply the same protection philosophy and principles used as the ac systems which can be called "Fully Selective Approach" [114] and the other is the "Open Grid" concept [115]-[116].

2.3.2.1 Fully Selective Approach

The fully selective approach considers the same philosophy and principles used in AC systems [114]. It means only those DCCBs associated with the faulted line will be tripped. Meanwhile, other breakers which are not located in range of the faulted line are not allowed to operate. For instance, in Fig. 2. 22, if a dc fault occurs in Line 1, only $DCCB_{34}$ and $DCCB_{43}$ will be tripped as long as the fault location is confirmed.

If fast fault clearance can be achieved by only isolating the faulted line, a blackout of the whole MTDC system will be avoided. The post-fault restoration of the fully selective method consists of restarting the converters which are blocked during the dc fault.

A clear advantage of the fully selective method is that only the faulted line will be isolated without expanding the blackout region. This way, the impact on the healthy circuit will be mitigated. However, this may impose a very high current interruption duty on those DCCBs, mainly due to the fault discrimination and location times.

2.3.2.2 "Open Grid"

In [115], an alternative dc fault isolation method, the "Open Grid" concept, has been proposed for the protection of MTDC grids. The "Open Grid" method reverses the normal protection sequence order. Each DCCB is allowed to autonomously trip following the detection of a fault without any delays associated with communications or discrimination logic. The re-closing of healthy circuits is based on residual voltages and currents.

Using this approach, the time used to discriminate and locate the fault is eliminated. Additionally, the current interruption duty is shared by different breakers. Thus, the DCCBs can open at a much lower fault current. Those DCCBs which cannot sense the fault will remain closed. Post-fault restoration is carried out by reclosing the DCCBs outside the faulted line based on the residual voltages and currents of the remaining circuits and by restarting the converters which have been blocked during the dc fault.

The "Open Grid" approach has the following drawbacks: the unpredictability of a tripping sequence and the possibility of expanding the blackout of the network.

2.3.3 Using fault blocking converters

As mentioned in Section 2.2.1.1, the converters, such as FB MMC, CSSM and AAC, have the capability of blocking ac infeeding currents by blocking the converters. Once all the converters within the MTDC grid are blocked, the dc fault currents will start to naturally decay to zero so that fast dc switches are able to operate to isolate the faulted circuit. The converters will be de-blocked once the faulted line is isolated and the dc grid will start to restore to a new steady state.

The FB MMCs are commercially available and they are beneficial for HVDC systems using OHLs [117]. The fault current blocking capability of AAC is illustrated in [38]. Based on the "Handshaking" method proposed in [110], fault locating and isolating schemes are proposed in [118] for FB MMC based MTDC grids. Some other dc fault ride-through methods of MMCs are summarised and reviewed in [119].

The higher capital costs and power losses of using fault blocking converters are the main drawbacks of employing this technology. Moreover, although the fault can be isolated without using DCCBs, the whole dc network will suffer an interruption of service and the associated ac system will be impacted as well [118]-[119].

2.4 Stability analysis of ac/dc grids subject to dc faults

Nowadays, most of the VSC HVDC projects are point-to-point connections, except several MTDC networks mentioned in Section 2.2.5. However, it is widely believed that with the development of VSC HVDC technology, large-scale ac/dc grids can be realised in the future [75]. Therefore, the stability of ac/dc systems is one critical aspect of system secure operation and needs to be studied.

In [120], a VSC MTDC grid is integrated with a multi-machine ac system. This paper provides methods of the study on the stability of an ac/dc transmission system and the dynamic interactions between ac and dc grids. Firstly, the modal analysis of this ac/dc system was performed. The root locus of the poles of the test system shows that the system is stable but with a poor damping capability. Secondly, the

dynamic interactions between the dc grid and its connected ac system were analysed. The influences of both ac and dc side faults on the overall ac/dc system were also discussed. The results show that the overall system can recover to a stable operating condition. However, the power angles between any two generators start to oscillate after the faults which shows the presence of the poorly damped but stable interarea modes.

Small-signal stability analysis of MTDC grid and its connected ac system has been presented in [121]. A 4-terminal VSC HVDC grid with the integration of two offshore wind farms was built to supply a load at the point of common coupling (PCC) of an ac grid. The impacts of VSC control parameters on the overall stability of the whole system were studied. The system is divided into smaller subsystems. Each of the subsystems is presented in state-space model. Then, the subsystem state-space models are integrated into a single model in order to represent the overall system. The dynamic performance of the system was presented in small and large perturbations. With the small-signal stability model, the controller parameters are improved, which will improve the stability of the system operation and control.

Damping subsynchronous resonance (SSR) in an ac system with VSC HVDC transmission system was performed in [122]. SSR is an electric power system condition where the electric network exchanges energy with a turbine generator at one or more of the natural frequencies of the combined system below the synchronous frequency of the system. A three-machine ac system representing the Great Britain transmission network with a VSC HVDC link is modelled in [122]. Primary and auxiliary controllers of the VSCs are designed. With the auxiliary controller, an anti-phase signal is injected into the ac system, the target resonant frequency will be damped. The design of the damping controller depends on the target resonant frequencies of different systems. The results in [122] show that the HVDC system will not influence the stability of the ac system. On the contrary, with proper design, the HVDC system improves the stability of the ac system.

The impact of different types of ac disturbances (faults) on the operation and control of an integrated ac/dc system was analysed in [123]. The studies were conducted in PSCAD time-domain simulation. A five-terminal MMC HVDC grid

replaces a congested area in the IEEE 39-bus (New England) test system. The modified test system forms a large-scale ac/dc system. The transient responses of the ac/dc grid to the ac side disturbances were investigated. The investigation results conclude that: the adverse effects of the ac side disturbances do not considerably propagate between different ac systems that are separated from each other by the MMC HVDC grid; the fast and effective controllers of the converters can provide nearly constant voltage support at the ac terminal of the converters during their ac side unbalanced faults and therefore improve the power quality and voltage stability.

The analysis and studies in the above literature did not consider the stability issues of ac/dc grids subject to dc faults. Faults in ac systems have a reduced impact on other parts of the network at locations far away from the fault [115]. Compared to ac systems, a dc network is a "low inertia" system. During a dc fault, the dc voltages will drop quickly in all terminals. Although IGBTs will be blocked by the local protection systems of the converters, currents from the ac side will feed to the fault through anti-parallel diodes (except for the cases where fault blocking converters are used). This is equivalent to a three-phase short-circuit on the ac side of a converter which may produce a severe impact on the ac grid.

In [124], the power generated by a single synchronous generator was transmitted through a transmission corridor which consists of an HVDC link and an HVAC transmission line. Based on this system, the ac system stability under dc link faults was studied. The equal area criterion was utilised to analyse the transient processes of the synchronous generator when the dc link subject to dc faults. The transient stability characteristics of three different MMC configurations, the HB MMC, CDSM MMC and hybrid LCC-MMC, were studied and compared. However, it only considered a single machine system. The stability of an ac/dc system which contains an MTDC grid and ac systems with multi-machine is still under-researched.

In an integrated ac/dc system, the dc grid may connect to ac systems at multiple locations (converters) and the ac system may contain multiple synchronous generators. From the viewpoint of the dc grid connected ac system, a fault within the dc grid can be seen as "multiple faults". If the dc fault cannot be isolated quickly and in a reliable manner, the dc fault will be continuously penetrating the adjacent

ac grids. This may lead to instability of the overall ac/dc system. Therefore, the transient behaviour and stability of the ac and dc grids during a dc fault need to be studied. Moreover, the impact of different dc fault clearance approaches on the stability of integrated ac/dc systems also requires consideration.

2.5 Analysis and protection of converter ac side faults

Converter ac side faults are important aspects in the operation of MMC-HVDC systems and thus have received significant attention in the literature. Fig. 2. 23 depicts the possible types of converter ac side faults. Faults F1 to F5 are between the converter and the transformer. Faults F6 to F10 are at grid side. The categories of the ac faults are summarised in Table 2. 3.

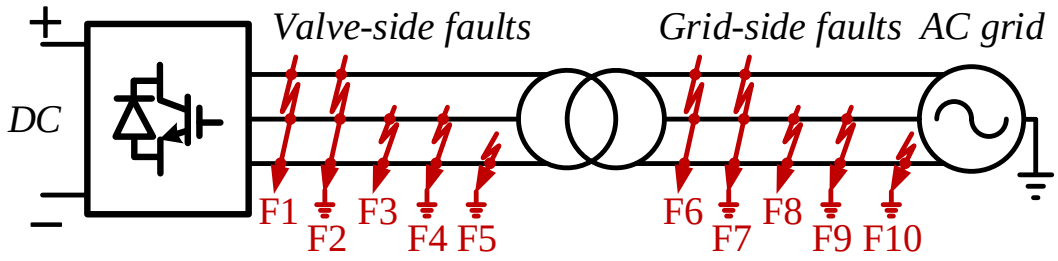


Fig. 2. 23. Schematic diagram of converter ac side faults.

Table 2. 3. AC fault categories

Faults	Schematic diagrams
Three-phase short-circuit	
Three-phase-to-ground	
Two-phase short-circuit	
Two-phase-to-ground	
Single-phase-to-ground	

It is known that, in three-phase systems, balanced faults might cause more severe consequences than unbalanced faults. However, unbalanced faults, especially

single-phase faults, are more common than three-phase faults. Therefore, there are a number of studies undertaken on converter grid-side unbalanced fault.

According to the analysis in [16]-[23], converter grid-side single-phase fault (see F10 in Fig. 2. 23) will result in double-frequency harmonics in dc voltage, and therefore, cause dc voltage oscillations. The power delivered to the ac grid will be affected as well. Positive and negative damping controllers have been proposed in [21]-[23] for MMCs under grid-side unbalanced ac conditions. The proposed controllers performed well in solving the above issues. Although there are studies on converter grid-side unbalanced conditions, MMC station internal unbalanced ac faults remain an under-researched topic.

In both LCC and MMC stations, the converter transformers are typically deployed outside the halls housing the converters. For instance, Fig. 2. 24 shows the MMC station of the INELFE link. There are switchgears and converter grounding devices (Starpoint reactors) between the wall bushings and the power transformers. This area is in the overlapping protective zone of the converter and the transformer needs high insulation to withstand high voltages and large currents. Therefore, valve-side SPG faults occur in this area might lead to severe consequences, such as commutation failures in LCCs, dc voltage oscillations in symmetrical monopole MMCs, and non-zero-crossing fault currents in bipole MMCs [29]-[30], [127]

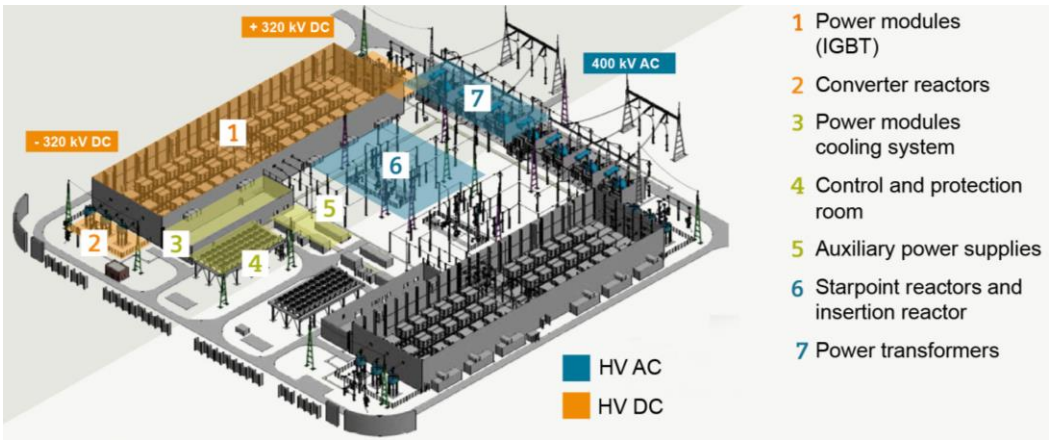


Fig. 2. 24. The schematic diagram of the VSC station of the INELFE link [125].

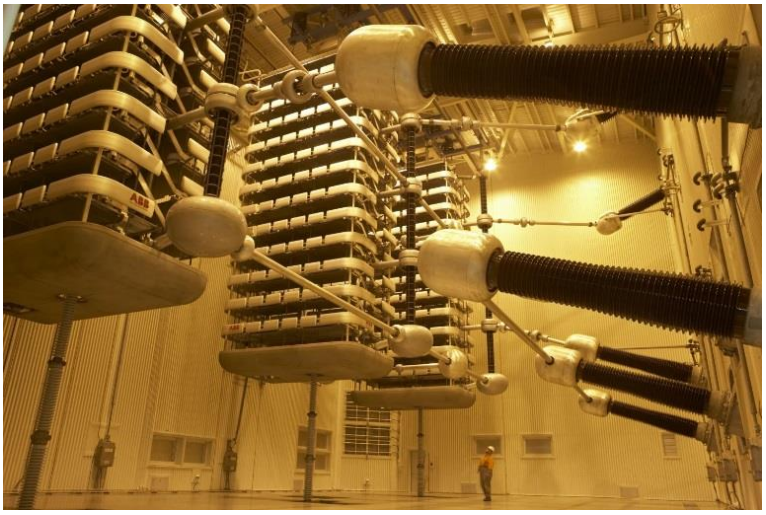


Fig. 2. 25. LCC transformer wall bushings inside the valve hall [126].

Moreover, as shown in Fig. 2. 25, the LCC's valve-side winding bushings of these power transformers protrude through the hall wall to connect to converter ac buses [24]-[25]. Insulation failure and flashover of wall bushings may cause an internal single-phase-to-ground (SPG) fault between the converter and the transformer. Both LCCs and VSCs have experienced these faults in practical installations [26]-[27], [128].

In [27] and [128], the characteristics of valve-side SPG faults in LCCs were analysed and possible solutions using a phase selection strategy and zero-sequence voltage compensation were proposed. However, these cannot be applied to MMCs due to the differences between converter topologies. Internal ac bus faults in two-level VSCs were investigated in [77]-[78], but their findings are not totally applicable to MMCs either. MMC station internal ac faults were studied in [28], [129], however, the work was restricted to symmetrical monopole configurations. In addition, the simplified lumped parameter line models used in these references hardly reflect real fault characteristics.

Valve-side SPG faults also induce special fault behaviours in asymmetrical monopole HB-MMCs. An initial study was performed in [26], where solutions to the overvoltage arising in upper arm SM capacitors were proposed. However, this type of fault also produces high dc components in the ac side fault currents which may prevent grid-side ACCB from operating due to the absence of zero-crossings. References [29]-[30] propose installing an auxiliary ACCB on the grid side to

create the required current zero-crossings, but no further insight into the presence of the dc offsets is provided. Moreover, a shortcoming of this approach is that the three-phase short-circuit created by the additional ACCB will lead to severe voltage drops at the ac grid, and therefore may aggravate the fault impact. In addition, the installation of an auxiliary ACCB will increase capital costs.

Given that an asymmetrical monopole MMC HVDC link is the building block of bipole systems, these will inherit its drawbacks. Although [130] analyses the non-zero-crossing fault currents caused by valve-side SPG faults in a bipole system, the faulted phase reactance has been ignored and, as such, the fault current calculation accuracy is reduced. Additionally, the protection strategy is complex, and the three-phase short-circuit created during the fault may burn the semiconductor devices. Moreover, the converter transformer and other equipment may be damaged by the large currents arising from closing the auxiliary arm protection switches. A hybrid MMC topology based on HB and FB SMs has been used in [127] to address the above issues. However, the adoption of such a configuration would greatly increase capital costs due to the additional IGBTs and hence increased power losses.

The study of HB MMCs subject to station internal faults is currently under-researched both in the industry and academia. To bridge this gap, theoretical analysis of SPG fault characteristics at the valve-side of HB MMC based transmission systems under various station configurations needs to be carried out. Protection strategies should be proposed based on the theoretical studies.

2.6 Summary

The state-of-the-art of VSC HVDC technologies is reviewed in this chapter. It can be seen that the VSC HVDC technologies are widely applied in renewable energy integration, long distance and bulk power transmission and grid interconnections. However, there are still problems that the future VSC HVDC systems need to cope with. For instance, the design and manufacture of fast and reliable DCCBs, HVDC cables, converting ac lines into dc operation and dc gird protections.

Moreover, due to the low impedance of the dc network, a dc fault within a dc grid might severely affect the operation of the dc grid and its connected ac systems.

Therefore, the impact of dc grid faults and different dc fault protection approaches on the stability of integrated ac/dc systems need to be studied.

The study on the protection of converter ac side fault is another important aspect. Particularly, more attention is necessary to be paid to converter valve-side single-phase faults which is an under-researched topic.

The research work in this thesis investigated the above problems and propose relevant solutions.

Chapter 3

Application of DCCB in DC Grids

3.1 Introduction

As the hybrid DCCB (HCB) possesses a fast fault current interruption speed and produces low steady-state power losses, HCB has been widely considered as the most common DCCB design topology for HVDC applications [131]. As discussed in Section 2.2.3, the studies in the literature were mainly focussed on the topology design of DCCBs. More research needs to be carried out on investigating the operating characteristics and system behaviour of DCCBs. The experimental validation of the application of DCCBs in dc grids is also necessary to verify the performance of DCCBs.

In this chapter, the voltage and current characteristics and the response time of the HCB are first investigated in simulations. The factors, such as parameters of the current limiting reactor and the surge arrester, affecting the performance of the HCB are considered in the studies. Moreover, the design of DCCBs using metal–oxide–semiconductor field-effect transistors (MOSFETs) to emulate the HCB is described. Finally, the DCCBs was deployed in a three-terminal VSC HVDC test-rig for the test of interrupting dc fault currents in a dc grid.

3.2 Operating characteristics of hybrid dc circuit breakers

Although various HCBs have been proposed by both industry and academia, the operating principles of those HCBs are similar. Therefore, the HCB proposed in [13] is used to investigate the operating characteristics of HCBs. The factors affecting the fault behaviours of the HCB are studied.

3.2.1 Operating principles

A test model, as shown in Fig. 3. 1, has been built in PSCAD/EMTDC. The HCB is built according to [13]. A dc voltage source with an internal resistor R_s is used to produce the dc voltage. R_{dc} and L_{dc} is the equivalent resistance and inductance (R: 0.0192 Ω/km and L: 0.24 mH/km [5]) of a 200 km XLPE cable. R_{Load} is the dc load. The residual current breaker is to isolate the faulty line from the healthy circuits after fault clearance.

The voltage V_{dccb} across the HCB, the total current passing through the HCB, the currents in each branch of the HCB and the terminal voltage V_{dc} are the

measurements. The value of the current limiting reactor and the rated voltage of the surge arrester are changed to investigate the influences on the fault current interrupting performance. Parameters of the test circuit are given in Table 3. 1.

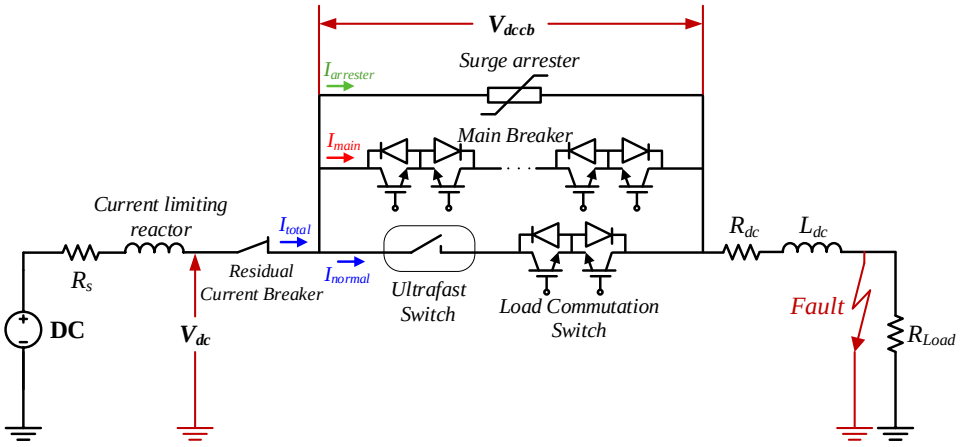


Fig. 3. 1. The test circuit of a typical HCB.

Table 3. 1. Parameters of the DCCB test circuit.

Parameters	Real value	In per unit
DC source voltage (kV)	320	1 p.u.
L_{dc} (H)	0.048	-
R_{dc} (Ω)	3.84	0.012 p.u.
DC load R_{Load} (Ω)	320	1 p.u.
DC source internal resistance R_s (Ω)	0.1	0.00003 p.u.
Surge arrester clamping voltage (kV)	384 (variable)	1.2 p.u.
Current limiting reactor (mH)	100 (variable)	-

The algorithm of the fault discrimination is shown in Fig. 3. 2. The tripping signals will be generated once the current I_{total} reaches 5 kA. The tripping signals will be directly sent to the load commutation switch (LCS) and the main breaker. The ultrafast switch (UFS) will open at zero current and voltage once the fault current totally commutates into the main breaker. Therefore, the UFS can open without interrupting arcs, which allows the UFS to open at a fast speed (1-2 ms) [13]. In this test, a time delay of 2 ms, which emulates the operating time of the UFS, is applied to the tripping signal sent to the UFS.

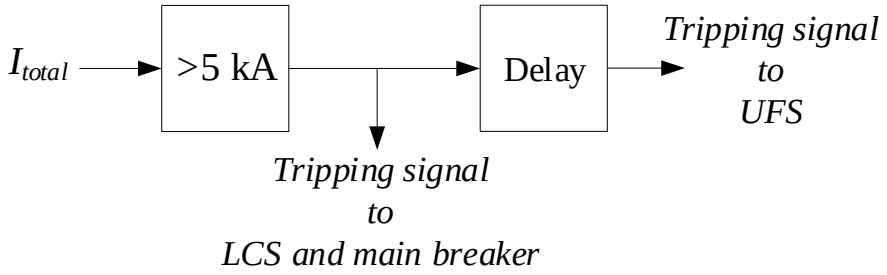


Fig. 3. 2. The algorithm of fault discrimination.

The sequence of the fault current interruption process is as follows:

(i) A solid fault is triggered at t = 0.1 s;

(ii) The LCS will be turned off and the main breaker will be turned on simultaneously once their tripping signals are received;

(iii) The fault current in the normal operation branch will start to commutate into the main breaker;

(iv) The UFS will be turned off 2 ms after receiving the tripping signal;

(v) The main breaker will be blocked once the UFS is fully opened;

(vi) The fault current will be forced into the surge arrester where it will be totally dissipated;

(vii) The residual breaker will open once the fault current decays to zero.

It should be mentioned that the test focuses on the system level dynamic responses of the DCCB, thus the test does consider the time delay of turning on the LCS and the main breaker. Moreover, the current commutation process is not considered.

The currents and voltages of the HCB during the dc fault are shown in Fig. 3. 3(a)-Fig. 3. 3(b). Fig. 3. 3(c)-Fig. 3. 3(f) show the status (1 is on and 0 is off) of different switches. It can be seen from Fig. 3. 3(a) that the current before the fault was 1 kA and it started to increase once the fault occurred. The LCS was turned off and the main breaker was turned on simultaneously once the fault current reached 5 kA. The fault current kept increasing to 9 kA until the UFS was turned off. The main breaker was turned off once the UFS was fully opened. Then the fault current

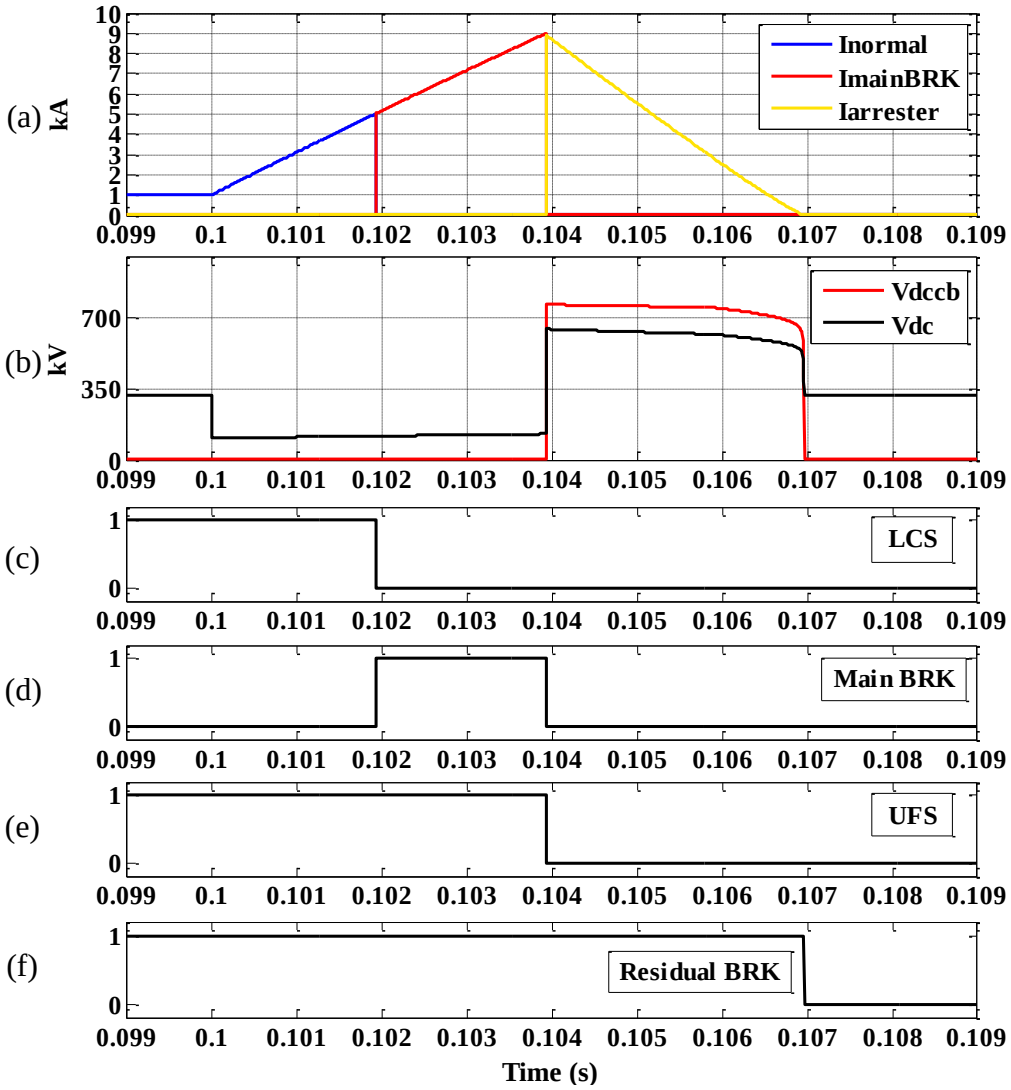


Fig. 3. 3. The fault responses and operating status of different switches of the HCB. (a) Currents in the three branches; (b) Voltage over the HCB and the dc terminal voltage; (c)-(f) Operating status of the LCS, main breaker, the UFS and the residual current breaker.

was forced into the surge arrester where the fault current was totally dissipated. In this test circuit, the fault current is fully interrupted within 6.9 ms.

Fig. 3. 3(b) illustrates the voltage across the HCB and the dc voltage at the dc terminal. The dc voltage V_{dc} dropped to 102 kV immediately when the fault occurred. V_{dc} did not drop to zero because the high rate-of-change of the fault current led to transient voltages on both current limiting reactor and the dc line reactor. The voltage V_{dccb} over the HCB was zero before the main breaker was turned off. The surge arrester produced a large transient overvoltage when the main breaker was blocked. The overvoltage disappeared once the fault current was dissipated.

3.2.2 Factors affecting the operation of hybrid dc circuit breakers

In order to investigate the factors affecting the performance of the HCB, the parameters of the current limiting reactor and the surge arrester are varied. The base case is the test system in the above section where the current limiting reactor is 100 mH and the rated voltage of the surge arrester is 384 kV (1.2 times of the dc voltage). The HCB currents with different parameter values of current limiting reactors and surge arrester rated voltage are shown in Fig. 3. 4.

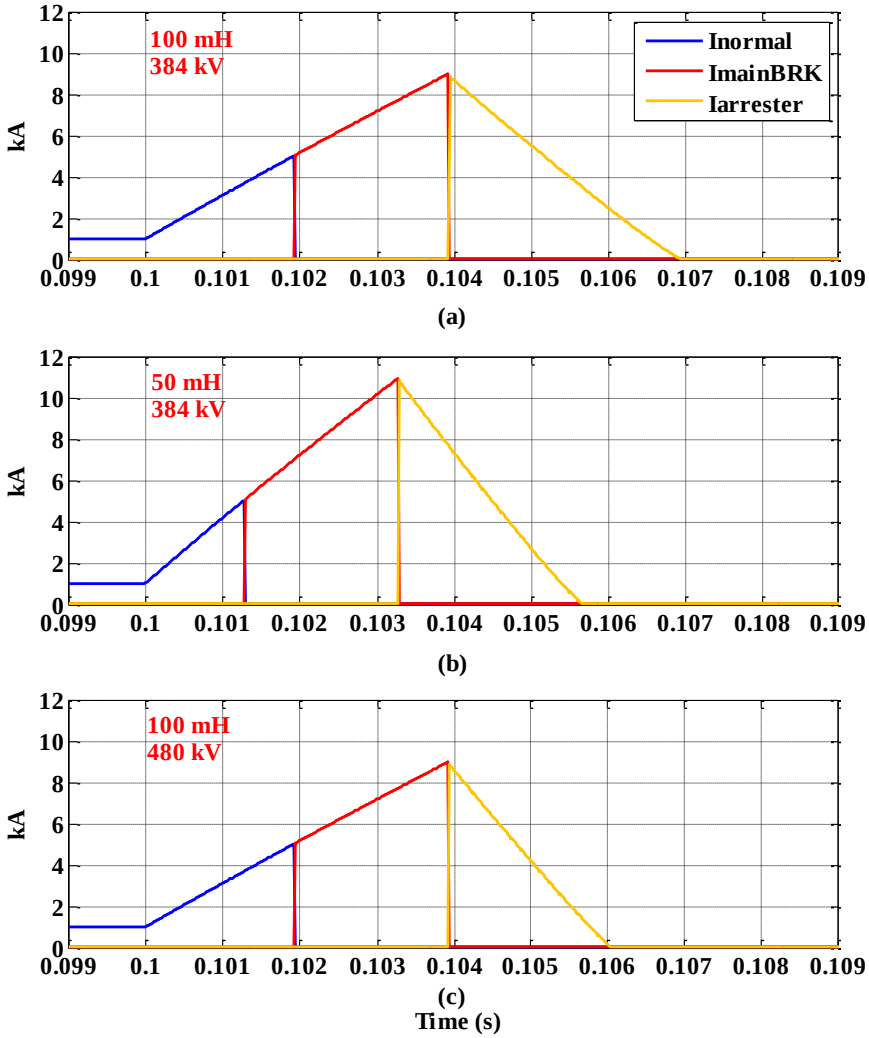


Fig. 3. 4. The current behaviours under different parameters of the current limiting reactor and the surge arrester.
(a) The reactor is 100 mH and the surge arrester clamping voltage is 384 kV; (b) The reactor is 50 mH and the surge arrester clamping voltage is 384 kV; (c) The reactor is 100 mH and the surge arrester clamping voltage is 480 kV.

It can be seen from the comparison of Fig. 3. 4(a) and Fig. 3. 4(b), a smaller reactor led to a larger current rate-of-change. The fault current in the case with a

smaller reactor reaches the threshold faster than the case with a larger reactor. Therefore, the LCS and the main breaker in the case with a 50 mH reactor were turned off earlier than the base case. The fault current has reached 11 kA in the case with a 50 mH reactor when the UFS was turned off. The fault current was dissipated by the surge arrester within 1.6 ms which is faster than the base case. It means that, with the same rated voltage of the surge arrester, a larger fault current will lead to a faster dissipation process.

It can be found from the comparison of Fig. 3. 4(a) and Fig. 3. 4(c) that in the case of a higher surge arrester clamping voltage, the time of the fault current being dissipated in the surge arrester is 2 ms which less than the case with a lower surge arrestor clamping voltage. It means that, a higher surge arrestor clamping voltage will lead to a faster dissipation process.

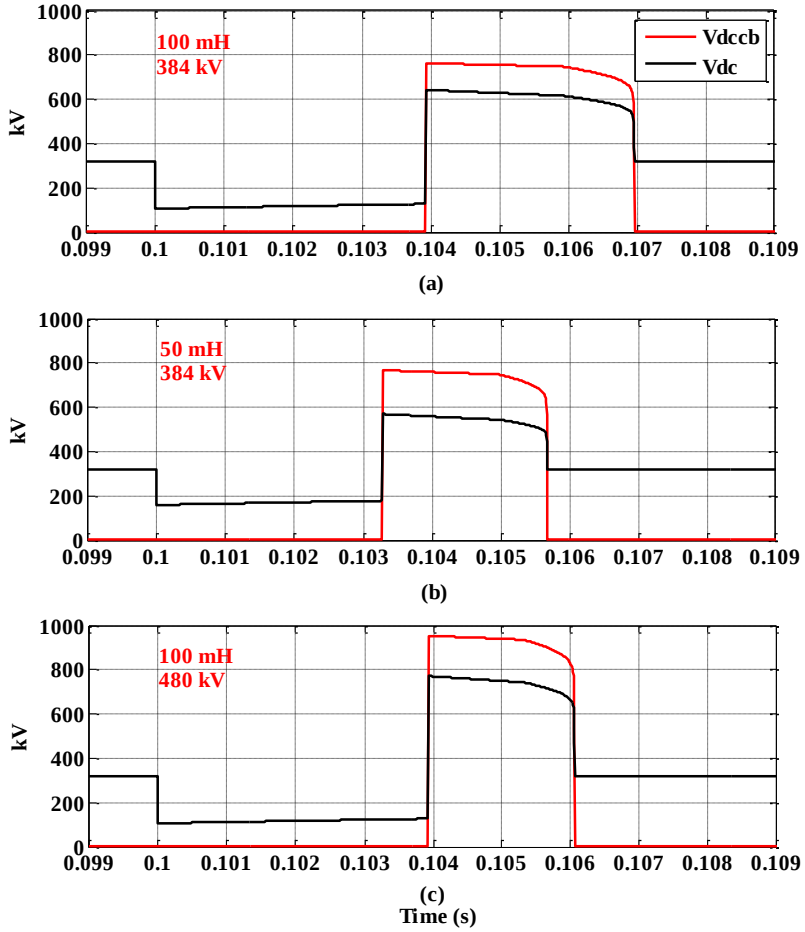


Fig. 3. 5. The voltage behaviours under different parameters of the current limiting reactor and the surge arrester.
(a) The reactor is 100 mH and the surge arrester clamping voltage is 384 kV; (b) The reactor is 50 mH and the surge arrester clamping voltage is 384 kV; (c) The reactor is 100 mH and the surge arrester clamping voltage is 480 kV.

Fig. 3. 5 shows the voltage across the HCB and the dc terminal voltage. The voltage across the HCB depends on the non-linear characteristic of the surge arrester. The comparison between Fig. 3. 5(a) and Fig. 3. 5 (b) shows that the same clamping voltage gives the same overvoltage. However, a higher current through the arrester gives a shorter dissipation time.

It can be observed from the comparison of Fig. 3. 5(a) and Fig. 3. 5(c) that a higher surge arrester clamping voltage leads to a higher overvoltage. Moreover, the surge arrester with a higher clamping voltage reduces the time of the fault current being dissipated.

From the simulations, it can be concluded that the current limiting reactor and rated voltage of the surge arrester affect the characteristics of the voltage and current of the HCB. The rate-of-change of the fault current was limited by the current limiting reactor. However, it should be highlighted that a large reactor may increase the time constant of a dc system; which will affect the system dynamic response and, in the worst case, may cause instability. A high rated voltage of the surge arrester can reduce the current dissipation time in the surge arrester. However, the overvoltage produced by the surge arrester will be high. The insulations of the HCB connected devices may be damaged by this overvoltage. Therefore, the design of HCBs requires to be assessed comprehensively both at device and system levels.

3.3 Experimental validation of applying dc circuit breakers in multi-terminal dc grids

The above studies show that the rate-of-change of dc fault currents is quite high (several kiloamperes per milliseconds) due to the small impedance of dc circuits. DCCBs are required to interrupt fault currents within several milliseconds. The characteristics of fault currents and voltages of the HCB have been studied through time-domain simulations. To investigate the performance of using DCCBs to isolate dc faults in a dc grid, scale-down physical models of solid-state CB have been built and implemented in a three-terminal VSC HVDC test-rig to isolate dc faults. The studies mainly focus on system behaviour instead of DCCB's internal performance.

3.3.1 Small-scale dc circuit breaker design

Solid-state circuit breakers were built and installed in a VSC HVDC test-rig to emulate the fault isolation process in a dc grid. The schematic diagram of the small-scale DCCB is shown in Fig. 3. 6.

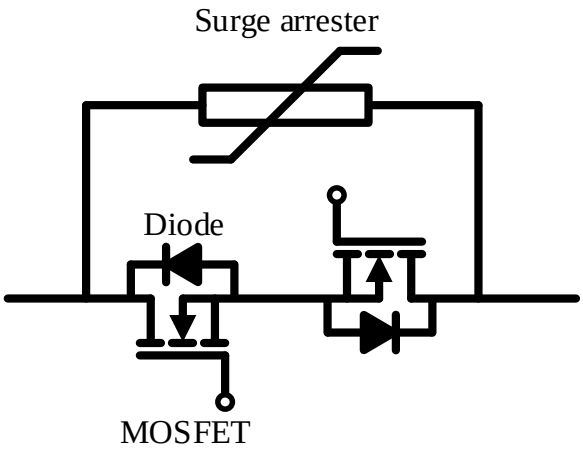


Fig. 3. 6. Schematic diagram of the small-scale DCCB.

MOSFETs are used to build the main breaker. To protect the MOSFETs, diodes are installed in parallel with them. In each DCCB, the MOSFETs are anti-series connected in order to interrupt bidirectional fault currents. The performance of the designed DCCBs is accurate enough to investigate the system behaviour of dc faults and the system dynamic responses in a dc grid. A surge arrester is equipped in parallel with the main breaker branch to dissipate the energy from the fault current once the breaker is turned off. The parameters of the DCCB are given in Table 3. 2.

Table 3. 2. Parameters of the small-scale DCCB.

Parameters	Values
Rated current (A)	20
Rated dc voltage (V)	800
Surge arrester clamping voltage (V)	170

Fig. 3. 7 shows the printed circuit board (PCB) of the small-scale DCCB. The MOSFETs are individually controlled via non-bootstrapped opto-coupler based drivers. The state of each DCCB is set using dSPACE.

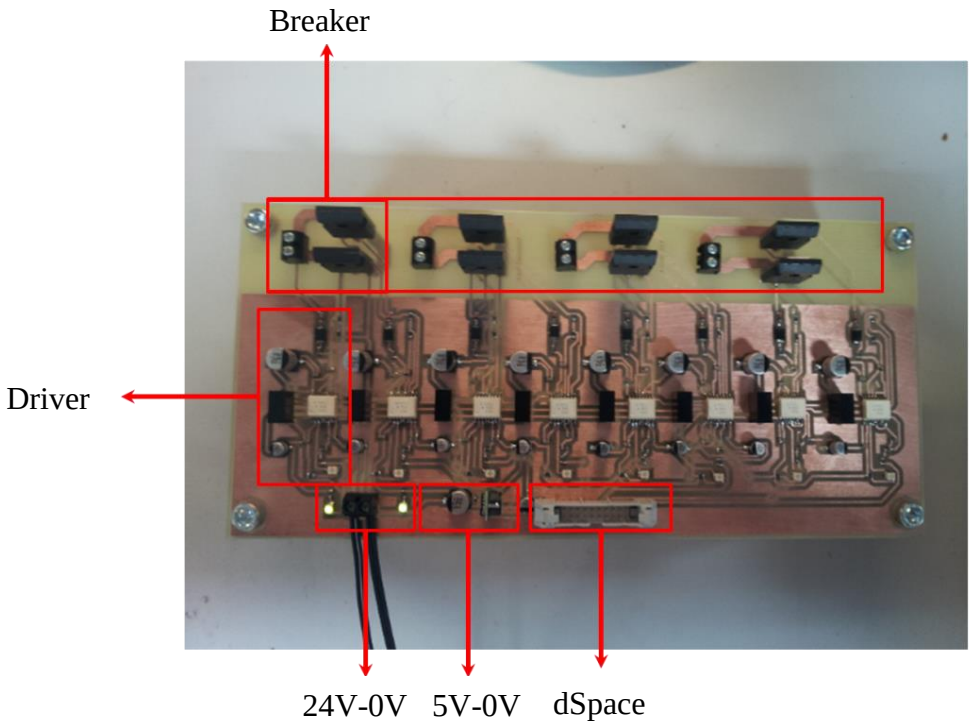


Fig. 3. 7. The DCCB board.

3.3.2 VSC HVDC test-rig

The test-rig consists of three 10 kW two-level VSCs, dc lines and a dSPACE controller. Fig. 3. 8 shows the setup of the test-rig. The arrangement of these devices in the lab is depicted in Fig. 3. 9. In the dc side, a delta connection (meshed network) is formed. At the ac side, the three VSCs are connected to the same ac grid. The four DCCBs are deployed in the two ends of the dc line between VSC1 and VSC2. The parameters of the test-rig are listed in Table 3. 3.

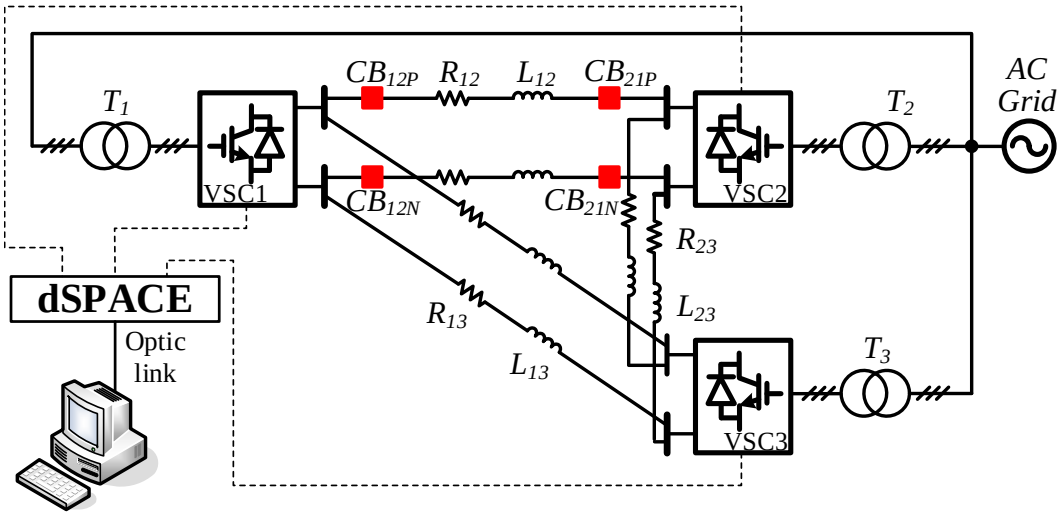


Fig. 3. 8. The set-up of the VSC HVDC test-rig.

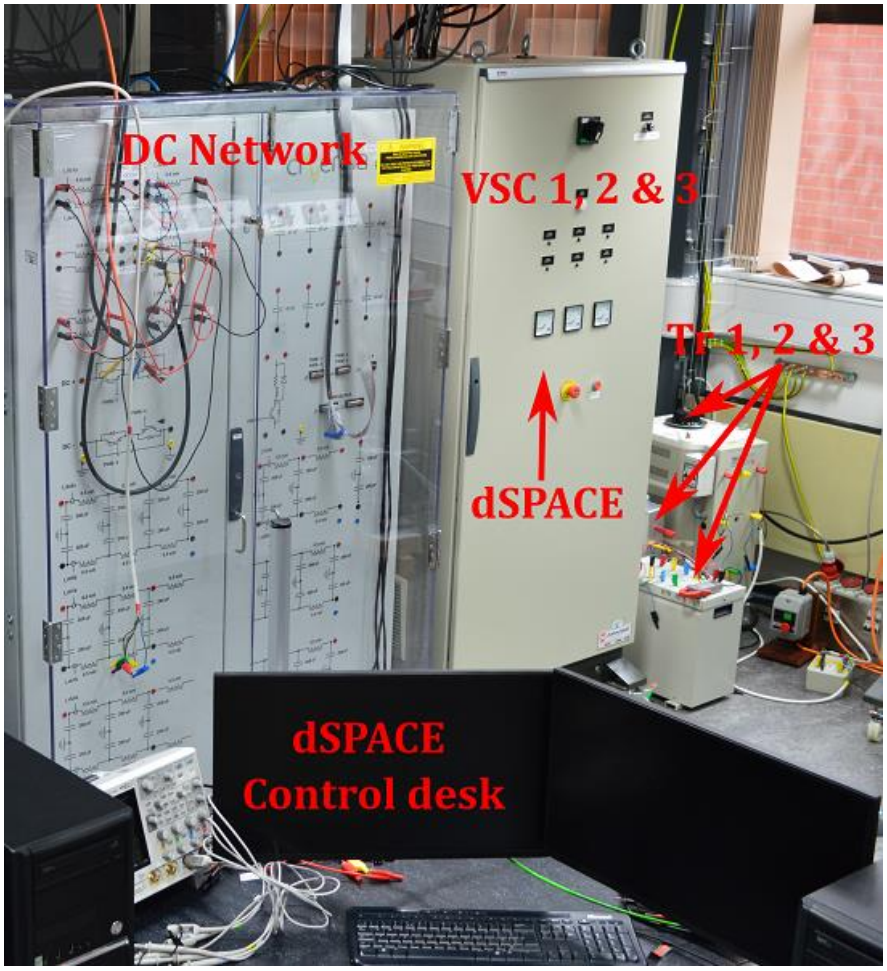


Fig. 3. 9. The arrangement of the test-rig in the lab.

Table 3. 3. Specifications and parameters of the test-rig.

Devices	**Specifications**	**Equipment ratings**	**Operating rating**
Converters	Rated power	10 kW	2 kW
	Rated ac voltage	415 V	145 V
	Rated dc voltage	800 V	250 V
	Topology	Two-level	
AC inductors	L_{g1}, L_{g2}, L_{g3}	2.2 mH	
DC lines	L_{12}	2.4 mH	
	L_{13}	5.8 mH	
	L_{23}	11.8 mH	
	Equivalent resistance R_{12}	0.045 Ω	
	Equivalent resistance R_{13}	0.68 Ω	
	Equivalent resistance R_{23}	0.18 Ω	
DC capacitors	C_{g1}, C_{g2}, C_{g3}	1020 µF	
Control system	dSPACE / ControlDesk (Simulink interface)		

The master-slave control scheme is utilised to control the VSCs. The control blocks of the dc voltage and reactive power (V_{dc} and Q) control scheme and the active and reactive power (P and Q) control scheme are depicted in Fig. 3. 10 and Fig. 3. 11. VSC1 controls the dc voltage. VSC2 and VSC3 control the power.

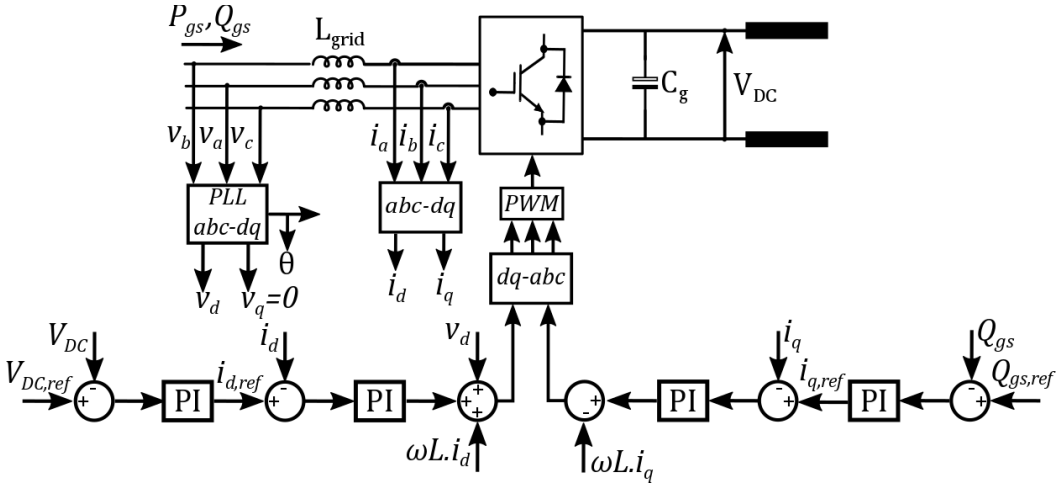


Fig. 3. 10. V_{dc} and reactive power control scheme.

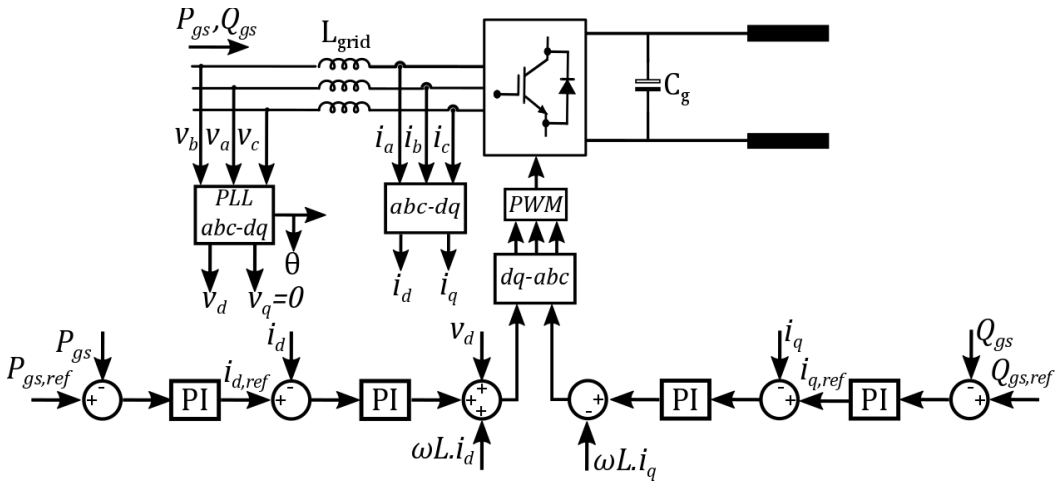
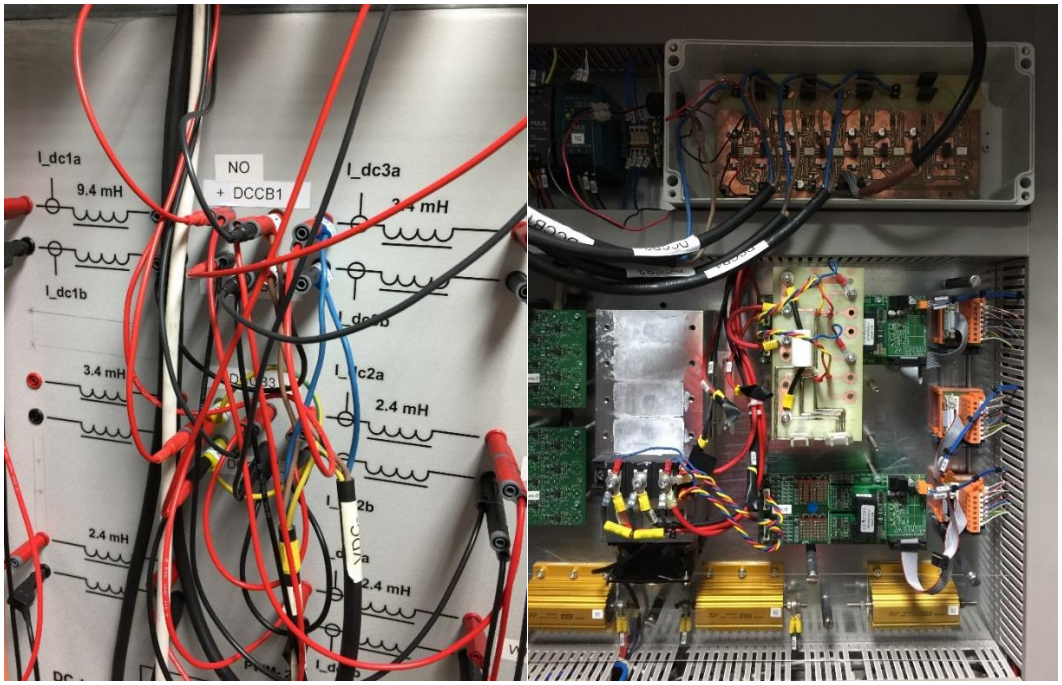


Fig. 3. 11. Active and reactive power control scheme.

Fig. 3. 12 shows the deployment of the DCCBs in the dc network cabinet. The DCCB board shown in Fig. 3. 7 is installed inside the cabinet. The topology of the dc network and locations of the DCCBs within the dc network can be changed outside the cabinet.



(a) External. (b) Internal

Fig. 3. 12. Deployment of DCCBs.

Table 3. 4. Parameters of the dc fault generator.

Parameters	Values
Rated current (A)	30
Rated voltage (V)	900
Resistor R (Ω)	14
Reactor L (mH)	45

A dc short-circuit generator (SCG) is employed to produce dc faults within the dc circuit. The SCG, shown in Fig. 3. 13, consists of a series connected resistor and an inductor. In order to ensure the safety of the devices, the fault current is limited by the size of the resistance and the inductance. The SCG is deployed in the dc line between VSC1 and VSC2. The SCG is closed to the CB_{21P} and CB_{21N}. A pole-to-pole fault will be produced once the IGBT inside the SCG is triggered. The currents I_{12}, I_{13} and I_{23} of the positive poles are measured, as shown in Fig. 3. 13.

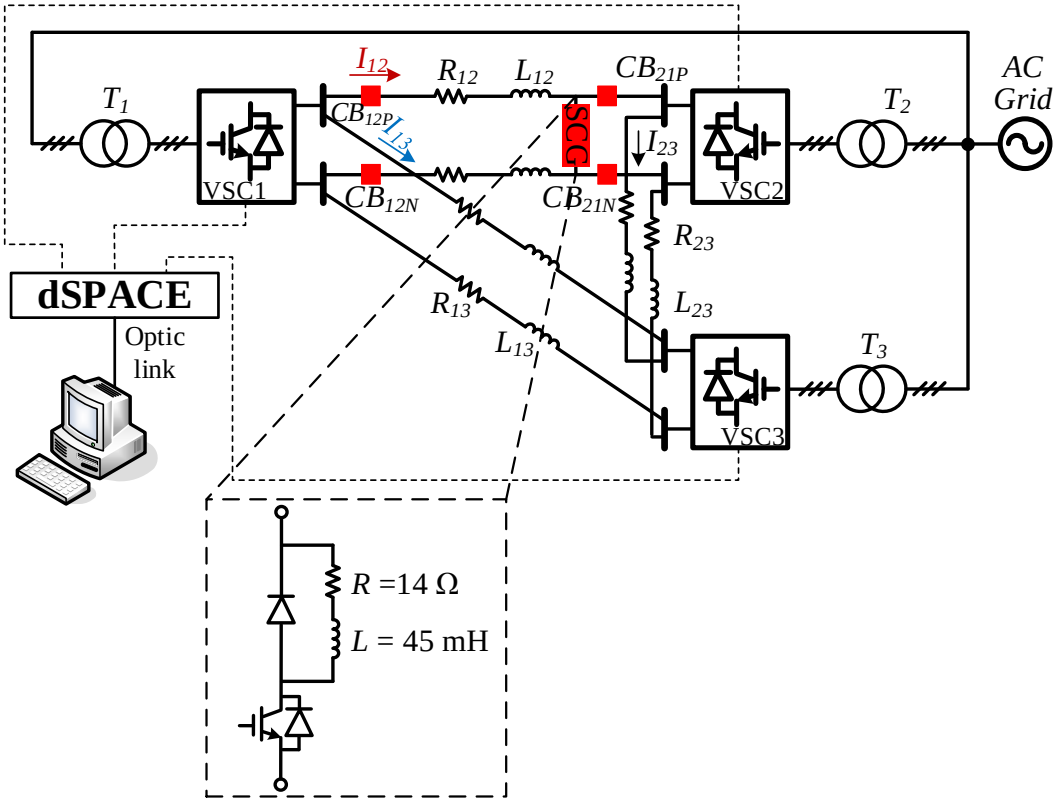


Fig. 3. 13. Short-circuit generator.

3.3.3 Experimental results

A pole-to-pole fault was triggered at t = 2 s. Due to the reactor within the SCG, the rate-of-change of the fault current is not high. Also, in order to guarantee the safety of the devices and system operator, a conservative threshold of triggering the DCCBs is set. The DCCBs will be turned off once the magnitude of the dc current is above 1.2 p.u. As shown in Table 3. 3, the operating power and voltage of the VSC is 2 kW and 250 V. Therefore, the maximum operating current is 8 A. In this way, the DCCBs are set to be turned off once the current is above 9.6 A. Moreover, as the fault currents have been limited to safe levels, the converters will not be blocked during the fault test.

The currents I_{12}, I_{13} and I_{23} in the positive pole of the dc network are shown in Fig. 3. 14. The dc currents contain distortions due to the harmonics and noise produced by the circuit. Before the fault, the current through the CB_{21P} was about 2 A. The CB_{21P} and CB_{21N} were turned off immediately once the current I_{12} increased to 9.6 A. The fault current through the CB_{21P} decayed from 9.6 A to zero within 6 ms. Then, the faulted line was successfully isolated.

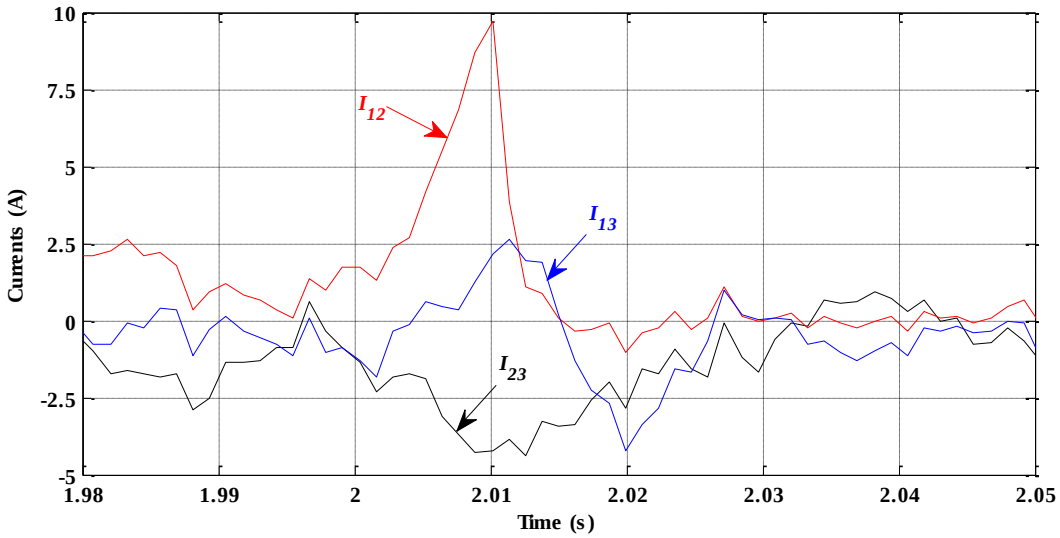


Fig. 3. 14. Positive pole dc currents.

Fig. 3. 15 depicts the voltages across the breakers CB_{21P} and CB_{21N}. In normal operation, the voltage across a DCCB is caused by the on-state resistance which is a small value. The voltage over the DCCBs increased to quite high values once the DCCBs were turned off. At the same time, the fault current was commutated to the surge arrester and started to decrease. The fault current in the surge arrester established a counter voltage [13], and this voltage reduced the fault current to zero by dissipating the energy stored in the reactor of the dc line. It should be noted that as the measurements of the DCCB voltages were from the oscillograph, the time axis shown in Fig. 3. 15 is different from the time period in the control system.

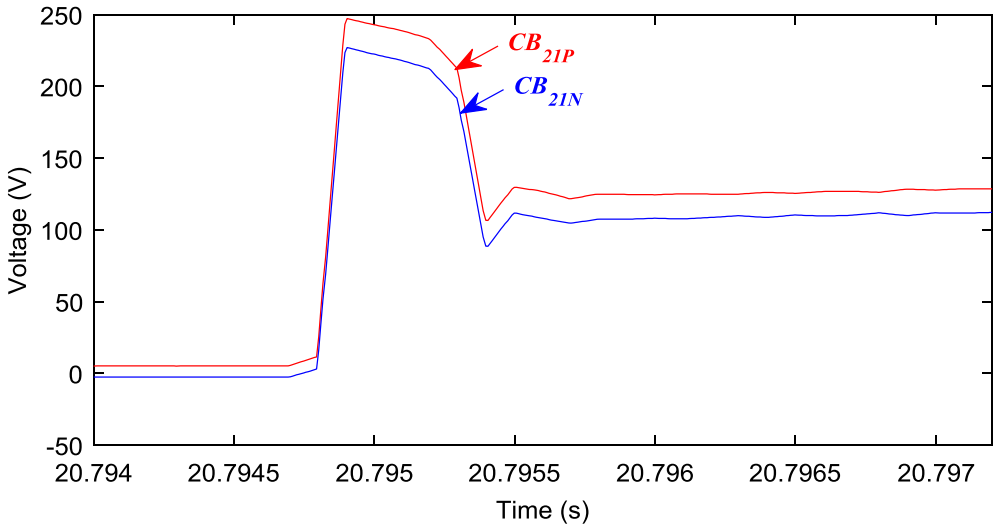


Fig. 3. 15. Voltages across the DCCBs.

The dc terminal voltages of each VSC are illustrated in Fig. 3. 16. It can be seen that the dc voltages dropped immediately when the fault occurred. However, the dc voltage started to recover once the faulted line was isolated. The voltages experienced oscillations during the recovery period. The system became stable 0.5 s after isolating the fault.

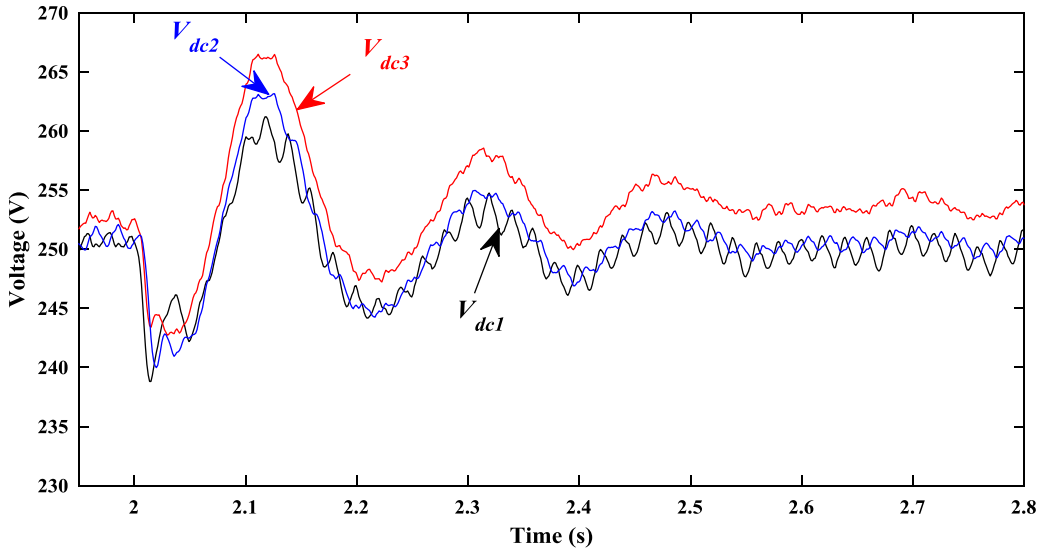


Fig. 3. 16. VSC dc terminal voltages.

Fig. 3. 17 shows the grid side ac voltages of the VSCs. The grid side voltages are not affected seriously. The reason is that the dc fault was not severe due to the limitation of the fault impedance, and the fault was quickly isolated by the DCCBs.

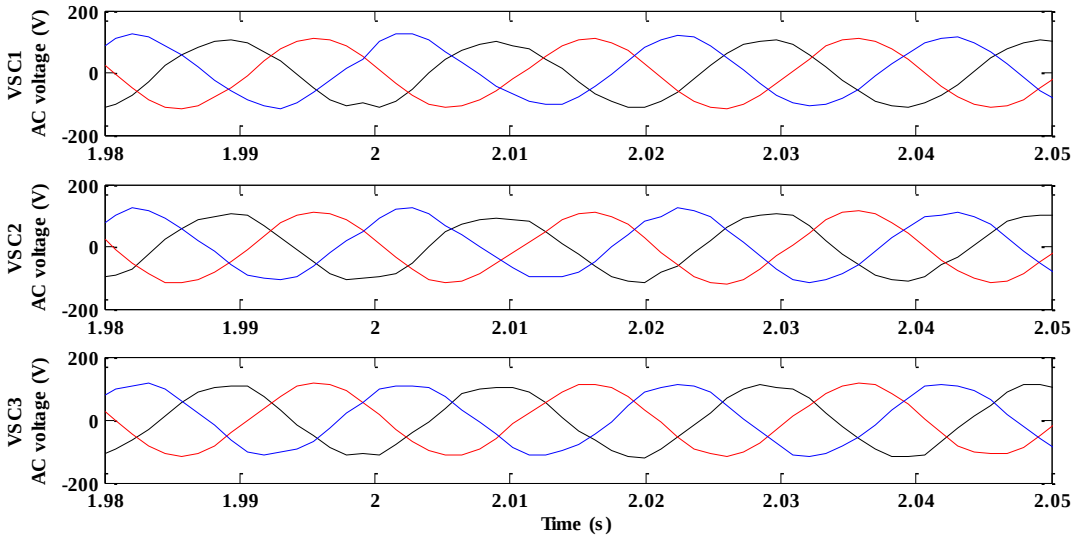


Fig. 3. 17. Converter ac side voltages.

3.4 Summary

In this chapter, the principle and operating characteristics of the HCB were analysed through a test circuit built in PSCAD/EMTDC. The voltage, current and response time of the HCB were analysed.

By changing the parameters of the current limiting reactor and the rated voltage of the surge arrester, the factors that affect the performance of the HCB were investigated. The studies show that the current limiting reactor limits the rate-of-change of the fault current, and the surge arrester affects the overvoltage on the breaker and the current dissipation time once the main breaker is blocked. However, a large reactor increases the time constant of the system, and therefore, affects the system dynamic performance. Also, the energy stored in a large reactor might pose a burden on the surge arrester to absorb a large amount of energy. Therefore, the application of DCCBs needs to be properly designed based on the actual conditions.

The studies of dc fault characteristics in time-domain were demonstrated through the experiment on a VSC HVDC test-rig. The system behaviour of isolating a dc fault in a dc grid was also studied. The experimental results show that DCCBs successfully interrupted the dc fault currents and isolated the faulted line.

Chapter 4

Dynamic Interactions of AC and DC Grids subject to DC Faults

4.1 Introduction

The development of an interconnected market will facilitate cross-border exchanges in electricity. The role of HVDC in integrating renewable energy generation and cross-border electricity exchanges is widely recognised. Proposals of using dc grids linking the transmission systems of different countries and renewable generation are being promoted. As mentioned in Section 2.3, the fault current interruption and protection technologies are still obstacles for the development of MTDC grids. The impact of utilising different dc grid protection approaches on the dynamic interactions of integrated ac/dc grids subject to dc faults are still under-researched.

In this chapter, the impact of dc faults on ac and dc grids are studied. Various dc grid protection approaches are compared and evaluated. Fault currents, ac voltages, power angles, system restoration time and interruption of power supply are key quantities which are used to evaluate the performance of ac grids during dc faults.

4.2 Test system modelling

An integrated ac/dc power transmission system, as shown in Fig. 4. 1, has been developed in PSCAD/EMTDC. The system consists of a 4-terminal meshed HVDC grid and a modified 4-machine two-area ac system. The parameters of the ac system have been taken from [132]. Each generator has been modelled to include an exciter, a turbine and a governor. The dc grid connects to the ac system via two ac buses.

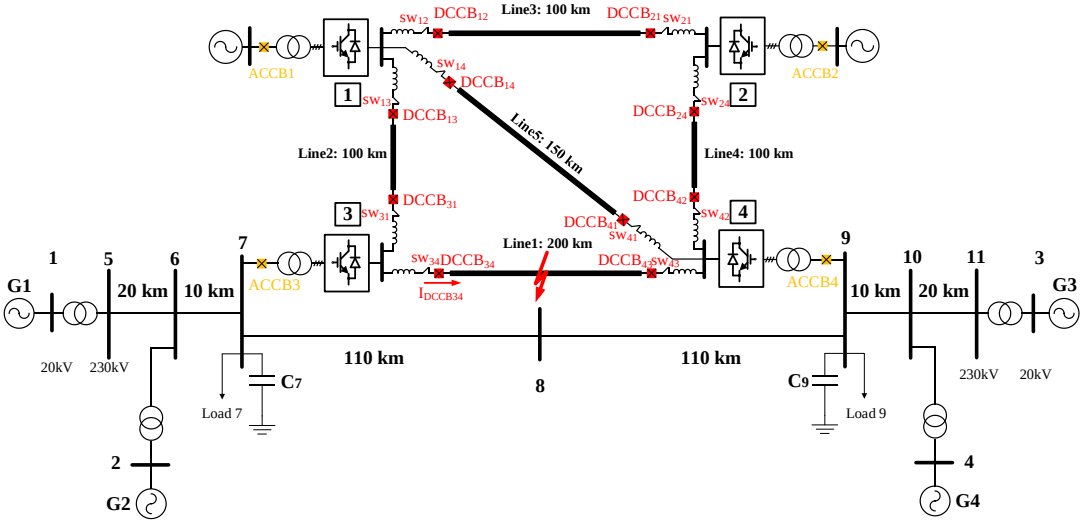


Fig. 4. 1. The test integrated ac/dc transmission system.

The parameters of the synchronous generators are: R_a = 0.0025, X_l = 0.2, X_q = 1.7, X'_q = 0.55, X''_q = 0.25, X_d = 1.8, X'_d = 0.3, X''_d = 0.25, T'_{d0} = 5.0 s, T'_{q0} = 0.4 s, T''_{d0} = 0.03 s, T''_{q0} =0.4 s, H_1=6s , H_2=6s , H_3=5s , H_4= 5s. Each generator has a rating of 900 MVA and 20 kV and the parameters are given in per unit. The transformer has an impedance of 0+j0.15 per unit on 900 MVA and 20/230 kV base. The ac transmission system voltage is 230 kV. The parameters of the lines in the base of 100 MVA and 230 kV are: r = 0.0001 p.u./km, x_L = 0.001 p.u./km, b_C = 0.00175 p.u./km. The capacity of the synchronous generators is 900 MVA.

The parameters of the dc grid are given in Table 4. 1. Both HB and FB MMCs will be modelled. The converter station configuration is symmetrical monopole. The parameter of the HVDC cable has been taken from [133]. The configuration and dimensions of the PSCAD cable model are illustrated in Appendix I. The cable lengths are indicated in Fig. 4. 1. ACCBs are equipped at the grid side of the converter transformers. DCCBs are deployed at the two ends of each HVDC cable. DC current limiting reactors are equipped with each DCCB. The MMC controllers are shown in Appendix II. The control modes and output power of the converters are given in Table 4. 2.

Table 4. 1. Parameters of the dc grid.

Parameters	Real value	In per unit
Converter rated power (MW)	1000	1
DC voltage (kV)	± 320	1
AC side voltage (kV)	230	0.575
Transformer leakage reactance (p.u.)	0.1	0.1
Transformer ratio (kV/kV)	230/400	0.575/1
Number of SMs in each arm	10	-
SM capacitance (mF)	2.5	-
Arm inductance (H)	0.05	0.09817
Arm resistance (Ω)	0.1	0.0000625
AC system frequency (Hz)	50	-
DC current limiting reactor (mH)	100	-

Table 4. 2. The control modes and output power of the converters.

Converters	Control mode	Output power
MMC1	V_{dc} and reactive power	V_{dcref1} = ± 320 kV; Q_{ref1} = 40 MVAr
MMC2	Power control	P_{ref2} = -300 MW; Q_{ref2} = -30 MVAr
MMC3	Power control	P_{ref3} = 400 MW; Q_{ref3} = 40 MVAr
MMC4	Power control	P_{ref4} = -600 MW; Q_{ref4} = -120 MVAr

* The active and reactive power flows from the AC system into each converter are positive.

As this chapter focuses on the responses of the ac/dc system to dc faults, the internal design of the DCCBs was assumed to have little influence on the system dynamic responses [134]-[135]. Therefore, a simplified DCCB has been modelled as an ideal breaker with a surge arrester, as shown in Fig. 4. 2. The surge arrester is rated at 1.5 p.u. of the rated pole-to-ground dc voltage. A delay timer is set to emulate the time of fault discrimination and the opening time of the breaker. This DCCB model can emulate an HCB whose operating time is several milliseconds or a mechanical DCCB whose operating time is tens of milliseconds.

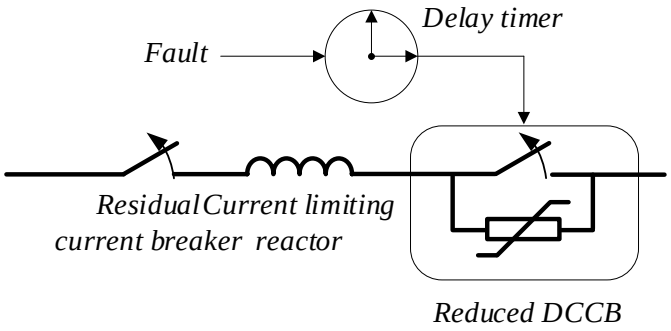


Fig. 4. 2. The simplified DCCB model.

The converter local protection is based on overcurrent and over current-rate-of-change. Tripping signals will be sent to block the IGBTs either the rate-of-change of the current flows through the VSC is higher than 3 kA/ms or the magnitude of the current flows through the VSC exceeds 3 kA. The algorithm of the converter local protection is shown in Fig. 4. 3. Moreover, to make sure that the IGBTs are not damaged by the transient overcurrent or overvoltage during the period of system restoration, the converters will be blocked for 20 ms.

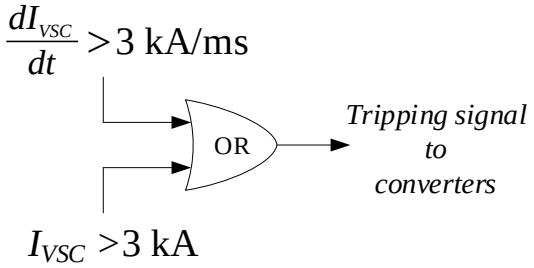


Fig. 4. 3. The algorithm of converter local protection.

4.3 Simulations and analysis

The transient responses and stability of the test ac/dc system subject to a dc fault is assessed. It is to be noted that novel fault isolation and post-fault restoration algorithm is not within the scope of this work. Typical fault isolation time and devices discussed in Section 2.3 are applied and evaluated.

In order to investigate the worst situation, a solid pole-to-pole fault has been applied in the middle of Line 1 at t = 6 s for each case, as shown in Fig. 4. 2. A fault resistance of 1 Ω has been considered. The current flows through $DCCB_{34}$ in Fig. 4. 1, the dc terminal voltages of each converter, the voltages of ac buses 7 and 9, the power angle difference between generators G1 and G3, and the power transferred in the ac corridor are the measured. The protection approaches using HB MMC with DCCB, HB MMC with ACCB and FB MMC are considered for isolating the fault. It should be mentioned that the fault detection and discrimination time can be less than 5 ms in the literature. In this study, a conservative 5 ms for fault detection and discrimination is applied. The results and conclusions may be different if other fault detection and discrimination time is applied.

4.3.1 Case 1 — HB MMC + DCCB

In this study, HB MMCs are used in the dc grid in test system shown in Fig. 4. 1. The Fully Selective Approach and the "Open Grid" concept are employed to isolate the fault in the middle of Line1.

4.3.1.1 Fully Selective Approach

The tripping logic for the DCCBs using the Fully Selective Approach is shown in Fig. 4. 4. The DCCB tripping signal will be generated either the dc terminal voltage is below 80% of the dc voltage reference value or the magnitude of the

current flows through the DCCB is over 3 kA. A 5 ms delay is considered for the fault discrimination. It is assumed that after the fault discrimination, only the faulted line associated with DCCBs are selected to isolate the fault. Moreover, a 5 ms delay is added for the operating time of the DCCBs. Therefore, a 10 ms time delay is added before tripping the faulted line associated with DCCBs. The converter local protection algorithm is based on the scheme shown in Fig. 4. 3.

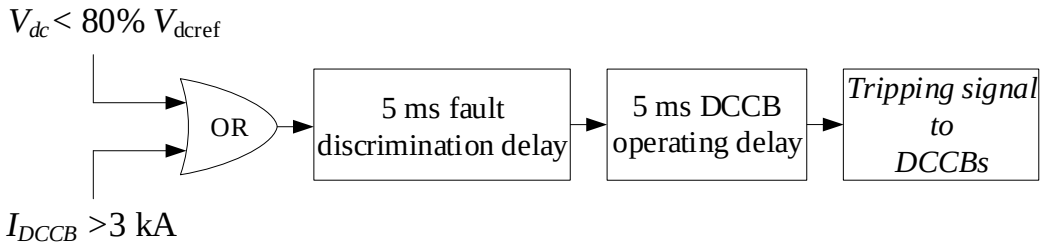


Fig. 4. 4. The algorithm of tripping DCCBs using the Fully Selective Approach.

In this case, only the faulted Line1 associated with $DCCB_{34}$ and $DCCB_{43}$ will be tripped. Fig. 4. 5 shows the positive and negative pole currents flowed through the $DCCB_{34P}$ and $DCCB_{34N}$. As the fault is pole-to-pole, the currents in the positive and negative poles are symmetrical. The magnitude of the fault current $I_{DCCB34P}$ reached 3 kA at t = 6.017 s. Then the tripping signal was generated and sent to the breakers after a 10 ms delay. The maximum magnitude of the fault current was 9.74 kA. The fault currents became zero at t = 6.0136 s.

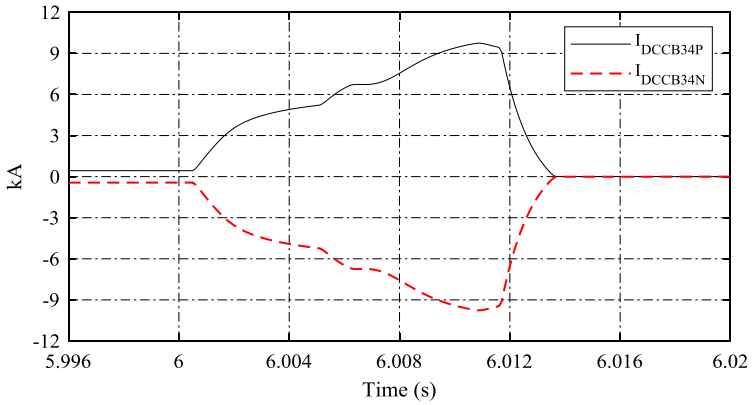


Fig. 4. 5. The fault current passing the DCCB34.

Fig. 4. 6 shows the positive dc terminal voltages of the four converters. As the positive and negative pole voltages are symmetrical during the pole-to-pole fault, only the positive terminal voltages are depicted. The dc voltages started to drop once the fault occurred. The voltages of the converters 3 and 4 dropped earlier and

lower than the other two converters as the fault is closed to the converters 3 and 4. The voltages started to recover once the fault was isolated. The dc voltages experienced oscillations during the recovery period and became stable 0.4 s after isolating the fault. It should mention that the dc voltage did drop to zero during the dc fault because the fault is 100 km away from the converters and the dc reactor also limit the voltage drop.

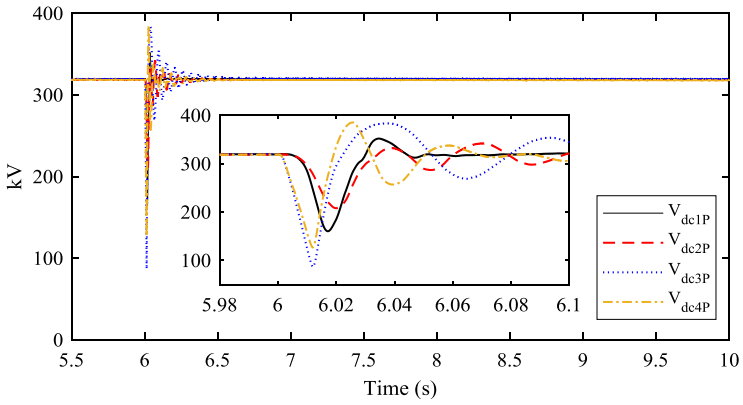


Fig. 4. 6. Converter positive dc terminal voltages.

The voltages of ac buses 7 and 9 are illustrated in Fig. 4. 7. As the converters 3 and 4 were blocked by their local protection system, the ac currents were infeeded to the fault through the uncontrollable bridges. This is equivalent to a three-phase short-circuit on the ac bus. However, due to the limitation of the impedance of the converter interface transformer and the fast fault isolation using DCCBs, the ac voltages did not drop to zero, and it started to recover once the fault was isolated.

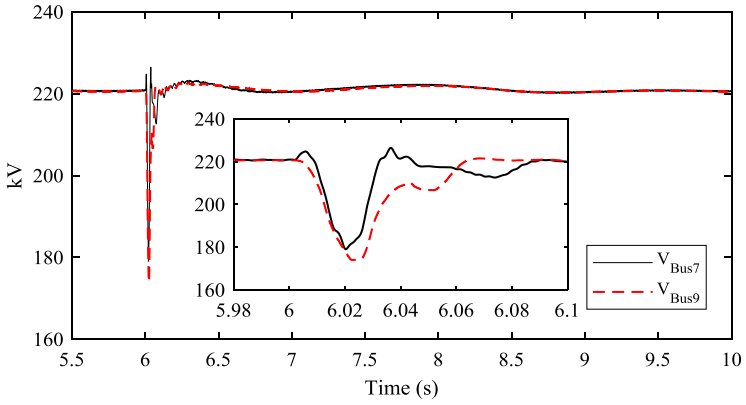


Fig. 4. 7. Voltages of ac buses 7 and 9.

It also should be noted that the two ac buses were impacted by the dc fault at almost the same time. The reason for this behaviour is that unlike the ac counterparts, MTDC grids are “low-inertia” systems and thus the dc voltage drop

propagates quickly within the MTDC grid once a dc fault occurs. The ac system will be affected at multiple locations (converters). From the viewpoint of ac systems, a dc fault within the dc grid can be seen as "multiple faults".

Although the faulted dc line was isolated, the power in this line shifted to other routes within the dc grid. The converters are capable of operating at the pre-fault output power. For this reason, the power transferred in the ac corridor recovered to the original value after the fault, as shown in Fig. 4. 8.

Fig. 4. 9 shows the power angle difference between the generators G1 and G3 which are the two generators that have the farthest electrical distance. The power angle difference reached steady state after oscillations.

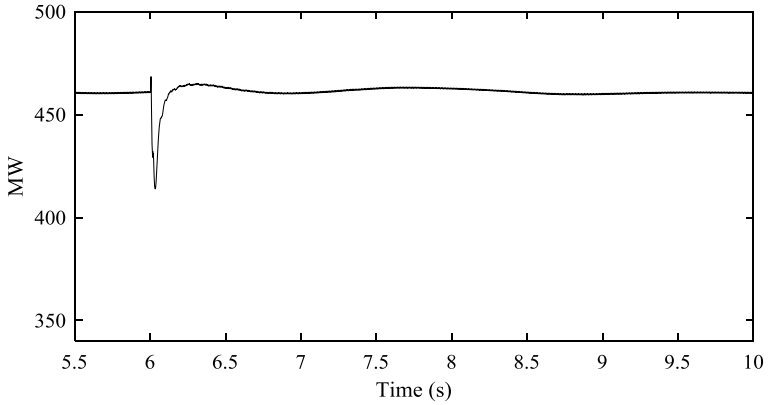


Fig. 4. 8. The power in the ac transmission line.

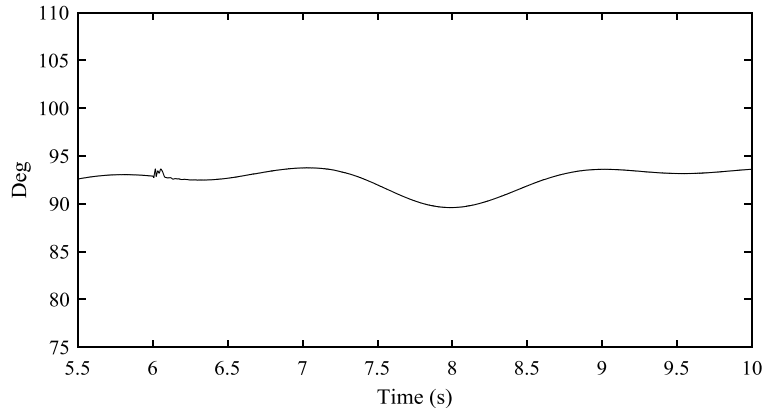


Fig. 4. 9. The power angle difference between generators G1 and G3.

4.3.1.2 "Open Grid" Approach

In this case, the "Open Grid" Approach is employed to isolate the same fault in the last section. The tripping logic for the DCCBs, in this case, is shown in Fig. 4. 10. The tripping signals for DCCBs will be generated once the dc terminal voltage

is below 80% of the dc voltage reference value or the magnitude of the DCCB current is over 3 kA. The difference between the "Open Grid" Approach and the Full Selective Approach is that all the DCCBs will be tripped immediately depending on their local measurement without fault discrimination. A 5 ms delay is added for the operating time of the DCCBs. A 5 ms delay is considered for the fault discrimination using the residual voltages and currents of the remaining circuits. It is assumed that after the fault discrimination, only the faulted line associated DCCBs are selected to isolate the fault and other DCCBs will be reclosed. The converter local protection algorithm is based on the scheme shown in Fig. 4. 3.

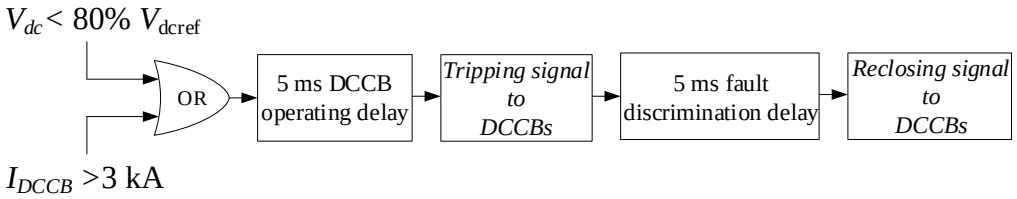


Fig. 4. 10. The algorithm of tripping DCCBs using the "Open Grid" Approach.

Fig. 4. 11 shows operating status (the low state is on and the high state is off) of the DCCBs in the positive poles. $DCCB_{34}$ and $DCCB_{43}$ detected the fault earlier than other breakers, and therefore tripped earlier. Even though the $DCCB_{31}$ connected to the same dc bus with $DCCB_{34}$, $DCCB_{31}$ detected the fault later than $DCCB_{34}$ due to the limitation of the current liming reactors in the dc lines. This applies the same to $DCCB_{42}$ and $DCCB_{41}$ that connected to the same dc busbar with $DCCB_{43}$. The $DCCB_{34}$ and $DCCB_{43}$ were permanently turned off after the fault discrimination while other breakers were reclosed.

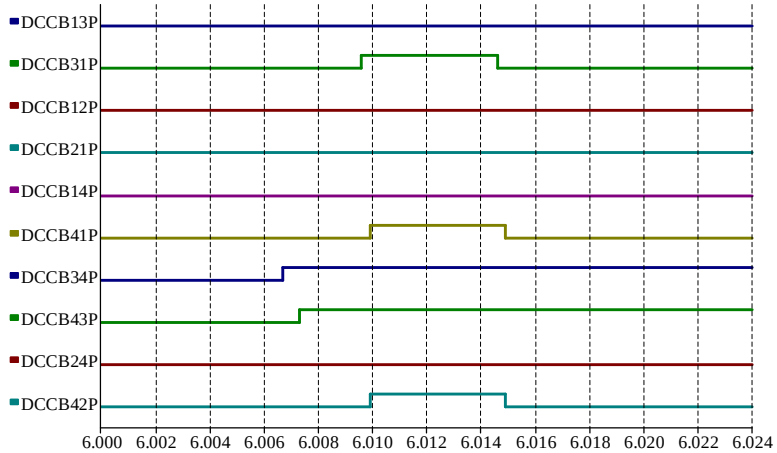


Fig. 4. 11. Tripping and reclosing signals for DCCBs (Only the DCCBs in the positive pole are shown due to the symmetrical fault characteristics of the positive and negative poles).

The fault currents passing through $DCCB_{34}$ are illustrated in Fig. 4. 12. Because the breakers were turned off without fault discrimination, the maximum fault current was reduced to 6.73 kA (31% lower than the case using the Fully Selective Approach). The fault currents dissipated to zero at t = 6.0079 s.

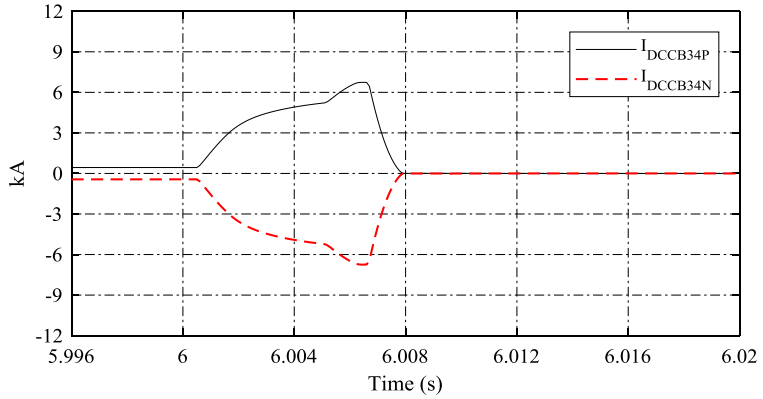


Fig. 4. 12. The fault current passing the DCCB34.

Fig. 4. 13 shows the positive dc terminal voltages of the four converters. As the faulted line was isolated earlier than the case of using the Fully Selective Approach, the dc voltages stopped dropping earlier than the previous case. This resulted in higher dc voltages after isolating the dc fault. The higher dc voltages facilitated the post-fault restoration, for instance, reducing the magnitudes of the voltage oscillations compared to the previous case.

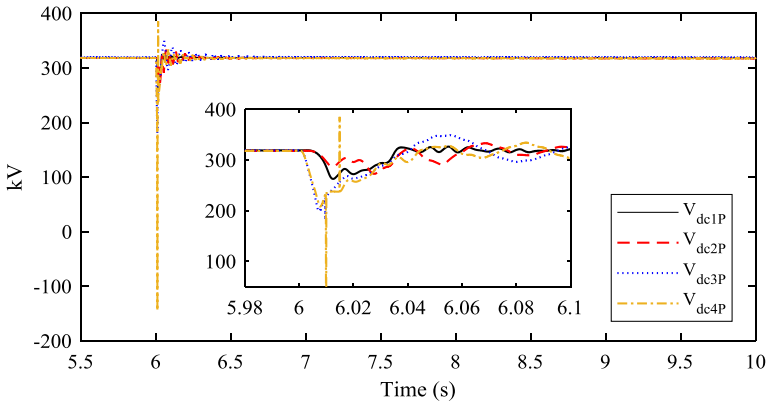


Fig. 4. 13. Converter positive dc terminal voltages.

It should be noted that the transient overvoltage of V_{dc4P} was caused by the current limiting reactors connected with the $DCCB_{42}$ and $DCCB_{41}$. $DCCB_{42}$ and $DCCB_{41}$ were turned off almost at the same time once their fault detection logics were triggered by detecting the low dc voltages. The $DCCB_{43}$ was turned off earlier than the two breakers. Therefore, converter 4 were totally isolated from the rest of

the dc circuits once all the three breakers were turned off. There was no current path for dissipating the reactors' currents. The energy stored in these current limiting reactors were dissipated in a short time which led to the transient overvoltage.

Due to the short fault isolation times, the system was impacted less severely than the case employed Fully Selective Approach. Fig. 4. 14 shows the ac bus voltages. The earlier isolation of the faulted line stopped the further dropping of the ac voltages. Fig. 4. 15 and Fig. 4. 16 show the ac line power and the power angle between the generators G1 and G3, respectively. The overall system restored to the steady state faster than the previous case.

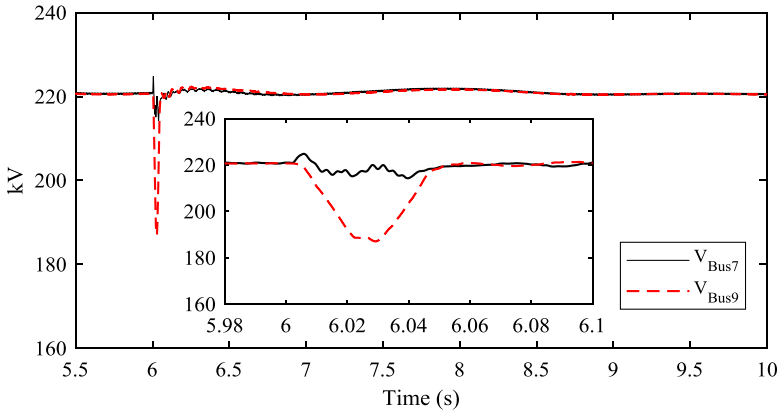


Fig. 4. 14. Voltages of ac buses 7 and 9.

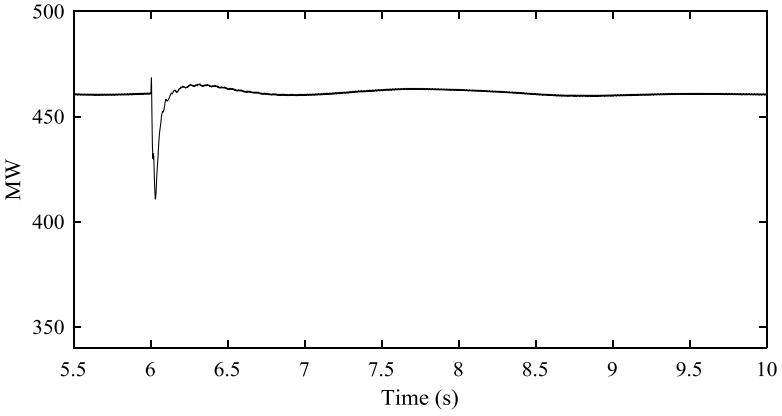


Fig. 4. 15. The power in the ac transmission line.

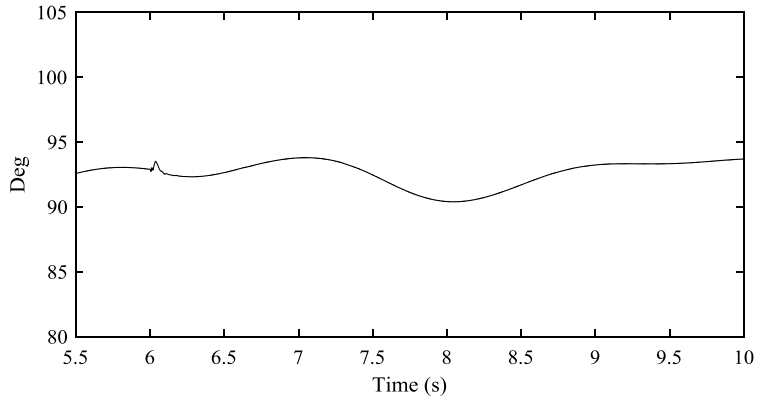


Fig. 4. 16. The power angle difference between generators G1 and G3.

4.3.2 Case 2 — HB MMC + ACCB

In this study, the ACCBs have been employed to protect dc grid against the same dc fault in the previous cases. The "Handshaking" method proposed in [110] is applied. The detailed steps in implementing the method are in Appendix III.

Due to the long operating time of ACCBs, all converters were blocked by the converter local protection before the ACCBs were turned off. A waiting time of 80 ms was used to emulate the operating time of ACCBs. It is assumed that the fault discrimination and location were completed within this period. The ac currents kept infeeding into the dc side through the controllable bridges as shown in Fig. 4. 17. Therefore, the dc fault current was keeping increasing. The maximum fault current reached 13.98 kA within 80 ms, as shown in Fig. 4. 18. The fault currents started to neutrally decay once the ACCBs were turned off. The faulted line associated dc switches opened when the currents decay to a low value (20 A).

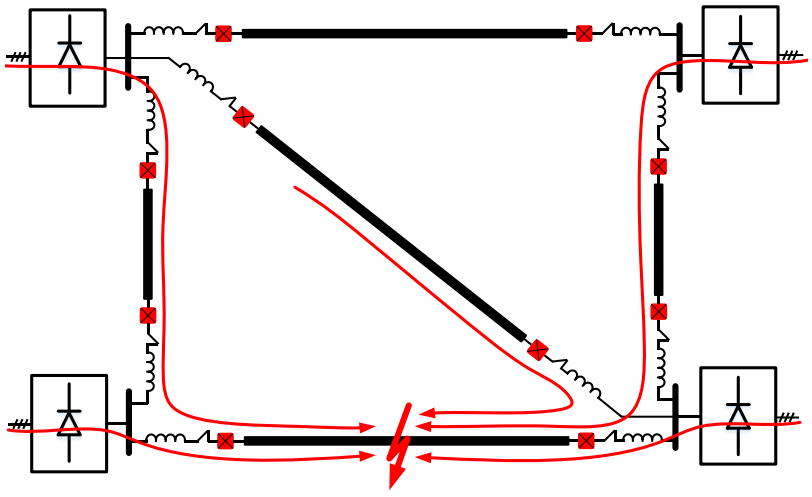


Fig. 4. 17. Equivalent circuit of the dc grid after all converters were blocked.

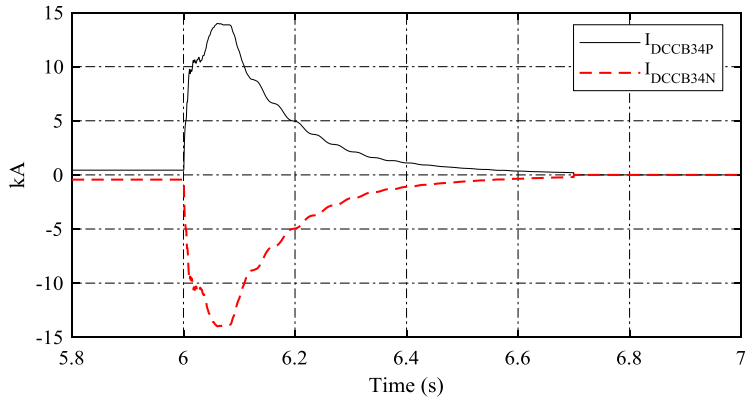


Fig. 4. 18. The fault current passing the DCCB34.

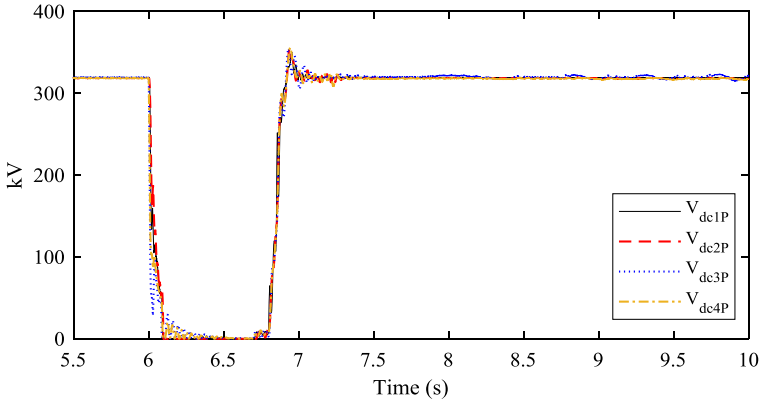


Fig. 4. 19. Converter positive dc terminal voltages.

Fig. 4. 19 shows the positive dc terminal voltages of the four converters. The dc voltage of the whole dc network dropped to zero due to the long waiting for the current to decay to an acceptable low value for the dc switches. The post-fault restoration process started once the faulted line was isolated and thereafter the dc voltage started to recover.

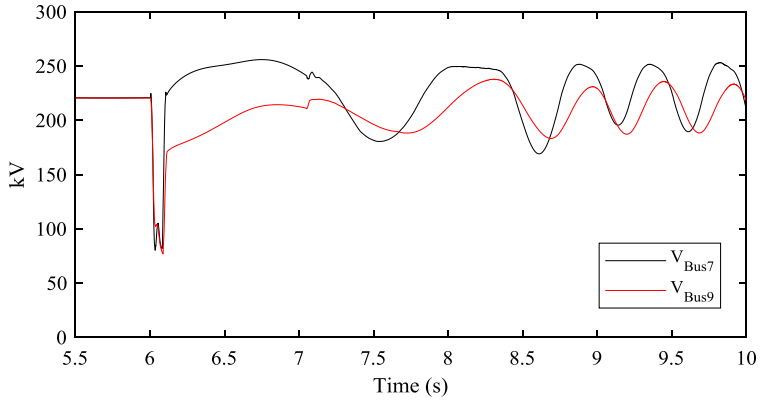


Fig. 4. 20. Voltages of ac buses 7 and 9.

The ac voltages of buses 7 and 9 are illustrated in Fig. 4. 20. The two ac voltages started to drop once the dc fault occurred. The infeeding currents through the controllable bridges drew a large amount of reactive power in converter ac side. Thus, ac voltages dropped more severely than the previous cases. As previously pointed out, the ac system was suffering "two faults" at buses 7 and 9 caused by the dc fault.

Moreover, as observed from Fig. 4. 20 to Fig. 4. 22, after the isolation of the dc fault, the power transferred in the ac corridor and the power angle of the generators experienced large oscillations. Finally, the ac voltages became unstable. It means that the long fault isolation and post-fault restoration time (several hundred milliseconds) were not acceptable for the ac system.

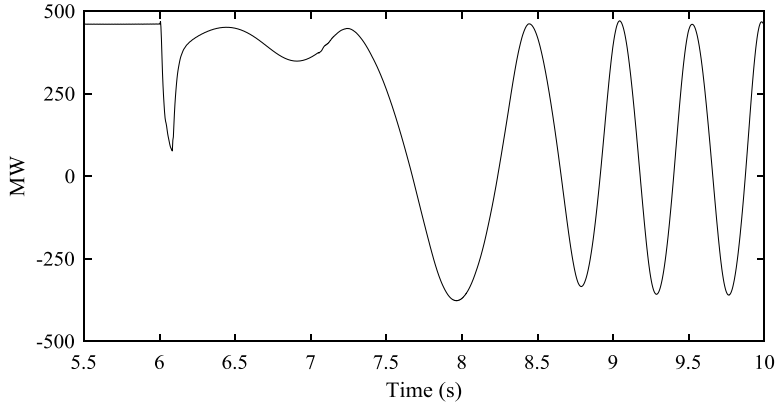


Fig. 4. 21. The power in the ac transmission line.

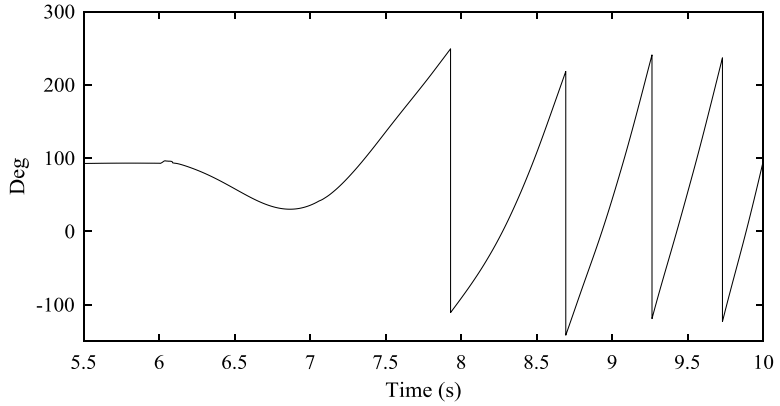


Fig. 4. 22. The power angle difference between generators G1 and G3.

4.3.3 Case 3 — FB MMC

In this case, the HB MMCs in the dc grid were replaced by FB MMCs. The converters are blocked immediately once a dc fault is detected. As explained in

Section 2.2.1.4, the ac infeeding currents will be blocked if the sum voltage of all SM capacitors in the arms is higher than the valve-side line voltage. The equivalent circuit of the dc grid after blocking all converters are shown in Fig. 4. 23.

The voltage dropped quickly at the fault location. However, the converter dc terminal voltages did not drop instantaneously due to the voltage support from the distributed capacitance and inductance of the HVDC cable. Moreover, right after the occurrence of the fault, voltage surges started to travel from the fault location into both directions toward the terminals [133]. Upon the arrival at the terminals, the voltage surges were reflected as reversed voltage surges, as illustrated in Fig. 4. 23. At the same time, due to the resistance and distributed capacitance along the transmission line, the magnitudes of the surges decay gradually. Therefore, once all the converters within the dc grid were blocked, the converter terminal voltages started to periodically reverse polarity with decaying magnitudes. The period of the reversing polarity and the magnitude decaying speed depend on the system parameters and the fault impedance.

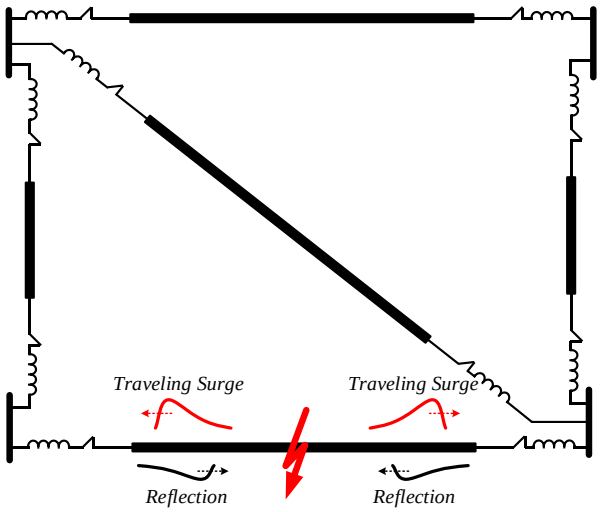


Fig. 4. 23. Equivalent circuit of the dc grid after all converters were blocked.

Fig. 4. 24 illustrates the positive and negative pole currents passed through the $DCCB_{34P}$ and $DCCB_{34N}$. The fault current has reached 3.12 kA at the moment the converters were blocked. Then the converter terminal voltages started to oscillate with decaying magnitudes, as shown in Fig. 4. 25, which resulted in the oscillations of the fault currents.

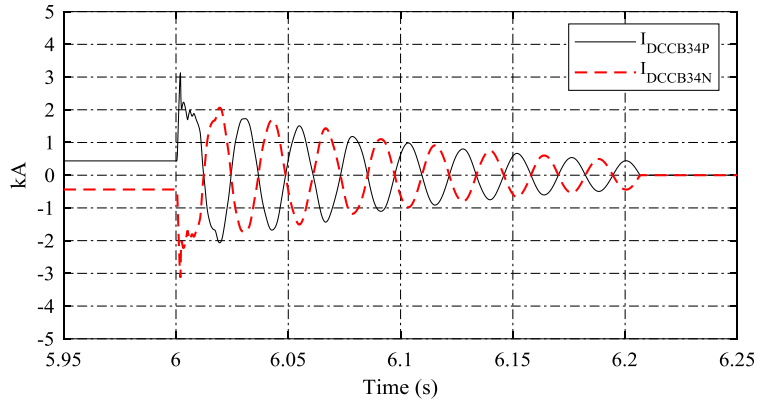


Fig. 4. 24. The fault current passing the DCCB34.

It can be seen that the fault currents were reversing directions and decaying. As the fault currents have zero-crossings, switches which can interrupt a few hundred amperes can be utilised to interrupt this type of fault currents. In this study, the switches were turned off once the magnitude of the fault current was below 500 A. The rate-of-decay of the fault current depends on the parameters of the dc circuit and fault impedance. A larger fault resistance leads to a faster decay. In this case, the fault resistance is 1 Ω. The results of a 10 Ω fault resistance are shown in Appendix IV. Although some work has been conducted using controlled discharge during system shutdown in point-to-point FB MMC links [136], more work needs to be carried out for MTDC grid.

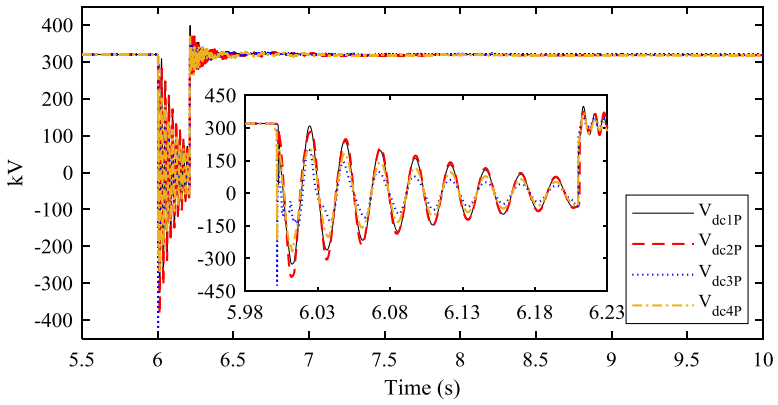


Fig. 4. 25. Converter positive dc terminal voltages.

Fig. 4. 26 shows the currents at the grid-side of the MMC3. The current became near zero once the MMC3 was blocked. There was no contribution to the dc fault currents from the ac side. Therefore, the maximum dc fault currents were significantly reduced compared to the cases using DCCBs and ACCBs.

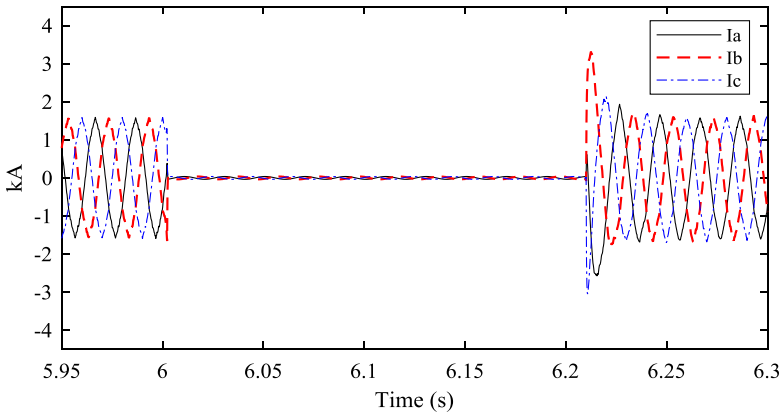


Fig. 4. 26. Currents at the grid side of MMC3.

Fig. 4. 27 illustrated the ac voltages at buses 7 and 9. Both buses were impacted by the blocking of the converters. Before the fault, the MMC3 was absorbing power from the bus 7. The power transmitting through the MMC3 became zero once the converter was blocked, which led to the voltage increase of bus 7. The MMC4 was injecting power to the bus 9. Therefore, the voltage of bus 9 dropped once the MMC4 was blocked.

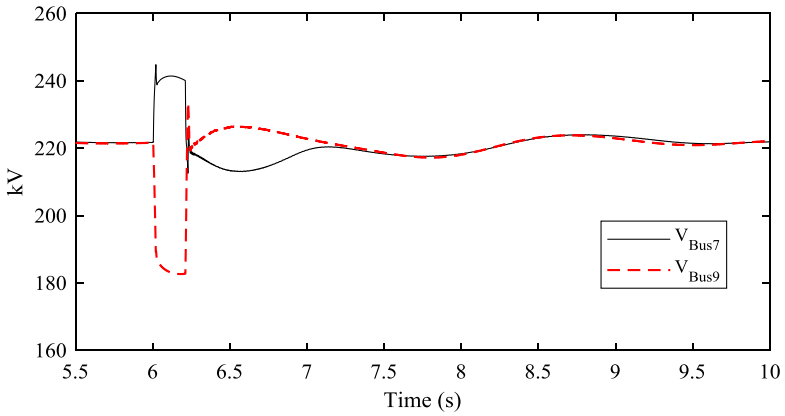


Fig. 4. 27. Voltages of ac buses 7 and 9.

Fig. 4. 28 and Fig. 4. 29 show the ac line power and the power angle between the generators G1 and G3. It can be seen from Fig. 4. 27 to Fig. 4. 29 that the ac system restored to the steady state.

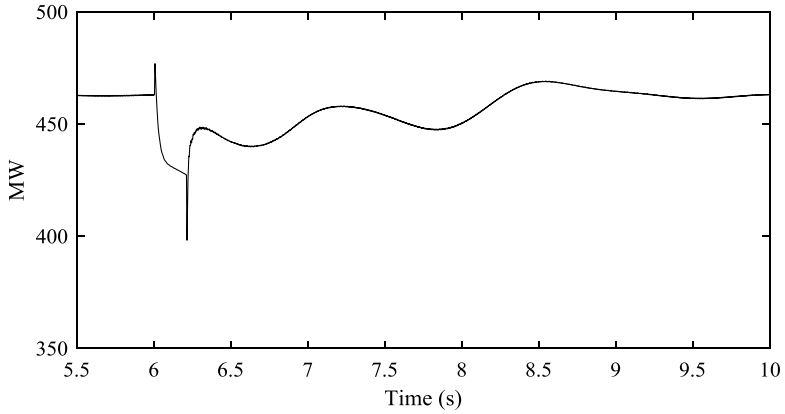


Fig. 4. 28. The power in the ac transmission line.

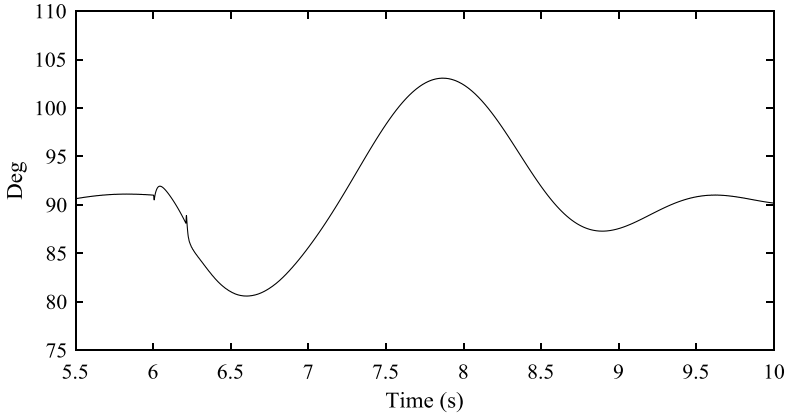


Fig. 4. 29. The power angle difference between generators G1 and G3.

4.4 Summary

In this chapter, the dynamic interactions between a dc grid and its connected ac system subjected to dc faults were analysed and assessed. Different fault isolation methods were employed in the simulations. The comparisons of the studied protection methods are given in Table 4. 3.

Table 4. 3. Comparisons of different protection methods

Indicators	**HB MMCs with DCCBs (FullySelective)**	**HB MMCs with DCCBs (OpenGrid)**	**HB MMCs with ACCBs**	**FB MMCs with dc switches**
DC fault currents	Medium	Low	High	Low
De-energisation of the entire DC grid	Parts	No	Yes	Yes
Time for fault isolation	Short	Short	Long	Medium
Impacts on converter ac side voltages	Low	Low	High	Low

In the case of using DCCBs as fast fault clearance devices, the dc fault can be isolated quickly. The Fully Selective Approach imposed quite a high current interruption duty on the faulted line associated breakers. The fault isolation time can be less than ten milliseconds. The entire dc grid will not be fully discharged.

On the other hand, the "Open Grid" method reduced the current interrupting requirement for DCCBs by reversing the protection sequence order. However, this method may extend the outage area of the dc grid. Moreover, the unpredictability of a tripping and/or reclosing sequence may lead to transient overvoltage and overcurrent.

The use of ACCBs needs to be carefully assessed as this method leads to the de-energisation of the entire dc grid. The dc system requires several hundred milliseconds to isolate the fault and restore to the steady state. A long fault isolation and restoration time can easily lead to the instability of the overall ac/dc system. Therefore, the approach using ACCBs as fault clearing devices may not be suitable for an overlay ac/dc transmission system with high power supply requirement.

FB MMC-based dc grid can block the ac infeeding currents by blocking all the converters. This method leads to the outage of the entire dc grid. DC switches which can interrupt currents with zero crossings are needed to isolate the faulted line. However, the switches need to wait for the decay of the fault currents to acceptable low values. A long wait may lead to the instability of the overall system. Moreover, the quick voltage polarity reversing after blocking all the converters may damage the dc cables. In addition, the high capital costs and operating losses are the drawbacks of this method.

Chapter 5

Single-phase Faults at the Valve-side of Symmetrical MMCs

5.1 Introduction

The studies in previous chapters focused on the dc side faults. The impact of converter ac side faults also needs to be taken into account in the designing of HVDC systems. Although there have been research on converter grid-side ac faults, MMCs subject to station internal faults are not widely studied both in the industry and academia.

The area between the converter valve and the interface transformer is in the overlapping protective zones of the converter and the ac system [137], as shown in Fig. 5. 1. The valve-side winding bushings of these transformers protrude through the hall wall to connect to converter ac buses [24]-[25]. The ac buses in this area need high insulation to withstand high voltages and large currents. Insulation failure and/or flashover of wall bushings may cause single-phase-to-ground (SPG) faults, which are typically permanent, between the converter and the transformer. Valve-side SPG fault can lead to severe consequences, such as commutation failures in LCCs, dc voltage oscillations in symmetrical monopole MMCs, and non-zero-crossing fault currents in bipole MMCs [29]-[30].

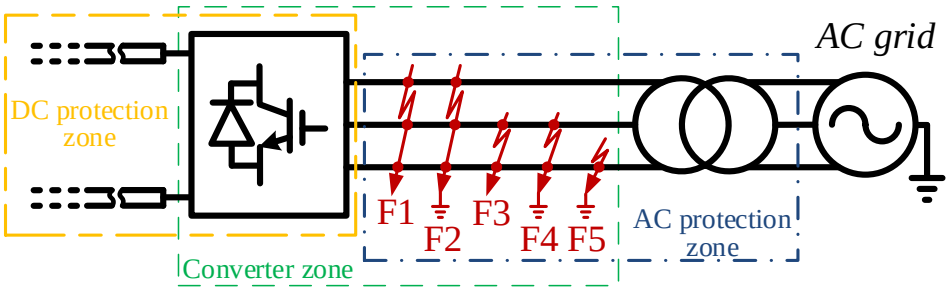


Fig. 5. 1. Schematic diagram of station internal ac faults and protection zones.

In this chapter, the characteristics of SPG faults at the valve-side of symmetrical monopole HB MMCs are theoretically analysed. Then, the factors, such as the converter grounding schemes, dc lines and fault resistance, that might influence the fault characteristics are studied. A protection strategy has been proposed for point-to-point MMC HVDC transmission systems based on the theoretical analysis. For completeness, the analysis and the proposed protection is validated by simulations performed in PSCAD/EMTDC.

5.2 Valve-side single-phase faults in symmetrical monopole MMC

Fig. 5. 2 shows the topology of a symmetrical monopole MMC. Each phase consists of one upper and one lower arm. Each arm has N series-connected SMs and one inductor L. The equivalent circuit resistance is represented by resistor R. Each SM contains two IGBTs, two diodes and one capacitor C_{SM}. As the grounding scheme Δ/Yg presented in Section in 2.2.5.2 has been widely used in practical applications, this grounding scheme is applied as the base case.

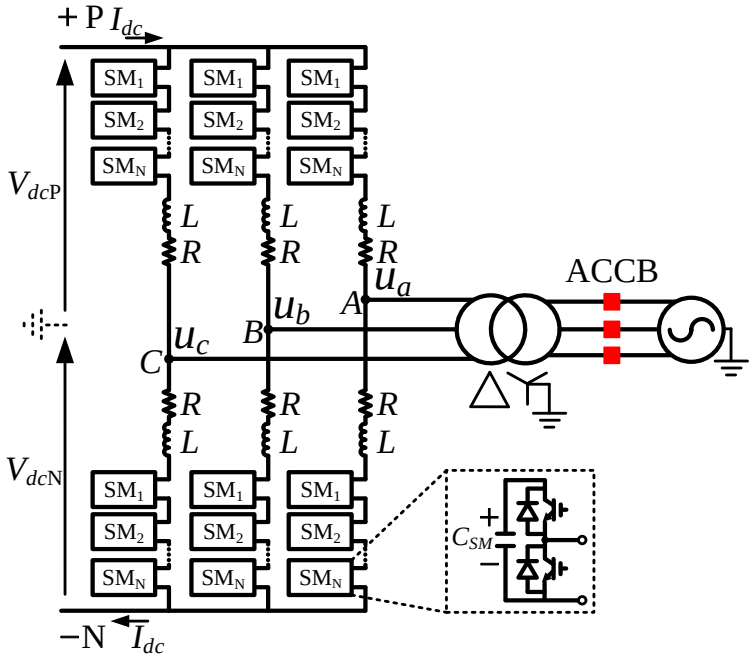


Fig. 5. 2. Converter topology of a symmetrical monopole HB MMC.

Fig. 5. 3 illustrates the single-phase equivalent circuit of the MMC shown in Fig. 5. 2. u_x is the ac phase-to-ground voltage, i_x the phase current, $u_{x\mathrm{P}}$ and $u_{x\mathrm{N}}$ are the voltages produced by SMs in the upper and lower arms, $i_{x\mathrm{P}}$ and $i_{x\mathrm{N}}$ the arm currents, i_{xcirc} the circulating current, and $V_{dc\mathrm{P}}$ and $V_{dc\mathrm{N}}$ the dc pole-to-ground voltages, with $V_{dc\mathrm{P}} = -V_{dc\mathrm{N}} = 1/2V_{dc}$, where V_{dc} is the dc terminal voltage. In normal operation, the sum of the voltages of all SM capacitors in each arm approximately equals to V_{dc}.

According to Fig. 5. 3, the MMC is characterised by the following equations:

$$u_x = -\frac{1}{2}L\frac{di_x}{dt} - \frac{1}{2}Ri_x + \frac{u_{x\mathrm{N}} - u_{x\mathrm{P}}}{2} \quad (x = a, b, c) \tag{5.1}$$

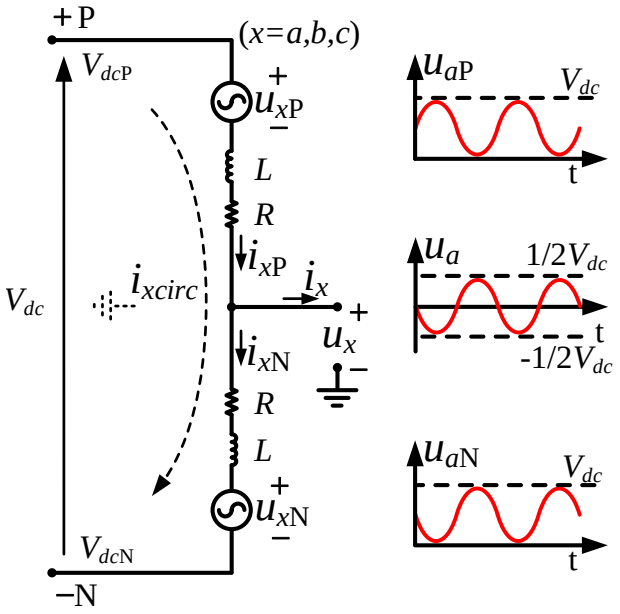


Fig. 5. 3. Single-phase equivalent circuit of an MMC.

$$L\frac{di_{xcirc}}{dt}+Ri_{xcirc}=\frac{1}{2}V_{dc}-\frac{u_{xN}+u_{xP}}{2}\ (x=a,b,c) \tag{5.2}$$

Equation (5.1) describes the dynamics between the MMC and its connected ac grid. The power exchange can be controlled through regulating the switching states of upper and lower arm SMs. Equation (5.2) shows the inner dynamics of the MMC. The circulating current i_{xcirc} can be reduced to quite a low value using damping controllers to reduce second harmonics and power losses [138].

If the circulating currents and the voltage drops on arm reactors and resistors are ignored, from Fig. 5. 3, the dc pole voltages can be obtained as

$$\begin{cases} V_{dcP}=u_x+(u_{xP}+L\dfrac{di_{xP}}{dt}+Ri_{xP})\approx u_x+u_{xP} \\ V_{dcN}=u_x-(u_{xN}+L\dfrac{di_{xN}}{dt}+Ri_{xN})\approx u_x-u_{xN} \end{cases} \tag{5.3}$$

where u_{xP} and u_{xN} can be expressed as:

$$\begin{cases} u_{xP}=1/2V_{dc}[\sin(2\pi ft+\theta_x)+1] \\ u_{xN}=1/2V_{dc}[1-\sin(2\pi ft+\theta_x)] \end{cases} \tag{5.4}$$

where θ_x is the phase-angle, f is the system fundamental frequency. Voltages u_{aP}, u_{aN} and u_a in phase A are illustrated in Fig. 5. 3.

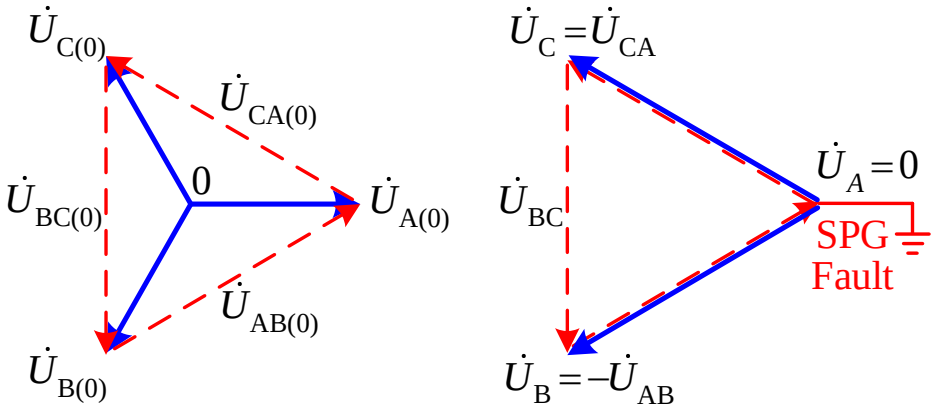
According to (5.3), the following relationships can be obtained:

$$\begin{cases} u_{ab} \approx u_{b\mathrm{P}} - u_{a\mathrm{P}}, u_{ca} \approx u_{a\mathrm{P}} - u_{c\mathrm{P}} \\ u_{ab} \approx u_{a\mathrm{N}} - u_{b\mathrm{N}}, u_{ca} \approx u_{c\mathrm{N}} - u_{a\mathrm{N}} \end{cases} \tag{5.5}$$

where u_{ab} and u_{ca} are the valve-side line voltages.

Fig. 5. 4(a) depicts the converter valve-side voltages before a valve-side SPG fault in phase *A*. The neutral point voltage is 0 because the three-phase voltages are symmetric. The fault creates a solid grounding point as shown in Fig. 5. 4(b). It can be seen that the magnitudes of the line voltages remain unchanged, however, the phase voltages become

$$\dot{U}_{\mathrm{A}} = 0,\ \dot{U}_{\mathrm{B}} = -\dot{U}_{\mathrm{AB}},\ \dot{U}_{\mathrm{C}} = \dot{U}_{\mathrm{CA}}. \tag{5.6}$$



(a) Pre-fault voltages. (b) Post-fault voltages.

Fig. 5. 4. Valve-side voltages before and after the fault.
(Solid lines are phase voltages; dash lines are line voltages)

If the converter is not blocked, $V_{dc\mathrm{P}} \approx u_{a\mathrm{P}}$ and $V_{dc\mathrm{N}} \approx -u_{a\mathrm{N}}$ can be obtained by substituting (5.6) into (5.3) and (5.5). According to (5.4), $u_{a\mathrm{P}}$ and $u_{a\mathrm{N}}$ contain a large dc offset and oscillate sinusoidally with the fundamental frequency. Therefore, the dc pole-to-ground voltages $V_{dc\mathrm{P}}$ and $V_{dc\mathrm{N}}$ will also oscillate sinusoidally. Moreover, if the dc voltage is regulated by other MMCs, then $V_{dc\mathrm{P}} - V_{dc\mathrm{N}} \approx u_{a\mathrm{P}} - (-u_{a\mathrm{N}}) = V_{dc}$. It means the pole-to-pole dc voltage will not be impacted as a result of the same offsets in the dc pole voltages and the dc voltage control of other MMCs.

It should be emphasised that, as the three ac phases are symmetrical, the analysis of the fault in phase *A* is applicable in the other two phases. Therefore, it can be concluded that a valve-side SPG fault will result in overvoltage at the non-faulted

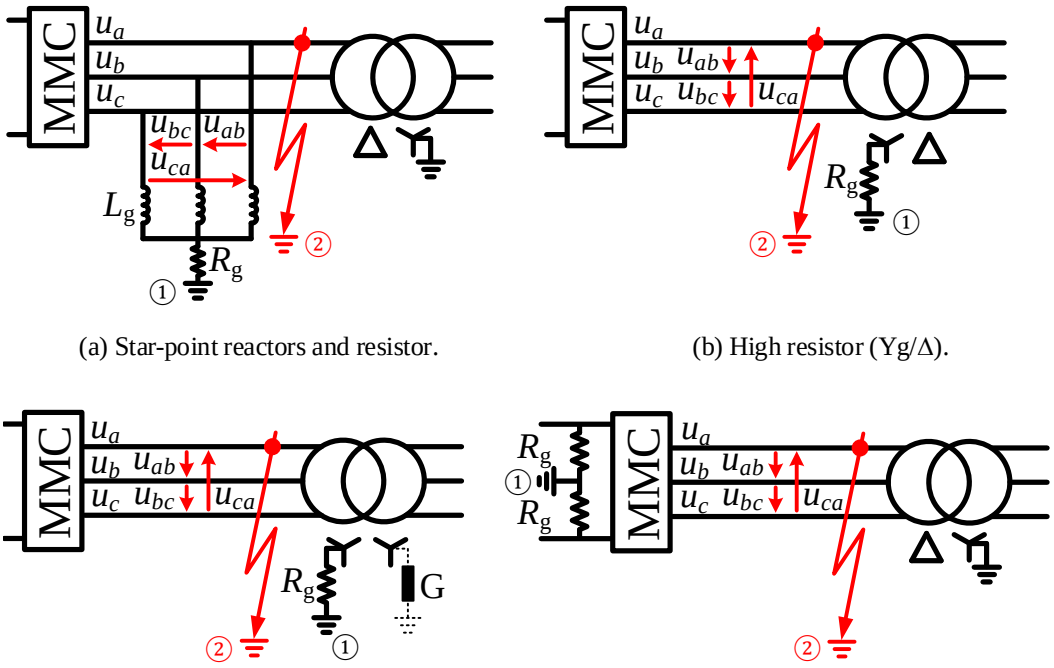
ac phases and dc pole voltage oscillations. And the behaviours of the dc pole voltage oscillations depend on the arm voltages in the faulted phase.

5.3 Factors affecting the SPG fault characteristics

The factors, for instance, the converter grounding systems and the dc transmission lines, that may affect the fault characteristics are analysed in this section.

5.3.1 Influence of converter grounding schemes

Fig. 5. 5 illustrates a phase *A* to ground fault under different grounding schemes. ① is the pre-fault system grounding point and ② is the grounding point created by the fault. According to the previous analysis, the post-fault line voltages will not be affected by an SGP fault due to the valve-side delta connection of the transformer. Therefore, the line voltages on the star-point reactors, as shown in Fig. 5. 5(a), will not change. As the reactance and resistance are large, the current flowing through the reactors and resistor under fault conditions will be limited to small values.



(a) Star-point reactors and resistor.

(b) High resistor (Yg/Δ).

(c) High resistor (Yg/Δ).

(d) DC side high resistors.

Fig. 5. 5. Schematic diagrams of phase *A* to ground fault under different grounding schemes.

In Fig. 5. 5(b) and Fig. 5. 5(c), as the grounding resistance is large, the previous analysis is applicable in these two schemes, and therefore fault current will be small under fault conditions. The grounding scheme of the grid-side Y connection in Fig.

5. 5(c) depends on the requirements of the grid-side network, which will lead to different fault responses in the grid-side. For instance, there will be no zero-sequence current in the grid-side if the Y connection is ungrounded, or there will be zero-sequence current if the Y connection is grounded through an impedance.

The dc side has a solid grounding point in the case shown in Fig. 5. 5(d). Therefore, the significant oscillations of the dc pole voltages caused by a valve-side SPG fault will result in fault currents in the two grounding resistors. However, as the two resistors are large, the fault currents will be small.

It can be concluded that fault characteristics of a valve-side SPG fault will not be affected by different grounding schemes discussed in section.

5.3.2 Influence of dc transmission lines

Fig. 5. 6 shows that the delta connection of the transformer prevents valve-side SPG faults from creating closed paths for fault currents from the dc side and discharging currents from the SM capacitors. Hence, there will be no fault current if the effects from the dc line are ignored. However, there are distributed capacitors of dc transmission lines, especially for long HVDC cables [139]. According to the previous analysis, a valve-side SPG fault will lead to severe oscillations of the dc pole voltages. Therefore, the energy stored in the HVDC line will discharge through the distributed capacitors and in turn lead to serious fault currents.

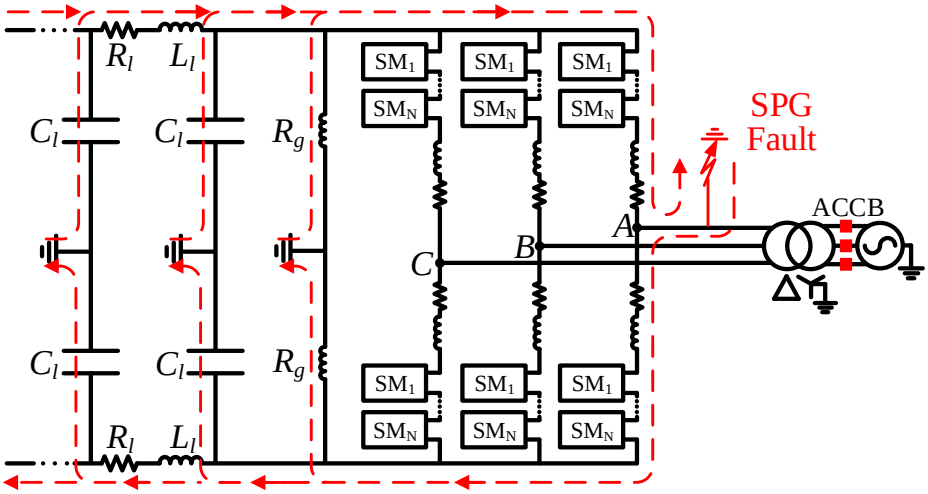


Fig. 5. 6. Current discharging paths of the distributed capacitors of the dc line.

Fig. 5. 6 illustrates an MMC with dc line which is modelled using multiple PI

sections. R_l and L_l are the resistor and reactor and C_l the distributed capacitor. The discharging paths of the distributed capacitors through the faulted phase are depicted in the figure. It should be noted that the discharging currents flow through the non-faulted phases and create closed paths with the transformer. For clarity, they are not shown in the figure. As mentioned in the last section, if the grounding scheme using dc resistor is employed, there will also be currents flow through the two resistors. However, these currents flow through the resistors will be small due to the large resistance.

It can be noted that the longer the dc line is and the higher the dc voltage, the more energy will be stored in the line, and therefore, more significant fault currents will be generated. In order to guarantee the security of the system operation and hence protect devices, actions are required which will be discussed in the following sections.

5.4 Protection strategy for valve-side SPG fault

From the previous analysis, it can be concluded that a valve-side SPG fault will lead to ac side overvoltage in the non-faulted phases and oscillations in the dc pole voltages. In addition, significant fault currents will be generated if the HVDC line is long and the dc voltage is high. In order to protect the semiconductors and other devices, the converter will be blocked once the fault is detected.

An MMC will become an uncontrollable bridge once it is blocked. The single-phase equivalent circuit of a blocked converter is shown in Fig. 5. 7. C_{eq} represents the equivalent capacitor of all SM capacitors in each arm. It can be seen that the upper and lower arm capacitors will be charged through diodes once the following requirements are satisfied.

$$V_{dc\mathrm{P}} - u_x > u_{x\mathrm{P}(0^-)} \tag{5.7}$$

$$u_x - V_{dc\mathrm{N}} > u_{x\mathrm{N}(0^-)} \tag{5.8}$$

where $u_{x\mathrm{P}(0\text{-})}$ and $u_{x\mathrm{N}(0\text{-})}$ are the sum voltages of all SM capacitors in each arm at the moment when the converter is blocked.

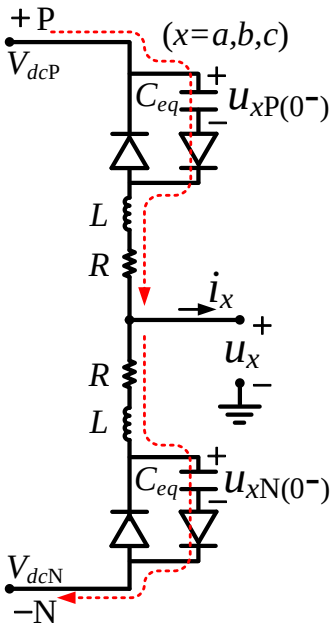


Fig. 5. 7. Single-phase equivalent circuit of a blocked HB MMC.

As aforementioned, the sum of the voltages of all SM capacitors in each arm approximately equal to V_{dc} in normal operation. Therefore, $u_{x\mathrm{P}(0\text{-})}$ and $u_{x\mathrm{N}(0\text{-})}$ are approximately equal to V_{dc}. Take an SPG fault in phase *A* as an example, u_a will be zero, and the magnitudes of $V_{dc\mathrm{P}}$ and $-V_{dc\mathrm{N}}$ are normally lower than the pole-to-pole voltage V_{dc} even through the dc pole voltages are oscillating as a result of the fault. Thereafter, equations (5.7) and (5.8) will not be satisfied in phase *A*. SM capacitors in the faulted phase will not be charged and will remain constant after being blocked.

For the two non-faulted phases, the phase voltages will increase to line voltages and the dc pole voltages will oscillate, according to equations (5.7) and (5.8). The upper arm SM capacitors can be charged during the negative part of u_x and the lower arm SM capacitors can be charged during the positive part of u_x. Therefore, the faster the fault is isolated, the lower the voltage will increase.

It should be mentioned that if the sending end converter is not blocked or switched to a static synchronous compensator (STATCOM) mode, the transmitting power will also lead to the increase of the SM capacitor voltages.

Assuming the transmitting power from the sending end is *P* during a time interval Δt, the voltage change of the SM capacitor is ΔV_{SMdc}, one can obtain that

$$P\Delta t = \frac{3}{2}C_{eq}(V_{dc} + \Delta V_{SMdc})^2 - \frac{3}{2}C_{eq}V_{dc}^{\ 2} \tag{5.9}$$

As $\Delta V_{SMdc} << V_{dc}$, the second order items can be ignored. One can obtain from equation (5.9) that

$$\Delta V_{SMdc} = \frac{P\Delta t}{3C_{eq}V_{dc}} \tag{5.10}$$

It can be seen that the higher the transmitting power (P) and the longer time (Δt) to stop transmitting the power, the higher the voltage increase of the SM capacitors will be. Moreover, the currents discharged from the distributed capacitance of the dc line will contribute to the overcharging of the SM capacitors.

According to the above analysis, a protection strategy is proposed and summarised in the following steps:

Step 1: SPG fault detection (the valve-side voltage unbalance and overcurrent or dc terminal overvoltage can be used as the fault criterion);

Step 2: Blocking of IGBTs and opening of the ACCB;

Step 3: The non-faulted converter switches to STATCOM mode;

Step 4: The ACCB is re-closed after clearing the fault;

Step 5: IGBTs are de-blocked and the non-faulted converter switches back to normal operation;

Step 6: Power ramped up and normal operation resumed.

It should be emphasised that the valve-side SPG faults are normally permanent. The system will not re-start immediately once the fault is isolated. Therefore, the post-fault restoration process is proposed, however, it is not conducted in simulations.

5.5 Simulations and analysis

The previous analysis is verified through time-domain simulations in PSCAD/EMTDC.

5.5.1 Base case modelling

A point-to-point symmetrical monopole MMC HVDC link, shown in Fig. 5. 8,

was modelled as the base case. The main parameters of the converter station are based on the INELFE project [9] and listed in Table I. Given that the number of SMs will not affect the control performance under fault conditions, a detailed switching model with 11-levels is implemented to ensure acceptable simulation times. The MMC controllers are shown in Appendix II.

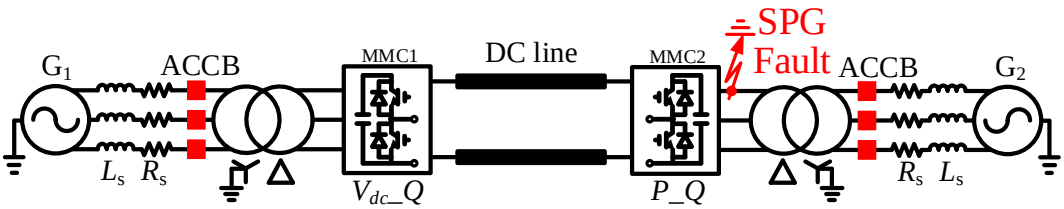


Fig. 5. 8. Schematic diagram of an MMC-HVDC transmission system.

Table 5. 1. Parameters of the test MMC HVDC link.

Parameters	Real value	In per unit
Capacity (MVA)	1050	1
Rated DC voltage (kV)	± 320	1
AC grid frequency (Hz)	50	-
Rated AC voltage (kV)	400	1
Transformer ratio (kV/kV)	333/400	1/1.2012
Transformer leakage reactance (p.u.)	0.18	0.18
Number of SMs in each arm	10	-
SM capacitance (mF)	2.5	-
Arm inductance L (H)	0.05	0.15
Arm resistance R (Ω)	0.1	0.000095
AC system equivalent resistance R_S (Ω)	1.51625	0.014357
AC system equivalent reactor L_S (H)	0.04826	0.14357

MMC1 operates in a dc voltage and reactive power control mode, while MMC2 operates in an active and reactive power control mode. The MMC2 transmits 600 MW and 120 MVar to the ac system. As the fault responses at the power receiving terminal are severer than the power sending terminal, the fault is set on MMC2 at t = 2 s. A fault resistance R_F = 0.1 Ω is assumed. G_1 and G_2 represent the two ac grids

which are modelled as ideal voltage sources with short-circuit impedances represented by L_S and R_S. The X_S/R_S and the short-circuit ratio are assumed as 10. In the base case, the grounding scheme Δ/Yg is employed. Also, a lumped parameter cable model only considering the resistance and reactance (R: 0.0192 Ω/km and L: 0.24 mH/km [5]) of an XLPE cable is used. ACCBs are equipped in the grid-side of the converter transformers.

5.5.2 Influence of converter grounding schemes

Firstly, simulation was performed in the base case, and then different grounding schemes were varied to test the influences on the fault behaviours. The symbols of the valve-side voltages and currents, dc pole voltages and fault current are illustrated in Fig. 5. 9.

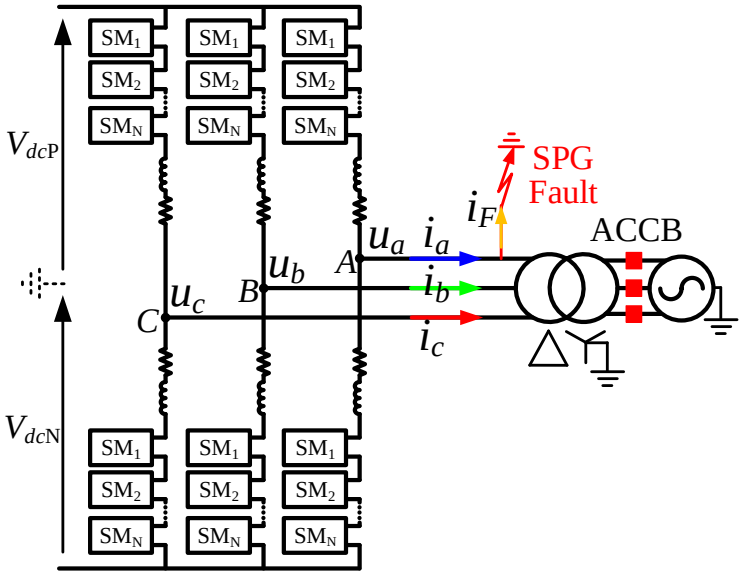
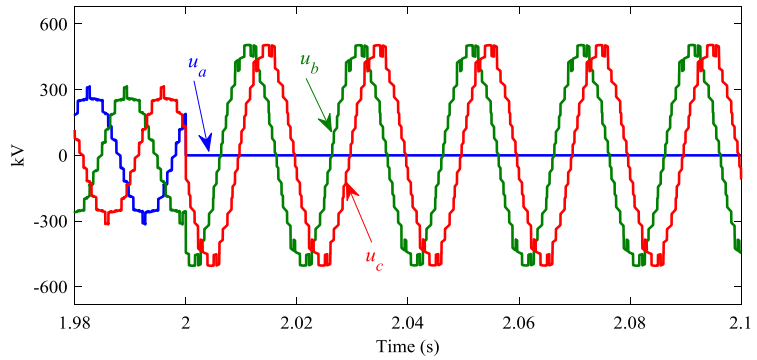
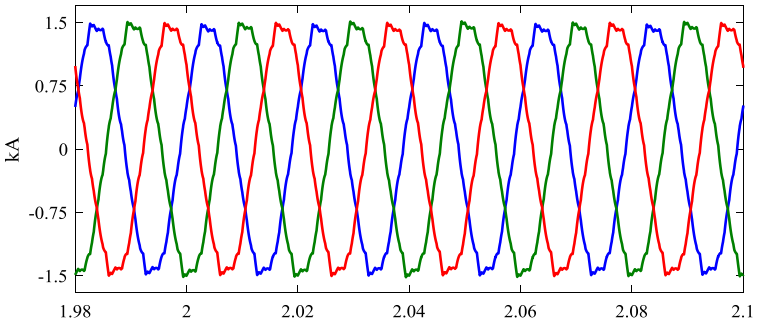


Fig. 5. 9. The illustration of the measurements during the SPG fault.

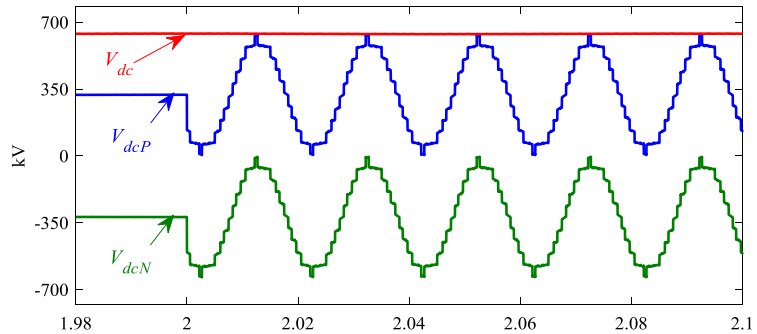
The converter was not blocked during the fault. Fig. 5. 10(a) illustrates that, due to the SPG fault, the valve-side voltage u_a dropped to zero, while the other two phases exhibited line voltage magnitudes. The valve-side output ac currents were not affected by the fault, as shown in Fig. 5. 10(b). It can be seen from Fig. 5. 10(c) that the dc pole voltages V_{dcP} and V_{dcN} started to oscillate sinusoidally with the fundamental frequency and the dc pole-to-pole voltage V_{dc} was not affected. Fig. 5. 10(d) shows the fault current i_F flowed into the ground which was caused by the valve-side small zero-sequence voltages. The fault current was less than 0.6 A, which can be ignored compared to the output ac currents.



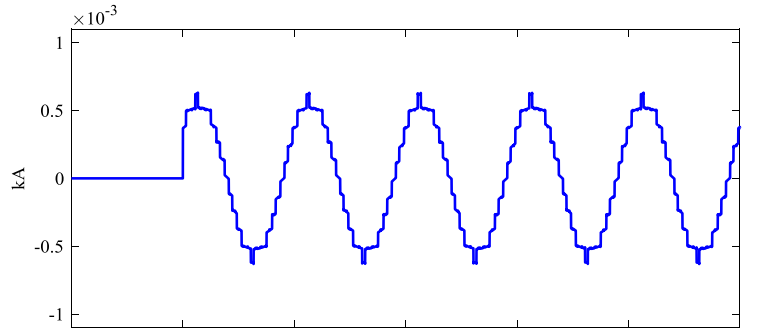
(a) Converter valve-side voltages



(b) Converter valve-side currents i_a, i_b, i_c



(c) Converter dc voltages



(d) Fault current i_F

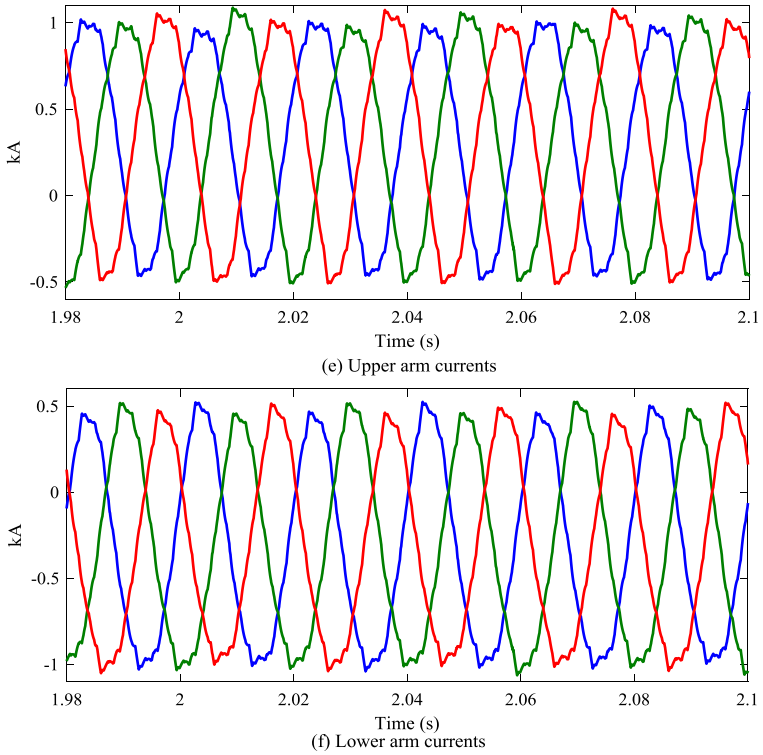


Fig. 5. 10. The base case subject to the valve-side SPG fault.

In order to test the influence of different grounding schemes on the fault responses, the grounding schemes shown in Fig. 5. 5 were employed in the base case model. The reactance and resistance of the scheme shown in Fig. 5. 5(a) were chosen from the INELFE project [9]: 5 H and 5 kΩ. The grounding resistance for both schemes in Fig. 5. 5(b) and Fig. 5. 5(c) was 10 kΩ. The grid-side Y connection of the scheme in Fig. 5. 5(c) was ungrounded. The dc grounding resistance for the scheme in Fig. 5. 5(d) was 50 kΩ. Simulations showed that fault behaviours of the system by changing the grounding schemes were quite similar to the results in Fig. 5. 10. Hence, these results were not duplicated in this section.

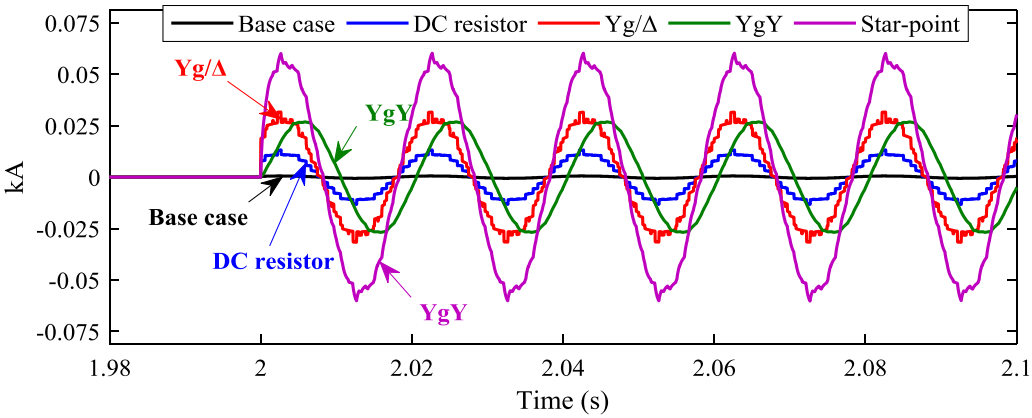


Fig. 5. 11. Fault currents under different grounding schemes.

The fault current i_F under different grounding schemes is illustrated in Fig. 5. 11. The fault current in the base case was zero in that the fault did not create closed current path. The fault current is small (less than 0.013 kA) when the grounding scheme of using dc side resistors was employed. The fault current was caused by the oscillating dc pole voltages which led to the discharging of the dc line distributed capacitors. The fault currents in the cases of using Yg/Δ and YgY were caused by the valve-side zero-sequence voltage during the SPG fault. The currents were less than 0.03 kA which can be reduced if the grounding resistor was increased. The 30˚phase angle between the two currents were due to the different transformer winding connections. The fault current, which was less than 0.06 kA, in case of using start-point reactor and resistor was higher than other cases. The reason is that the equivalent impedance of this ground scheme is lower than other schemes.

It can be concluded that, from the above analysis, different grounding schemes produce little impacts on the fault currents.

5.5.3 Influence of dc lines

In the previous analysis, the effects of dc lines were not considered. In this section, both Frequency Dependent (Phase) cable and overhead lines (OHL) models are applied in the base model to investigate the impacts on the fault behaviours caused by a valve-side SPG fault. The parameters of the cable are from [133] and the parameters of the OHL are from [140]. The segments and conductor details of the cable and OHL models are given in Appendix I.

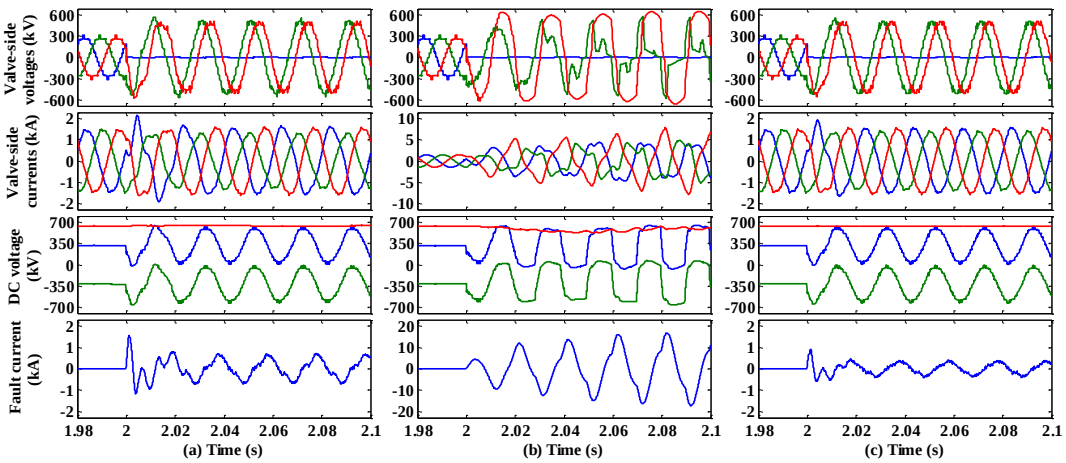


Fig. 5. 12. The effects of dc lines.
(a) 20 km frequency dependent cable model. (b) 200 km frequency dependent cable model. (c) 200 km frequency dependent OHL model.

Fig. 5. 12(a) illustrates the system responses when a 20 km frequency dependent cable model was employed. Comparing to the results in Fig. 5. 10, distortions emerge in the valve-side voltages and currents and dc voltages after the fault. The fault current appeared with a steady-state maximum value of 0.7 kA. As aforementioned, this occurred since the energy stored in the dc line discharged through the distributed capacitors, which was caused by the oscillations in the dc pole voltages.

The system response became significantly worse for the case in Fig. 5. 12(b) when the length of the frequency dependent model was set to 200 km. Since the energy stored in the cable was much greater than the case in Fig. 5. 12(a), the currents discharged from the distributed capacitors had much larger magnitudes. These currents fed into the fault location that produced a large fault current and led to severe distortions in the dc voltages, valve-side voltages and currents. The fault current reached an intolerable level which was higher than 16 kA.

Fig. 5. 12(c) shows the results when a 200 km frequency dependent OHL model was implemented. It can be seen that the fault consequences were much better than the case in Fig. 5. 12(b). This is because the distributed capacitance of an OHL line was much lower than a cable with the same length. Even though the fault current was not quite high and the valve-side line-to-line voltages and ac currents were not impacted severely, the dc pole voltages still oscillated severely.

Due to the severe fault responses, the system is required to be shut down immediately to guarantee safe operations.

5.5.4 Influence of fault resistance

The severity of a fault depends on the value of the fault resistance and on the characteristics of the fault current discharging paths. The lower the fault resistance is, the severer the fault responds. A valve-side fault, for example, an insulation damage, may not be solid grounded but through a fault resistance. The fault resistance can affect fault behaviours. The design of converter protection systems requests the consideration of these situations.

The value of the fault resistance in the cable based model studied in Fig. 5. 12(b) was varied to test the impacts on fault behaviours. Fig. 5. 13(a) depicts the fault

responses with a fault resistance R_F = 10 Ω, which is 100 times of the case studied in Fig. 5. 12(b). It can be seen that the voltage at the faulted phase was no longer zero because the fault current flowed through the fault resistor and produced a voltage drop on it. However, the oscillations and distortions of the voltages at the non-faulted phases were still severe. The magnitudes of the valve-side currents only slightly reduced. The dc pole voltages still oscillated severely. The magnitude of the fault current was reduced, however, still exceeded the acceptable range.

When the fault resistance was increased to 100 Ω, as shown in Fig. 5. 13(b), the severity of the fault responses was alleviated. The valve-side overvoltage and overcurrent were reduced even though they were still unbalanced and contained significant distortions. The oscillations of the dc pole voltages were much lower as a result of the overvoltage of the valve-side voltages. The fault current became less than 3 kA which was much lower than the case in Fig. 5. 13(a).

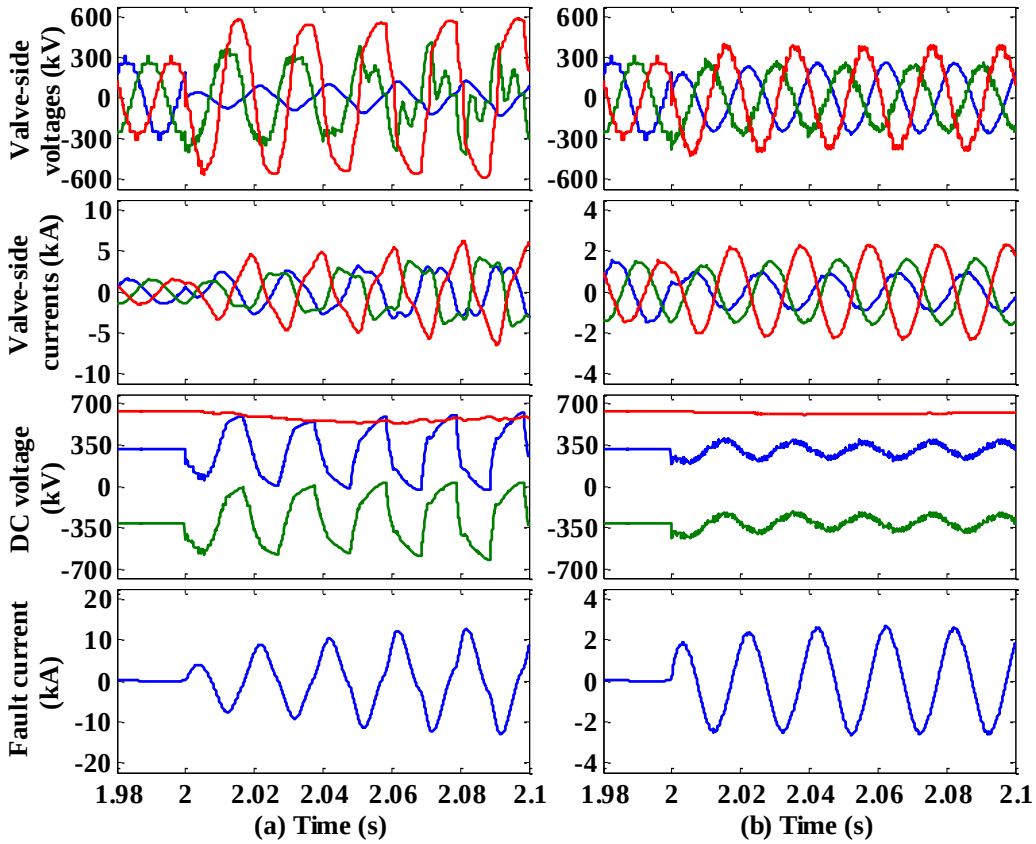


Fig. 5. 13. System responses under different fault resistance.
(a) R_F = 10 Ω. (b) R_F = 100 Ω.

5.5.5 Protection strategy validation

The proposed protection strategy has been applied in both 200 km cable and OHL

based systems. The MMC2 is blocked once the fault currents flow through the IGBTs are above 2 kA. The ACCB at the grid G2 is tripped 80 ms after the fault to emulate the opening time. The simulation results are shown in Fig. 5. 14.

Fig. 5. 14(a) shows system responses in the case of using the 200 km frequency dependent cable model. It can be seen that the magnitudes of the valve-side currents, the dc pole voltage oscillations and the fault current were significantly reduced once the converter was blocked compared to the results in Fig. 5. 12(b), where no action has been taken after the fault. The distortions of the dc voltages were caused by the uncontrollable bridge. It can be seen that the voltages of the SM capacitors in the faulted phase *A* remained constant once the converter was blocked and the SM capacitors in the non-faulted phases were overcharged. The highest overvoltage occurred in the lower arm of phase *B* which reached 1.21 p.u.

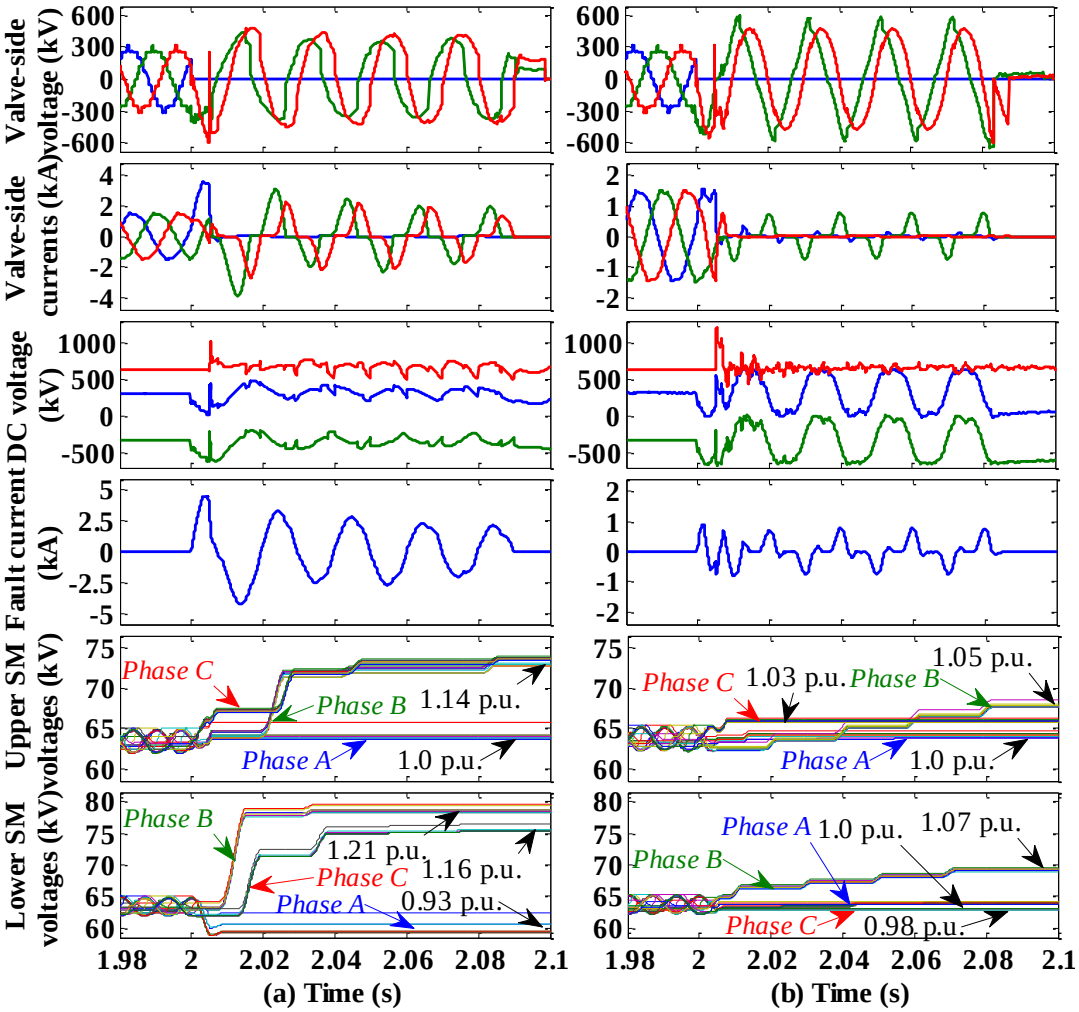


Fig. 5. 14. System responses under the proposed protection strategy.
(a) Cable based model. (b) OHL based model.

In Fig. 5. 14(b), the dc circuit is an OHL. The valve-side voltages and the dc voltages exhibited distortions due to the uncontrollable bridge compared to the results in Fig. 5. 12(b). The valve-side currents were significantly reduced once the converter was blocked. There was still fault current after blocking the converter as the SM capacitors were overcharged. However, the overvoltage of the SM capacitors was less severe than the cable-based system. Therefore, the requirements of SMs' overvoltage capability in OHL based systems can be released than the systems using cables.

5.6 Summary

This chapter investigates fault characteristics during valve-side single-phase faults in symmetrical MMC HVDC stations. Theoretical analysis has been carried out and validated through time-domain simulations in PSCAD. The studies conclude that a valve-side SPG fault will lead to:

1) Valve-side overvoltage at the non-faulted phases;
2) Severe dc pole voltage oscillations;
3) Significant discharging currents from HVDC cable-based systems;
4) SM capacitors overvoltage once the MMC is blocked.

Moreover, the studies show that the grounding schemes of MMCs will negligibly affect the fault behaviours. With the increase of the length of an HVDC line, the fault consequences will be worse. Both a low resistance and a high resistance fault will lead to severe fault consequences.

A protection strategy based on the theoretical analysis and fault characteristics has been proposed for a point-to-point MMC HVDC transmission system. The fault currents and the dc pole voltage oscillations are significantly mitigated through the protection strategy.

Chapter 6

Single-phase Faults at the Valve-side of Asymmetrical and Bipole MMCs

6.1 Introduction

The studies in the last chapter focused on the impact of valve-side single-phase faults on symmetrical monopole HB MMCs. In contrast, valve-side SPG faults will induce special fault behaviours in asymmetrical monopole MMCs. For instance, non-zero-crossing fault currents. Given that an asymmetrical monopole MMC HVDC link is the building block of bipole systems, bipole MMCs will inherit the drawbacks of asymmetrical MMCs.

In this chapter, the fault characteristics of asymmetrical and bipole MMCs are studied. An *LR* parallel circuit is employed to address the issues arising from non-zero-crossing fault currents in asymmetrical and bipole systems. Protection strategies have been proposed for each station configuration based on a thorough theoretical analysis. The analysis is verified by simulations in PSCAD/EMTDC.

6.2 Valve-side single-phase faults in asymmetrical monopole MMC

Fig. 6. 1 shows the topology of an asymmetric monopole HB MMC. There is only one positive pole in the dc terminal and the other pole is grounded.

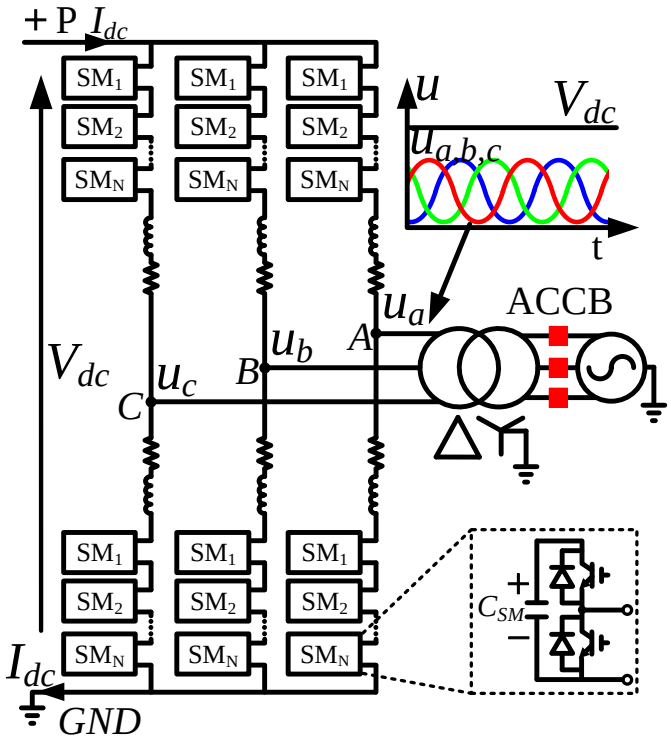


Fig. 6. 1. Converter topology of an asymmetrical monopole HB MMC.

If circulating currents are neglected, according to Fig. 6. 1, the valve-side phase voltages can be expressed as

$$u_x = -\frac{1}{2}L\frac{di_{vx}}{dt} - \frac{1}{2}Ri_{vx} + \frac{u_{xN} - u_{xP}}{2} + \frac{1}{2}V_{dc} \quad (x = a, b, c) \tag{6.1}$$

where u_{xP} and u_{xN} are the voltages produced by SMs in the upper and lower arms. It can be seen that u_x contains a dc component ($1/2V_{dc}$) which makes the valve-side voltages always positive, as illustrated by $u_{a,b,c}$ in Fig. 6. 1. As a result, the converter transformers need to be specially designed to withstand the high voltage stress on the valve-side winds.

Since a Δ/Yg transformer connection is used, the post-fault valve-side voltages are similar to those exhibited by the symmetrical MMC configuration presented in Section 5. However, significant fault currents will be generated due to the converter dc grounding. To protect the system, the IGBTs is requested to be blocked immediately once the fault is detected. The equivalent circuit of a blocked converter during a valve-side SPG fault at phase *A* is shown in Fig. 6. 2. C_{equ} represents the equivalent capacitor of all SM capacitors in each arm.

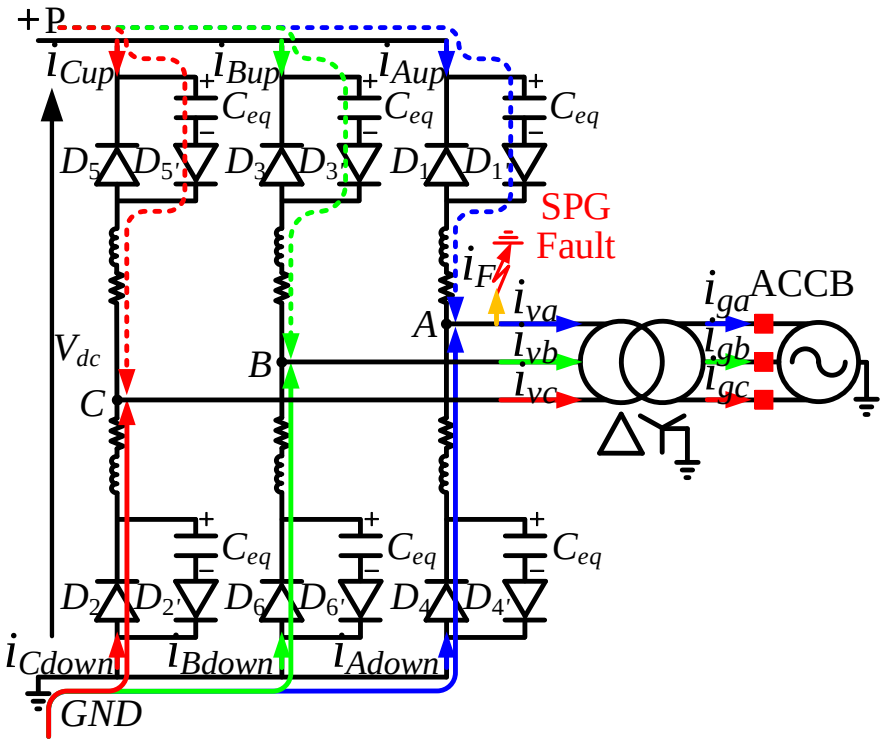


Fig. 6. 2. Equivalent circuit of a blocked asymmetrical monopole HB MMC.

6.2.1 Overvoltage in upper arm SM capacitors

Post-fault equivalent circuit of the faulted phase *A* is illustrated in Fig. 6. 3. As shown in the figure, an SPG fault results in a new zero potential reference. Due to their forward-bias characteristic, diodes D_1 and $D_{4'}$ will become reverse-biased once the converter is blocked. Because of the arm reactor, D_4 will be reverse-biased until the transient current i_{Adown} decays to zero. The upper arm capacitors in phase *A* will be charged through $D_{1'}$ as a result of the dc side transient overvoltage caused by the fault. $D_{1'}$ will be reverse-biased once the capacitor voltage u_{AP} is equal to or higher than V_{dc}. Then, u_{AP} will remain constant.

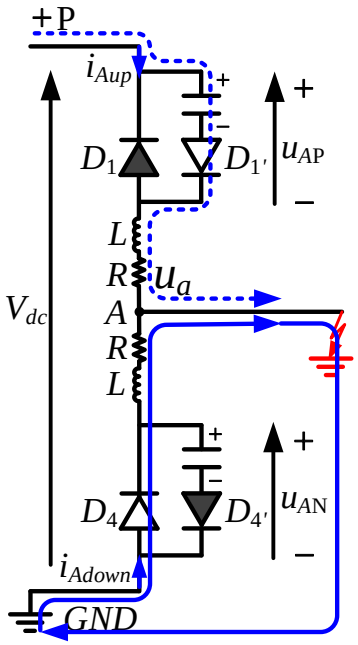


Fig. 6. 3. Post-fault equivalent circuit of phase *A*.

Post-fault equivalent circuits of the non-faulted phase *B* is illustrated in Fig. 6. 4. The analysis presented for phase *B* also applies to phase *C*. The L_{equ} in Fig. 6. 4 is the total equivalent reactance of the transformer and the grid side reactance referred to the valve-side. The ac source represents the transformer's post-fault voltage u_{vb}. D_3 and $D_{6'}$ will be reverse-biased since both the dc voltage V_{dc} and the capacitor voltage u_{BN} encounter a higher magnitude than u_b. However, $D_{3'}$ and D_6 will conduct during every negative half-cycle of u_b. If the arm resistance is neglected, u_b can be estimated by:

$$u_b \approx u_{vb} \times L/(L+L_{equ}) \tag{6.2}$$

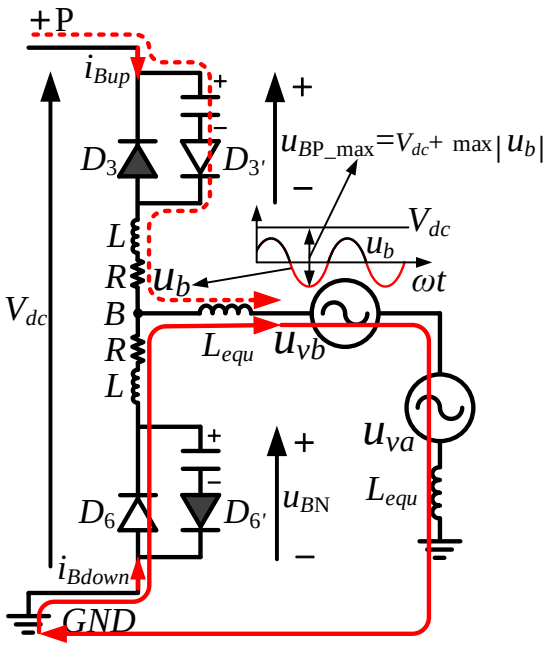


Fig. 6. 4. Post-fault equivalent circuit of phase *B*.

The upper arm capacitor will stop charging once

$$u_{BP\_max} = V_{dc} + \max |u_b|. \tag{6.3}$$

According to (6.3), the voltage increase is given by the amplitude of the post-fault voltage u_b. Hence, in steady-state, all upper arm capacitors will be overcharged and no more current will flow through the upper arms.

It can be seen from (6.2) and (6.3) that the upper arm overvoltage in non-faulted phases is dependent on system parameters. For instance, a small arm reactor or a large transformer leakage reactor will reduce it. However, arm reactors are expected to be large enough to limit the circulating and fault currents. In addition, a large circuit reactance will increase power losses and affect the system dynamic characteristics.

According to (6.3), blocking the MMC that regulates V_{dc} will further reduce the dc voltage and consequently will mitigate the overvoltage. DC overcurrent protection based on fault characteristics can be applied to such MMC so that it is blocked immediately after the local fault detection. Alternatively, choosing a low valve-side voltage for the transformer can mitigate upper arm overvoltage, but this approach may affect the system dynamics in the meantime. It can be concluded that

a comprehensive design that considers not only the system parameters but also the fault characteristics is required.

6.2.2 DC offsets in fault currents

According to Fig. 6. 2, an SPG fault creates closed current paths through the lower arms in non-faulted phases and the converter dc grounding. The lower arms in non-faulted phases will start to conduct large fault currents during the negative half-cycles of the valve-side voltages. Moreover, due to the inductor freewheeling effect, the diode will keep conducting when the positive half-cycles of the valve-side voltage appear. Therefore, there will be instances when the two lower arms in the non-faulted phases conduct at the same time. The resistance in the current path affects the duration of the inductor freewheeling. As analysed in the Appendix V, the current will keep conducting in both the positive and negative voltages if the resistance is ignored. The following analysis is based on this phenomenon.

The equivalent circuit illustrated in Fig. 6. 5 is used to analyse the fault currents. The transformer's valve-side and grid side voltages are respectively given by u_{vx} and u_{gx} (with x = a, b, c). The resistors and reactors represent the equivalent resistance and reactance within the circuit. Currents will be positive if they flow in the directions illustrated in the figure.

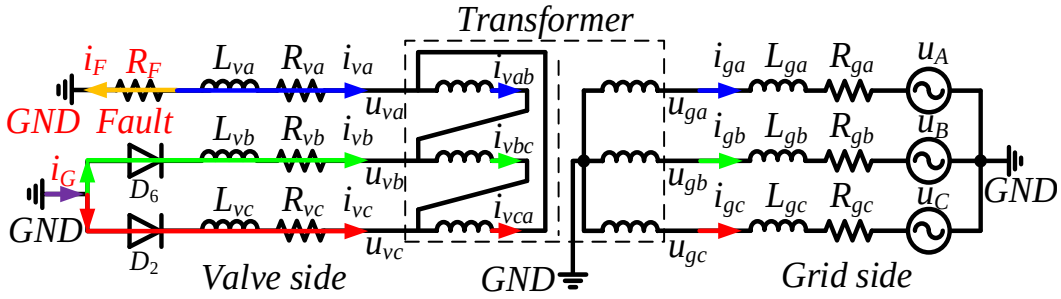


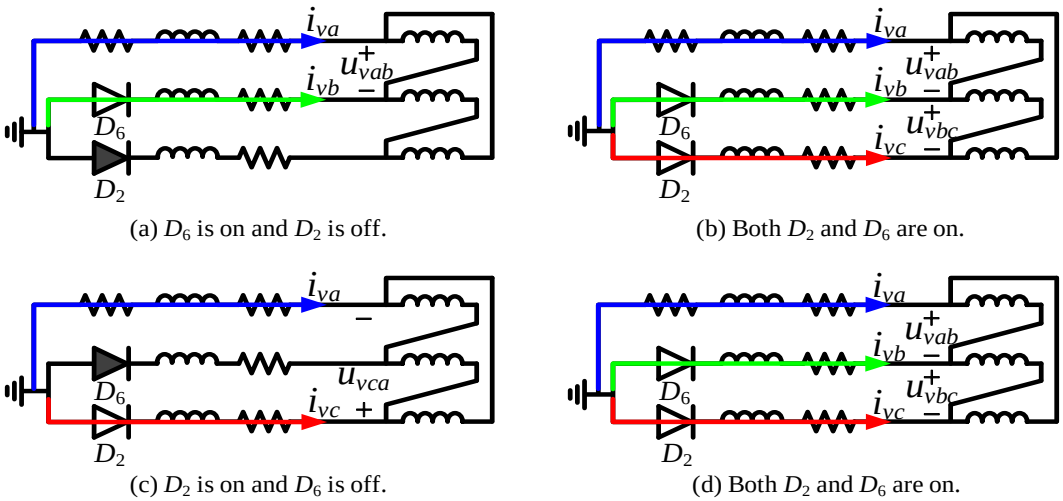
Fig. 6. 5. System equivalent circuit during a valve-side SPG fault in phase *A*.

Recall that there is no zero-sequence current present in the valve-side due to the transformer's delta connection. Thus, the three-phase valve-side currents satisfy:

$$i_{va} + i_{vb} + i_{vc} = 0 \tag{6.4}$$

Due to the forward-bias characteristic of diodes, i_{vb} and i_{vc} will always be positive. Thus, i_{va} will always be negative according to (6.4). This implies that the current in all phases contains dc components.

There will be instances when both D_2 and D_6 conduct due to the reactors within the circuit. Fig. 6. 6 illustrates the diode conducting sequences in the non-faulted phases. The conduction pattern of the lower arm diodes will keep repeating from Fig. 6. 6(a) to Fig. 6. 6(d). There will be instances when both D_2 and D_6 are conducting due to the inductor freewheeling. The conducting modes of D_2 and D_6 are given in Table 6. 1. It is assumed that u_{vb} is negative and u_{vc} positive when the IGBTs are blocked.



(a) D_6 is on and D_2 is off.

(b) Both D_2 and D_6 are on.

(c) D_2 is on and D_6 is off.

(d) Both D_2 and D_6 are on.

Fig. 6. 6. Conducting modes of the lower arm diodes in the non-faulted phases.

Table 6. 1. Conducting modes of the diodes D_2 and D_6.

Conducting modes	**(a)**	**(b)**	**(c)**	**(d)**	**(a)**	**…**
Conducting diode(s)	D_6	D_2&D_6	D_2	D_2&D_6	D_6	…

Given that fault currents flow through first-order *LR* circuits, the decay of transient dc components will be governed by a time constant $\tau = L/R$. In this case, τ is large since the reactance is much greater than the resistance. Therefore, the dc component will not decay considerably during each conducting mode. If the resistance is ignored (see Fig. 6. 7), the circuit will be purely inductive. In steady-state, the diodes in this circuit will always be conducting. The reader is referred to the Appendix V for further details.

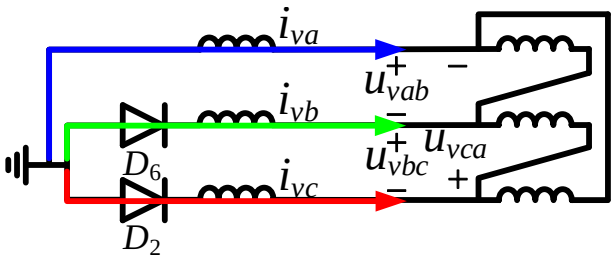


Fig. 6. 7. Equivalent circuit ignoring resistances.

According to Fig. 6. 7, the following expressions are derived:

$$\begin{cases} -L_{va}\dfrac{di_{va}}{dt}+L_{vb}\dfrac{di_{vb}}{dt}=u_{vab} \\ -L_{vb}\dfrac{di_{vb}}{dt}+L_{vc}\dfrac{di_{vc}}{dt}=u_{vbc} \\ -L_{va}\dfrac{di_{va}}{dt}+L_{vc}\dfrac{di_{vc}}{dt}=-u_{vca} \end{cases} \tag{6.5}$$

where u_{vab}, u_{vbc} and u_{vca} are the line voltages, given by

$$\begin{cases} u_{vab}=\sqrt{3}U\sin(\omega t+\varphi) \\ u_{vbc}=\sqrt{3}U\sin(\omega t+\varphi+120^\circ) \\ u_{vca}=\sqrt{3}U\sin(\omega t+\varphi-120^\circ) \end{cases} \tag{6.6}$$

where ω is the system frequency, φ is the initial angle and U is the transformer's valve-side pre-fault peak phase voltage. Differential equations for i_{vb} and i_{vc} can be obtained from (6.5):

$$\begin{cases} \dfrac{di_{vb}}{dt}=\dfrac{(L_{va}+L_{vc})u_{vab}+L_{va}u_{vca}}{L_{va}L_{vb}+L_{va}L_{vc}+L_{vb}L_{vc}} \\ \dfrac{di_{vc}}{dt}=-\dfrac{L_{va}u_{vab}+(L_{va}+L_{vb})u_{vca}}{L_{va}L_{vb}+L_{va}L_{vc}+L_{vb}L_{vc}} \end{cases} \tag{6.7}$$

As shown in Appendix V, an initial condition can be chosen at any moment when the current is zero:

$$\begin{cases} i_{vb}(0^+)=i_{vb}(0^-)=0 \\ i_{vc}(0^+)=i_{vc}(0^-)=0 \end{cases} \tag{6.8}$$

According to (6.5)-(6.8), i_{vb} and i_{vc} can be derived as follows:

$$\begin{cases} i_{vb}=M_1\left[1-\sin(\omega t+\Phi_1)\right] \\ i_{vc}=M_2\left[\sin(\omega t+\Phi_2)+1\right] \end{cases} \tag{6.9}$$

where M_1, M_2, Φ_1 and Φ_2 are provided in the Appendix V. Thus, current i_{va} can be expressed as:

$$i_{va} = -(i_{vb} + i_{vc}) = -\left\{M_1\left[1 - \sin(\omega t + \Phi_1)\right] + M_2\left[\sin(\omega t + \Phi_2) + 1\right]\right\} \tag{6.10}$$

It can be seen from (6.9) and (6.10) that i_{vb} and i_{vc} are always positive and that i_{va} is always negative. Hence, all valve-side fault currents contain high dc components and do not exhibit zero-crossings. As shown in equation (A4) in Appendix V, the current magnitudes are mainly determined by the transformer's valve-side voltage and circuit reactors.

The currents at both sides of the transformer (Delta lags Star 30°) are related as follows:

$$\begin{cases} i_{va} = \dfrac{\left(i_{ga} - i_{gc}\right)}{\sqrt{3}} \times k \\ i_{vb} = \dfrac{\left(i_{gb} - i_{ga}\right)}{\sqrt{3}} \times k \\ i_{vc} = \dfrac{\left(i_{gc} - i_{gb}\right)}{\sqrt{3}} \times k \end{cases} \tag{6.11}$$

where k is the transformer's turn ratio. Since there is no zero-sequence current in the transformer's grid side, the grid side currents satisfy:

$$i_{ga} + i_{gb} + i_{gc} = 0 \tag{6.12}$$

From (6.11)-(6.12), the grid side currents can be rewritten as

$$\begin{cases} i_{ga} = -\dfrac{(2i_{vb} + i_{vc})}{\sqrt{3}k} \\ i_{gb} = \dfrac{(i_{vb} - i_{vc})}{\sqrt{3}k} \\ i_{gc} = \dfrac{(i_{vb} + 2i_{vc})}{\sqrt{3}k} \end{cases} \tag{6.13}$$

It can be observed from (6.9) and (6.13) that i_{ga} is always negative and i_{gc} is always positive. The dc offset of i_{gb} is given by $(M_1 - M_2)/(\sqrt{3}k)$, which has a small magnitude and hence will not lead to a non-zero-crossing.

The analysis presented in the last two sections shows that a valve-side SPG fault at an asymmetrical HB MMC will cause upper arm overvoltage and large dc offset in currents at both sides of the converter transformer. Due to the absence of zero-crossings, ACCBs will not be capable of interrupting arcs within the parting time of the contactors in real applications.

6.2.3 Protection strategy for valve-side single-phase faults

To limit upper arm overvoltage, the converter needs to be blocked once a fault is detected. At the same time, the voltage-regulating MMC can be blocked using local dc overcurrent protection to reduce the dc side voltage which, in turn, will further assist to reduce the overvoltage.

In order to damp the dc components in fault currents, an *LR* parallel circuit is employed as the converter dc grounding. This is shown in Fig. 6. 8. Resistor R_G will not only damp the dc components during a valve-side SPG fault, but will also limit fault current caused by dc side faults. Inductor L_G will limit the ac components of fault currents and drive the currents into R_G, which will damp the dc components. During normal operation, R_G is bypassed by L_G. In this way, the normal operation will not be affected, and power losses will be avoided.

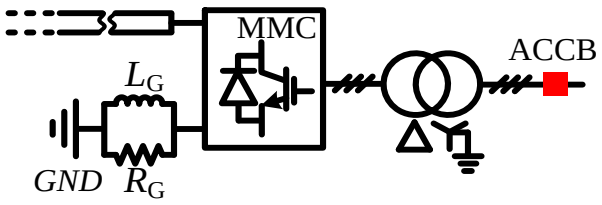


Fig. 6. 8. Asymmetrical MMC equipped with an *LR* parallel grounding circuit.

The selection of a suitable *LR* circuit needs to consider the system parameters such as arm reactors and resistors, transformer impedance, and resistance of switches. The value of R_G will ensure that dc components are damped enough so that zero-crossing currents arise in the grid side. Then, L_G can be selected as low as possible. The *LR* parallel circuit can also be deployed in systems with a metallic return path.

A protection strategy based on the previous analysis is proposed and the main steps in the proposed method are as follows:

Step 1: SPG fault detection (the valve-side voltage unbalance and overcurrent can be used as fault criterion);

Step 2: Blocking of faulted and dc voltage-regulating MMCs;

Step 3: Opening of ACCB once zero-crossings in grid side currents are detected;

Step 4: The non-faulted converter is switched to STATCOM mode;

Step 5: The ACCB is re-closed after clearing the fault;

Step 6: IGBTs are de-blocked and the non-faulted converter switches back to normal operation;

Step 7: Power is ramped up and normal operation is resumed.

It should be emphasised that the valve-side SPG faults are normally permanent. The system will not re-start immediately once the fault is isolated. Therefore, the post-fault restoration process is proposed, however, it is not conducted in simulations.

6.3 Valve-side single-phase faults in bipole MMC

Since bipole systems consist of two symmetrical and independently controlled asymmetrical monopole links, the analysis made in Section 6.2 is applicable. An *LR* parallel circuit can also be used for both bipole systems shown in Fig. 2. 7(c) and Fig. 2. 7(d). However, such an approach encounters one drawback for the bipole systems: transient fault currents caused by both ac and dc side faults will produce a transient voltage on the parallel circuit, which temporarily affects the operation of the healthy pole.

To ensure the security, disconnectors S_p and S_n are installed, as shown in Fig. 6. 9. The disconnector associated with a fault will be tripped once the residual current in reactor L_G decays to zero after tripping the faulted link's grid side ACCB.

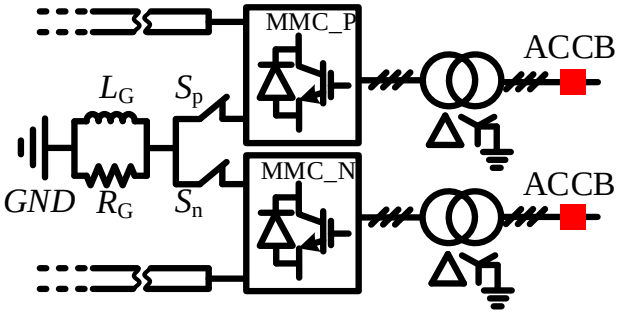


Fig. 6. 9. Bipole MMC system equipped with an *LR* grounding circuit.

The protection strategy for asymmetrical monopole MMC is applicable to bipole systems. The differences are the opening of the disconnector in the faulted pole after opening the ACCB and the re-closure of the disconnector before restoring the converter.

6.4 Simulations and analysis

To verify the analysis presented in the previous sections, the symmetrical monopole and bipole HB MMC based HVDC links have been built in PSCAD/EMTDC, as shown in Fig. 6. 10 and Fig. 6. 11.

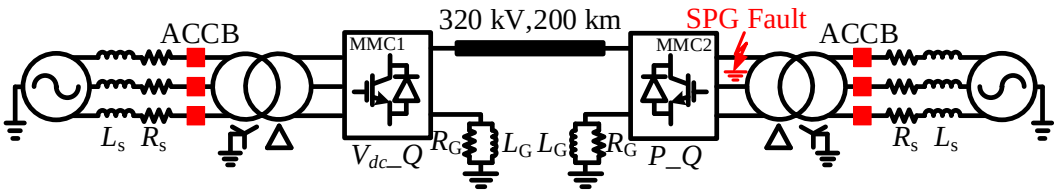


Fig. 6. 10. Asymmetrical monopole MMC link.

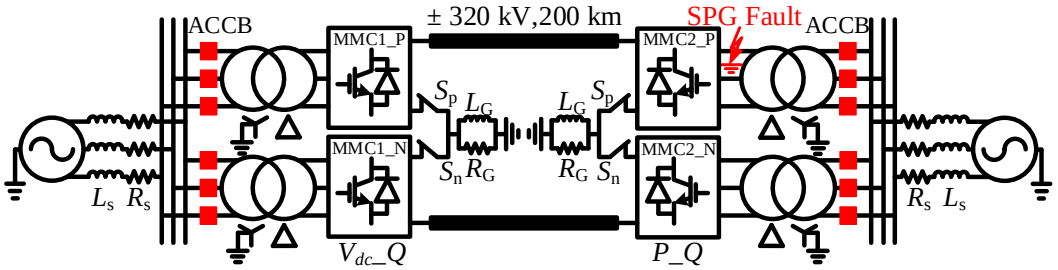


Fig. 6. 11. Bipole MMC link.

Considering that the number of SMs will not affect the equivalent circuit of a converter once it is blocked, a detailed switching model with 11-levels is implemented to ensure acceptable simulation times. The MMC controllers are shown in Appendix II. The bipole system in Fig. 6. 11 consists of two of the asymmetrical links in Fig. 6. 10. The parameters of the systems are given in Table 6. 2.

Since the impact of an SPG fault in power-receiving MMCs is worse than that of dc voltage-regulating MMCs, a valve-side SPG fault at t = 2 s is applied in phase A in the power-receiving MMCs for both topologies. A fault resistance R_F = 0.1 Ω is assumed. The ac systems are modelled as ideal voltage sources with short-circuit impedances formed by L_S and R_S. For all cases, X_S/R_S and the short-circuit ratio are assumed as 10. A frequency dependent dc cable model is used, with parameters

found in [133]. The *LR* parallel circuit with R_G: 5 Ω; L_G: 0.2 H. The MMC2 will be blocked immediately once any arm current exceeds 2 kA. It should be mentioned in most practical applications the asymmetrical monopole is built as one pole of bipole systems, therefore there will be no current during normal operation in the *LR* parallel circuit. Therefore, the inductance of *L* can be large, for example 0.2 H used in this study.

Table 6. 2. Parameters of the test asymmetrical and bipole MMC links.

Parameters	Real value	In per unit
Capacity (MVA)	1000	1
Rated dc voltage (kV)	± 320	1
AC grid frequency (Hz)	50	-
Rated ac gird voltage (kV)	230	1.15
Transformer ratio (kV/kV)	200/230	1/1.15
Transformer leakage reactance (p.u.)	0.1	0.1
Number of SMs in each arm	10	-
SM capacitance (mF)	2.5	-
Arm inductance *L* (H)	0.05	0.15
Arm resistance *R* (Ω)	0.1	0.000095
AC system equivalent resistance R_S (Ω)	1.05275	0.014357
AC system equivalent reactor L_S (H)	0.03351	0.14357

6.4.1 Simulation results of the fault in the asymmetrical monopole

Considering the asymmetrical monopole configuration provided by Fig. 6. 10., Fig. 6. 12 illustrates the fault responses. Currents are positive if they flow in the directions illustrated in Fig. 6. 2.

It can be seen from Fig. 6. 12(a) that the non-faulted phase currents i_{vb} and i_{vc} are always positive. Current i_{va} in the faulted phase is always negative and exhibits a large dc offset. The grid side fault current i_{ga} is always negative, whereas i_{gb} is always positive. As a result, grid side ACCBs are not able to interrupt such fault

currents. The upper arm capacitors start to be charged immediately after the fault. Particularly, the upper arm SM voltages in the non-faulted phases reach 1.19 p.u., but all lower arm SM voltages remain constant once the converter is blocked. The upper arm currents are all positive but become zero once the SM capacitors have been charged to their maximum values. The lower arm current i_{A_down} decays naturally through diode D_4 after the converter has been blocked.

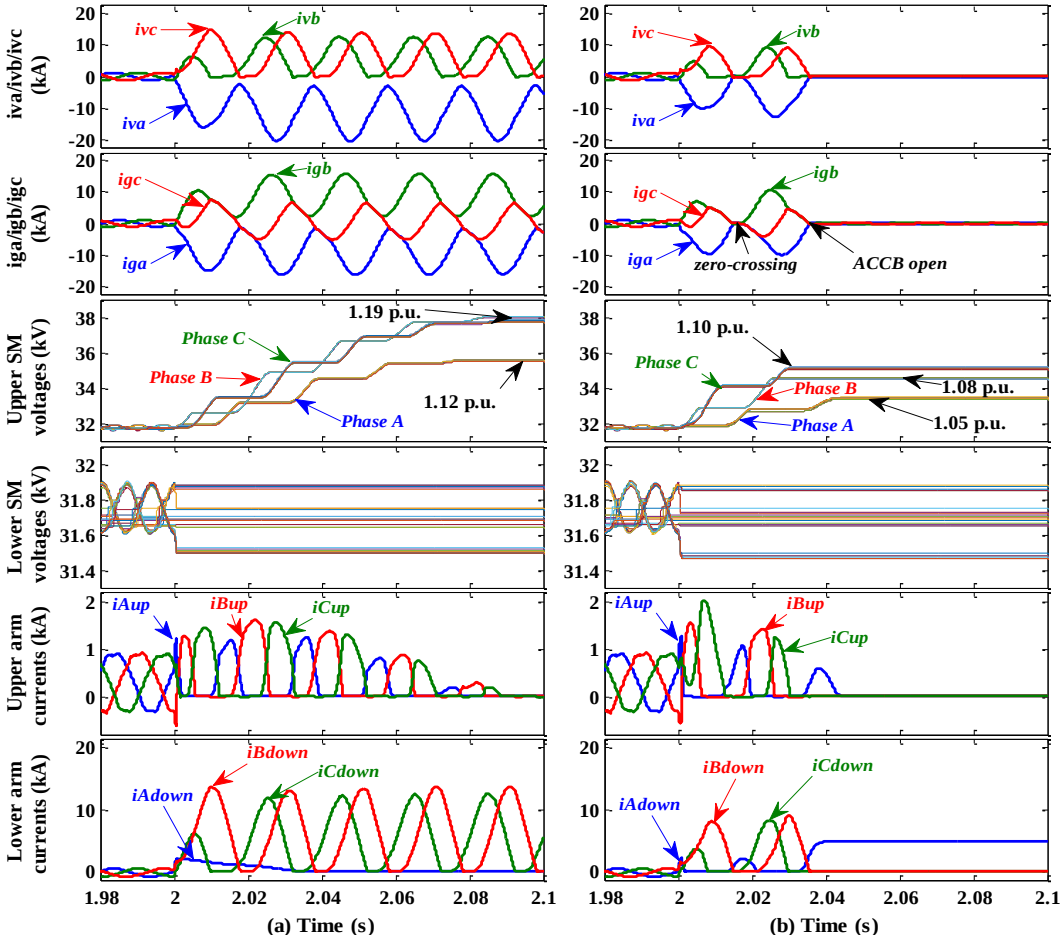


Fig. 6. 12. Fault responses.
(a) The proposed protection strategy is not employed. (b) The proposed protection strategy is employed.

Fig. 6. 12(b) illustrates the results when an *LR* parallel circuit and the proposed protection strategy were applied. It can be seen that fault currents were reduced significantly. More importantly, current zero-crossings appear and, therefore, grid side ACCBs can interrupt the fault quickly. As a result, the maximum overvoltage in the upper arm SM capacitors is reduced to 1.1 p.u. The residual current in the reactor of the *LR* parallel circuit decays naturally through diode D_4 after the grid side ACCBs are tripped.

Fig. 6. 13 compares the steady-state current i_{vc} obtained from the simulation with that analytically calculated for the case when no protection is employed. As it can be observed, no significant difference appears, which, in turn, verifies the theoretical analysis.

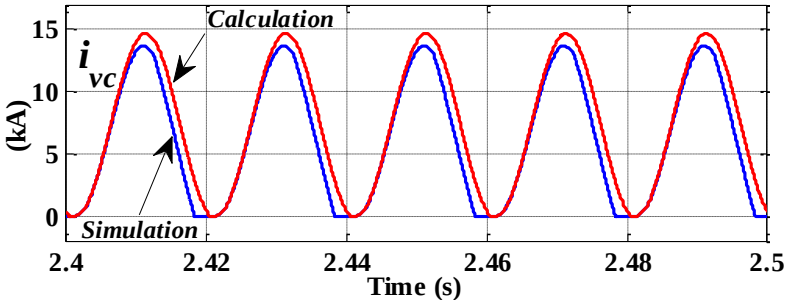


Fig. 6. 13.Simulation and analytical calculation results for i_{vc}.

6.4.2 Simulation results of the fault in the bipole

The *LR* circuit was employed in the bipole system shown in Fig. 6. 11. The fault responses of the faulted pole are similar to those in Fig. 6. 12(a) and hence are not shown. Fig. 6. 14 illustrates that the dc voltage of the healthy pole experiences oscillations. This is a result of the fault current flowing through the *LR* circuit, which produces transient voltages. The operation of the healthy pole is not impacted after the fault transients.

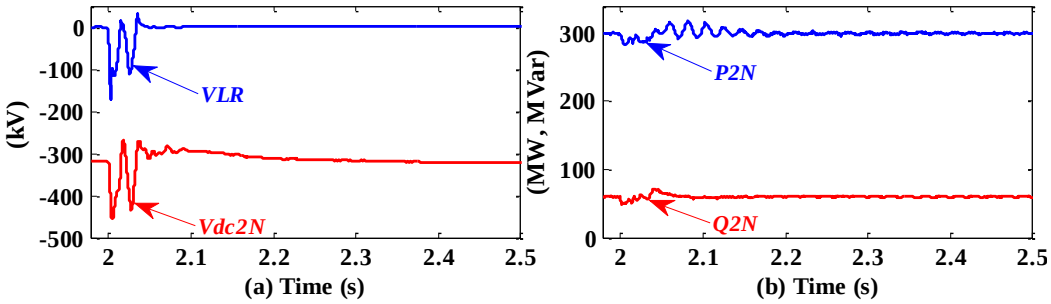


Fig. 6. 14. Responses of the healthy pole.
(a) Negative pole voltage and the voltage on the *LR* circuit. (b) Output power of the healthy pole.

6.5 Summary

In this chapter, the characteristics of valve-side SPG faults in both asymmetrical and bipole MMC systems have been investigated.

The studies presented in the paper show that valve-side SPG faults at asymmetrical and bipole HB-MMCs will produce overvoltage in the upper arm SM

capacitors and non-zero-crossing fault currents at both sides of the interface transformer. To address these issues, the MMC controlling the dc voltage is blocked to mitigate the upper arm overvoltage and an *LR* parallel circuit is employed to create zero-crossings currents so that grid side ACCBs can interrupt the fault.

Chapter 7

Conclusions

7.1 Conclusions

VSC HVDC technology plays an increasingly important role in transmitting bulk power over long distances and integrating renewable energy. However, there are still technical challenges that have to be addressed before this technology becomes a mature and reliable solution. The research work in this thesis investigated the fault behaviour of VSC HVDC systems subject to ac and dc faults.

7.1.1 Application of DCCB in dc grids

Since the resistance dominates the impedance of the dc circuit, a fault in an MTDC grid can be seen from the ac system as simultaneous multi-faults at each of the connection points with the dc grid. DCCB can be an effective solution to isolate dc fault quickly and in a reliable manner. The operating characteristics of DCCBs were studied in Chapter 3. The factors influencing the performance of DCCBs were investigated. Moreover, experimental validation of applying DCCBs in a VSC HVDC grid test-rig was conducted.

The studies show that DCCB's current limiting reactor and the surge arrester are the main factors affecting the performance of interrupting dc fault currents. A large reactor limits the rate-of-change of dc fault current significantly. With a large reactor, the impact of a dc fault on the stability of the overall system is reduced. On the other hand, a large dc reactor increases the time constant of the dc system, which can produce negative effects on the dynamic stability of the dc system. The surge arrester affects the dissipating time of the fault current arc and the transient overvoltage during the current dissipating period. Therefore, it is concluded that the design of the reactor is project specific.

The experimental results show that the DCCBs are capable of isolating a dc fault in a dc grid quickly, and the dc system can recover to the steady state after the fault isolation.

7.1.2 Dynamic interactions of ac and dc grids subject to dc faults

Chapter 4 studied different approaches for clearing a dc fault within a dc grid and the dynamic interactions between the ac and dc grid caused by the dc fault.

There are two alternative solutions for fast clearance of a dc fault when DCCBs are available.

The first solution is based on a Fully Selective Approach and applies the same protection philosophy and principles as used in ac systems. Only the DCCBs associated with the faulted line are tripped. This means that the time is taken for the communications and the fault discrimination logic between fault detection and tripping of the DCCBs.

The second solution is based on the "Open Grid" concept, where each DCCB is allowed to trip autonomously on detection of a fault without fault discrimination and location. The non-faulted line associated breakers are re-closed based on the residual voltage and current of the healthy circuit.

The studies of the two solutions show that the Fully Selective Approach imposes quite a high current interruption duty on the DCCBs associated with the faulted line and will have a greater impact on its connected ac system than the "Open Grid" approach. However, the "Open Grid" will possibly extend the outage area of the dc grid because DCCBs close to the fault can also be tripped. Moreover, the unpredictability of a tripping and/or reclosing sequence will lead to transient overvoltage and overcurrent.

Clearing a dc fault using ACCBs was demonstrated in Chapter 4 as well. The comparatively long fault clearance time associated with this solution leads to the de-energisation of the entire MTDC grid. The overall ac/dc system becomes unstable due to the long fault clearance and restoration time. Therefore, the approach using ACCBs as fault clearing devices seems not suitable in an overlay ac/dc transmission system with the high power supply requirement.

An FB MMC based MTDC grid can achieve fast fault isolation by blocking all the converters. However, this method leads to the outage of the entire dc grid. Moreover, the dc switches need to wait for the decay of the fault currents to acceptable values which can lead to the instability of the overall ac/dc system. In addition, the voltage polarity reversing after blocking all the converters can damage the dc cables. Auxiliary devices, for instance, dc choppers, can be installed in the dc side to consume the residual energy in the dc circuit and therefore reduce the

duration of the power outage. In addition, the high capital costs and operating losses are also drawbacks limiting the applications of FB MMC based MTDC grids.

It can be concluded that each solution has the merits and demerits which needs trade-off according to the requirements of the real applications.

7.1.3 MMC valve-side single-phase faults

The valve-side single-phase faults in MMC stations were studied in Chapters 5 and 6. Three MMC station configurations have been investigated in detail. The theoretical analysis and simulation results show that such a fault in symmetrical monopole HB MMCs will lead to valve-side overvoltage at the non-faulted phases and severe dc pole voltage oscillations. In addition, the energy stored in a long dc line will discharge through its distributed capacitors due to the dc pole voltage oscillations, and thereby result in severe fault currents. As a result, the converter needs to be blocked and the grid side ACCBs is tripped to protect the system.

The valve-side single-phase faults at asymmetrical and bipole HB MMCs will cause overvoltage in the upper arm SM capacitors and non-zero-crossing fault currents at both sides of the interface transformer. To address these issues, the MMC controlling the dc voltage is blocked to mitigate the upper arm overvoltage and an *LR* parallel circuit is employed to create zero-crossings currents. The grid side ACCBs can interrupt the fault.

The results and analyses presented in the two chapters are valuable for the design of the protection systems for station internal ac grounding faults in MMC HVDC transmission systems.

7.2 Contributions of the research work

The main contributions of this thesis are summarised as follows:

- Studied the factors affecting the operating characteristics of DCCBs through simulations;
- Conducted experimental validation of the effectiveness of utilising DCCB to interrupt dc fault currents in a VSC HVDC test-rig.

- Compared and evaluated different dc fault protection approaches in terms of maximum fault currents, system restoration time and interruption of power supply.
- Investigated the interactions between ac and dc systems when the dc grid subjects to dc faults in terms of the stability of the overall ac/dc system.
- Developed theoretical analysis of the fault behaviours of valve-side single-phase faults in three MMC configurations.
- Proposed protection strategies to mitigate the impacts from the valve-side single-phase fault.

7.3 Future work

The following future work is outlined:

7.3.1 AC and dc systems coordinated protection and control

As concluded in Chapter 4, a dc fault is equivalent to a "multi-fault" to the dc grid connected ac systems. The overall system can be unstable if the dc fault cannot be isolated fast enough. In this thesis, only the dc side protection approaches were analysed. The ac system protection and control will be considered to coordinate with the dc side protection actions. For instance, increase power generation and/or switch off loads once a power injecting converter is blocked. This study will contribute to mitigating the overall impact on the ac/dc system when the system subject to dc faults.

7.3.2 SM capacitor overvoltage caused by the valve-side single-phase faults in symmetrical monopole MMC

In Chapter 5, the studies focused on factors affecting system fault behaviour in terms of dc voltage oscillations, valve-side voltages and fault currents. The issues of SM capacitor overvoltage caused by MMC valve-side single-phase faults were not investigated further. The factors, for instance, converter grid side short-circuit ratio and transformer leakage inductance, can affect the overvoltage will be studied in the future. Protection and/or control strategies to mitigate the overvoltage will be developed.

7.3.3 The valve-side faults in MVDC and LVDC systems

There are more and more researches focusing on the area of medium voltage (MV) and low voltage (LV) dc systems [141]-[143]. The converters in the MVDC and LVDC systems have the risk of suffering valve-side single-phase fault. Therefore, the work in Chapter 5 and 6 can be extended to the areas of MVDC and LVDC systems. As the converter topologies in the MVDC and LVDC systems will differ from the converters used in HVDC systems, such as the cascade three-level NPC used in [142], the fault characteristics can be different from the studies in Chapter 5 and 6. Hence, the protection strategies for the MVDC and LVDC systems will be different from the HVDC system. Therefore, it is worth investigating the valve-side fault in MVDC and LVDC system.

Publications

Publications related to this thesis:

Book chapter:

1. **G. Li**, C. Li and D. V. Hertem, "HVDC technology overview: HVDC Grids for Offshore and Supergrid of the Future," ***Wiley-IEEE Press***, April 2016.

Under review or preparation journal papers:

1. **G. Li**, J. Liang, F. Ma, C. E. Ugalde-Loo and H. Liang, "Analysis of Single-Phase-to-Ground Faults at the Valve Side of HB-MMC in HVDC Converter Stations," ***IEEE Trans. Ind. Electron.*** (**Frist round review finished, waiting for second round review decision**).
2. **G. Li**, Z. Song, J. Liang and C. E. Ugalde-Loo, "Analysis and Protection of MMC-based HVDC Systems under Valve-Side Single-Phase-to-Ground Fault Conditions," **(**Under preparation for submission to ***IEEE Trans. Ind. Electron.*****)**
3. F. Ma, **G. Li** and J. Liang, "A Novel Protection Method for Multi-Terminal MMC-HVDC Systems against Pole-to-Pole DC faults," (Under preparation for submission to ***IEEE Trans. Power Del.***).
4. S. Wang, C. Li, O. Adeuyi, **G. Li**, C. E. Ugalde-Loo and J. Liang, "Coordination of MMCs with Hybrid DC Circuit Breakers for HVDC Grid Protection," ***IEEE Trans. Power Del.*** (**Frist round review finished, waiting for second round review decision**).

Conference papers:

1. **G. Li**, J. Liang, S. Balasubramaniam, T. Joseph and C. E. Ugalde-Loo, "Frontiers of DC Circuit Breakers in HVDC and MVDC systems," in *1st IEEE Conference on Energy Internet and Energy System Integration*, Beijing, China, Nov. 2017.
2. T. Joseph, J. Liang, **G. Li**, A. Moon, K. Smith and J. Yu, "Dynamic Control of MVDC Link Embedded in Distribution Network: Case Study on ANGLE-DC," in *1st IEEE Conference on Energy Internet and Energy System Integration*, Beijing, China, Nov. 2017.
3. **G. Li**, J. Liang, F. Ma, C. E. Ugalde-Loo, H. Liang and H. Li, "Analysis of single-phase-to-ground faults at the valve-side of HB-MMCs in bipole HVDC systems," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, USA, 2017, pp. 2659-2665.

4. **G. Li**, J. Liang, C. E. Ugalde-Loo, P. Coventry Paul, "Impacts of DC circuit breakers on AC/DC system stability subject to DC faults," in *2nd International Conference on HVDC (HVDC 2016)*, Shanghai, China, Oct. 2016.
5. S. Wang, C. Li, O. D. Adeuyi, **G. Li**, C. E. Ugalde-Loo and J. Liang, "Coordination of DC circuit breakers and modular multi-level converters for HVDC grid protection," in *2nd International Conference on HVDC (HVDC 2016)*, Shanghai, China, Oct. 2016.
6. **G. Li**, J. Liang, C. E. Ugalde-Loo, P. Coventry and J. Rimez, "Dynamic interactions of DC and AC grids subject to DC faults," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, Hefei, China, pp. 2627-2633.

Joint publications during the PhD studies:

Peer-reviewed journal papers:

1. L. Zhang, J. Liang, W. Tang, **G. Li**, Y. Cai and W. Sheng, "Converting AC Distribution Lines to DC to Increase Transfer Capacities and DG Penetration," ***IEEE Trans. Smart Grid***, vol. PP, no. 99, pp. 1-1. doi: 10.1109/TSG.2017.2768392
2. G. Yan, S. Duan, S. Zhao, **G. Li**, W. Wu, and H. Li. "Research on the Mechanism of Neutral-point Voltage Fluctuation and Capacitor Voltage Balancing Control Strategy of Three-phase Three-level T-type Inverter." ***Journal of Electrical Engineering & Technology***, vol. 12, no. 6, pp. 2227-2236, Aug. 2017.
3. A. Avinash, **G. Li** and J. Wu, "Performance of an Electrical Distribution Network with Soft Open Point during a Grid Side AC Fault," ***Applied Energy*** (2017). (**Accepted, In Press**).
4. G. Wu, J. Liang, X. Zhou,Y. Li, A. E. Álvarez, **G. Li**, H. Peng and X. Zhang, "Analysis and Design of Vector Control for VSC-HVDC Connected to Weak Grids," ***CSEE Journal of Power and Energy Systems***, vol. 3, no. 2, pp. 115-124, June 2017.
5. A. Avinash, **G. Li**, and J. Wu. "Grid Side Unbalanced Fault Detection using Soft Open Point in an Electrical Distribution Network." ***Energy Procedia***, vol. 105, pp. 2859-2864, May 2017.
6. Y. Zhou, C. Wang, J. Wu, J. Wang, M. Cheng and **G. Li**, "Optimal scheduling of aggregated thermostatically controlled loads with renewable generation in the intraday electricity market," ***Applied Energy***. vol. 188, pp. 456-465. Feb 2017.

7. L. Zhang, W. Tang, J. Liang, **G. Li** and Y. Cai, "Power-Voltage Coordinated Control in Hybrid AC/DC Medium Voltage Distribution Networks based on VSC," ***Proceedings of CSEE***, vol. 36, no. 22, pp.6067- 6075, Nov. 2016.
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1. "Integrated AC/DC transmission system simulation," in *Special Session on Offshore and HVDC Grids in IEEE EnergyCon 2016*, Belgium, April 2016.

Presentations:

1. "Converting AC Distribution Lines to DC to Increase Transfer Capacities and DG Penetration," in *8th HVDC Colloquium*, Cardiff, Sep. 2017.
2. "Dynamic interactions of integrated AC/DC transmission systems subject to DC faults," in *Elia*, Belgium, Dec. 2015.
3. "MTDC Grid for Large-Scale Renewable Energy Transmission in West China 2030-2050" in *China Electric Power Research Institute*, Dec. 2014.
4. "Integrated AC/DC transmission system simulation" in *China Electric Power Research Institute*, Nov. 2014.

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Appendix I

The HVDC cable and the OHL model used in the time domain simulations in this research study are modelled using the Frequency Dependent (Phase) models in PSCAD.

Fig. A. 1 illustrates the parameters, configuration and dimensions of the cable model. Detail cable parameters can be found in [133]. The parameters and arrangement of the OHL are obtained from [140], as shown in Fig. A. 2.

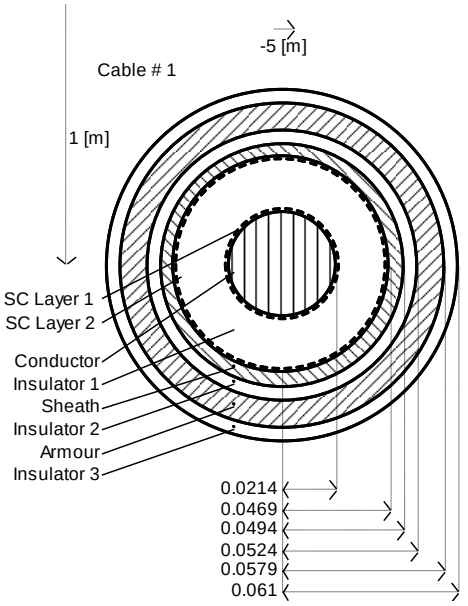


Fig. A. 1 Parameters, configuration and dimensions of the HVDC cable.

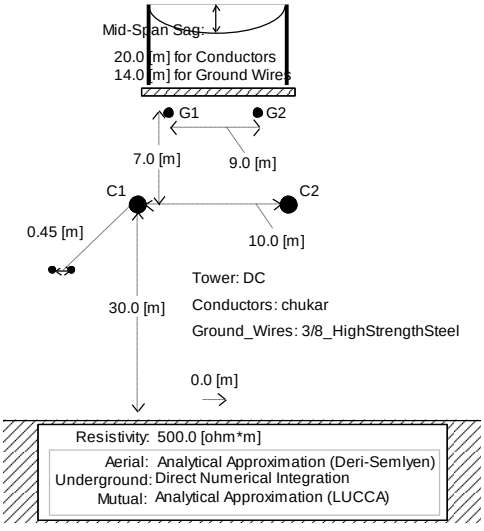


Fig. A. 2 Parameters, configuration and dimensions of the HVDC OHL.

Appendix II

This appendix shows the control systems of the MMCs used in this research work.

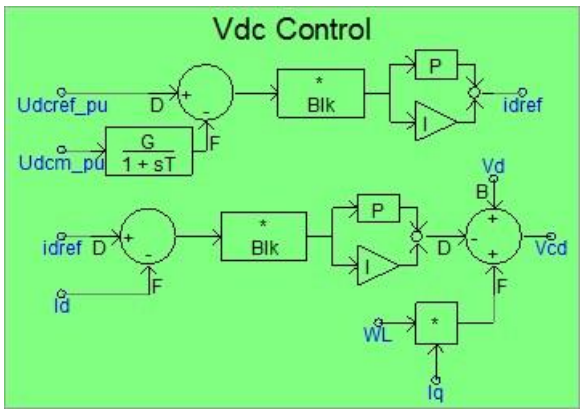


Fig. A. 3. DC voltage controller.

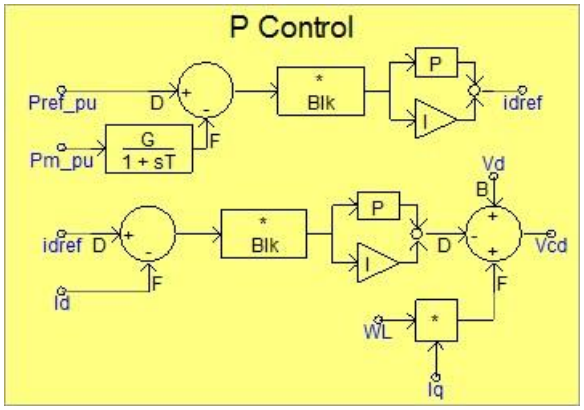


Fig. A. 4. Active power controller.

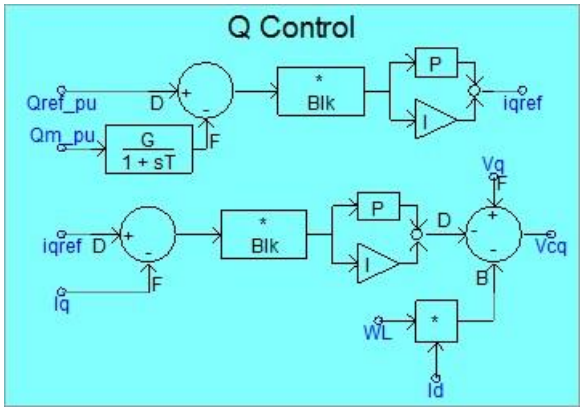


Fig. A. 5. Reactive power controller.

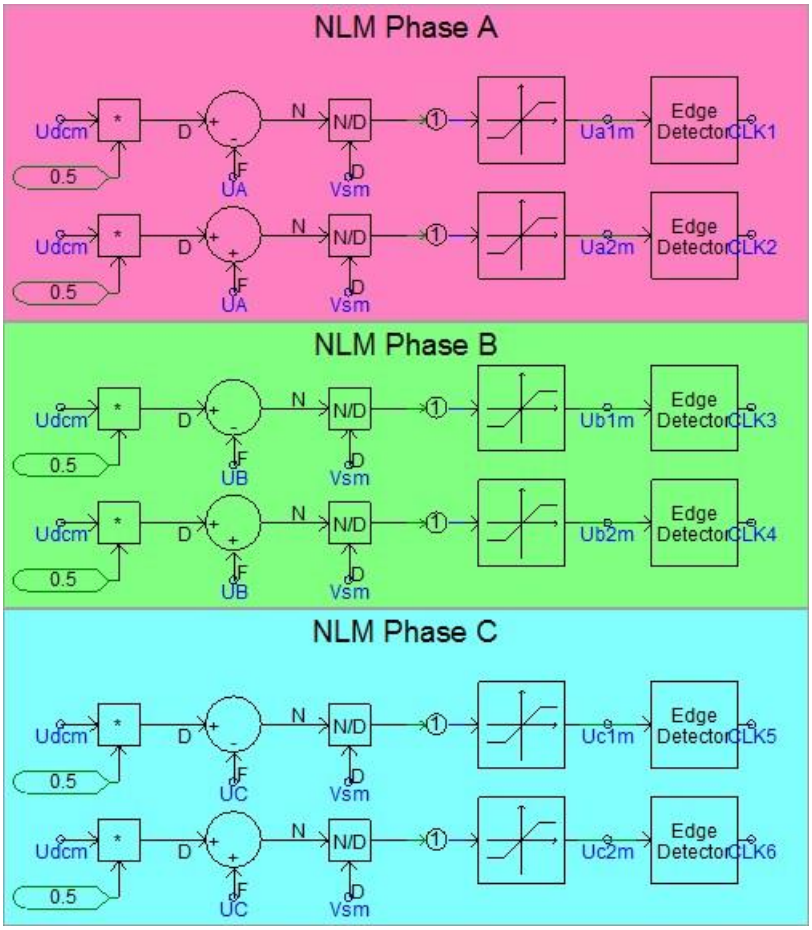


Fig. A. 6. The nearest level modulation.

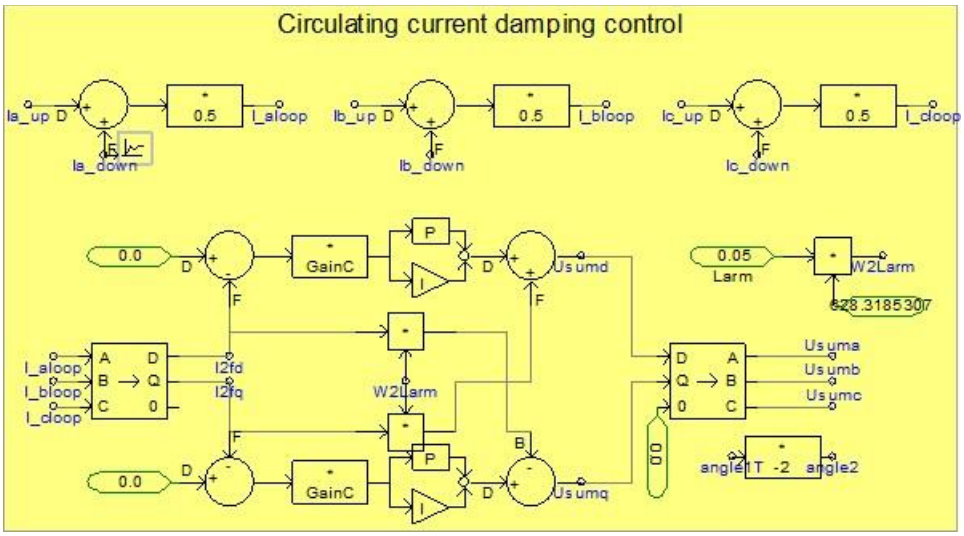


Fig. A. 7. The circulating current damping controller.

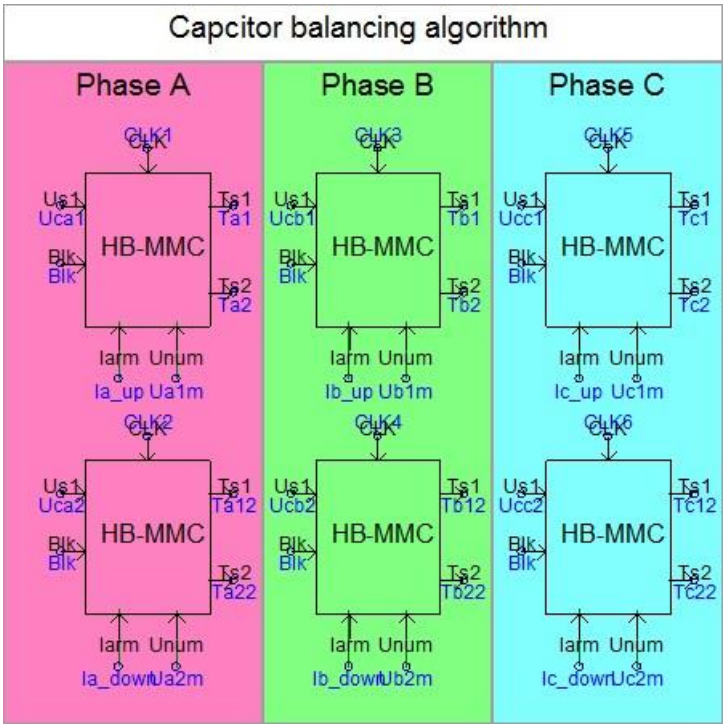


Fig. A. 8. The SM capacity voltage balancing control for HB MMC.

The algorithm in the block shown in Fig. A. 8 are shown as follows:

```
 # LOCAL INTEGER T1(10)
 # LOCAL INTEGER T2(10)
 # LOCAL REAL M(10)
 # LOCAL REAL M1
 # LOCAL REAL N1
 # LOCAL REAL Uk(10)
 # LOCAL REAL Ukk(20)
 # LOCAL REAL NUM

NUM=10

IF ($Blk<0.1) THEN
     DO I=1,NUM
     $Ts1(I)=0
     $Ts2(I)=0
     END DO
ELSE

IF ($CLK>0.9) THEN

 DO I=1,NUM
 Uk(I)=$Us1(I)
 END DO
```

```
 DO K=1,NUM
 Ukk(K)= K
 Ukk(NUM+K)=Uk(K)
 END DO

IF ($Iarm>0) THEN

      DO I=1,NUM-1
       DO J=1,NUM-I
        IF (Ukk(NUM+J)>Ukk(NUM+J+1))THEN
            M1=Ukk(J+1)
            N1=Ukk(NUM+J+1)
            Ukk(J+1)=Ukk(J)
            Ukk(J)=M1
            Ukk(NUM+J+1)=Ukk(NUM+J)
            Ukk(NUM+J)=N1
        END IF
       END DO
      END DO

        DO I=1,NUM
         T1(I)=0
         T2(I)=1
        END DO

        DO I=1,$Unum
         M(I)=Ukk(I)
         T1(M(I))=1
         T2(M(I))=0
        END DO

END IF

IF ($Iarm<0) THEN

      DO I=1,NUM-1
       DO J=1,NUM-I
        IF (Ukk(NUM+J)>Ukk(NUM+J+1))THEN
            M1=Ukk(J+1)
            N1=Ukk(NUM+J+1)
            Ukk(J+1)=Ukk(J)
            Ukk(J)=M1
            Ukk(NUM+J+1)=Ukk(NUM+J)
            Ukk(NUM+J)=N1
        END IF
       END DO
      END DO

        DO I=1,NUM
```

```
          T1(I)=0
          T2(I)=1
        END DO

        DO I=1,$Unum
         M(I)=Ukk(NUM+1-I)
         T1(M(I))=1
         T2(M(I))=0
        END DO

END IF

      DO I=1,NUM
      $Ts1(I)=T1(I)
      $Ts2(I)=T2(I)
      END DO

END IF

END IF
```

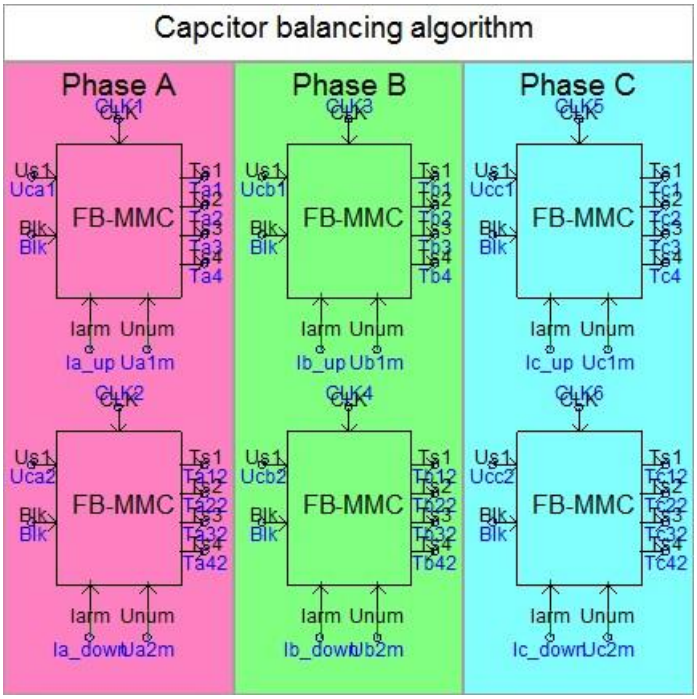


Fig. A. 9. The SM capacity voltage balancing control for FB MMC.

The algorithm in the block shown in Fig. A. 9 are shown as follows:

```
 # LOCAL INTEGER T1(10)
 # LOCAL INTEGER T2(10)
 # LOCAL REAL M(10)
 # LOCAL REAL M1
 # LOCAL REAL N1
 # LOCAL REAL Uk(10)
 # LOCAL REAL Ukk(20)
 # LOCAL REAL NUM

NUM=10

IF ($Blk<0.1) THEN
     DO I=1,NUM
     $Ts1(I)=0
     $Ts2(I)=0
     $Ts3(I)=0
     $Ts4(I)=0
     END DO
ELSE

IF ($CLK>0.9) THEN

 DO I=1,NUM
 Uk(I)=$Us1(I)
```

```
 END DO

 DO K=1,NUM
 Ukk(K)= K
 Ukk(NUM+K)=Uk(K)
 END DO

IF ($Iarm>0) THEN

      DO I=1,NUM-1
       DO J=1,NUM-I
        IF (Ukk(NUM+J)>Ukk(NUM+J+1))THEN
            M1=Ukk(J+1)
            N1=Ukk(NUM+J+1)
            Ukk(J+1)=Ukk(J)
            Ukk(J)=M1
            Ukk(NUM+J+1)=Ukk(NUM+J)
            Ukk(NUM+J)=N1
        END IF
       END DO
      END DO

        DO I=1,NUM
         T1(I)=0
         T2(I)=1
        END DO

        DO I=1,$Unum
         M(I)=Ukk(I)
         T1(M(I))=1
         T2(M(I))=0
        END DO

END IF

IF ($Iarm<0) THEN

      DO I=1,NUM-1
       DO J=1,NUM-I
        IF (Ukk(NUM+J)>Ukk(NUM+J+1))THEN
            M1=Ukk(J+1)
            N1=Ukk(NUM+J+1)
            Ukk(J+1)=Ukk(J)
            Ukk(J)=M1
            Ukk(NUM+J+1)=Ukk(NUM+J)
            Ukk(NUM+J)=N1
        END IF
       END DO
      END DO
```

```
            DO I=1,NUM
             T1(I)=0
             T2(I)=1
            END DO

            DO I=1,$Unum
             M(I)=Ukk(NUM+1-I)
             T1(M(I))=1
             T2(M(I))=0
            END DO

END IF

      DO I=1,NUM
      $Ts1(I)=T1(I)
      $Ts2(I)=T2(I)
      $Ts3(I)=0
      $Ts4(I)=1
      END DO

END IF
```

Appendix III

The steps of the dc fault isolation and post-fault restoration control scheme using ACCBs are proposed as follows:

Step 0) Detecting DC fault;

Step 1) Block the IGBTs of VSCs by converter local protection;

Step 2) Select the potential faulted dc line for the opening of its fast dc switch;

Step 3) Trip ACCBs; A waiting time of 80 ms is used to simulate the ACCB operating time;

Step 4) Wait for the voltage and current of the selected line to decay to zero;

Step 5) Trip the dc switch of the selected faulted line when Step 4) is satisfied;

Step 6) Deblock all converter IGBTs to balance the positive and negative dc voltages; The converter will be blocked again before Step 7);

Step 7) Reclose the ACCBs of the converter operating on V_{dc}_Q control mode;

Step 8) Wait for the dc voltage reach to a pre-set value U_s;

Step 9) Bypass the ac side start-up resistors of the converters operating on V_{dc}_Q control mode; Wait for a short period to protect IGBTs from the inrush currents.

Step 10) Deblock IGBTs of the converter operating on V_{dc} control; Set Q_{ref}=0;

Step 11) Wait the dc voltage reaches to V_{dcref};

Step 12) Reclose ACCBs at other converters connecting with active ac networks; Bypass the start-up resistors of these converters;

Step 13) Deblock converters connecting with active ac networks (P_Q control mode); Set P_{ref}=0, Q_{ref}=0;

Step 14) Deblock all the rest converters connecting with passive ac networks (V_{ac} control mode); Set V_{acref}=0;

Step 15) Power and V_{ac} ramp up;

Step 16) Restoration process complete.

Appendix IV

The results of a 10 Ω fault resistance in the FB MMC dc grid are shown below. The dc switches are tripped once the fault currents decay to below 0.5 kA.

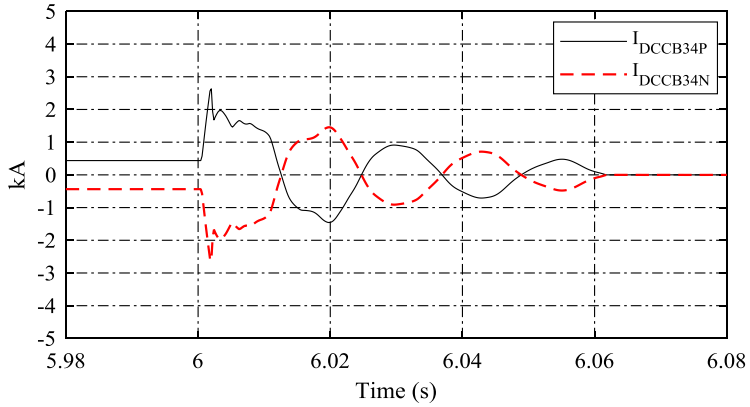


Fig. A. 10. The fault current passing the DCCB34.

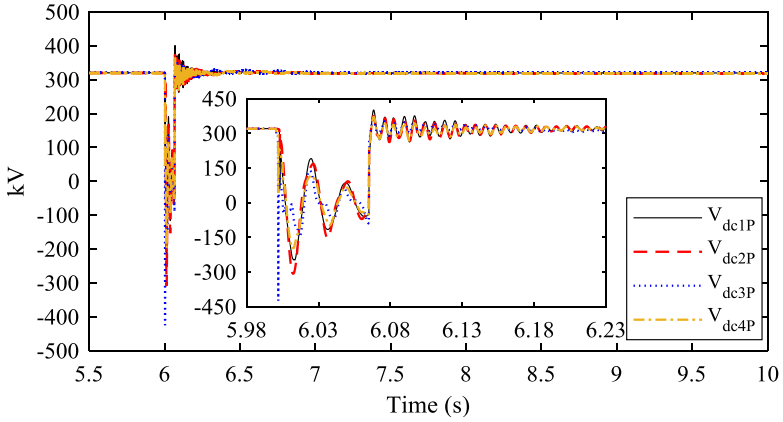


Fig. A. 11. Converter positive dc terminal voltages.

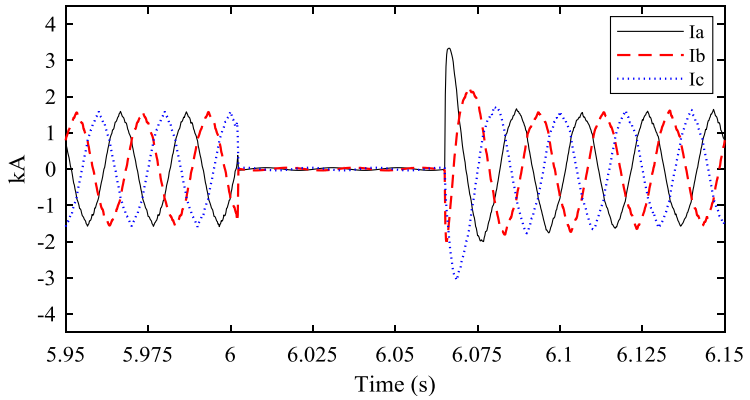


Fig. A. 12. Currents at the grid side of MMC3.

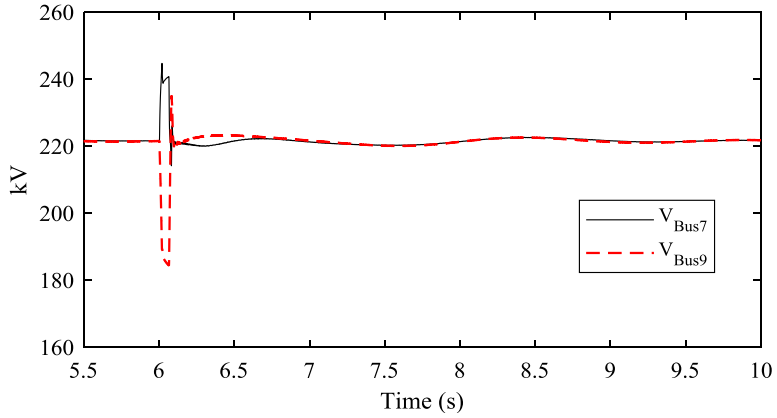


Fig. A. 13. Voltages of ac buses 7 and 9.

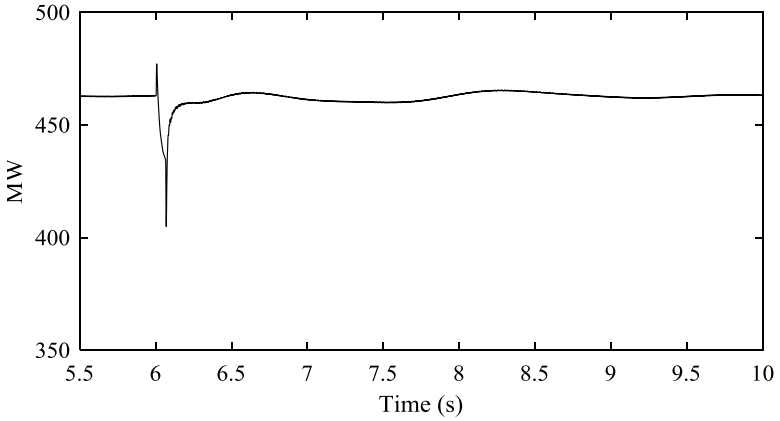


Fig. A. 14. The power in the ac transmission line.

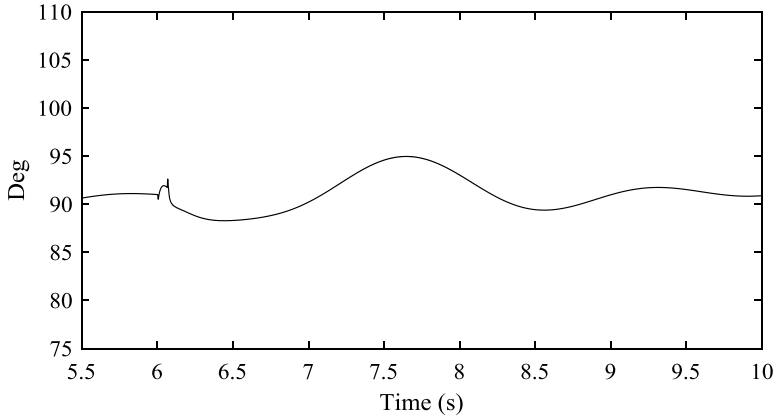


Fig. A. 15. The power angle difference between generators G1 and G3.

Appendix V

Consider a diode in series with an inductor as shown in Fig. A. 16. The current characteristic of this circuit is explained below to derive the coefficients in equation (6.9). The ac voltage is assumed as sinusoidal.

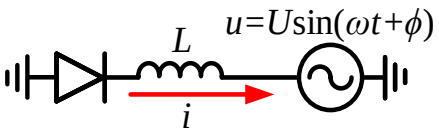
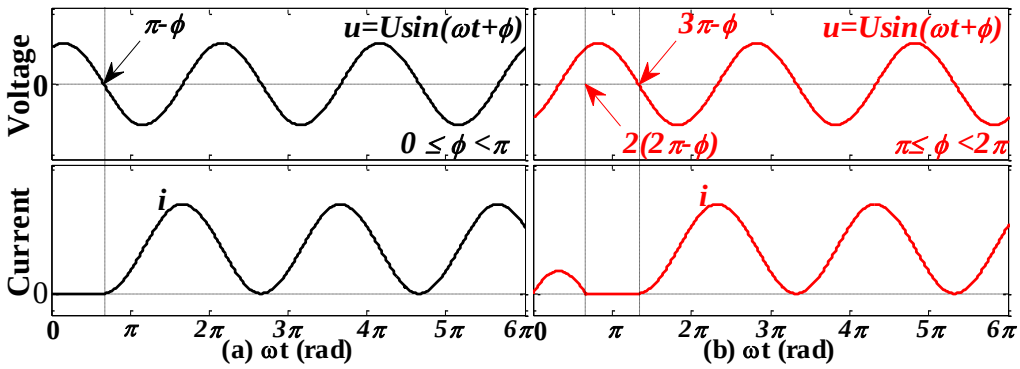


Fig. A. 16. An inductor in series with a diode.

Fig. A. 17 illustrates the voltage and current waveforms in the circuit shown in Fig. A. 16 for ac voltages with different initial phase angles. The diode will conduct from the first negative period if the initial phase angle is $0 \le \phi < \pi$, as shown in Fig. A. 17(a). Current i is expressed as:

$$\begin{cases} i = 0 & , 0 \le \omega t < \pi - \phi \\ i = \dfrac{U}{\omega L}[\cos(\omega t + \phi) + 1], & \pi - \phi \le \omega t \end{cases} \tag{A.1}$$



(a) $0 \le \phi < \pi$. (b) $\pi \le \phi < 2\pi$.

Fig. A. 17. Schematic diagram of the voltage and current waveforms:

It can be seen from (A1) and Fig. A2(a) that the diode will conduct from the first negative period. If the initial phase angle is $\pi \le \phi < 2\pi$, the initial ac voltage will be negative and the diode will conduct immediately from a zero state. However, it will stop conducting early before the next negative period, but will start conducting once the subsequent negative period starts. At this stage, current i can be defined as

$$\begin{cases} i = \dfrac{U}{\omega L}\cos(\omega t+\phi) - \dfrac{U}{\omega L}\cos\phi, & 0 \le \omega t < 2(2\pi-\phi) \\ i = 0, & 2(2\pi-\phi) \le \omega t < 3\pi-\phi \\ i = \dfrac{U}{\omega L}[\cos(\omega t+\phi)+1], & 3\pi-\phi \le \omega t \end{cases} \tag{A.2}$$

It can be seen from (A.1) and (A.2) that the steady-state current will become non-zero-crossing regardless of its initial state. As a result, the diode will remain conducting in steady-state.

According to (6.7), the following expressions can be obtained:

$$\begin{cases} i_{vb} = \dfrac{-\sqrt{3}U\left[(L_{va}+L_{vc})\cos(\omega t+\varphi) + L_{va}\cos(\omega t+\varphi-120^\circ) + \mathrm{C}_1\right]}{(L_{va}L_{vb}+L_{va}L_{vc}+L_{vb}L_{vc})\omega} \\ i_{vc} = \dfrac{\sqrt{3}U\left[L_{va}\cos(\omega t+\varphi) + (L_{va}+L_{vb})\cos(\omega t+\varphi-120^\circ) + \mathrm{C}_2\right]}{(L_{va}L_{vb}+L_{va}L_{vc}+L_{vb}L_{vc})\omega} \end{cases} \tag{A.3}$$

Considering the initial conditions in (6.8), i_{vb} and i_{vc} are given by:

$$\begin{cases} i_{vb} = M_1\left[1-\sin(\omega t+\Phi_1)\right],\ i_{vc} = M_2\left[\sin(\omega t+\Phi_2)+1\right], \\ \text{where } \Phi_1 = \varphi + \arctan\dfrac{L_{va}+2L_{vc}}{\sqrt{3}L_{va}},\ \Phi_2 = \varphi + \arctan\dfrac{L_{va}-L_{vb}}{\sqrt{3}(L_{va}+L_{vb})}, \\ M_1 = \dfrac{\sqrt{3}U\sqrt{\left(\dfrac{\sqrt{3}}{2}L_{va}\right)^2 + \left(\dfrac{1}{2}L_{va}+L_{vc}\right)^2}}{(L_{va}L_{vb}+L_{va}L_{vc}+L_{vb}L_{vc})\omega} = \dfrac{\sqrt{3}U\sqrt{{L_{va}}^2+L_{va}L_{vc}+{L_{vc}}^2}}{(L_{va}L_{vb}+L_{va}L_{vc}+L_{vb}L_{vc})\omega}, \\ M_2 = \dfrac{\sqrt{3}U\sqrt{\left[\dfrac{\sqrt{3}}{2}(L_{la}+L_{lb})\right]^2 + \left[\dfrac{1}{2}(L_{la}-L_{lb})\right]^2}}{(L_{va}L_{vb}+L_{va}L_{vc}+L_{vb}L_{vc})\omega} = \dfrac{\sqrt{3}U\sqrt{{L_{va}}^2+L_{va}L_{vb}+{L_{vb}}^2}}{(L_{va}L_{vb}+L_{va}L_{vc}+L_{vb}L_{vc})\omega} \end{cases} \tag{A.4}$$