



# Monolithically integrated InAs/InGaAs quantum dot photodetectors on silicon substrates

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**Abstract:** We report InAs/InGaAs quantum dot (QD) waveguide photodetectors (PD) monolithically grown on silicon substrates. A high-crystalline quality GaAs-on-Si template was achieved by aspect ratio trapping together with the combined effects of cyclic thermal annealing and strain-balancing layer stacks. An ultra-low dark current of 0.8 nA and an internal responsivity of 0.9 A/W were measured in the O band. We also report, to the best of our knowledge, the first characterization of high-speed performance and the first demonstration of the on-chip photodetection for this QD-on-silicon system. The monolithically integrated waveguide PD shares the same platform as the previously demonstrated micro-ring lasers and can thus be integrated with laser sources for power monitors or amplifiers for pre-amplified receivers.

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**OCIS codes:** (230.5590) Quantum-well, -wire and -dot devices; (230.5160) Photodetectors; (250.5300) Photonic integrated circuits.

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## 1. Introduction

The established silicon (Si) complementary metal-oxide semiconductor (CMOS) technology infrastructure can be leveraged to revolutionize on-chip integration of photonics and electronics with low-cost and high-volume manufacturing capabilities [1–6]. For optoelectronic integrated circuits (OEIC), it is essential to achieve on-chip detection of light with a photodetector (PD) [7,8]. To circumvent the inefficient light absorption from Si and achieve wafer-scale integration of PDs on a Si platform, typically additional material compatible with group IV semiconductor processing is required. Due to the strong linear absorption of Germanium (Ge) up to 1.55  $\mu\text{m}$  and its compatibility with standard CMOS processes, comprehensive work has been conducted using Ge PDs for Si-based photodetection [9,10]. However, the dark current of Ge PDs is much higher than that of their conventional III-V counterparts [11,12] and low responsivity is a problem at wavelengths longer than 1.55  $\mu\text{m}$ . Integration of III-V materials on Si represents a promising alternative to leverage the economies of scale of Si while maintaining the highest efficiency and yield [13,14].

Currently, wafer-bonding based heterogeneous integration has been widely explored by industry to introduce new datacom and telecommunication products with lower cost, higher capacity and performance that have been enabled by integration [15]. However, considering the stringent bonding requirements and the limitation of the maximum bonding size set by the largest available III-V substrates (typically no larger than 150 mm for InP and 200 mm for GaAs), being able to epitaxially grow and thereby monolithically integrate III-V materials onto the Si platform represents an important solution in the long term [16]. In the last few years, the insertion of quantum dot (QD) III-V active regions for both dislocation filtering and as advanced gain material has given rise to high-performance QD devices monolithically grown on Si [17–22]. The overall device performance was rapidly elevated towards that of devices grown on native substrates, and reliable, long term operation is now the focus. By introducing GaAs on V-groove patterned silicon (GoVS) templates using CMOS-compatible, on-axis (001) silicon wafers without offset, our group recently demonstrated 1.3- $\mu\text{m}$  InAs QD micro-cavity lasers under both optical pumping and electrical injection with record-low threshold currents [23,24].

In this paper, we report a monolithically integrated InAs/InGaAs QD waveguide PD and a proof of principle demonstration of laser photodetector integration via free-space coupling developed on the same material platform. We adopted the design of a waveguide p-i-n photodetector that allows for light absorption perpendicular to the current collection, for high-speed, high-efficiency and relatively bias-insensitive operation [25,26]. The PD operates with an internal responsivity of 0.9 A/W in the O-band and a dark current of less than 0.8 nA at a reverse bias of  $-1$  V. Characterization of high-speed performance was also conducted. The 3-dB bandwidth was extracted to be 2.3 GHz considering the combined effects of transit time,

RC response and carrier trapping. To analyze the discrepancy between the RC limited 3-dB bandwidth and the optical-electrical response obtained from the  $S_{12}$  measurement, a thermally activated tunneling model was constructed. The carrier escape mechanisms for both electron and hole in QDs have been investigated, and the hole trapping in the QD is identified to be the main cause for the limitation of device speed. To demonstrate the flexibility of the III-V/Si device platform, a preliminary on-chip detection system was further explored. The measured photocurrent suggests a lasing threshold of around 21 mA for a 50- $\mu\text{m}$  outer-ring radius micro-ring laser, with a mesa width of 4 $\mu\text{m}$ . This successful demonstration of on-chip photodetection via a QD active region illuminates a promising path towards photonic integrated circuits (PIC) on the GoVS material platform.

## 2. Experiments and results

The virtual GaAs-on-Si template was prepared using a V-groove patterned Si substrate by aspect ratio trapping in a metal-organic chemical vapor deposition (MOCVD) system [27,28]. With the combined effects of cyclic thermal annealing and strain-balancing layer stacks, the threading dislocation density has been reduced to  $7 \times 10^7 \text{ cm}^{-2}$ . Molecular beam epitaxy (MBE) was used to grow the epitaxial structure of the p-i-n PD, which is identical to that of the previously demonstrated micro-ring lasers [29], as shown in Fig. 1(a). The active region of the PD consists of seven-stacked InAs dot-in-a-well (DWELL) structures [30], with QD density of  $6 \times 10^{10} \text{ cm}^{-2}$ , as evidenced by the plan-view transmission electron microscopy (TEM) image of one layer of the QDs in Fig. 1(b).

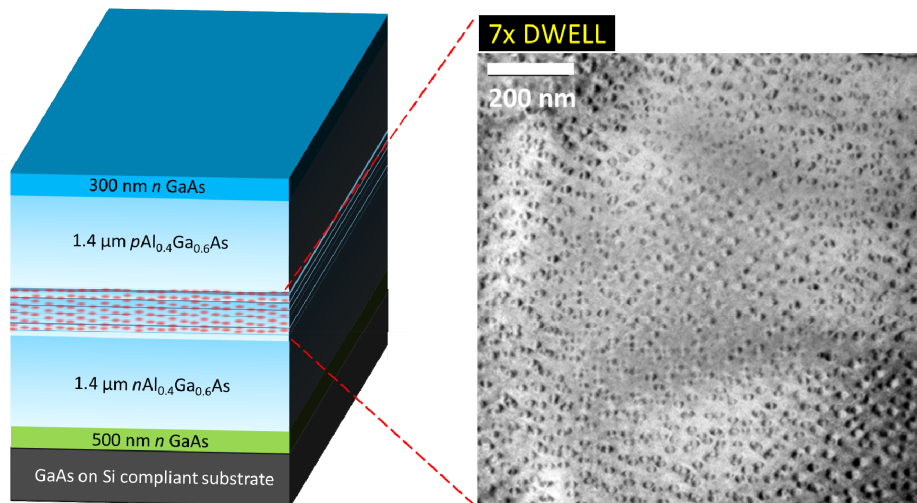


Fig. 1. (a) Epitaxial structure of the epitaxial structure of the p-i-n PD; (b) TEM image of one layer of the QDs.

A rectangular mesa (20- $\mu\text{m}$  in width and 50- $\mu\text{m}$  in length) was defined by inductively coupled plasma (ICP) etching, which stopped at the GaAs  $n$ -contact layer. Pd/Ti/Pd/Au and Pd/Ge/Au layer stacks were deposited by E-beam evaporation to form the  $p$  and  $n$  ohmic contacts. 12-nm atomic-layer deposited (ALD)  $\text{Al}_2\text{O}_3$  together with a 1  $\mu\text{m}$ -thick sputtered  $\text{SiO}_2$  layer were used as the passivation layer to help suppress the dark current. After via opening, 1.5  $\mu\text{m}$ -thick Ti/Au was deposited to form ground-signal-ground (GSG) pads for measurement. The facet of the PD was diced and polished, with no additional application of an anti-reflection coating. A schematic representation of the PD fabricated on the GoVS template is shown in Fig. 2(a). In Fig. 2(b) and (c), top-view and 90° tilted cross-sectional view scanning electron microscope (SEM) images of a fabricated device are presented.

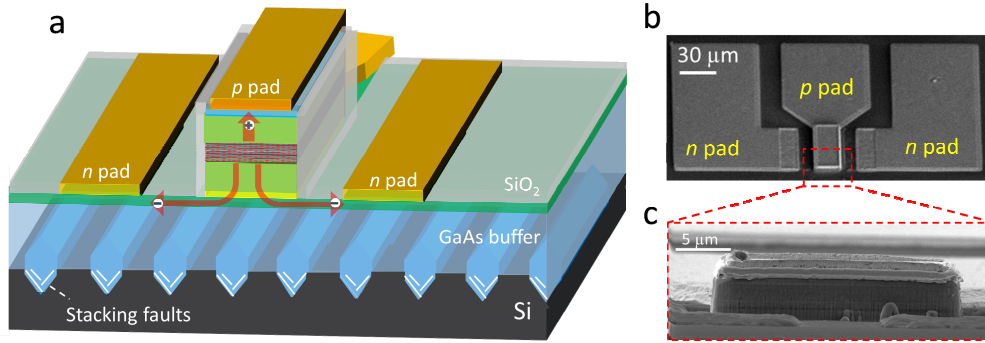


Fig. 2. (a) Schematic plot of the PD fabricated on the GoVS template; (b) top-view and (c) cross-sectional view SEM images of a fabricated device.

Without any illumination, the typical current-voltage (I-V) characteristics for the rectangular photodiode of 20  $\mu\text{m}$  in width and 50  $\mu\text{m}$  in length has been recorded in Fig. 3(a). The measured dark current is within the range from 0.1 nA to 20 nA with a bias from  $-1$  V to  $-5$  V. A zoomed-in view of the I-V characteristics is presented in Fig. 3(b). For bias voltages of  $-1$  V, the dark current was as low as 0.8 nA, corresponding to  $\sim 0.08$  mA/cm<sup>2</sup> dark current density. This value is two orders of magnitude lower than the competing Ge-on-Si PDs with thin Ge or SiGe buffer layers (typically in the order of 10 mA/cm<sup>2</sup>) [9]. The dark current includes diffusion current, generation-recombination current, tunneling current and surface leakage current. Since these current components are closely related to the material and junction quality, the ultra-low value obtained for the PD indicates the high-crystalline quality of the III-V/Si epitaxial materials, and is also attributed to the low dislocation density, shorter diffusion lengths, and good sidewall passivation.

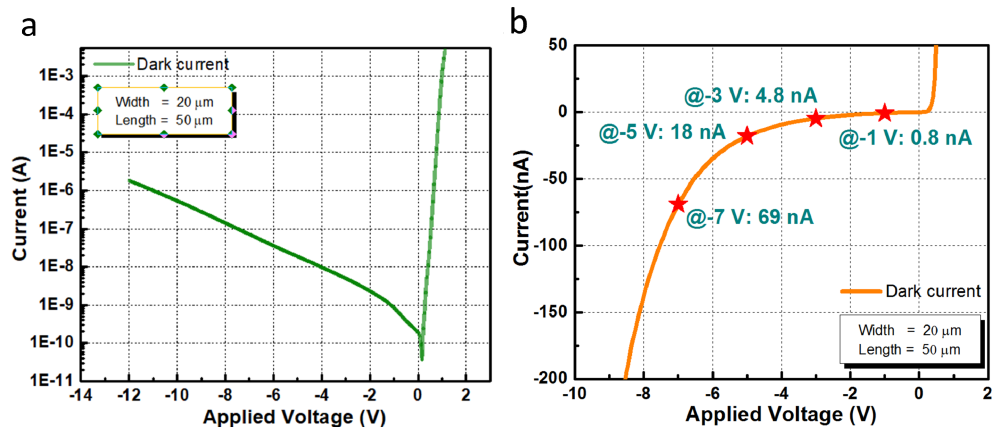


Fig. 3. (a) full-scale and (b) zoomed-in scale of the I-V curve without light input for a rectangular photodiode of 20  $\mu\text{m}$  in width and 50  $\mu\text{m}$  in length.

To measure the responsivity, light from a 1.3  $\mu\text{m}$  laser source was coupled into the polished PD facet using a lensed fiber. The input polarization is controlled by a polarization controller. The incident photons absorbed in the InAs/InGaAs QDs generate electron-hole pairs that are subsequently collected via the applied reverse biased electric field. Responsivity is obtained by dividing the photo-generated current by the incident optical power. The spectral response with different voltage bias is shown in Fig. 4(a). Fiber coupled responsivity values in excess of 0.3 A/W were obtained in the 1240-1340 nm spectral range. The responsivity as a function of reverse bias is presented in Fig. 4(b). When applied with a higher reverse bias, the edge of the spectral response is redshifted since the applied electric field

increases the photon absorption at longer wavelengths [31]. The measured responsivity at 1250 nm is  $\sim 0.33$  A/W, and is roughly constant over a range of bias conditions from  $-1$  V to  $-6$  V. Taking into consideration the  $\sim 30\%$  reflection off the waveguide facet and an estimated 3 dB coupling loss, the PD responsivity was estimated to be  $\sim 0.94$  A/W, comparable to the  $\sim 1$  A/W responsivity of high quality Ge on SOI waveguide PDs [32]. The extracted internal responsivity ( $0.9$  A/W) corresponds to 90% internal efficiency.

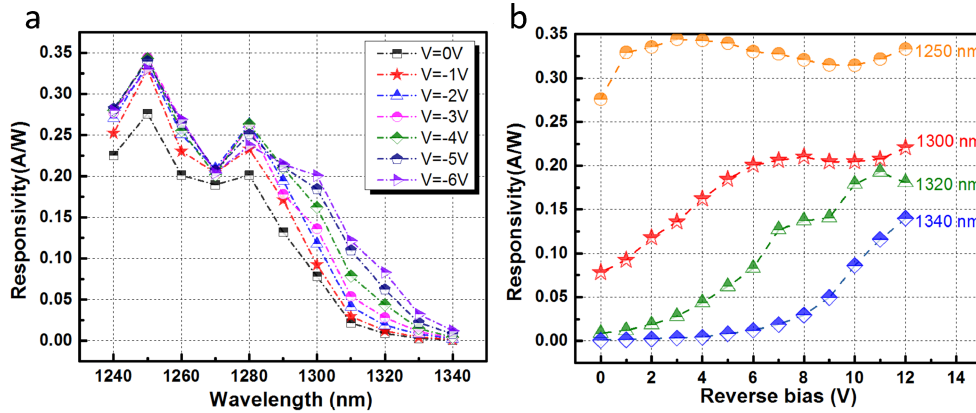


Fig. 4. (a) Spectral response at different voltage biases; (b) responsivity as a function of reverse bias in the O band for a rectangular photodiode of 20  $\mu\text{m}$  in width and 50  $\mu\text{m}$  in length.

The high-speed performance of the PD was characterized at 1550 nm by a lightwave component analyzer (LCA). The electrical characteristics of the PD can be described by the quasi-static circuit model shown in Fig. 5(a). The circuit parameters were de-embedded from IV characteristics as well as the electrical reflection ( $S_{22}$ ) measurement. The procedure for parameter extraction closely follows the one described in [33], in which the equivalent resistance of the photocurrent source  $R_p$  was obtained from the slope of the IV curve under reverse bias; the junction capacitance  $C_j$  and the series resistance  $R_{sm}$  were obtained from the imaginary and real part of the calculated load impedance at high frequency. The values of the circuit parameters are summarized in Fig. 5(b). The validity of the extracted values can be seen from the good agreement between the measured and modeled traces on the Smith chart in Fig. 5(c).

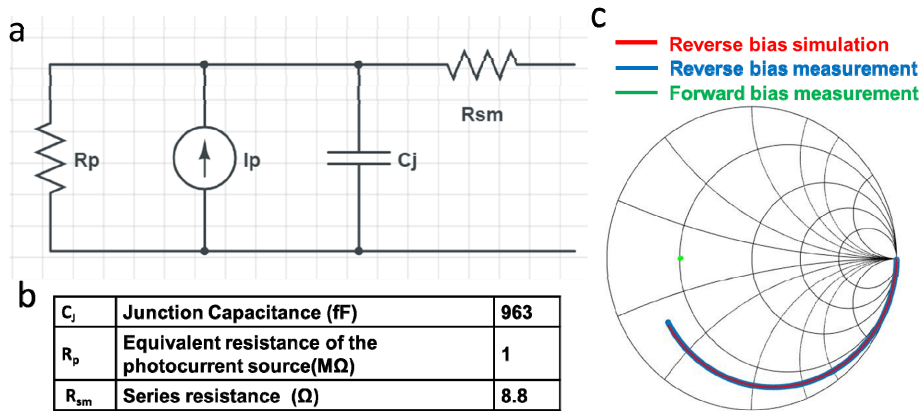


Fig. 5. (a) The small signal equivalent circuit used to extract series resistance and capacitance from the PD; (b) the extracted series resistance and capacitance of the device; (c) fitting results of the Smith chart.

Using the circuit parameter values, the RC limited 3-dB bandwidth was calculated to be  $\sim 2.9$  GHz, as shown in the red curve in Fig. 6(a). However, the optical-electrical (OE) response obtained from the  $S_{12}$  measurement of the LCA (the blue dots in Fig. 6(a)) shows a device 3-dB bandwidth of roughly 2.3 GHz. The discrepancy is attributed to the carrier trapping effect of the QDs. In GaInAs/InP p-i-n photodiodes, hole trapping at the intrinsic GaInAs and p-doped InP hetero-barrier has been reported to slow down the device [34]. In the InAs/GaAs QD devices, carrier escape mechanisms for both electron and hole in QD have been studied [35,36]. It is found that in these devices, carriers escape the QD by thermally activated tunneling, with the nuance that electron tunneling relies on excited QD state as intermediate state whereas for hole the intermediate state is the wetting layer state. To estimate the carrier escape rate from the QD, we used the thermally activated tunneling model described in [35]:

$$\frac{1}{\tau_{tot}} \cong \frac{\hbar\pi}{2m^*L_2^2} \exp\left(-\frac{4\sqrt{2m^*}(E_I^*)^{\frac{3}{2}}}{3q\hbar F}\right) \times \exp\left(-\frac{E_h - E_I^*}{k_B T}\right)$$

where  $\tau_{tot}$  is the total tunneling time,  $\hbar$  is the reduced Planck constant,  $m^*$  is the effective mass of the carrier,  $L_2$  is the height of the QD,  $E_I^*$  is the energy level of the intermediate state,  $q$  is the electron charge,  $F$  is the electric field strength,  $E_h$  is the carrier localization energy before tunneling,  $k_B$  is the Boltzmann constant and  $T$  is the temperature. For our QD band structure, the dot height is  $\sim 5$  nm; and the localization energies are  $\sim 160$  meV and  $\sim 120$  meV for electrons and holes, respectively. We used electron and hole effective masses of  $0.04 m_0$  and  $0.4 m_0$  respectively. The electric field strength is 93 kV/cm, which corresponds to  $-3$  V reverse bias on the device. The calculation result is shown in the inset in Fig. 6(a). Note that the hole emission rate is much slower than that of electron and is therefore the major limit to the PD speed. Assuming an intermediate state 30 meV above the valence band of the wetting layer, the escape time of the hole is calculated to be  $\sim 30$  ps. Taking this into the bandwidth calculation, the result is shown in the dark line in Fig. 6(a). The curve obtained from the combined effects of RC response and the carrier trapping (dark line) matches well with the measured OE response (blue dots).

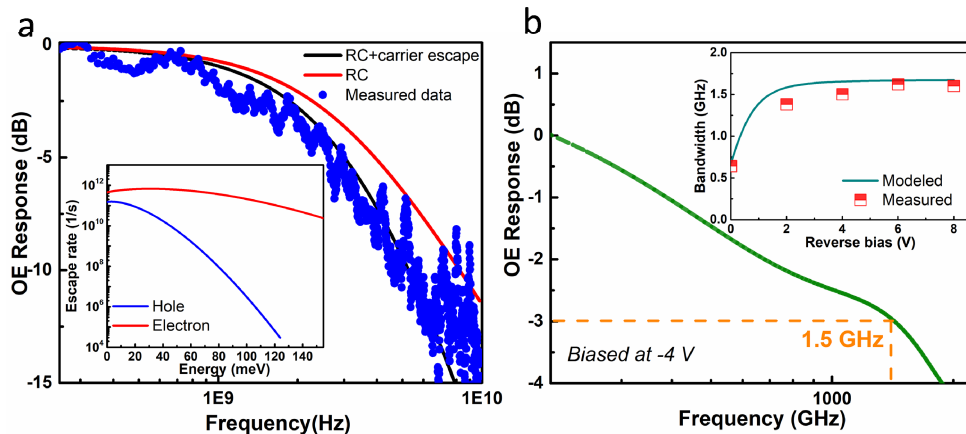


Fig. 6. (a) RC limited OE response extracted from a quasi-static circuit model (red line), calculated OE response considering the combined effects of RC response and the carrier trapping (dark line), OE response obtained from the  $S_{12}$  measurement (blue dots). Inset: calculation result of the hole escape and electron escape rate. (b) OE response of a QD PD obtained by measuring optically generated RF signal. Inset: Bias dependence of the measured and modeled 3-dB bandwidth of this device.

To further verify the carrier trapping effect in the QD PD, the OE response was measured using a different technique on a different device by beating the optical signals from two tunable lasers and detecting the optically generated RF signal power from the PD [37]. The frequency of the RF signal can be precisely controlled by the wavelength separation of the two tunable lasers down to 0.2 GHz. With this method, the bandwidth of the device was measured to be 1.5 GHz at a reverse bias of 4 V at 1300 nm (Fig. 6(b)). The inset in Fig. 6(b) shows the measured and modeled 3-dB bandwidth versus reverse bias at 1300 nm. At higher reverse bias, the tunneling probability increases due to a narrower tunneling barrier. Such improvement in the device bandwidth at higher reverse bias reaffirms the existence of carrier trapping in our QD PDs. The high-speed performance of the QD photodiodes can be improved by engineering the design of the epitaxial layers, reducing the device sizes, changing the passivation materials, and applying traveling wave electrodes. Currently, the complete epitaxial structure is comprised of a  $\sim 4$   $\mu\text{m}$  thick GaAs/AlGaAs graded-index separate confinement heterostructure (GRINSCH), not optimized for a high-speed photodiode. The rectangular mesa size (20- $\mu\text{m}$  in width and 50- $\mu\text{m}$  in length) is relatively large and can be scaled down to reduce the capacitance of the device. A 1  $\mu\text{m}$ -thick sputtered SiO<sub>2</sub> layer was used as the passivation layer and can be changed to a several micron-thick benzocyclobutene (BCB,  $\epsilon = 2.6$ ) layer to minimize the  $p$ -pad capacitance. Moreover, traveling-wave electrodes can be designed to achieve higher bandwidth, overcoming the tradeoff between the bandwidth and the quantum efficiency [38].

For application in PICs, this waveguide PD would be connected to lasers and modulators via waveguides and splitters [39]. To demonstrate the flexibility of the III-V/Si device platform, a preliminary on-chip detection system was further explored. Here, to integrate PDs with lasers without any additional fabrication steps, the two devices were fabricated on a single active region design. As shown in Fig. 7(a), a micro-ring laser was directly connected to a 1  $\mu\text{m}$ -wide waveguide irregularity in the center region. The connected waveguide breaks the perfect circularity of the cavity and facilitates the light scattering around the waveguide irregularity. The intentionally induced scattering of light can then be free-space coupled to a rectangular PD of 20  $\mu\text{m}$  in width and 50  $\mu\text{m}$  in length. The laser emission from the micro-laser can be probed via the changes in the photocurrent induced in the PD, realizing on-chip light detection in the micro-scale. Since the waveguide connected to the micro-laser was not injected, it was designed with a relatively small size (1  $\mu\text{m}$  in width and 9  $\mu\text{m}$  in length) to avoid potential optical loss. The photocurrent was measured from the photodiode at a  $-1$  V bias, while forward-biasing the micro-ring laser. Figure 7(b) shows the measured photocurrent as a function of the injection current for a micro-ring laser with a mesa width of 4  $\mu\text{m}$  and an outer-ring radius of 50  $\mu\text{m}$ . The measured photocurrent suggests a lasing threshold of around 21 mA. The large quantum dot spontaneous emission (excited states, wetting layer, etc.) contributes to the measured light by the photodiode. On-chip photodetection from a monolithically integrated QD micro-ring laser through waveguide coupling is now being researched to realize high efficiency directional emission and detection.



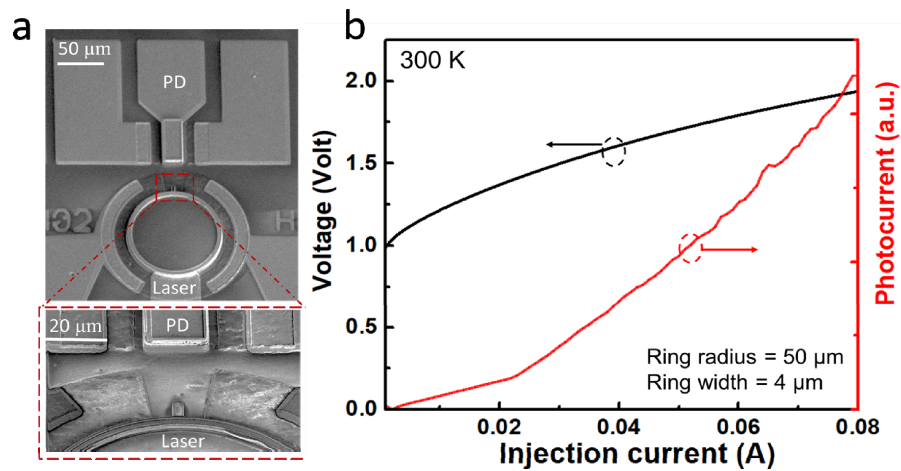


Fig. 7. (a) Top-view of the fabricated laser-PD systems through free-space coupling; (b) measured laser voltage and detector photocurrent as a function of the injection current for a 50- $\mu\text{m}$  outer-ring radius micro-ring laser, with a mesa width of 4 $\mu\text{m}$ .

### 3. Conclusions

In conclusion, we report on-chip QD PDs directly grown on (001) Si substrates with an ultra-low dark current of 0.8 nA (at  $-1$  V). A proof of principle demonstration for the on-chip photodetection via free-space coupling is presented. A great potential for fabricating the entire PIC from the epitaxially deposited III-V layers is suggested. In the future, instead of using the same epi-structure for each component, multiple bandgap materials could be obtained via butt-joint regrowth or QD intermixing, in similar fashion to the complete suite of technologies in InP PICs. Utilizing a QD gain region to combat defects, to realize low-threshold lasing and low dark current photo-detection, represents an important advancement towards substituting III-V/Si epitaxy on silicon for epitaxial growth on InP or replacing the wafer bonding techniques on silicon for dense integration and low power consumption.

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