

Chemical Vapor Deposited Monolayer MoS₂ Top-Gate MOSFET with Atomic-Layer-Deposited ZrO₂ as Gate Dielectric

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Abstract—For the first time, ZrO₂ dielectric deposition on pristine monolayer MoS₂ by atomic layer deposition (ALD) is demonstrated and ZrO₂/MoS₂ top-gate MOSFETs have been fabricated. ALD ZrO₂ overcoat, like other high-*k* oxides such as HfO₂ and Al₂O₃, was shown to enhance the MoS₂ channel mobility. As a result, an on/off current ratio of over 10⁷, a subthreshold slope (*SS*) of 276 mV/dec, and a field-effect electron mobility of 12.1 cm²·V⁻¹·s⁻¹ have been achieved. The maximum drain current of the MOSFET with a top-gate length of 4 μm and a source/drain spacing of 9 μm is measured to be 1.4 μA/μm at V_{DS} = 5 V. The gate leakage current is below 10⁻² A/cm² under a gate bias of 10 V. A high dielectric breakdown field of 4.9 MV/cm is obtained. Gate hysteresis and frequency-dependent capacitance-voltage measurements were also performed to characterize the ZrO₂/MoS₂ interface quality, which yielded an interface state density of ~3×10¹² cm⁻²eV⁻¹.

Keywords: Atomic layer deposition, ZrO₂, MoS₂, top-gate transistor

I. INTRODUCTION

With a sizable bandgap that changes from indirect to direct in single layers, semiconducting two-dimensional molybdenum disulfide (MoS_2) has recently gained tremendous interest for transistors, photodetectors and electroluminescent devices [1-3]. Thanks to the enhanced electrostatic control of the gate over the channel [2-4], MoS_2 field effect transistors (FETs) have demonstrated outstanding device performance, such as high on/off current ratios up to 10^8 [2-3], a near-ideal subthreshold swing of 60 mV/dec [3-4], and good carrier mobilities [5]. To increase the gate capacitance and preserve a high channel mobility through the dielectric screening effect [6], integration of high- k technology with MoS_2 transistors is essential. However, atomic-layer deposition (ALD) of high-quality gate dielectrics on 2D materials has proven challenging [7-10] because of the lack of surface-dangling bonds.

The high- k dielectrics investigated to date include TiO_2 , SrTiO_3 , Al_2O_3 , HfO_2 , ZrO_2 , and the associated silicates [11-15]. Among these, Al_2O_3 , HfO_2 , and ZrO_2 have been widely studied and are believed to be the most promising candidates due to their high dielectric constant, good thermodynamic stability, and reasonable band gap [16, 17]. Although Al_2O_3 and HfO_2 have been intensely used to fabricate MoS_2 top-gate transistor [18, 19], ZrO_2 is, to the best of our knowledge, only reported in back-gate transistors [20]. By transferring MoS_2 flakes onto a pre-deposited high- k dielectric layer, the back-gate approach bypasses the challenges associated with ALD deposition on 2D materials. However, there would remain significant interest in readily using the chemical vapor deposition (CVD) grown MoS_2 films to build top gate transistors which are more in line with mainstream transistor design and integration.

Previous studies on high- k/MoS_2 based top-gated transistors have almost exclusively been focused on mechanically exfoliated flakes. However, due to the small size of few-layer films and

possible extraneous contamination from exfoliation process, mechanical exfoliation is not a scalable or reproducible method for commercial use [21]. New synthetic routes such as CVD allow for both high-quality and large-area thin films. In fact, a variety of 2D materials including graphene [22], boron nitride [23] and MoS₂ [24] have reportedly been synthesized by CVD methods. However, the electrical properties of CVD MoS₂, especially the device performances of top-gated transistors, have not been comprehensively studied.

In this work, we report the first realization of CVD monolayer MoS₂ top-gate transistors with ALD ZrO₂ as gate dielectric. Using a low-temperature ALD process, we achieve direct deposition of ZrO₂ on pristine monolayer MoS₂. The fabricated top-gate transistors exhibit well-behaved characteristics with high on/off current ratios and low gate leakage current. The influence of ALD ZrO₂ on the electrical performance of MoS₂/SiO₂ back-gate transistor is discussed. The dielectric properties, as well as the MoS₂/ZrO₂ interface quality have been investigated.

II. EXPERIMENTAL DETAILS

Fig. 1(a) displays a cross-section schematic of the MoS₂ MOSFET with a top-gate electrode. A top-view optical microscope image of a fabricated device is shown Fig. 1(b). Monolayer MoS₂ reported in this work were grown by chemical vapor deposition on a heavily doped Si substrate capped with 300 nm SiO₂. High purity MoO₃ and S powder were used as precursors. The as-grown single-crystal [25] triangular shaped MoS₂ (with average edge length ~40 μm) was characterized by Raman scattering. As shown by the Raman spectrum in Fig. 1(c), the frequency difference between the in-plane (E_{2g}^1 , ~385.1 cm⁻¹) and out-of-plane (A_{1g} , ~405.1 cm⁻¹) phonon modes confirms that the deposited MoS₂ is of monolayer thickness [26]. The device fabrication started with deposition of source/drain (S/D) electrodes (10/90 nm Ti/Au) by standard

lithographic patterning. ZrO_2 was then deposited directly on the MoS_2 films in an Oxford OpAL ALD reactor at a temperature of 200 °C. Tetrakis ethylmethylamino zirconium (TEMAZ) and water were used as precursors. After 300 ALD cycles, ~ 27 nm ZrO_2 was deposited and confirmed by ellipsometry measurement. Subsequently, source/drain contact holes were opened using a combination of dry and wet etching of the ZrO_2 layer. Finally, gate metal (10/90 nm Ti/Au) was defined. A dimension 3100 AFM system was used to examine the surface morphology after ALD deposition. All electrical tests were carried out using an Agilent 4156C precision semiconductor parameter analyzer at room temperature.

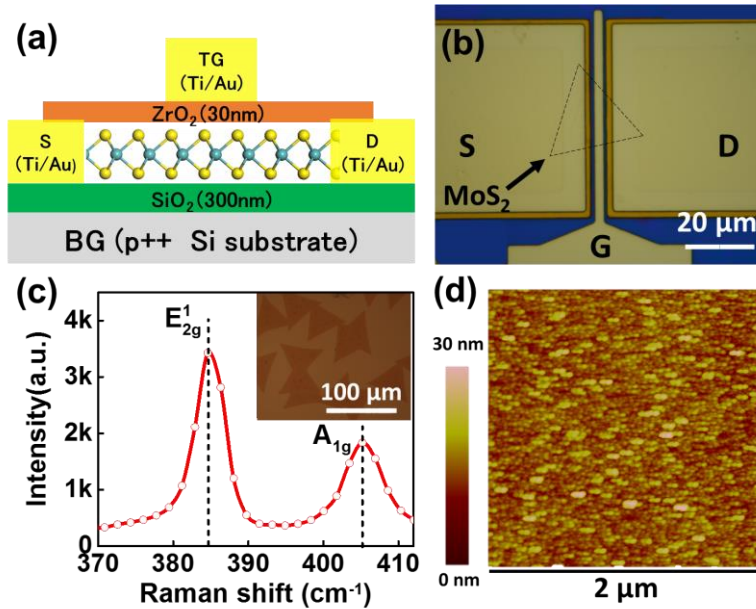


FIG. 1. (a) Schematic illustration of a monolayer $\text{ZrO}_2/\text{MoS}_2$ top-gate field-effect transistor. The p++ Si substrate acts as global back gate (BG) while Ti/Au metal stack as top gate (TG). (b) Optical microscope image of a typical MoS_2 device. (c) Raman spectrum of the as-grown MoS_2 film on Si/ SiO_2 substrate measured at room temperature. Laser wavelength for Raman measurement is 514 nm. The inset shows the optical image of monolayer MoS_2 on SiO_2/Si substrate. (d) AFM image of the ALD- ZrO_2 on MoS_2 .

III. RESULTS AND DISCUSSION

Fig. 1(d) shows a representative AFM image of the surface of the atomic-layer-deposited ZrO_2 on single-layer MoS_2 . The ZrO_2 is continuous but exhibits island type morphology [27]. A root

mean square (RMS) roughness of 2.95 nm was obtained across a scanning area of $2 \times 2 \mu\text{m}^2$. This surface roughness is inferior when compared with the optimized ALD deposition of Al_2O_3 on MoS_2 (0.58 nm in rms for Al_2O_3 on MoS_2 [28]) and needs to be further optimized. The roughness could undermine the mobility of MoS_2 underneath and cause gate leakage fluctuations. Nevertheless, microscope observations indicated a complete coverage of direct ALD on pristine MoS_2 , which is attributed to physical absorption of precursors on the basal plane. This is also observed in previous demonstrations of ALD Al_2O_3 [10] and HfO_2 [27] on MoS_2 at the optimized temperature window.

We first discuss the influence of ALD ZrO_2 overcoat on the electrical performance of CVD monolayer $\text{MoS}_2/\text{SiO}_2$ back-gate transistor. Fig. 2 shows the transfer and output characteristics of a $\text{ZrO}_2/\text{SiO}_2$ back-gate FET before and after the deposition of ZrO_2 . Previous studies have shown that high- k oxides HfO_2 and Al_2O_3 encapsulation can greatly improve the MoS_2 channel mobility through Coulomb scattering screening effect. [6] In our case, the device shows more than doubled drive current after ZrO_2 deposition, implying mobility improved by ZrO_2 overcoating which is similar to HfO_2 and Al_2O_3 . The field-effect mobility is extracted from the I_D versus V_{bg} curves in the linear region by using the expression $\mu = L/V_{\text{DS}}C_{\text{ox}} \times (dI_{\text{DS}}/dV_{\text{bg}})$, where L and W are the channel length and width, V_{DS} is the source-drain voltage, and C_{ox} is the back-gate capacitance per unit area. At room temperature, the extracted mobility before and after ZrO_2 top dielectric are $6.9 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and $11.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, respectively. We attribute the mobility enhancement to the suppressed charged impurity scattering, which is similar to the $\text{Al}_2\text{O}_3/\text{MoS}_2$ and $\text{HfO}_2/\text{MoS}_2$ top-gate transistors. [6, 18] The mobility with ZrO_2 overcoating is not as high as that of the best transistor using HfO_2 [7] as the gate dielectric, which is possibly attributed to the large Coulomb scattering from fixed charges near the ZrO_2 surface induced by the comparatively

lower ALD deposition temperature [29]. In addition, we observe that while our device was intrinsically n-doped (a negative bias voltage required to reach neutral point) for both before and after ALD growth, the threshold voltage was positively shifted after the ZrO_2 deposition. The reason for this shift is not clear and is still under investigation.

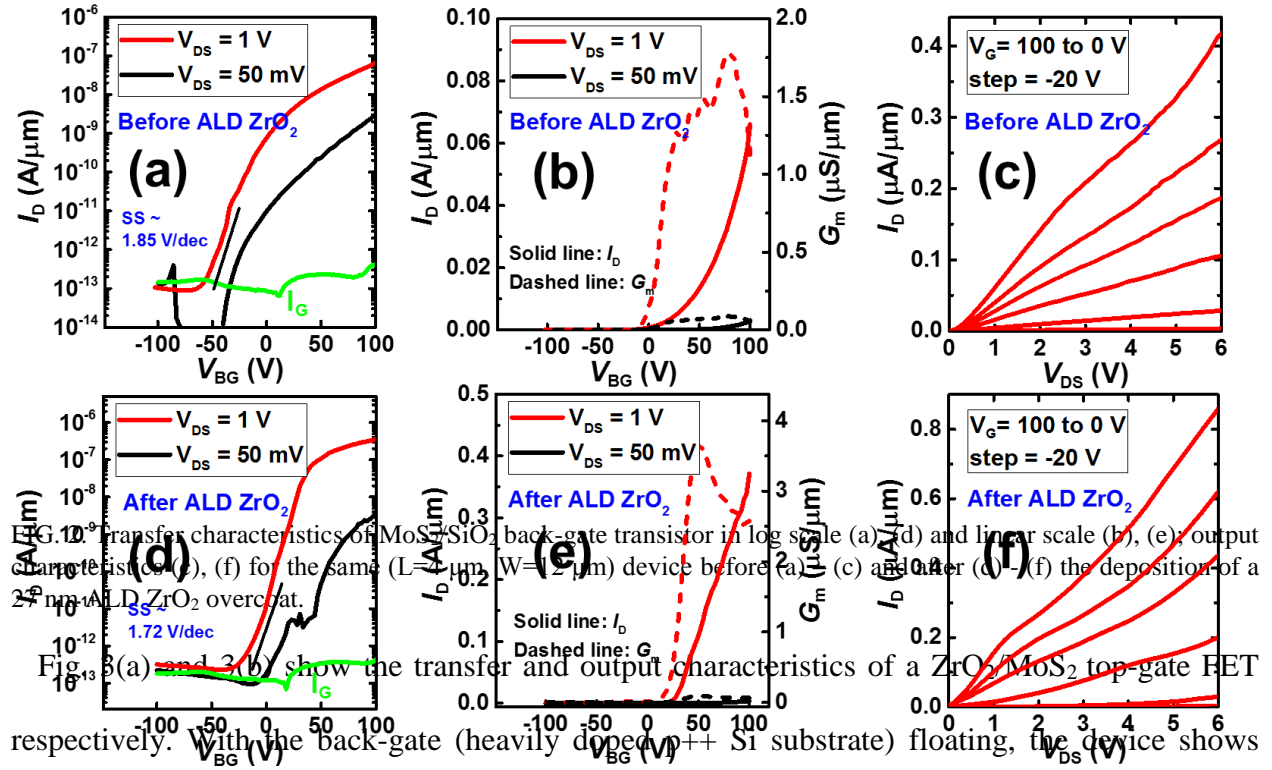


FIG. 12. Transfer characteristics of $\text{MoS}_2/\text{SiO}_2$ back-gate transistor in log scale (a), (d) and linear scale (b), (e); output characteristics (c), (f) for the same ($L = 1 \mu\text{m}$, $W = 2 \mu\text{m}$) device before (a), (c) and after (d)–(f) the deposition of a $2 \mu\text{m}$ ALD ZrO_2 overcoat.

Fig. 13(a) and 13(b) show the transfer and output characteristics of a $\text{ZrO}_2/\text{MoS}_2$ top-gate FET respectively. With the back-gate (heavily doped $p++$ Si substrate) floating, the device shows typical n-type conduction behavior and an on/off current ratio of $\sim 10^6$. At $V_{DS} = 5$ V, the subthreshold slope (SS) is 276 mV per decade. The relatively large SS can be attributed to the un-optimized $\text{MoS}_2/\text{ZrO}_2$ interface. Furthermore, with $V_{DS} = 5$ V and back gate floating, we note clear reduction of drain current when top-gate voltage is increased. We speculate this is likely due to the injection and trapping of electrons inside the gate dielectric (Fig. 3(c)). When the top gate is biased at lower voltage, electron injection from the channel to the ZrO_2 dielectric is suppressed by the large tunneling barrier. With increased V_{TG} , this process would be greatly enhanced since the tunneling barrier is reduced. If a large proportion of electrons are trapped, the current is then reduced.

The ZrO₂/MoS₂ to-gate transistors in this work are gate-underlap transistors with large S/D access regions (Fig. 3(d)). Previous studies have found that the un-gated channel regions can lead to significant access resistance and contact resistance, thus obscuring the intrinsic performances of the top-gate MoS₂ transistors. [30] To minimize such influence and obtain the intrinsic device parameters, devices are also characterized under a large positive back-gate voltage. The positive back-gate voltage induces electron accumulation within S/D access region and thus reduce the access resistance and contact resistance. From Fig. 3(a), when a back-gate voltage of 100 V was applied, drive current was enhanced by 20 times, leading to a greater on/off current ratio of over 10⁷. The current enhancement is also shown in output characteristics in Fig. 3(b), where the on-state resistance was significantly improved under a positive back-gate bias. Consequently, the maximum drive current reached ~1.4 μA/μm at V_{DS} = 5 V and V_G = 3.5 V. The extracted mobility with the back-gate biased at 100 V is 12.1 cm²·V⁻¹·s⁻¹, which is close to the value determined from back-gate transistor. Table 1 summarizes the device parameters from CVD monolayer MoS₂ MOSFETs using different high-*k* oxides as top-gate dielectrics.

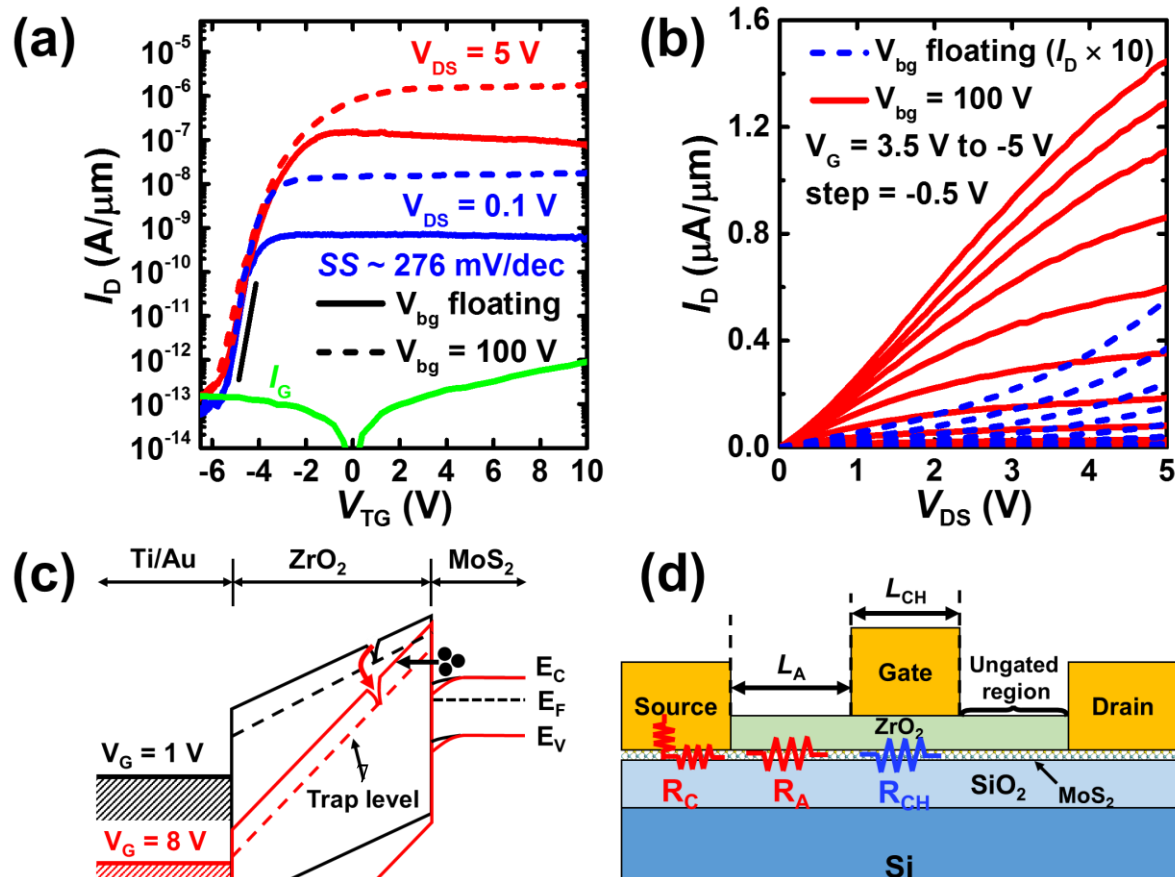


Fig. 3. (a) Transfer characteristics of $\text{ZrO}_2/\text{MoS}_2$ top-gate transistor ($L=4 \mu\text{m}$, $W=12 \mu\text{m}$) and (b) Output characteristics of device indicated in (a). For clarity, the drain current with back-gate floating is multiplied by 10 times. (c) Schematic band diagram of $\text{Ti}/\text{ZrO}_2/\text{MoS}_2$ MOS structure at $V_{\text{TG}}=1 \text{ V}$ and $V_{\text{TG}}=8 \text{ V}$. With a high top gate voltage, electron injection and trapping would occur due to the reduced tunneling barrier. (d) Schematic illustration of access resistance and contact resistance in a gate-underlap MoS_2 transistor. R_{C} : contact resistance, R_{A} : access resistance, R_{CH} : channel resistance, L_{A} : access region length.

Table 1. The comparison of some key device parameters between different CVD monolayer MoS_2 top-gate MOSFETs.

Dielectrics	Al_2O_3	HfO_2	ZrO_2 [this work]
On/off	10^7 [19]	10^8 [35]	10^7
Off state leakage	$10^{-7} \mu\text{A}/\mu\text{m}$ [19]	$10^{-7} \mu\text{A}/\mu\text{m}$ [32]	$10^{-7} \mu\text{A}/\mu\text{m}$
Mobility	$24 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [19]	$55 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [33]	$12 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$
Drive current	$1.0 \mu\text{A}/\mu\text{m}$ [19]	$55 \mu\text{A}/\mu\text{m}$ [19]	$1.4 \mu\text{A}/\mu\text{m}$
G_{m}	-	$38 \mu\text{S}/\mu\text{m}$ [19]	$2.23 \mu\text{S}/\mu\text{m}$
SS	$140 \text{ mV}/\text{dec}$ [31]	$110 \text{ mV}/\text{dec}$ [32]	$276 \text{ mV}/\text{dec}$
D_{it}	$< 10^{13} \text{ cm}^2\text{eV}^{-1}$ [34]	-	$3 \times 10^{12} \text{ cm}^2\text{eV}^{-1}$

To study the electrical properties of the $\text{ZrO}_2/\text{MoS}_2$ gate stack, gate leakage current was measured at both bias polarities in our top-gate transistor. A bias was applied to the gate terminal, with both the drain and source grounded. As shown in Fig. 4(a), the gate leakage current density J_{L} falls in the range 10^{-4} - $10^{-2} \text{ A}/\text{cm}^2$ under gate biases below 10 V, which is considerably lower than that of direct ALD deposited $\text{HfO}_2(28 \text{ nm})/\text{MoS}_2$ gate stack [35]. The inset of Fig. 4(a) plots the J_{L} as a function of the electric field E_{F} . The breakdown field (E_{BD}) for 27 nm ALD ZrO_2 on MoS_2 is calculated to be 4.9 MV/cm, comparable to the value of $\text{ZrO}_2/\text{Al}_2\text{O}_3$ bilayer reported in the literature [36]. Fig. 4(b) plots the $J_{\text{L}}-E_{\text{F}}$ curve at positive gate

biases. With $\ln(1/E_F) < -0.8$ ($V_G > 6$ V), electron injection from MoS₂ follows the Fowler-Nordheim tunneling rule, as evidenced by the linear J/E_F^2 versus $\ln(1/E_F)$ relationship. The low leakage current and high breakdown field suggest good dielectric properties of ALD ZrO₂ on MoS₂.

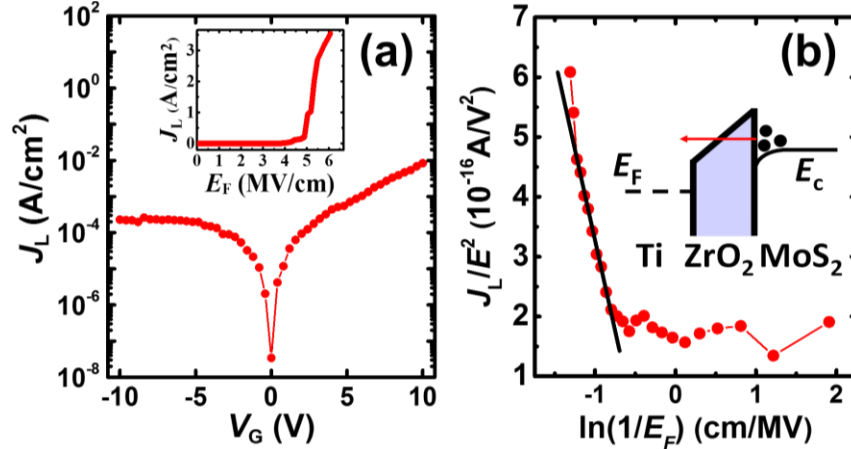


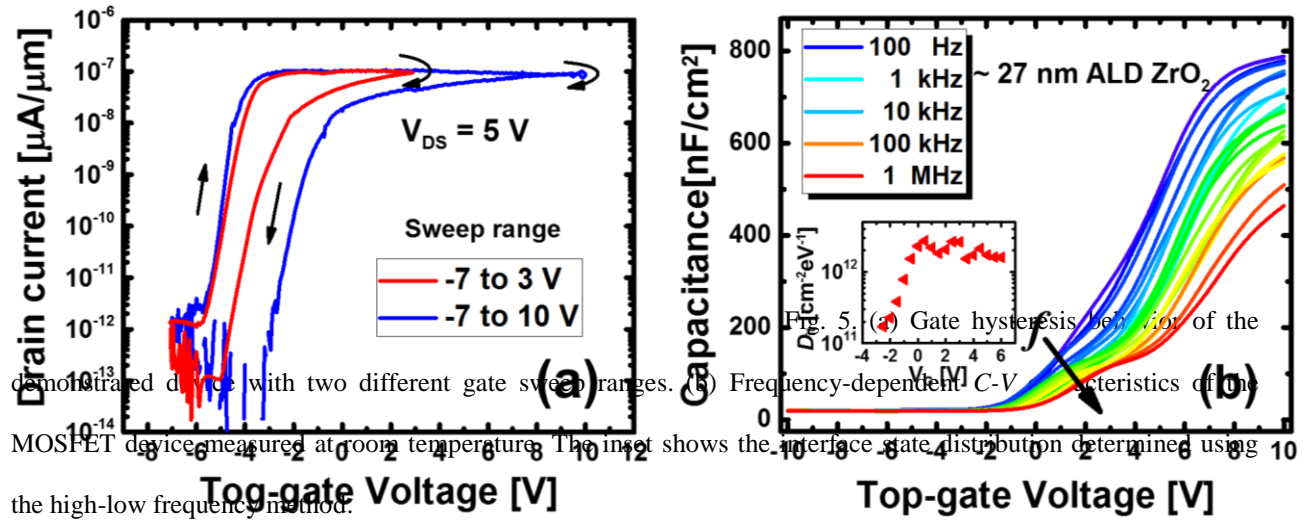
Fig. 4. (a) Leakage current characteristics of a MOSFET structure (Ti/ALD-ZrO₂/MoS₂). The inset of the figure shows the breakdown field of 27nm ALD ZrO₂ on MoS₂. (b) A J/E^2 vs $\ln(1/E)$ plot for the positive biasing condition, consistent with Fowler–Nordheim tunneling behavior.

Gate hysteresis and frequency-dependent capacitance-voltage (C - V) have been measured to investigate the interface quality between ZrO₂ and MoS₂. In Fig. 5(a), the gate is swept from negative to positive then back to negative voltage, with the back gate floating. The hysteresis becomes more pronounced when the sweep range is increased. This behavior, together with larger hysteresis gap at higher gate voltage, suggests a higher interface trap state density near the conduction band since the larger gate voltage, the closer the fermi level is to the conduction band. In Fig. 5(b), the C - V curve shows typical n-type MOS capacitor behavior, with a clear transition from depletion to accumulation when the gate voltage increases. The gate oxide capacitance C_{ox} was determined to be 790 nF/cm² from the maximum capacitance at 100 Hz, which corresponded to an EOT of 4.4 nm. A larger frequency dispersion was observed at the accumulation region, which also indicates a high interface trap state density close to the

conduction band. We further quantitatively extracted the interface state density using the high-low frequency method which gives the formula [37]:

$$D_{it}(V_G) = \frac{C_{ox}}{q} \left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}} \right) \quad (1)$$

where V_G , D_{it} , q , C_{lf} , and C_{hf} represent gate voltage, interface state density, the elementary charge, low-frequency capacitance, and high-frequency capacitance, respectively. The inset to Fig. 5(b) plots the calculated D_{it} vs. gate voltage in the transition region of the CV curve (from accumulation to depletion). The D_{it} is approximately $3 \times 10^{12} \text{ cm}^{-2} \cdot \text{eV}^{-1}$. To reduce the gate hysteresis and interface states, further studies should focus on the chemical absorption process during the ALD growth and the improvement of high- k /MoS₂ interface quality.



Further, in view of device-to-device variation, a statistical study of the key device parameters is performed to gain a comprehensive understanding of the electrical performances. The data are presented in Fig. 6. A total of 20 devices are studied with different channel lengths and widths. The average values and standard deviations are analyzed. These figures show a broad distribution of different electrical parameters which can be connected to the nonuniformity of synthesized MoS₂ film and fabrication process. The large fluctuations of gate leakage also

suggest nonuniform thickness of ZrO₂ which has been discussed in the previous part.

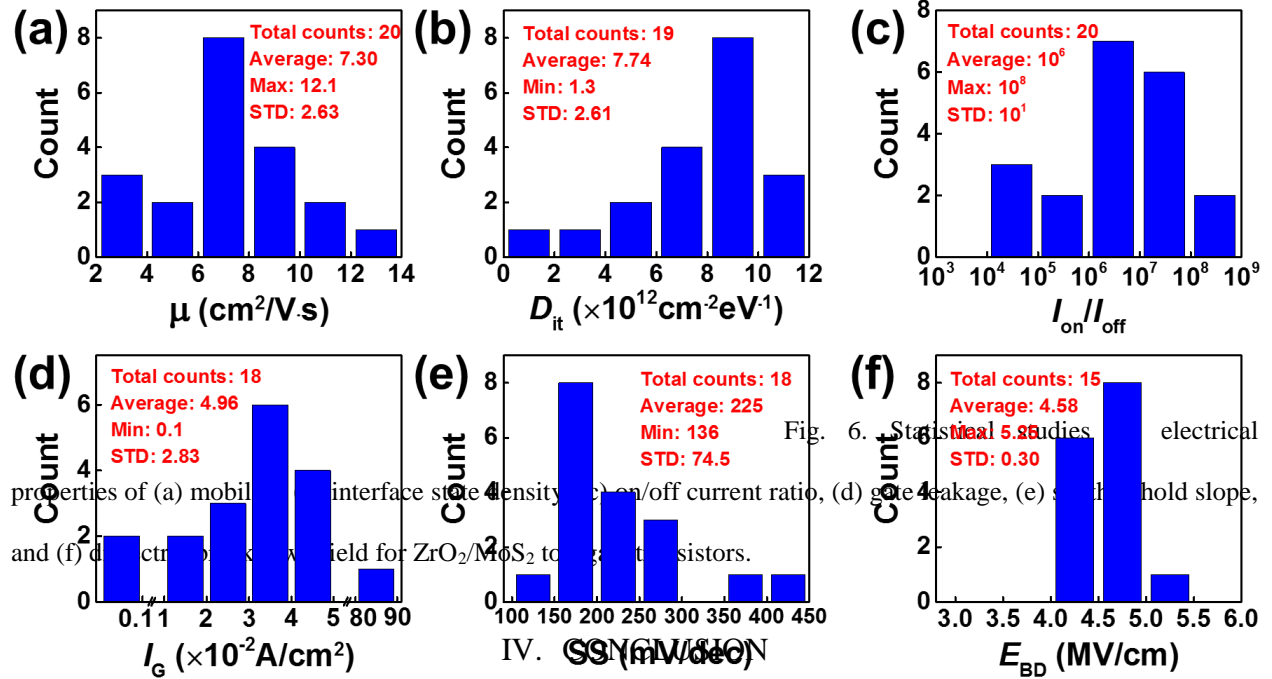


Fig. 6. Statistical studies of electrical

properties of (a) mobility, (b) interface state density, (c) on/off current ratio, (d) gate leakage, (e) subthreshold swing, and (f) breakdown electric field for ZrO₂/MoS₂ transistors.

In summary, we have experimentally demonstrated top-gate MOSFETs with monolayer MoS₂ channel and ALD ZrO₂ as gate dielectric. AFM and *I-V* studies show that ALD ZrO₂ can be directly deposited on MoS₂ with low leakage current and high breakdown field. ZrO₂ overlayer can improve the MoS₂ channel mobility. Gate hysteresis and *C-V* measurements reveal a ZrO₂/MoS₂ interface state density of about 3×10^{12} cm⁻²·eV⁻¹. These results suggest that ALD ZrO₂ could be a promising candidate for gate dielectric application in MoS₂-based MOSFETs.

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