



USE OF WAVEFORM ENGINEERING TO STRESS
TEST, CHARACTERISE AND DESIGN A HIGHLY
EFFICIENT MMIC POWER AMPLIFIER

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Summary

This thesis brings together different areas of waveform engineering in power amplifier research, from load pull and reliability testing through to measuring finished designs. It shows how using all this knowledge together can enable an engineer to start with just a transistor, and progress to a functional design much faster with the use of waveform engineering at every stage.

Initially this project looked at expanding the conventional voltage standing wave ratio sweep to address more than the fundamental impedance with static harmonic impedances by including full harmonic impedance sweeps. This showed there were voltage peaking interactions that could potentially cause device failure, these were caused by interactions between the fundamental and harmonic impedances. The next step was to identify the cause of failures that had occurred during voltage standing wave ratio sweeps. This demonstrated the need for waveforms to identify failures caused by peak voltage and/or current.

Waveform data can also be used to analyse and compare the different device technologies and analyse their performance, allowing deep insight into the ‘knee’ region of the RF-IV plot, and how it affects performance of a technology using a novel data processing approach.

The final use of waveforms in this thesis is at the design stage, where a Continuous Class B design was done on a quasi-MMIC. This design was then fabricated and tested, showing that Continuous Class B and other continuous modes can be used for quasi-MMIC designs at S-band as well as the previously used laminate designs. Another topology that was used in this thesis was Doherty, which has traditionally struggled with bandwidth, but using a novel 50 V GaN FET supplied by Qorvo allowed a more broadband Doherty design to be fabricated.

List of Key Contributions

Contribution 1

Demonstrating the need for novel multi-harmonic impedance sweeps during a voltage standing wave ratio stress test.

Contribution 2

Demonstrating the need for the novel use of waveform data during the voltage standing wave ratio stress test to allow detection and diagnosis of peak RF voltage and/or current failure.

Contribution 3

Developing a novel method to process the waveform information obtained from generating a RF-IV plot to allow insight into the effects of the knee region, and knee walkout on performance.

Contribution 4

Design, fabrication and measurement of the first Continuous Class B quasi-MMIC at S-band.

Contribution 5

The use of novel 50V GaN FET to design a broadband Doherty.

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Glossaries

Glossary

Continuous Class B: This refers to the extended impedance/waveform space that allows for the same operating performance as the classical class B.

DC-IV: This is a plot that shows the DC operating characteristics of a device, often done by sweeping the output bias voltage and the input voltage or current.

Extrinsic Current Generator Plane: This refers to the plane of the device where the device ends, and any packaging starts. This will include parasitic components like C_{ds} .

Intrinsic Current Generator Plane: This refers to the plane of the device where the current is generated and does not include any parasitic component.

Package Plane: This refers to the plane of the device where the package ends, and the output matching starts. This will include parasitic components like bond wires from chip and on chip pre-matching.

RF-IV: This is a plot that shows the RF characteristics of a device, often looking at the knee region.

Acronyms

16-QAM: 16 state Quadrature Amplitude Modulation.

2DEG: 2-Dimensional Electron Gas.

4G: 4th Generation.

Acronyms

5G: 5th Generation.

64-QAM: 64 state Quadrature Amplitude Modulation.

8-PSK: 8 state Phase-Shift Keying.

BJT: Bipolar Junction Transistor.

CAD: Computer Aided Design.

CHEF: Centre for High Frequency Engineering.

CM: Continuous Mode.

CW: Continuous Wave.

DC: Direct Current.

DLL: Dynamic Load Line.

DPD: Digital Predistortion.

DUT: Device Under Test.

EDGE: Enhanced Data rates for GSM Evolution.

ELP: Envelope Load Pull.

EU: European Union.

extrinsic i-gen: extrinsic current generator plane.

FDMA: Frequency Division Multiple Access.

FET: Field Effect Transistor.

GMSK: Gaussian Minimum Shift Keying.

GSM: Global System for Mobile communication.

HBT: Heterojunction Bipolar Transistor.

HEMT: High Election Mobility Transistor.

HPA: High Power Amplifier.

HSUPA: High Speed Uplink Packet Access.

HVHBT: High Voltage Heterojunction Bipolar Transistor.

intrinsic i-gen: intrinsic current generator plane.

LTE: Long Term Evolution.

MMIC: Monolithic Microwave Integrated Circuit.

OBO: Output Back-Off.

OFDM: Orthogonal Frequency Division Multiplexing.

PA: Power Amplifier.

PAPR: Peak to Average Power Ratio.

PDK: Process Design Kit.

QPSK: Quadrature Phase Shift Keying.

RF: Radio Frequency.

RFPA: Radio Frequency Power Amplifier.

SC-FDMA: Single-Carrier Frequency Division Multiple Access.

UK: United Kingdom.

UMTS: Universal Mobile Telecommunications Service.

VNA: Vector Network Analyser.

VSWR: Voltage Standing Wave Ratio.

Symbols

α : Transport factor, often describing the ratio of the emitter current to the collector current in a BJT.

β : Current gain, often describing the ratio of the base current to the collector current in a BJT.

Γ : Magnitude of the reflection coefficient.

Γ_{IDEAL} : Ideal VSWR sweep points that are swept around 50Ω .

η : Output efficiency of a transistor. Often called drain or collector efficiency (%).

ϕ : Electrothermal feedback coefficient, typically 1.25 for GaAs ($\frac{mV}{^\circ C}$).

A: Area of an object (m^2).

A_E : Area of the emitter in a BJT or HBT (m^2).

- BV: Breakdown voltage (V).
- BV_{CB} : Breakdown voltage of the base-collector junction (V).
- BV_{CE} : Breakdown voltage of the base-emitter junction (V).
- D_n : Electron diffusion constant ($\frac{m^2}{s}$).
- $D_{n,B}$: Electron diffusion constant in the base ($\frac{m^2}{s}$).
- D_p : Hole diffusion constant ($\frac{m^2}{s}$).
- $D_{p,E}$: Hole diffusion constant in the emitter ($\frac{m^2}{s}$).
- FBW: Fractional Bandwidth (%).
- G: Charge carrier generation rate ($m^{-3}s^{-1}$).
- G_{AV} : The available gain of a system (dB).
- G_{CB} : Charge carrier generation rate in the collector-base junction ($m^{-3}s^{-1}$).
- g_m : Transconductance, the measure of the change in input voltage to output current in a transistor (S).
- g_{m0} : Transconductance when $V_{GS} = 0V$ (S).
- G_{MAG} : The maximum available gain if the input is perfectly matched (dB).
- I: Current (A).
- I_B : Base current (A).
- I_{BC0} : Normal thermally generated current through the base-collector junction (A).
- I_C : Collector current (A).
- I_D : Drain current (A).
- I_{DC} : DC component of a current waveform (A).
- I_{DSS} : Drain current when $V_G = 0V$ (A).
- I_E : Emitter current (A).
- $I_{E,n}$: Electron current in the emitter (A).
- $I_{E,p}$: Hole current in the emitter (A).
- I_{FUND} : Fundamental components of the RF current waveform (A).
- I_{MAX} : Maximum value of the RF current waveform (A).
- I_P : Peak drain current (A).
- I_{RF} : Single harmonic component of an RF current waveform (A).
- I_s : Reverse saturation current (A).

- k : Boltzmann's constant $= 1.38 \times 10^{23} J/K$.
- L_n : Electron diffusion length (m).
- L_p : Hole diffusion length (m).
- m : Mass of an object (kg).
- M : Multiplication factor.
- M_{CB} : Multiplication factor for the collector-base junction.
- n : Ideality Factor, where un-modelled physical variations in the device will cause different results n is used to account for these differences. Most commonly used in association with diode junctions.
- N_B : Base doping density (m^{-3}).
- N_E : Emitter doping density (m^{-3}).
- n_i : Intrinsic carrier density (m^{-3}).
- n_{p0} : Electron density in an p-type semiconductor in thermal equilibrium (m^{-3}).
- P_{dBm} : Power in dBm (dBm).
- P_{DC} : DC power (W).
- P_{DRIVE} : Power of source driving the circuit (W or dBm).
- P_{IN} : Input power (W).
- p_{n0} : Hole density in an n-type semiconductor in thermal equilibrium (m^{-3}).
- P_{OUT} : Output power (W or dBm).
- P_{RF} : RF power (W).
- P_W : Power in W (W).
- PAE: Power Added Efficiency, this efficiency takes into account η and the drive power supplied to the device (%).
- q : Magnitude of electronic charge $= 1.6 \times 10^{-19}$ (C).
- R_0 : Resistance of drain-source channel when $V_{GS} = 0V$ (Ω).
- R_B : Resistance of base (Ω).
- R_{DC} : Resistance presented at DC (Ω).
- R_{DS} : Resistance of drain-source channel (Ω).

- R_E : Resistance of emitter (Ω).
- R_{ON} : The resistance of the drain channel when the FET is not saturated, or as the FET is turning on (Ω).
- R_{OUT} : The resistance of the drain channel once the drain current has saturated (Ω).
- R_{TH} : Thermal resistance of base (Ω).
- T_K : Absolute temperature in kelvins (K).
- v : Velocity of an object ($\frac{m}{s}$).
- V_a : Applied potential between two ports (V).
- V_{BE} : Potential across base-emitter junction (V).
- V_{CB} : Potential across base-collector junction (V).
- V_{CE} : Potential across collector-emitter junction (V).
- V_D : Potential at the drain (V).
- V_{DC} : DC component of a voltage waveform (V).
- V_{DS} : Potential across drain-source junction (V).
- V_{FUND} : Fundamental components of the RF voltage waveform (V).
- V_G : Potential at the gate (V).
- V_{GS} : Potential across gate-source junction (V).
- V_{MAX} : Maximum value of the RF voltage waveform (V).
- V_P : Value of V_G that pinches the channel fully off resulting in no current flow between the drain and source (V).
- V_{RF} : Single harmonic component of an RF voltage waveform (V).
- V_t : Thermal voltage (V).
- w_b : Width of base region (m).
- w_e : Width of emitter region (m).
- W_K : Kinetic energy ($\frac{m}{s}$).
- w_n : Width of an n-type region (m).
- w_p : Width of an p-type region (m).
- Z_0 : Normalised impedance, often of a Smith Chart (Ω).
- Z_L : Load impedance (Ω).
- Z_{OPT} : Optimum target impedance (Ω).

Units

Z_{RF} : Impedance of a harmonic (Ω).

Z_{VSWR} : Impedance that is part of a VSWR sweep (Ω).

Units

$^{\circ}C$: Celsius, unit for temperature.

$^{\circ}K$: Kelvin, unit for temperature.

Ω : Omega, unit for electrical impedance.

A: Ampere, unit for electric current.

C: Coulombs, unit for electronic charge.

dB: Decibel, unit for measuring the relative magnitude of two values, $10 \log(P_2/P_1)$.

dBm: Decibel-milliwatts, unit of power relative to 1 mW.

Hz: Hertz, unit for frequency.

J: Joule, unit for energy.

kg: Kilogram, unit for mass.

m: Metre, unit for distance.

s: Seconds, unit for time.

S: Siemens, unit for electrical admittance.

V: Voltage, unit for electric potential.

W: Watt, unit for electrical power.

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1

Introduction

1.1 Global Drive

Since the 1860s and 1870s there has been an interest in renewable energy [1] partly driven by increasing interest in reducing our reliance on non-renewable energy and the amount of power used, trying to make sure its use and generation is sustainable [2]. This is due to an increased awareness of our impact on the local and global environment. As a result, the communications industry is under the same pressure to reduce power consumption, which is achieved by increasing the efficiency of the communication chain.

The underlying reality is however that the communications industry has a long way to go, but there are also a lot of extra pressures outside environmental considerations that are driving this change. Inefficient products are not only bad for the environment but are also the main cause for short battery life on handhelds, and cause a significant increase in running costs for base stations (with increased energy usage and extra costs for cooling). Adding to these pressures, there is now political pressure within the United Kingdom (UK) Government, which is now committed to reducing the amount of CO_2 that the UK emits as a nation, due to the European Union (EU)'s 2020 targets [3].

There are two factors that impact the amount of energy used in the mobile communications industry; the amount of data being sent and received over the network, and the efficiency of the hardware used to send and receive the data. Vodafone published a report in 2017 [4] that details how the energy is used across their business and, as seen in figure 1.1, the total power used is going up year on year despite numerous efficiency improvements detailed in the report. The largest consumer of power are their mobile networks.

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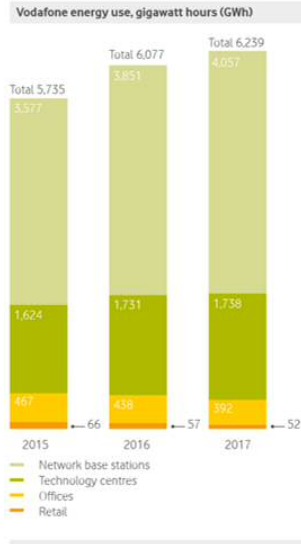


Fig. 1.1: Power usage of the whole of the Vodafone business over the past 3 years. [4]

The increase in power consumption is driven by the ever-increasing user base and the need to expand network coverage. This is shown in a report published by Cisco in 2016, [5], where the data used per month is increasing at an almost exponential rate and predicted to increase for the foreseeable future.

The next generation of mobile networks, 5G, is likely to significantly increase the number of devices connected to the network with the hopes of powering the “smart life”, where every electronic device on a person, or that a person interacts with, connects to the internet, as seen in figure 1.3.

With Vodafone’s report showing in figure 1.1 that most of their power usage is from base stations, in this case 65% of the total energy used by the company, it is required to next look at the power usage within a base station. Looking at how the power is used within a typical base station, it is seen in figure 1.4 that Radio Frequency (RF) Power Amplifier (PA) (Radio Equipment in figure 1.4) is the main consumer of power. As the RF PA is often less than 50% efficient and all the wasted energy is output as heat, the power used for cooling is also due to the RF PA. This means that making the

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RF PA more efficient will reduce the amount of power the radio equipment needs and reduce the amount of power the cooling needs.



Fig. 1.2: Cisco's network usage predictions 2015-2020, [5] a) Data used by region b) Data used by type c) Total number of devices d) Number of wearable devices

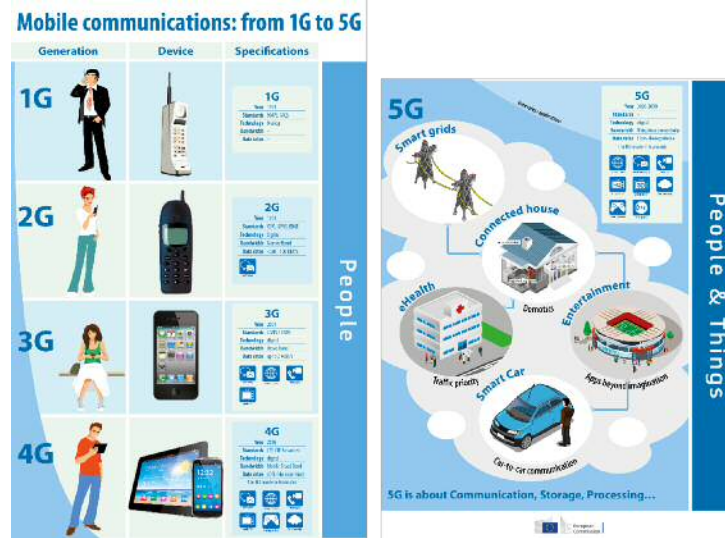


Fig. 1.3: Evolution of telecoms from 1G to 5G Infographic, [6]

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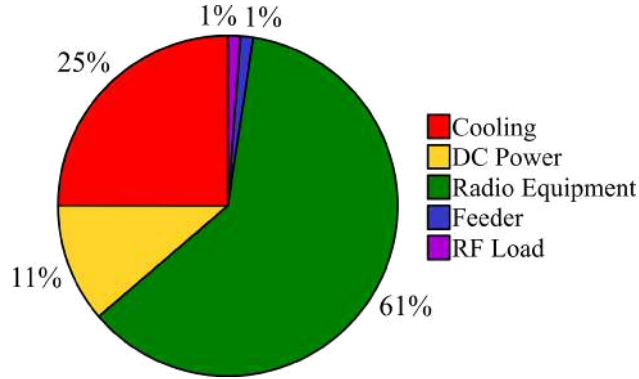


Fig. 1.4: Typical power usage in a mobile base station, [7]

1.2 Research Aims

One overarching aim drives this project:

Increase the efficiency of the RF PA to reduce the power consumption of the mobile communications system.

This thesis meets this aim by three objectives of how this thesis meets this aim:

1. Use waveforms to gain a deeper insight into the failure mechanisms of transistors operating in high efficiency modes.
2. Generate new ways of presenting waveform data that help the designer make highly efficient designs and understand how the transistor technology affects performance.
3. Design of a highly efficient High Power Amplifier (HPA) MMICs using Doherty and continuous mode theory.

1.3 Thesis Overview

To show how the thesis met these objectives the thesis has been arranged into the following chapters.

Chapter 1 - Introduction:

This is the current Chapter and aims to give the reader an overview of where the motivation for this research comes from, and how this thesis meets it.

Chapter 2 - Literature Review:

This section contains all the relevant theory behind the work Chapters in this thesis, it will then go on to look at comparable publications for each section of the thesis and how this work compares.

Chapter 3 - Multi-Harmonic Waveform based VSWR Sweeps:

This is the first contribution Chapter, it presents an advancement to conventional VSWR sweeps that have been previously used to identify and diagnose failure locations of new technologies and PA designs. This advancement was driven by harmonic terminations being critical to achieve objective 1, as they are required to make sure all potential failure conditions are captured and then not presented to the device because of harmonic terminations used in high efficiency designs. This Chapter will develop the theory behind VSWR sweeps and go through a theoretical case study that was performed using these sweeps to predict the peak voltage failure locations without triggering any failures. This showed the need for both multi-harmonic terminations to trigger peak RF voltage failures that would have otherwise gone un-noticed and waveform data to see these peak RF voltages.

Chapter 4 - Case Study of VSWR Failures Using Waveforms:

Building on Chapter 3, this Chapter also directly addresses objective 1 by taking a group of real failures that all have similar fundamental, second and third harmonic impedance locations at the point of failure. Then identify the different causes of failure by first looking at the impedance locations, then adding information typically obtained from a conventional load pull system and then finally waveform data. The additional information waveform data can add, both working alone

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and with conventional data, can help make a quick diagnosis of failures and with added insight into the mechanisms causing the failures. This Chapter also introduces two GaN 50 V FET devices.

Chapter 5 - Using Waveform Data to See the Effects of Knee Walkout:

Two competing GaN 50 V Field Effect Transistor (FET) processes were made available to this project, so their performance was evaluated and compared. One of the problems with FET devices is the knee walks out with increasing drain voltage, which reduces performance. This Chapter presents a new method of analysing how the knee effects the performance of the device, and then applies this to the two devices allowing the performance of each device to be directly compared. The plots that resulted from this are how this thesis meets objective 2.

Chapter 6 - Design of a Continuous Class B Quasi MMIC:

This is the first of two design Chapters that focus on meeting objective 3, where each develop a quasi MMIC design that address different problems. As these two Chapters use the new GaN FET technology, rather than the GaAs Heterojunction Bipolar Transistor (HBT) devices, reliability was not a concern and these designs focus purely on achieving maximum performance. This Chapter's aim was to make a highly efficient broad band PA using Continuous Class B theory as a starting point. It will show the steps taken to design the quasi MMIC and how this compares to a laminate and partial MMIC simulations. Designing for a MMIC over laminate was one of the main challenges, as all S-band designs at Cardiff have been based on laminate so far. Although, the move to a MMIC based design caused a move away from the ideal impedances expected to be presented to a Continuous Class B device, but the quasi MMIC was still able to obtain reasonable efficiencies and bandwidth. The design was then fabricated and measured, with lower than simulated results. The lower than predicted performance is thought to be because the measurements were performed using a

1. INTRODUCTION

Continuous Wave (CW) source. The CW measurements will cause the device to heat up, which is thought to be the cause of the current compression in the waveforms, seen in Chapter 6 and figure 6.18. The device would need to be re-measured using a pulsed input signal to obtain a performance that is closer to the simulated results. This unfortunately is where time ran out for this project, but the partnership with Qorvo is ongoing and so future work will be able to investigate the difference between simulated and practical results.

Chapter 7 - Design of a Doherty Quasi MMIC:

One weakness of the Continuous Class B, and most other classical modes (A, B, C etc.), is their back-off performance, which is important when high peak to average signals are being transmitted and the RF PA is mainly used in a backed-off state. To address this problem a parallel design was developed based on the Doherty topology, which can retain performance over back-off. Doherty based topologies are inherently bandwidth limited by the quarter wave line that are used to realise them. Chalmers University have done a design based on Doherty, [8], that has good back off performance over a wide bandwidth, 1 - 3 GHz, which inspired the initial design phase of this MMIC Doherty. Although, due to the transmission lines used in the Chalmers design, the design had to be changed from the original to make it compatible with the MMIC design space. It was then changed again to make it more MMIC friendly and broadband by using the unique periphery that the GaN 50 V device offers.

2

Literature Review

2.1 Introduction

This Chapter will introduce the basic concepts that need to be known before following the main work of this thesis, and to review published work in the same area. Due to the varied nature of the thesis, this Chapter will be split up into different sections, each covering a different theme in the thesis:

- **Waveform Engineering:** This section will cover what waveform engineering is and how a waveform based load pull system works and compares to a conventionally used system and what the advantages are of using one.
- **Transistor Theory:** To understand the results of any stress test, or PA design it is first required to understand the nature of the transistors used. This section will go over the basics and physics of both the Bipolar Junction Transistor (BJT) and FET based transistors.
- **VSWR Sweeps and Stress Tests:** This section will introduce and explain what a VSWR sweep is, how and why it is used, and then show how it is carried out. It will also look at other stress tests that are employed and how they compare and what waveform based VSWR can add.
- **PA Theory and Continuous Modes (CMs):** Starting with classical PA modes of operation, the principles of PA design will be covered leading on to CMs. These identified that the classical modes are just one point in a continuum of impedances that obtain the same performance. This section will go into how that is accomplished for the Continuous Class B and reviews its implementation as a PAs.

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- **Doherty PA:** This section will go over the theory of the Doherty PA which has better back-off performance compared to classical modes. This section will also look at how the Doherty accomplishes this and look at some comparable designs that have been done using the Doherty topology.

2.2 *Waveform Engineering*

Waveform engineering is when current and voltage waveforms are used to generate and use data that can only be obtained from waveform measurements. Waveform measurements enable the plotting of waveforms, dynamic load lines, polar plots, along with numerous extra variables that can now be plotted on linear plots such as peak RF voltage and current.

The waveforms can be directly measured on an oscilloscope, which can suffer from limited RF bandwidth and limited dynamic range or limited resolution. They also tend to be slower at measuring than their Vector Network Analyser (VNA) counterparts due to the need to average. A different method of measuring waveforms is to use a VNA with a phase reference. This allows the speed of the VNA and its large dynamic range to be used to measure waveforms. It achieves this by having an external phase reference to re-align the phases of the measured frequencies to then re-form the waveform.

The real power of waveforms is to gain insight into how the device is operating and explaining the cause for performance of a PA. This deeper insight into how the device is operating can allow for a closer link between the ideal theory and the actual operation of the device, as the ideal theory uses waveforms to define the mode of operation. The application of waveform engineering in PA design has shown that the ability to view and control the waveforms can lead to high efficiency modes being realised. One example of how waveform engineering was used to achieve high efficiencies was seen in work done at Cardiff on a 10 W Cree GaN chip [9]. Looking at the waveforms in figure 2.1, they conform very closely to the ideal theory for inverse class-F, with half-wave rectified voltage and square current. This design was able to achieve efficiencies of 81.5 % using waveform engineering.

2. LITERATURE REVIEW

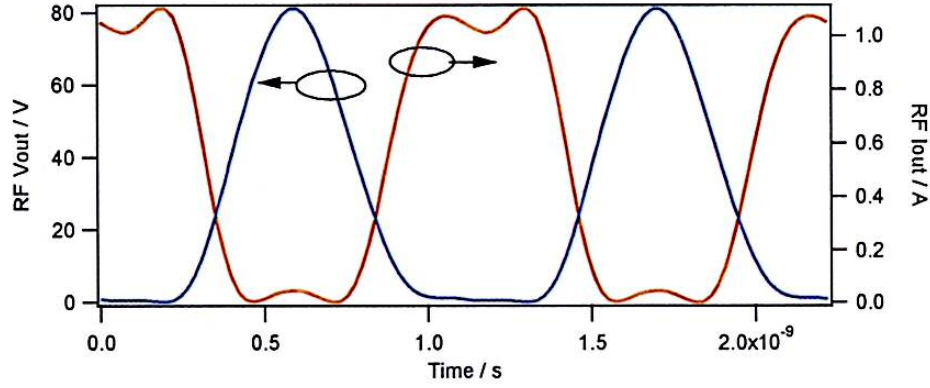


Fig. 2.1: Measured inverse class-F RF waveforms from a design completed using waveform engineering, [9]

The ability to measure waveforms also means that instead of measuring the consequences of the physical limitations of the device (such as transconductance, output conductance dispersion, RF power and efficiency), it is now possible to see the physical limitations more directly in the waveforms [10]. For example, the effects of surface traps are observed in the RF knee walkout (plotting the RF current waveform vs. the RF voltage waveform to form the dynamic load line), which is also increases with increased drain voltage [11]. An example of knee walkout is seen in figure 2.2

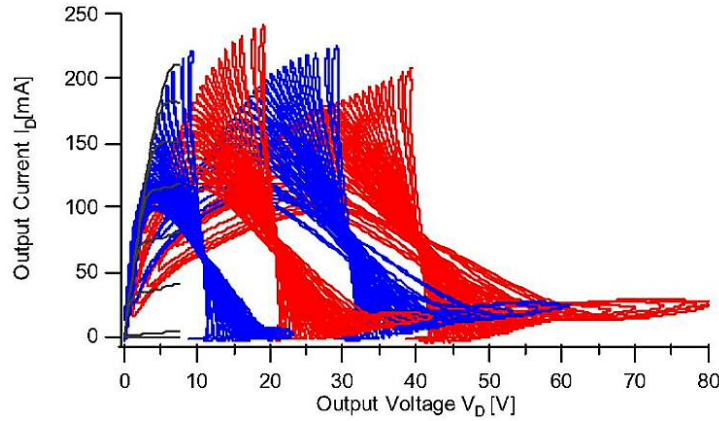


Fig. 2.2: Measured RF Dynamic Load Line (DLL) waveforms showing knee walkout caused by surface traps, [11]

2. LITERATURE REVIEW

The use of waveforms to observe and analyse the physical properties of a device requires the waveforms to be observed in the desired reference plane, which is often the intrinsic current generator plane (intrinsic i-gen) of the device, which is defined as shown in figure 2.3.

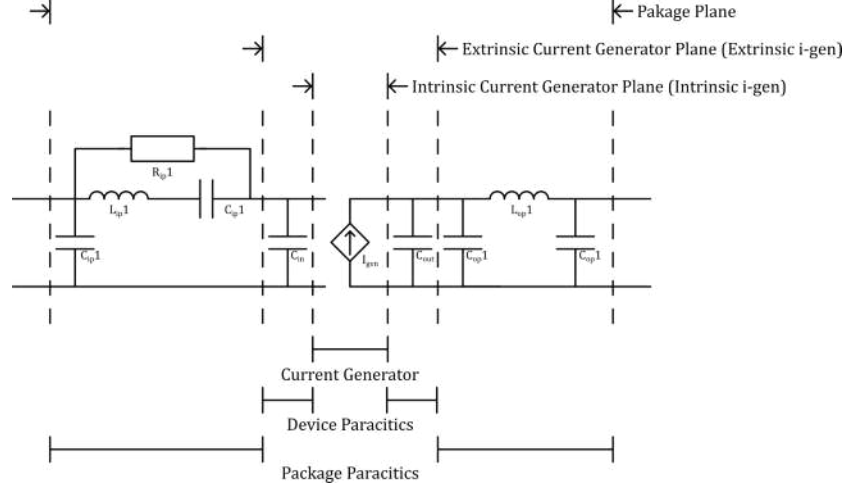


Fig. 2.3: An example of some commonly used components within very basic device model and where this thesis defines the different de-embedding planes.

The need to move down to the intrinsic i-gen plane is to enable the channel's performance to be analysed. This is where the waveforms that relate to the ideal theory will be observed. It is not possible to directly measure the intrinsic i-gen plane and so de-embedding is required. In this thesis de-embedding was performed by using either s-parameter de-embedding which is directly available in the Mesuro load pull software or by using an VI data exported from the Mesuro load pull software and then using ABCD matrix maths to manually de-embed.

2. LITERATURE REVIEW

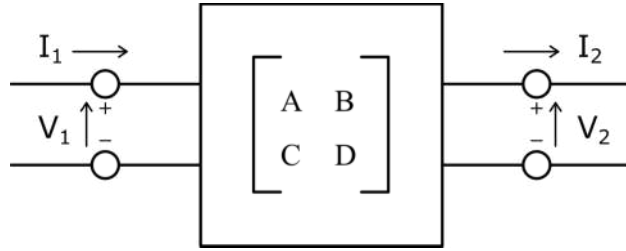


Fig. 2.4: A diagram showing the polarity of the current and voltages and how the ABCD matrix is structured.

The ABCD matrix and equations shown in figure 2.4 and equation 2.1

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad (2.1)$$

$$V_1 = AV_2 + BI_2$$

$$I_1 = CV_2 + DI_2$$

can be used for when the current is flowing out of the device, which is the case for de-embedding the output. When de-embedding the input of the device they need to be re-arranged to make V_2 and I_2 the subject as the direction of current flow is in the opposite direction. This requires matrix division to be performed on the ABCD matrix to move it to the other side of the equation, which gives the equations shown in equation 2.2.

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} \begin{bmatrix} A & B \\ C & D \end{bmatrix} \frac{1}{AD - BC} = \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad (2.2)$$

$$V_2 = \frac{DV_1 - BI_1}{AD - BC}$$

$$I_2 = \frac{-CV_1 + AI_1}{AD - BC}$$

The limitation of this method is that it can only de-embed lumped element components and if more complex de-embedding is required, for example if a varactor is present, this method of de-embedding can only provide an estimate to what the waveforms will look like.

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2.2.1 Load Pull

Load pull systems are systems that can automate the process of changing the load presented to the Device Under Test (DUT) [12]. This makes load pull systems ideal tools to measure transistors with, as it allows the fundamental and harmonic impedances to be swept and the optimum found experimentally rather than relying on models and simulations. Most modern load pull systems can change their reflection coefficient with relative ease allowing for a wide range of impedances to be presented to the DUT. Load pull systems were used in this thesis during the development life cycle of a transistor, in particular to look at the reliability of the device. The load pull system allows for the optimum to be found and then VSWR reliability tests to be performed on the new processes. They can also be used to help develop the PAs matching by allowing tuning of the fundamental, second and third harmonic impedance to find the optimum, which can then be used for Computer Aided Design (CAD) based designs. Another option for the PA designer is to verify and/or generate a non-linear model which can then be used to simulate the transistor response in a CAD based design environment to reduce the time spent taking load pull measurements. There are two main load pull systems on the market, passive load pull and active load pull, where Cardiff and this project use active load pull.

Passive Load pull

The majority of load pull systems today use passive load pull. They get their name from the passive tuners they use to perform load pull, often made from tunable transmission lines, to transform the impedance away from a matched impedance, as shown in figure 2.5. The passive tuner works by tuning either the main line length or the stub length to move the impedance away from the matched load. The arrows correspond between figure 2.5 (a) and figure 2.5 (b) to show the direction the different lines will move the impedance. A practical implementation of a passive tuner can be seen in [13], the advantages of passive load pull are:

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- **Stable:** It does not need to keep presenting an active load, once the load is set it does not drift away from the desired impedance.
- **Safer:** While damage can be caused to the DUT if care is not taken, the amount of power reflected back to the device is always less than or equal to the output of the device. This means that a negative impedance can never be presented to the device. Also, due to the passive nature of the load, it will keep presenting the impedance even after power to the load pull system is lost, preventing any sudden changes in impedance if power is lost to the system.
- **Simpler:** A modern passive tuner can often consist of less parts, which allows it to take up less space and cost less.

While this is a compelling list of advantages over active load pull systems, there are disadvantages:

- **Losses:** While modern passive tuners are improving and the losses within them are being reduced, due to internal losses they cannot totally reflect the output power of the device back to it and achieve any reflection coefficients of 1.
- **Slower:** Passive load pull is a mechanical process where it takes time to move the components inside making it slower than a comparable active system, which can change its phase and magnitude as fast as the signal source can change. The calibration time of the passive system also tends to be slower as the tuner needs to be characterized whereas with the active system just the RF path from the DUT to VNA needs to be characterized.
- **Unknown harmonic termination:** Where fundamental only passive load pull is used the harmonic impedances are left free which can cause misleading results. As this thesis will show, the harmonic impedance terminations can significantly affect the performance of the device. While this is not something that cannot be overcome it is often overlooked in passive load pull systems.

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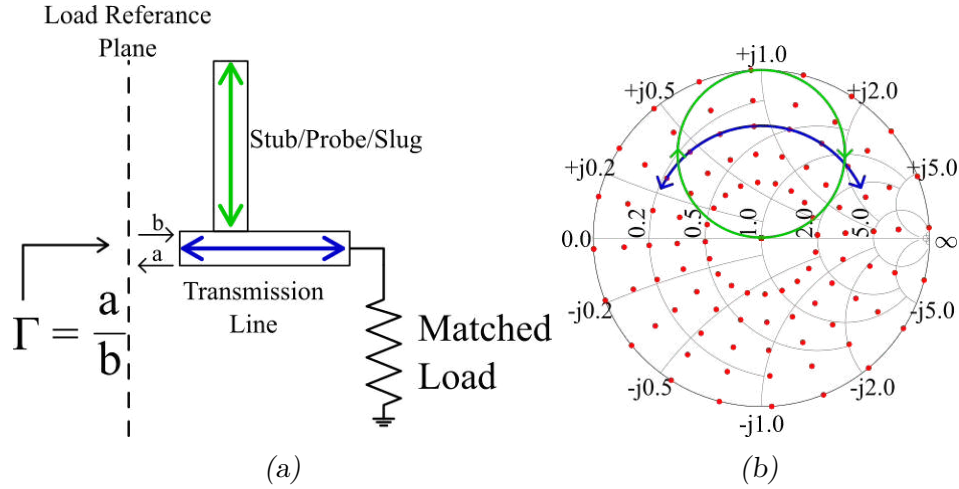


Fig. 2.5: A basic example of how passive load pull works. (a) The components within the load tuner. (b) The direction the load tuner will move the load on the Smith Chart

Active Load pull

Active load pull achieves the same goal as passive load pull, but instead of presenting a lumped/passive load it presents an active load. This works on the premise that if the passive load shown in figure 2.6 (a) presents a load determined by equation 2.3,

$$\Gamma = \frac{a}{b} \quad (2.3)$$

then the reflected 'a' waves magnitude and phase is determined by the load attached to the DUT. To then replace this passive load with an active load, the forward and reflected waves, 'a' and 'b', need to be isolated with the 'a' wave being generated/controlled by the load pull system and the 'b' wave terminated into a load. This will allow the user to manipulate the 'a' wave to represent any impedance desired.

This is practically achieved by terminating the 'b' wave into a load using a circulator, meaning nothing from this wave is reflected back to the DUT. If the system was left like this then it would be presenting a perfect match. To move the impedance away from being perfectly matched and allow the load to move freely, a phase coherent signal generator is required to feed a

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signal back into the DUT. The signal generator needs to be fully controllable in both its phase and magnitude to be able to emulate any load. Another consideration of the signal generator is the power it can output, as often it will not produce more than one or two watts of output power (30-33 dBm) and so not be able to load pull larger devices. For devices that requires more power to load pull than the signal generator can supply, the active system will only be able to present impedances within a restricted area of the Smith Chart. To overcome this the signal will need to be amplified by a drive PA to achieve required levels. Finally, the signal is fed back into the output of the device via the circulator, so emulating the desired impedance, as shown in figure 2.6 (b).

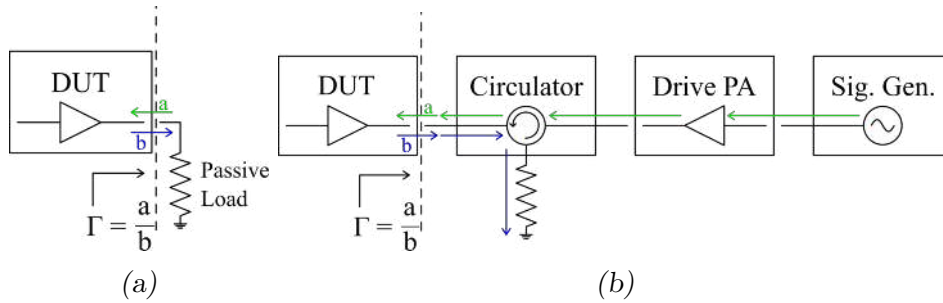


Fig. 2.6: A basic example of how active load pull works. (a) How a passive load works (b) How active load pull simulates this load

As with the passive load there are various advantages to this system:

- **Powerful:** The 'a' wave is as big as the drive PA can make it, meaning that the $\Gamma = 1$ boundary is now accessible and impedances outside the Smith Chart can now be realized.
- **Fast:** As mentioned for the passive system as a negative, active load pull can move the load as fast as the signal generator can change. To take full advantage of the fast switching time, a closed loop active load should be used to reduce the amount of iterations required to set the impedance to the right location. One example of this is Envelope Load

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Pull (ELP) [14], which has two advantages; 1. Allows the load to move very quickly to the desired location. 2. It holds the load in place very accurately.

But there are negatives:

- **Power Levels:** If a large enough drive PA is used then it becomes possible to inject significant amounts of power into the DUT, which could cause failure if care is not taken.
- **Active:** Active loads require a power source to present the impedance. If power is lost to the system there is no way to know what impedance will be presented to the DUT as the system shuts down, so could move the load somewhere dangerous before anything can be done to prevent it.
- **Complex:** As shown in figure 2.6 the active load pull system is more complex than a passive load, and increased complexity often comes with increased cost.

Cardiff has invested in active load pull research systems with all 5 of its systems being driven by active loads, which in turn means every measurement in this thesis was taken on an active load pull system, with an example shown in figure 2.7.

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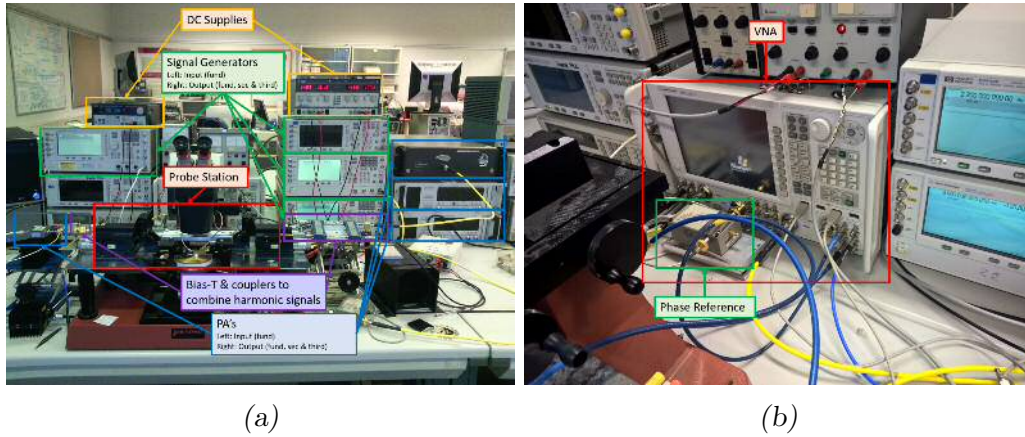


Fig. 2.7: A picture of the PNA-X based load pull system at Cardiff University used to make the majority of the measurements in this thesis. (a) Front view with probe station (b) PNA-X configuration with comb generator as the phase reference.

2.2.2 Waveform Receiver

The other building block in creating a system capable of measuring waveforms is a microwave receiver, as shown in figure 2.8, where a traditional load pull system will use a VNA and a waveform based system will use an oscilloscope or VNA with phase reference. The conventional VNA based system will allow measurements to track the impedance and power (if calibrated correctly), but not the large signal waveforms. This is due to the relative phase of the individual harmonic waves measured by the VNA not being referenced to each other. This means that when the different harmonic components are summed together using what the VNA measured alone it is often wrong and different every time. To fix this an external phase reference needs to be added to the VNA, which means that the VNA needs to have at least 3 ports so that there is a third measurement that is known and unchanging. The software can then use this third measurement to correct the individual harmonic components so that when they are used to generate the large signal waveform they reconstruct the correct wave.

Looking more at the differences shown in figure 2.8, whilst knowing the

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performance does enable designs to be done, it only gives limited diagnostic capabilities into why the performance is increasing or dropping, what mode of operation the device is operating in, or if the DUT does fail, answering why. Another added benefit of a system capable of measuring waveforms is that the waveforms can be converted into a VI matrix and so be de-embedded using an ABCD matrix approach as shown in figure 2.4, allowing for the waveforms at the various levels of de-embedding to be seen including the intrinsic i-gen plane if de-embedding network is known. Waveforms can also aid in finding the de-embedding network, as knowing the physical limits of the device at the intrinsic i-gen plane allow the user to determine if the waveforms are truly de-embedded down to the intrinsic i-gen plane or not and correct the current de-embedding.

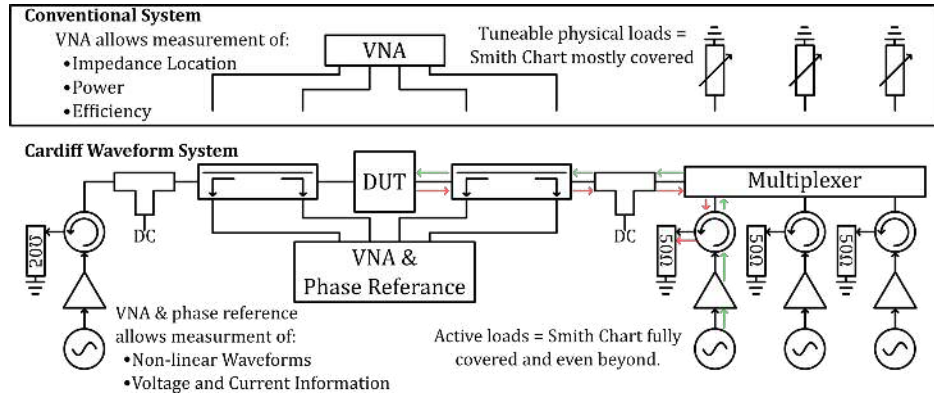


Fig. 2.8: A comparison of a conventional load pull system with passive loads vs. Cardiff waveform based load pull system using active loads

2.3 Transistor Theory

This section looks at the main differences between BJT and FET based devices and why being able to measure peak RF voltage is critical for stress testing BJT based devices, as they are more vulnerable to peak voltage stress. The basic structure of FET and BJT devices and the layer stack for a HBT and a High Election Mobility Transistor (HEMT), are seen in figure 2.9 and

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figure 2.10 respectively. In both figures electrons are used as the main charge carriers.

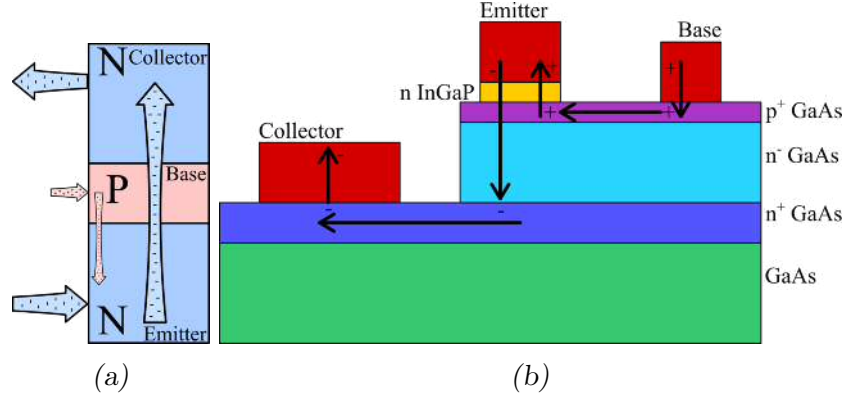


Fig. 2.9: The structure of a BJT device. (a) An ideal view of the diode junctions. (b) A process stack for a HBT device, [15].

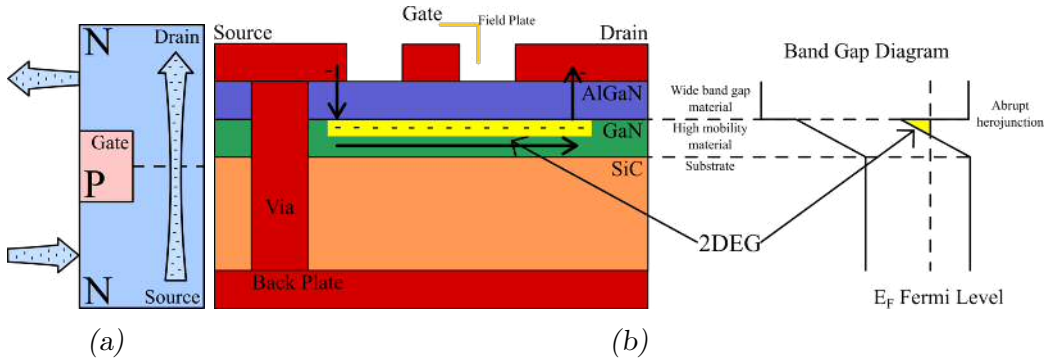


Fig. 2.10: The structure of a FET device. (a) An ideal view of the diode junctions. (b) A process stack for a HEMT device, [16].

2.3.1 Diode Theory

Both devices operate using diode junctions, the BJT has a forward biased diode junction with current flowing through it, whereas the FET uses a

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reverse biased diode junction to control the current channel size. Both junctions are governed by the diode equation, shown in equation 2.4,

$$I = I_s e^{\left(\frac{V_a}{nT_K}\right)} - 1 \quad (2.4)$$

and the thermal voltage referenced in it is shown in equation 2.5.

$$V_t = \frac{kT_K}{q} \quad (2.5)$$

The diode equation shows that for increasingly positive values of V_a the current will be exponentially increasing, as shown in figure 2.11, but for increasingly negative values of V_a the equation tends to $-I_s$. But, as the device is not an ideal mathematical equation it will reach physical limits. For the region of positive V_a the current flowing through the junction will saturate and the current will level off with increasing values of V_a . For the reverse bias region, where V_a is negative, as the magnitude of the negative voltage increases the velocity of the charge carriers will increase, until eventually they are carrying enough energy ($W_K = \frac{1}{2}mv^2$) to ionise other electrons causing an avalanche effect, where a dramatic increase in reverse current is seen. The avalanche breakdown most commonly occurs when the depletion region is lightly doped and long enough to allow the electrons to accelerate enough to cause the cascading effect to take hold. There is another breakdown mechanism, known as Zener breakdown, that most commonly occurs in heavily doped diodes, where the depletion region is very thin (often caused by the high doping of the materials). The thin depletion region then allows for quantum mechanical tunnelling to occur when enough potential is applied. This then allows for a large current to flow through the apparent “wall” in the way of the electrons.

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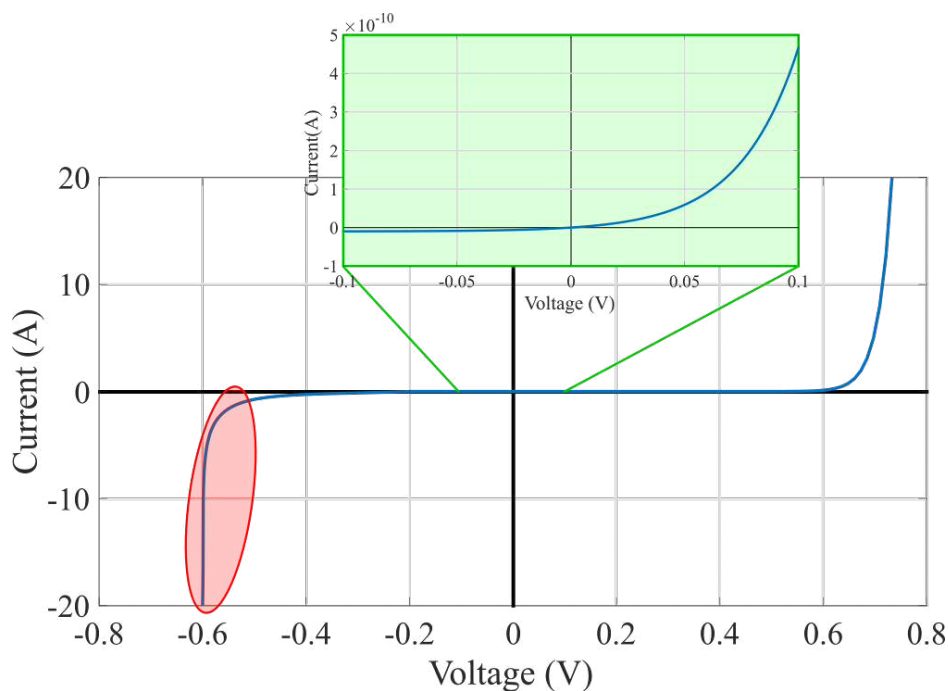


Fig. 2.11: A plot showing the diode equation using typical values for silicon, plotted -0.2 to 0.8 V. From -0.8 to -0.2 V were added after to show the typical behaviour of a Zener diode.

To apply equation 2.4 to BJT theory, it is important to note that the diode current is made up of both electrons and holes which, in the case of the BJT, are subtracted from each other. This means it is important to understand what factors affect the two currents, which can be done by expanding the diode current equation, shown in equation 2.6.

$$I = qA \left(\frac{D_n n_{p0}}{L_n} + \frac{D_p p_{n0}}{w_n} \right) \left(e^{\frac{V_a}{V_t}} - 1 \right) \quad (2.6)$$

Assuming a short diode junction (for which width/length is much smaller than 1, and causes most of re-combinations to happen in the conducting contacts, rather than in the depletion region) equation 2.6 can be written as

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equation 2.7

$$I_{E,n} = qn_i^2 A_E \left(\frac{D_{n,B}}{N_B w_b} \right) \left(e^{\frac{V_{BE}}{V_t}} - 1 \right) \quad (2.7)$$

for the electron current across the junction, and equation 2.8

$$I_{E,p} = qn_i^2 A_E \left(\frac{D_{p,E}}{N_E w_e} \right) \left(e^{\frac{V_{BE}}{V_t}} - 1 \right) \quad (2.8)$$

for the hole current across the junction.

Key points to note from these equations are that the current through the junction is dependent on the voltage across it and the area and carrier diffusion properties of both materials. The doping of both materials also affects the current, as a more heavily doped material will provide more free carriers and so the current produced by them will be increased. Doping will also affect how many carriers make it to the contact or re-combine early.

2.3.2 BJT and HBT Theory

A BJT is constructed by forming two diode junctions back to back, using three ports, as seen in figure 2.9; the emitter which is where the electrons enter the device, the base which controls the current leaving the emitter and the collector which is where the electrons leave the device. They are made from the same material that then gets doped to form the diode junctions, using the same material reduces the stress on the bonds at the junctions and helps prevent defects in the structure.

The current flowing in the device is also shown in figure 2.9, where it is seen that both positive (holes) and negative (electrons) current flows in the structure. This is where the BJT gets the ‘bi’ polar part of its name, bi being Latin for ‘having two’ as this device ‘has two’ charge carriers flowing within it.

The configuration for the devices tested in this thesis were common emitter, meaning that the emitter port is grounded and so both the base and collector are biased relative to the emitter, and the currents within the de-

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vice under normal operation are seen in equation 2.9.

$$I_E = I_C + I_B \quad (2.9)$$

To make sure the device has gain and is useful as an amplifier, the two diode junctions need to be biased as follows:

Emitter/Base Junction: This is the input junction and controls how much current flows from the emitter into the base. This junction will be forward biased under normal operation and so there will also be a reverse current from the base into the emitter of minority carriers. The reverse current needs to be much smaller to allow the transistor to achieve gain. The relationship between forward current from the emitter into the base to the reverse from the base into the emitter is proportional to the doping in each. As such, the doping in the emitter will often be much larger than the base to reduce the reverse current compared to the forward. The relationship between the forward and reverse currents across a diode junction is a linear relationship, so it is universally common to define the input of the base by the base current rather than the base voltage across the diode, which allows the performance of the BJT to be very linear.

Base/Collector Junction: As the base is very thin compared to the rest of the device, the current from the emitter will have enough physical momentum to keep flowing into the collector, although a small amount will not and recombine, leaving the device via the base terminal, this will increase the base current, which is undesired. To reduce this current and encourage as much of the current from the emitter to flow into the collector as possible the base/collector junction is reverse biased, as the majority carriers from the emitter are the minority carrier in the base and reverse biasing the base collector junction will encourage any minority carriers from the base into the collector. It will also stop any back flow of electrons from the collector back into the base.

To help understand the flow of current through these junctions, band gap

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diagrams and fermi levels are often used to show how the BJT works, shown in figure 2.12. When the BJT is put into forward bias it is seen that the base fermi level was raised to allow the electrons to flow into the base, and then the effect of reverse biasing the base collector junction is now clearly seen, allowing the electrons to then be swept into the collector.

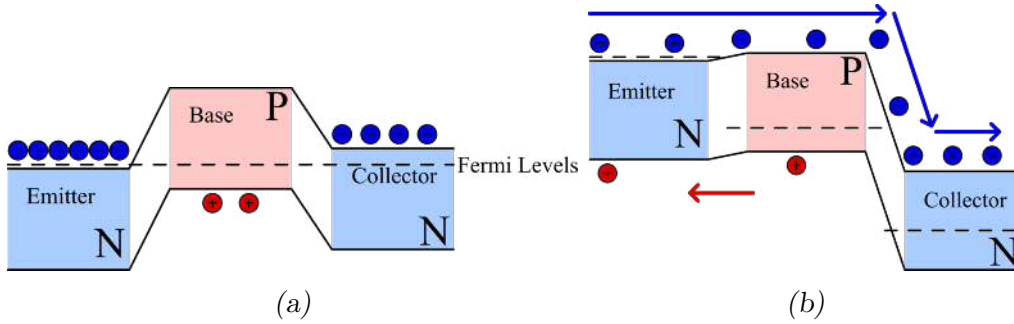


Fig. 2.12: Band diagram and fermi levels for (a) BJT at rest and thermal equilibrium (b) BJT forward biased

Because of the recombination that occur in the base not all the current injected in by the emitter makes it to the collector. Alpha is the current gain between the emitter and the collector and represents how much of the current leaving the emitter makes it to the collector, as seen in equation 2.10.

$$\alpha = \frac{I_C - I_{BC0}}{I_E} \quad (2.10)$$

As the reverse current is often very small equation 2.10 is often just written as equation 2.11.

$$I_C = \alpha I_E \quad (2.11)$$

Alpha is also a measure of efficiency, as in an ideal world all the current injected into the emitter will make it to the collector.

Current gain between the collector and the base is known as beta, which is often the parameter that is used when designing a PA as it represents

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the gain from the input to the output, as seen in equation 2.12.

$$\beta = \frac{I_C}{I_B} \quad (2.12)$$

Then using equation 2.9 with equation 2.12 gives equation 2.13.

$$I_C = (\beta + 1)I_B \quad (2.13)$$

Using equation 2.9 and replacing I_E and I_B with re-arranged versions of equation 2.11 and equation 2.13 respectively, gives equation 2.14,

$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta} \quad (2.14)$$

finally dividing through by I_C and re-arranging gives the relationship between α and β , seen in equation 2.15

$$\beta = \frac{\alpha}{1 - \alpha} \quad (2.15)$$

Within a BJT the same material is used in all three sections and then doped to be either n-type or p-type. As a result the forward and reverse current across a diode junction is given by equation 2.7 and equation 2.8. As stated, when designing a PA it is desirable to have a high beta for a good power gain performance. This requires the reverse current, from the base to the emitter, to be as small as possible and the forward current, from the emitter to the base, to be as large as possible. One method of achieving this is to heavily dope the emitter and to only lightly dope the base, as the currents are proportional to the number of charge carriers available. But if you only lightly dope the base then its resistance will also go up, and reduce the carrier diffusion length, leading to an increase in the base current. Also, a heavily doped emitter will increase the emitter/base capacitance which needs to be small to operate at high frequencies.

This is one of the problems the HBT tries to solve. The HBT is no longer made from one material and instead uses a wider band gap material for the

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emitter; and so making a larger barrier for the reverse current moving from the base into the emitter, which is clearly seen in figure 2.13. Now when the device is forward biased the reverse current from the base still has a barrier to overcome, which reduces the reverse current and allows for more flexibility in base doping.

This is where the HBT gets its name, as it now has a heterojunction in it, as “hetero” is Greek for “different”, as the emitter-base junction is now made of two different materials.

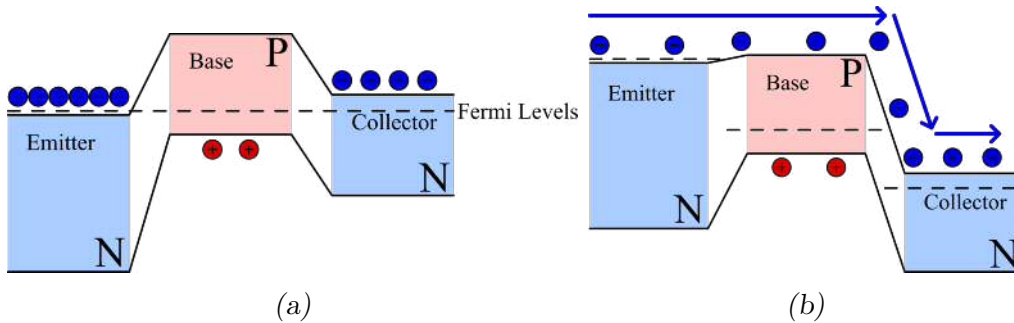


Fig. 2.13: Band diagram and fermi levels for (a) HBT at rest and thermal equilibrium (b) HBT forward biased

Next, looking at the base-collector junction of a BJT or HBT, it is noted that this junction will have a larger voltage differential across it than the emitter-base junction. The voltage across the base-collector is also reverse biased, both of these together makes it the junction that will often fail due to voltage stress. Within the junction these high reverse bias voltages cause impact ionisation in the depletion region, which potentially will cause an avalanche effect. Avalanche breakdown is characterised either with an open emitter, applying the reverse bias between the base and the collector, or with an open base and applying the reverse bias between the emitter and the collector. The impact ionizations will cause an increase in holes flowing into the base due to all the dislodged electrons, which will either leave the device via the base (open emitter) or be forced into the emitter (open base). For the open base characterization, the flow of holes into the emitter from impact ionisation will cause the emitter-base junction to go into forward

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bias, or further forward biases it, and cause an increase in current leaving the emitter and so entering the collector, which increases the avalanche effect. Avalanche breakdown can cause lattice damage due to the impact ionisations or cause thermal damage due to the increased currents flowing. Avalanche breakdown is characterised by the multiplication factor, which is the ratio between normal operating current and the current under breakdown. For the collector-base junction with an open emitter, the multiplication factor is seen in equation 2.16,

$$M_{CB} = \frac{1}{1 - \left(\frac{V_{CB}}{BV_{CB}} \right)^n} \quad (2.16)$$

which is related to the applied voltage and the breakdown voltage for the collector-base junction, which was formed from the general equation seen in equation 2.17.

$$M = \frac{1}{1 - \left(\frac{V_a}{BV} \right)^n} \quad (2.17)$$

When operating with a common emitter and an open base, the current flowing into the collector is made up of three parts:

- Current due to thermal generation.
- Current due to impact ionisation, which is the collector current multiplied by the current generation factor for the collector-base junction, G_{CB} .
- Current injected by the emitter, which is the hole current multiplied by beta and as the base is open, the hole current is equal to the sum of the other two currents.

The equation for the current injected by the emitter is seen in equation 2.18,

$$I_C = I_B + G_{CB}I_C + (I_B + G_{CB}I_C)\beta \quad (2.18)$$

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and then re-arranging to make I_C the subject and using equation 2.19,

$$G = \frac{M - 1}{M} \quad (2.19)$$

where $M = M_{CB}$ as the ionising occurs in the collector-base junction, gives equation 2.20.

$$I_C = \frac{(\beta + 1)I_B}{1 - \left(\frac{M_{CB} - 1}{M_{CB}}\right)(\beta + 1)} \quad (2.20)$$

When avalanche breakdown is occurring the current, I_C , tends to infinity. Equation 2.20 tends to infinity when the denominator tends to 0, which happens when equation 2.21 is true.

$$(\beta + 1)\left(\frac{M_{CB} - 1}{M_{CB}}\right) = 1 \quad (2.21)$$

Re-arranging this to make M_{CB} the subject gives equation 2.22,

$$M_{CB} = \frac{(\beta + 1)}{\beta} \quad (2.22)$$

then finally equating equation 2.16 and equation 2.22 and rearranging to make the V_a the subject, which in this case is V_{CE} . Then as M is the case for avalanche breakdown, V_a is the breakdown voltage under open base operation, so BV_{CE} , as seen in equation 2.23.

$$BV_{CE} = BV_{CB} \frac{1}{(\beta + 1)^{\frac{1}{n}}} \quad (2.23)$$

This is the breakdown under common emitter configuration, which is how the devices used in this thesis are configured. It shows that the breakdown voltage will be reduced compared to common base mode and why peak RF voltage failure is a particular concern for BJTs and HBTs in common emitter mode.

Another cause of breakdown within BJT/HBT devices is thermal run-

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away, which is where an increased junction temperature leads to the bandgap energy on the materials to decrease and so the base-emitter junction potential to drop. This in turn causes the emitter current to increase. Modifying the diode equation in equation 2.4 to fully show the effects of temperature on the channel gives equation 2.24,[17].

$$I = I_s e^{\left(\frac{q}{kT_K} (V_{BE} - R_E I_E - R_B I_B + R_{TH} \phi I_C V_{CE}) \right)} \quad (2.24)$$

Added to this when the device is operating at high voltages the current bends over on itself and so for certain voltages there are two possible current solutions, as seen in figure 2.14. If a device has multiple fingers some fingers may go into the high current state and others into the low current state. As a result the high current fingers will heat up and are likely to thermally run away. One method to help prevent this from happening is to add a resistance to the emitter, or add base ballast resistors.

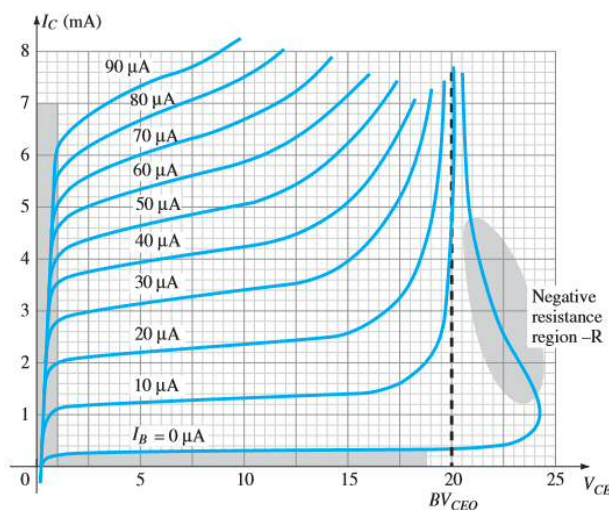


Fig. 2.14: DC characteristics of a BJT operating in common emitter mode, highlighting the breakdown region at high voltage. [18]

Both avalanche and thermal runaway can feed into each other and can

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be triggered by high voltages on the output of the device. This is the reason for wanting to be able to see peak RF voltages. When performing reliability tests on a BJT or HBT it is important to be able to both trigger and observe any potential RF voltage peaking effects.

2.3.3 FET and HEMT Theory

The FET uses the diode junction in a fundamentally different way. This time instead of current flowing through the diode junction, the FET uses the depletion region formed by a reverse biased junction to control the width of the channel that charge carriers flow through. This leads to ideally no current flowing out of the gate, and making this a voltage controlled current source. This effect can be seen in figure 2.15.

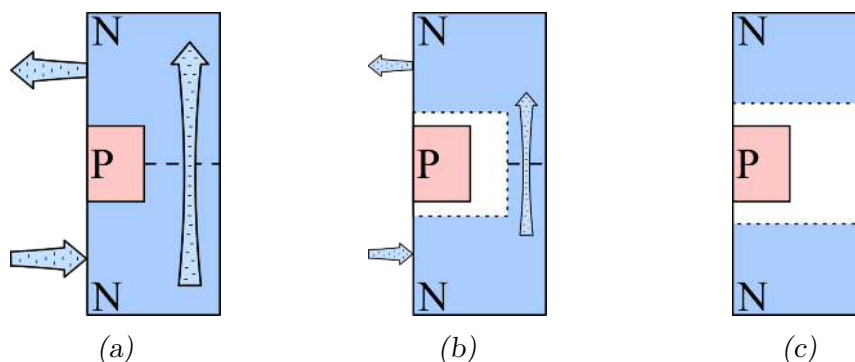


Fig. 2.15: How a FET controls the current flow using the depletion region between the gate and the drain/source (a) No bias on the gate. (b) Small negative bias. (c) Enough negative bias to “pinch” the device off.

The changing width of the channel causes the channel resistance to change with it, once the channel is fully open or closed the channel resistance will then become constant. This effect is seen when plotting out the transfer characteristics of a FET device, as seen in figure 2.16 (a).

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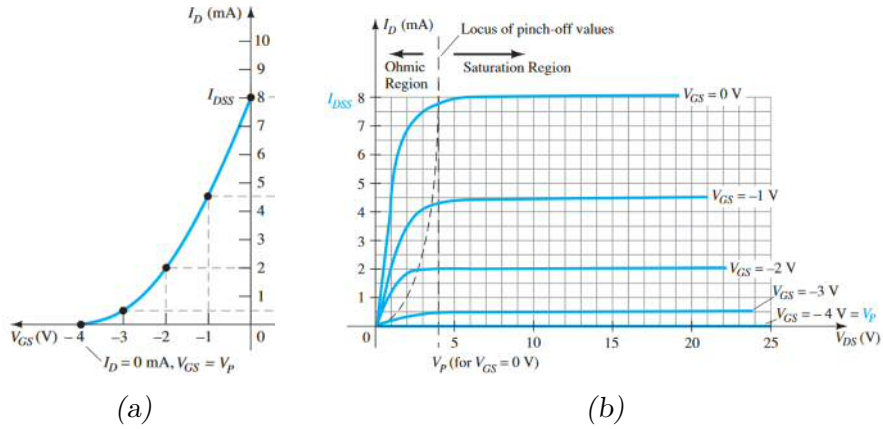


Fig. 2.16: Direct Current (DC) characteristics of a FET device (a) Transfer characteristics (b) Output characteristics. [18]

When the FET is in the ohmic region, as shown in figure 16 it is possible to measure the impedance of the channel, which is characterised by equation 2.25.

$$R_{DS} = \frac{R_0}{\left(1 - \frac{V_{GS}}{V_P}\right)^2} \quad (2.25)$$

In a BJT the input and output current relate to each other in a linear manner as they both relate to the voltage across the diode junction, as seen in equation 2.7 and equation 2.8, but the link between input voltage and output current for FET devices is not linear. The diode junction is governed by Shockley's diode equation, seen in equation 2.26,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad (2.26)$$

where the squared term causes an exponential relationship rather than a linear one. These equations are still bound by the physical limits of the device, I_D will saturate eventually and at the other extreme reduce to 0. These two physical limits of the FET operating in depletion mode are called I_{DSS} which is the current when $V_{GS} = 0$ V as I_D will start saturating beyond this point, and V_P which is the value of V_{GS} that $I_D = 0$ A. By using

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a reverse biased diode junction, it allows a large current to be controlled by a small voltage, with ideally no power dissipated at the input due to the reverse biased junction not conducting any current. It also means that FET based devices are not vulnerable to the thermal runaway effect, as there is no current flowing through a forward biased diode junction. The transconductance, g_m , is the measure of the change in V_{GS} to I_D , as seen in equation 2.27.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad (2.27)$$

An effect of the non-linear relationship between V_{GS} and I_D is that g_m becomes bias dependant, as seen in figure 2.17, where the changing gradient of the transfer characteristic shows that as V_{GS} is increased so does g_m .

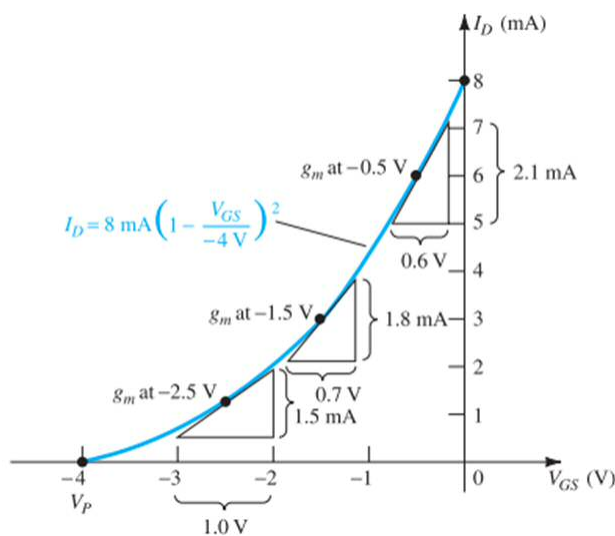


Fig. 2.17: Plot showing drain current vs. gate voltage, using the gradient to find g_m [18]

The relationship between g_m and V_{GS} is seen in equation 2.28,

$$g_m = \frac{2I_{DSS}}{|V_P|} \left(1 - \frac{V_{GS}}{V_P}\right) \quad (2.28)$$

which is formed by differentiating equation 2.26 with respect to V_{GS} . Using

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equation 2.28 and looking at the case for when $V_{GS} = 0$ V gives g_{m0} , which is seen in equation 2.29.

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} \quad (2.29)$$

As I_D starts to saturate beyond the $V_{GS} = 0$ V, g_{m0} represents the point at which g_m is maximum, putting g_{m0} back into equation 2.28 gives equation 2.30.

$$g_m = g_{m0} \left(1 - \frac{V_{GS}}{V_P} \right) \quad (2.30)$$

The performance of a FET based device can be increased by reducing the resistance of the channel or increasing I_{DSS}/mm of the channel. Reducing the resistance will increase I_D for a given V_D and V_G , from $V = IR$, which will allow an increase in g_m , from equation 2.27. Increasing I_{DSS}/mm will allow larger current swings and so there is potential for more Watts/mm.

These can be achieved by improving the channel through which the current flows. One of the biggest advancements in this area is to confine the electrons into a 2-Dimensional Electron Gas (2DEG) that significantly improves their mobility, [19]. The confinement of electrons in the channel can be done by using a double heterojunction, as shown in figure 2.9. This double heterojunction forms the basis for HEMT devices. The three materials that make up the double heterojunction are: a wide band gap material, a material that has high electron mobility - where the 2DEG is formed, and a base material. The high electron mobility material is often an un-doped intrinsic material, so that it has no dopant impurities to increase resistance. As the high mobility material is intrinsic there are little/no charge carriers natively in it and it needs to gain some from outside itself. These can be from a numerous of different ways:

- **Increased Temperature:** As the temperature increases some of the outer shell electrons will break free and become mobile charge carriers, unfortunately these will be lost if the temperature is reduced.
- **Doping Surrounding Material:** This is probably the most common, as the base material will be doped anyway and is the normal way to

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introduce free charge carriers into the transistor.

- **Piezo Strain:** This is a result of the heterojunction, where the bonds between the two materials do not line up and so puts strains on the joining atoms and the bonds become stretched. When this happens, this can form a di-pole within the atom, which can then become large enough to free an electron into the 2DEG.
- **Defects:** This is not a desirable method to introduce electrons into the 2DEG, but there often are defects in the lattice that then free charge carriers.

Another observation about FET devices is that the current does not flow across the diode junction, unlike with BJT devices, which means they are not susceptible to the same breakdown mechanisms that BJT devices are. This means that FETs tend to be the more robust of the two devices and are heavily used within mobile base stations due to their robust high power handling. Due to the higher power applications FET devices experience higher RF voltage swings which have issues of their own. One problem that occurs due to larger V_{DS} voltages is hot carriers, which is where an electron or hole gains enough kinetic energy to inject themselves (and often trap themselves) into parts of the device they should not be. When this happens they form what is known as traps, which then degrade the performance of the device, and in some cases, make it unusable. The traps often gather between the gate and the drain, as shown in figure 2.18, [20][21], which then form a virtual gate that then causes a loss in performance.

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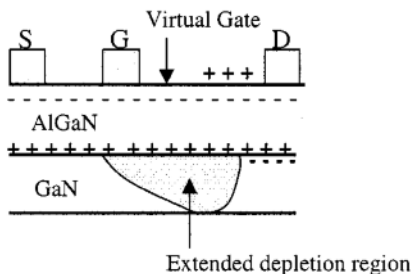


Fig. 2.18: Current flow for effects of traps on a HEMT creating a virtual gate

Hot carriers can also cause impact ionisation, which if the carriers have enough energy cause permanent lattice damage. The four main causes for hot carrier injection are:

Drain avalanche hot carrier injection: This is typically the most common occurrence of hot carriers in normal operation, due to the high voltage on the drain, charge carriers are accelerated to have high kinetic energy which causes impact ionisation. This causes the generation of more charge carriers that may have enough energy to form traps as seen in figure 2.19.

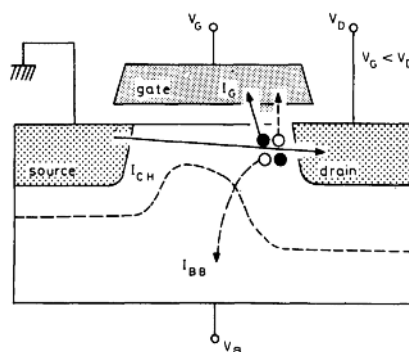


Fig. 2.19: Current flow for drain avalanche hot carrier injection [22]

Channel hot charge injection: This often occurs when the gate and drain voltages are significantly higher than the source, and $V_G \approx V_D$,

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then the charge carriers get driven towards the gate and then leave the device as gate current, reducing its performance, shown in figure 2.20. They may also get trapped near the gate as shown in 2.18.

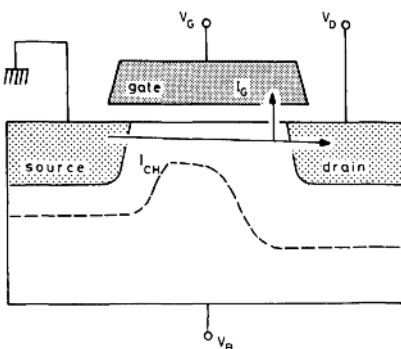


Fig. 2.20: Current flow for channel hot charge injection [22]

Substrate hot charge injection: This is caused when the substrate has a large positive or negative bias on it, to the point where charge carriers gain enough energy to leave the substrate and then form traps. This is not an issue for the devices in this thesis as the base plate is grounded.

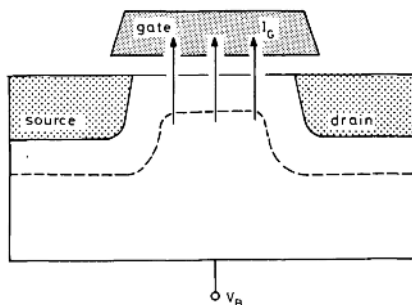


Fig. 2.21: Current flow for substrate hot charge injection [22]

Secondary generated hot charge injection: This effect is very similar to drain avalanche hot carrier injection, but this is where hot carriers are generated by another hot charge.

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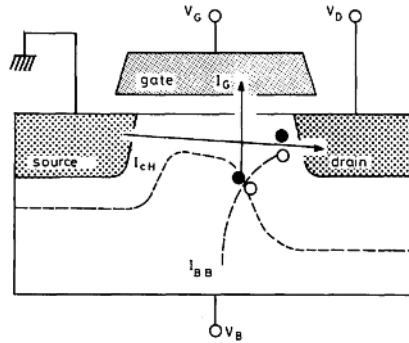


Fig. 2.22: Secondary generated hot charge injection [22]

On top of hot carriers causing performance loss the gate-source junction is reversed biased, so if the voltage is large enough avalanche failure can also occur at the gate in FETs devices. Although it's not common for this voltage to be large and so is a low risk. Also all the FETs devices used in this thesis have the back plate as ground and so also reduces substrate hot charge injection.

While the effects of peak voltage on the BJTs and FETs devices are very different, where BJTs has current flowing through a diode junction and FETs do not. Having current flowing through the diode junction makes BJTs vulnerable to thermal runaway and avalanche breakdown, both of which can cause permanent failure to the device. Compared to FETs where the most common problem is the effects of traps and, in extreme cases, permanent damage caused by impact ionisation. Both cases benefit from the addition of knowing the voltage and current waveforms in the channel in the lead up to these breakdown conditions.

2.4 VSWR Sweeps

The VSWR sweep is where the load is mismatched to form a particular voltage standing wave ratio at the output of the DUT and then the phase is swept through 360° . In the past couple of years there has been an increased interest in VSWR sweeps with the dawn of higher powered applications (plasma

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generation and laser driver circuits, being some examples), that may require higher load mismatch [23], and also with the dawn of GaN as the next material to compete for the high power transistor market. Within the communications market, the high VSWR scenarios could be caused by a variety of things, such as antenna damage, jamming signals or if the device is placed in an unexpectedly reflective location - like a lift. While the applications in this thesis are not for ultra-high power applications, the need to perform VSWR and for the device to survive unexpected harmonic terminations is still required. This is because there is an increasing lack of tolerance in the wider public for any disruption in service cause by devices failing, which can be caused by unexpected harmonic terminations being presented to the device. To help prevent these failures VSWR sweeps are performed on every design before it is used in the field. During the VSWR sweep the impedance is moved away from the optimum. Moving the impedance away from the optimum will simulate the effects of stressing the device as though it were placed in a highly reflective environment or if damage has occurred to the antenna.

2.4.1 Theory

The basic principle of a VSWR sweep is to mismatch the real part of the impedance by a set value, for example $\text{VSWR} = 5$, and then the phase is swept around 360° to form a constant VSWR circle. This is seen best when the Smith Chart is normalised to the impedance around which the VSWR sweep is performed. Using $50\ \Omega$ as an example for the optimum and then performing a 5:1 VSWR and plotting it, seen in figure 2.23, will cause the VSWR circle to cross points on the real axis that are five times larger ($1 \times 5 = 5$) and five times smaller ($1 \div 5 = 0.2$) than unity.

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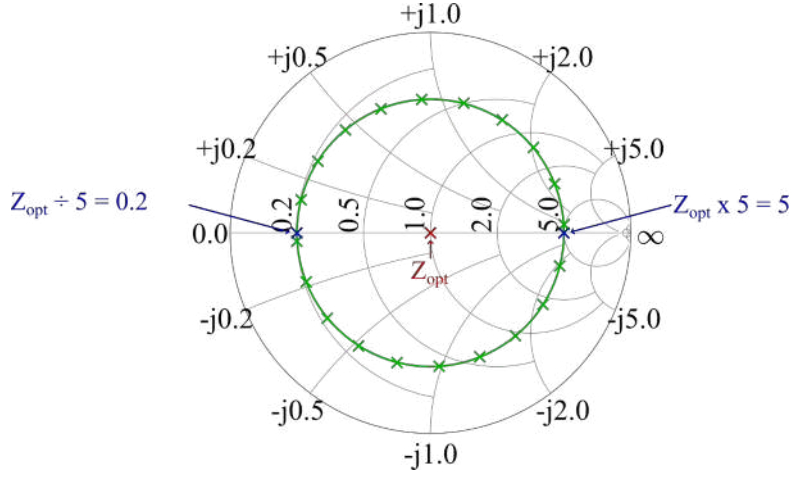


Fig. 2.23: A 5:1 VSWR sweep performed around 50 Ω

To find the magnitude of the impedances being swept (Γ) equation 2.31 can be used.

$$VSWR = \frac{1 + |\Gamma|}{1 - |\Gamma|} \Rightarrow |\Gamma| = \frac{VSWR - 1}{VSWR + 1} \quad (2.31)$$

Then to plot the VSWR circle Γ is held constant and the phase is swept to form a circle. Considering an example for 5:1 VSWR and putting 5 into equation 2.31 will give the radius of the circle to be 0.6. Next, assuming $Z_0 = 50\Omega$ and using equation 2.32,

$$Z_L = Z_0 \frac{1 + |\Gamma|}{1 - |\Gamma|} \quad (2.32)$$

to convert this back into an impedance, with phase set to 0° , gives 250 Ω , then doing the same for when the phase is 180° to get the low point (magnitude/phase form was converted too real/imaginary) gives 10 Ω , which when normalising to 50 Ω gives 5 and 0.2 respectively as shown in figure 2.23. Taking the 5:1 VSWR example a step further, a simple simulation was done to look at how the voltage and current were affected by making the impedance five times larger and then five times smaller when using 50 Ω as the Z_{OPT} value, shown in figure 2.24. This shows when the impedance is five times larger (250 Ω) the voltage will be 1.6 times the optimum value, and the

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current is 0.3 times the optimum. When the impedance was five times smaller ($10\ \Omega$) the reverse is true, so the voltage is 0.3 times the optimum and the current is 1.6 times the optimum.

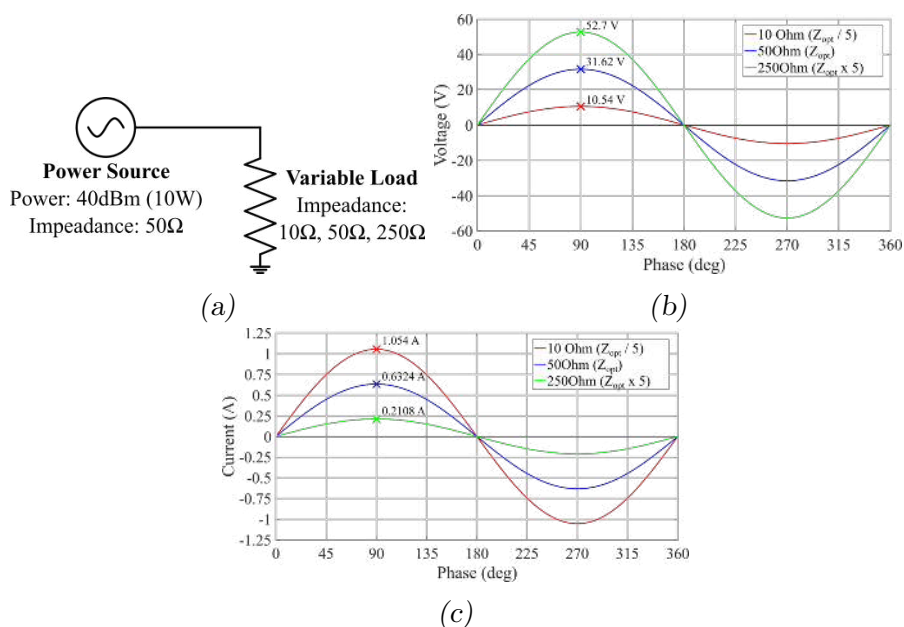


Fig. 2.24: Example showing how the current and voltage waveforms are changed during a VSWR sweep. (a) The circuit used to simulate. (b) The voltage waveforms. (c) The current waveforms

This sweep can be done for any level of VSWR with 10 often being the upper limit, although as stated in [23] this is increasing. Although it assumes that the Smith Chart is normalised to the same impedance that the VSWR is being swept around. But often this is not the case, as most people tend to work with Smith Charts exclusively normalised to $50\ \Omega$ to reduce confusion when working in teams, and enable quick analysis and comparisons. This then requires the VSWR circle to be plotted around an impedance other than the impedance the Smith Chart is normalised to. A small MATLAB® function was used to do this in the following two steps:

1. Plot an ideal circle for the desired VSWR ratio around the centre of

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the Smith Chart, regardless of what the Smith Chart is normalised too.

2. Move each point depending on what the desired optimum is.

If the optimum is purely real, then it is just a matter of re-normalising the points on the ideal VSWR circle. However, if they are complex then the VSWR still only occurs around the real part of the impedance, and so the complex component is added on once the re-normalisation has been done. This can be seen when looking at equation 2.33,

$$Z_{VSWR} = \text{real}(Z_L) \frac{1 + \Gamma_{IDEAL}}{1 - \Gamma_{IDEAL}} + \text{complex}(Z_L) \quad (2.33)$$

as it shows how the function moves the points, a graphical example for the 5:1 VSWR is shown in figure 2.25 for different optimums.

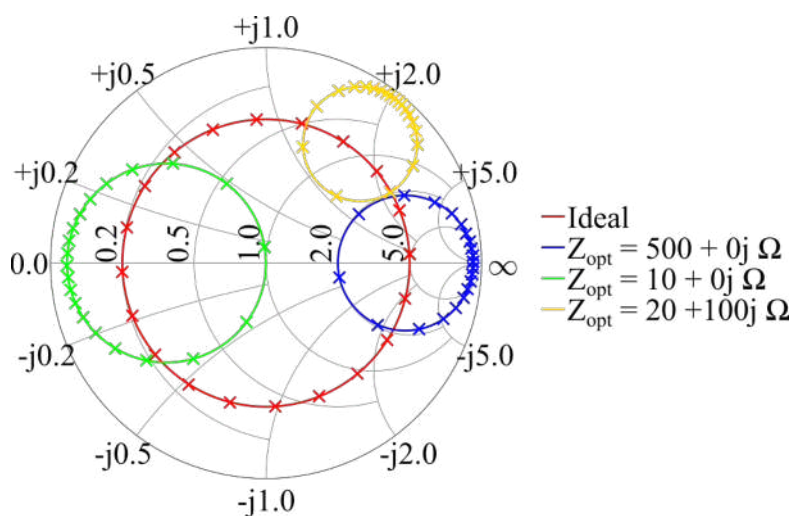


Fig. 2.25: A 5:1 VSWR sweep performed around various impedances

2.4.2 Improvements to the VSWR sweep

Novel improvements to the VSWR sweep could be categorised into the following two groups:

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Sweep Procedure: The procedure with which the device is stressed, ranging from bias to impedance sweeps.

Diagnostic Ability: The ability of the system to reveal the causes for performance changes and failures.

This thesis will add novel improvements to both of these, by showing the need to increase the impedance space, swept to make sure all potential failure conditions are simulated, and adding waveform data to improve the diagnostic ability of the sweep.

Improvements to Sweep Procedure

Improving the sweep procedure requires innovating new ways to stress the device which can simulate the effects of the real world more accurately. There are two main categories within this research, stressing the device to see what its physical limits are, the other attempts to accurately reproduce real-world stresses and then do lifetime tests to predict the products expected lifetime. The primary focus of this thesis is addressing what to do with the harmonic impedances during these tests, as typically they are not controlled during the VSWR sweep. This is because most robust commercial PAs tend to employ the proven classical modes of operation (covered in Section 2.5.1) where the fundamental harmonic impedance has the most effect on output performance, and so only aim to terminate the fundamental harmonic with their matching networks. Only sweeping the fundamental harmonic impedance during a VSWR sweep means the effects of the second harmonic impedances and above are not seen during the sweep. Although with the dawn of harmonically dependant modes, such as Continuous Class B, bring a need to explore an increased harmonic space during these sweeps.

Previous work has been done on this at Cardiff [24], where work was focused on identifying the cause of breakdown of a GaN HEMT and monitoring gradual degradation over time and GaNs ability as a technology to operate without a circulator. This was done by investigating an infinite VSWR sweep, using active load pull, and how changing various parameters

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would change the stress on the device, such as device size (by performing the same sweep on different device sizes), drain bias and drive power. Harmonic impedance were part of this test but they were placed in either an open or short location and so did not fully characterise the harmonic space [25]. This work expands on this by fully characterising the harmonic spaces and looking for more interactions between the fundamental and second/third harmonics. This showed that there is a need to fully characterise the harmonic space, not just at open and short impedance locations. Also, with CMs increasing in popularity, this work needed expanding to fully cover the harmonic space. This new VSWR sweep has two applications; firstly measuring the transistor before the design stage to make sure it can tolerate the peaking RF currents/voltages the new modes of operation require to increase power/efficiency; secondly on the finished device to make sure there is not any undesired interactions between the fundamental and harmonics when an unexpected load is presented to the device that then cause the device to fail. The main research areas in the area of VSWR sweeps is to: increase variables swept during the sweep, or identify new patterns of behaviour from existing variables that indicate failure. The majority of the research done in this area has been to identify new patterns or behaviours that allow failure detection, where commonly swept parameters are swept in a particular order to trigger a response that represents real world stress. This thesis will tread new ground by adding harmonic impedance sweeps to a conventional fundamental VSWR and using waveform measurements to investigate how they will affect the stresses on the device.

Improvements to Diagnostic Ability

The diagnostic ability is how well the information provided by the measurement system can help explain/diagnose the cause for the failure or performance change during a VSWR sweep, or any other sweep a system may perform. As GaN is a relatively new technology, there has been an increased research interest in this area trying to understand and remove the weaknesses observed in GaN based devices. Cardiff's contributions to this area involves

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using waveform engineering, which can allow deep insight into the current and voltage waveform features at the intrinsic i-gen plane of the device at or near the time of failure. Similar work has been done in this area looking at indications of degradation while varying various parameters, such as:

- Operating input/output voltage
- Temperature
- Device geometry
- Fundamental Impedance
- Drive power

Looking at the literature there are already many non-waveform based solutions for monitoring and diagnosing device degradation and failure:

1. **Visual:** This is often not the “go-to” approach, as it requires a high quality camera that is often very expensive, and a trained eye that knows what to look for. But degradation can be observed visually [26] which can then trigger an investigation into other parameters that may indicate how this device has degraded/failed, which can then be monitored by software.
2. **DC-RF Dispersion:** This is a measure of how the static DC-IVs compare to a similar measurement done with a RF drive, the RF-IV. Under the RF, or pseudo RF conditions, the knee of the device is said to “walkout” as the drain voltage is increased. This can be measured using a pulsed IV setup by setting the DC resting point for the DC drain to be the same as the drain bias under RF conditions.

It has been reported [24] that this is due to an effect called “trapping” [27], where electrons tunnel into “traps” on the surface of the transistor, and so form a second gate and extend the depletion region. This effect can be seen in figure 2.2. It has been observed that this is not always a permanent failure and time, appropriate light injection [28] or heat can all help recover the device performance.

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3. **Gate/Base Leakage:** This is a measure of how much current flows in the gate/base of a transistor under normal operation [26][27][29]. In FETs, one of the factors that influences this is gate edge degradation [30], which is thought to occur due to defects occurring in the channel under the gate that allows the flow of electrons from the gate into the channel. Measurements show this to be a time dependant failure mechanism that can eventually cause permanent damage. This effect can be seen by monitoring gate leakage, as seen in figure 2.26, where the diode between the gate and the source has been degraded, causing “hot spots” of current to be observed in the physical structure due to a degraded reverse bias operation.

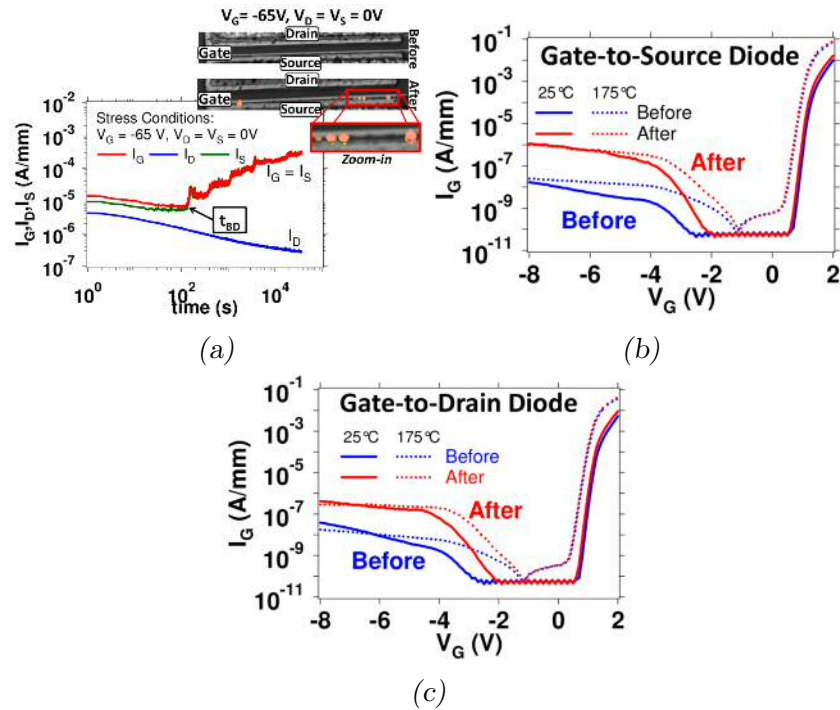


Fig. 2.26: Measurements looking at gate leakage, [29] (a) Photos showing the current “hot spots” resulting from gate leakage current and current measured over time (b) Effects of the stress on gate-source diode (c) Effects of the stress on gate-drain diode

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4. **Pinch-Off:** This is where the pinch off voltage is changed. In FETs the failure indicator is if the pinch-off voltage increases, as seen in figure 2.27. This is due to the build-up of charge under the gate [24][26], so acting as a separate parameter to gate leakage that can be observed.

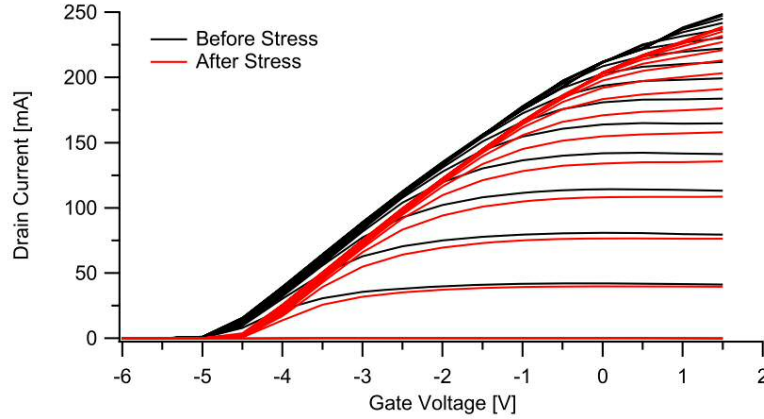


Fig. 2.27: Effects of traps on pinch-off,[24]

5. **R_{ON} and R_{OUT} :** The resistance of the channel, with the “on resistance” being the resistance of the channel in the knee region and the output resistance for when the device is saturated. They can be measured under DC conditions and can indicate any structural changes in the channel [26]. One example is seen in figure 2.28 where the whole of the output DC-IV has been collapsed due to a reduction in the current carrying capabilities of the channel and an indicator of channel damage.

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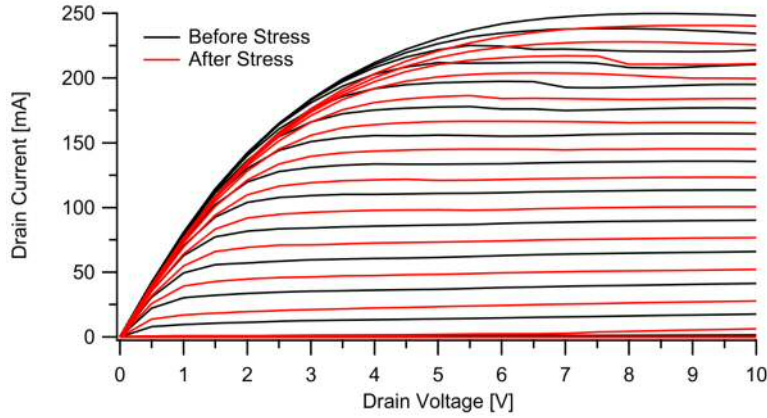


Fig. 2.28: Effects of traps on pinch-off,[24]

Waveforms can add to the diagnostic ability of a system in the following ways:

1. **DC-RF Dispersion:** This can be measured using non-waveform methods as seen in the previous list but can also be observed using a waveform system by measuring actual RF current and voltage waveforms. The first advantage of this is that the dispersion effect is now observed under actual RF operating conditions rather than pseudo RF operating conditions. As actual RF waveforms are being used, performance data can also be collected that give deeper insight into the performance of the DUT. This thesis uses this data in a novel way in Chapter 5 to look for the optimum of the device, process this data, and display how the DC-RF Dispersion affects the performance.
2. **Peak RF voltage and current breakdown:** As the de-embedded voltage and current waveforms are available, they can provide insight into the operating conditions of the intrinsic i-gen at or just before the point of failure.

In Chapter 3 the need to measure RF waveforms is considered and shows that peaking voltage waveforms are caused that would have otherwise gone un-diagnosed without waveform based measurements.

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Then in Chapter 4, failures are identified where waveforms provide unique diagnostic insights that conventional data are unable to conclusively diagnose. It is also seen that using waveforms alongside the data obtained from a non-waveform based system also allows for a clearer and more conclusive diagnosis after a failure has occurred.

2.5 Continuous Modes

2.5.1 Power Amplifier Theory

The operation of a PA is generally based on presenting a load to the transistor that will determine the performance of the PA, where there are many trade-offs, the main being power, efficiency and linearity, although in use cases where the device is battery operated the DC current can also be a hard limit that affects the choice for load conditions. The classical modes, known as Class A, B & C ideally present the optimum for power transfer, which can be found using the DC-IV characteristics and noting the peak voltage and current, as shown in figure 2.29.

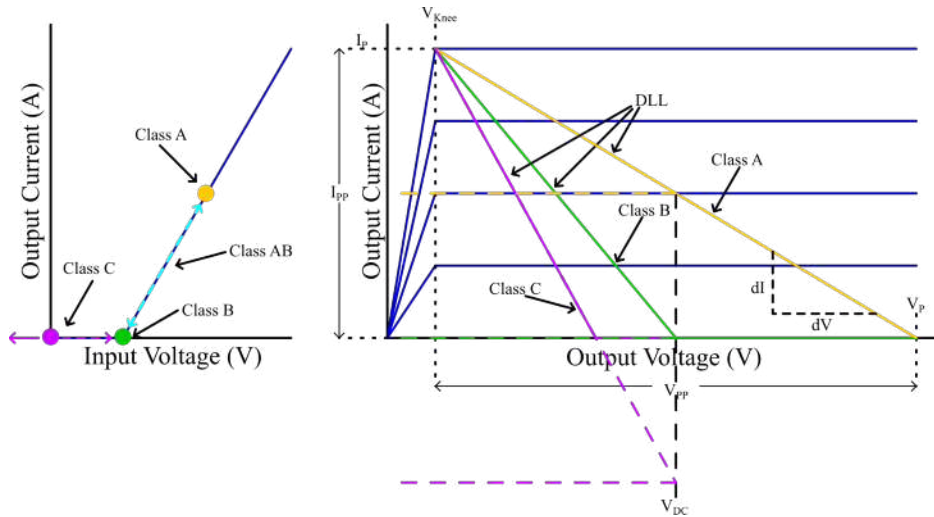


Fig. 2.29: An example of a DCIV for both transfer (left) and output (right). The various load lines are overlaid, and key points marked.

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The main difference between these modes, as noted in figure 2.29, is the input bias point, as the output bias point remains fixed:

Class A: This allows the full current wave to be amplified, and so when realising it in a real design is the easiest to linearize as there is no harmonics in the current waveform, but also has the highest quiescent point, $I_P/2$, which gives an ideal efficiency of 50%.

Class B: This is when the input bias is set to the pinch off voltage. This means that only half the output current wave occurs when the channel is not pinched off. This results in a half rectified current waveform, which contains extra harmonics, so when realising a PA in this mode the harmonic terminations as well as the fundamental need to be considered to remove these harmonics from the output voltage. This often means Class B PAs are not as linear as Class A. This also reduces the quiescent point which is now equal to I_P/Π , which results in a higher efficiency than class A (78.5% ideal). As seen in figure 2.30 Class B has the same output power as Class A.

Class AB: This is the most common operating point for PA design as it occupies all the regions below class A and above class B, so it allows for a compromise between realisable linearity and efficiency. As well as this, figure 2.30, shows that the power output in this region is higher than at Class A or Class B and so making it a very desirable operating region. This is due to an increased fundamental current component, allowed for by the harmonics present in the current waveform, as seen in figure 2.31.

Class C: This is any bias point below class B, and so reducing the bias point further and increasing efficiency, but also increasing harmonic content which negatively impacts linearity in realised devices. The power reduces as the bias point is moved further into the Class C region, as seen in figure 2.30, Class C PAs tend to be used only when high efficiency is a large concern, as is the case with auxiliary PA in a Doherty.

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The fundamental impedance is set by the gradient of the DLL that is conducting. Knowing the bias point and the ideal impedance will cause the device to generate the current waveforms discussed above. The voltage waveform still needs to be shaped. If a $50\ \Omega$ load is applied to the transistor that covers the fundamental and harmonics, then the voltage will mirror the current. However the efficiency predictions above assumed a sinusoidal voltage wave, so the harmonics need to be presented with a short circuit to remove the harmonic content from the voltage waveform.

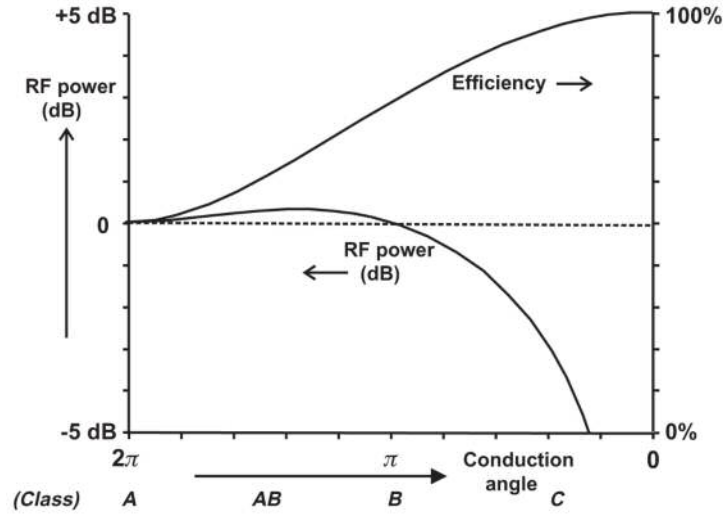


Fig. 2.30: A graph showing how power and efficiency change with the different classes of operation, [31]

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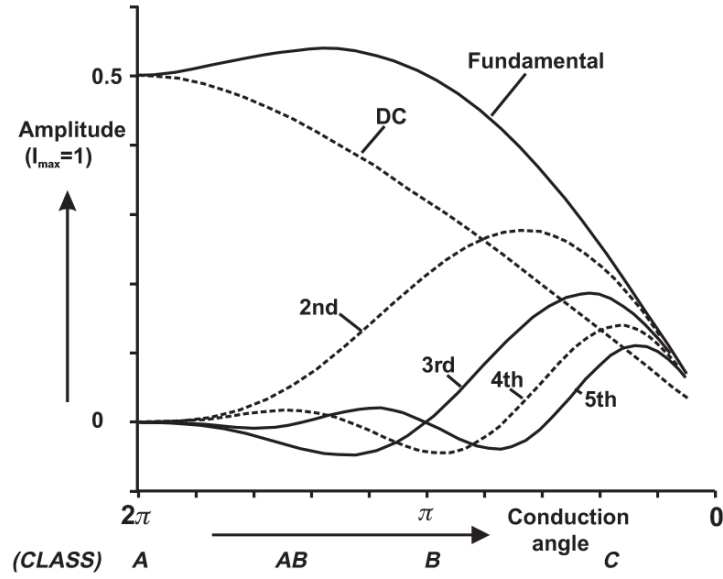


Fig. 2.31: A graph showing how the harmonic content changes with the different classes of operation, [31]

2.5.2 PA Equations

This section goes over the commonly used equations used to characterise and measure any PA. These are the equations used for any results plotted in this thesis.

$$P_{DC} = V_{DC} I_{DC} \quad (2.34)$$

$$P_{RF} = \frac{|real(V_{RF})^* (I_{RF})|}{2} \quad (2.35)$$

$$P_{dBm} = 10 \log_{10}(1000 \times P_W) \quad (2.36)$$

$$\eta = \frac{P_{OUT_RF}}{P_{OUT_DC}} \quad (2.37)$$

$$PAE = \frac{P_{OUT_RF} - P_{IN_RF}}{P_{OUT_DC}} \quad (2.38)$$

$$G_{MAG} = \frac{P_{OUT}}{P_{IN}} \quad (2.39)$$

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$$G_{AV} = \frac{P_{OUT}}{P_{DRIVE}} \quad (2.40)$$

The last equation is for finding the impedance from the VI matrix generated by the load pull system:

$$Z_{RF} = \frac{V_{RF}}{I_{RF}} \quad (2.41)$$

It should be noted that the magnitude of the current in equation 2.41 will need to be inverted for DC and the fundamental on the input as they are entering the device from an external source. On the output, it is just the DC as all the harmonics are being generated by the device (or vice versa if your software has forward current in the opposite direction).

2.5.3 Continuous Mode Design

PA theory defines the classical modes, such as Class A, B & C, by a specific voltage and current waveform that are achieved by a specific set of fundamental and harmonic impedance locations. The impedance locations for classical modes is often the fundamental at a real impedance chosen by the designer and then short at the harmonics. As a result, designs have focused on networks that match the fundamental well, and then short the harmonics the best they can. But even just matching the fundamental to a single point over a wide bandwidth is challenging, often due to the output capacitance of the device and also due to the components used in matching networks not presenting a constant impedance with frequency. This causes the matching network to have an impedance trajectory with frequency rather than having a fixed impedance with frequency, and so the matching network does not present the ideal load at all frequencies. One way to make the design of the matching network less complex, is to allow the fundamental impedance to change with frequency, and to then match the trajectory of the matching network to the that of the fundamental impedance. One of Cardiff's research areas was Class J which showed that if a capacitive load is presented to the fundamental impedance and then the second harmonic impedance is tuned with an inductive load, then the original performance can be recovered. This re-obtaining the optimum performance is caused by

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the voltage waveform peaking as the second harmonic impedance is tuned with the fundamental impedance. This theory was also investigated by other groups, for example [32][33]. This means the output capacitance of a device could be incorporated into the matching network, meaning it is no longer a hindrance to the matching network but now positively contributes to the output performance.

Class J theory then evolved into CMs which put a series of these points together and assign each of the impedance points to a frequency, and so forming an impedance trajectory for the matching network. It was observed that the tuning of the harmonic impedances could be performed in conjunction with the fundamental impedance to obtain ideally constant performance across a range of impedance locations. Taking Class B as an example, the family of waveforms and impedance locations that are a part of the Continuous Class B continuum share the same current waveform and the voltage waveforms can be found using equation 2.42.

$$V_J = (1 - \cos(\theta))(1 - \alpha \sin(\theta)) \quad (2.42)$$

The ideal impedances and waveforms that are a part of the continuous class B continuum are seen in figure 2.32, where the voltage waveform peaking effect can be seen. The voltage waveform peaking is what allows CMs to maintain ideally constant performance across a trajectory of impedances in the case of Continuous Class B.

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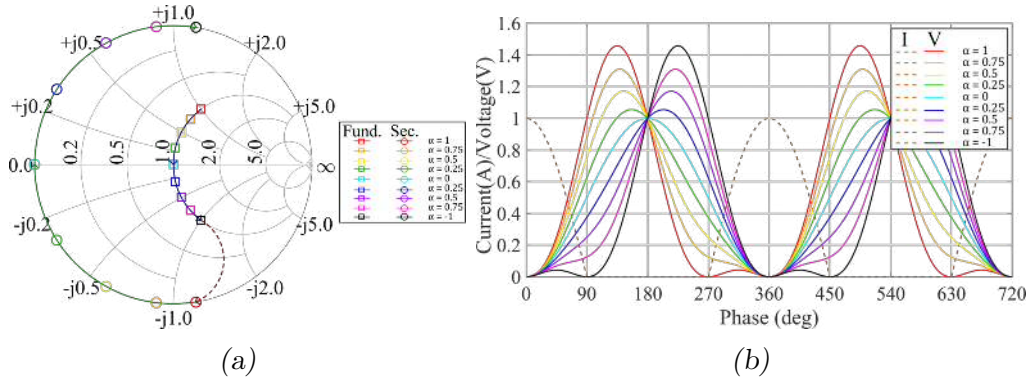


Fig. 2.32: Ideal Continuous Class B operation sweeping α from -1 to 1 (a) Impedance locations (b) Current and voltage waveforms.

This shows that the classical class B impedance is just one of a continuum of impedances that can achieve the same ideal performance. This theory has been re-applied to other modes of operations, showing that most of the other classical modes are part of a wider family of impedance locations. This allows the fundamental and second harmonic to have a trajectory, rather than a single impedance point, which allows an extra degree of freedom when doing broadband designs. Although this extra room is not unlimited, as to obtain the ideal performance requires a fundamental and second harmonic impedance pair, with the fundamental moving around the optimum and the second moving around a $\Gamma = 1$ circle. If the bandwidth of the PA is an octave, as shown in figure 2.33, then at the top of the fundamental bandwidth, in this case 2 GHz, the fundamental needs to be at an impedance around the optimum, but then the second will need to be at a $\Gamma = 1$ location when the fundamental is 1 GHz, and 2 GHz is now the second harmonic.

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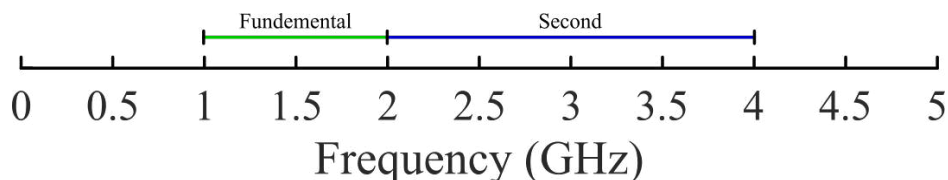


Fig. 2.33: The fundamental and second harmonic for a PA with fundamental 1 - 2 GHz.

This shows that continuous modes, while enabling an extended bandwidth, are inherently still bandwidth limited. There also needs to be space in the bandwidth between the top of the fundamental and the bottom of the second to allow the impedance to transition between one impedance space and the other, which means the bandwidth needs to be less than an octave.

2.5.4 Specification Review

The idea of CMs has become a viable design methodology to help increase the bandwidth of PAs, and a lot of work has been done in this area. In this review, only papers that have a similar specification to the specifications of the Continuous Class B design carried out in Chapter 6 are considered, and then the performance compared.

Bandwidth: The target bandwidth is 1.7-2.7 GHz. This was set to perform a balance between the octave bandwidth limitation of the Continuous Class B and still cover a wide range of frequency bands in use within the telecommunications industry. Looking at figure 2.34 the 1.7 – 2.7 GHz frequency band covers the upper half of the 4th Generation (4G) Long Term Evolution (LTE) frequencies, while maintaining less than an octave bandwidth. This allows for a single PA to be used for multiple functions, saving on space and development costs. It is thought that 5th Generation (5G) will occupy the same frequencies as 4G but also increase the frequencies of operation to allow for new modes of operation, allowing this design to be compatible with the planned 5G network too.

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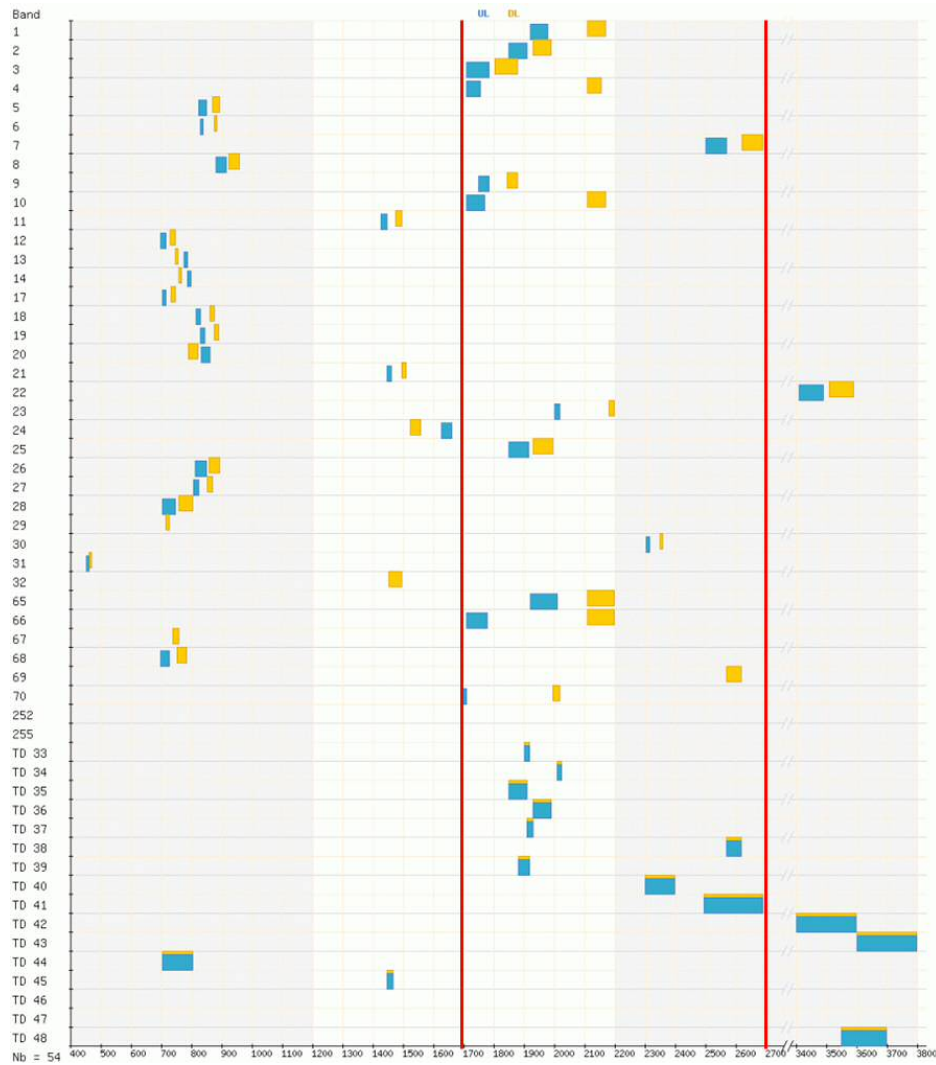


Fig. 2.34: 4G LTE Spectrum Bands, [34]

Power: The power output was set by the devices being used, which were sized to target a 20 W device to be used within a macro cell, or a large micro cell, as seen in figure 2.35

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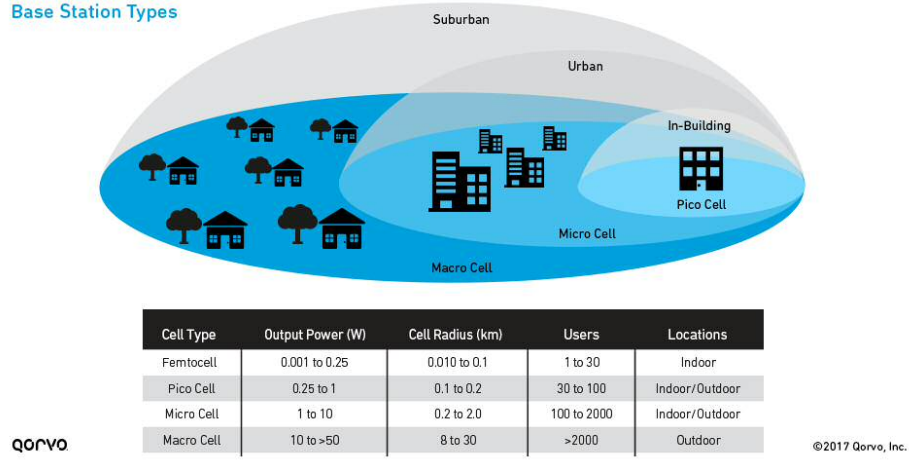


Fig. 2.35: Qorvo’s graphic about different base stations power levels for 5G networks, [35]

Drain Efficiency: The ideal performance for a class B design is 78.5% so assuming losses in the matching network and non-ideal matching network a target efficiency of 60% was set.

Technology: GaN MMIC, GaN was chosen because of the high breakdown voltage it can achieve.

A table of comparable designs was formed, shown in table 2.1, where ‘This’ is the design carried out in Chapter 6. It is split into three sections, the top section shows laminate designs, the lower section shows MMIC/hybrid designs and then the final section shows the different results from the design carried out in Chapter 6.

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Tab. 2.1: A table of similar designs

Paper	Band		P_{OUT}	P_{OUT}	η	η	Device
	(GHz)	(%)	Min	Max	Min	Max	
			(W)	(W)	(%)	(%)	
Technology: GaN Package							
[36]	1.35-2	39	48	100	65.8	76.3	Cree CGH40045F
[37]	0.9-2.3	87.5	49	69	53	63	Cree CGH40045F
[38]	1.8-2.3	24	31	56	50	75	Cree CGH40045F
[39]	1.2-2.5	70.3	7.9	11.2	45	70	Cree CGH40010F
[40]	1.1-2.6	81	8	12.5	57	67	Cree CGH40010F
[41]	1.3-2.8	73	10.2	17.8	67.5	82	Cree CGH40010F
This	1.8-3.1	53	10	15	30	52	Qorvo GaN50
[42]	1-3	100	8	14	55	65	Cree CGH40010F
Technology: GaN MMIC							
This	1.8-3.1	53	10	15	30	52	Qorvo GaN50
[33]	2.2-3.2	37	0.13	0.65	45	59	0.8um GaN
This: Design in Chapter 6 - Specification vs. Simulated vs. Measured							
Specification	1.7-2.7	45	20	20	60	60	Qorvo GaN50
Simulated	1.7-2.7	45	19	20	52	59	Qorvo GaN50
Measured	1.8-3.1	53	10	15	30	52	Qorvo GaN50

The top two sections of the table are ordered by highest frequency achieved, showing as max frequency increases power tends to reduce, whereas the efficiency remains constant, with high efficiency designs across the table. Comparing the fabricated Continuous Class B quasi MMIC design done in Chapter 6 (identified by ‘this’ in the table) with the laminate based designs it is seen that this design has lower efficiency, with other designs in the same band obtaining up to 82% over 52% for this design. This is due to the ability to use tuning lines to match the transistor, as these are much lower loss than some MMIC based components, primarily the inductors. As this is the first attempt to design a full Continuous Class B PA on MMIC at S band it is expected the topology could be modified and further iterations to the design

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may make the efficiency performance more competitive.

Looking at the second section of table 2.1 and the other MMIC design done using CM theory, it should be noted that the power is an order of magnitude lower. It should also be noted that this paper only has the output matching network on MMIC and biases the device externally to the chip, which removes one of the inductors required and so allowing a higher performance to be observed. These limitations allowed the paper to look at the problems when moving to MMIC, where one of their main findings was that the MMIC based inductors cause a loss in the output performance, and a plot taken from this paper, shown in figure 2.36, shows that as the quality factor of the inductor decreases the efficiency drops, as does the output power. This problem was also faced during the design in this work, which led to a design exercise based purely around increasing the Q-factor of the inductors used, as seen in Chapter 6.

There has also been work done at X-band frequencies, 7.5-11.5 GHz, [43]. This was not included in the table as due to the higher operating frequency it was able to use length of line to match the impedances which was not possible with the design in Chapter 6.

Looking finally at the last section of table 2.1, is seen that this design had a noticeable performance drop in power when moving from simulated to measurements. It is thought this is due to thermal compression and the PA will perform closer to the simulated results when it is measured using a pulsed signal. It was also noticed that the frequency band shifted up extending its bandwidth out to 3.1 GHz. This is likely caused by the inductor designs, as they were done by the author due to the Process Design Kit (PDK) only having a limited selection of components.

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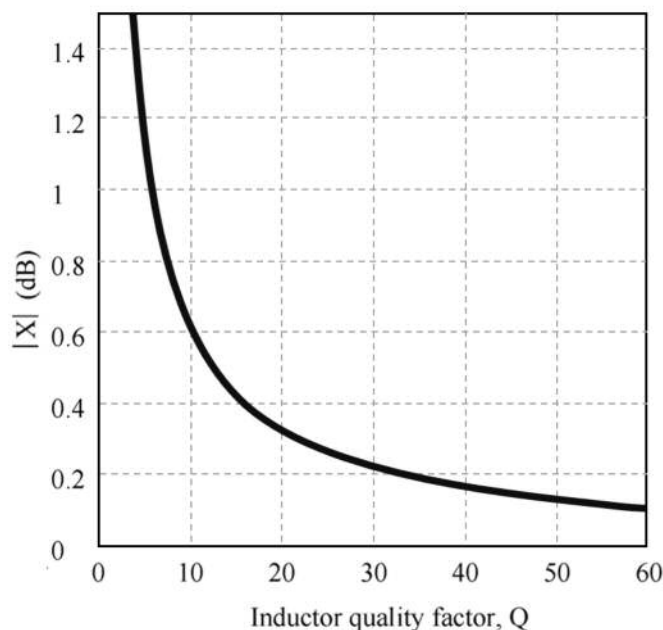


Fig. 2.36: A plot showing how the relative reduction in performance, X , increases with lower values of an inductor's quality factor, Q . [33]

While this design will not break new ground when compared to its laminate brethren; it does build on the start made by [33], to now design a hybrid MMIC PA that addresses all the design limitations of MMIC chips, and that outputs enough power to be used in a small base station. It is also anticipated that this design will be a platform for more MMIC based designs in the future to push CMs to the next stage of their development.

2.6 Doherty

2.6.1 Doherty Theory

The Doherty PAs architecture is fundamentally different to a CM PA, where the Doherty has two devices: the main device, and an auxiliary device - that load pulls the main. This architecture aims to solve the main problem of

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all classical architectures and CMs; the back-off efficiency. In classical architectures the efficiency is directly proportional to drive and as the input power is backed off, the output power reduces too. This is an important consideration when the application of these PAs involve modulated signals. These signals will not require a single output power level but, due to modulation, will vary between the backed-off state and various levels of peaking depending on the data being sent and the modulation used. The difference between the backed off state and the peak power state is characterised as the Peak to Average Power Ratio (PAPR), where different PAPR levels for different mobile standards are shown in table 2.2, [44]. The classical theory analyses the Doherty to a 6 dB back-off, which covers the majority of use cases, but with the increasing usage of 4G LTE and 5G looking to potentially use Orthogonal Frequency Division Multiplexing (OFDM) the back-off requirements will be much tougher than just 6 dBm and future work will need to investigate back-off extension.

Tab. 2.2: Levels for different standards and modulation types

Standard	Modulation Type	Typical Uplink PAPR
GSM	GMSK	0 (dB)
EDGE	8-PSK	3-4 (dB)
UMTS	QPSK	3-5 (dB)
HSUPA	16-QAM and 64-QAM	5-7 (dB)
LTE	various (SC-FDMA)	6-8 (dB)
General OFDM	various(OFDM)	10-13 (dB)

Due to its ability to maintain efficiency over back-off the Doherty is often chosen to tackle the back-off problem. A general overview of how the Doherty works is seen in [45], which uses the basic structure shown in figure 2.37, where a main/carrier device has its load actively modulated by an auxiliary/peaking device. By allowing the load of the main PA to be modulated as the power is backed off, it is possible to keep the efficiency of the main device constant for a set back off period.

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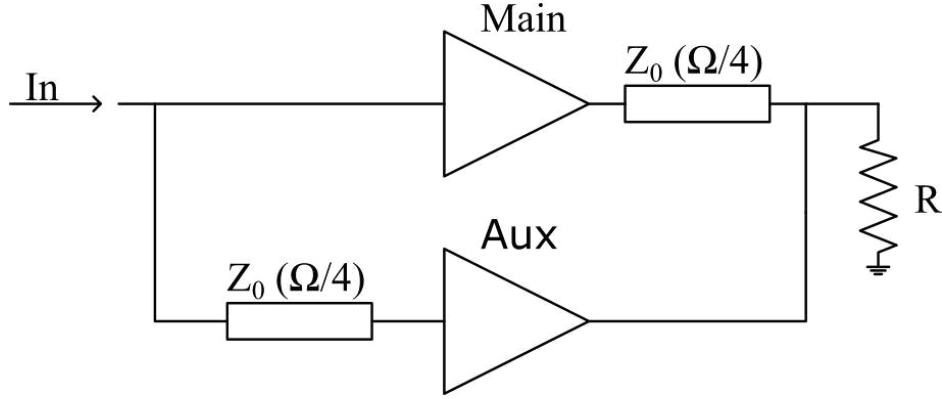


Fig. 2.37: A simple example of an ideal Doherty configuration.

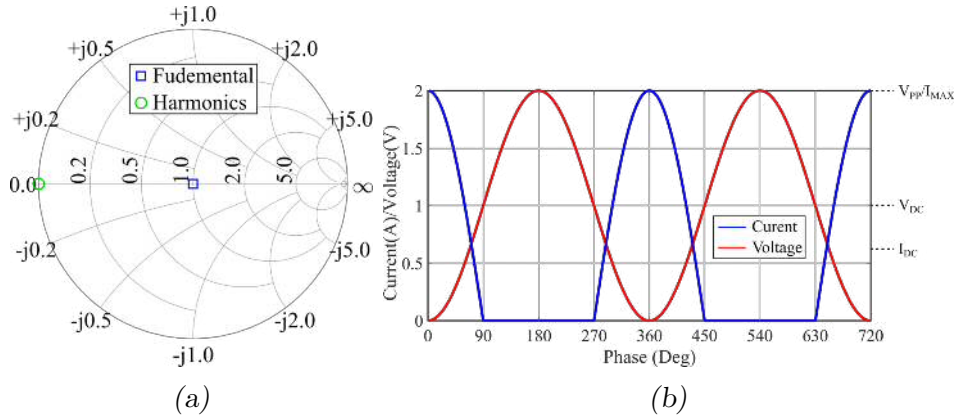


Fig. 2.38: Ideal operation of a Class B PA. (a) Impedances (b) Waveforms

To see how this is achieved, the best starting place is a classical class B design and look at how the performance decreases with back-off, [31]. Evaluating the ideal class B waveforms, seen in figure 2.38, and using equation 2.35, with equation 2.43

$$\begin{aligned} V_{RF} &= V_{DC} \\ I_{RF} &= \frac{I_{max}}{2} \end{aligned} \quad (2.43)$$

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being true for class B, then equation 2.44 is the P_{RF} for a class B PA.

$$P_{RF} = \frac{V_{DC}}{\sqrt{2}} \frac{\frac{I_{MAX}}{2}}{\sqrt{2}} = \frac{V_{DC} I_{MAX}}{4} \quad (2.44)$$

Next, equation 2.34 can be applied to the waveforms to give equation 2.45

$$P_{DC} = V_{DC} I_{DC} = V_{DC} \frac{I_{MAX}}{\pi} \quad (2.45)$$

Using both, equation 2.44 and equation 2.34, the drain efficiency can be found, as seen in equation 2.46.

$$\eta = \frac{P_{RF}}{P_{DC}} = \frac{\frac{V_{DC} I_{MAX}}{4}}{\frac{V_{DC} I_{MAX}}{\pi}} = \frac{\pi}{4} \quad (2.46)$$

Finally, looking at the impedance used to generate the DC loading is shown in equation 2.47.

$$R_{DC} = \frac{V_{DC}}{\sqrt{2}} / \frac{I_{MAX}}{2\sqrt{2}} = \frac{2\sqrt{2}V_{DC}}{\sqrt{2}I_{MAX}} = \frac{2V_{DC}}{I_{MAX}} \quad (2.47)$$

This can then be used to look at how the power and efficiency are affected by a reduction in input power. This analysis was done assuming a FET device, as there is little or no input current and it is the voltage that governs the output current. This means the output current is directly proportional to the input voltage. If the input voltage is reduced by a factor of ρ , then the output current is reduced as shown in equation 2.48.

$$I_{FUND} = \frac{I_{MAX}}{2\rho} \quad (2.48)$$

Using $V = IR$, and equation 2.47 and equation 2.48, gives the effect of input back-off on the voltage, as seen in equation 2.49.

$$V_{FUND} = \frac{\frac{I_{MAX}}{2\rho}}{\frac{2I_{DC}}{I_{MAX}}} = \frac{V_{DC}}{\rho} \quad (2.49)$$

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Next, using equation 2.48 and equation 2.49 to find how backing off the input power affects the output power using equation 2.44, is seen in equation 2.50.

$$P_{RF} = \frac{1}{2} \frac{V_{DC}}{\rho} \frac{I_{MAX}}{2\rho} = \frac{V_{DC} I_{MAX}}{4\rho^2} \quad (2.50)$$

Also, using equation 2.45 to find the effects of input power back-off on DC power consumption, is seen in equation 2.51.

$$P_{DC} = V_{DC} \frac{I_{MAX}}{\rho\pi} \quad (2.51)$$

Finally, using equation 2.46 to see the effects of input power back-off on drain efficiency is seen in equation 2.52.

$$\eta = \frac{V_{RF}}{V_{DC}} = \frac{\frac{V_{DC} I_{MAX}}{4\rho^2}}{\frac{V_{DC} I_{MAX}}{\pi\rho}} = \frac{\pi\rho}{4\rho^2} = \frac{\pi}{4\rho} \quad (2.52)$$

Which shows that as the input power is backed off the efficiency also reduces. To solve this problem the Doherty tries to keep the fundamental voltage of the main device constant as back-off occurs. The DC power is un-affected by holding the RF voltage constant as the DC supply is constant, so it is just the current that affects the DC power, which is the same in both cases. But the RF power is affected by this, using equation 2.48 for the current and now using equation 2.43 for the voltage, the effects of not changing the output voltage with back-off is seen in equation 2.53

$$P_{RF} = \frac{V_{RF}}{\sqrt{2}} \frac{I_{RF}}{\sqrt{2}} = \frac{1}{2} V_{DC} \frac{I_{MAX}}{2\rho} = \frac{V_{DC} I_{MAX}}{4\rho} \quad (2.53)$$

Next looking at how holding the voltage constant affects the efficiency by using equation 2.51 for P_{DC} and equation 2.53 for P_{RF} , which is seen in equation 2.54.

$$\eta = \frac{P_{RF}}{P_{DC}} = \frac{\frac{V_{DC} I_{MAX}}{4\rho}}{\frac{V_{DC} I_{MAX}}{\rho\pi}} = \frac{\pi\rho}{4\rho} = \frac{\pi}{4} \quad (2.54)$$

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The result seen in equation 2.54 shows that the output efficiency of a PA can remain constant as input power is modulated. But it raises the problem of how to hold the output voltage constant as the output current is decreasing with input back off. Simply using $V = IR$ shows that if I is decreasing then R needs to increase to compensate this effect and keep V constant. Which means load modulation needs to occur as the input power is being backed off, where load modulation is when the load being presented to the device changes dynamically with the input drive. The other issue with this solution is that equation 2.53 shows that the output power is no longer proportional to ρ^2 and so there is a non-linear relationship between input back off and output back off, as shown in figure 2.39.

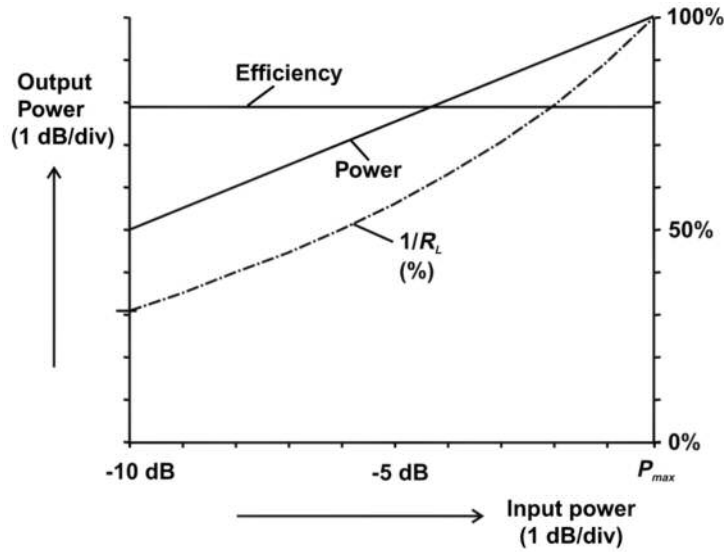


Fig. 2.39: Power and efficiency characteristic of a PA where the voltage is held constant as input power is reduced.

The Doherty solves both problems by using active load modulation to modulate the load with back-off. The basic premise of active load modulation is that two current sources are connected to the same load, as shown in figure 2.40(a).

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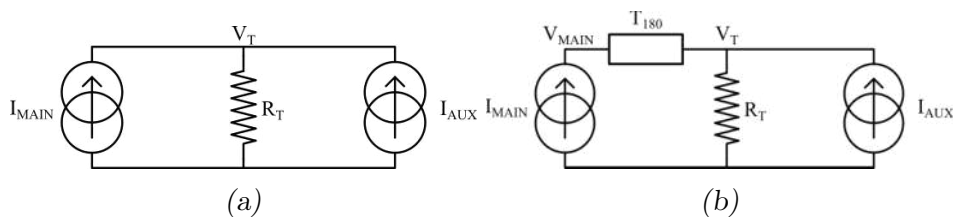


Fig. 2.40: A simple example of an ideal active load modulator. (a) Basic load modulator (b) with the 180 deg phase shift line.

The first case to consider is when I_{AUX} is off, and so $I_{AUX} = 0$ (A), and the only source that is producing current is $I_{MAIN} = 0$. In this case the voltage across the load is $V_T = I_{MAIN} \times R_T$. Next consider if the aux source turns on and starts to produce a current, so now the voltage across the load is equal to $V_T = (I_{MAIN} + I_{AUX}) \times R_T$. This essentially increases the voltage across the load as I_{AUX} increases, which is the same effect as keeping the I_{AUX} source turned off and increase the load, so load modulation. To see how this works in practice, table 2.3 shows the impedance presented to both current sources and the voltage across the load as I_{MAIN} is reduced in the circuits shown in figure 2.40. The current decreasing represents what would happen to the drain current as the input power is backed off, then I_{AUX} was varied to show the effect this would have. The top half of table 2.3 shows the effects as I_{AUX} increases as I_{MAIN} decreases, then the lower half shows I_{AUX} decreasing as I_{MAIN} decreases. It is seen that for the circuit shown in figure 2.40(a) the voltage across the load is held constant when I_{AUX} increases as I_{MAIN} decreases, but for figure 2.40(b) the voltage is held constant when I_{AUX} decreasing as I_{MAIN} decreases. From a circuit design point of view it is much more desirable to have both current sources increasing and decreasing in the same direction, as then they can be both driven by the same input with a power splitter.

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Tab. 2.3: A table showing the effect of adding in the impedance transformer shown in Figure 2.40, with $R_{OPT} = 50$, so $R_T = 25$.

I_{MAIN} (A)	I_{AUX} (A)	a - no Inverter			b - with inverter		
		Z_{MAIN} (Ω)	Z_{AUX} (Ω)	V_T (V)	Z_{MAIN} (Ω)	Z_{AUX} (Ω)	V_T (V)
2	0	25	∞	50	25	∞	$50 \angle 180$
1.8	0.2	27.7	250	50	22.2	200	$40 \angle 180$
1.6	0.4	31.25	125	50	18.75	75	$30 \angle 180$
1.4	0.6	35.71	83.3	50	14.29	33.3	$20 \angle 180$
1.2	0.8	41.6	62.5	50	8.3	12.5	$10 \angle 180$
1	1	50	50	50	0	0	0
3	1	33.3	100	75	16.6	50	$50 \angle 180$
2.8	0.8	32.14	112.5	90	17.86	62.5	$50 \angle 180$
2.6	0.6	30.8	133.3	80	19.231	83.3	$50 \angle 180$
2.4	0.4	39.17	175	70	20.83	125	$50 \angle 180$
2.2	0.2	22.73	300	60	22.73	250	$50 \angle 180$
2	0	25	∞	50	25	∞	$50 \angle 180$

The results shown in table 2.3 for figure 2.40(b), provide a way for the voltage to be held constant and be driven by a single source, reducing complexity of the drive circuit. However the problem with the Doherty design is the 1/4 wave transformer is often constructed using a length of transmission line as they have a low bandwidth, due to their electrical length changing with frequency, where at 50% away from the frequency of operation in either direction the phase will have moved by 45° . This change in phase causes the aux PA not to modulate the load of the main PA correctly and leads to a loss in performance. Introducing the 1/4 wave transformer solves the back off problem, but it introduces back the bandwidth problem.

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2.6.2 Doherty Specification Review

Unlike the CM market which is just starting to make its way into industry, the Doherty market is much more mature with a lot of commercial designs employing it. But it has been seen that the Doherty is narrow band in nature, whereas CM PAs are broad band. The ideal would be to combine these designs into a broadband high efficiency Doherty PA, that uses CM theory. As has been pointed out, it is not the transistor that is narrow band, it is the $1/4$ wave transformer, which when added to a matching network to present the desired impedance to the main device to ensure optimum performance means the matching and $1/4$ wave transformer network can become quite complex, and so lossy, which reduces performance.

Qorvo's novel 50V GaN technology presents a unique opportunity in realising a more broadband matching and $1/4$ wave transformer network. Running at 50 V means their currents can be set to have an optimum impedance of 100 Ohm and 25 Ohm for the aux and main devices respectively. This means both devices require minimal matching, reducing the losses in the matching/combining network. Reducing this loss allows for capacitors and inductors to be used to realise the impedance inverter, which are more broadband than a $1/4$ wave line. This new network is based on a paper presented by Chalmers [8] and then modified to work better in a MMIC design, and then modified again to fully take advantage of the device's periphery. With the fact that Doherty is more band limited than the Continuous Class B the specification has been relaxed for this first attempt at a MMIC Doherty at Cardiff. This Doherty will use two of the 20 W devices used to make the Continuous Class B design and so has twice the power expectation.

Bandwidth: The target bandwidth is 1.7-2.7 GHz, as with the Continuous Class B, as this device is still covering the same frequencies as shown in figure 2.34.

P_{OUT} : Looking at figure 2.35, using two 20 W parts means the Doherty is expecting 40 W out and so can power a medium sized macro cell. A second design was done to use the operating voltages and currents to

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better help with the matching, but this means lowering the voltage of one and targeting a lower current on the other, leading to only expecting 20 W from this design.

Efficiency: As the back off efficiency is of interest the efficiency requirement was lowered compared to the Continuous Class B to 45-50%

Technology: GaN MMIC

The bandwidth limitations of the Doherty are seen in table 2.4, which shows the larger the bandwidth the lower the average efficiency is. Table 2.4 is split into two halves; the top section compares the final design in Chapter 7 which targets an output power of 20 W (denoted by “this 20 W” in the table) to other similar designs. The lower section compares all the different designs shown in Chapter 7.

Looking at how this design compares, it is seen to perform well on power and band-width, but is lower efficiency than the Chalmers design [8] which has a wider band-width. But as with the Continuous Class B it needs to be noted that this will be a quasi MMIC design and all but one, [46], are laminate designs, using Cree again. The problem of the inductor came up again for this design but proved to be a more significant problem in this case, to the extent that a new topology was used to reduce the number of inductors in the design. It is also hard to compare to [46], as that has a very narrow bandwidth, but as a result has very good efficiency performance, whereas this design sacrifices peak efficiency for broad band performance. It should also be noted that this table does not show the peak efficiencies achieved and while the 40 W simulated design carried out in this thesis does not have as wide a bandwidth, it does have significantly higher peak efficiencies, with the peak η equalling 65% and the peak η at Output Back-Off (OBO) reaching 69%.

Looking at the Chalmers paper, [8], it out performs all the other designs in regards to bandwidth and has similar back-off efficiency to the other designs. The main advantage of the Chalmers design is that it utilises the capacitors in the output network, which helps increase the frequency band-

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width of the design. This was the main inspiration of the first design done in Chapter 7, but as was mentioned, the inductor losses forced a re-design and a change of topology. The Chalmers paper also allows the tuning of phase for the auxiliary to help compensate the limited bandwidth of the $1/4$ wave transformer to transform the impedances properly. The design in Chapter 7 also does something similar and so instead of having a single input, has a dual input to allow tuning of the AUX to maximise performance, but the phase of the AUX is held constant across bandwidth in this design to reduce measurement time.

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Tab. 2.4: A table showing other Doherty designs in the same band with similar power levels

Paper	Freq. (GHz)	Peak (%)	Peak P_{OUT}		η		Device
			Max (W)	Min (W)	Peak (%)	OBO (%)	
[46]	2.5-2.8	11	30	22	72	57	MACOM x 2 GaN Hybrid
[47]	2.3-2.8	20	44.3	44.3	73	55	Cree x 2 CGH40010F
[48]	2.2-2.9	27	15.5	10	60	42	Cree x 2 CGH4000P
[49]	1.5-2.14	35	28	16	61	37	Cree x 2 CGH40010F
This 20 W	1.7-2.7	45	15.8	12.6	37.5	42	Qorvo x2 GaN50 MMIC
[8]	1-3	100	28.8	20	57	55	Cree x 2 CGH60015D
This design - Specification vs. Simulated vs. Measured							
Specification	1.7-2.7	45	40	40	50	50	Qorvo x2 GaN50 MMIC
Simulation 40 W	1.8-2.4	29	40	45.6	50	55	Qorvo x2 GaN50 MMIC
Simulation 20 W	1.7-2.7	45	17.8	20.6	31	29	Qorvo x2 GaN50 MMIC
Measurement 20 W	1.7-2.7	45	15.8	12.6	37.5	42	Qorvo x2 GaN50 MMIC

2.7 Devices and Specifications

This final section will give a short summary of all the devices that are used in this thesis.

2. LITERATURE REVIEW

2.7.1 *High Voltage HBT*

This was the original device that was used at the start of the project, it is a High Voltage Heterojunction Bipolar Transistor (HVHBT) designed by Qorvo. The new high voltage nature of the device will hopefully allow HBT devices to break into the base station market and provide real competition to the FETs that are currently used. Unfortunately, there were reliability issues with the unit cell. Despite this, some very high power designs were tested prior to this project [50][51][52]. The unit cell came in two variants, the 22 μm and the 26 μm , where their performance is comparable and output power around 5 W. The only difference is the emitter length, one is HVHBT22 and the other is HVHBT26. These devices will be used in Chapter 3 & Chapter 4 and the failure testing will be primarily done on these devices. These are also the devices that are compared to the GaN FET devices in Chapter 5. If it was not for the failures this device performed very well and would have competed well against FET devices.

2.7.2 *HBTv6*

This is an evolution of the HVHBT, and fixes some of the issues that the HVHBT had. It had an emitter length of 20 μm compared to the 22 μm and 26 μm of the HVHBT. It was a smaller device overall and only capable of 3 W output power.

2.7.3 *GaN25HV*

This is the first of the two GaN 50 V processes. It came in many variants, but the unit cell that was used in this thesis is a 4 x 280 μm , which is 4 gate finger device, with a gate width of 280 μm , giving it a total width of 1.12 mm. This device was used as it is comparable to the GaN50 counterpart of around 10 W/mm. This device was only used in the comparison with the GaN50 as no circuit designs were done on it. It gets its name from having a gate length of 0.25 μm

2. LITERATURE REVIEW

2.7.4 GaN50

This is the second 50 V GaN process under development by Qorvo. As with the GaN25HV there are many different variants, but the one of interest is the 2x500 μm . This means it has two gate fingers of width 500 μm each, making its total width 1 mm. It is a 10 W/mm technology so should be able to have a peak of power of 10 W. A variation of this cell was then used for the designs that was a 20 W part. It had 3 unit cells of 2 x 350 μm , so having a total size of 2.1 mm.

2.7.5 Comparison

These devices are compared with the results shown in table 2.5.

Tab. 2.5: Comparison of the different devices used in this Thesis.

Device	Theoretical Breakdown Voltage (V)	Theoretical Breakdown Current (A)	Output Power (W)
HVHBT22	65	0.8	5
HVHBT26	65	0.8	5
HBT6	60	0.8	3
GaN25HV_1x4x280	150	1	10
GaN50_1x2x500	150	1	10
GaN50_3x2x350	150	2.5	20

Multi-Harmonic Waveform Based VSWR Sweeps

3.1 Introduction

The VSWR sweep has long been a standard reliability test due to its ability to realistically test how the DUT will perform under various load conditions. It is also a critical test to do as device mismatch is often the cause of failure for PA, as driving them full power into an open or short can cause voltage or current maxima that can lead to device failure. Often protection mechanisms are used to counteract this, or a device technology is used that can tolerate high VSWR conditions [25]. For this reason, VSWR sweeps are likely to be part of reliability sweeps for the foreseeable future, but it is also evolving slowly over time to improve the sweep area and its ability to diagnose failures when they occur, as was discussed in Chapter 2.4.2. The data obtained from a VSWR sweep is used to help diagnose what causes the device to fail during the sweep, which can then be used to make the technology more robust or give information to the PA designers to make sure impedances that may cause the device to fail will not be seen by the device.

The structure of this Chapter will start by going through each stage of the sweep and cover what occurs at each to show the methods used at Cardiff. Using this procedure the DUT will then be tested, but to prevent failures during the characterisation stage a reduced supply voltage will be used, and then the results scaled up to look for areas where peak voltage failure may occur. This shows how the addition of waveform data, and by sweeping the extra harmonics, the peak voltage stress can be observed, where before, using conventional data or single harmonic sweeps it went un-seen. With the widening interest in harmonic terminations for PA design, it is now seen to

3. MULTI-HARMONIC WAVEFORM BASED VSWR SWEEPS

be essential to perform multi-harmonic VSWR sweeps and use waveforms to identify potential failure locations.

3.2 *Background*

This chapter will increase the usefulness of VSWR sweeps twofold; by both showing the need for the harmonic impedance space to be swept in conjunction with the fundamental, and to add waveform data to these sweeps. Neither of these are novel to the industry, but so far they have mainly been used to aid with device characterisation [53] and achieving high efficiency PA modes [54], whereas this chapter will to re-apply them to produce a much more comprehensive and robust VSWR sweep structure.

1. **Harmonic Impedance Sweeps:** While the ability to do this has been around for some time, it is very costly, as it requires independent hardware for each harmonic. Also, harmonics were seen as having a large impact on performance but not necessarily on reliability so only the fundamental impedance would typically be swept during the VSWR sweep. It was also often done using passive load pull and done at the extrinsic device plane, which means that the stress on the actual device and particularly at the device intrinsic i-gen remains unknown, limiting the diagnostic ability of the approach. But hardware is decreasing in size and cost which means it is much more widely available, allowing VSWR systems to do much more than they used to, but one feature that is not widely done, if at all, is multi-harmonic VSWR sweeps. This chapter will show that sweeping the extra harmonics during VSWR sweeps can trigger failures that would otherwise have gone un-noticed, which is especially important with the advent of continuous modes that rely on harmonic tuning in the matching network.
2. **Waveform Data:** This is an area that Cardiff helped enable, and has been deeply involved with, but has been primarily used in the PA design life cycle rather than to improve VSWR sweep analysis. One exception of this is seen in [24] where waveform data was used

3. MULTI-HARMONIC WAVEFORM BASED VSWR SWEEPS

in conjunction with VSWR sweeps to monitor degradation over time and look at how changing the load magnitude stressed the device; with an aim of removing the protection circuitry required. This chapter will expand on this work and show how waveform data can be used in a typical VSWR sweep to give unique insight into how the device is operating during the sweep and what state the device was in just before failure.

To show these two additions in action this chapter will start by giving an overview of VSWR sweeps, and then go through the sweep procedure, noting any additions that have been added to conventional VSWR sweeps. This procedure will then be used on a device that was sent to Cardiff for failure analysis. This work will span two chapters, this Chapter and Chapter 4.

- **Chapter 3:** This Chapter will introduce the new sweep methodology and added data that can be obtained from a waveform based system, and then go on to measure the HVHBT and the HBT6 that was sent to Cardiff - as seen in Chapter 2.7. It was initially believed that these devices were failing under peak voltage stress. As waveforms could not be measured by the company peak voltage stress is the primary focus of this chapter. Additionally, extra harmonics will be added to the sweep to see how they affect the peak voltage and current waveforms. As a result this chapter will focus on the effects that multi-harmonic sweeps have on peak voltage, where it was seen that sweeping the fundamental and second together causes a voltage peaking effect.
- **Chapter 4:** This Chapter is a case study on real failures that were experienced while doing the VSWR sweeps. They all fail in a similar impedance space, so this chapter will emphasise how adding waveform data to conventional data can help separate out the different failure mechanisms. It also goes on to show a new device variant that was then tested and using waveform measurements confirming that the failure mechanism had been removed. The chapter finishes with the introduction of the GaN FET devices that then replaced the HBT devices due

3. MULTI-HARMONIC WAVEFORM BASED VSWR SWEEPS

to failures that time did not allow a full investigation for. The GaN FET was put through the same test procedure as the HBTs and passed without any failures, demonstrating the more robust nature commonly associated with FET devices. The result also showed that the GaN50 outperformed the GaN25HV. Because of this the GaN50 FET devices were taken on to design the Continuous Class B PA and then the Doherty also.

3.3 VSWR Review

3.3.1 Voltage Standing Wave Ratio

A VSWR sweep moves the impedance around the optimum while keeping a constant VSWR Ratio. If the optimum impedance to be swept around is located at the centre of the Smith Chart, as seen in figure 3.1(a), then the VSWR sweep forms a circle around the optimum. It is not always possible to re-normalise the Smith Chart to a complex optimum, as was the case with the software used in this thesis. As a result, these sweeps need to be performed around a complex optimum, which is shown in figure 3.1(b).

The sweeps shown in figure 3.1(b) are an example of plotting around a complex optimum, it highlights the effect that moving the optimum away from the centre has on the sweep pattern. In the case of this thesis the software used to perform the VSWR sweeps was unable to normalise the Smith Chart to a complex optimum and there was no option to perform a VSWR sweep around a complex optimum, so the sweep impedances were generated in an external program and then manually set in the application. But as the second harmonic sweep was performed automatically in the software the spacing of the second harmonic is uniform, as seen in figure 3.1(a), regardless of whether the optimum is complex or not.

3. MULTI-HARMONIC WAVEFORM BASED VSWR SWEEPS

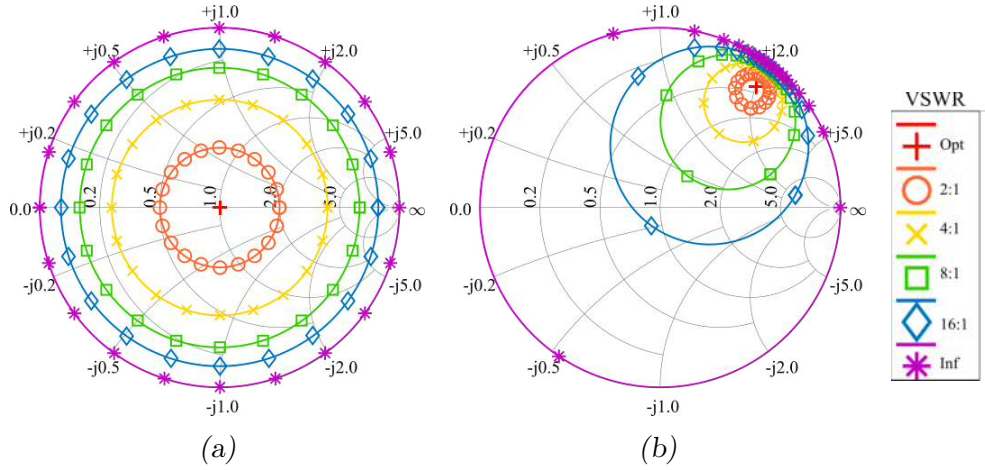


Fig. 3.1: An example of Increasing VSWR sweeps (a) VSWR sweep around the optimum with the optimum as the centre of the Smith Chart. (b) Shows the VSWR sweep around a complex optimum with the Smith Chart normalised to 50Ω

3.4 Testing Methodology

3.4.1 De-Embedding

Devices will often be characterised at the package plane, shown in figure 2.3, as this is the plane designers will use. This is acceptable for PA designers, but means that investigations into the technology will be hidden behind the various parasitic networks. To understand how the device is operating and being stressed the intrinsic i-gen waveforms are required, to obtain these waveforms it is required to de-embed down to the intrinsic i-gen plane, as shown in figure 2.3. This will allow VSWR sweeps to generate results, including voltage and current waveforms, that are representative of how the channel is operating. This is important as this is where the current is generated, and so where peak voltage and current failure will originate.

This will also allow for a more accurate picture of how the device is being stressed, especially when waveforms are added in. Unfortunately, de-embedding down to the intrinsic i-gen is not a simple task, and some of

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the parasitic components cannot be represented with simple lumped element equivalents. For these tests, some of the de-embedding was provided by Qorvo, but it does not take the reference plane all the way down to the intrinsic i-gen and so extra de-embedding was need.

As this work is using chip based devices, it is often acceptable to just de-embed a lumped output capacitance, but this should only be done if there is confidence that the output capacitance is the only component left, as package devices will often have a more complex parasitic network than a chip device. The problem with de-embedding a lumped element capacitor for output capacitance is that it is non-linear, but due to limitations in the software it was not possible to de-embed a non-linear capacitor during this project, so a linear capacitor was used. The problems of using a linear capacitor to de-embed the output capacitance is seen in figure 3.8. There are two main ways to de-embed the output capacitor:

- **Current Waveform:** This assumes the main cause of displacement current is from the output capacitor and so the de-embedding capacitor can be tuned until there is no more displacement current at the optimum.
- **Optimum Impedance:** This assumes that the intrinsic i-gen plane is purely real and so the optimum impedance for power and efficiency will be on the real axis. After performing a load pull sweep to find the optimum, the de-embedding capacitor can be tuned to move this optimum down onto the real axis.

3. MULTI-HARMONIC WAVEFORM BASED VSWR SWEEPS

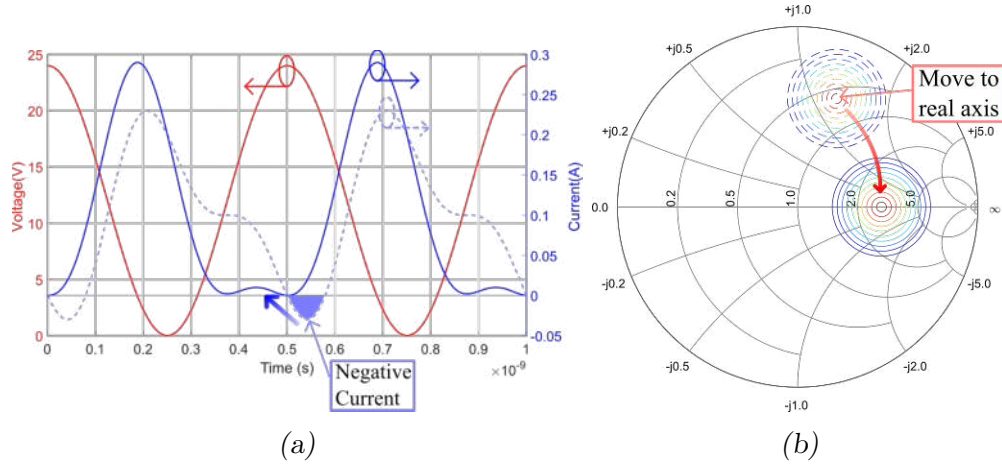


Fig. 3.2: (a) Ideal voltage and current waveforms where capacitive de-embedding has been applied - dashed: before, solid: after. (b) An idealised fundamental sweep showing the optimum where capacitive de-embedding has been applied - dashed: before, solid: after.

3.4.2 Identifying the Fundamental Impedance

Finding the optimum is a common starting point for most tests, not just a VSWR sweep, as it is where the device will be loaded during normal operation. Then, for VSWR sweeps, the optimum will be the location to sweep around. Finding the optimum involves sweeping both the power and the fundamental impedance, while keeping the second and third harmonics shorted. Although control of the harmonics is not always available, so in industry they may be terminated into a set load or left terminated into an unknown impedance. The sweep to find the optimum is executed by doing a power sweep at each fundamental location, selecting the desired compression level and using contours at that compression level obtaining the optimum.

3.4.3 Fundamental VSWR

Once the optimum fundamental load has been found, a conventional VSWR sweep is performed. This involves moving the fundamental around the optimum at various levels of VSWR. These sweeps will follow the paths shown

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in figure 3.1 while the second and third harmonic have a short presented to them at the intrinsic i-gen plane - as that is the highest number of harmonics that can be actively controlled at Cardiff currently. For the harmonics above the third, a broadband $50\ \Omega$ load will be used. This set of sweeps will allow the stress results from the fundamental impedance variation alone to be seen, which can then be used as a base line for comparison when the harmonics are swept also.

3.4.4 Harmonic VSWR

Sweeping the fundamental impedance is where conventional sweeps stop, as the fundamental impedance is the main impedance that is matched. For the harmonic sweep the fundamental will be held at its optimum and then the harmonics swept around a $\Gamma = 1$ circle, as shown in figure 3.3, which equates to an infinite VSWR sweep. This is because the harmonics will often be found on the $\Gamma = 1$ circle for high efficiency designs. This is only feasible with an active system that can control multiple harmonics so a complex optimum can be presented to the fundamental while the harmonics are swept.

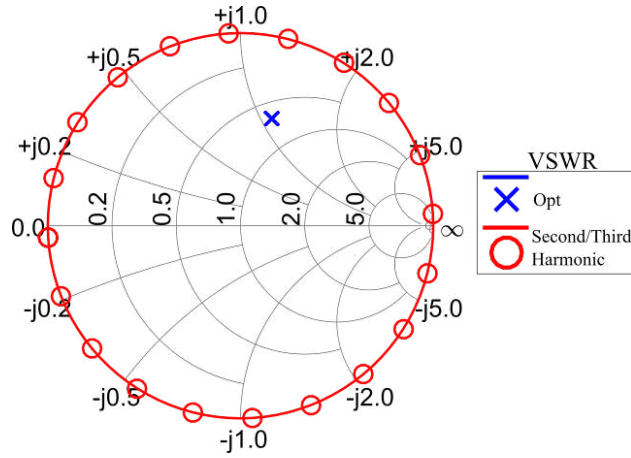


Fig. 3.3: Impedance locations for harmonic VSWR

3. MULTI-HARMONIC WAVEFORM BASED VSWR SWEEPS

3.4.5 Combined Sweep

This set of sweeps puts everything together, a harmonic impedance sweep will be combined with the fundamental impedance sweep. This involves performing a fundamental VSWR sweep, where at every point of the fundamental sweep, one of the harmonics will be swept, as shown in figure 3.4. This allows the full impedance space for the fundamental and harmonics to be characterised, which will show how the fundamental impedance and harmonic impedance interact to form peak voltages and currents and see what stress this puts the device under. The combined sweep will also allow the design engineers to have more confidence in their product knowing that they have been put through a much wider stress test that includes previously unknown variables. This is because the outside world is not under the engineer's control and can affect the fundamental and harmonic impedances in unknown ways, meaning the more fundamental/harmonic impedance combinations that are swept the less potential there is an un-tested state to be presented to the device while it is in use.

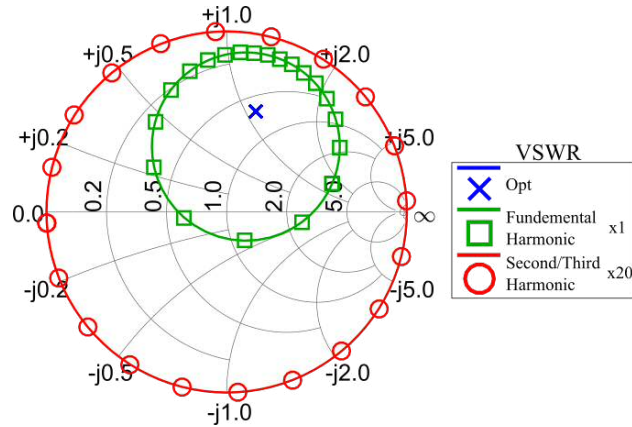


Fig. 3.4: Impedance locations for harmonic VSWR

3.5 Measurement Results

This section will follow the same flow as Section 3.4, but this time real data will be shown and discussed. It will focus on using the new waveform data

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to detect peak RF voltage stress in the channel, which is where the peak RF voltage goes above the operating limits of the device. Peak RF voltage stress is thought to be the main cause for failure prior to testing, and this Chapter shows that peak RF voltage stress only occurs in a combined fundamental and second harmonic impedance sweep. The following subsections will use the HVHBT26, as discussed in Chapter 2.7 to perform these tests, and only using a 12 V supply to prevent any failures due to peak RF voltages during these stress tests.

3.5.1 *Finding the Optimum Fundamental Impedance*

Due to the fragile nature of the DUT, the automated power and fundamental sweep were swept separately. First using the DC-IVs to estimate a starting location, then the power was swept to find the 1 dB compression point. Then an impedance sweep around the optimum was performed and contours plotted on the result. While performing these sweeps, the system was de-embedded to the extrinsic current generator plane (extrinsic i-gen) plane, using the Qorvo de-embedding network. This meant the optimum was not on the real axis, as seen in figure 3.5. Measurements were always taken at extrinsic i-gen plane, to make sure the measurements were done at a known reference plane, defined by Qorvo. But for the voltage and current in the channel to be observed the measurements plane needed to be the intrinsic i-gen plane and so further de-embedding was done post measurement, this de-embedding is discussed in Section 3.5.2. The aim of any design being done on this project would be to obtain maximum efficiency, so when doing the VSWR sweeps the optimum efficiency from figure 3.5 will be used.

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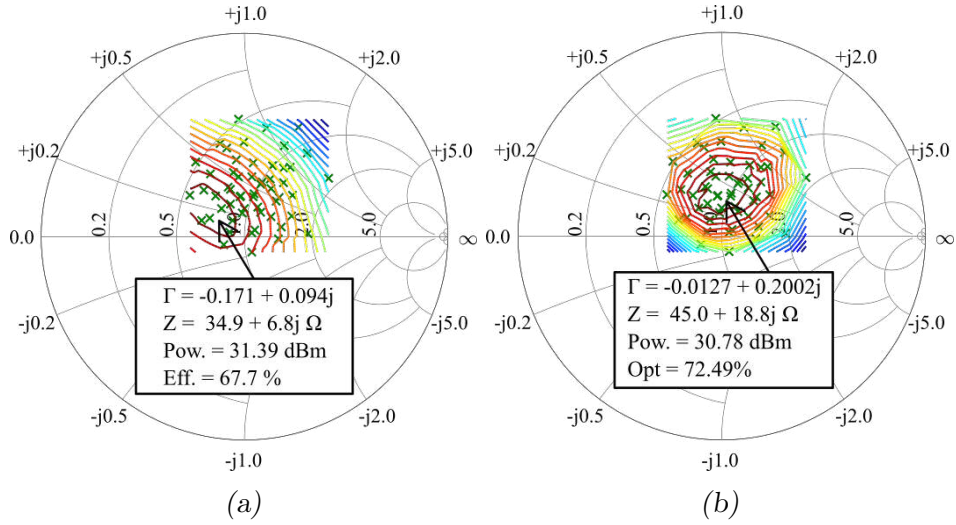


Fig. 3.5: Finding the optimum using Contour plots for HVHBT26 at 12V. (a) Power Contours (b) Efficiency Contours

3.5.2 De-Embedding

The de-embedding of this device was done in two stages. The first was to load s2p files of Qorvo's de-embedding network, seen in figure 3.6, into the load pull software, then de-embed the residual output capacitance with a lumped capacitor. This was required because the Qorvo files did not move the reference plane all the way down to the intrinsic i-gen plane, as seen in figure 3.5, and so assuming the remaining de-embedding is all or part of the output capacitance the next step is to de-embed a parallel capacitor. The results of the two methods described in Section 3.4.1 are shown in figure 3.7 for the Smith Chart and figure 3.8 for the waveforms.

3. MULTI-HARMONIC WAVEFORM BASED VSWR SWEEPS

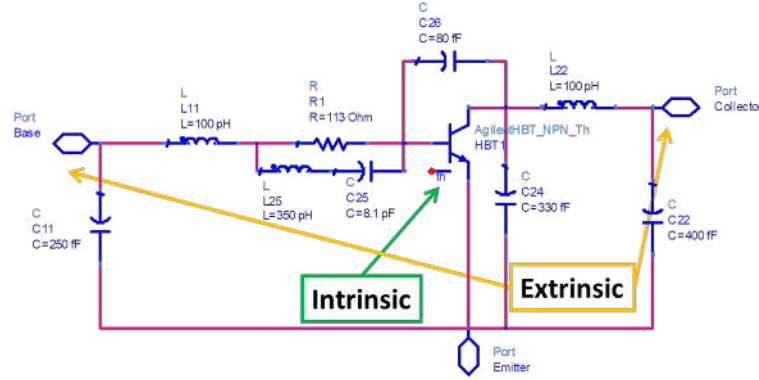


Fig. 3.6: De-embedding network generated by Qorvo for the HVHBT

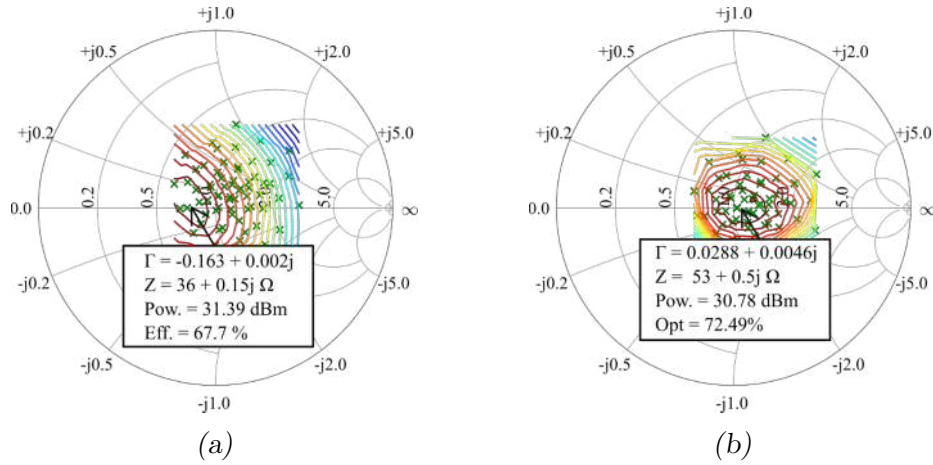


Fig. 3.7: De-embedding using Optimum Contour plots for HVHBT26 at 12V, showing de-embedded with a parallel 0.6pF capacitor. (a) De-embedded power contours (b) De-embedded efficiency contours

3. MULTI-HARMONIC WAVEFORM BASED VSWR SWEEPS

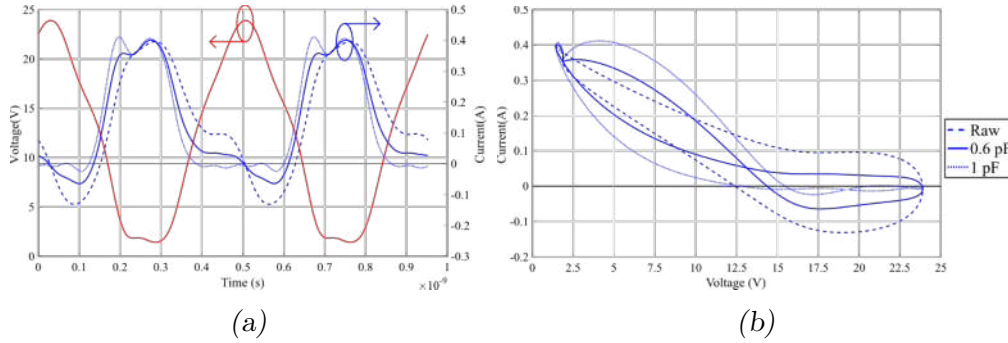


Fig. 3.8: De-embedding using output waveforms for HVHBT26 at 12V, showing the various de-embedding levels, 0pF (Raw), 0.6pF (Smith optimum), 1pF (Minimal -ve Current) (a) Voltage and current waveforms (b) Dynamic Load Lines

Using the current waveforms and displacement current to de-embed the output capacitance gives a de-embedding value 1 pf, whereas moving the optimum onto the real axis gives a C_{ds} 0.6 pF. This shows the complexity of the de-embedding process and in this case the inadequacy of simple lumped element de-embedding. Looking at the DLL, seen in figure 3.8(b), and the shape it forms as it is de-embedded through the optimum given by the contour plots and onto to the value that gives the minimum displacement current, the low voltage part (left) of the DLL balloons out, while the high voltage part of the DLL (right) deflates, showing that this capacitor is not a constant capacitor at all but a varactor. This cannot be de-embedded using s2p files so it was decided to use 0.6 pF given by the Smith Chart optimum, as when looking at the DLL the “ballooning” is equally distributed and allows the optimum to be moved onto the real axis.

In conclusion, the de-embedding was done using the files supplied from Qorvo during the measurements, and then de-embedded as close to the intrinsic i-gen plane using a 0.6 pF capacitor which will be applied post measurements.

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3.5.3 Optimum Performance

Before performing any VSWR sweep it is required to find the optimum impedance which will need to be swept around, the results from this will also act as a baseline for evaluating stress in the later results. The device is expected to operate at 28 V, but due to failures these sweeps were performed at 12 V to prevent any peak voltage failures and reduce stress on the device. The results for when the device is operated at 12 V are shown in figure 3.9, showing the optimum output power to be just over 1 W and 67% collector efficiency. The waveforms show the peak voltage and current are at 24 V and 0.4 A respectively, which is expected when operating in Class B and is not near the voltage or current failure limits of the device, seen to be 65 V and 0.8 A in table 2.5.

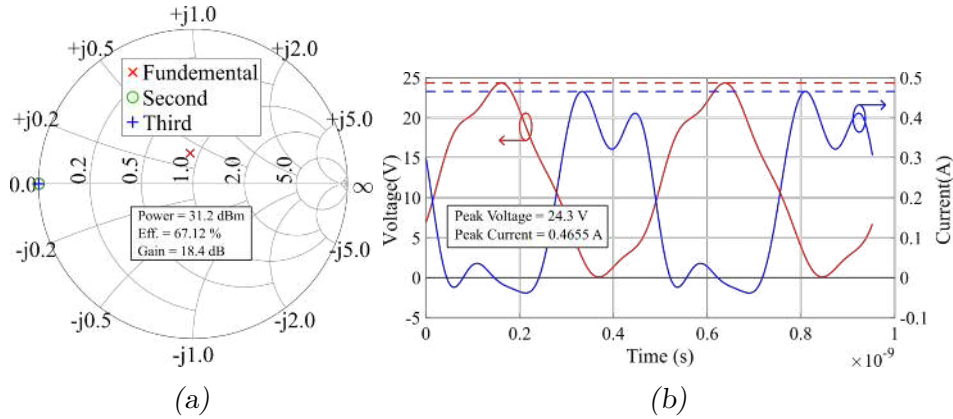


Fig. 3.9: Results from the Optimum measurement (a) Impedance locations and conventional performance data (b) Waveforms with waveform data

This was repeated at 28 V to obtain a peak voltage for the optimum at 28 V. This peak voltage can be used to scale the other results obtained at 12 V when looking for peak voltage stress. The results of the 28 V optimum sweep are seen in figure 3.10, which showed the peak voltage to be 56 V.

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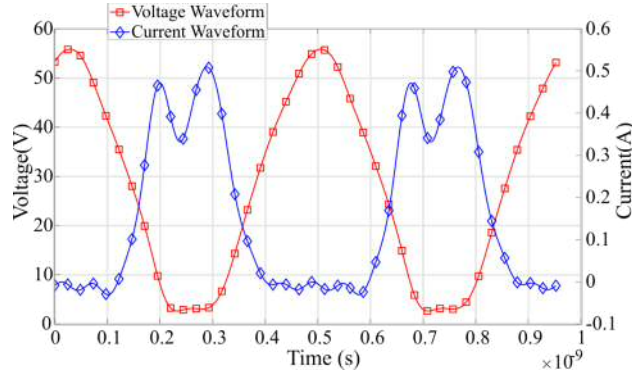


Fig. 3.10: Waveforms from the optimum measurement at 28 V, showing the peak voltage to be 56 V

3.5.4 Fundamental Impedance Sweep

This section shows the results of a conventional load pull sweep, where the sweep pattern followed in this section is shown in figure 3.11. The sweep involves holding the second and third harmonic impedances at a short circuit while the fundamental is swept around the complex optimum in a 5:1 VSWR circle.

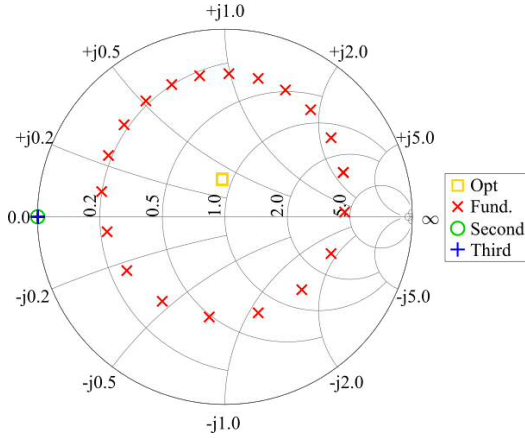


Fig. 3.11: Impedance locations for fundamental only 5:1 VSWR

The results from this sweep are shown in figure 3.12, where the results from a conventional system are seen in (a), then the peak RF voltage and

3. MULTI-HARMONIC WAVEFORM BASED VSWR SWEEPS

currents in (b) and the DLLs in (c), where all the results have been de-embedded using a 0.6 pF capacitor to show what is occurring at the intrinsic i-gen plane.

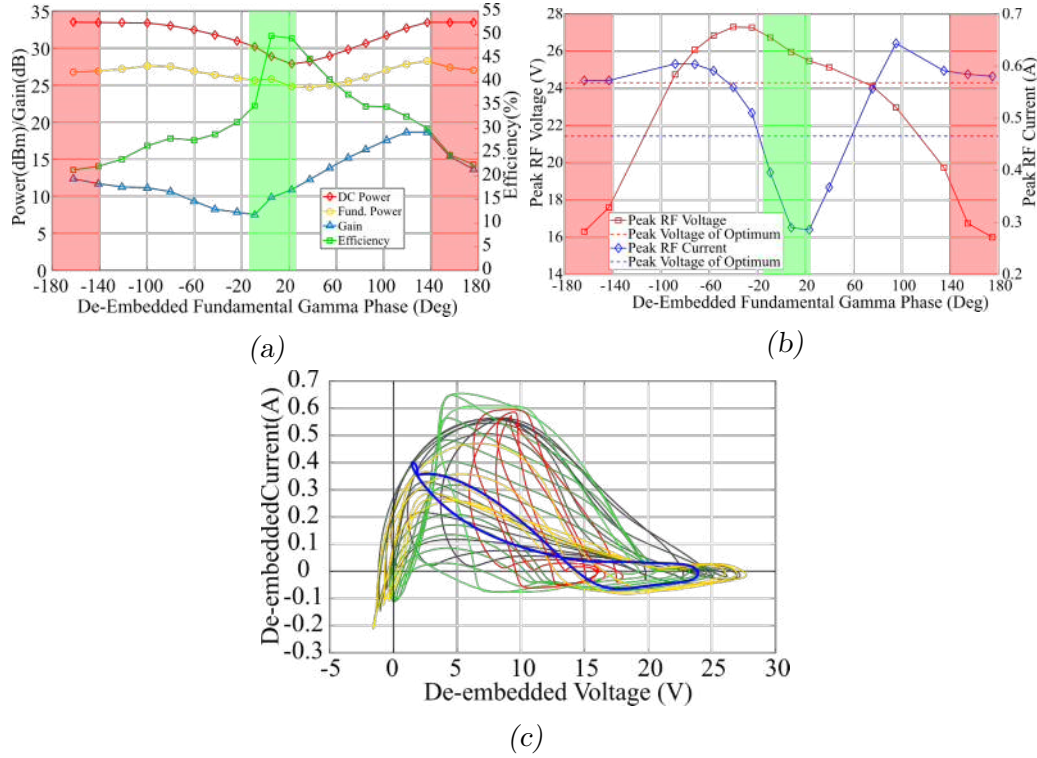


Fig. 3.12: Results from the fundamental only sweep a) Conventionally obtained data b) Waveform data, in the form of DLL's

Examining figure 3.12(a) it is seen that the point of highest stress is when the efficiency is low and the DC power is high, as this will mean more of the power is being dissipated as heat, so putting stress on the device. This occurs while the fundamental is nearest the short and these regions have been highlighted in red in figure 3.12. The area highlighted in green is where the DC power is low and the efficiency is higher meaning the device will be running cooler. Looking, next at figure 3.12(b), the same red and green areas have been drawn on from (a), where it is seen that the peak voltage

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stress occurs in the same location as the high efficiency and so voltage stress is not present in the conventional data, and the conventional data would even make the designer place the impedances at high efficiency locations and so inadvertently trigger peak voltage failure. This shows the need for waveform data to be present when stress testing a device. Finally, in (c) the DLLs have been plotted, with the DLLs that fall into the red section identified in (a) plotted in red, the DLLs that fall into the green sections identified in (a) plotted in yellow and the thicker blue line is the DLL when the fundamental impedance is at the optimum location for efficiency. This plot shows that the high dissipation of power is linked directly with the high current/low voltage DLLs, which causes self-biasing and low voltage swing, the self-biasing is due to the increased DC components generated by the asymmetric shape of the current waveform. As the peak current and the high thermal stress impedance locations are the same, if the thermal stress causes thermal runaway then applying cooling may help prevent failure, but if the peak currents are too high for the structure applying cooling will not prevent these currents from forming and not help prevent breakdown. Comparing these values to the breakdown limits of the device, current increased from 0.466 A, at the optimum, to 0.65 A at the peak of the sweep, this is an increase of 0.184 A and so an increase of 39.48%. This value will not scale as the DC voltage is scaled up, so in this case the peak current is not a potential failure mechanism as even at its peak, it did not exceed the device's current rating. The peak voltage that occurred increased from 23.9 V, at the optimum, to 27.7 V at the peak of the sweep, this is an increase of 3.8 V and so 16%. Using the results from the optimum and scaling up, the expected peak voltage from performing this sweep at 28 V is 65 V which is the same as the breakdown limit of the device and so may cause failure. In general peak voltage stress is a common cause of failure for HBT devices due to avalanche breakdown and thermal runaway, so makes it doubly important to be able to obtain the waveform data during the VSWR sweeps.

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3.5.5 Separate Second and Third Harmonic Impedance Sweep

This section will perform another single harmonic VSWR sweep, but this time use the sweep pattern shown in figure 3.13(b), where figure 3.13(a) is what ideally would be plotted when sweeping around a complex load. Unfortunately, the software is not capable of re-normalising to a VSWR sweep around a complex load or loading a custom load pull sweep yet and this meant that the second harmonic sweep had to be swept around the centre of the Smith Chart rather than the complex optimum. This led to the harmonic impedances not being equally spaced once the results had been further de-embedded down to the intrinsic i-gen plane.

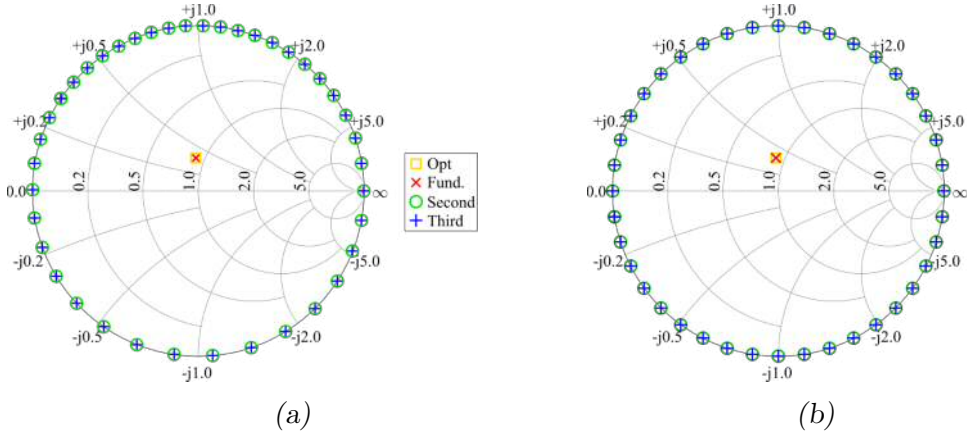


Fig. 3.13: Impedance locations for the fundamental, second and third impedance locations, where the second and third are swept around a $\Gamma = 1$ VSWR circle. (a) The correct locations (b) The actual locations that allow automated sweeping

The harmonics impedances were swept individually, and while one harmonic impedance was being swept the other was held at a short. The first sweep done was the second harmonic impedance and the results are shown in figure 3.14, then the third harmonic sweep results are shown in figure 3.15.

3. MULTI-HARMONIC WAVEFORM BASED VSWR SWEEPS

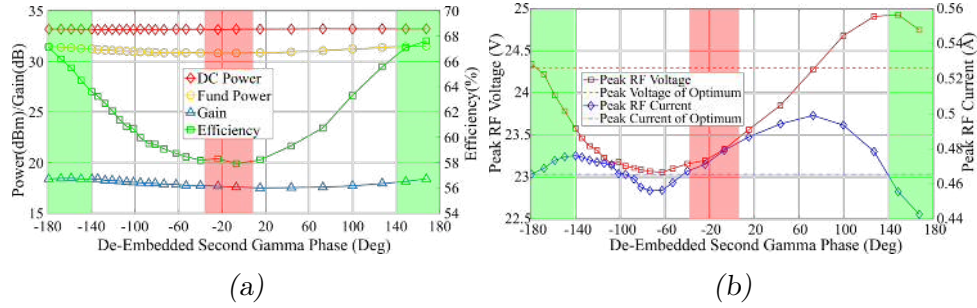


Fig. 3.14: Results from holding the fundamental at the optimum and sweeping the second harmonic impedance around $\Gamma = 1$ VSWR circle (a) Data gained during a conventional sweep (b) Data gain from adding waveform information

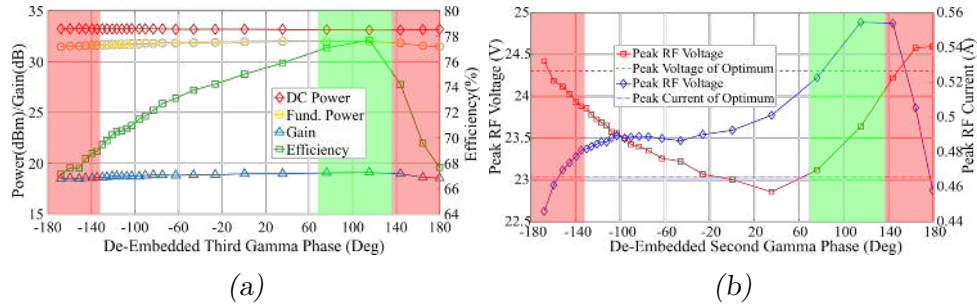


Fig. 3.15: Results from holding the fundamental at the optimum and sweeping the third harmonic around a $\Gamma = 1$ VSWR circle (a) Data gained during a conventional sweep (b) Data gain from adding waveform information

Looking at the de-embedded results in figure 3.14 and figure 3.15 the effects of not being able to perform a VSWR sweep around the complex optimum results in the points all being grouped to the left after the post measurement de-embedding. In a more extreme case this may cause peaks and troughs in the results not to be observed.

Again, looking purely at the conventional data first, in figure 3.14(a) and figure 3.15(a), the harmonics have the opposite effect when compared to each other, the second decreases efficiency, fundamental power and gain, as the

3. MULTI-HARMONIC WAVEFORM BASED VSWR SWEEPS

sweep moves away from the optimum ($\pm 180^\circ$), while the third increases them over the optimum. From this it would be assumed that the second harmonic is stressing the device more than the third, due to the increased thermal stress. The points of least stress have been highlighted in green and the most stress in red.

Looking next at the waveform data, figure 3.14(b) and figure 3.15(b), it is seen that the peak voltage is mostly decreased by both harmonics, and where it does go above the optimum it is not by a significant amount; with the second increasing it by 0.5 V (2% increase over the optimum- at 28 V this leads to a peak of 57.16 V) and the third 0.25 (1% increase over the optimum- at 28 V this leads to a peak of 56.6 V), neither of these increases is a cause for concern. The current in both these cases were mostly increased above the optimum to 0.035 A for the second and 0.09 A for the third, which is not as much as was seen when sweeping the fundamental alone. This shows the second has more influence over the voltage and the third over the current, when comparing the stress regions that have been copied across from both (a) plots, it is seen that the peak current and voltage both fall in the green area where stress is lowest according to the conventional data.

This section has shown that for sweeping the harmonics no significant voltage or current strain has been observed, but what increases did occur are hidden by the conventional data and so requiring the addition of waveforms to help identify potential causes of failure.

3.5.6 *Combined Fundamental and Second Harmonic Impedance Sweep*

This section combines the fundamental and second harmonic impedance sweep to show how the fundamental and second harmonic impedances interact to stress the device and cause peak voltages that are above the breakdown voltages. Due to there being two sweep variables, the plots are very crowded, but putting all the data on one plot allows for comparison of the full impedance space. They are formed by sweeping the second harmonic at every fundamental location, and then plotting each fundamental location against the swept second harmonic, which then forms a plot of many lines.

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Due to the number of lines on the plots, each parameter has its own plot, and only the key data, P_{RF} , η , V_{MAX} and I_{MAX} are plotted with the optimum shown on each plot, shown in figure 3.16.

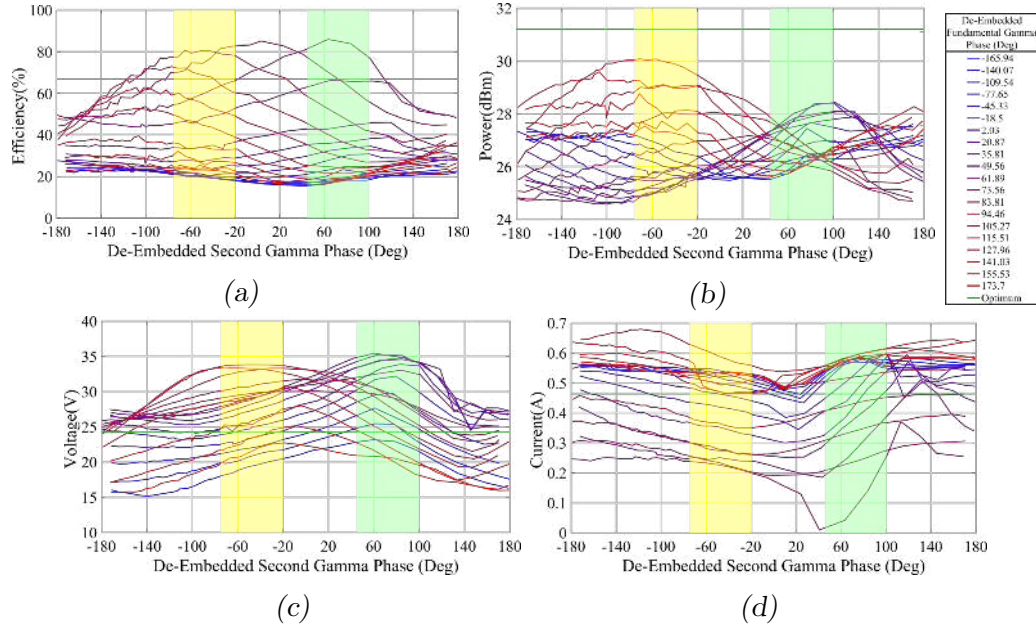


Fig. 3.16: Results from combined sweep (a) Drain Efficiency (b) RF Output Power (c) Peak RF Voltage (d) Peak RF Current

Starting with the waveform data first and looking at the voltage, two distinct peaks are seen, where each has been highlighted, one green and one yellow. Unlike with previous sweeps, these peaks are significantly more than the peak voltage of the optimum. Looking at the larger of the two (rightmost peak, green), it is seen that it is 35.45 V, up from 24 V which is an increase of 35.45% which is significantly above what was seen before when sweeping the fundamental (16%). Scaling this up from operating at a bias of 12 V to 28 V, it is expected that this peak will reach nearly 75 V, which is over the peak voltage limit rating for this device, 65 V, from table 2.5. This result shows the need for both the waveform data to be present to observe this and the requirement to sweep both the fundamental and second harmonic together

3. MULTI-HARMONIC WAVEFORM BASED VSWR SWEEPS

to trigger these peak voltages.

Looking at the conventional data, it is seen that these peak voltages are hidden by peak efficiencies that are above even the optimum. As was observed previously, this will make these impedance combinations attractive to a designer, but they will need the waveform data to be aware of the peaking voltages that are occurring at the same time. Next, looking at the power, these peaks are also observed but, unlike the efficiency, they do not recover the performance to the same level as the optimum, and the lower of the two power peaks corresponds to the larger of the two voltage peaks.

Looking now at the current, it is seen that the areas of low efficiency are the areas where the current peaks occur. As previously discussed, in section 3.5.4, solving the thermal problems that often are associated with low efficiency will not fix any peak RF current issues. This too could result in a potentially very troublesome problem to diagnose when the waveform data is not there to enhance the result set.

In this section, the full usefulness of the combined harmonic sweep and added waveform data has been seen; without it, potentially fatal voltages are hidden behind unassuming/attractive conventional data or may even never be tested during a conventional fundamental impedance VSWR sweep, leading to failures in the field that are not replicable in the lab environment. This ultimately will mean the failures go un-diagnosed and unfixed, and lead to a product being scrapped, this can make the design effort put into a product wasted, and this is why this project has been funded by Qorvo to help prevent this happening to the HVHBT.

3.5.7 *Combined Fundamental and Third Harmonic Impedance Sweep*

This section shows the effects of sweeping the fundamental impedance with the third harmonic impedance, although due to there being no obvious peaking effects only a preliminary experiment was done, which is shown in figure 3.17. The lack of any significant peaks in the voltage shows that the fundamental and third are not interacting here to trigger any voltage or current peaking effects that may cause the device to fail as the second does. Even

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the current increase that was observed in figure 3.17(d) does not see any significant third harmonic correlation, and the increases can be attributed to the fundamental, as seen in figure 3.12, not the third. The power and efficiency are seen to be reduced in general because from the optimum as the fundamental VSWR causes the device to perform sub-optimally, and the third is not able to recover the performance as was the case with the second, as seen in figure 3.16

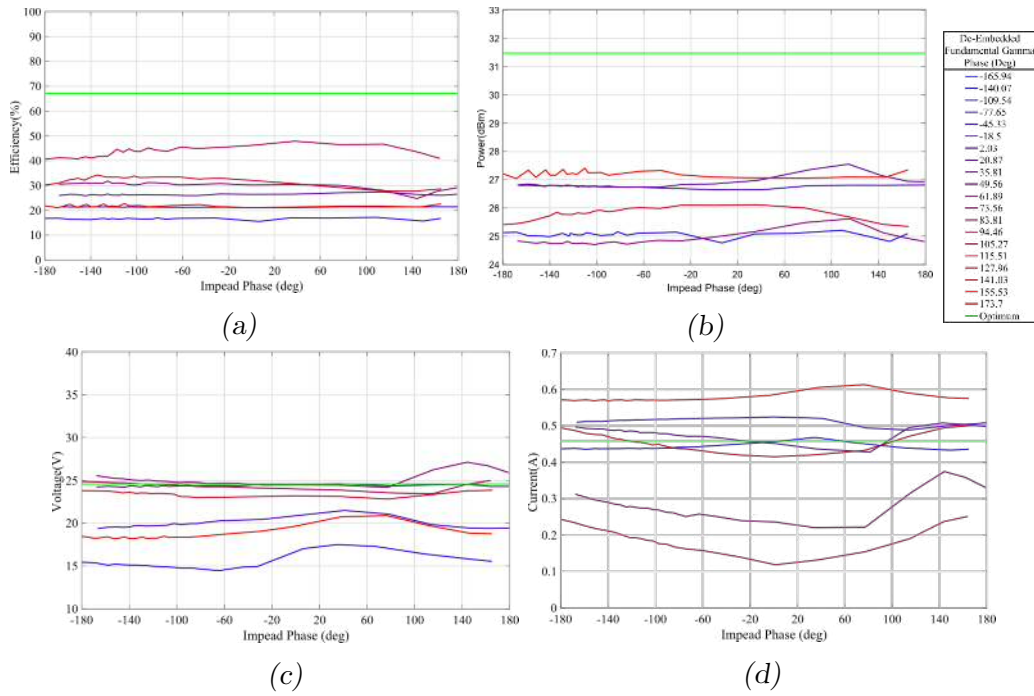


Fig. 3.17: Results from combined sweep a) Efficiency b) Power c) Peak Voltage d) Peak Current

The lack of impact on the peak voltage and current waveforms is due to the small magnitude of the third harmonic in this test, as seen in figure 3.18, where the fundamental and second/third component is plotted on a polar plot. Each loop represents a different fundamental impedance location and then the second/third impedance location was swept to form the loop. Both the voltage and the current have been plotted, with the voltage seen in (a) and (b) and the current seen in (c) and (d). The main observation from

3. MULTI-HARMONIC WAVEFORM BASED VSWR SWEEPS

these plots is that the third harmonic is almost half the magnitude of the second (seen by the size of the red circles) and so has less impact on the performance. But other operating conditions may result in a larger third harmonic, and so it is still important to include the third harmonic in these VSWR sweeps when looking for peak voltages and current.

3. MULTI-HARMONIC WAVEFORM BASED VSWR SWEEPS

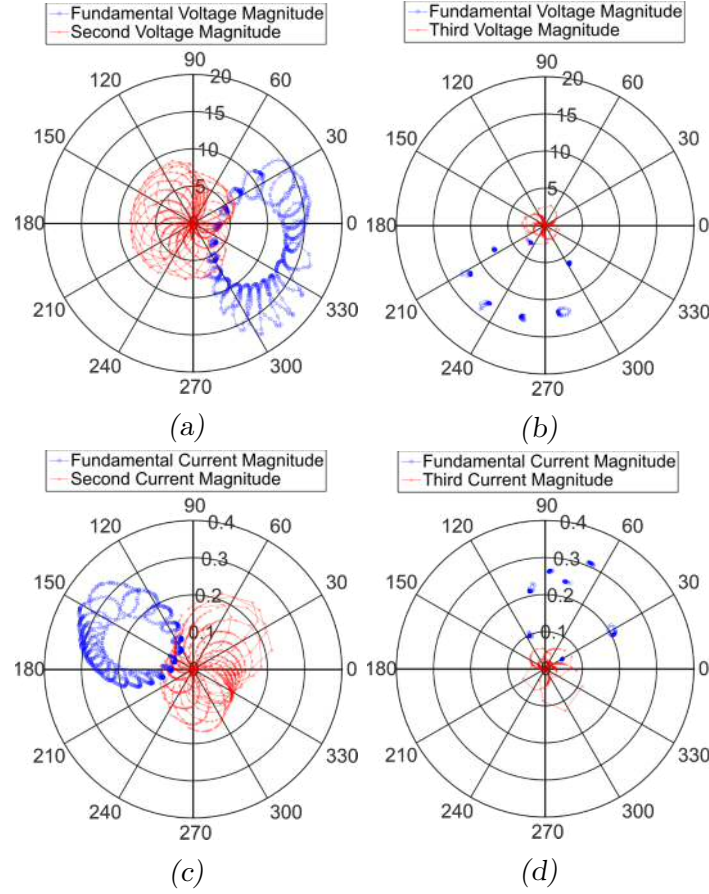


Fig. 3.18: Polar plots of the voltage and currents comparing the results from the combined fundamental and second sweep to the fundamental and third sweep. Each loop is a different fundamental location with the loop being the result of sweeping the second/third harmonic (a) Combined fundamental and second harmonic voltage plot (b) Combined fundamental and third harmonic voltage plot (c) Combined fundamental and second harmonic current plot (d) Combined fundamental and third harmonic voltage plot

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3.6 Conclusions

The primary motivation for carrying out the investigation into multi-harmonic waveform based VSWR was to look for the cause of failure of the HVHBT, which was thought to be peak voltage. This investigation observed peak voltages that when scaled up could cause the device to fail, which are summarised in Table 3.1.

Tab. 3.1: Potential damage caused by Peak Voltage

Sweep Type	Peak 12V (V)	% Increase Over Optimum (%)	Predicted Peak 28V (V)
Opt.	24	0	56
Fund. Only	27.7	16	65
Sec. Only	24.5	4	57.16
Third Only	24.25	0	56.6
Fund. + Sec.	35.45	32.3	75.6
Fund. + Third	27.12	13	63.28

Any voltage peaks that may cause breakdown when the peak voltage is scaled up to the theoretically expected peak voltage are highlighted in red in Table 3.1. It also showed the necessity for adding harmonics into the standard VSWR set up. With designers becoming more adventurous with harmonic terminations they may even stumble into a mode of operation that causes peaking voltages without realising it. It also shows the need to measure with waveforms, as when there were peak voltages the conventional data did not indicate a cause for concern but showed an increase in efficiency that is positive for a designer. It was also noticed that the current was increasing significantly above the optimum during these sweeps, but in this case not high enough to cause failure. Looking more deeply at the peak voltage result seen during the combined fundamental and second harmonic sweep and plotting the harmonic impedance locations at the point of peak voltage, it is seen that the impedance locations are grouped together. This has been plotted out graphically in figure 3.19, where one pair of fundamental and second

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harmonic locations were highlighted in yellow, and the other pair in purple. The arrangement of impedances strongly supports the idea that the device is being put into a form of continuous mode, as when the fundamental is capacitive the peak voltage is caused when the second harmonic is inductive and vis versa. It is likely that the device is being inadvertently put into inverse class F, [55], with the third shorted and the second open. The loss in power is most likely due to the fact the fundamental is removed from the optimum. This is an interesting discovery as it was expected that performance will degrade as the VSWR increases, due to the impedance moving away from its optimum location, especially since the fundamental has the most impact on performance. But this shows that there are be pockets of increased performance explained by CM theory, but this may also come at the expense of unexpected peak voltages or currents, and so will put the device under unexpected stress unless it is tested first using a multi-harmonic waveform based VSWR sweep to identify these areas of potential failure ahead of time.

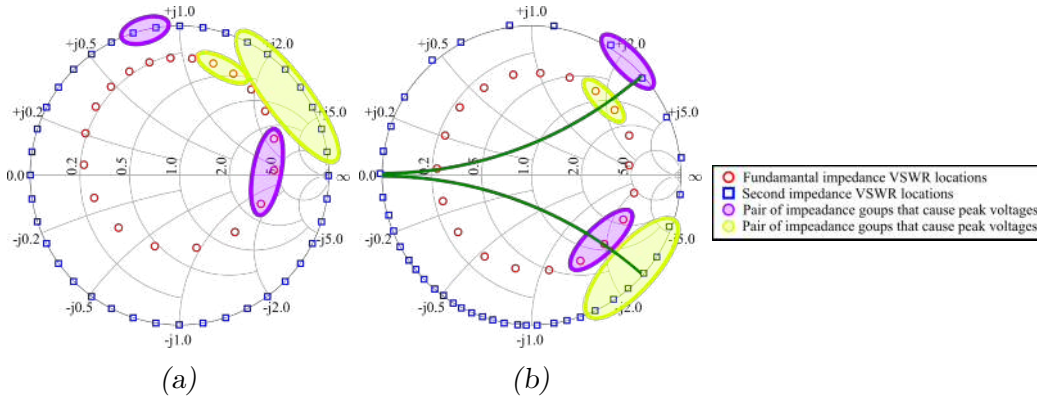


Fig. 3.19: Impedance locations of peak voltage (a) measurement plane (b) intrinsic i-gen plane

4

Case Study of VSWR Failures Using Waveforms

4.1 Introduction

The previous chapter looked at how VSWR sweeps are carried out and then how these sweeps can be enhanced to investigate potential peak voltage and current failure. This chapter will look at the real failures experienced during these VSWR sweeps, and how the different types of data can be used to help diagnose them. This will show the advantage of adding waveforms to conventional data to help diagnose a problem that otherwise would not have been possible and to show how this type of system could be used in a commercial environment to fault find and diagnose.

This chapter will first look at the sweep procedure, then identify the failure locations within this. To show how the different types of data can help diagnose failures during a VSWR sweep they are introduced in stages, firstly looking at the failure locations alone to identify a pattern to the failures, then adding the conventional data to identify some potential failure mechanisms and finally using waveforms to diagnose any remaining failures, and confirm the failures diagnosed using the conventional data. The results from this investigation focus around a grouping of failures where the fundamental and second harmonic locations are near one of the peak voltage areas identified in the previous chapter.

Prior to the investigation it was assumed that all these failures were due to peak voltage, but upon investigation other causes were identified. The majority of the failures were caused by increased negative current and voltage at the base of the HBT, which is clearly seen when looking at the DLLs in figure 4.6. Both these types of failure were caused by behaviour not

4. CASE STUDY OF VSWR FAILURES USING WAVEFORMS

observable or not clear when looking at the conventional data, thus requiring the addition of waveforms for a quick diagnosis of the problem. This chapter shows in a very practical way, how the addition of waveforms can detect the causes of breakdown that are undetectable using just conventional data.

4.2 *Sweep Procedure*

The sweep procedure is largely the same as described in the previous section but is now extended to include some extra sweep variables; both VSWR level and bias. All failures that occurred did so during the automated second harmonic sweep with all the other variables fixed. Where Chapter 3.4.2 can be looked at for how the optimum of the device was found, then the following parameters were systematically swept about the optimum:

Fundamental Harmonic: VSWR = 0 (opt), 5, 7 & 10

Second Harmonic VSWR = ∞ ($\Gamma = 1$)

Output DC Bias: $V_{COL} = 5, 12, 18, 22, 25, 28$

Input DC Bias: Class AB (specified by Qorvo, on a per technology basis)

These parameters were swept by following the flowchart shown in Figure 4.1. Note, it is saying that every time a new DC bias is used, the optimum was re-established, then once the optimum was found for a specific DC bias the fundamental impedance would be swept around a VSWR and finally for every point of the fundamental impedance VSWR the second harmonic impedance was automatically swept around a $\Gamma = 1$ circle.

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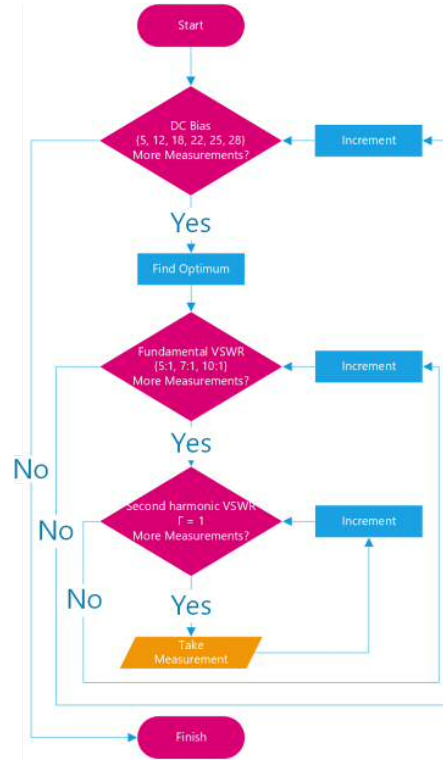


Fig. 4.1: Flowchart used to describe the sweep procedure

4.3 Failure Analysis

4.3.1 Failure Location

The device used during these failures were the HVHBT22 and HVHBT26, where an example of a pre and post failed device is seen in figure 4.2, where it is seen the collector feeds have burnt out, indicating some form of avalanche failure causing a spike in current.

4. CASE STUDY OF VSWR FAILURES USING WAVEFORMS

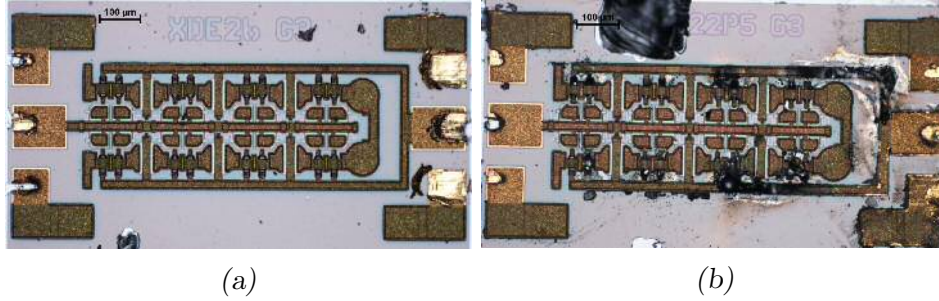


Fig. 4.2: HVHBT devices (a) An example of a HVHBT26 before failure (b) An example of a HVHBT22 after failure

A table showing a list of failure points is shown in table 4.1, where a unique failure number and symbol is given to each failure to help track it through the analysis; then the device type, operating voltage, and fundamental VSWR for which the failure occurred are all shown.

Tab. 4.1: List of failure locations

Failure Number	Plot Symbol	Device Type (um)	DC Drain Voltage (V)	VSWR
1	☆	22	12	5-1
2	○	22	12	5-1
3	*	22	12	5-1
4	+	22	12	5-1
5	□	22	28	5-1
6	☆	22	28	5-1
7	◇	26	18	10-1
8	▽	26	22	5-1
9	▷	26	22	5-1
10	×	26	22	5-1

It should be noted that there was not an equal number of tests done at all possible variables, as until the repeatability of the failure was observed, the 22 um, 12 V and 5-1 VSWR condition was repeated, which has led to the disproportionately high number of failures under this test condition.

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Then, when moving onto other test locations, caution was taken to avoid the suspected failure location, and once a failure had occurred near the suspected failure location no more measurements were done in that area, so reducing the number of failures under other operating conditions.

The impedance locations where failure occurred is shown in figure 4.3(a), where both the fundamental and second impedance location has been plotted and joined together with a dotted line. The arrows around the edge denote which direction the second harmonic was swept in.

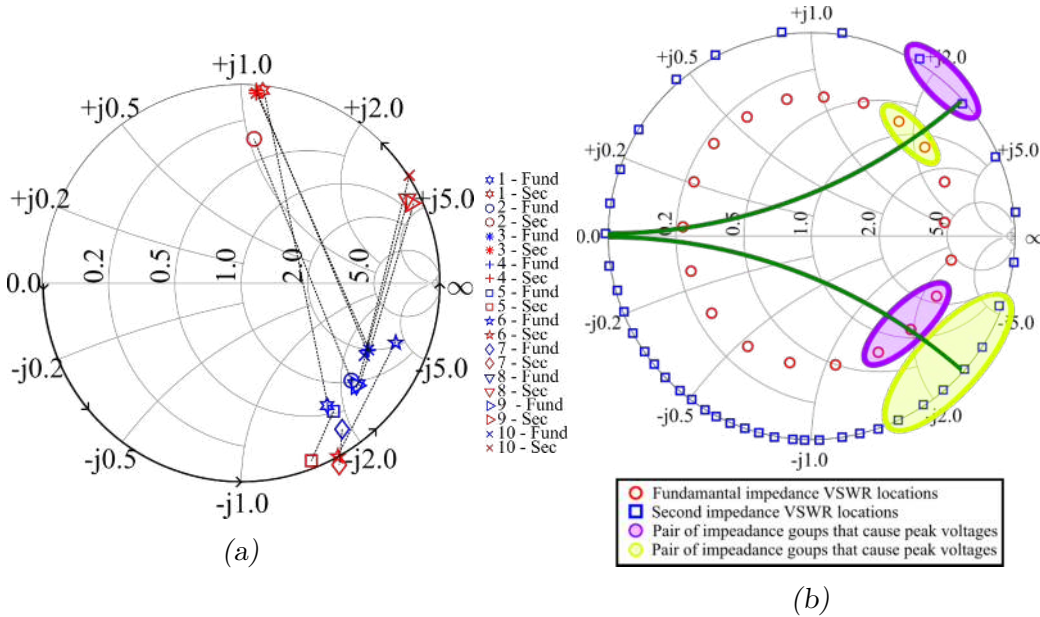


Fig. 4.3: (a) A Smith Chart showing the de-embedded fundamental and second harmonic impedance locations just before failure. Each fundamental and second harmonic pair are joined by a dotted line. fundamental impedance = blue; second harmonic = red (b) The de-embedded impedance locations that cause peak voltages

First, looking at figure 4.3(b), which is just a copy of figure 3.19, shows the fundamental and second impedance locations that caused peak voltage stress, so failures at these impedance pairs would indicate high voltage failure. Next, looking at figure 4.3(a), where the actual failures occur, it is seen that

4. CASE STUDY OF VSWR FAILURES USING WAVEFORMS

most of the fundamental and second locations are in or near the purple peak voltage region, indicating these could be peak voltage failures. In this case the 28 V failure could be peak voltage failure as the devices failed before reaching the optimum location for peak voltage. The 18 V failure also failed at the same location as the 28 V failures, but due to the lower bias operation it is not likely to be peak voltage failure, which suggests a second failure mechanism or none of these are peak voltage failures. Similarly for the 12 V and the 22 V failures, due to the lower operating voltages they are not peak voltage failure. Looking at the impedance locations for the 12 V and the 22 V failures, the 12 V failures allow the second harmonic to move out of the predicted peak voltage stress zone, which could also indicate a failure mechanism other than peak voltage.

From just using the impedance to try and diagnose the failures, some initial hypothesis about what the failure mechanisms might or might not be have been stated, but there is not enough evidence to draw firm conclusions yet. At this point more questions have been raised than answers by increasing the number of potential failure mechanisms, this shows the need for more information before these failures can be diagnosed.

4.3.2 *Conventional Data*

The next layer of data that can be added is the data obtained from a conventional load pull system, in this case DC & RF output power, DC input current and drain efficiency, which is obtainable from most VNA based load pull setups. This conventional data is shown in figure 4.4 where the sweep leading up to the point of failure is shown so that any trends leading up to the failure can be seen. The plotted line stops at the point of device failure.

4. CASE STUDY OF VSWR FAILURES USING WAVEFORMS

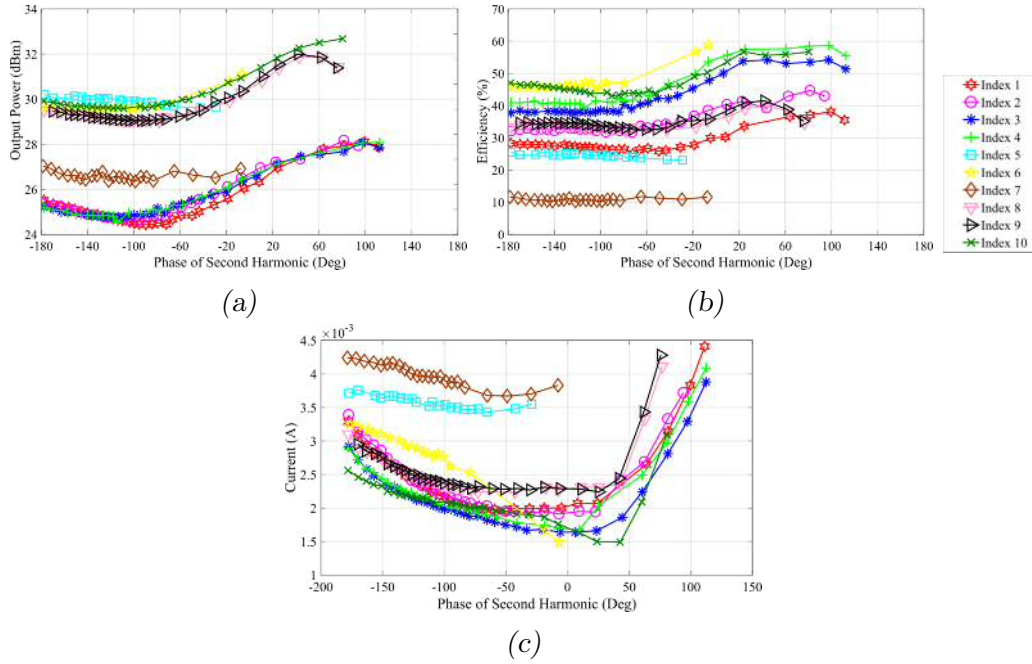


Fig. 4.4: Second harmonic impedance sweep leading up to failure
(a) RF output power (b) Drain efficiency (c) Input DC current

Looking across all the plots, there are two failures that do not follow the trend of the wider group, failure's 5 & 7, where it is seen that although their power levels are not dissimilar, their efficiencies are lower and they have too much input current. As covered in Chapter 2.4.2, input current leakage is a signal that there is some physical damage to the device that went un-noticed in previous sweeps and was likely a gradual degradation until finally failing during this sweep. The fact they failed in such close proximity to each other may suggest another underlying stress mechanism is at work, but it is not possible to tell from this data.

Looking at the other 28 V failure (failure 5) it is seen that it has good efficiency and its power matches other results, but it fails at a lower power than the other sweeps. Also looking at DC current it fails at one of the lowest recorded currents, and so there does not seem to be any direct cause of failure identified here.

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Next, looking at the 12 V failures (failure's 1 - 4) it is seen that they have lower power, which is to be expected from the lower DC operating point, their efficiencies are not consistent - but not showing any obvious trends. From just looking at the output data there is not an obvious cause of failure. The same can be said for the 22 V results (failure's 8 - 10), although their power levels are higher, although they peak at just below 2 W which is much lower than the devices expected power capabilities. But looking at the input current, both the 12 V and 22 V failures have a spike in input current, seen in figure 4.4, starting when the second impedance phase is at 50° , which shows a common trend before failure. Failure 10 seems to be a bit of an outlier as it failed with a much lower input DC current. When discounting failure 10 the spread of current just before failure is slightly over 0.5 mA. It is also noticed that the partially failed devices seem to survive this peak input current despite being damaged, which may steer the investigation away from input current as a cause, if waveform data was not available to help.

4.3.3 Waveform Data

The final layer of information, waveform data, is added in this section and shown in figure 4.5. The peak RF voltage is shown in (a) and the minimum RF voltage is shown in (c), the peak RF current is shown in (b) and the minimum RF current shown in (d). For figures e-h the input and output DLLs are shown for the measurement before failure and the failures. The failure plotted on e-h are split into two groups to help prevent the plots becoming over-crowded; the 12V and 22V failures (failure's 1-4 & 8-10) have their input DLLs in (e) and output DLLs in (f), with the 28V and 18V failures (failure's 5-7) have their input DLLs in (g) and output DLLs plotted in (h).

4. CASE STUDY OF VSWR FAILURES USING WAVEFORMS

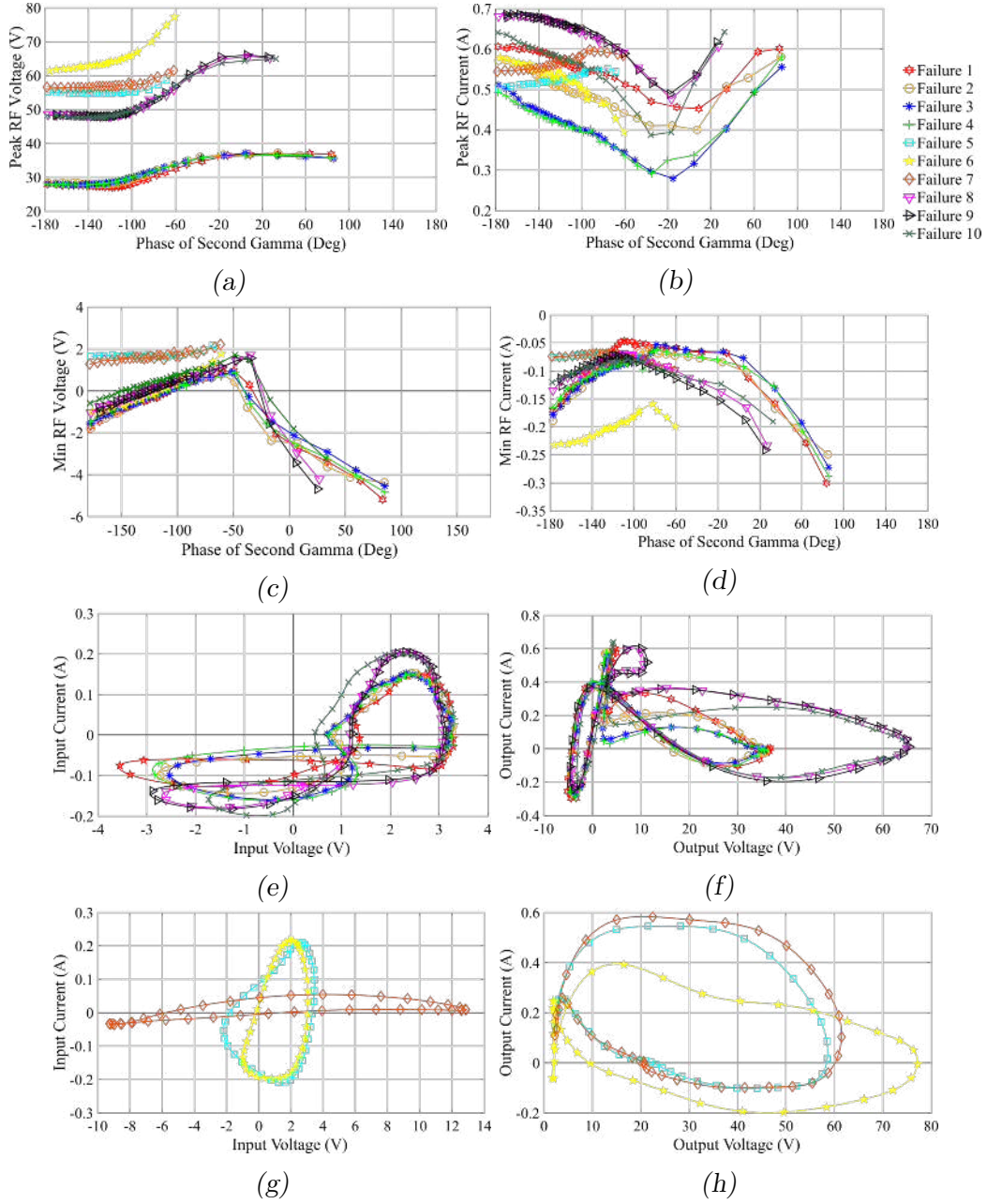


Fig. 4.5: Waveform data used to analyse failure locations (a) Peak output RF voltage (b) Peak output RF current (c) Minimum output RF voltage (d) Minimum output RF current (e) Input DLLs of failures 1-4 & 8-10 at the point before failure (f) Output DLLs from failures 5-7 at the point before failure (g) Output DLLs from failures 1-4 & 8-10 at the point before failure (h) Output DLLs from failures 5-7 at the point before failure

4. CASE STUDY OF VSWR FAILURES USING WAVEFORMS

Looking first at the peak voltage plot in figure 4.5 (a), it is seen that failure 6 is a peak voltage failure consistent with operation over the expected voltage rating for the device before failure, showing again that peak voltage failures can leave little/no evidence in the conventional data to identify them, and without waveform data it would be extremely hard/impossible to diagnose them. But with waveform data they are diagnosed very quickly.

Looking next at peak RF current for failures 1-4 & 8-10 in figure 4.5 (b), where the peak output RF current takes a similar trajectory before failure for each of these failures. Also this was seen in the input DC current, as shown in figure 4.4 (c) which is to be expected given the link between input and output current in HBTs. They do not fail at the same peak output current measured for each device, showing that the failures are not related to peak output RF current.

The minimum output RF voltage and current shown in figure 4.5 (c) and (d) respectively shows that there is also an increasingly negative trajectory leading up to the point of failure, for failures 1-4 & 8-10. The grouping for the minimum output RF voltage and current, not including the outlier (failure 10), is a 1 V spread for the output RF voltage and 60 mA for the output current. This combined effect is most clearly seen in the output DLLs for these failures in figure 4.5 (f), where they all push into the third (bottom left) quadrant where the voltage and current are both negative, which is most likely the cause of the failure. The negative voltage and current would represent the base-collector junction becoming forward biased and so an increase in current coming the wrong way across the junction into the base, which can cause sudden and catastrophic failure with the forced increase in base current.

Comparing this to the input DLLs shown in figure 4.5 (e), it is seen that there is also a corresponding negative voltage and current swing, which would also explain the increase in input DC current. By adding waveforms, a much more comprehensive picture of what is happening within the device is seen. This allows changes/fixes to be made with a much higher level of confidence, in this case to change the physical structure to prevent the RF current and voltage going into the third quadrant.

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Finally, in figure 4.5 (g) and figure 4.5 (h), the input and output DLLs are shown for the remaining failures (failure 5-7). Looking first at (h) the peaking voltage is seen for failure 6, which in a design situation would be desirable, but in this instance it is detrimental to the lifespan of the DUT as it caused failure. Looking lastly at the waveforms for the devices that suffered a gradual degradation over time (failures 5-7), shows that while the output waveforms of the two devices are similar, the input DLLs are different from each other, with failure 5 seeming to be functioning better than failure 7. These different input DLLs show there may have been very different failure mechanisms in each instance and just a coincidence that they failed at similar impedance locations. It could have also been that previous measurements weakened the device and then the peak RF voltage was the cause, as both peak voltages are close the devices predicted peak RF voltage breakdown limit of 65 V, or thermal stress caused by high instantaneous RF current and voltage.

In summary the waveform data allowed the voltage failure to be clearly seen and worked together with conventional data provide a fuller picture of what was occurring within the device during the third quadrant failures. This extra waveform data also showed more clearly how to mitigate future failure. Overall this shows that combining multi-harmonic VSWR with waveform data provides a comprehensive and necessary set of tools to run failure diagnostics with.

4.4 *Solving the Problem*

The main cause of failure was brought about by the DLL pushing into the third quadrant. While this project was progressing, and feeding the results back to Qorvo, a newer version of the HVHBT, called the HBT6, was developed. It is not known exactly what changes were made to the structure of the HVHBT to make the HBT6, other than the emitter length being changed to 20 μm , from 22 and 26 μm on the HVHBT. This new device was tested using the same sweep as before to see if it solved any of the failures. To see if the failure mechanism has been fixed a comparison of the output DLLs is

4. CASE STUDY OF VSWR FAILURES USING WAVEFORMS

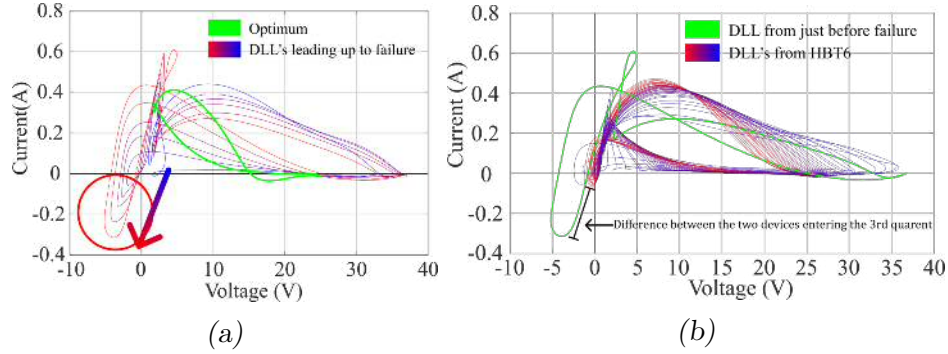


Fig. 4.6: Output DLLs comparing the new HBT6 with older HVHBT failures (a) HVHBT waveforms, with cause of failure marked by a red circle (b) HBT6 waveforms

shown in figure 4.6. The change in how much the new device allows the DLL to penetrate the third quadrant has been reduced, where in (b) the entire sweep was carried out and no failures occurred due to the HBT6 DLLs not pushing into the third quadrant like the HVHBT.

4.5 GaN FET Competitor

Qorvo were also developing GaN FETs that compete with the HBT processes. They had two different 50 V GaN processes they were developing, named GaN25HV and GaN50. Both processes had passed internal VSWR testing, but this system did not sweep the harmonics or capture waveforms. This section applies the VSWR sweep to these new GaN FET devices to make sure the peak RF voltage was never reached. The same principle was re-applied to these tests, a scaled back drain voltage was applied, in this case 20 V, down from 50 V, and then the various sweeps were run and the results for each device are shown in figure 4.7 for the GaN25HV and figure 4.8 for the GaN50.

4. CASE STUDY OF VSWR FAILURES USING WAVEFORMS

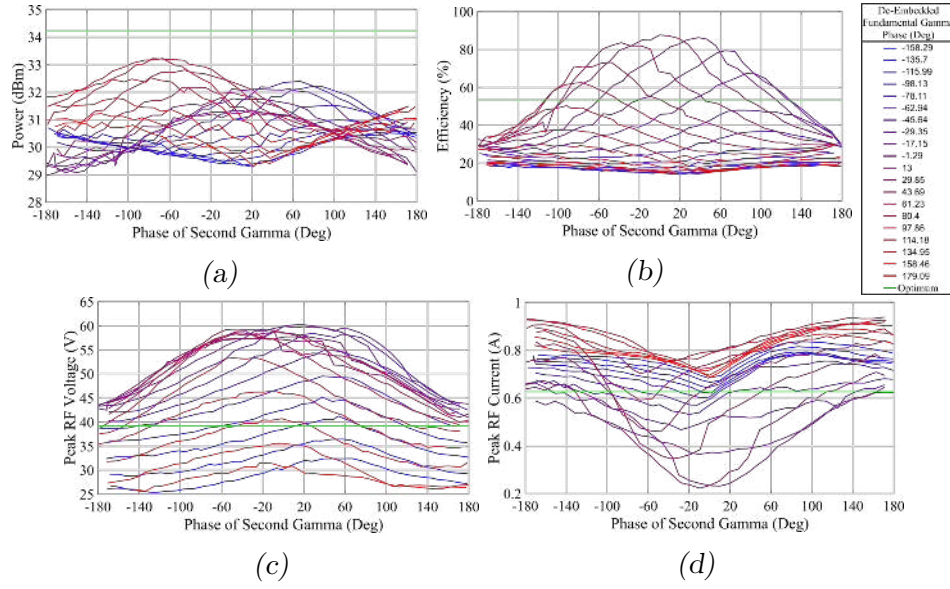


Fig. 4.7: GaN25HV VSWR results, done at 20 V (a) RF output power (b) Drain efficiency (c) Peak output RF voltage (d) Peak output RF Current

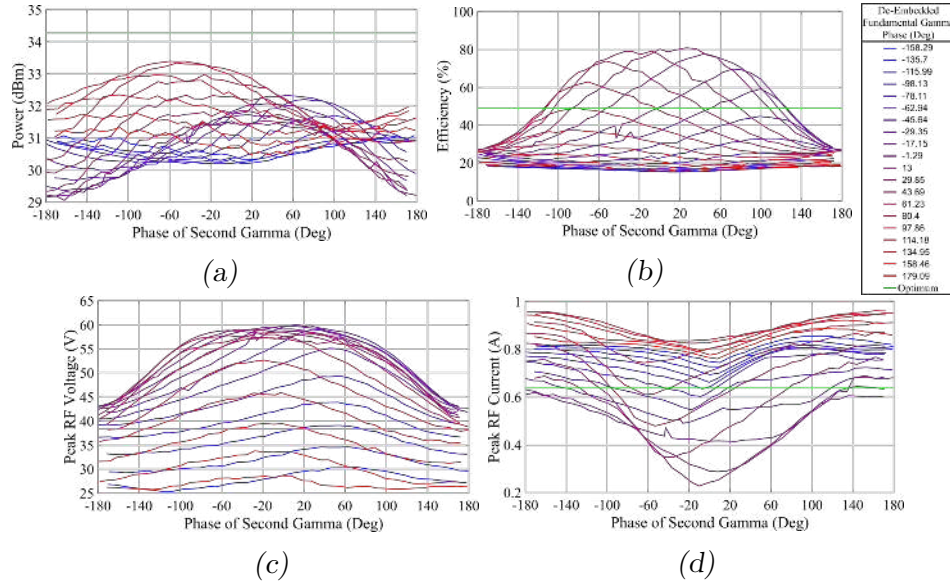


Fig. 4.8: GaN50 VSWR results, done at 20 V (a) RF output power (b) Drain efficiency (c) Peak output RF voltage (d) Peak output RF Current

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These results are very similar, despite being based on very different processes. The GaN FET results show all the same characteristics as the HBT results, with a relative decrease in RF output power seen in (a) of figures 4.8 & 4.7 and increase in drain efficiency seen in (b) of figures 4.8 & 4.7, peak voltage seen in (c) of figures 4.8 & 4.7 and peak RF current seen in (d) of figures 4.8 & 4.7. Looking first at (c), the peaks in the peak RF voltage seem to have merged, compared to the voltage peaks shown for the HBT in figure 3.16(c). This is due to different fundamental locations that are causing the peaking effect that have an overlapping second harmonic component that merges the two peaks. It is also seen in (c) that a significant voltage increase is seen for both devices, this time from 39.23 V to 60.22 V for the GaN25HV and then 38.35 V up to 60.03 V for the GaN50, which is an increase of 34.86% for the GaN25HV and 36.12% for the GaN50. This shows that FET based devices have the same voltage peaking effect as HBT devices, and their voltages were increased by a comparable amount to the HBT which had an increase of 32.3%. Scaling these voltages back up gives an expected peak voltage of 136.12 V for the GaN25HV and 132.3 V for the GaN50, which are less than the breakdown voltages seen in table 2.5. One reason the peaking voltage is not a problem for the GaN FET devices is the GaN technology which has much higher breakdown voltages than GaAs, which is what the HBT devices were based on. Another point of comparison is efficiency seen in (b). The FETs optimum efficiency is 12% lower than the HBT, dropping down from around 67% for the HBT to 55% for the FET, which is a common observation and would cause HBT to be the preferred design choice if it was not struggling with failures.

4.6 Conclusions

At the start of this chapter a group of failures were presented which all occurred at a similar fundamental impedance location, with some separation in the second harmonic. Then, by building up the data in stages the merits of each set of data was seen and especially how the waveform data can both identify previously unseen possibilities for failure, and work together with

4. CASE STUDY OF VSWR FAILURES USING WAVEFORMS

conventional data to gain insight into why failures were occurring.

The third quadrant failure was clearly identified by the waveform data, where as the conventional data only hinted at the solution, showing the advantage of having access to the waveform data and being able to better understand the device and why it was failing. The waveform data also allowed for the peak voltage failure to be diagnosed where there was no evidence of failure in the conventional data, this again showing the necessity of waveform data to be able to diagnose and better understand why failures are occurring.

This chapter has shown that adding waveform data with the novel multi-harmonic sweeps will:

- Increase knowledge of the device's weaknesses before costly designs are done
- Increase speed of diagnosis
- Identify previously unseen failures
- Identify cause of conventionally observable failures

It has also been seen that FET based devices also show that same voltage peaking effects as HBT devices, but due to their much higher breakdown voltage as a result of being based on GaN means these peak voltages are not an issue for these FET devices. This and the more rugged channel construction means that FET based devices will remain the device of choice for most base-station applications due to their increased rigidity, despite lower efficiencies.

Analysing Performance Effects of DC-RF Dispersion

5.1 Introduction

This chapter introduces a novel way to analyse waveform data to show how the DC-RF dispersion affects performance and allows meaningful comparison between device technologies. Chapter 4 showed that HBT based devices had higher performance than the GaN FET competitors, but the FET devices were more robust, and so chosen as the technology to use for any future design.

The next step was to use waveform data to do performance analysis on the two potential GaN 50 V processes (GaN50 and GaN25HV), to show which has the better performance. As knee walkout is a dominant performance limiting effect at high output bias levels, this will be the focus of the investigations and how it affects performance. Knee walkout is the dispersion between RF-IV and the DC-IV characteristics around the knee region, and how this difference increases at higher output bias voltages.

This chapter will start by going over the basics of what is being measured and why, and then showing how to transform these measurements into more meaningful plots that allow a comparison of both FET devices. Then, using these plots, it was seen that the GaN50 had higher output power than the GaN25HV at the compression level so was chosen to progress the Continuous Class B design.

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5.2 *Theory*

To make a RF-IV using waveforms, it is first required to make a fan diagram, which is something Cardiff has been able to do for some time, and any waveform based load pull systems can do it. But extracting useful performance information from these plots to clearly show effects of DC-RF dispersion and allow comparisons of different devices, has not yet been done. This Chapter lays out how these performance plots are produced and then uses them to compare the two GaN FET technologies under consideration for the Continuous Class B design. The fan diagram uses several RF DLLs at different impedances to build and show the extreme limits of the RF-IV. This then shows what the knee looks like for the current output bias voltage. It is used to show how the RF knee differs from the DC knee, often to show how increasing the DC drain voltage will cause the knee to walkout. This is important because the knee directly affects the power and efficiency.

This allows fan diagrams to provide insight into how different device technologies perform and more importantly why, showing waveform engineering can be a valuable tool in performance analysis too, not just failure analysis. This thesis then uses multiple fan diagrams measured at different DC bias points, and then sets a target peak RF current level to allow performance vs. knee walkout to be examined, allowing an optimum to be found, or to identify any trade-offs in performance when targeting different current levels or DC bias points and why.

5.2.1 *Fan Diagram*

The fan diagram was first used when investigating the drop in efficiency as the DC drain voltage was increased. This became much more apparent in early GaN based FET devices, leading to GaN struggling to compete with GaAs on efficiency, which is also true for SiC based high power transistors. The DC-RF dispersion can be measured using pulsed DC measurements, but using waveform based measurements allows for a much larger dataset to be generated with the DC-RF dispersion plot which this research seeks to take

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advantage of for the first time.

This subsection sets out how the knee is measured and plotted to give the reader a firm understanding of what data is used to generate the performance plots that are generated in this chapter and will be used to evaluate the two technologies. The main data source for the fan diagram, are a collection of DLLs, measured at a constant drain DC voltage, but at different real impedances to map different areas of the knee. The fundamental impedance is kept on the real axis to reduce any looping in the waveforms, causing the DLL to form as close to a single line as possible that can be used to accurately identify the RF knee. An ideal example of the fundamental impedance swept and the DLLs obtained is shown in figure 5.1.

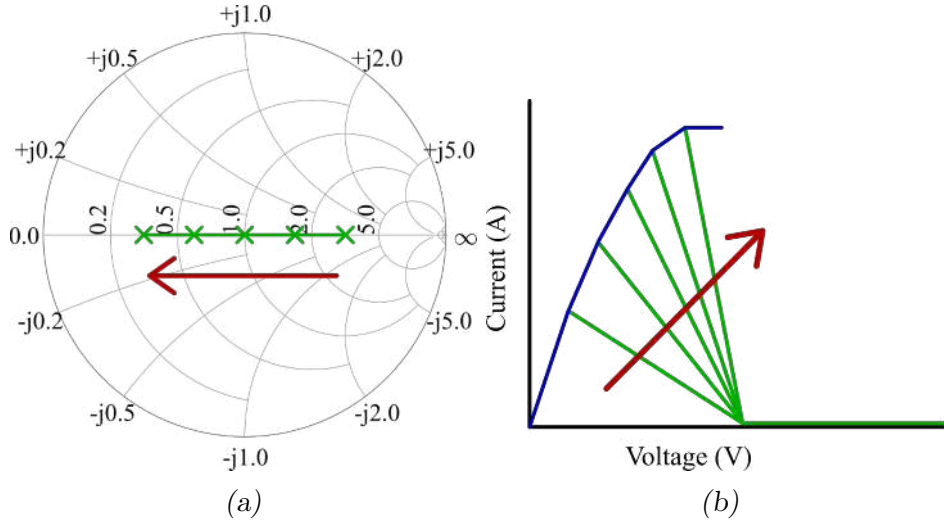


Fig. 5.1: Example DLLs that form a fan diagram (a) The impedances used, and the direction they are swept in (b) The DLLs generated from the sweep and then the blue line shows how they are used to draw out the RF knee

There are two different ways of measuring the DLLs, shown in figure 5.2. One where the harmonic impedances are held at the same location as the fundamental impedance, (a), and the other where all but the fundamental impedance is shorted, (b). Comparing (a) and (b) it is seen that the main

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difference between the two methods is that when all the impedance locations are held at the same location the DLL will go up to the knee and then compress, rather than following the knee down. Shorting the harmonics would seem like the obvious choice, allowing a much larger portion of the knee to be mapped out by a single measurement. But plotting thin lines like the ideal plot shown in (b) is not always possible, although it has been achieved in the past [11]. What you often actually get is a looping effect comparable to that shown in (c). When this looping does occur, due to reactive components in the voltage and current in some of the uncontrolled harmonic impedances, an average line can be drawn down the middle to estimate the knee boundary, but this causes the knee boundary to become a fuzzier region, rather than a sharp edge, which can be problematic for diagnosing efficiency drops in a new process. Holding all the impedances at the same location helps solve this issue as there is only a small amount of looping at the top of the DLL and so the edge of the knee can be much more clearly identified.

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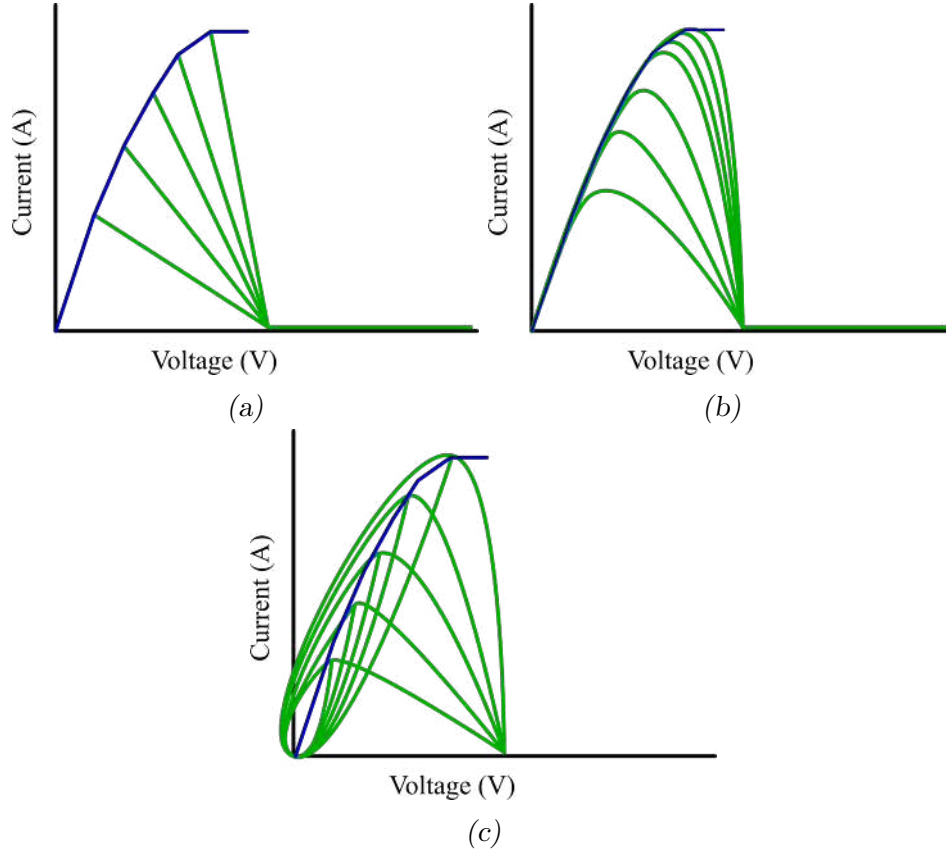


Fig. 5.2: Example DLLs being used to map out the knee (a) Keeping all the harmonics at the same location as the fundamental (b) Shorting the harmonics (c) Effects of looping on the DLLs using the shorted harmonic impedances as an example

The next step is to re-do this process at different drain bias levels to observe the knee walkout phenomenon, as shown in figure 5.3, where an idealised example of how a full knee walk out plot is put together.

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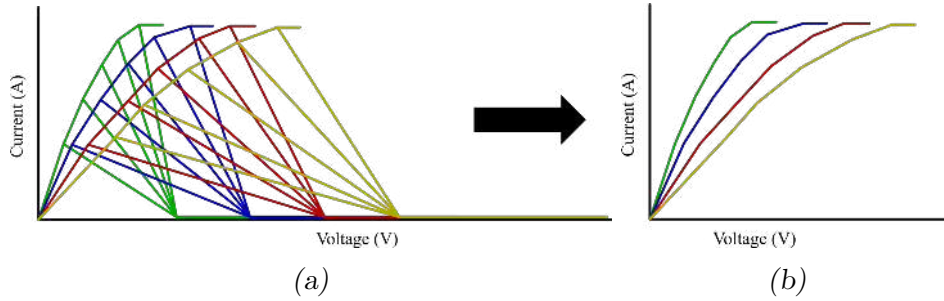


Fig. 5.3: Example DLLs that then form a fan diagram (a) Plotting each set of DLLs and draw a line of best fit on them (b) remove the DLLs to more clearly show the knee walkout

Plotting knee walkout with all the DLLs on the same plot, as shown in figure 5.3(a), causes the plot to become crowded and hard to understand what is occurring, so they are often removed and just the knee line for each bias point shown, as shown in figure 5.3(b), to allow the knee walkout to be shown clearly. While the RF knee is compared directly to the DC knee, the RF knee is not as “hard” as the DC knee, especially on GaN devices. As the drive is increased it will cause the knee to slowly push back into the DC knee until it cannot reduce any further, often at 6-10 dB of compression. But devices are not often run more than 3dB into compression due to linearity limitations. To obtain meaningful knee results, the device needs to be driven to the same level as it is intended to run at, preventing the knee giving better results than would be seen in real use and obtaining higher power/efficiency than the device outputs under normal operating conditions. To do this and to make the knee plots comparable to the DC-IV, the drive power is swept with the fundamental impedance at the optimum and then the input voltage is noted at the desired level of compression and then the knee is mapped out by driving the device to this input voltage every time.

5.2.2 Constant Current Plots

While the knee plot has now been generated, it does not show how walkout affects power, efficiency, gain and other parameters important to designs. The method shown in this section achieves this by extracting the useful

5. ANALYSING PERFORMANCE EFFECTS OF DC-RF DISPERSION

performance information from fan diagrams. It starts from the assumption that every device has a peak current and DC supply where the performance is optimum, this optimum is determined by the following factors:

Knee: As higher and higher currents are targeted the knee voltage increases. As shown in figure 5.1(b), this will start trading the peak voltage swing for smaller and smaller amounts of increased current swing until it saturates and there is no current swing increase, which will eventually start to cause a loss in performance rather than an increase. This means there will be an optimum output impedance that compromises between peak voltage swing and peak current swing.

Voltage Breakdown: The devices physical limits are not infinite and so there is an upper limit on what the DC bias can be to prevent failure, which will vary with the class of operation, and device/material type.

Knee Walkout: As the knee walks out and reduces performance it will make targeting higher DC voltage bias points less attractive, as the net performance increase for using higher bias points reduces until there is none. This will lead to an optimum DC bias for efficiency and power.

The fan diagram is the key data source in this chapter with the expectation that it will be able to extend its capabilities to include how performance varies up and down the knee and with knee walkout. To plot the performance parameters requires the use of two different plots in conjunction, the fan diagram made in the previous sub-section and a similar plot, but instead of plotting voltage vs. current it plots knee voltage vs. a performance parameter, as shown ideally in figure 5.4.

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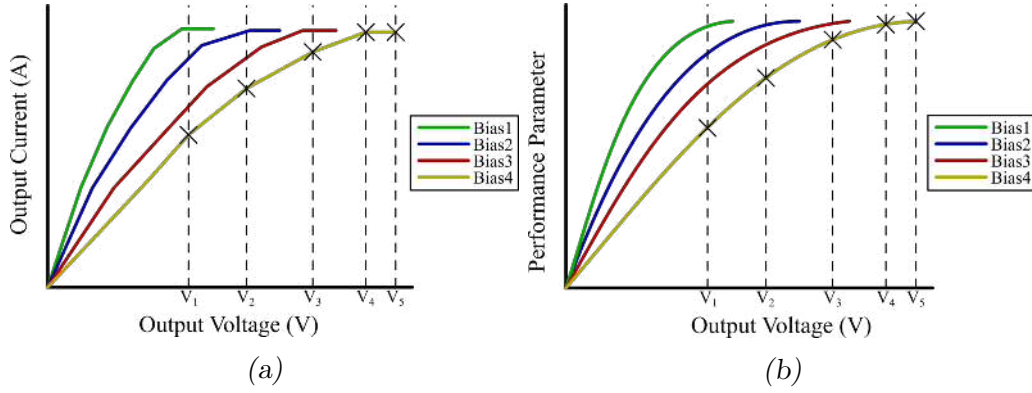


Fig. 5.4: Converting the RF-IV to performance plot, each black 'X' represents data from a single DLL (a) The RF-IV plot shown in figure 5.3 with the data points marked on the Bias4 line with an 'X' (b) The performance plot, instead of plotting output voltage vs output current, plotting output voltage against the performance parameter of interest.

This is then used to generate the final result, an example of this that shows how performance varies with bias and different peak target currents is seen in figure 5.6(b), where the bias is plotted along the x-axis and the different target currents are represented by different lines, so it is easy to see how increasing target current and bias voltage affects the performance. One example of how to generate the plot in figure 5.6(b) is to plot output DC bias vs. knee walkout. To do this a target current is selected, as shown in figure 5.5(a), then where that line intersects each RF-IV the voltage is read off, giving a value of knee walkout for each output bias point. This is then plotted as shown in figure 5.6(b), skipping the plot shown in figure 5.5(b), as in this case the B and P variables are equal. This process is then repeated for different target currents to form a family of lines to plot, as shown in figure 5.6(b).

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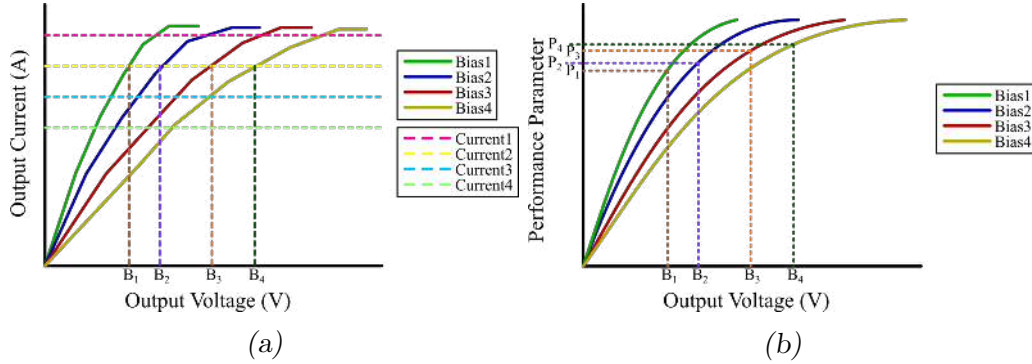


Fig. 5.5: Plot Showing the process of reading off the performance data for the target currents (a) On the RF-IV plot the voltage is read off where the target current intersects the different RF-IV lines. Using ‘Current1’ as an example, the various output voltages are noted (B1-B4) (b) The voltages (B1-B4) are then plotted on the performance plot and the performance for each point read off (P1 - P4)

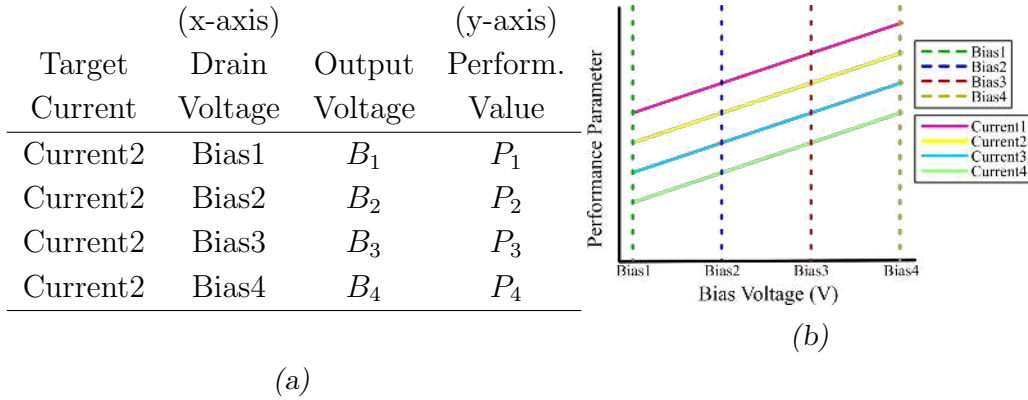


Fig. 5.6: Plot generated that shows how performance varies with bias. (a) Table showing the data that has been used to generate a single line. (b) The plot generated from combining multiple target currents into one plot.

This can then be repeated for various performance parameters, but an added step is required in that the desired parameter needs to be plotted

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against output voltage, as shown in figure 5.5(b). This then allows for the RF-IV plot to be lined up with the performance plot and the performance of each intersection between the target current and the RF-IV plot to be read off as shown in (b). Then like the knee walkout plot the performance parameter can then be plotted against the output DC bias.

This process can be split into the following steps:

1. Using the RF DLLs, plot the RF-IV, as shown in figure 5.3. This is done by plotting the ‘output knee voltage from DLL’ vs. ‘output knee current from DLLs’
2. Plot a similar graph to (1), but instead of plotting output voltage vs. output current, replace it with the performance parameter of choice (knee walkout, Power, Gain, etc.) given by the DLL for that data point. This process is shown in figure 5.4.
3. Now both the RF-IV plot and performance plots have been generated a selection of target currents can be chosen to evaluate how performance changes by targeting different currents. This is shown in figure 5.5(a) where it is seen that the output voltage is noted for every location the target current line intersects the RF-IV.
4. Now that an output voltage has been generated for each bias level tested, plot these voltages on the performance plot generated, as shown in figure 5.5(b). This will then allow the performance parameter to be read off for each bias point tested, allowing the table shown in figure 5.6(a) to be generated for each target current.
5. Finally, the data from each target current can be plotted to produce the final plot that has bias level plotted vs. performance and each line representing a target current, as shown in figure 5.6(b).

5.3 Fan Measurement Setup

This section will go over which system settings are used and why.

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5.3.1 Drive Level

As with most measurements, the first thing to do is find the optimum load at the desired drive level, which then will act as a constant parameter to allow for a meaningful comparison between results. How the optimum was found is covered in Chapter 3.4.2, but as mentioned these measurements use the input voltage as the constant value to allow comparison with the DC-IV. The power sweeps are shown in figure 5.7(a), where a GaN50's power was swept and then the different compression levels are shown with the corresponding peak input voltages in figure 5.7(b).

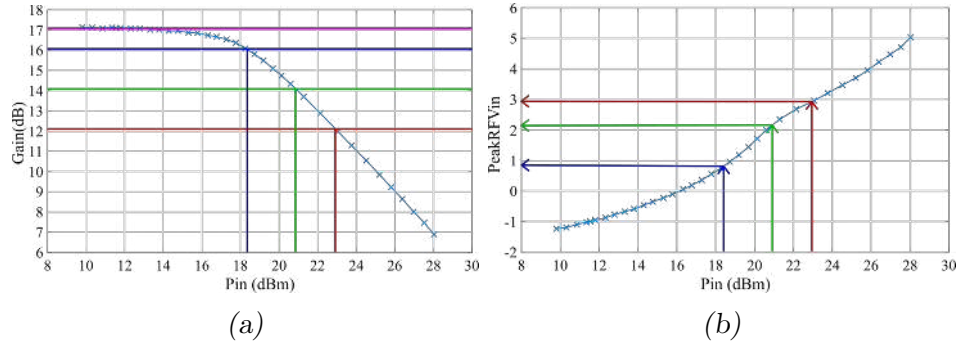


Fig. 5.7: The results from a power sweep showing the various compression points, blue = 1 dB, green = 3 dB and red = 7 dB (a) P_{IN} vs. Gain (b) P_{IN} vs. Peak RF voltage

These experiments compared 2 levels of compression, 1 dB, blue lines in figure 5.7, and 7 dB, red lines in figure 5.7. The 1 dB results will be used to represent the normal operating conditions, although the FET will be driven to 3 dB, only driving it to 1 dB allowed for direct comparison with the HBT. Then the other drive level is 7 dB which was determined experimentally by collecting measurements at different output bias levels to see how hard the devices needed to be driven before the knee effect would not decrease any further.

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5.3.2 Harmonic Impedances Shorted vs Combined with Fundamental

The difference between shorting the harmonics and keeping them at the same location as the fundamental is seen in figure 5.2, and real measurements shown in figure 5.8(a) and (b).

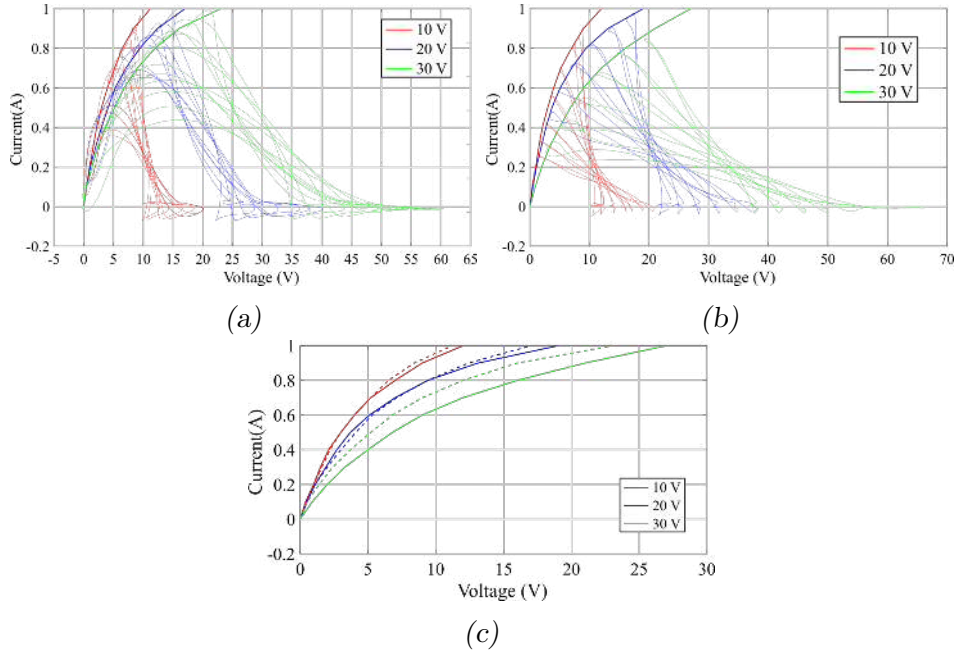
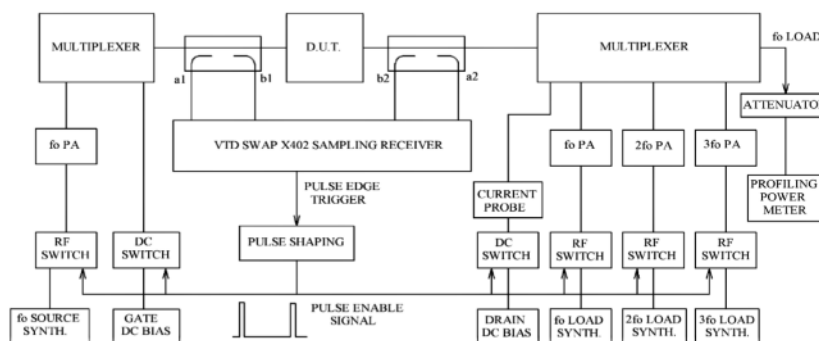


Fig. 5.8: A set of plots showing the difference between the different harmonic impedance locations (a) Harmonic impedances shorted (b) Harmonic impedances with the fundamental (c) Knee plot showing the difference

The looping effect is more prominent in (a), making it harder to know where the knee is. The knee lines have been added to each (a) and (b), then plotted together in (c), which shows while the 10 V and 20 V RF-IV plots match well between the two modes, the 30 V measurements do start to show a variance. There is now a trade-off between what method to use, as while it is clear combining the harmonics with the fundamental will give the more accurate knee, putting the harmonics where they will be at design time (in this case shorted for class B) will allow for the design performances

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5.3.3 Continuous Wave vs Pulsed RF



The pulse width of the system was 100 us and the duty cycle was 10%, leading to the drive signal shown in figure 5.10.

Fig. 5.10: An example of the pulsed signal used to drive the DUT

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For the pulsed measurements the RF was pulsed, but the DC was left on, due to the Class-AB (near Class B) bias point. When the RF is off the drain current is also reduced and gives the device time to cool down between pulses. The pulsed set up is more complicated than the CW set up, as shown in figure 2.8. Real world applications use modulated signals that are closer to a pulsed signal than a CW signal. Therefore, pulsed measurements are more representative of real world conditions. The results in figure 5.11 show a comparison of CW and pulsed results, where significant current compression is observed when using CW, which is to be expected due to the extra heat generated as the device is never off. Whereas under pulsed conditions, the device is off for the majority of the time, allowing the device to cool down.

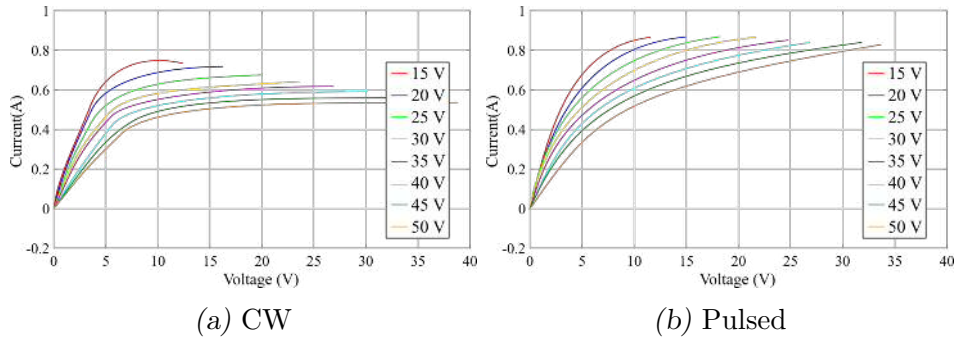


Fig. 5.11: An example of measured fan diagrams for the GaN50 GaN FET device (a) CW (b) Pulsed

The comparison shows the CW compressing heavily at the higher DC operating points, where the DC results do not go above 0.55 A/mm at 50 V the pulsed will operate over 0.8 A/mm. As there is such a difference in the results it was decided to only use pulsed for these measurements, allowing the devices to show how they would perform under modulated conditions.

5.3.4 HBT vs FET RF Knee

A comparison between the HBT and the FET device was done to examine if they both suffer from the same knee walkout effect, where the results are shown in figure 5.12 with the HBT in red and the FET in blue. It compares

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the lowest measured DC bias value of the FET that allowed the full current swing with the same from the HBT. Due to the difference in DC knee for each device, this was a different bias voltage for each device, but should show the best-case scenario for each.

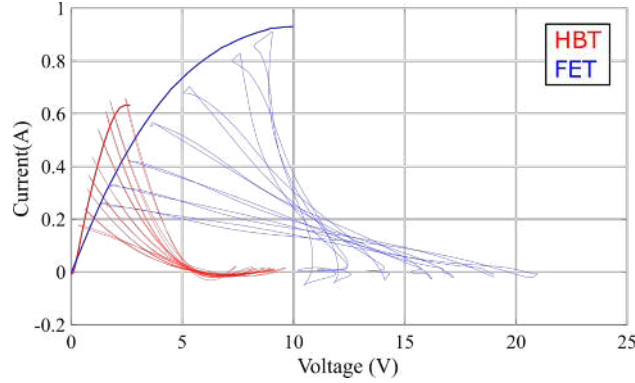


Fig. 5.12: A single RF-IV diagram done for the HBT and the FET devices, comparing the lowest value measured of each, with the HBT in red measured at $V_{cc} = 5$ V and the FET in blue measured at $V_{dd} = 10$ V

Looking at figure 5.12 the solid lines are measured DC-IV results, showing what is theoretically the best possible case, and the DLLs are shown to reveal any RF-DC dispersion and so allowing the comparison of both DC and RF. The first noticeable difference is the DC-IV results, which show the knee is worse for the FET when compared to the HBT. This shows a 1 V difference at the HBTs peak current. This is one of the reasons HBTs can perform better than FETs under normal operating conditions, and this gap would increase as the HBT targets higher currents. This will give the HBT an increasing performance advantage over FET devices at higher power applications, again showing the potential for these devices commercially in the base station space if the failures can be resolved. The other difference is the effect of the RF knee. With the FET device it is seen that the DLLs push up against the knee and start to flatten off, showing that the DC-IV is a hard limit. Note the RF knee is not as shallow as the DC-IV knee, leading to performance degradation for the FET. Whereas the HBT does not seem to have the same

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knee “walk out” effect, and even pushes through the DC-IV knee and does not show any signs of flattening off. This could be a result of the ineffective de-embedding for the more complex HBT device, but should be close to the actual results, showing a double win for the HBT technology. Not only is the DC knee shallower than its FET counterpart, the RF waveforms do not suffer from the same “knee walkout” effect. This shows the compromise between reliability and performance being made in the base station application space, having to sacrifice performance for a more rugged and reliable device that has performances limitations.

5.4 *GaN50 vs. GaN25HV at 1-dB compression*

This next section looks at comparing the two proposed GaN FET devices, the GaN50 and the GaN25HV. The first step is to draw a fan diagram for each device by sweeping the bias from 15 V to 50 V, shown in figure 5.13. It was formed by holding the harmonics with the fundamental as just the effects of the knee of the two devices are of interest in this section.

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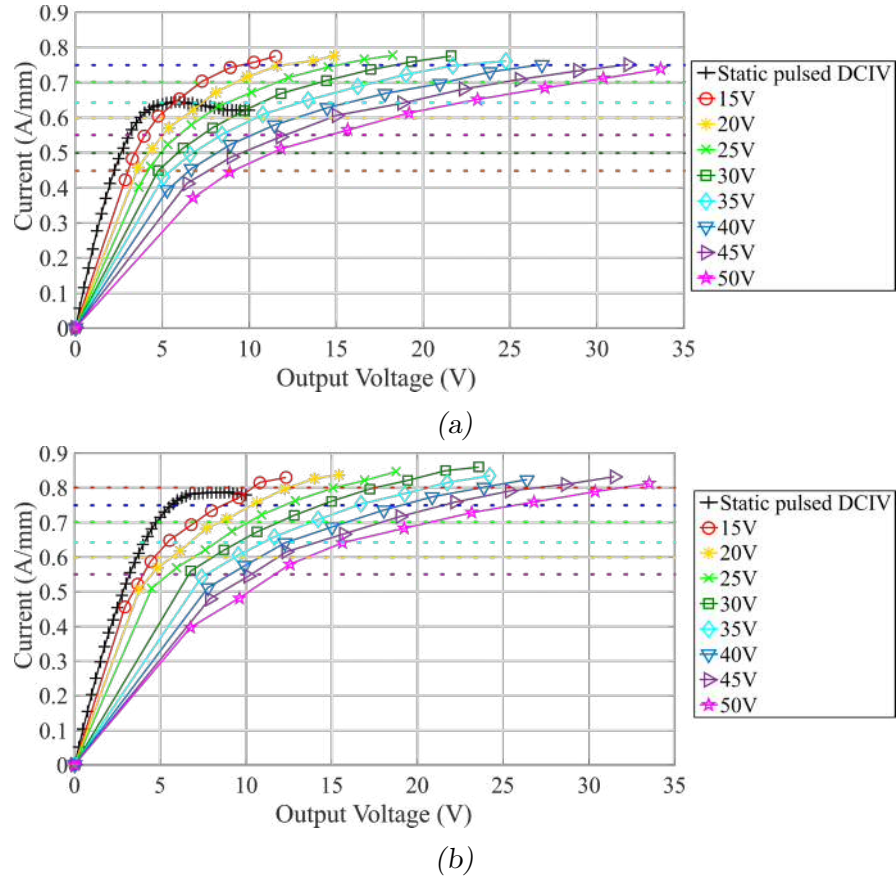


Fig. 5.13: RF-IV for the two devices with the horizontal dotted lines representing the target currents. (a) GaN25 (b) GaN50

The symbols on the plots represent an actual data point so only target currents within or very close to measured data were considered for this comparison. The currents are A/mm to allow a direct technology comparison, rather than a device comparison. Comparing figure 5.13(a) and (b) shows that the GaN50 outperforms the GaN25HV, able to achieve slightly higher current densities for a given output voltage, and is able to target 0.8 A/mm where the GaN25HV had compressed too much in the higher bias points.

The next step is to generate the performance data for the chosen target currents. Figure 5.14 shows an example of this using the GaN25HV plot

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from figure 5.13(a) using a target current of 0.65 A/mm.

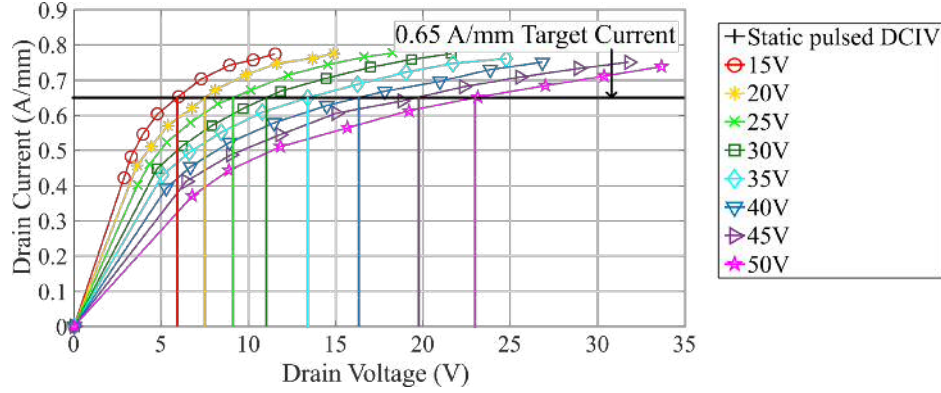


Fig. 5.14: An RF-IV from the GaN25HV with the target current drawn on and the output voltage noted

Next, taking drain efficiency as an example to plot the performance plot drain voltage vs. drain efficiency is plotted as shown in figure 5.15.

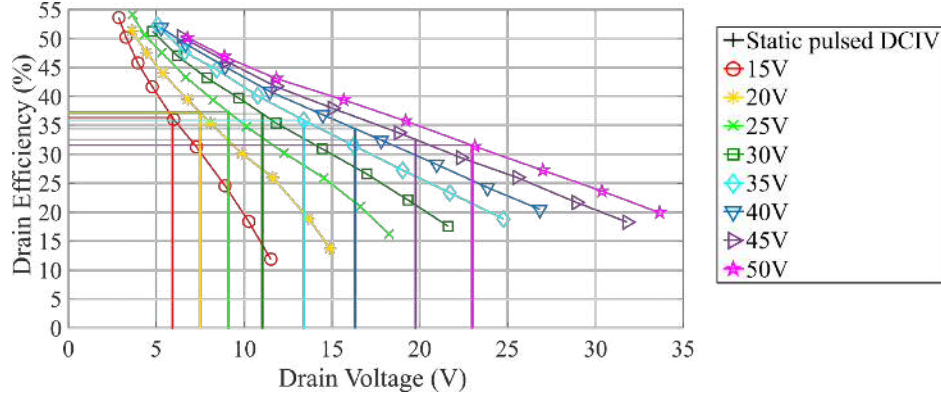


Fig. 5.15: Output voltage plotted against drain efficiency for the GaN25HV, with the output voltages noted in figure 5.14 marked in this plot to read off the performance information

The process shown in figure 5.14 and figure 5.15 is the same process shown in figure 5.5, but now with real data. First the target current is selected and has been marked on figure 5.14. Then where this current value intersects each

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RF-IV line the drain voltage is noted. This can then be read off directly from the x-axis to get the knee walkout for this chosen target current. In this case, how the drain efficiency changes with the knee walkout is of interest, so the efficiency values for each drain voltage are read off, seen in figure 5.15.

Finally, these values are plotted as shown in figure 5.16(d), and this is repeated for each target current to generate the multiple lines seen in the plot. This is a very labour-intensive process that, while it was aided by plotting programs and manipulating/interpolating tables of data rather than drawing lines on graphs, it needs to be improved to make these plots easier to generate. This process was then repeated for power and gain, and then for the GaN50, with all the results shown in figure 5.16. The GaN25HV is denoted by a star and GaN50 is denoted by the circle and the different colours are varying target currents.

Due to lack of time to develop a proper analysis tool, these plots are made from manual measurements and so a verification plot is required to show this method of plotting works. Looking firstly at figure 5.16(b) it is seen that the power in watts has been plotted. Due to the physical nature of the device the power plot should pass through (0,0). This was used to check the data being plotted was accurate, hence the plots have been extended with dotted lines back through the origin to see how well the line fits. In the case of targeting the lower currents it seems to fit very well, but there is a discontinuity noticed between the dotted and solid lines for the higher target currents, showing a slight offset from the results. Mostly there is a good match here between the ideal (dashed line) and measured (solid line) showing that this method of plotting is working as expected.

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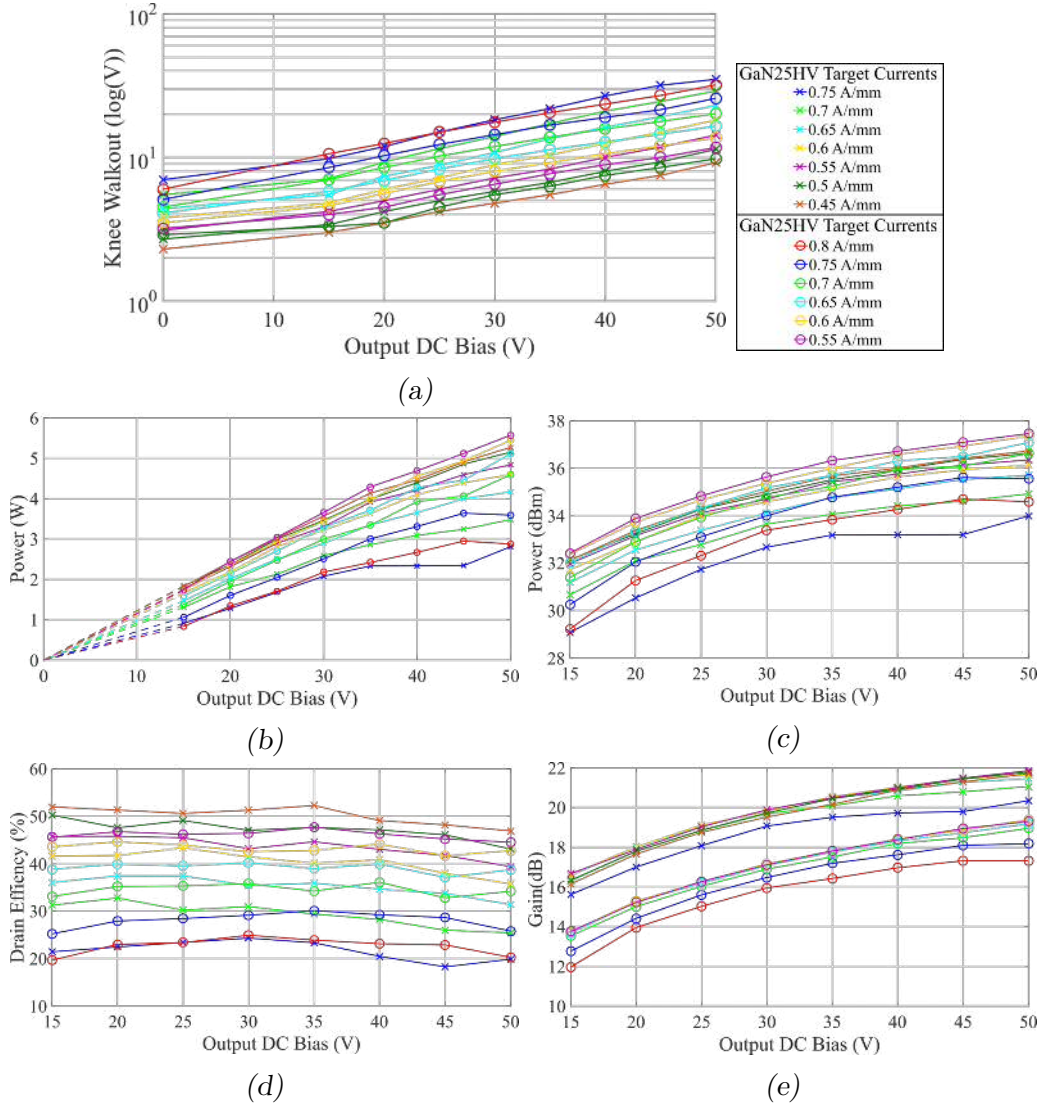


Fig. 5.16: The performance plots looking at the effects of knee walkout as the bias is increased, comparing the GaN25HV and GaN50 devices (a) Knee Walkout vs. Output Bias (b) Output power in Watts vs. Output Bias (c) Output power in dBm vs Output Bias (d) Drain efficiency vs. Output Bias (e) Gain vs. Output Bias

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Next looking at figure 5.16(a), the knee walkout is shown vs. DC bias, using 0 V to represent the static knee, and with the y-axis plotted as log, showing an exponential relationship between the knee of these devices and the bias conditions. This logarithmic relationship is slightly offset by the static knee measurement. Although this is not a problem as the static knee value was only added to this plot as a reference and is not an RF result for Bias = 0 V. This shows that if the knee keeps walking out exponentially as the bias voltage increases, the knee will eventually be “walking” out faster than any increase in bias could compensate for, hence leading to a reduction in performance, making using the device above this bias point undesirable. Looking especially at the GaN25HV results in figure 5.16(a) it is seen that the GaN25HV also suffers from worse knee walkout for any given target current, with the difference increasing as higher currents are targeted. However, for the lower target currents there is very little difference.

This decreasing performance return with increasing drain voltage due to knee walkout is shown clearly in figure 5.16(c) where power in dBm is plotted and is seen to be saturating with increasing drain bias, especially the higher target currents where the power seems to be fully saturated and even in decline for the GaN50 at 0.8 A and 0.75 A target currents. If time had allowed further investigation at higher bias levels, it is expected that the power would start to decrease with increasing levels of output bias. This decreasing performance gives an optimum operating bias that could be used if the physical limits of the device allow it. It should also be noticed that targeting higher currents did not yield higher output power, due to the trade-off between voltage and current, but this is partly due to the harmonics being held at the same location as the fundamental. If the voltage was able to move back down the knee, as is the case for shorting the harmonics, this voltage swing would have remained constant. This result of not gaining power from targeting higher currents shows the effect of the GaN FET knee, that will require high levels of compression or specific harmonic termination to make full use of the power capabilities of the device.

Next looking at the efficiency in figure 5.16(d), it follows that the device with higher power density/mm and reduced knee will also provide higher

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efficiencies for a given target current, which is the GaN50. Again, the higher target currents produce lower efficiencies because of the reduction in output RF voltage and increase in DC current from targeting higher currents. For the results targeting lower RF currents the efficiency is reducing with increasing output bias, but for the results targeting higher target currents the peak efficiency for both devices occur around 30 V. If efficiency was the only concern, this would mean running it at a lower DC bias and so achieving a lower output power.

The final parameter to be looked at is gain, in figure 5.16(e), where the GaN25HV is clearly the better device as the worst result for the GaN25HV is better than the GaN50's best result. This shows that gain is not totally dependent on knee, and is more dependent on the device technology, but the gain does compress with power.

5.5 Using Fan Diagrams to Compare GaN50/GaN25HV at 7-dB Compression

A further test was done at 7dB compression, to see how the knee would change as the compression level increased. The knee fan diagram for this is shown in figure 5.17, where this time the harmonics were shorted to look at device performance in class B.

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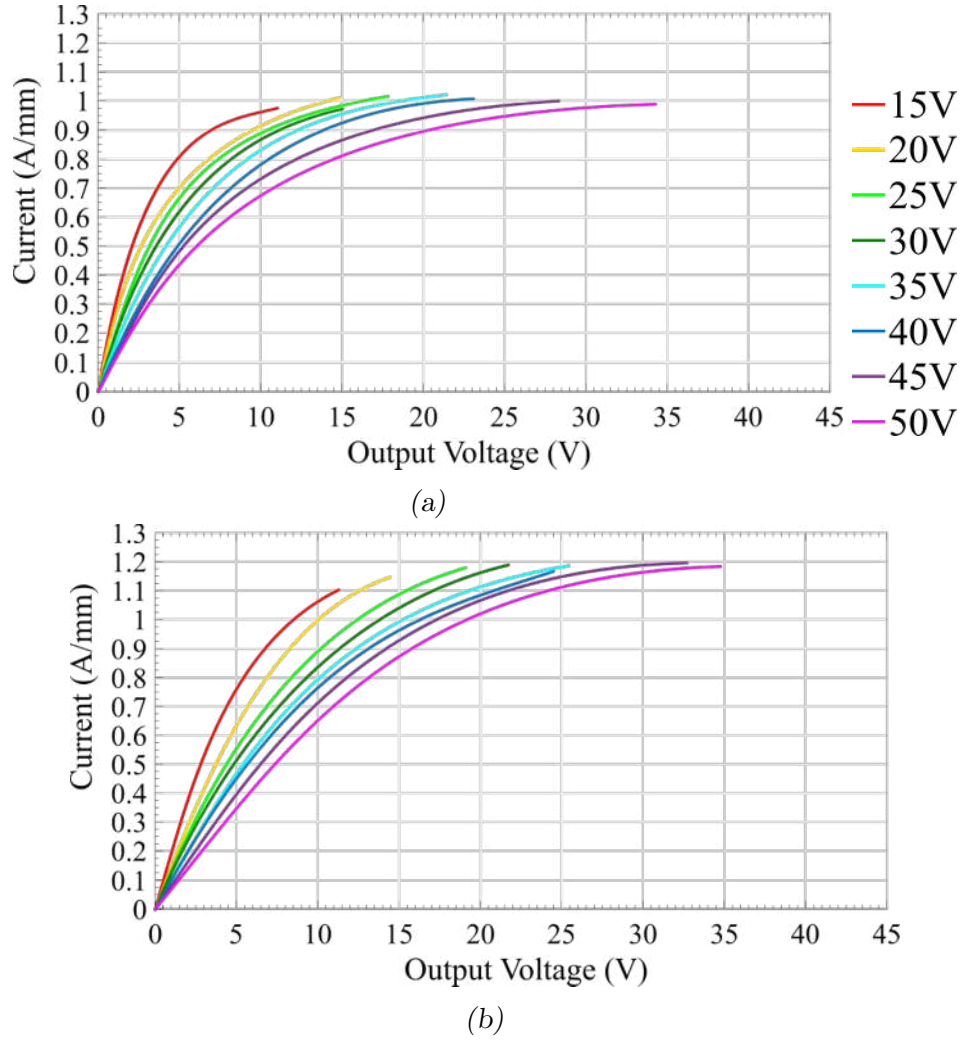


Fig. 5.17: The knee plot when the devices were pushed 7 dB into compression a) GaN25HV b) GaN50

Due to the looping nature of shorting the harmonics and trying to pinpoint the knee within the loops, especially at higher bias levels, lines were plotted and adjusted manually to find the average. This made plotting the performance for any given walkout especially hard as now a waveform covered an entire section of the knee instead of just one point, so the process was more manual, hence less robust, than the last set of plots, often using an

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approximate “by sight” fitting process to deal with the looping and form the RF-IV.

Although, even if the absolute values may contain absolute error, relative comparisons can still be made between the 1 dB results, and each of the two devices. Looking at the relative difference between the results shown in figure 5.17 and figure 5.13 shows that both devices obtain higher current/mm, which means for a given target current the knee has been reduced. The knee at 0.75 A/mm and 50 V bias is 12.5 V walkout for the GaN25 and 12 V for the GaN50. These results show, as before, that the GaN25HV’s current starts to compress before the GaN50, but the knee is similar and even better in places. But due to the higher power densities available with the higher current densities puts the GAN50 device at an advantage over the GaN25HV device.

Only one target current was evaluated for these results, 0.75 A/mm to allow comparison to the results performed under 1 dB compression, with the results of the 7 dB compression seen in figure 5.18.

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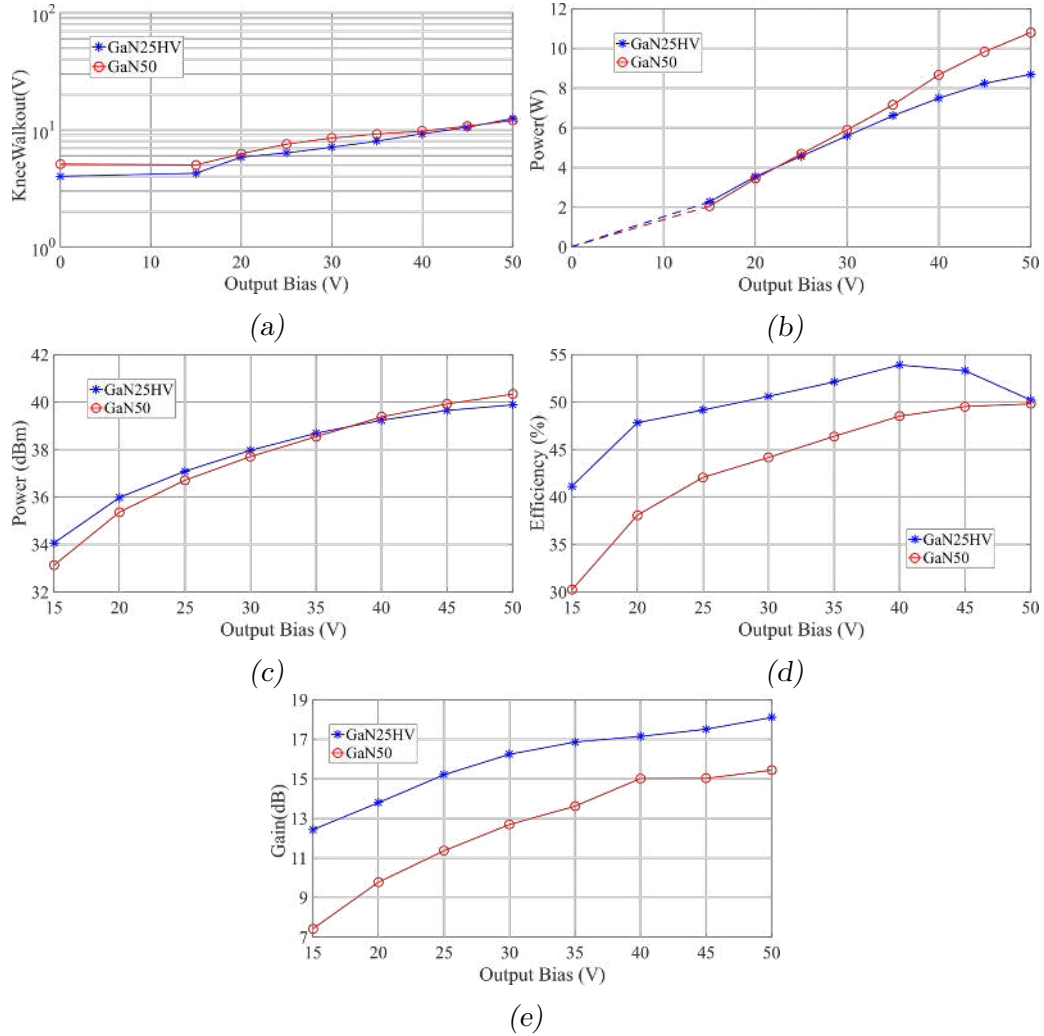


Fig. 5.18: Device performance plotted against bias, generated from the 7 dB compressed RF-IV plots (a) knee walkout vs. bias (b) Output power in watts vs. bias (c) Output power in dBm vs bias (d) Drain efficiency vs. bias (e) Gain vs. bias

Firstly, checking to see if the measurements are still valid, looking at figure 5.18(b) it is seen that the interpolated lines (dotted) are offset from the measured ones (solid), showing the effects of the fuzzy edge that shorting the harmonics gives, but they are still usable results showing the right trends

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and compression levels.

The improvement in knee for both devices is shown in figure 5.17(a), where it is seen that the GaN25HV gains an advantage over the GaN50 for lower bias points and only performs worse at 50 V. Comparing this back to the 1 dB plot, in figure 5.16 it is seen that the rate at which the knee walks out now has decreased also, and this time the devices push very close to the DC knee, almost drawing level with them.

This improvement in knee is reflected in the power and efficiency plots, seen in (c) and (d), as the GaN25HV now has a higher efficiency than the GaN50, and performs better than the GaN50 for output power until 40 V where the GaN25HV starts to compress, and the GaN50's higher current density allows it to outperform the GaN25HV.

The gain of the GaN25HV is still much higher than the GaN50, significantly outperforming it again, as seen in (e).

These results are with the harmonics shorted and so better represent what to expect from the device during a design, which shows that at these high compression levels the GaN25HV device wins some very key points with improvements in efficiency over the GaN50 device, and maintains its advantage in gain, and so only losing out in power density. As linearity becomes less important these changes with compression will become more and more relevant.

5.6 Conclusions

This chapter's aim was to analyse two different GaN FET devices by looking at the effects of knee walkout on performance. In part to look for the bias level that gives the best compromise in performance, but the main aim was to compare these two devices with an aim to perform a Continuous Class B design on the best performing device.

After performing the analysis on both devices, it is seen that they both have strengths. The GaN50 performs well at low compression levels, and the GaN25HV at high compression levels, but the GaN50 also has higher current density and so higher power density. The higher power density allowed

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the GaN50 to meet the 10 W/mm target for these technologies, whereas the GaN25HV fell short of this performance target. If power is the critical requirement then the GaN50 is the best choice. However, if efficiency is a key requirement then the drive level needs to be considered, which is often determined by the Digital Predistortion (DPD), or other linearising technology that is available. For this project having 10 W/mm power density and good performance at lower compression levels makes the GaN50 the best choice, and so was the device taken forward into the designs to follow.

Another result of this work was the novel way the data from the fan diagram was manipulated to allow the effects of DC-RF dispersion to be analysed. While in this case it was used to compare two competing devices, it could be used more widely to help designers get the best out of their devices, or device makers better understand how well their devices perform.

6

Design of a Continuous Class B Quasi MMIC

6.1 Introduction

This chapter is the first of two design chapters which uses a variation of the GaN50 10 W tested in Chapter 5, the GaN50 20 W. The technology was chosen for reliability over the HBT and for having higher current density than the GaN25HV process. This chapter starts with Continuous Class B design theory, then progresses to a simulated design on laminate as proof of concept, then moved it into a MMIC design space to show the challenges involved with this and then finally into a quasi MMIC design that was fabricated.

The theory section will also look at the circuit topology that was used to achieve the Continuous Class B impedances. Simulations were then executed, presenting ideal impedances to the model to show the absolute best performance that should be expected from this device. The chosen circuit topology was then applied to the GaN50 model and tuned to show what a traditional laminate build would produce. Finally, the last section will look at the specific challenges that were faced during the MMIC phase of the design and then the final results.

MMICs are a much more desirable end point for commercial designs as they are a lot more compact than laminates, also allowing for integrated designs, which reduce losses in the overall system. To reduce cost, this project targets a quasi MMIC where the main device is a GaN chip and the matching is done on a GaAs substrate and then these elements are wire bonded together, as seen in figure 6.16. This is comparable to a full MMIC and so the performance achieved is expected to be comparable to a full MMIC design.

The simulated performance achieved for the MMIC optimised design with

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ideal components was comparable to the laminate simulation results, which given the move away from the ideal impedance locations was an unexpected, but good, result. Then simulating with real MMIC components shows a steep drop in performance such that it then struggled to meet the performance specification.

Finally, the devices were measured, but the performance was much lower than the simulated performance. This is likely due to the measurements being done under CW in the absence of the hardware required to do pulsed measurements, meaning the heat the 20 W device is producing in such a small area likely causing significant thermal compression. While CW characterisations can still give valid results, it needs to have sufficient cooling applied which was not available for these tests. However, under pulse like modulated signals, the device is only operating over very short pulse width and do not produce as much heat and provides the device time to cool down in-between pulses, so it is expected that the performance would be significantly improved, both in terms of power and efficiency.

6.2 *Circuit Topology*

This section uses the Continuous Class B theory to pick an ideal circuit topology using ideal components that will achieve the desired impedance locations.

6.2.1 *Continuous Class B Continuum*

Continuous Class B continuum is a range of impedance locations that all give the same power and efficiency output despite moving away from the ideal Class B locations. It is achieved by the second harmonic impedance being tuned as the fundamental is moved away from the optimum. This causes voltage peaking and allows performance to remain the same. The impedance space and corresponding waveforms are shown in Figure 6.1.

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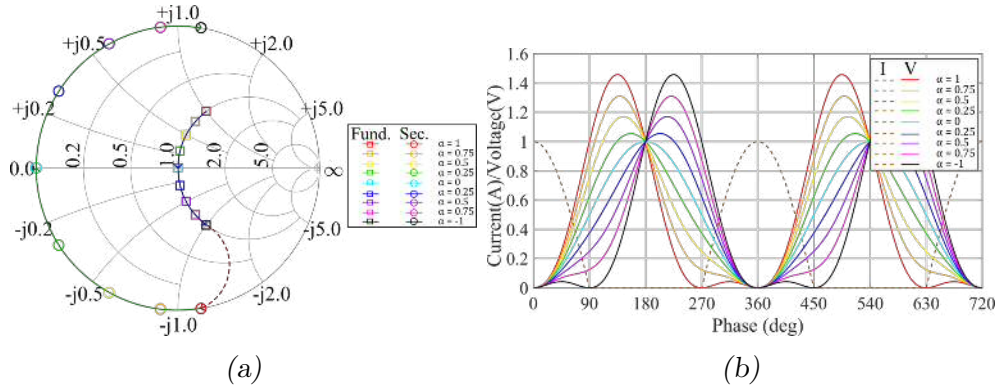


Fig. 6.1: Continuous Class B (a) Impedance space (b) Waveforms

Looking first at the impedances shown in figure 6.1(a), the load trajectory moves around the circle of constant real impedance and passes through the ideal Class B location. It then goes onto the second harmonic which follows a mirror trajectory, but this time it moves around a $\Gamma = 1$ circle. This means that the system is inherently band limited as above one octave there are frequencies where it needs to be both fundamental and a second harmonic and occupy two different impedance locations, which with passive networks is not possible. Looking at the target frequencies for this design; fundamental: 1.7-2.7 GHz and second 3.4-5.4GHz, there are no overlapping frequencies and even has a band (2.71-3.39 GHz) that will form the red dotted line joining the end of the fundamental impedance location to the start of the second in (a). Looking at a different example with fundamental of 1-3 GHz, and second of 2-6 GHz, shows that the frequencies 2-3 GHz are in both fundamental and second harmonics, meaning that as both conditions cannot be satisfied, either the fundamental or second harmonic tuning will need to be sacrificed.

Looking now at figure 6.1(b) shows the current and voltage waveforms generated by the ideal impedances, with each line colour matching the impedance pair for the voltage. The current is seen to be a half rectified sinusoidal wave generated by the classical Class B bias point for all locations and is shown by the dotted line. When the second harmonic is shorted for classical Class B, the voltage wave is sinusoidal and 180° out of phase with the current. But then when moving the fundamental away from this ‘ideal’ location would

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normally mean a reduction in efficiency/power, due to the reduction in the phase difference between the current and voltage and increased overlap between them. However, by tuning the second harmonic as the fundamental is moved away from the ideal the voltage is seen to peak and so compensate for the change in phase offset between the fundamental and second harmonic. This then allows the power and efficiency to remain the same across this impedance space while the fundamental and second harmonic are appropriately matched.

6.2.2 Ideal Circuit Topology

To realise these ideal impedances, the circuit topology shown in figure 6.2 was used, looking at each section in turn.

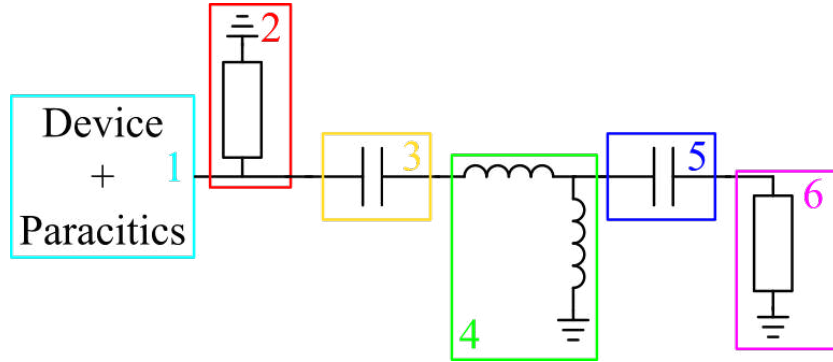


Fig. 6.2: Ideal circuit topology used to present ideal Continuous Class B impedances

Section 1 is just the device model, which when doing ideal analysis on this topology would consist of a current generator and a parallel capacitor to represent C_{ds} . Alternatively, this could be replaced by a full device model. At the other end section 6 is the output load, which is often $50\ \Omega$ and was for this design. Section 5 is combined with section 4 to form a filter network that does broadband match for the fundamental, where it will resonate out the parallel C_{ds} . The two inductors shown in section 4 are the core of this matching network, they enable the matching of a broadband load and transform the impedance down depending on how they are configured.

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To show the function of the inductors in section 4 and what they are doing, an example using two circuits, each with a different configuration, is shown in figure 6.3 were simulated.

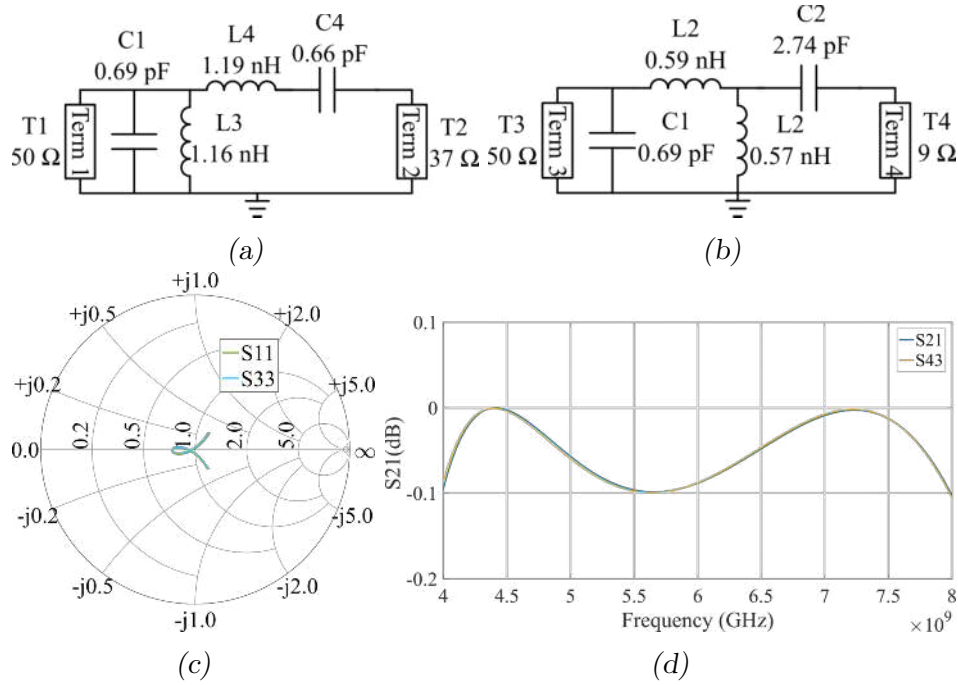


Fig. 6.3: An example showing how the inductors in section 4 of figure 6.2 works (a) Topology 1 with the inductors ordered shunt/series (b) Topology 2 with the inductors ordered series/shunt (c) S11 performance of each topology (d) S21 performance of each topology

In figure 6.3(a) the parallel inductor is closest to T1 and in (b) the series inductor is closest to T3. The results show that both topologies can achieve similar match performance, but the topology shown in (b) is also able to impedance match down much lower than (a). Also, in (a) and (b) it can be seen that the topologies are capable of matching the impedances well over a wide bandwidth, 4-8 GHz shown in (d). Unfortunately, the Continuous Class B design does not want the impedance of all frequencies to be matched to the same location. The second harmonic impedance needs to be matched

6. DESIGN OF A CONTINUOUS CLASS B QUASI MMIC

along the $\Gamma = 1$ circle. This is achieved by section 2 of figure 6.5, a line whose length is set to present a short to the middle of the second harmonic band pulls the second harmonic around to the short rather than staying close to the fundamental. Comparing the topologies shown in figure 6.3(a) and (b) to that shown in figure 6.5 it is seen that a parallel capacitor is missing, this is because it is embedded within the device model as C_{ds} .

For the topologies shown in figure 6.3(a) and figure 6.3(b) the DC can enter by the parallel inductor and then the series capacitor will act as a DC block, but now that the line has been added, which was used to feed the DC in another capacitor needs to be added between the line and the inductor to stop the current flowing out through the inductor, shown by section 3 in figure 6.2.

Putting all this together was the starting point of this design, and tuning for performance is what lead to the final design.

6.3 *Simulated Ideal Results*

The first step is to analyse the GaN50 20 W, which would normally be done with physical measurements as in previous chapters, but as this device was not available to measure, so equivalent simulations were done instead. To do this a load pull schematic was made in ADS, as shown in figure 6.4, that shows a custom tuneable source and load that allows for up to ten harmonic load and source pull, although only the first three loads are of interest.

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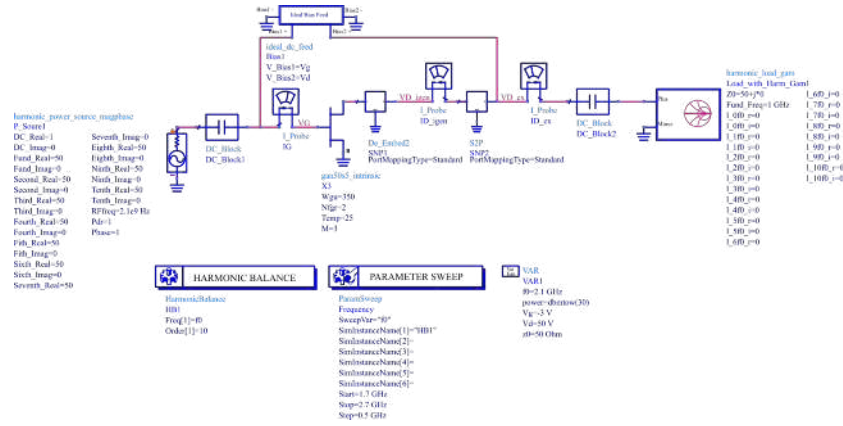


Fig. 6.4: An example of the load pull circuit used in ADS.

Any de-embedding back down to the intrinsic i-gen plane was done using the paired “de-embed” and “s2p” blocks within ADS which both hold the same file. To generate the s2p files a modified version of the Qorvo model was produced (as a fully open model was provided) that allowed most of the parasitic elements to be simulated as an s2p file, this then allows the de-embedding done in the simulator to be replicated on any measurement system. The transistor is a model Qorvo sent, that can be scaled to be any of their GaN50 devices and is set appropriately for the 20 W version this design is using. The DC sweeps and measurements are done in the ideal bias feed, with any other sweeps being done with a parameter sweep block, which can be stacked up, often sweeping, frequency, drive and real and imaginary parts of loads, which is all simulated using a harmonic balance simulation tool.

First a DC sweep generated the DC-IVs, and then a load pull sweep was performed with power and fundamental load swept at 2.2 GHz, as this is the centre frequency, with all other loads shorted. This allowed the DC-IV plot to be overplayed by optimum waveform DLL, and plot the power and efficiency contours, as shown in figure 6.5.

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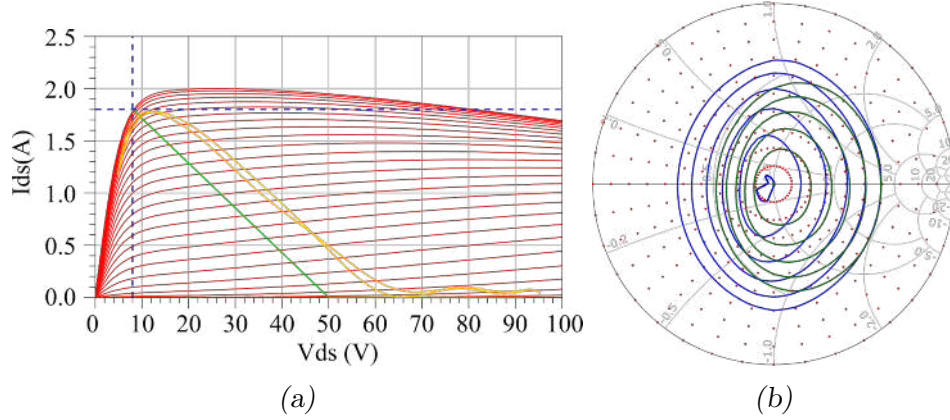


Fig. 6.5: Simulation results from sweeping the DC and fundamental load (a) DC-IV showing the DC curves and the de-embedded DLL of the optimum at 3 dB compression (b) Smith Chart showing all swept fundamental loads with de-embedded power and drain efficiency contours plotted

Looking first at the DC-IV results in figure 6.5(a), the ideal Class B load line have been overlaid onto it in solid green, and then the DLL of the 3 dB compressed waveform has also been overlaid in yellow. To find the ideal predicted power, efficiency and target impedance of this device, the ideal Class B load line was used. Starting with the output RF power, modifying equation 2.44 for use by a non-ideal Class B gives equation 6.1.

$$P_{RF} = \frac{(V_{DC} - V_{Knee})I_{MAX}}{4} = \frac{42 \times 1.8}{4} = 18.9 \text{ W} \quad (6.1)$$

Next finding the efficiency, using equation 2.37, is shown in equation 6.2.

$$\eta = \frac{P_{OUT_RF}}{P_{OUT_DC}} = \frac{18.950}{\pi} = 65.97 \quad (6.2)$$

Then finally the optimum load is found using equation 2.41 and seen in equation 6.3.

$$Z = \frac{V}{I} = \frac{84}{1.8} = 46.6 \quad (6.3)$$

This shows the output power would be ideally just below 20 W with

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no compression, but then comparing this to the simulated result, shown in table 6.1 (location 3 at 2.2 GHz), it is 43.6 dBm so a jump up to 22 W which is caused by the extra voltage swing gained from pushing the device into compression. Next comparing the efficiency shows that this increase in compression and move away from the ideal world has gained power but lowered efficiency, which is now down to 57.8% from 65.97%. This loss will also be caused by the bias point changing from ideal Class B in figure 6.5 to Class AB in table 6.1 to match with Qorvo's operating point. This is a steep drop in performance and puts the simulated results below the targeted specification. Next, looking at figure 6.5(b) and equation (6.3) both measured and simulated impedances are ideal for broadband design as they are near the standard $50\ \Omega$ that the next stage in the communications chain will likely present. The ideal load pull simulations predicts it to be 46.7% at $50\ \Omega$, with the efficiency favouring a slightly higher impedance, as this will give a larger voltage swing with lower DC current, comparable to what was observed when measuring the knee. With 20 W being the lower limit for output power and the optimum for power being $50\ \Omega$ this location was taken forward.

The next step is to investigate the Continuous Class B space around the ideal Class B impedance. This was done using a modified impedance sweep shown in figure 6.6(a), where the fundamental was swept around the circle of constant impedance for $50\ \Omega$ and the second harmonic was swept around the $\Gamma = 1$ circle. The bias was also changed at this point to represent the Class AB bias that Qorvo expected the device to operate at, and so a slight drop in efficiency is seen from the ideal, as has already been noted. Once this was done, five locations were chosen to see if the ideal Continuous Class B waveforms were being achieved along with its performance. Points 1 and 5 are set just beyond $\alpha = 1$ and so show how the performance is affected beyond the ideal limits, points 2 and 4 are within the Continuous Class B regime and should conform to the ideal waveforms and performance and finally point 3 represents Class B. All the results are shown in Table 6.1.

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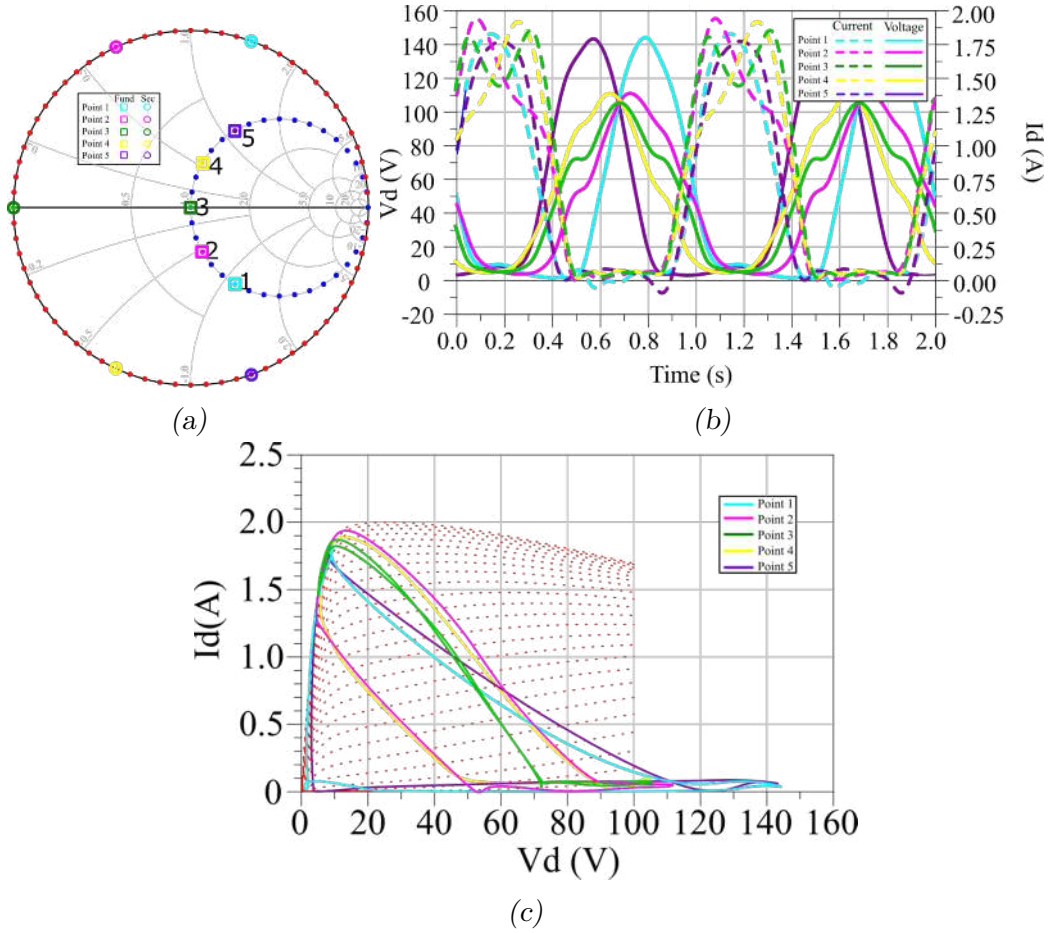


Fig. 6.6: The results from the Continuous Class B simulations, that used both the Qorvo de-embedding files and the de-embedding capacitor (a) Ideal impedance locations presented (b) Voltage and current waveforms at each point (c) DLLs at each point

The ideal theory states that the current should remain the same and the voltage will peak symmetrically about point 3, but looking at the waveforms in figure 6.6(b) it is seen that current is not the same each time. This is due to the increased compression level, which causes the DLL to push into the knee, which is seen more clearly in (c). The DLL push into the knee at different angles depending on the fundamental offset from the real axis,

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causing it to have a similar symmetrical offset around the centre. The voltage shows that the desired peaking effect has occurred, although it is not until the impedances moves outside the $\alpha = 1$ space with points 1 and 5 that the voltage shows a more dramatic change.

For each impedance pair the frequency was swept over three points, as shown in table 6.1, this shows how well the de-embedding is moving the reference plane down to the intrinsic i-gen. A shift in performance with frequency is caused by the imperfect de-embedding. Impedance location 3 is where the ideal Class AB impedance is presented and so can be used as a base line to compare the other impedances to.

Looking at points 2 and 4, the power is held reasonably constant with a slight drop off in both directions but looking at the efficiency it is seen that while there is not a huge difference there is an asymmetrical change, where point 2 increases in efficiency slightly and point 4 decreases in efficiency slightly. This is a symptom of the de-embedding and shows there is another reactive component that favours a slightly capacitive reactance to be presented to the device. This issue will likely be taken care of by tuning/optimising as the impedances will naturally move into the areas of highest performance which is the Continuous Class B space for this bandwidth. This will allow the impedances presented to the real intrinsic i-gen plane to be close to ideal without needing perfect de-embedding. The reverse is seen with the gain, but it favours an inductive load rather than a capacitive one. As frequency is increased all the parameters drop, even after driving the device harder to compensate for the loss of gain, showing the increasing impact of parasitics on performance as frequency is increased.

6. DESIGN OF A CONTINUOUS CLASS B QUASI MMIC

Tab. 6.1: 3dB simulation data

Location (Figure 6.6)	Freq. (GHz)	P_{OUT} (dBm)	η (%)	P_{DRIVE} (dBm)	G_{AV} (dB)	P_{IN} (dBm)	G_{MAG} (dB)
1	1.7	43.11	69	28	15.11	25	18.12
1	2.2	43.11	69.14	30	13.11	26.7	16.4
1	2.7	43	69	31	12.1	27.2	16
2	1.7	43.4	59.6	27	16.4	22.61	20.826
2	2.2	43.3	59.7	28	15.3	23	20.2
2	2.7	43.4	59.4	30	13.4	24.8	18.4
3	1.7	43.8	58.1	27	16.8	20.7	23.1
3	2.2	43.6	57.8	28	15.6	21.2	22.4
3	2.7	43.4	57.4	29	14.4	21.8	21.67
4	1.7	43.33	58	26	17.3	12.612	30.713
4	2.2	43.3	57	28	15.3	15.1	27.6
4	2.7	43.2	56.6	29	14.2	16.6	26.6
5	1.7	43.1	65.7	27	16.1	19.3	23.8
5	2.2	43.1	65.3	29	14.1	20.1	23
5	2.7	43.1	65.5	31	12.1	18.3	24.8

Points 1 and 5 present some surprising results, as firstly they show a large increase in peak voltage but a reduction in peak current which is most clearly seen in figure 6.6(c), which does lead to a slight drop in power performance compared to the Continuous Class B space, but an increase in efficiency. Looking at the shape of the DLL, it shows that the bias current will be lower than the Class B point and this will be partially responsible for the increase in efficiency, with the same asymmetric results shown in point 1 and point 5, with point 1 performing better. The waveforms are not what is expected from Continuous Class B as the impedances are outside the Continuous Class B design space, and while it would be beneficial to the design to extend the impedance space into it, as the design progressed it became clear that reaching these targets was not achievable as it meant stretching out the impedances to levels beyond the capabilities of this network.

6. DESIGN OF A CONTINUOUS CLASS B QUASI MMIC

Looking at the results of points 2, 3 and 4 give a good impedance space to work over that should allow for a broadband design to be achieved. So now the next step is to apply the circuit topology and tune it to meet these impedances. Figure 6.7 shows the target trajectory for the fundamental and second harmonics. Figure 6.7 shows the target trajectory for the fundamental and second harmonics.

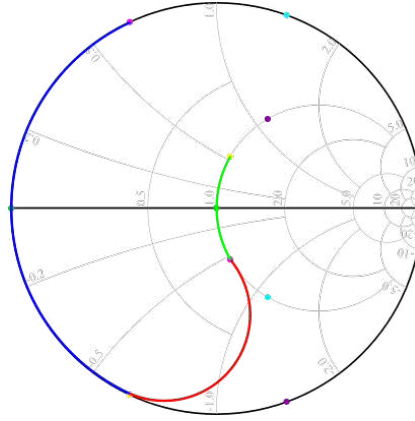


Fig. 6.7: The ideal trajectory for each impedance, green - fund 1.7-2.7, blue = second 3.4-5.4 and red is the movement between harmonics 2.8-3.3

6.4 Ideal Design

After identifying the ideal impedances, the next task was to simulate a version of the topology using ideal components, shown in figure 6.2 and values in figure 6.3, this was then tuned to operate over the frequency space of interest with this device's C_{ds} . This early version of the circuit was using components available to laminate designs, as Cardiff has experience in this space and is what this topology was designed for. To do this, the modified Qorvo model was attached directly to the output of the ideal matching network, shown in figure 6.8. Allowing the impedances close to the current generator to be observed, although as is seen from previous results this de-embedding is not perfect.

6. DESIGN OF A CONTINUOUS CLASS B QUASI MMIC

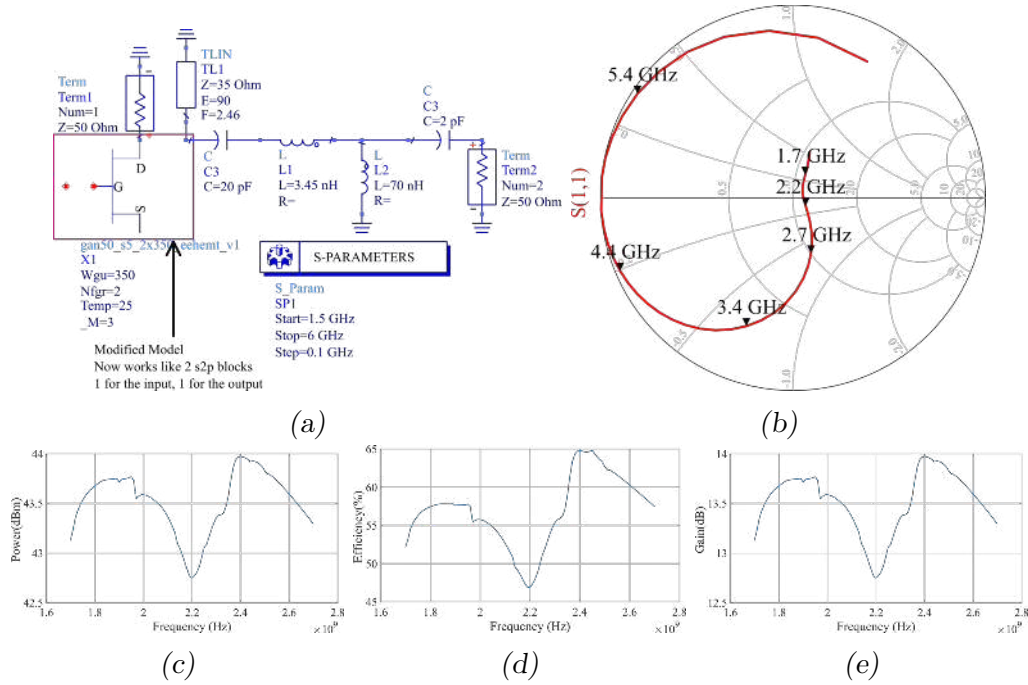


Fig. 6.8: Simulations of the design using ideal components (a) ADS schematic used to simulate S-parameters (b) Results from S-Parameters simulations (c) Power results from the harmonic balance simulation (d) Efficiency results from the harmonic balance simulations (e) Gain results from the harmonic balance simulation

Simulating this circuit gives the results shown in Figure 6.8(b), where the right impedance trajectory is seen, with the fundamental impedance following a constant resistance circle and the second harmonic touching the short. But it is also observed that the second harmonic impedances are all slightly removed from their ideal locations. This is due to the fundamental being given priority over the second harmonic while tuning. This was done because previous work has shown that the location of the second harmonic does not need to be fixed but can occupy an area [57]. Looking at the trajectory of the impedances it is also clear why targeting the impedance points just outside the $\alpha = 1$ space is not a feasible option with this circuit topology, as with the upper band already the least well matched, trying to

6. DESIGN OF A CONTINUOUS CLASS B QUASI MMIC

expand this out further caused a loss in performance, not a gain.

This circuit was then placed at the output of the model and then a full harmonic balance simulation was performed, using a circuit comparable to the one shown in figure 6.9, and the results shown in figure 6.8(c), figure 6.8(d) and figure 6.8(e).

The simulation results show that the efficiency performance was lower than the specification expectations for the majority of the frequency band only exceeding the desired value after 2.35 GHz, the power specification is met for all but a small bandwidth around 2.2 GHz and the gain mirrors the output power.

This circuit was then re-tuned seeking to optimise the performance of the circuit and the results are seen in figure 6.9, where the new circuit values are shown in figure 6.9(a) and the impedances are shown in (b) and the results in (c), (d) and (e). The results of tuning the circuit has improved the performance notably, with the power now exceeding the specification, the efficiency has inverted the frequencies it meets the specification, now being over 60% for all frequencies below 2.38 GHz, and does not drop as low as the previous design, showing improvement here too. The gain also sees an increase, although this is likely due to also having to re-tune the simple PI input network to level the drive power across the band and make sure it is 3 dB compressed at all frequencies. Although looking at the impedances in figure 6.9(b) they have been moved dramatically away from where the optimum locations say they should be. But it should be noted that the fundamental and second harmonics are always on opposite sides of the Smith Chart. With the performance improved and the circuit tuned this design was taken forward to the next stage of design of the MMIC.

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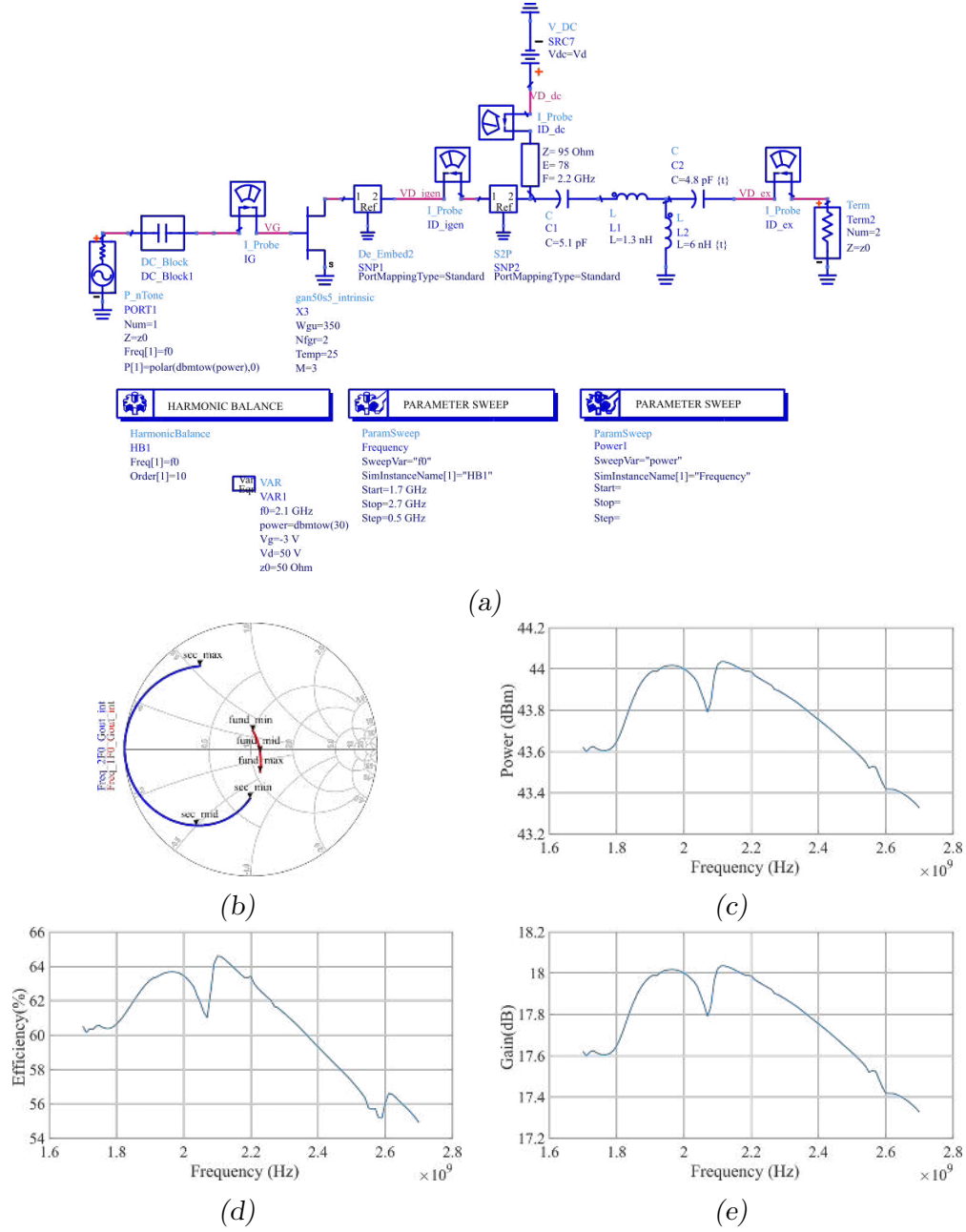


Fig. 6.9: Post performance tuning HB simulations of the ideal design (a) ADS schematic used to simulate harmonic balance (b) Re-tuned impedances from harmonic balance simulations (c) Output power (d) Drain efficiency (e) Gain

6. DESIGN OF A CONTINUOUS CLASS B QUASI MMIC

6.5 *MMIC design*

6.5.1 *Ideal MMIC design*

This section shows the transfer process of the ideal design into a MMIC design, which meant removing the line and replacing it with an inductor.

Once the substrate PDK for the matching networks was supplied, it was determined that the maximum component size was around 10 nH and 10 pF for the inductor and capacitor respectively, although, it was seen the smaller the inductor the better. The circuit in figure 6.9 was re-tuned to lower the component values below 10 nH and 10 pF, but the line could not tuned down small enough due to the frequencies this design would be operated at. The line was replaced by an inductor, as seen in figure 6.10. However, removing the line's ability to short the second harmonic results in the impedances being moved away from the ideal Continuous Class B continuum, this inadvertently led to an increase in performance. Once the line had been removed the components again were re-tuned to maximise the performance, resulting in the component values shown in figure 6.10(a).

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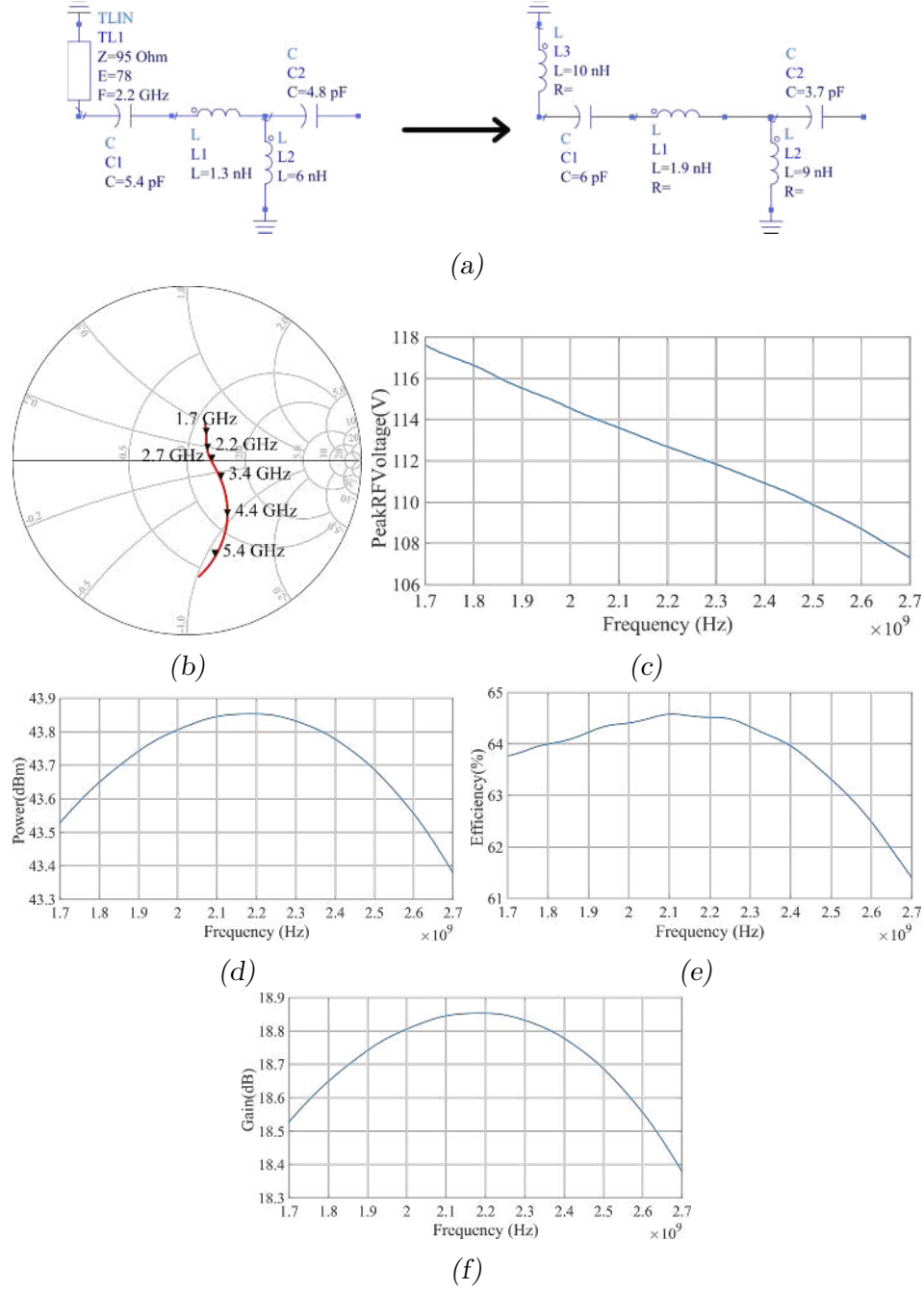


Fig. 6.10: Results from the ideal MMIC circuit (a)Changes to circuit topology (b) Impedance locations (c) Peak RF voltage (d) Output power (e) Drain efficiency (f) Gain

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The peak RF voltage plot, shown in figure 6.10(c), shows that there is a peaking effect that occurs as the frequency is decreased. Comparing this with the impedance trajectory seen in figure 6.10(b) shows the fundamental moving further and further away from the real axis as the frequency decreases. Then looking at figure 6.6 and comparing it to where the low frequency end of the fundamental is, the peak voltage caused by the ideal Continuous Class B theory is expected to be no more than 1.2x larger. Comparing this to figure 6.1, the peaking voltage for the ideal load pull sweep goes from 105 V to 120.75 V, which is 1.15x larger. Looking now at the voltage change in the ideal MMIC, seen in figure 6.10(c), the voltage swing is from 107.5 V to 117.5 which is a voltage increase of 1.1x. The voltage peaking effect is still being seen even though the impedances are not in the ideal locations. Looking at the impedances it is seen that the fundamental impedance is purely capacitive and the second harmonic impedance is purely inductive, which is what is required to peak the voltage, even if the second harmonic is far from the ideal $\Gamma = 1$ locations. It is also possible that the third harmonic is involved, as at these higher levels of compression, the role of the third harmonic will be increased, but it was not taken into consideration during this design process.

In conclusion, despite not presenting the ideal results the peaking voltage does suggest that this device is at least partially in Continuous Class B.

6.5.2 *Moving to MMIC Substrate*

By way of introduction to MMIC components a typical substrate used in MMIC designs is shown in figure 6.11. The designer will then selectively choose to place metal and dielectric to form different components. Capacitors are made by using two metal layers sandwiching a dielectric layer, thus forming an ideal capacitive structure. Inductors are formed by making a spiral in metal that lays flat on the substrate, with the centre then bridged to the outside, where the spiral imitates a coil of wire. Forming the inductor this way naturally creates a capacitance with the substrate causing them to resonate which needs to be taken into consideration when designing, and

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means that the inductors are the most loss prone components in the system.

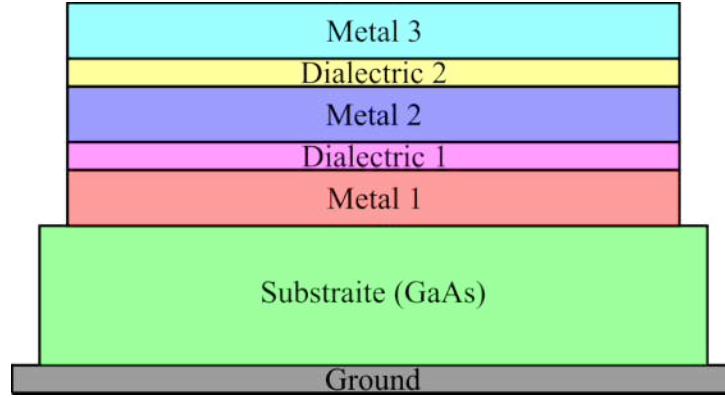


Fig. 6.11: Idealised MMIC substrate example on GaAs.

A MMIC using Qorvo's built in components was implemented in stages. Looking at figure 6.12(a) the first components to be moved to use MMIC based models were the series components (C1, L2 and C2), then adding in the parallel inductors (L1 and L3) and finally any extra input, bias and stability networks. This was done as the series inductor L2 is relatively small and the capacitors do not affect the circuit significantly and so will help isolate the effects of the larger components. The ideal performance is plotted in red on Figure 6.12(b)-(e), then moving the series components to MMIC is shown by the blue and then the two parallel inductors in green. The rest of the circuit was never converted due to the significant performance loss in adding in the parallel inductors.

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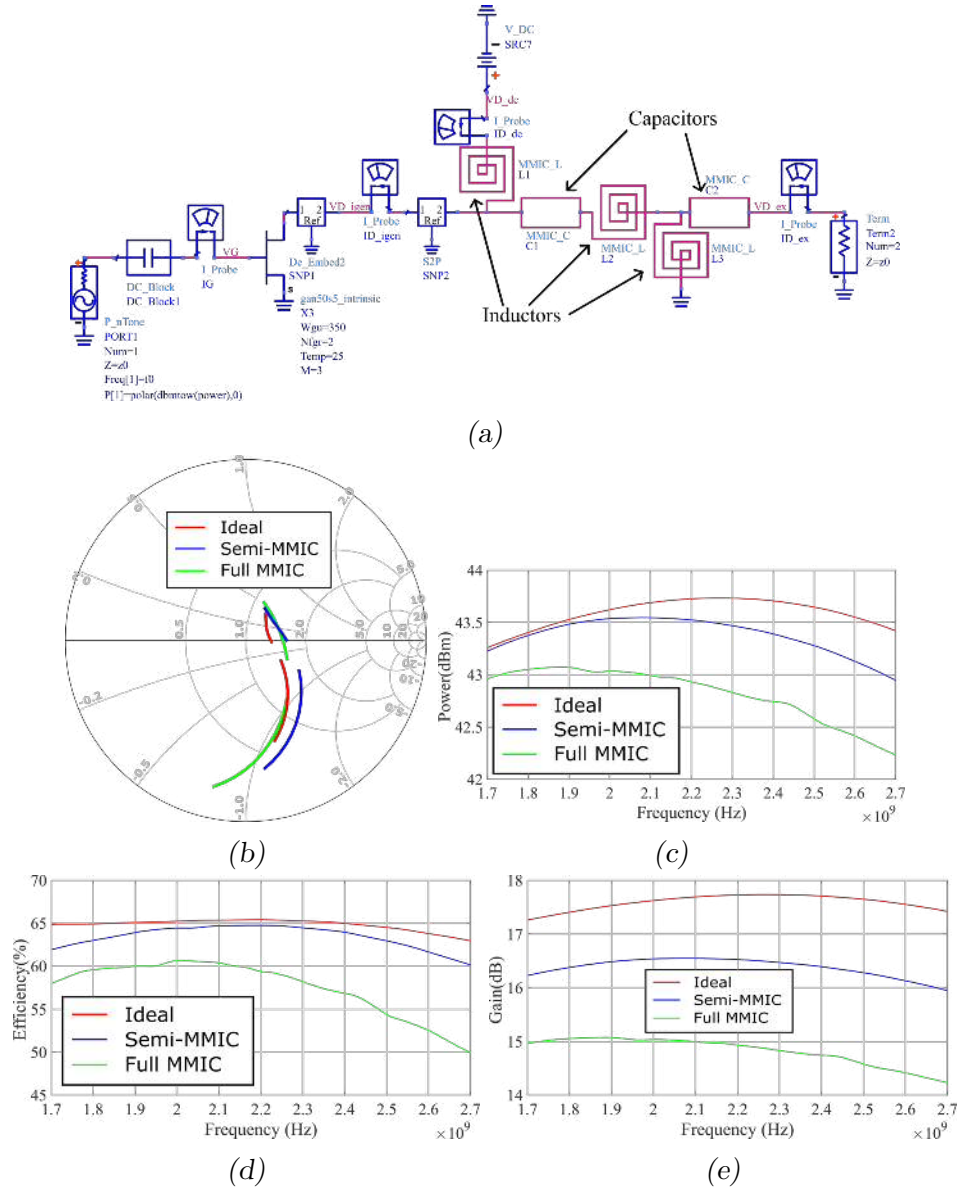


Fig. 6.12: Simulation results; Ideal = ideal components, Semi-MMIC = series components MMIC models with ideal parallel components and Full MMIC = All components as MMIC models (a) Circuit diagram with labels for MMIC components (b) Fundamental and second harmonic impedance locations (c) Output power (d) Drain efficiency (e) Gain

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The movement in impedance shown in figure 6.12(b) was achieved by tuning L2 after every iteration. This moved the impedance roughly up and down the real impedance axis and traded power for efficiency and vice versa, as shown by the two optimums in figure 6.5. Efficiency was optimum at a higher impedance and power at a lower. This in turn caused the power to drop very slightly lower than 43 dBm but allowed the efficiency to remain over 60%, which could easily be tuned to go back in the other direction. However, adding in the two big inductors L1 and L3 added a noticeable amount of parallel capacitance that cannot be recovered by tuning. Hence, the fundamental drops into the capacitive side of the Smith Chart resulting in a performance drop, with both power and efficiency both only meeting specification in the lower half of the band. Looking at the impedances, the lower fundamental is similar across all measurements and then stretches out further from the ideal component simulation at higher frequencies. This is then seen in the relative reduction of the power and efficiency where for the lower frequencies of both, the performance does not drop as much as the higher frequencies. Looking at the gain in figure 6.12(e) it is seen that the drop in power is due to the increased losses in the MMIC components, which also causes the gain to drop.

6.5.3 Inductor design

Looking at how to reduce the losses by modifying the inductor, there are two problems introduced. The first is the loss, measured by the Q factor associated with the component, and the other is the increase in capacitance added by the inductors causing the impedances to move to less desirable locations that cannot be undone with tuning. The loss/Q is mostly affected by the metal properties, which is unchangeable, and the line properties which can be modified. The impedance movement and the drop in Q is affected by the capacitance in the inductors as this directly links to the components resonant frequency. To improve the performance of this circuit required the capacitance in the inductors to be removed/reduced. One source of the low Q and increased capacitance was the bridge used to get the feed line from

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the centre of the inductor to the outer edge. It was decided that bond wires could be used for this design as it was just a prototype, which significantly helps reduce the overall capacitance in the inductor and so improve the Q .

The next stage of improving inductor design was to undertake an investigation into how all the different parameters affected the Q . All the parameters swept are shown in figure 6.13 where two inductors were tested, one with a bridge, and one with a bond wire.

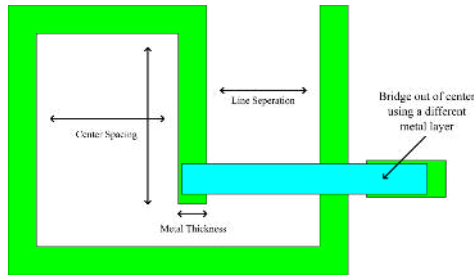


Fig. 6.13: A simplified layout for an inductor with all the sweep variables added.

These were also then tested on a small 1 nH inductor and a much larger 10 nH inductor to see how the changes scaled with size, as seen in figure 6.14.

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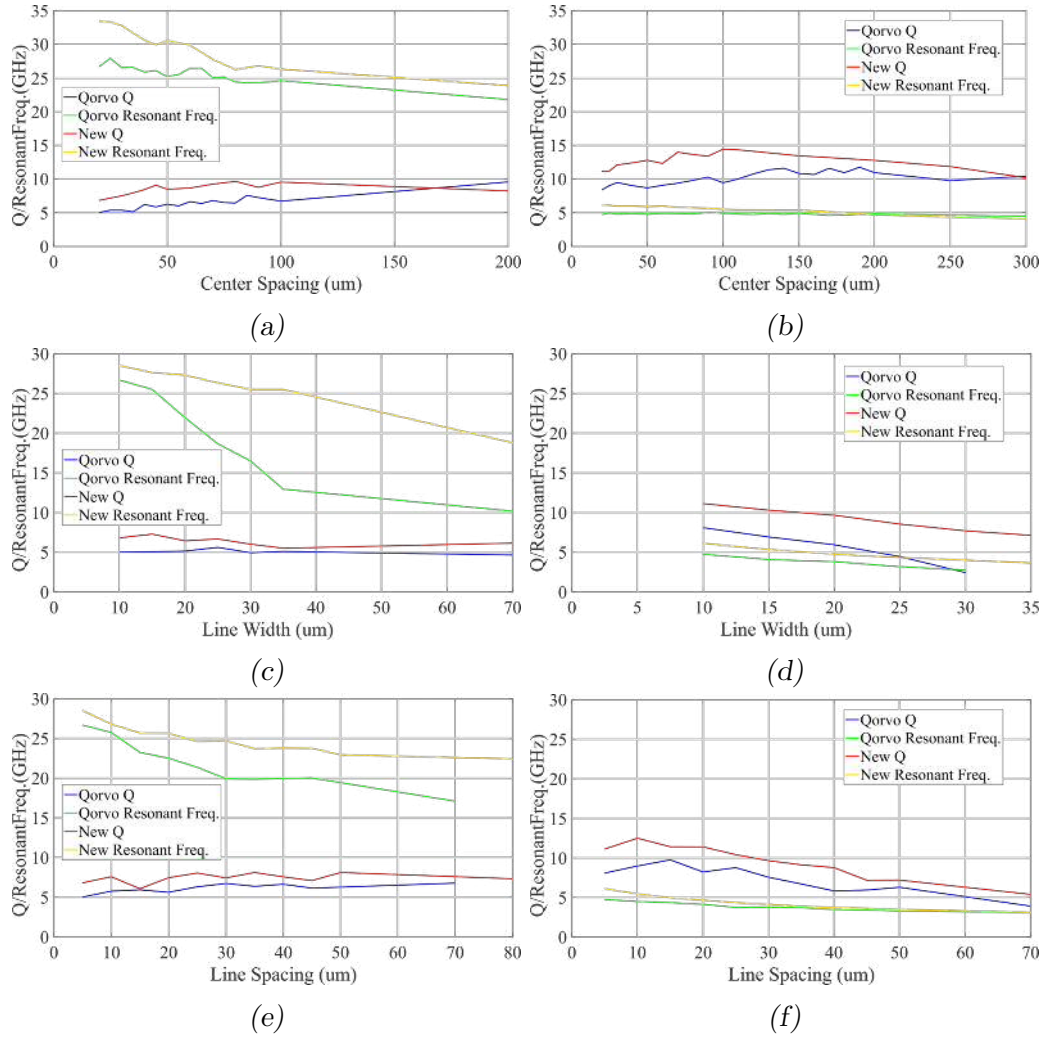


Fig. 6.14: Results from the MMIC inductor tests, (a) Centre Spacing 1 nH (b) Centre Spacing 10 nH (c) Line Thickness 1 nH (d) Line Thickness 10 nH (e) Line Spacing 1 nH (f) Line Spacing 10 nH

As centre spacing increases, shown in figure 6.14(a) and (b), the Q improves on the small 1 nH inductor for both the Qorvo version and the new version. But the new inductor decreased Q when a very large centre spacing was tested. This is likely because the new inductor always took the bond wire from the centre and so as the centre spacing increased so did the bond wire

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length. This would eventually start to increase the capacitance between the bond wire and the substrate, eventually reducing performance. Whereas the Qorvo model would only bridge the rings and so had a constant length bridge in this sweep and so gaining Q with increasing centre spacing. Because of this, the final inductor design will place the bond pad nearer the edge, where it can, to avoid this problem on the new results and take full advantage of the centre spacing Q improvements. For the 10 nH inductors, the new inductor saturates at 100 μm , while the Qorvo model at 200 μm . But the Qorvo inductor had a lower Q than the new model across the board due to the much larger bridge required this time with the increased turn count, so increasing the capacitance. The saturation of Q in the new inductor design is thought to be due to the increasing bond wire length, so the final design should be able to achieve a higher Q . Unfortunately, while centre spacing increases Q it decreases the resonant frequency. For the smaller inductors this is not a problem as it is significantly outside the frequency band of interest meaning large centre inductors can be used. For larger inductors the resonance is sitting in the second harmonic and slowly reducing with increasing centre spacing, so there is a trade-off that needs to be made here to prevent the resonant frequency from coming into the fundamental band.

Line width shows some suppressing results, where it is thought that with increasing line width there is a reduction in resistance/loss and so increasing Q , but for smaller inductors it seems to only reduce the resonance without increasing the Q , and for large inductors this causes a decrease in Q . This is most likely to do with the capacitance between the inductor metal and the ground plate, which increases with increasing line width, and so causes a reduction in resonant frequency for all inductors. For 10 nH inductor as the resonance frequency comes inside the fundamental frequency band, Q is then effected and reduces too. Leaving the only way to increase Q with metal thickness being to stack the different metals on top of one another and increase the metal thickness without increasing its width. Unfortunately, the line thickness cannot be as small as the PDK will allow for all the inductors, as there are some significant currents that the DC feed needs to carry, and although the other inductors can be reduced in size their power handling will

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also have to be considered.

Line spacing has a positive effect for smaller inductors, but as the size increases it starts to become a hindrance. This is again due to the capacitance caused between the metal and the ground plate as this decreases the resonant frequency until it is in band and so reduces the Q , rather than allowing it to increase.

In conclusion the larger inductors have increased capacitance which reduces the resonant frequency until it is close to the frequencies of interest and this then brings down the Q with it, which means the resonant frequency is the main issue causing the reduction in Q . In seeking to increase Q , modifications to the inductor structure can be made, but they often also reduce resonant frequency and so end up reducing performance rather than increasing it. The conductor thickness is one way to achieve higher Q s without increasing the inductor's surface area. Another option is to reduce the overall surface area of the inductor and so the capacitance will also reduce, which will increase the resonant frequency and so lead to a net increase in Q .

A comparison of the final inductor and the previous inductor supplied by Qorvo is shown in figure 6.15. It is seen that the resonance is lower for the new inductors, but this has been traded off for a significant increase in Q in the fundamental band, where there is a doubling of performance in some cases. This allows the circuits these are used in to perform much better overall as the fundamental is the most influential harmonic on performance.

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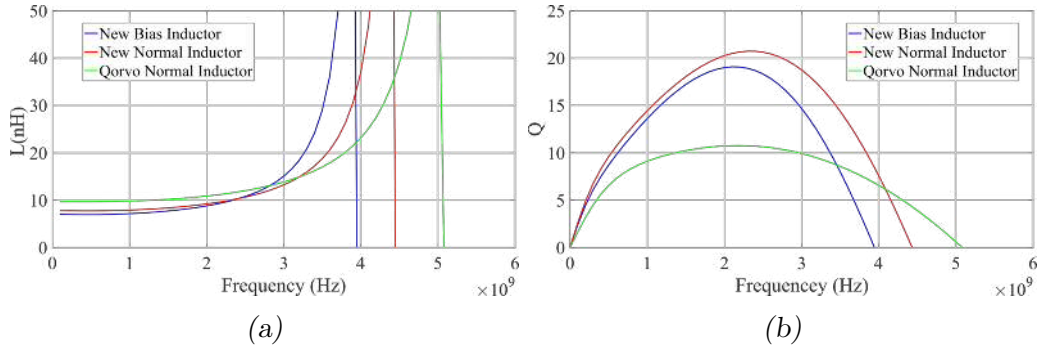


Fig. 6.15: The results of increasing Q . Comparing the worst case with the original Qorvo inductor to the new bias feed and new normal inductor (a) Plot comparing L (b) A plot comparing Q

6.5.4 Final Design

By using the new inductors, the final design was made incorporating all the components, showing an improvement or comparable results in figure 6.17 for the simulations for the full MMIC over those shown in figure 6.12. This shows just how much the new inductors affected the results, as now instead of having half the design reducing the performance beyond what is tolerable, the whole design is near to or meets the specification.

The new inductor significantly improves performance at the higher frequencies and is now above the 43 dBm requirement for all but 2.7 GHz, where it drops to 42.62 dBm (18 W). While the efficiency does not quite reach 60% it does peak at 59% and does not drop below 50% so nothing is lost when compared to the original simulation. The slight drop in gain is likely due to the changes made to the input network and losses within it, due to it now using MMIC inductors.

Looking at back-off performance, efficiency, as expected is low. The simulations predict an average of just over 30% back-off efficiency which is very poor, but with the Class B based designs not having anything to recover efficiency at back-off this is to be expected.

This design was then fabricated by Qorvo, as seen in figure 6.16. Char-

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acterization involved performing power sweeps vs. frequency. The 3 dB compression results are shown next to the simulated results in figure 6.17, where a significant reduction in performance is seen. This is likely due to thermal compression as these tests were done under CW conditions and so a lot of heat would have been generated by the device. One indication of this is current compression, which is observed in the output waves shown in figure 6.18.

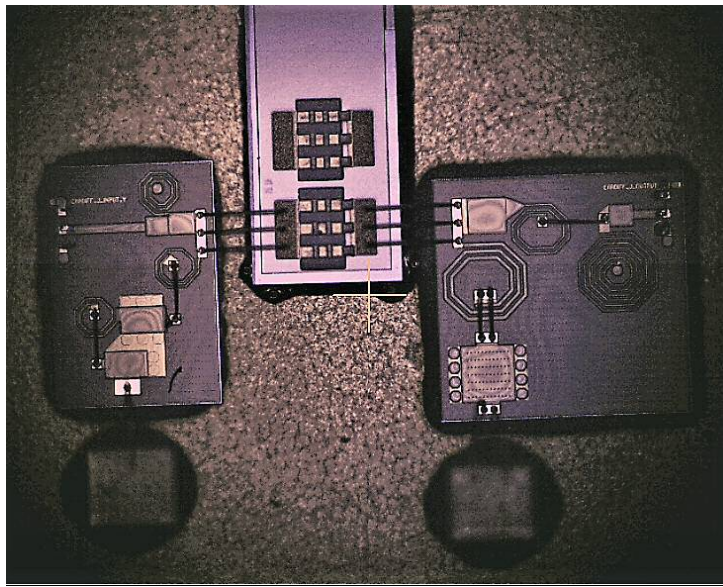


Fig. 6.16: Picture of the final Continuous Class B quasi MMIC

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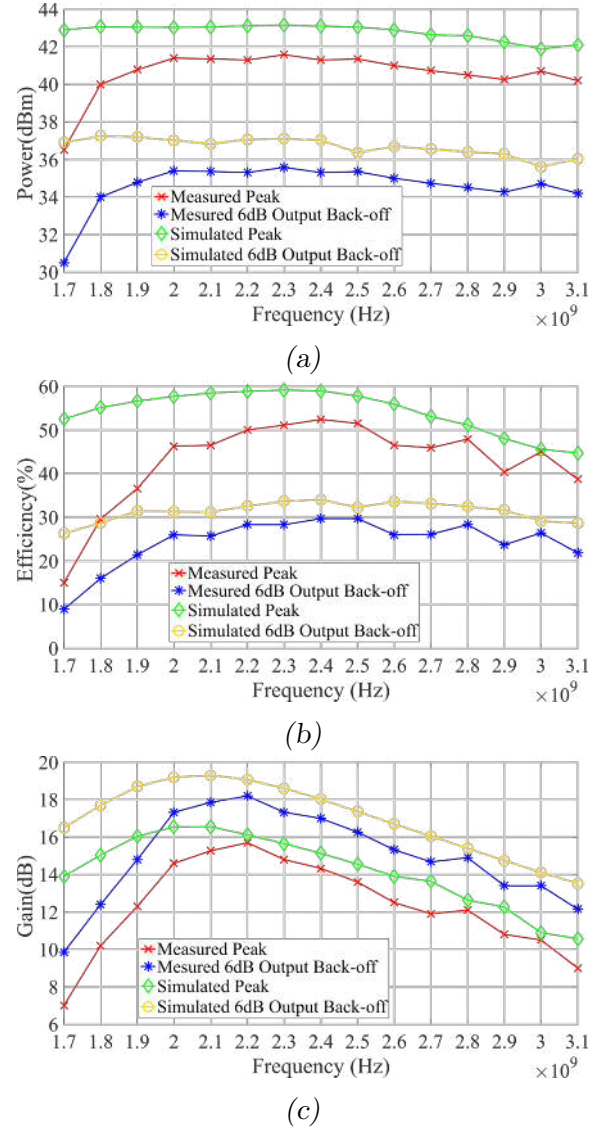


Fig. 6.17: Final simulated and measured results at peak and 6 dB OBO performance (a)output power (b) Drain efficiency (c) Gain

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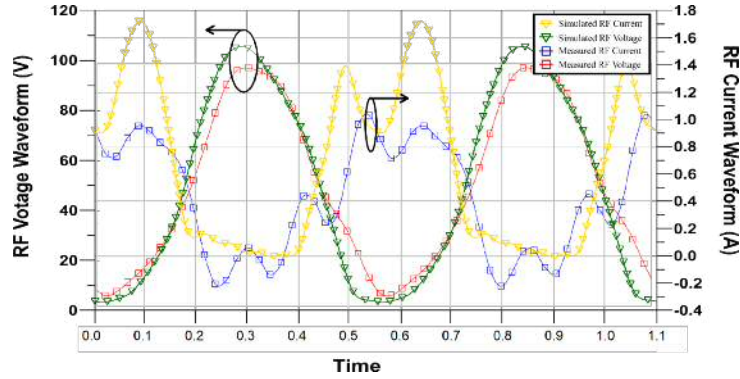


Fig. 6.18: Measured and simulated waveforms to show the current compression

Due to time limitations on the project there was only time for CW tests. It is anticipated that these tests will be re-done by a future student under pulsed conditions, where it is expected that both the current and performance will see improvements.

6.6 Conclusions

This chapter laid out the first MMIC Continuous Class B PA at S-band. It started with a new novel 50 V GaN FET and then using waveform engineering theory concluded with the first quasi MMIC using Continuous Class B theory. The final quasi MMIC was also well performing given the inductor losses and CW compression, which shows real potential for improvement with further measurements and design adjustments. For a first design, this was a success and was proof of concept that continuous modes can make the jump to MMIC and so expanding their usefulness further. The move from laminate based designs to a MMIC design was not a direct topology translation, changing the line for an inductor prevented the second harmonic impedance to be presented with the required short. Further improvements to the inductor designs should be possible and this opens the door to a lot of future work to be done on MMICs with continuous modes.

Design of a Doherty Quasi MMIC

7.1 Introduction

This chapter uses novel 50 V GaN FETs to extend the bandwidth of a Doherty PA by taking advantage of the impedances the higher voltage operating point offers. It is a parallel design to Chapter 6, where the back-off performance was low, which is what the Doherty addresses. The downside to the Doherty is that it is an inherently narrowband design due to the impedance transformer that is often implemented as a $1/4$ wave line. The final aim of this research is to apply some of the broadband nature of the Continuous Class B into the Doherty. This chapter starts this research by fabricating a Doherty design on MMIC. This design extends the bandwidth by taking advantage of the periphery the new 50 V GaN FET, supplied by Qorvo, to use lumped element impedance transformation rather than a $1/4$ wave line.

The final design was an evolution of a broadband Doherty inspired by a design proposed by Chalmers, [8], which tries to incorporate C_{ds} in the matching network to increase bandwidth. The first iteration of the design then suffered performance issues due to the MMIC inductors, as seen in Chapter 6.5.3. To reduce the number of inductors in the design, and help mitigate the inductor loss, the design topology was changed again. This chapter will follow a similar flow to the previous design chapter and starts by looking over the Doherty theory and how the Chalmers design intends to use C_{ds} as part of the matching network and so increase the bandwidth. It then goes on to discuss any changes that need to be made to the Chalmers design to allow it to be fabricated on a MMIC substrate. As with the previous Continuous Class B the Chalmers Doherty is fabricated on laminate and uses a transmission line, which at these frequencies, is too long to be implemented on a MMIC. The next step was to then change the design again to take full

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advantage of the GaN50's periphery, which was the design that was taken forward, fabricated and measured. The measurements were carried out by a colleague.

7.2 Doherty Theory

The fundamental idea behind Doherty PAs is to load pull the main PA with an auxiliary PA, changing the load presented to the main PA to keep the voltage constant during back-off and so holding the efficiency constant also. The ideal topology of a Doherty is seen in figure 7.1.

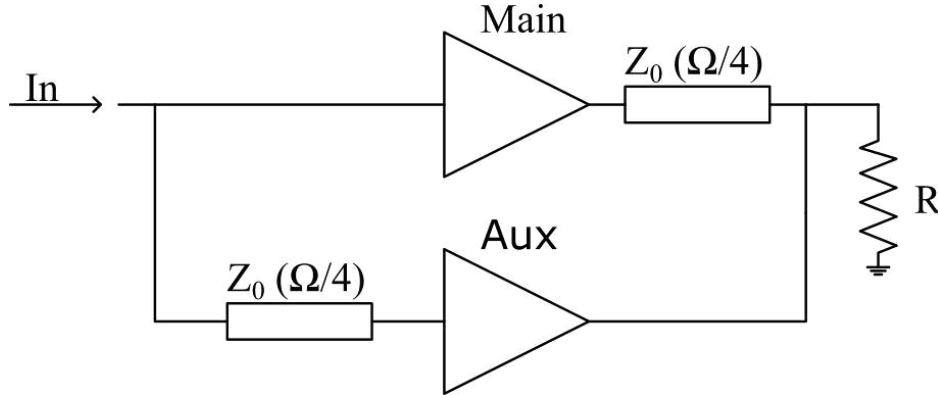


Fig. 7.1: Ideal Doherty structure

The main limitation to this is fabricating a broad band impedance inverter to go on the output of the main PA. This is normally done using a $1/4$ wave line which by its nature is very narrow band. The Chalmers design, [8], aims to include the output capacitor in the matching networks and does not just use one $1/4$ wave line to invert the impedance. These changes combined with using two sources, one for each device seen in figure 7.2, and then tuning of each source allows this design to achieve broadband performance.

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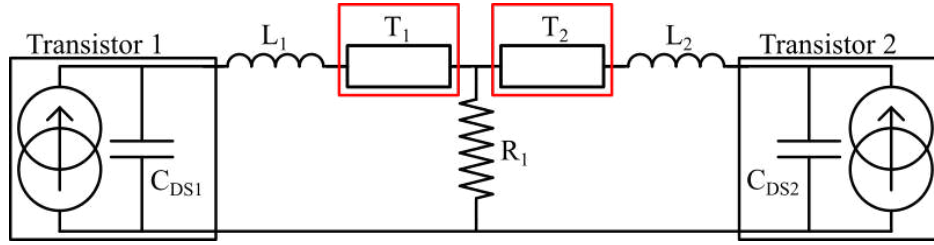


Fig. 7.2: A simple diagram of Chalmers design

The two sources shown in figure 7.2 allow an extra degree of freedom to tune the Aux PAs source phase as frequency changes. This will compensate for the impedance inverter not functioning at its optimum, as the frequency of operation moves away from the optimum design frequency. Following Chalmers lead, this Doherty PA design will also be a dual input PA, but the phase between them kept constant. This was done to allow a degree of freedom that most Doherty PAs do not get, while not making the design so open that simulations and measurements take longer than the time available.

As described in their paper, the circuit is brute force optimised to match the periphery and C_{ds} of the device. Unfortunately, as with the previous design, the lines in the matching network (highlighted with a red box in figure 7.2) cannot be easily transferred into MMIC for this frequency range. This means that like the previous design the circuit needs to be modified, but unlike the previous design the line cannot be swapped out for an inductor, so there needs to be a more fundamental change to the circuit topology.

The next step took the basic idea of using C_{ds} as a part of the matching network from the Chalmers design, while at the same time replacing the function of the $1/4$ wave line. To achieve this the line was replaced with a lumped component equivalent. The various ways this can be achieved for this design are shown in figure 7.3, where (a) would meet all the required specifications, as it has parallel C's that can encompass C_{ds} and will also act as an impedance inverter like the line as shown in equation 7.1.

$$\text{Line} = \begin{bmatrix} \cos(\theta) & jZ_0 \sin(\theta) \\ \frac{j}{Z_0} \sin(\theta) & \cos(\theta) \end{bmatrix} \Rightarrow \begin{bmatrix} 0 & jZ_0 \\ \frac{j}{Z_0} & 0 \end{bmatrix}, \text{ if } \theta = \frac{\pi}{2} \quad (7.1)$$

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$$\text{CLC } \Pi = \begin{bmatrix} 1 - \omega^2 LC & j\omega L \\ j\omega C(2 - \omega^2 LC) & 1 - \omega^2 LC \end{bmatrix} \Rightarrow \begin{bmatrix} 0 & j\omega L \\ j\omega C & 0 \end{bmatrix}, \text{ if } \omega^2 LC = 1 \quad (7.2)$$

$$\text{LCL } \Pi = \begin{bmatrix} 1 - \frac{1}{\omega^2 LC} & \frac{1}{j\omega C} \\ \frac{1}{j\omega L}(2 - \frac{1}{\omega^2 LC}) & 1 - \frac{1}{\omega^2 LC} \end{bmatrix} \Rightarrow \begin{bmatrix} 0 & \frac{1}{j\omega C} \\ \frac{1}{j\omega L} & 0 \end{bmatrix}, \text{ if } \omega^2 LC = 1 \quad (7.3)$$

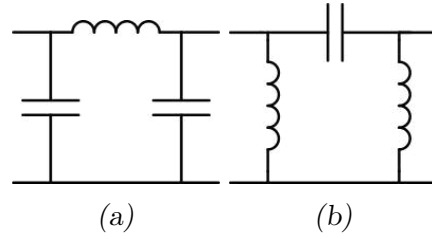


Fig. 7.3: Examples of transmission line replacement networks (a) CLC Pi (b) LCL Pi

This is not a new idea and has been used in designs before but is often not capable of also impedance matching the Doherty to the output. However, with the periphery of the 50 V GaN starting to remove this problem by being able to set target currents and voltages consistent with simple 50 Ω and 25 Ω loads, now is a good time to start re-visiting older solutions and applying them to newer technology. It was also decided to revert the overall network back to the more traditional configuration over the Chalmers distributed approach and only have the impedance inverter on the output of the main, which will also allow the traditional Doherty action to be observed in the back-off period.

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7.3 Ideal Designs

7.3.1 Chalmers Based Design

The CLC network was applied to the Chalmers layout, as shown in figure 7.4(a), then using the $C_{ds} = 0.9$ pF for C and 2.2 GHz this then allows L to be calculated to be 5.8 nH, shown in equation 7.4.

$$\omega^2 LC = 1 \Rightarrow C = \frac{1}{2\pi f L} = \frac{1}{2\pi \times 2.2 \times 10^9 \times 0.9 \times 10^{-12}} = 5.8 \times 10^{-9} \quad (7.4)$$

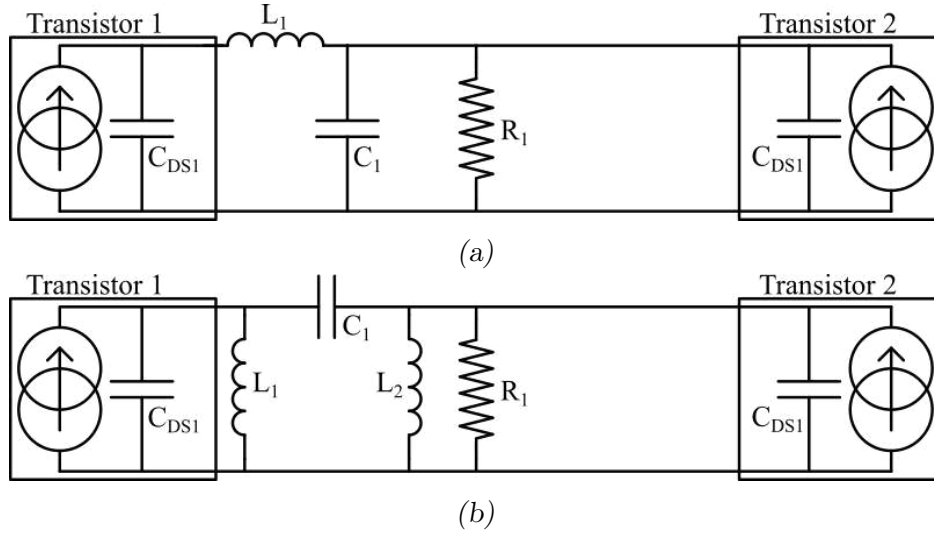


Fig. 7.4: The two versions of the Doherty that were realised. (a) Based on the Chalmers Paper to include C_{DS} (b) Re-configured version to use two inductors that can be used for both matching and as bias feeds

Then simulating with these values and the Qorvo model gave some good results after only a small amount of tuning, seen in figure 7.5.

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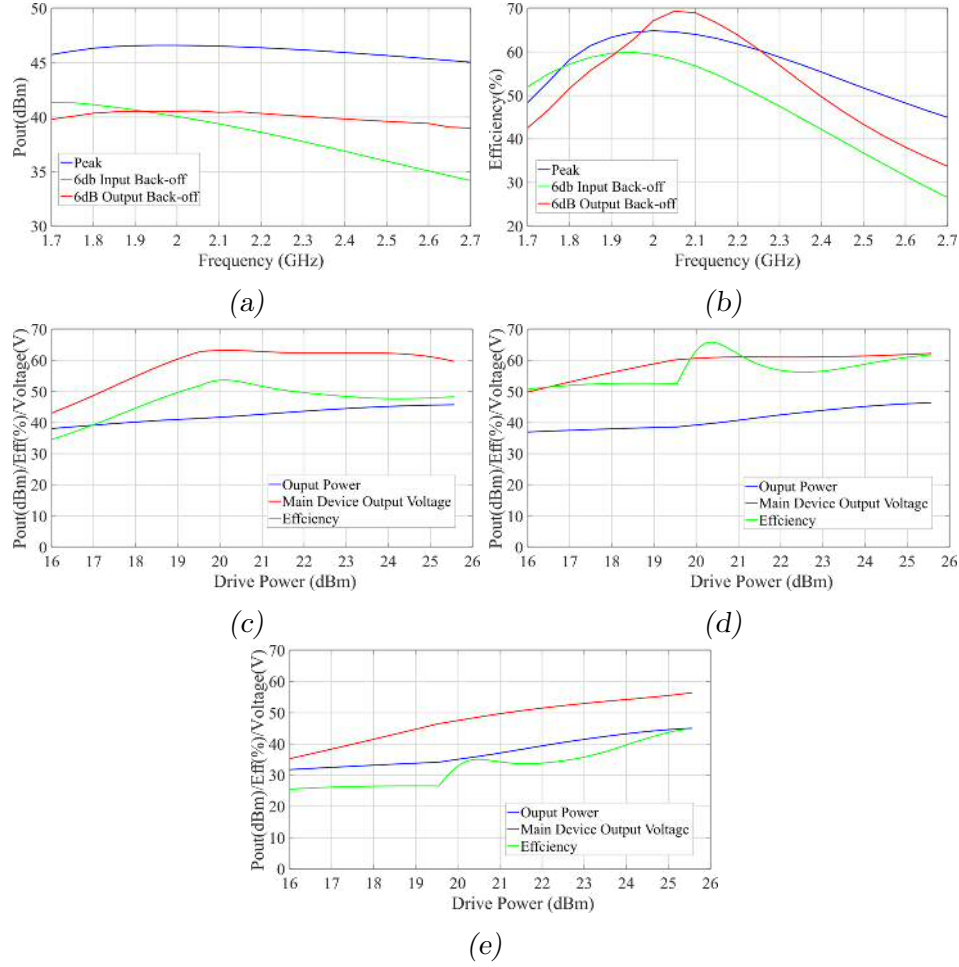


Fig. 7.5: The results from simulating ‘figure 7.3(a)’ (a) Output power across bandwidth (b) Drain efficiency across bandwidth and back-off (c) Output power, efficiency and Main PA voltage back-off action for 1.7 GHz (d) Output power, efficiency and Main PA voltage back-off action for 2.2 GHz (e) Output power, efficiency and Main PA voltage back-off action for 2.7 GHz

Looking at figure 7.5(b) the peak efficiency is when the device is operating at peak output power, in this case 46 dBm. The input back-off is when the input power is backed off by 6 dBm. The OBO is looking at the efficiency at whatever drive power gives a 6 dBm drop in output power, which will

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vary with frequency due to different compression levels. It is most important to see the output power back-off efficiency as this removes the effects of the differing compression levels across the band. Also, the modulated signal will need to see 6-9 dBm change in the output power of the PA, not the input drive level. The input back-off is included here to show how the compression level will need to be compensated for.

If the bandwidth target of the design is reduced by just under half to 1.8-2.4 GHz and reducing the peak efficiency specification from 60% to 50% a good back-off efficiency can be obtained, where the Continuous Class B had a back-off efficiency of 29-33%, the Doherty has simulated over 50%, seen in figure 7.5(b) and the power stays over 46 dBm (40 W) as shown in (a). While this still does not have the same bandwidth as the Continuous Class B, it does have much better back-off efficiency. This makes the Doherty more attractive than the Continuous Class B for applications that involve modulated signals, as some can spend most of their time at the 6-9 dB back-off, which makes having a good back-off efficiency more important for some use cases than peak efficiency.

The Doherty action seems to peak at 2.2 GHz, as shown in figure 7.5(d), where the main device's voltage is held flat over the full 6 dB back-off period and the efficiency recovers just before the 6 dB point. Also, the power is within 3 dB of compression when starting from 19.5 dBm input drive. The voltage at 1.7 GHz is also very flat and while the efficiency is lower, it is increasing with back-off, so giving it an overall good performance. Although looking at figure 7.5(c) it is seen that the voltage is starting to drop at the peak output power, and for frequencies lower than 1.7 GHz this effect increases causing a quick roll off in performance. At 2.7 GHz the Doherty effect is not fully working and the voltage is no longer held level with back-off, as seen in figure 7.5(e), and with it the efficiency also drops with back-off.

As with the Continuous Class B, once the ideal design had been tuned and finalised it was moved onto Qorvo's substrate where again the inductors proved problematic. Even with the optimised inductors the performance drop made it comparable to the Continuous Class B back-off at 30% on average and so the bandwidth performance of the Continuous Class B wins out. The

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main issue arose when large inductors were added for the bias feeds, which are not shown in the ideal circuit analysis, so the design was changed again to reduce the number of inductors.

7.3.2 MMIC Optimised Design

To help restore the performance lost due to inductors, the LCL network was used instead, shown in Figure 7.3(a) and Figure 7.4(b), with its impedance inverting performance shown in equation 7.3. While this network does not account for the C_{ds} of the devices it does have a pair of parallel inductors that can be used to feed the bias in, and so recover more performance when moving to MMIC than what is lost due to C_{ds} .

Another change made to the designs was to lower the DC drain voltage used for the Main PA and the peak current used for the Aux PA. The Main device operated at a drain bias voltage of 25 V and target a current of 1 A, whereas the Aux will run at drain bias voltage of 50mV and target 0.5 A. This will give the Main an optimum impedance of 25 Ω and the Aux an optimum of 100 Ω . This will allow the Main device to reach peak voltage at 25 Ω , which will then be load pulled up to 50 Ω by the Aux device, which at peak output power will remove the need for a matching network between the Doherty PA and the 50 Ω presented by the outside world. This should help increase the design bandwidth, which is only possible with the new 50 V GaN FET supplied by Qorvo.

The Main PA load requirement is 25 Ω , then due to the impedance inverter the Aux PA will be presented with 100 Ω at back-off which is what the Aux PA will be presenting. In both cases the periphery of the device requires no matching network and should allow a natural broadband match. Due to the novelty of the 50 V GaN devices this is the first time the periphery of the device has been utilised in this way to realise a Doherty.

To investigate the effects of how much C_{ds} will impact the ideal results, ideal current generators were used to simulate the network and then parallel capacitors were added to view the reduced performance due to C_{ds} , seen in figure 7.6.

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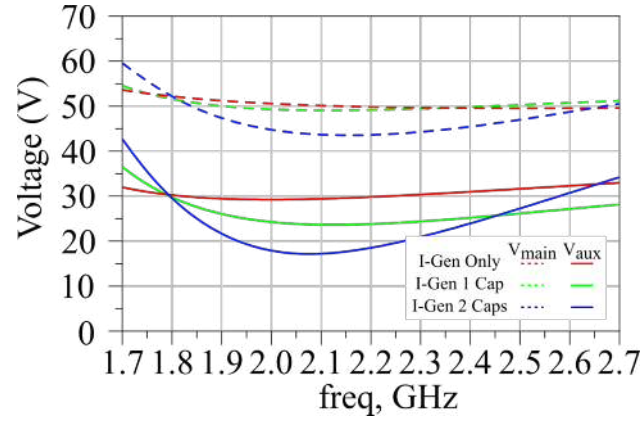


Fig. 7.6: Effect of adding capacitors to the new topology

The effects of just adding one capacitor at the Main PA shows that the circuit still manages to hold its performance, but then adding in the second capacitor at the Aux PA causes significant deviations from the optimum performance.

Applying these changes to the Qorvo model and re-tuning the network gives the results shown in figure 7.7. The peak power has dropped, which is to be expected with the reduction in voltage and current, although it still maintains more than 44 dBm (25 W) for the majority of the band width, which would be the new target for power.

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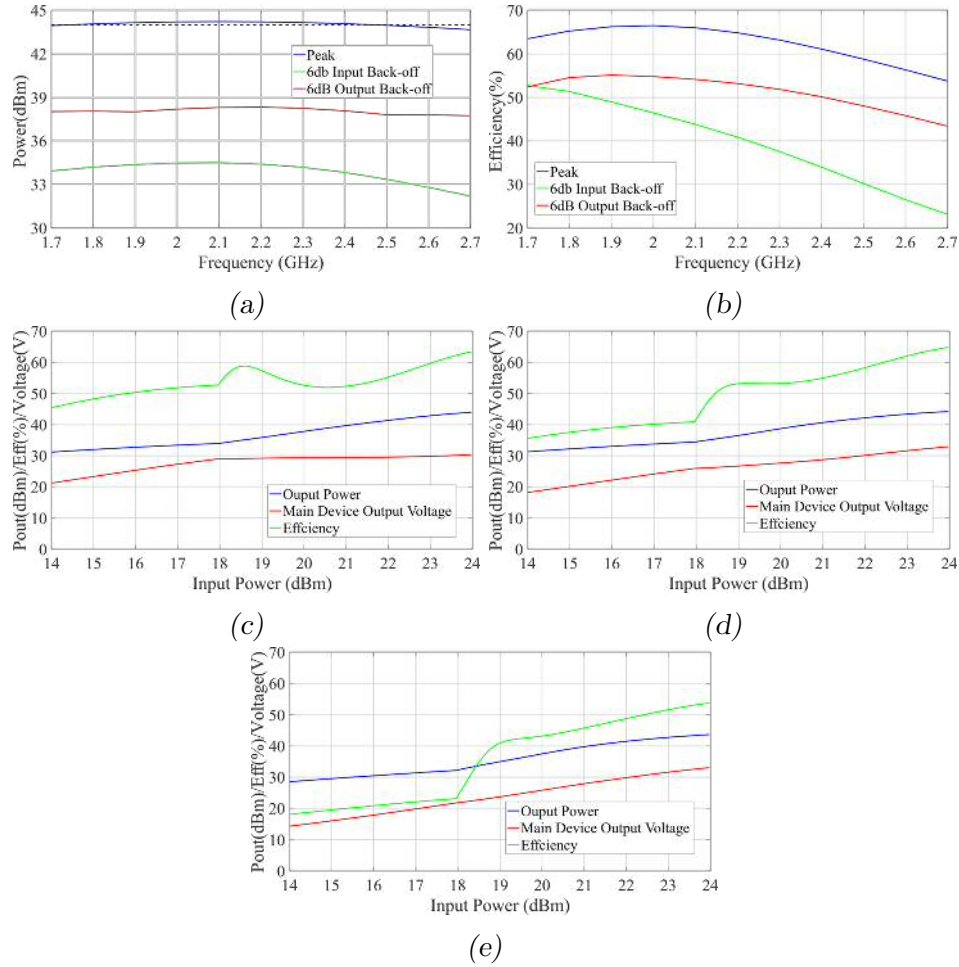


Fig. 7.7: The results from simulating ‘figure 7.3(b)’ (a) Output power across bandwidth (b) Drain efficiency across bandwidth and back-off (c) Output power, efficiency and Main PA voltage back-off action for 1.7 GHz (d) Output power, efficiency and Main PA voltage back-off action for 2.2 GHz (e) Output power, efficiency and Main PA voltage back-off action for 2.7 GHz

The other big change is the efficiency, as now while the maximum back-off and peak efficiency have reduced, the overall average performance has improved, due to the increased broadband performance of the circuit. The Doherty action at individual frequency points has been degraded, with only

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1.7 GHz now being the only point with a flat voltage response over back-off, showing the typical Doherty response has been degraded but this allows the bandwidth to be increased. Despite this design having reduced power it has comparable and even improved efficiency performance and is now functioning over a wider bandwidth and with the reduced inductor count meant this design was ready to be designed as a MMIC.

7.4 MMIC Design Simulations

Designing the Doherty as a MMIC followed a similar path as the Continuous Class B of tuning and re-tuning components, especially inductors, and despite this new design where the bias feed inductors and impedance transforming network inductors were combined, there was still loss to the performance, as seen in figure 7.8. Peak drain efficiency is near 45%, which is a significant improvement over the Continuous Class B, but as with the peak output power, the drain efficiency is less than the Continuous Class B. As the back-off is more important for use with modulated signals, this is often an acceptable compromise. Looking at the performance the voltage behaviour is degraded and does not remain level during back-off. The efficiency still shows some signs of peaking at back-off in figure 7.8(c) and (d), and is flat in (e). It is expected that the degradation in performance is because of C_{ds} no longer being taken into account in the impedance transformation network and so now degrading the performance.

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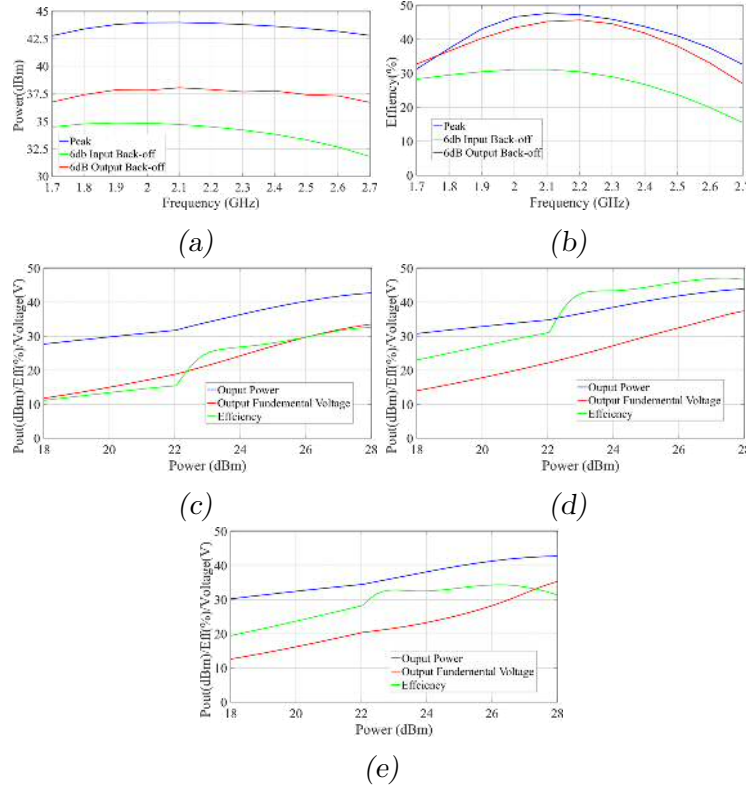


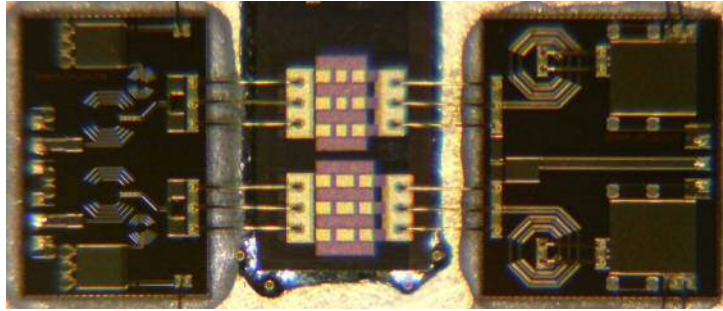
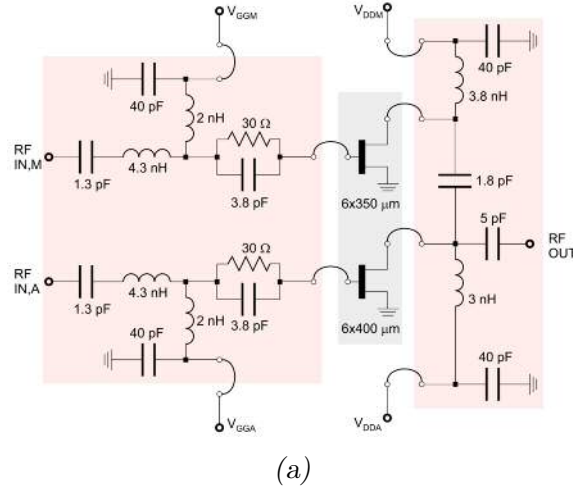
Fig. 7.8: Simulation results from the final MMIC (a) Output power across bandwidth (b) Drain efficiency across bandwidth and back-off (c) Output power, efficiency and Main PA voltage back-off action for 1.7 GHz (d) Output power, efficiency and Main PA voltage back-off action for 2.2 GHz (e) Output power, efficiency and Main PA voltage back-off action for 2.7 GHz

7.5 MMIC Design Measurements

The Doherty was laid out, measured and then published by Roberto Quaglia, [58]. The final fabricated Doherty is shown in figure 7.9, where both the block diagram and the final circuit was shown as a Quasi MMIC. Then the measured results are seen in figure 7.10. They show that the measured performance has a reduction in power, as seen with the Continuous Class

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B results, likely also to be due to being measured under CW rather than pulsed. Looking at the peak drain efficiency of the measured results, there is good correlation to the simulated measurements seen in figure 7.8, and even an improvement at the band edges. The OBO drain efficiency is not as well correlated, showing a reduction in the measured results centre band, but still maintaining over 40% for most of the band.



(b) Final results for the Doherty MMIC, measured by Roberto Quaglia, [58]

Fig. 7.9: Final quasi MMIC that was fabricated (a) Circuit diagram (b) Photo of Doherty quasi MMIC

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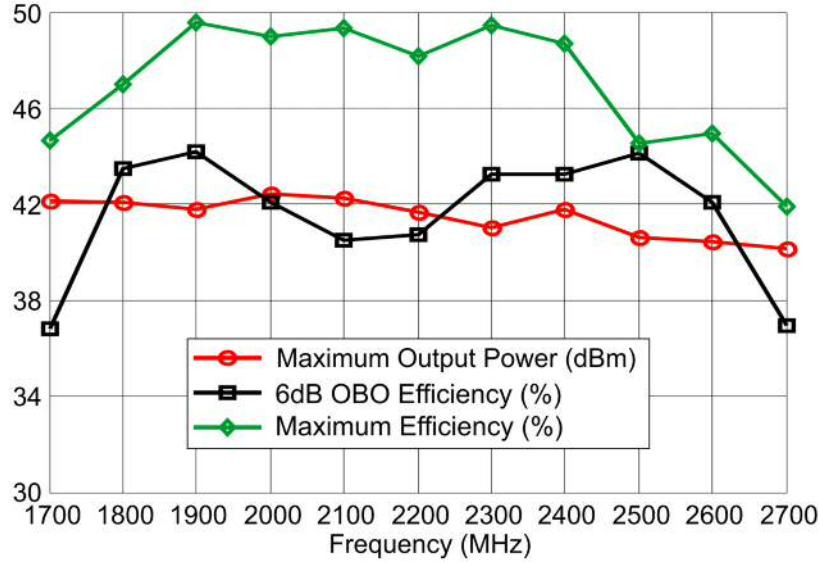


Fig. 7.10: Measured CW performance vs. frequency. Bias: $V_{DDM} = 28$ V, $I_{DDM} = 24$ mA, $V_{DDA} = 50$ V, $V_{GGA} = -3.5$ V. [58]

7.6 Conclusion

This design started by seeking to build on the Chalmers paper and go back to basic principles to start and increase the bandwidth of MMIC designs. Using Qorvo's new 50 V GaN process it was possible to increase the bandwidth by removing the need for matching networks. This chapter has shown by using two different design topologies that the MMIC still has challenges at the target band, but it is possible to increase the bandwidth beyond the narrow bandwidth nature of the traditional Doherty design. It was seen that the CLC network can go a long way to reducing the effects of C_{ds} but struggles to perform in the MMIC environment, which means a topology that is more MMIC friendly needs to be used. However, this causes the effects of C_{ds} to return and limit the bandwidth, although in this case re-adjusting the topology of the devices re-gains the bandwidth lost to the capacitors. While this was a first attempt to investigate the possibility that the bandwidth of the Doherty can be increased by drawing on a variety of new and old

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techniques mixed with a new device type, and although met with variable success it shows there is potential to perform very well with some more work. Even with the dip in the back-off drain efficiency in the centre of the band the measurement results are competitive. The measured results also show good correlation to the simulated results. This design is a good first step in showing how using the novel 50 V GaN FET can help increase the bandwidth of a traditionally narrowband topology like the Doherty.

Conclusions and Future Work

This research was focused around one aim:

Increase the efficiency of the RF PA to reduce the power consumption of the mobile communications system.

This aim arose out of the need to reduce the power consumption for the whole communications chain for both environmental concerns of power usage and cost savings. This applies directly to the base station, which is the largest consumer of power, and the RFPA where low efficiencies will mean extra cooling is required. This extra cooling is an unwanted cost, complexity and power draw within the base station.

Conversely increased efficiency of the RFPA will reduce the cost, complexity, and power requirements of a base station, which have several secondary benefits for the whole communications network. Firstly, the reduced cost of a base station means that for a set budget more base stations can be built, leading to better coverage for the network. Next, reduced complexity in this case will mean reduced size, as the cooling will be reduced/removed, allowing the base station to be placed in previously unreachable locations. Then lastly, for a given output power an increase in efficiency will lead to a reduction in the supplied power and so cost savings.

One of the key factors in determining the efficiency of the system is the nature of the device used within the PA. In Chapter 4.5 and Chapter 5.3.4 the two different devices that are used within a PA, HEMT and HBT were compared. This comparison showed the HBT had up to 12% better efficiency than the HEMT before any efficiency enhancement techniques were utilised. This makes it a desirable device to use in base stations, but due to the peak voltage failure that it is prone to (as shown in Chapter 2.3.2), the HBT is not able to be used in high power markets like the base station market. To

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overcome this limitation, Chapter 3 introduces a new multi-harmonic version of the VSWR stress test which also measures waveforms that can be used to analyse devices and test for areas of peak voltage, to help diagnose and prevent the peak voltage failure HBTs are prone to.

The results in Chapter 3 showed that peak voltages were caused by sweeping the fundamental and second harmonic impedances during the VSWR test. Showing the need for multi-harmonic load pull to search out the areas of peak voltage that are caused by, in this case, combinations of fundamental and second harmonics, but could also be caused by other harmonics. In the example seen in Chapter 3, there were two pairings between the fundamental and the second harmonic that caused a peak voltage, one capacitive fundamental location and one inductive fundamental location. The capacitive fundamental location was paired with an inductive second harmonic to cause a peak voltage that could cause failure and the inductive fundamental impedance paired with a capacitive second harmonic location to also cause a peak voltage that could potentially cause failure. Neither of these peak voltage regions would have been observed without the new multi-harmonic waveform based VSWR sweep.

This work with VSWR sweeps was built on the work done previously at Cardiff [24] where the effects of holding the second and third at open and short locations were explored in order to explore what was thought to be the worst case scenarios at the time. This was expanded upon in this work to look at the full second and third impedance space. This resulted in the peaking voltage effect to be observed in this work that was previously un-observed.

The work done in Chapter 3 does not cover how the second and third harmonic impedances interact with each other, so future work should seek to characterise this impedance space and even harmonics beyond to look for other areas where the device is put under peak RF voltage or current stress. Also adding in extra harmonics will increase the sweep time and so this process will need to be more automated by software than it is now.

While using the new multi-harmonic VSWR sweep on the HBT, a group of failures were identified, which were investigated in Chapter 4. Due to peak RF voltage being a common failure mechanism in HBTs and the impedance

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locations matching the capacitive fundamental and inductive second impedance pairing that caused the peak voltages, it was expected that peak voltage was the likely cause and so waveform data is used to diagnose the failures. The failures were the result of a several different causes, with the main cause being the DLL penetrating into the negative voltage and negative current region. This was only clearly identifiable when using the waveform data, which was also used to verify that the next iteration of this HBT process did not suffer from the same failure. This showed the necessity of using waveforms when performing stress analysis as the conventional performance data that is often obtained during these sweeps does not always give a conclusive answer to what caused the failure.

The diagnostic work was also built on previous waveform based work done at Cardiff, and showed here how it can be further applied in new ways to help diagnose failures in high efficiency designs. To advance the work done in Chapter 4, and make the diagnosis process clearer, would be to see exactly where in the RF waveform the device failed. Future work should investigate adding a transient receiver to the test set up that monitors the RF voltage and current continuously, rather than at discrete points, or if the oscilloscope is the receiver in the system, using it to make this measurement.

Another way to enhance efficiency is to evaluate and improve the physical limits of a device technology. One common cause for degradation in efficiency is when the DC-IV knee moves away from a vertical position (R_{on} increasing). Adding to this when DC-RF dispersion occurs, which is where the RF-IV knee moves further away from the DC-IV knee with increasing output bias voltage, further efficiency reductions occur. Chapter 5 uses waveform engineering to characterise how this effect changes the device's performance. This is done using the waveform and performance data generated while mapping out the RF knee, and then processing and presenting it in a novel way. FET based devices are especially prone to DC-RF dispersion and so this new technique was used to compare two GaN 50 V FET devices, the GaN50 and the GaN25HV, to see how their different DC-RF dispersion characteristics affected each device's performance. The new data analysis technique was able to compare the two devices meaningfully. The results showed that the

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GaN50 has a higher power density/mm that led to better efficiency, although the gain was lower than the GaN25HV. Due to the higher power density/mm of the GaN50 this was taken forward and used in designs.

The measurement and data analysis process shown in Chapter 5 is in the early stages of development, so there is a lot of work still to be done in refining it. It is designed to work with the data gained from waveform based load pull systems like [59], to further expand their capabilities. There is a lot of data generated by the waveform measurements and a lot of it is hard to access due to the plotting method being convoluted. If the full breadth of waveform data is going to be utilised, then it needs to be easily accessible and quick to plot. This will involve designing software that can automate the process and allow users to quickly measure and analyse devices without having to spend days processing the data obtained. This new method also needs to be published to allow the wider community to start using and improving it. Time did not allow the project to measure more HBTs using this new measurement method to compare them with FET based devices of similar power output. Future work should also investigate why the RF DLL seems to push through the DC-IV, seen in figure 5.12, to allow a more meaningful comparison between HBT and FET devices to be seen.

The other way to improve efficiency is to use efficiency enhancing topologies; Chapter 6 and Chapter 7 show some of these in use. Chapter 6 focuses on a bandwidth extension topology, the Continuous Class B, and Chapter 7 looks to extend the bandwidth of a topology that has improved back-off performance, the Doherty. Both designs were developed as quasi MMICs, where the matching networks were fabricated on GaAs chips to reduce the cost, and the FET devices were fabricated on a GaN chip. Then both parts were bonded together to form the full device. The performance of these chips is comparable to a full MMIC and was only done to save the cost of a full GaN run.

The Continuous Class B design has been primarily implemented on laminate, such as Rogers 5800, so far [60] or at X-band [43], which allows the use of lines to control the second harmonic. Chapter 6 presents the first quasi MMIC Continuous Class B design at S-band, but as the matching was

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done on a MMIC chip the transmission line could not be used to control the second harmonic and so was replaced with an inductor. Replacing the line with an inductor moved the impedances away from the ideal theory for Continuous Class B, although this caused a performance improvement which was unexpected. The inability to use the line was not the only change that moving to a MMIC environment caused. MMIC based inductors have a low Q , which increases the loss in them and the matching network they are used in, which decreases the performance. They also have a resonant frequency that is close to the fundamental frequency, which also decreases performance. This was overcome by designing custom inductors that increased the Q and moved the resonant frequency away from the fundamental.

The measured results of the Continuous Class B design in Chapter 6 shows a drop in the performance compared to the simulated results, power dropped down from 19 - 20 W to 10 - 15 W and efficiency dropped from 52 - 59% to 30 - 52%. The performance drop is most likely caused by current compression due to thermal effects because of using a CW signal source to do the measurements. This effect is seen in the measured current waveform in figure 6.18, which shows a reduction in amplitude in the measured current compared to the simulated current measurement. Despite the measured results being lower than expected, they do indicate the final design can operate over a bandwidth of 1.95 – 3.1 GHz with an efficiency of 30%, which, while being shifted up in frequency, is an increase in fractional bandwidth from the simulations - 45% for the simulations to 53% for the measurements. The final measured results show the chip to be a promising design, and show the Continuous Class B theory can be implemented on a MMIC design at S-band.

Future work for this design would be to measure it under pulsed conditions to remove the thermal effects and see if the measured results better match the simulated results. Once this is done the results also need to be published. Also, investigation needs to be undertaken into why the performance increased when the line was replaced with an inductor. This investigation will need to look at the higher order harmonics and their influence on the broadband performance. Another area of investigation would be to consider

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the inductor structure and look for more ways to improve its Q and what else affects it, with the aim of recovering the bandwidth that was lost by the low Q .

Classical modes such as A, B and C all suffer poor back-off performance and as a result so do continuous modes - including the Continuous Class B design in Chapter 6. The Doherty is a topology that aims to improve back-off performance. Chapter 7 implements a Doherty design that was originally based on the Chalmers Doherty design [8]. This initial design had the same inductor issues as the Continuous Class B, where the matching lines had to be removed and the low Q of the inductors led to poor performance. This original design then changed away from the Chalmers Doherty design and focused on utilising the new device periphery of the GaN50 to its fullest to increase the bandwidth of the design by removing the need to impedance match the transistors. This final design was then manufactured and measured where it was seen that the efficiency peaked higher than the Continuous Class B design and the back-off was much improved over the Continuous Class B, but the bandwidth was lower but met specification and was 1.7 – 2.7 GHz. Future work for this design will be around increasing the band width further, which could involve incorporating Continuous Class B theory into the Doherty. Research around Doherty is also an active field, so parallel work that is ongoing should be considered for future investigations. Such as broadband matching techniques that could be applied to these 50 V GaN devices, such as [61], where two-point matching technique [62] was successfully used to extend bandwidth. Increased back-off was also required for LTE, which has been demonstrated using power controlling and matching techniques [63] and harmonic injection [64]. However, these methods require the addition of matching networks, which this work has tried to remove. A better method of extending the back-off would be to add more stages to help peak efficiency at increased back-off ranges, as seen in [65].

This work has presented how waveforms can be used to further increase the efficiency of HPAs. Firstly, by better understanding the underlining technology and failure mechanisms of transistors by measuring waveforms during a VSWR sweep and showing that the harmonic impedances can contribute

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to device failure if not properly characterised. Secondly, by introducing a new way to analyse the data measured, while forming a knee plot to allow deeper insight into how the knee affects the performance of a device, this allows high efficiency designs. Finally, two high efficiency quasi MMICs were designed, made and measured. One was the first Continuous Class B design to be done fully in the MMIC design space, the other was a Doherty that utilised the unique periphery of 50 V GaN devices to remove the need to use matching networks.

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APPENDIX

A

Using Waveform Engineering to
Understand the Impact of Har-
monic Terminations during 5:1
VSWR Stress Tests

Using Waveform Engineering to Understand the Impact of Harmonic Terminations during 5:1 VSWR Stress Tests

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Abstract—There are many applications where the operational environment of the antenna is challenging, which means its impedance can be highly variable, so the RF PA needs to be able to operate over a wide variety of loads without stress or failure. Assessing this is a key requirement of reliability testing, with VSWR sweeps being a typical way to test this durability. It is important to make sure the amount of information gained from these sweeps is maximized, so adding RF I-V waveform information can help give a more accurate view of what is occurring at the current generator plane. Also if the fundamental and second harmonic loads are systematically swept significant voltage stress, possibly not seen during the current conventional VSWR tests, is observed, which has implications in both the output matching network design and the current method of testing.

Index Terms—Failure Testing, HBT, Reliability Tests, VSWR, Waveform Engineering.

I. INTRODUCTION

In many wireless applications the operating environment of the antenna is uncontrolled, as a consequence the transmitting Radio Frequency (RF) Power Amplifier (PA) feeding this antenna must be able to operate, without stress or failure, into highly mismatched loads. A common way to test the reliability of a device under these conditions is the 5:1 Voltage Standing Wave Ratio (VSWR) stress test, where the device is stressed by sweeping the fundamental impedance around an optimum impedance. Clearly external transistor failure conditions can be observed with limited insight into the inner workings of the device, but the actual transistor operating conditions are not identified. As a consequence, 1) the level of voltage/current stress induced is unknown, and 2) the impact of the actual test conditions is unknown. Hence, this test does not ensure that the RF PA is robustly tested and any failure mechanisms identified and designed against to prevent unexpected failures in the field.

Previous papers have shown that there are five main breakdown mechanisms [1]-[3], some of which are linked; RF peak drain voltage/current, Unintentional reverse bias of Gate/Drain or Collector/Base diode, High RF Power, Bias Conditions and Temperature.

Without waveform information the first two failure mechanisms are not experimentally identified and so hard to diagnose using current techniques. Previous work also

showed that the fundamental and the harmonics can work together to effect the output waveforms [1] and so trigger different failure mechanisms. Clearly, a more systematic investigation of the impact of impedance mismatch, including the role of harmonics, on the level of voltage and/or current stress that the PA is subjected to is required.

II. DEVICE UNDER TEST

The device used in this investigation was a high power Heterojunction Bipolar Transistor (HBT), which was thermally bonded to a heat sink. HBT's are more prone to peak voltage failure, compared to their Field-Effect Transistor counterparts, which is why high voltage failure is of particular interest in this paper. The HBT in question was designed to run at 28V and with a breakdown voltage of 75V, but for these test studies it was run at 12V to ensure that no failures were caused during the investigations.

III. EXPERIMENTAL PROCEDURE

VSWR tests are used to mimic what might happen when the device under test has its output impedance changed un-expectedly, which is often caused by the antenna breaking or being placed on/near a ground plate. Using basic passive load pull systems, amplifier performance is typically analyzed by moving the fundamental away from the optimum; often with the harmonics free to move, uncontrolled, with the fundamental. It will be shown that this approach does not guarantee to fully mimic what could occur in the field. The impedance sweeps used for this study are shown in Fig. 1 where the fundamental is swept around a 5:1 VSWR mismatch contour and the second harmonic is independently swept around a unity circle, providing a comprehensive view of how the fundamental and second harmonic interacts.

Another weakness of classical load pull systems is that they only provide scalar performance parameters such as output power, gain and efficiency. The actual voltage and/or current values are not known and therefore if a device does fail there is no RF I-V information to help identify the source of the failure. This paper aims to show how the RF I-V information can help identify the cause of failures and so show there is a need to move to a more

advanced system that allows the RF I-V waveform information to be measured.

In this paper the VSWR test studies were done directly on the transistor with a system which allows the direct observations of the terminal RF I-V waveforms, along with active fundamental and second harmonic load pull to achieve the sweep patterns described above. Further details are provided in the remainder of this paper for specific situations.

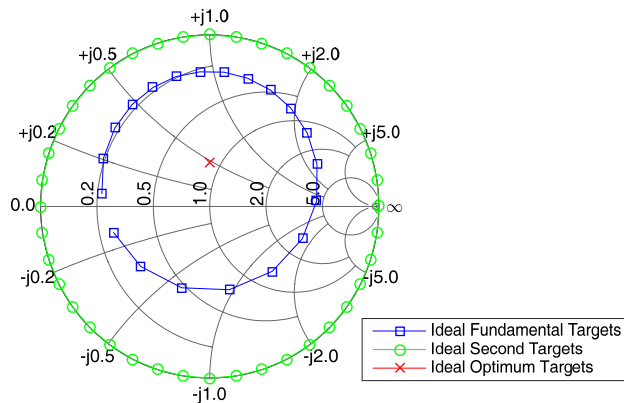


Fig. 1. Target locations of impedances during the combined fundamental 5:1 VSWR and second harmonic sweep, where the third was shorted

IV. EXPERIMENTAL OBSERVATIONS

A. Varying the Fundamental Alone

Consider first the results obtained doing just a fundamental VSWR sweep. In this case the second harmonic is held at a short circuit. The graph in

Fig. 2 shows the scalar performance parameter variations observed. This level of insight is identical to that obtained without waveform information. They show that the varying the fundamental load has a large effect on the DC power and a lesser effect on the RF output power. Hence the efficiency and dissipated power vary significantly. These results do show that there could be the potential for thermal stress or runaway should this test be re-done at 28V. While this information will allow design evaluations to be made, without RF voltage or current waveform information only speculations can be made as to how the fundamental mismatch is effecting the peak voltage or current and so reliability.

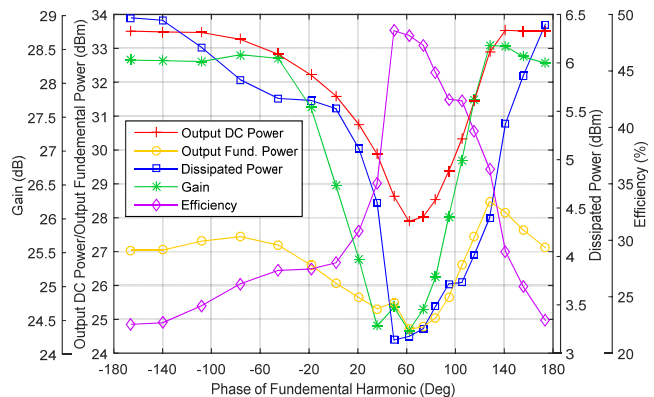


Fig. 2. Power/Efficiency/Gain vs. phase of Fundamental Harmonic, with the second and third shorted.

Consider now what can be learnt from interrogating the corresponding RF I-V waveform information. In Fig. 3, the Dynamic Load Lines (DLL's) are shown. These clearly highlight the effect of changing the fundamental load on the output waveforms. It is seen that the fundamental mismatch has a significant effect on the shape of the DLL's; the mismatch has a greater effect on increasing the peak RF current (100%), with reference to the optimum, than increasing peak RF voltage. Surprisingly the voltage's peak is only increased by $\approx 3V$ ($\approx 15\%$).

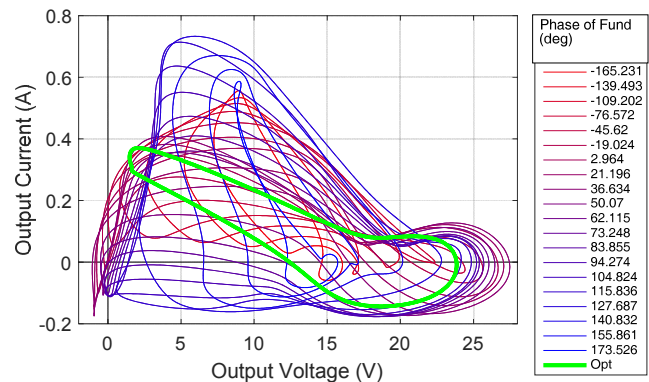


Fig. 3. DLL's of the fundamental VSWR

B. Combined Fundamental and Second Harmonic Sweeps

In this case a more advanced test is performed, both the fundamental and second harmonics were swept. The graphs in Fig. 4 and Fig. 5 show the scalar performance parameter variations observed. In this case these plots are laid out by plotting against the swept second harmonic (phase) and then each line represents each fundamental location.

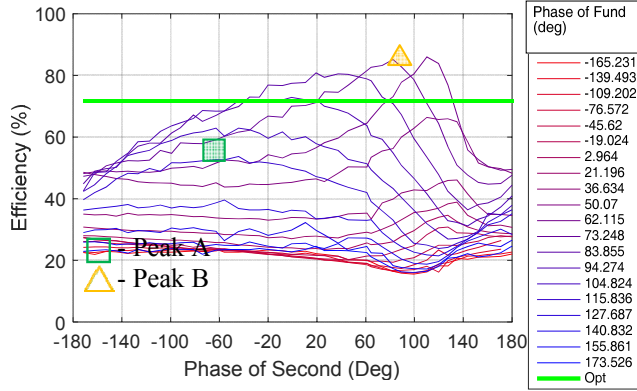


Fig. 4. Efficiency results from the combined sweep

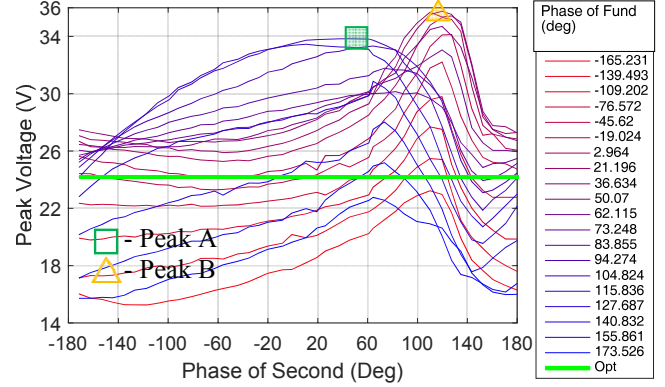


Fig. 6. Peak Voltage from results from the mixed sweeps.

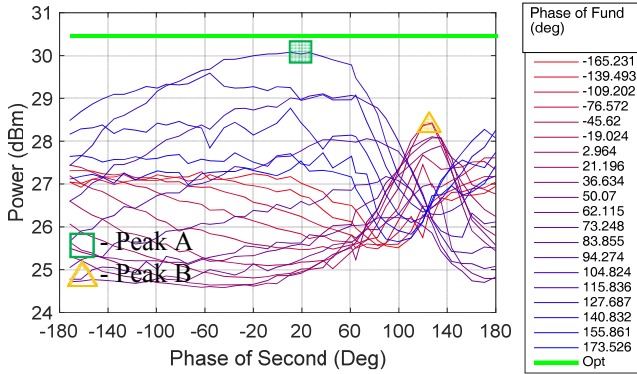


Fig. 5. Power results from the combined sweeps

These results show that certain combinations of fundamental and second harmonic loads (square and triangle on plots) can cause the RF performance to be increased as seen in the case of the efficiency, or nearly restored to the optimum in the case of the power. More importantly these locations correspond to an increase in the peak voltage as highlighted in Fig. 6.

Looking more closely at Fig. 6 it is seen that the peak voltage is increased up to 35.73V from 23.84V, which is a 50% increase, so scaling this up to 28V means that the peak voltage will be increased up to 82.42V, which is in excess of the 75V peak voltage rating of the device and hence potentially result in failure. Although looking at the output power this peak shows a decrease from optimum power, with an increase in efficiency, neither of which is inductive of failure.

The RF I-V waveform information is essential if the results from the VSWR sweeps are to be explained, without this waveform information the user would be unaware of the test conditions instigated. It is important that these peaking voltage conditions, which we will show can be associated with class J operation, are identified and included.

V. DISCUSSIONS

These results show that only sweeping the fundamental during a 5:1 VSWR does not necessarily cover all practical scenarios that may occur during the devices use in the field. It could very easily miss the impedance space that will cause significantly increased peak voltages. So to improve the detection of possible failure in the field it must incorporate the combined effects of fundamental and second harmonics, ideally with the addition of RF I-V waveform information.

The cause of these voltage peaks is the phase difference between the fundamental and second harmonic impedances providing the correct conditions to allow expansion of the RF voltage waveform. This process can be explained by referring to the Class B-J continuous mode literature [5]-[6], which predicts that there are a pairs of fundamental and second impedances that will trigger this process. Mapping these observed impedance locations to the intrinsic device current generator plane, as shown in Fig. 7, highlights their correlation with the class J conditions that would support the increased peak voltages and so recovery of output performance. The measured voltage increase in the output DLL's for these two pairs of points are shown in Fig. 8.

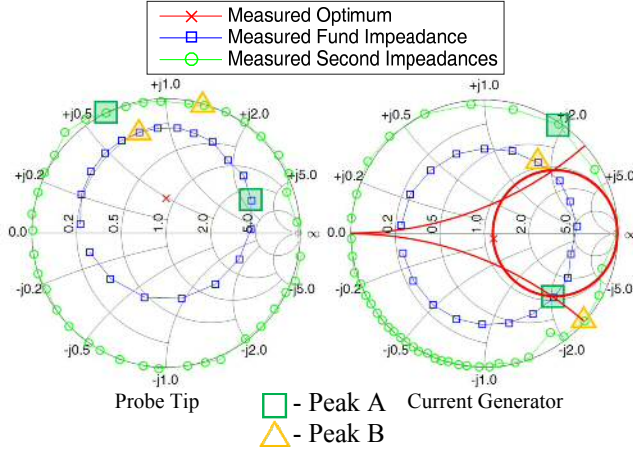


Fig. 7. Location of impedances causing the peak voltages. Left plot shows impedances seen at the probe tip, the right plot shows the same locations de-embedded down to the current generator plane, with loci identifying the Class-J locations

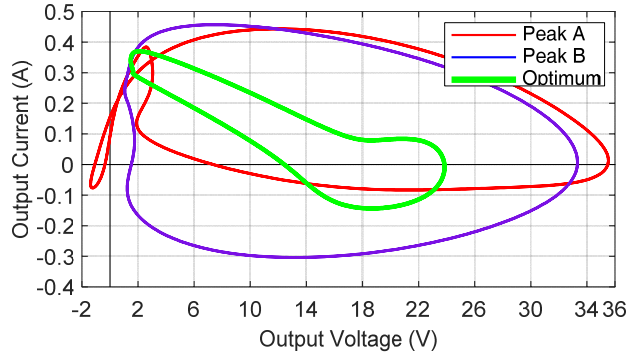


Fig. 8. Probe tip measurements of DDL's at the peak voltage locations.

VI. CONCLUSIONS

It has been experimentally shown that in order to ensure the transmitting RF PA is robust and has ability to operate reliably into highly mismatched loads, as could be expected in the field, then the impact of the harmonic impedance variations need to be incorporated into fundamental 5:1 VSWR stress tests. This is because it has been shown that there are pairs of mismatched fundamental and second harmonic impedances that cause the voltage to peak and so potentially stress the device under test. The location of these pairs can be explained by using the Class B to J continuous mode theory. This stress condition is only observable if I-V waveform measurements at the transistors terminal are done as a part of the 5:1 VSWR. These observations culminate to show the need to update the present stress testing scenarios and the output matching circuit design considerations for robust operation under impedance mismatch.

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B

**Design and characterization of
a 1.7–2.7 GHz quasi-MMIC Do-
herty power amplifier**

Design and characterization of a 1.7–2.7 GHz quasi-MMIC Doherty power amplifier

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Abstract—This paper presents the design and characterization of a Doherty power amplifier for small cells applications in the 1.7–2.7 GHz band. A quasi-monolithic realization is chosen for its cost advantages when compared to a fully-monolithic solution, and relies on GaN HEMT active devices, but passive networks realized on GaAs substrate. A lumped element Doherty combiner is designed to maximize the bandwidth at which the power amplifier shows high back-off efficiency that results higher than 37% in the 1.7–2.7 GHz band. The dual-input topology permits high flexibility in the optimization of performance, in particular in terms of bandwidth. The fabricated Doherty favourably compares to previously published power amplifiers.

Index Terms—Mobile communication, power amplifiers, gallium nitride.

I. INTRODUCTION

The pervasiveness of the mobile communication infrastructure is expected to grow constantly in the next years with the settling and advent of 4G and 5G technologies, respectively. The overall power consumption of the mobile networks will become a significant contributor to the worldwide energy demand, thus driving a large research effort in trying to maximize energy efficiency.

The high-frequency transmitters, and in particular the power amplifiers (PAs), of base-stations are identified as critical components from the power consumption viewpoint. For this reason, the Doherty PA [1] is widely adopted for its ability to maintain high power efficiency when amplifying high frequency, high peak to average modulated signals.

At the same time, the larger number of deployed base-stations to form complex heterogeneous networks will lead to lower output power levels (from hundreds to tens of watts). As a consequence, the integration in a single chip of the Doherty PA can be foreseen as a realistic and convenient choice.

In this framework, this paper presents the design and characterization of an integrated Doherty PA for the 1.7–2.7 GHz range, thus covering most of the LTE bands, and targeting an output power compatible with small cell base-stations. A quasi-monolithic microwave integrated circuit (q-MMIC) realization is chosen for its advantages in terms of cost if compared to a fully-monolithic solution. In particular, this design uses Qorvo's AlGaIn/GaN HEMT 0.25 μm high voltage technology, on SiC substrate, combined with Qorvo's IPC3 passive component process, on GaAs substrate. The IPC3 passive process features align well for use with GaN devices, including high breakdown capacitors and thick metal interconnects for peak current handling and low loss.

II. DESIGN

The active device parasitic and reactive effects play an important role in reducing the achievable bandwidth in any PA topology. Wide-band gap materials such as gallium nitride (GaN) can be operated at high drain voltage and have low parasitic capacitances per watt of output power. The high power and wide bandwidth potential of GaN HEMT devices is well documented [2]. However, in a Doherty PA, at least other two factors must be considered in broadband design: the impedance inverter and the main/auxiliary phase alignment.

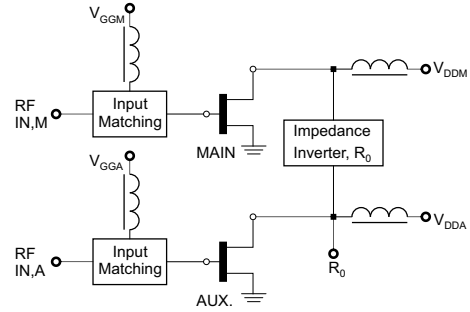


Fig. 1. Block scheme of the proposed Doherty PA.

The impedance inversion between the common node and the carrier device is a defining characteristic of the Doherty that allows to produce the correct load modulation. As firstly introduced in [4], a proper choice of the impedance inverter and common load equivalent impedances can lead to the optimization of the bandwidth with high back-off efficiency. In fact, as depicted in Fig.1, by choosing as equal to R_0 the impedance inverter and common load impedances, the impedance inverter does not introduce any bandwidth limitation at back-off. The application of this method requires some attention in the selection of drain bias voltages. To avoid an additional matching network on the auxiliary amplifier that would reduce bandwidth, it is necessary to select ideally $V_{DDA} = 2V_{DDM}$ that practically translates into a main device working at half its allowed bias voltage. This kind of reduction in the power utilization of the device is usually accepted in broadband PA design.

Phase alignment of currents from main and auxiliary branches is crucial to obtain the maximum output power at full drive. The dual-input or digital Doherty was introduced in [3], and allows for independent drive to the main and auxiliary inputs with different modulated signals. This added

degree of freedom can be exploited as beneficial on the PA bandwidth [4], and is adopted in the proposed DPA, see Fig. 1.

Once these general design guidelines are established, the specific implementation of the qMMIC Doherty uses other solutions to avoid bandwidth limitations and to minimize losses. The maximum output power can be estimated as $P_{MAX} = \frac{V_{DDA}^2}{2R_0}$: by using a 50 V GaN technology a $P_{MAX} = 25 W$ can be targeted without any additional output matching, i.e., $R_0 = 50 \Omega$. The integration of matching networks at base-station frequency has to rely on lumped elements to minimize the size of circuits. The impedance inverter can be ideally designed as a high-pass Π -network, where the shunt inductors are used for DC-feeding the two devices, and the series capacitance intrinsically decouples the main and auxiliary in DC. This choice is particularly convenient since it permits to avoid additional large DC-feed inductors with inherent low quality factor that leads to high losses. The output capacitance of the devices can be absorbed in the impedance inverter by re-tuning the shunt inductors. Similarly, the bond wires connecting the active devices to the passive network can be modelled through FEM simulations, and their effect absorbed in the inverter network. Regarding the input

relation to be set between the main and auxiliary inputs in order to obtain both reasonably flat gain and high back-off efficiency.

III. CHARACTERIZATION RESULTS

Fig. 3(a) shows a microscope picture of the qMMIC: total size is $5.2 \times 2.2 \text{ mm}^2$. The carrier plate has been fixed on a test fixture providing the DC supply, see Fig. 3(b).

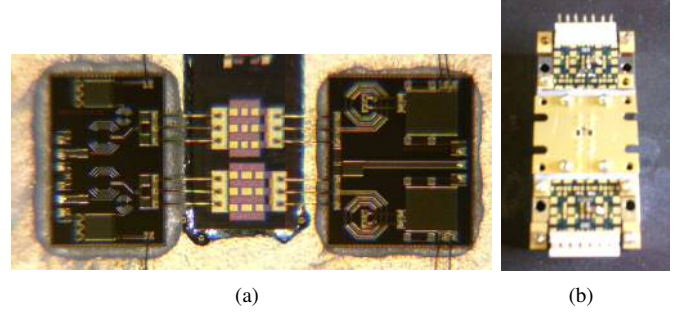


Fig. 3. Microscope picture of the fabricated qMMIC (a). Picture of the mounted test fixture (b).

As a first assessment, 2-port scattering parameters have been measured and compared with simulations. Port 1 is at the main input, port 2 at the output, while the auxiliary input is terminated with a 50Ω load. As indicated in Fig. 4 there is good agreement between measurements and simulations.

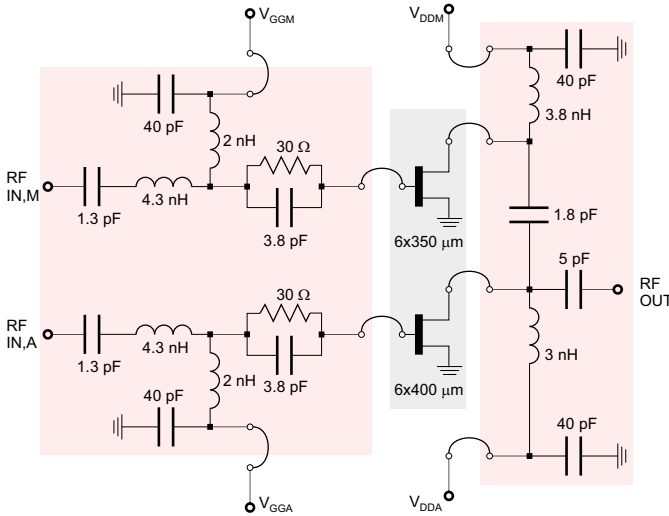


Fig. 2. Circuitual scheme of the designed Doherty PA.

networks, a lossy semi-lumped network has been selected to achieve simultaneous matching, gain equalization and broadband stabilization. The first by-pass capacitors, that influence the in-band behaviour, are integrated within the matching network substrates, while larger chip capacitors are bonded externally to the matching network for lower frequency by-pass. The RF ports are designed for wafer probing. The full schematic of the designed Doherty PA is shown in Fig. 2. The active devices have been chosen from a library of frequency-optimized FET layouts to meet the maximum current needs. Large signal simulations were performed using the foundry non-linear model and EM simulation of the matching networks to fine tune electrical response over the bandwidth. This also allowed an initial estimate of the correct phase and amplitude

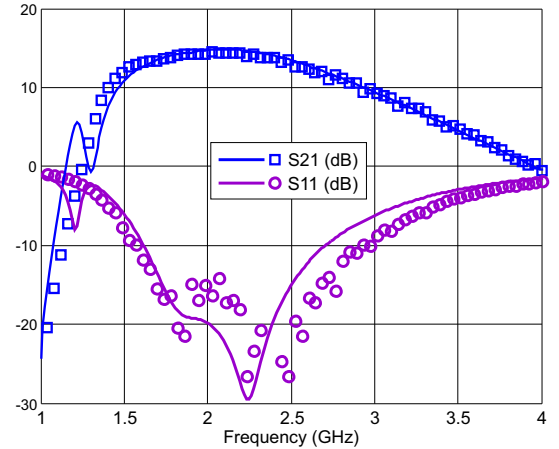


Fig. 4. Simulated (solid lines) and measured (symbols) scattering parameters. Auxiliary input is terminated. Bias: $V_{DDM}=28 \text{ V}$, $I_{DDM}=24 \text{ mA}$, $V_{DDA}=50 \text{ V}$, $V_{GGA}=-3.5 \text{ V}$.

CW measurements have been carried out using two separate sources for main and auxiliary, in order to have an arbitrary control on the phase and amplitude of the auxiliary input when referred to the main input. For low drive levels the auxiliary input is kept off, and then is gradually turned on at the expected 6 dB output back-off following the main input while trying to minimize gain compression. The phase is adjusted in order to maximize the output power for given amplitudes of main and auxiliary input levels. For this first

set of measurements, this operation was done manually, and was then used to create an initial look-up table for automated measurements. A similar procedure is used in the large signal simulation setup, and comparison between measured and simulated results at 1.9 and 2.3 GHz is shown in Fig. 5. It can be

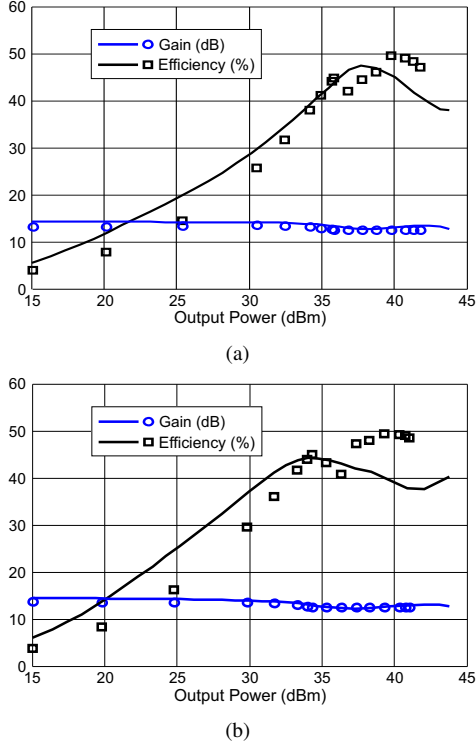


Fig. 5. Simulated (solid lines) and measured (symbols) CW power sweep results at 1.9 GHz (a) and 2.3 GHz (b), showing efficiency and gain vs. output power. Bias: $V_{DDM}=28$ V, $I_{DDM}=24$ mA, $V_{DDA}=50$ V, $V_{GGA}=-3.5$ V.

seen that the agreement is very good, except for the maximum output power achieved in CW measurements which is 1-2 dB lower than in simulation. However, future measurements using modulated signals will confirm if the expected output power of 25 W can be achieved instantaneously, with a much lower average power and reduced thermal issues. Modulated signal measurements will also be used to assess the “linearizeability” of the designed PA. Despite the thermal limitation met with CW measurements, the measured results are very promising, see Fig.6 resuming the main performance vs. frequency.

TABLE I
COMPARISON WITH PREVIOUSLY PUBLISHED DOHERTY PA ICs.

Ref.	Freq. (GHz)	$P_{OUT,MAX}$ (dBm)	η_{SAT} (%)	η_{OBO} (%)	OBO (dB)	Gain (dB)
[5]	2.14	40.5	60	52	7.1	16
[6]	2.14	41.2	57	43	4.7	20
[7]	0.75–0.77	39	46	37	7.2	46
[8]	2.1–2.7	41	n.a.	46	7.2	12
[9]	2.655	42.2	n.a.	47	7.1	31
This	1.7–2.7	40.2	42	37	6	12

The output power and 6dB back-off efficiency are higher than 40.2 dBm and 37%, respectively, on the whole band,

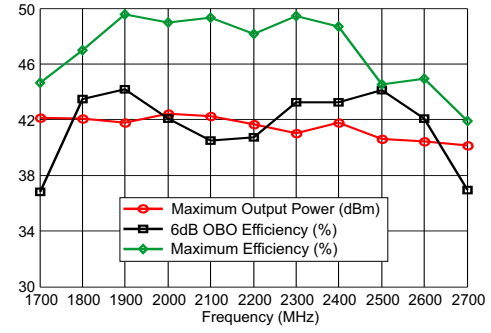


Fig. 6. Measured CW performance vs. center frequency. Bias: $V_{DDM}=28$ V, $I_{DDM}=24$ mA, $V_{DDA}=50$ V, $V_{GGA}=-3.5$ V.

with the latter higher than 40% on the reduced band from 1.8 to 2.6 GHz. According to these figures, the designed PA favourably compares to other extended bandwidth Doherty PAs previously published in the literature.

IV. CONCLUSION

The design and characterization of a broadband Doherty power amplifier, based on a quasi-monolithic realization, has been presented. The CW measured results can be considered as an advance in the state-of-the-art, and are in good agreement with the expected and simulated performance. Modulated signal measurements will confirm the achievable instantaneous peak power and test the linearity of the amplifier.

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