Buffer-Induced Current Collapse in GaN HEMTs on Highly Resistive Si Substrates

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Abstract—**We demonstrate that the highly resistive Si substrate in GaN-on-Si RF HEMTs does not act as an insulator, but instead behaves as a conductive ground plane for static operation and can cause significant back-gate-induced current collapse. Substrate ramp characterization of the buffer shows good agreement with device simulations and indicates that the current collapse is caused by charge-redistribution within the GaN layer. Potential solutions, which alter charge storage and leakage in the epitaxy to counter this effect, are then presented.**

Index Terms—**Current collapse, GaN buffers, high resistivity silicon, RF transistors, substrate ramps.**

I. INTRODUCTION

GAN-ON-SI technology is on course for rapid adoption in HEMT-based RF power amplifiers, with good performance and reliability having been demonstrated [1]–[3]. However, current collapse associated with reversible, slow negative charge trapping remains a concern for all GaN HEMTs. While the use of well-designed field plates and appropriate passivation strategies has reduced the effect of surface-induced current collapse [4]–[6], strategies to comprehend and minimize buffer-induced current collapse, especially given the different GaN epitaxial layer doping strategies (Fe, C, intrinsic defects) used to achieve high-resistivity RF buffers, remain an active research area [7], [8]. The use of conductive Si substrates for GaN-on-Si power devices has allowed a substrate voltage ramp technique to be used to infer the location and dynamics of charge trapping in the epitaxy [9], with deep depletion in moderately doped Si only observed at high fields when significant leakage occurs through the epitaxy [10]. In contrast, GaN-on-Si RF devices are normally fabricated on high-resistivity Si (HR-Si) substrates, with the expectation that the Si can be treated as an insulator and has minimal influence on electric field distribution in the epitaxy.

However, we demonstrate here that HR-Si acts as a ground plane for slow variations in bias, primarily due to carrier injection from the substrate. This results in the previously unrecognized fact that GaN-on-HR Si RF devices are significantly more susceptible to buffer-induced current collapse than those on insulating SiC. We observe negative charge storage, leading to current collapse, in the carbon-doped buffers of this work using the substrate bias technique. Device simulations based on a "leaky dielectric" model for buffer charge storage reveal that this is both qualitatively and quantitatively consistent with local charge redistribution within the epitaxy driven by the vertical field, rather than net vertical leakage [9]. Potential solutions to counter this effect are then discussed.

II. EXPERIMENTAL METHODS

AlGaN/GaN HEMTs were fabricated using a standard RF process flow on commercial epitaxial stacks from NTT-AT on 6"-diameter high-resistivity (>5 k$\Omega \cdot$ cm) Si substrates [11]. The stack consists of 2 μm strain-relief and C:doped (10^{19} cm^{-3}) GaN buffer, 250 nm of unintentionally doped (uid)-GaN channel layer, 1 nm AlN spacer, 25 nm of Al$_{0.2}$Ga$_{0.8}$N and 2 nm GaN cap. Transistors of width 2 × 125 μm, L$_G$ = 0.28 μm, L$_{SD}$ = 6 μm and L$_{SG}$ = 1 μm were used for this study (Fig. 1(a)). DC and pulsed-IV measurements (1 μs pulse width, 0.1% duty cycle), substrate ramp measurements (V$_{GS}$ = 0V, V$_{DS}$ = 1V, ramping V$_{SUB}$ from 0V to −50V) and RF measurements (large signal RF-IV Waveform Engineering system architecture based on a VTD SWAP-X402 receiver developed at Cardiff University [12]) under class B operation over a range of fundamental load impedances were performed.

Device simulations using Silvaco ATLAS employed a similar epitaxy with a 10 k$\Omega \cdot$ cm Si substrate of 10 μm thickness, C:doped linearly graded AlGaN strain relief layer and C:GaN buffer. The uid-GaN layer was assumed to have a shallow donor density of 5 × 10^{16} cm^{-3}, and the C:GaN and C:AlGaN layers, a deep acceptor level 0.9 eV above E$_V$ with a compensation ratio of 0.4 [13], [14]. Highly doped shallow source/drain contact regions were used in the uid-GaN, with Au gate and substrate contacts. No vertical leakage paths/shorts were implemented under the source/drain contacts, as has been used previously [9].

III. RESULTS AND DISCUSSION

A. Pulsed-IV and Load-Pull Measurements

A comparison of pulsed-IV output and transfer characteristics (Figs. 1(b, c)) for a representative 2 × 125 μm device from
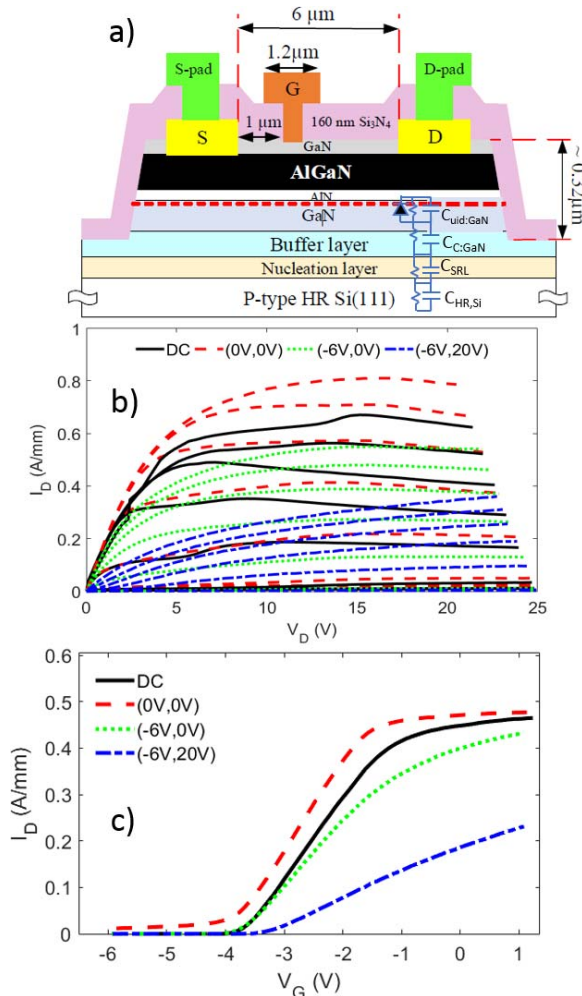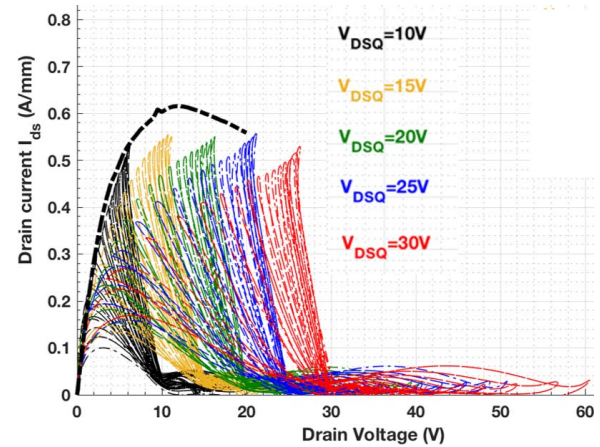
Fig. 1. (a) Device cross-section; also shown is the 1-D equivalent circuit between drain and substrate. DC and pulsed-IV (b) output characteristics (under the indicated quiescent bias points (V_G, V_D) for $V_G = -6V$ to $+1V$ in 1V steps) and (c) transfer curves ($V_D = 5V$) of a 2×125 μm transistor showing significant current collapse.

Fig. 2. RF fan diagrams of the 2×125 μm transistors under class B operation at 1 GHz for a range of fundamental impedances at 10V to 30V in 5V steps (dotted line indicates the DC-IV).

Fig. 3. (a) Substrate ramp measurements for GaN on HR–Si devices for sweep rates of 0.4, 4 and 25V/s. Dashed line indicates the ideal capacitance line and the loop traced indicates negative charge storage within the buffer. Vertical leakage was <5 μA (b) Device simulations of substrate ramps at 0.4, 4 and 25V/s showing good agreement with experiment. (c) Band diagram for the stack at -50V (point A in simulation) showing most of the voltage drops across the SRL, C:GaN and uid-GaN layer and not HR–Si. (d) Band diagram for the stack at 0V on the return sweep (point B) indicating exposed negative space charge at the top of C:GaN with corresponding positive charge at the top of the SRL.

different quiescent bias points clearly demonstrates current collapse. A 2-fold increase in R_{ON} and dramatic drops in g_m and I_{DSS} of 42% was observed by comparing quiescent biases of ($V_{GS} = 0V$, $V_{DS} = 0V$) and ($V_{GS} = -6V$, $V_{DS} = 20V$) without a major shift in V_{TH}, indicative of trapping in the drain access region. The source of such a current collapse would be a combination of surface and buffer effects whose separation is always difficult [5].
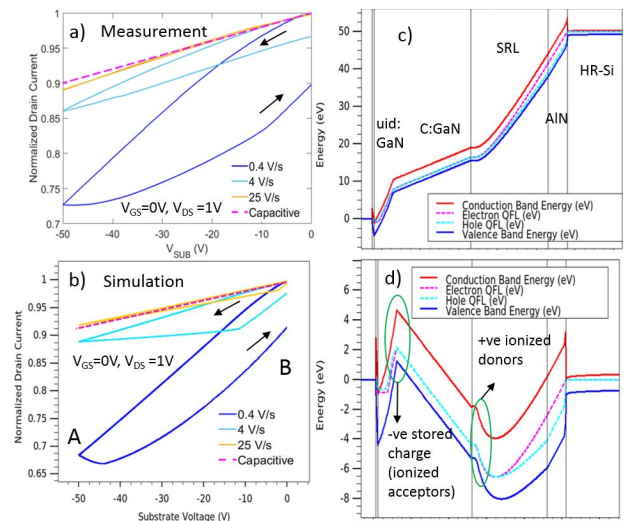
The impact of such a current collapse can also be seen in the RF performance of these devices. The RF-IV waveforms measured at 1 GHz for different bias conditions over a range of load impedances are transformed into RF dynamic load-line plots, $i_d(t)$ plotted versus $v_{ds}(t)$ to produce the results shown in Fig. 2. This plot, referred to as a "fan diagram", [15], [16] shows a clear DC-RF dispersion in current density. Furthermore, there is an increasing current collapse as drain bias increases from 10V to 30 V. The maximum output power obtained was 1.675 W/mm and a power added efficiency (PAE) of 59%.

B. Substrate Ramps for GaN-on-HR Si Substrates

Both the pulsed-IV and RF measurements apply a 2D electric field and are difficult to quantitatively interpret; so here

we use a substrate bias ramp to isolate the effect of buffer traps. Crucially this approach is surface insensitive due to the screening effect of the 2DEG and normally applies a 1-D vertical field allowing the direct measurement of the buffer component of trapping. In the case of GaN power devices on highly-doped Si substrates, the Si can simply be considered as a back electrode and the entire applied voltage drops across the epitaxy [9]. The validity of such an approach, however, needs to be tested for HR-Si substrates as the implicit assumption is that they are prone to deep-depletion effects even for static operation. We now show that this is not the case.

Fig. 3(a) shows a substrate ramp measurement for the same device, displaying the normalized drain current with substrate bias for 3 ramp rates. Also shown is the capacitive line corresponding to the epitaxial stack behaving as an ideal capacitor with a conducting Si ground plane. There are two key observations. Firstly, at low ramp rates (0.4V/s) the

conductivity falls below the capacitive line as discussed in the next section. Secondly, the normalized channel conductivity follows the capacitive line at fast ramp rates, with no evidence for deep-depletion even at 25V/s. The signature for deep depletion would be the drain current trace lying above the capacitive line due to an additional series capacitance from the substrate depletion layer (equivalent circuit in Fig. 1(a)). At low fields considered here (in contrast to those in studies such as [10], [17]) there is insignificant substrate leakage current and the resistivity of the nitride epitaxy is $>10^{10} \ \Omega \cdot$ cm, vastly higher than the Si, and hence a standard Si-MOS analysis applies [18]. Under the vertical field corresponding to positive drain bias, charge accumulation will occur at the top of HR-Si either as free electrons or interface charge, with the supply of electrons occurring by generation within the Si bulk or injection from substrate-contact/epitaxy. The thermal generation rate G_{th} is given by n_i/τ, where n_i is the intrinsic carrier density and τ, the carrier lifetime. Since HR-Si typically has $\tau > 1$ ms [19], the diffusion length of carriers $L_n > \sqrt{(D_n \tau)} = 1.9$ mm and almost all free electrons generated in the substrate bulk will be collected in the inversion region. The minimum ramp rate for observing deep depletion effects can be estimated as [20],

$$\frac{dV}{dt} \geq \frac{qG_{th}x}{C_{nitride}} = 4.4V/s \qquad (1)$$

where $C_{nitride}$ is the areal capacitance of the epitaxy. Substrate ramps below this rate should result in an inversion layer at the AlN/Si interface as previously seen for doped Si [21], [22], allowing the entire applied voltage to be dropped across the epitaxy and back-biasing the transistor under static operating conditions. However, the observed suppression of deep depletion at ramp rates of 25V/s, faster than predicted by (1) suggests this cannot be due to thermal generation in the Si alone. The simulation included generation, but also allowed injection of electrons from the substrate contact and this, rather than thermal generation, was found to be the primary source of electrons which form the Si inversion layer.

C. Negative Charge Storage in C:GaN Layers

HR-Si can therefore not be treated as an insulator under static operation, but in fact back-biases the epitaxial stack analogous to conductive Si for GaN power devices [9], [13], [23]. Substrate ramp measurements can hence probe the specifics of buffer charge storage even on HR-Si in contrast to conventional expectations. As shown in Fig. 3(a), at a ramp rate of 0.4V/s, channel conductivity initially follows the capacitive line but then drops below it with an increase in the back-gate transconductance. On the return sweep, the channel conductivity is lower than before, indicating negative stored charge in the buffer. Fig. 3(b) shows a simulation of the substrate ramp at 0.4V/s and is remarkably close to the experimental observation. The drop in current after returning to 0V is not due to a "net negative charge" in the epitaxy but arises from charge re-distribution within the C:GaN layer forming a dipole, and does not require current flow into the epitaxy from either the 2DEG or Si [9], [13]. The applied vertical electric field results in a localized current flow due to thermally generated holes within the C:GaN layer, generating a dipole with ionized acceptors at the top and exposed ionized donors at the bottom

resulting from the neutralization of acceptors. Because the Si acts as a ground plane, charges closest to the 2DEG will have a bigger impact on its density. Hence the negative charge of the dipole will dominate, reducing channel conductivity. Fig 3(c) shows the band diagram at point A with $V_{SUB} = -50V$ where field in the C:GaN layer is reduced (lower slope) as a result of the formation of the dipole. When the substrate bias is removed (point B, Fig. 3(d)), the stored space charge remains in place increasing the field under the 2DEG and reducing drain current. At faster sweep rates, the thermal generation rate of holes in C:GaN is insufficient to produce a significant dipole. This observation of negative charge storage is entirely consistent with the current-collapse in Figs. 1(b,c) and 2, demonstrating the presence of buffer-induced current-collapse in these devices.

D. Suppression of Back-Gating Effects

Countering the back-gate effect of HR-Si requires that the electric field is either screened or reduced. In GaN power switching HEMTs, screening of the field has been achieved by allowing a positively charged layer to form under the drain [9]. Several solutions to supplying the necessary holes have been suggested including injectors near the drain [24], [25] or by controlling the leakage properties of the reverse biased diode under the 2DEG [26], [27]. The latter approach has allowed the current-collapse to be reduced to a few percent at temperatures up to 150°C [28], and clearly this approach is also successful in RF GaN-on-Si devices which do not show significant bulk-induced current collapse [1], [2], [29], [30]. Alternatively, HR-Si offers the possibility to reduce the vertical field by ensuring that the Si is in deep depletion. This drops the net capacitance but requires a leaky epitaxy to sink injected charge from the Si. While the choice of silicon (n/p/n$^+$/p$^+$) has been recently shown to affect substrate depletion and leakage for GaN HEMTs [10], [17], this is less applicable to low-field operation and the highly-resistive Si used for GaN-on-Si RF devices considered here.

IV. CONCLUSIONS

HR-Si substrates are shown to act as a ground plane for GaN RF devices under static operation and result in a vulnerability to current collapse by back-biasing the epitaxial stack. This feature was exploited to measure and model buffer charge storage in GaN-on-HR-Si transistors using substrate ramps under a leaky dielectric framework, and the apparent stored negative charge was traced to charge-redistribution within the C:GaN layer. The previously unrecognized fact that Si acts as a ground plane, despite being highly resistive, means that in contrast to GaN-on-SiC devices where the substrate is insulating, measures need to be taken to control the resulting buffer induced current-collapse. Changes to the local leakage of the upper epitaxial layers are the most straightforward way of achieving this, while substrate deep depletion can also be ensured by making the entire epitaxy sufficiently leaky to allow suppression of inversion charge.

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