Pole Balancing and Thermal Management in Multi-Terminal HVDC Grids using Single H-Bridge Based Current Flow Controllers

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***Abstract*—Current flow controllers (CFCs) are power electronics based devices that may remove some technical barriers preventing multi-terminal HVDC (MTDC) grid deployment. In this paper, an inter-line CFC topology is investigated. The single H-bridge CFC (1B-CFC) alters the grid power flow by transferring power between neighboring dc lines. The operation and control of a 1B-CFC under a single modulation scheme is presented. A control strategy has been proposed to provide pole balancing support during imbalance conditions. Small-scale prototypes have been developed to demonstrate the functionality and operational range of the device. To this end, an experimental MTDC grid test-rig has been employed. It is shown that a 1B-CFC could be used to limit the dc line current and, additionally, it could be employed to enable asymmetrical tapping of dc lines. For completeness, the performance of the device has been experimentally validated under line overloading, pole imbalance conditions, and a pole-to-pole dc fault.**

***Index Terms*—Current flow controller, H-bridge, multi-terminal HVDC grids, voltage source converter.**

I. Introduction

MULTI-terminal HVDC (MTDC) grids constitute an enabling technology that will facilitate large-scale grid integration of renewables and cross-country energy exchange [1]. However, their deployment is still prevented by major technical challenges, such as grid protection, standardization and power flow control [2]–[4]. The current distribution within a meshed MTDC grid cannot be fully controlled and is determined by the grid's admittance matrix [5]. This lack of controllability of the branch currents (and hence branch power flow) creates challenges as the system increases in complexity; for instance, the power exchange at the dc nodes might need to be curtailed to operate within the dc cable thermal ratings.

Many research activities have taken place in recent years to address power flow regulation in dc grids [6]–[10]. Power flow management through converter control, although essential for the correct dc grid operation, offers limited flexibility and a reduced precision as the grid becomes more complex [11]. Alternatively, power flow can be regulated by auxiliary elements [12], which could be either connected in shunt (i.e. dc-dc converter/transformers) or in series. As reported in [13], [14], dc-dc converters achieve power flow control within a dc grid through the adjustment of the transformation ratio. Although dc-dc transformers have a great controllability over line power flow, their exclusive use for power flow regulation is not viable in terms of operational and capital costs. In contrast, a series current flow controller (CFC) is a power electronics device that provides dc line current regulation and thus thermal management with lower losses, maintenance and installation costs when compared to its shunt counterpart. Because series resistance of dc lines is relatively small, injecting a small portion of the line rated voltage in series with the line produces a significant current variation [15].

Although its adoption may improve the reliability and lifetime of HVDC cables, a CFC cannot completely prevent cable degradation as this process is influenced by operational and environmental conditions. Cable degradation in HVDC transmission systems may cause pole current imbalance, which is classified either as fast transient or slow drift [16]. Fast transients can be caused by severe cable damage and may require a fast-acting dc circuit breaker (DCCB). Conversely, slow drifts result from the different degradation rates between the positive and negative poles in cables, converter neutral current due to a floating potential point, or asymmetrical tapping of small loads. If an imbalance is caused by cable degradation or an asymmetrical load tapping, a star-point reactor can be installed at the ac side of the network to suppress the neutral current and, thus, to balance the positive and negative dc voltages [16]–[18]. Alternatively, a CFC can be used to eliminate pole imbalance from slow drifts by providing voltage compensation in series with dc poles.

Resistive-based CFCs regulate power flow by adjusting the effective resistance of a series-inserted resistor [15], [19]. However, the control flexibility of this topology is limited by the resistor's size. In addition, it exhibits high power losses. Such issues are avoided with voltage source based CFC configurations [11], [12], also known as power flow controllers, where power is exchanged between ac and dc points at the expense of requiring an ac connection to power up the devices—with major cost implications [20]. DC-powered (or inter-line) voltage source based CFC topologies, where power is exchanged between neighboring dc lines, have also been proposed [20]–[24]. Arguably, inter-line topologies provide a better solution in terms of footprint, losses and cost compared to ac-powered devices [20]. As a result, a number of dc-powered CFC variants have been suggested [25]–[29].

In this paper, a single H-bridge based inter-line CFC (1B-CFC) topology is investigated. The modeling, operation and control of the device are presented. An auxiliary scheme that provides pole balancing services irrespective of the pole con-

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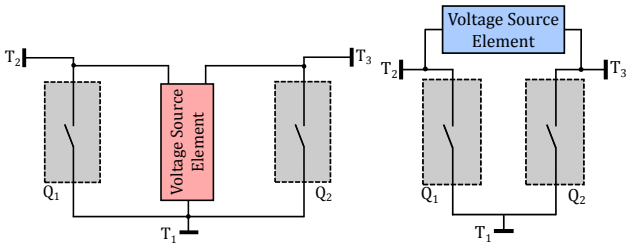
figuration is also introduced. Such supplementary controller may be employed upon imbalance conditions due to different cable degradation rates or asymmetrical tapping of dc cables. Simulations have been performed in MATLAB/Simulink to demonstrate the capabilities of the device to relieve line overloading and pole imbalances. Moreover, small-scale 1B-CFC prototypes have been designed and constructed. These have been employed in conjunction with an MTDC test-rig to validate the simulation results. For completeness, small-scale solid-state based DCCBs have been employed to experimentally assess the performance of a 1B-CFC upon dc faults.

II. Single H-Bridge CFC

In general, a CFC is composed of by-pass and voltage source elements and may be classified based on how these elements are arranged. A classification is proposed in Fig. 1. In Type I CFCs, the voltage source element is electrically coupled to all three terminals (T_1–T_3). In [21], a dual H-bridge based CFC (2B-CFC) was used to provide current regulation in a meshed MTDC grid. The voltage source in this device comprises two H-bridge modules and one capacitor. By modulating the H-bridges, the voltage source is inserted in series with either a single dc line or both. Switches Q_1 and Q_2 are used to by-pass the H-bridges when the required series dc voltage injection is zero.



(a) Type I (b) Type II

Fig. 1. Proposed classification of inter-line CFC module arrangements.

In a Type II CFC, the output CFC terminals (T_2 and T_3) associated with the dc lines are coupled by a voltage source (capacitor) and power electronics based by-pass elements are used to selectively connect the voltage source in series with either of the dc lines. However, as the voltage source is directly connected to the dc line terminals, the operation is limited to two quadrants as it cannot be discharged when line currents flow in opposite directions. An example of a Type II CFC was proposed in [29], [30], with the concept being experimentally validated in [31]. Unlike Type I devices, Type II CFCs can be easily integrated into the structure of DCCBs by utilizing the load-commutating switches. Such an approach reduces the total component count and footprint. It must be emphasized that the unidirectional topology presented in [30] could reduce the total component count by 33% compared to the simplified 2B-CFC topology reported in [24].

Additional power electronic switches may be included to unidirectional Type II CFCs to overcome operational limitations [30]. However, such an extended topology requires twice as many switches compared to a conventional 2B-CFC. Conversely, the 1B-CFC, shown in Fig. 2, extends the operation of Type II CFCs to all four quadrants while maintaining the total switch count of a 2B-CFC. It uses an

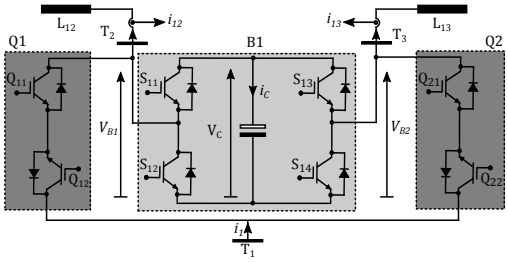


Fig. 2. Topology of 1B-CFC.

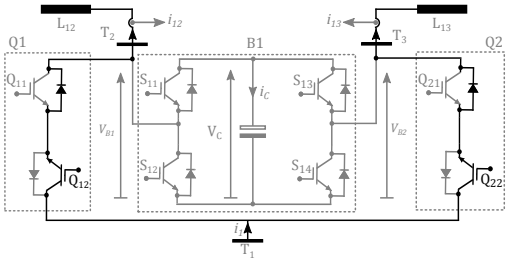
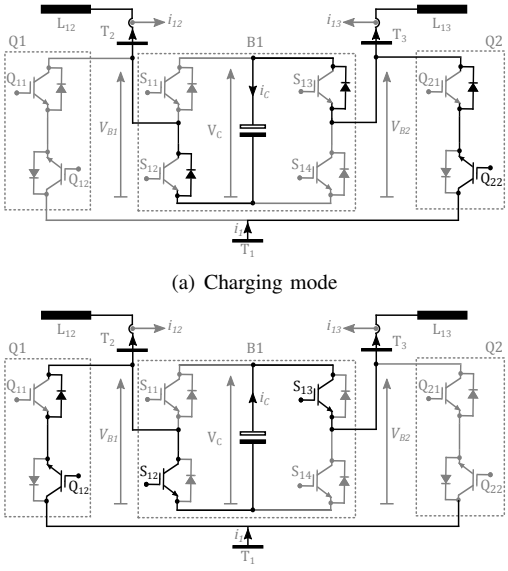


Fig. 3. By-pass mode for the 1B-CFC.



(a) Charging mode

(b) Discharging mode

Fig. 4. Operational stages of a 1B-CFC in CC mode.

H-bridge B_1 electrically coupled with a capacitor between by-pass switches Q_1 and Q_2. Each switch is composed by two anti-series connected IGBTs. The H-bridge input terminals are connected to T_1 and T_2. A dc voltage is established on the capacitor to provide a voltage source for current flow control.

A. Operation

1) By-pass Mode: The inserted dc voltages in series with dc lines L_{12} and L_{13} are zero. To achieve this, the duty cycles of Q_1 and Q_2 are set to 1 to by-pass B_1 (see Fig. 3).

2) Current Control (CC) Mode: Q_1, Q_2 and B_1 are modulated to provide dc voltage injections in series with L_{12} and L_{13}. This enables to increase or decrease the line impedances and, consequently, alter their current flow.

Let the current be flowing from terminal T_1 to terminals T_2 and T_3. It is desired to reduce the current flow in L_{12}. To achieve this, switches Q_{12} of Q_1, Q_{22} of Q_2, and S_{12} and S_{13} of bridge B_1 are modulated, while the remaining switches (Q_{11}, Q_{21}, S_{11} and S_{14}) are kept turned off. Q_{12} and Q_{22}

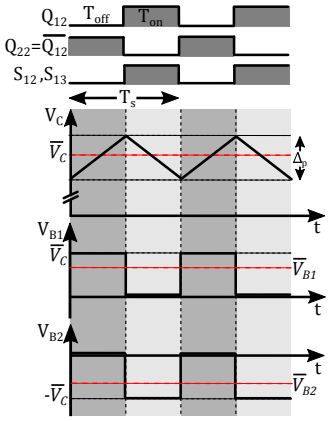


Fig. 5. Switching waveforms of a 1B-CFC under CC mode.

are complementarily modulated to avoid interruptions in the current flow i_1 of the converter (from T_1).

The operational stages of the 1B-CFC during the CC mode are shown in Fig. 4. The corresponding states of the controlled switches and changes on the bridge voltages are shown in Fig. 5. When Q_{12}, S_{12} and S_{13} are off (*i.e.* Q_{22} is on), line current i_{12} flows through Q_2 and the naturally commutated diodes of bridge B_1 (see Fig. 4(a)); this charges the capacitor rapidly. During this period, the voltage across T_1 and T_2 becomes the capacitor voltage V_C, while it is zero across T_1 and T_3. Thus, i_{12} decreases. If there are no changes in power demand or in the voltage references, the total current out of T_1 remains unchanged. This implies that current i_{13} in L_{13} must increase to maintain the current balance. The inserted dc voltages V_{B1} and V_{B2} can be expressed as follows:

$$V_{B1,\text{off}} = \overline{V}_C, \quad V_{B2,\text{off}} = 0, \tag{1}$$

where $\overline{V}_C$ is the average value of V_C.

A negative voltage must be inserted in series with L_{13} to increase its current i_{13}. This is done by switching on Q_{12}, S_{12} and S_{13} (see Fig. 4(b)). During this period the capacitor is discharged into L_{13}. The inserted voltages V_{B1} and V_{B2} are:

$$V_{B1,\text{on}} = 0, \quad V_{B2,\text{on}} = -\overline{V}_C. \tag{2}$$

As shown in Fig. 5, continuous switching of the by-pass and the H-bridge switches generates a pulsed positive dc voltage V_{B1} across the CFC terminals T_1 and T_2, which decreases i_{12}, and a pulsed negative dc voltage V_{B2} across T_1 and T_3, which increases i_{13}. The average bridge voltages $\overline{V}_{B1}$ and $\overline{V}_{B2}$ can be derived from (1)-(2) as:

$$\overline{V}_{B1} = \frac{V_{B1,\text{off}}T_{\text{off}} + V_{B1,\text{on}}T_{\text{on}}}{T_s} = \frac{\overline{V}_C T_{\text{off}}}{T_s} = \overline{V}_C(1-D), \tag{3}$$

$$\overline{V}_{B2} = \frac{V_{B2,\text{off}}T_{\text{off}} + V_{B2,\text{on}}T_{\text{on}}}{T_s} = \frac{-\overline{V}_C T_{\text{on}}}{T_s} = -\overline{V}_C D, \tag{4}$$

where D is the duty cycle of switches Q_{12}, S_{12} and S_{13}; T_s the switching period; and T_{on}, T_{off} the turn-on and turn-off times of the same switches.

In steady-state, the peak-to-peak ripple voltage Δ_p on the capacitor voltage V_C can be calculated as

$$\Delta_p = i_{12} \cdot \frac{T_{\text{off}}}{C_{\text{CFC}}} = i_{13} \cdot \frac{T_{\text{on}}}{C_{\text{CFC}}}. \tag{5}$$

Given that the power taken from one line is equal to the power added to the other line, the power balancing between switches Q_1 and Q_2 is given by:

$$\overline{V}_{\text{B1}} i_{12} + \overline{V}_{\text{B2}} i_{13} = 0 \;\Rightarrow\; \overline{V}_{\text{C}}(1-D)i_{12} - \overline{V}_{\text{C}} D i_{13} = 0. \tag{6}$$

B. Controller Design

A single modulation scheme, shown in Fig. 6, is used for the 1B-CFC control [21]. It consists of a nested structure where an outer loop regulates dc line current by generating a reference signal $V_{C,\text{ref}}$ to the inner capacitor voltage loop. The scheme in this section regulates the current through line L_{12}, with the impact of line L_{13} being considered as a disturbance.

Let the overall transfer function of an uncompensated 1B-CFC system $G_v(s)$ be defined by

$$G_v(s) = K_c \left(\frac{L_{eq}s + R_{eq}}{L_{12}s + R_{12}}\right) \cdot \left(\frac{1}{L_{13}Cs^2 + R_{13}Cs + 1}\right), \tag{7}$$

where L_{12}, R_{12} represent the inductive and resistive parts of dc line L_{12}; L_{13}, R_{13} for L_{13}; C the CFC capacitor; $L_{eq} = L_{12} + L_{13}$; and $R_{eq} = R_{12} + R_{13}$. $G_v(s)$ relates the capacitor voltage V_C (output) to the duty cycle D and was obtained using block diagram reduction techniques. Fig. 7 shows the open loop frequency response of $G_v(s)$ given the parameters provided in Table I. As it can be observed, the uncompensated system exhibits a poor phase margin (≈ 4 deg). The following controller is proposed to ensure an adequate closed-loop transient performance:

$$G_k(s) = K\left(\frac{s+z_c}{s+p_c}\right)\left(\frac{s+z_p}{s}\right). \tag{8}$$

$G_k(s)$ is a PI controller cascaded with a lead compensator, where z_p is the zero of the PI, z_c and p_c are the zero and pole of the compensator, and K is the overall controller gain. A suitably designed $G_k(s)$ ensures the elimination of the steady-state error through the integral action of the PI controller and, as also shown in Fig. 7, improves the overall system performance during transients through the phase margin increase afforded by the lead compensator.

Bandwidth separation is used to ensure a good performance of the control scheme. Assuming that the outer loop is ten times slower than the inner loop, the latter can be represented by a unit gain. Thus, the outer loop plant can be simplified to

$$G_i(s) = \frac{1}{L_{12}s + R_{12}}. \tag{9}$$

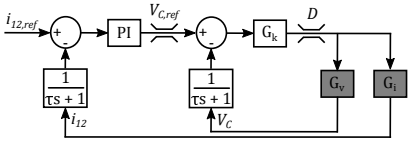


Fig. 6. 1B-CFC controller.

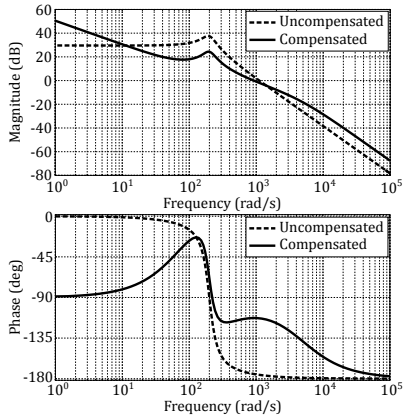


Fig. 7. System open loop frequency response (Bode plot): Uncompensated system $G_v(s)$ and compensated system $G_k(s)G_v(s)$.

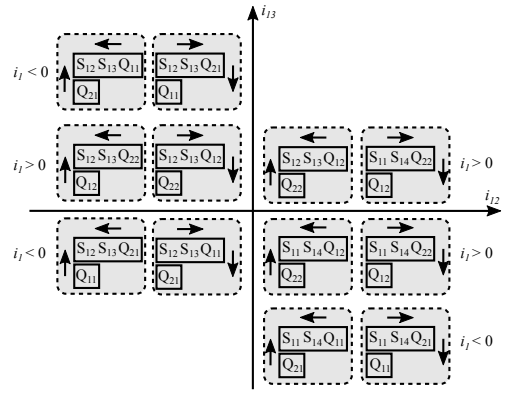


Fig. 8. 1B-CFC switch selection in CC mode.

A PI controller is used to regulate line current. To eliminate measurement noise, a 1st order filter with a cut-off frequency of 200 Hz has been used with the voltage and current controllers. All control parameters can be found in the Appendix.

Note: Although frequency dependent models are arguably the most accurate representation of cables, the controller design discussed in this section considers dc lines as simple RL sections where the cable capacitance is neglected. The rationale behind this approach is to enable consistency between simulation and experimental work. Since, the cable capacitance is shunt-connected, its effect on a series-connected CFC could be deemed as negligible. However, this has been considered as a disturbance to the system for completeness.

Fig. 8 shows the 1B-CFC switch selection under single modulation control. Switching patterns are given for four quadrant operation, where the quadrants and switching sequence are determined by the direction of currents i_{12}, i_{13}, i_1. An increment or decrement in bridge currents is represented by the arrow direction. The horizontal arrow represents a change in line current i_{12}, while the vertical arrow in i_{13}. In CC mode, four switches are modulated to provide current control. For instance, when i_{12}, i_{13}, and i_1 are positive, switches Q_{12} of Q_1, Q_{22} of Q_2, and S_{12} and S_{13} of bridge B_1 must be modulated to decrease the current on line L_{12}. Q_{12}, S_{12} and S_{13} are switched simultaneously while a complementary gating pulse triggers Q_{22}. Conversely, to increase the current on line L_{12}, Q_{22}, S_{11} and S_{14} are modulated simultaneously while a complementary gating pulse triggers Q_{12}.

C. On the Use of Multiple CFCs

In a large network incorporating multiple CFCs, the use of communication-free control schemes solely based on local measurements could lead to control conflicts between the CFCs. Since the required amount of series dc voltage compensation for current control is affected by the CFC location, a CFC with a low dc voltage requirement must be selected to reduce system losses and the stress levels on the device when more than one CFC is available. When multiple CFCs are used, a hierarchical control system is essential to enhance grid reliability and performance by coordinating their operation to optimize the required dc voltage compensation. Fig. 9 shows such control system. It consists of a centralized remote control centre (RCC) along with multiple local controllers (LCs). The RCC determines the status of each CFC prior to a scheduled power change, energy trade or system maintenance. Each LC has the cascaded control structure described by Fig. 6.

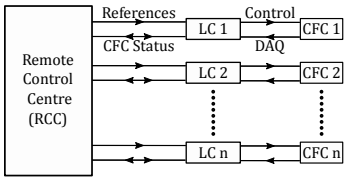


Fig. 9. CFC hierarchical control.

It should be highlighted that in droop-based MTDC systems, a CFC could alter the power sharing between dc terminals. Therefore, the operation of CFCs and VSCs must be carefully coordinated though a centralized controller that adjusts voltage and power references to compensate the effect of CFCs on grid power flow [32]. A centralized controller is composed, in general, by a secondary level controller which steers the MTDC grid towards its desired operating point and a tertiary level controller which minimizes grid losses and ensures its safe operation following the loss of any component. In the event of an unscheduled current regulation or upon communication failure, a local measurement-based control scheme, as proposed in [31], could be adopted to minimize terminal power deviations. Furthermore, as reported in [33], operation between multiple CFCs can be coordinated (under communication loss) through establishing pre-assigned control objectives (i.e., modes of operation) among the active CFCs.

III. Pole Imbalance Control

A 1B-CFC may be used to remove a dc pole imbalance i_m caused by slow drifts. This can be calculated as:

$$i_m = (i_{ab,+} - i_{ab,-}) \cdot 100\%, \tag{10}$$

where $i_{ab,+}$ and $i_{ab,-}$ are per-unit values of the positive and negative pole line currents of line L_{ab}, respectively. The current imbalance ratio Δ_i in the dc poles is calculated as:

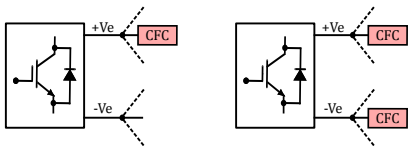
$$\Delta_i = \tfrac{i_m}{2}. \tag{11}$$

To achieve pole balancing, positive pole currents must be compensated by $-\Delta_i$ and negative pole currents by Δ_i.

Fig. 10 shows two CFC circuit arrangements for a dc grid. A uni-pole compensation scheme (Fig. 10(a)) is implemented by placing a CFC either at a positive or at a negative pole. Such a configuration is recommended for asymmetrical pole tapping only, where a single pole is compensated. To avoid imbalance between poles, a dual-pole compensation scheme should be adopted, with a CFC placed in each pole (Fig. 10(b)). Uni-pole compensation may be also achieved with a dual-pole compensation scheme if one CFC is by-passed.

Note: Pole balancing in the context of this paper means equalizing the distribution of injected currents within the positive and negative pole networks. It is not balancing of the pole currents injected at a bus as this is controlled by the terminal converters—where the CFC has no influence over. In meshed dc grids, series tapping could significantly affect the pole current distribution as it alters the cable impedance. In some cases, this may reduce the current through the tapping converter and, therefore, the desired power cannot be exported. Furthermore, series tapping could increase the grid power losses as the current is forced to flow via long cables. This can be overcome by using a 1B-CFC (or any CFC configuration) to offset the series voltage compensation by the tapping

converter. Although in this paper the discussion has been centered around a symmetrical monopole configuration, the pole balancing service could be extended to bipole topologies—however, this requires further investigation which falls out of the scope of this work.



(a) Uni-pole (b) Dual-pole

Fig. 10. CFC circuit arrangements in a dc grid.

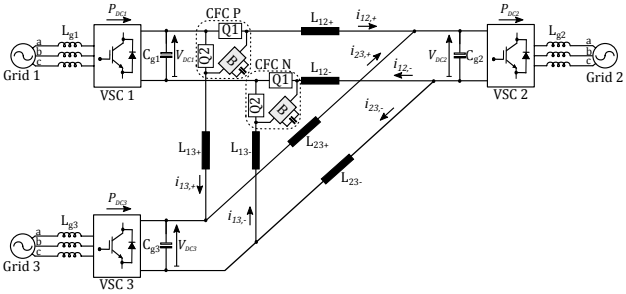


Fig. 11. Three-terminal MTDC grid with embedded 1B-CFCs.

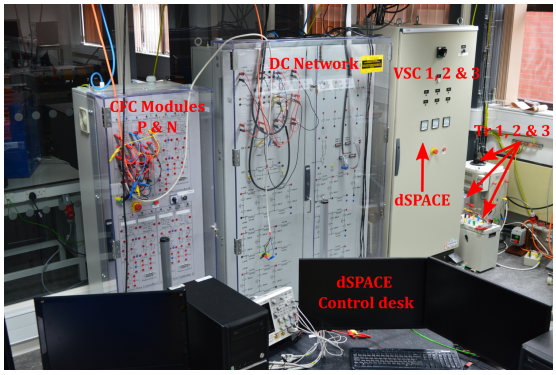
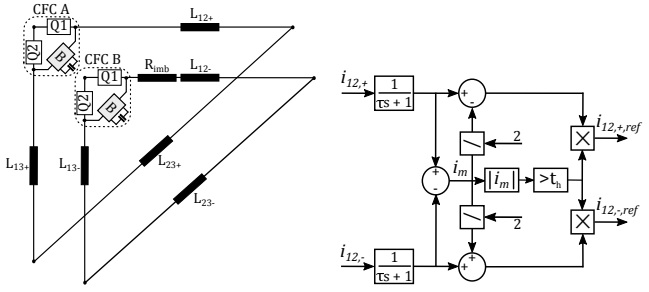


Fig. 12. Experimental setup.



(a) (b)

Fig. 13. (a) DC grid and CFC modules arrangement during pole imbalance. (b) Pole imbalance controller.

IV. MTDC Configuration and Control

To validate the operation and control of the 1B-CFC, a three-terminal MTDC grid is used (see Fig. 11). The VSCs have a two-level topology. Fig. 12 shows the experimental setup of the MTDC test-rig with embedded 1B-CFC prototypes. Specifications are provided in Tables I and II. The VSC terminals have been arranged in a symmetrical monopole configuration. Dual-pole compensation is afforded by placing CFC modules P and N in series with the positive and negative poles of lines L_{12} and L_{13}. A switching frequency of 2000 Hz is used to modulate the CFCs' switches. Each VSC is connected to an ac system through a phase reactor and a transformer. Autotransformers connected to the 415 V ac power supply represent the ac grids. A dSPACE system (DS1005/Control Desk 3.2) system is used to enable real-time operation and to control the test-rig and the CFCs.

It must be emphasized that the low voltage test-rig adopted in this paper cannot be considered as the electrical equivalent of a high voltage system. Despite the differences in operating voltages, the experimental platform closely represents the key characteristics of an HVDC grid. This is evidenced by the close correlation between simulation and experimental results presented in Section V.

TABLE I
SPECIFICATIONS AND PARAMETERS OF THE TEST-RIG

Devices	Specifications	Operating Rating
VSCs	Rated power Rated ac and dc voltage Topology	2 kW 140 V, ±125 V Two-level, symm. monopole
AC inductors	L_{g1}, L_{g2}, L_{g3}	2.2 mH
DC lines	L_{12}, L_{13}, L_{23} R_{12}, R_{13}, R_{23} (equiv.)	2.4 mH, 5.8 mH, 11.8 mH 0.26 Ω, 0.78 Ω, 0.98 Ω
DC capacitors	C_{g1}, C_{g2}, C_{g3}	1020 μF

TABLE II
SPECIFICATIONS AND PARAMETERS: 1B-CFCS

Devices	Specifications	Operating rating
CFC	Rated power and dc voltage	40 W, 5 V
DC capacitor	C	4400 μF
Switching frequency	f_{sw}	2000 Hz

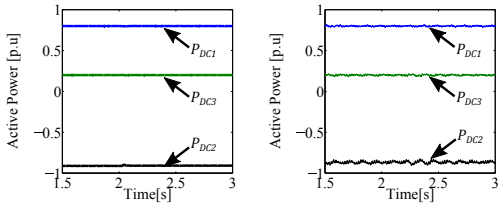
V. Simulation and Experimental Validation

Results in this section are expressed in per unit using the following bases: 2 kW, 125 V, and 8 A. VSCs 1 and 3 initially inject 0.8 and 0.2 p.u. of active power into the MTDC grid respectively, while VSC 2 is a slack busbar that maintains grid power balance by setting a constant dc voltage. To perform the simulations, the system in Fig. 11 was constructed in Simulink. The experimental validation is performed with the test-rig shown in Fig. 12.

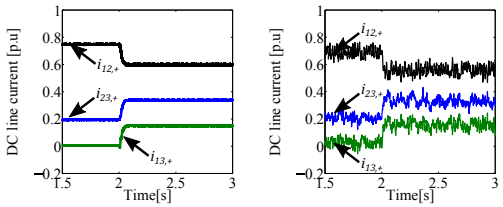
A. Pole Balancing – Dual-pole Compensation

In this test case, CFCs are used to provide support during imbalances due to series tapping. Fig. 13 shows the configuration of the test network. A resistor $R_{\text{imb}} = 0.6\ \Omega$ is connected in series with $L_{12,-}$ to represent a series tap converter inducing an imbalance i_m. Fig. 13(b) shows the block diagram of the reference calculator for a dual-pole compensation. The controller provides support if i_m exceeds the threshold value $t_h = 5\%$ (refer to the block diagram in Fig. 13(b)).

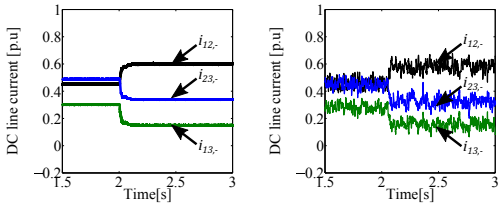
The MTDC grid responses are shown in Fig. 14. Initially, both CFCs are by-passed through switches Q_1 and Q_2. An imbalance $i_m = 25\%$ is observed between the poles in the experimental results. However, this value raises to $i_m = 30\%$ in simulations as a fixed diode voltage drop was assumed.



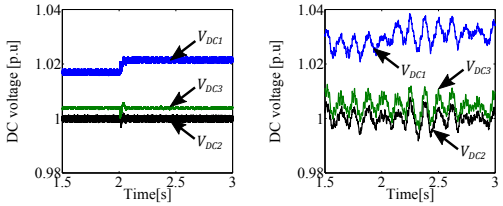
(a) VSC active power



(b) dc line current (positive pole)



(c) dc line current (negative pole)



(d) dc terminal voltage

Fig. 14. DC grid response during dual-pole balancing: Simulation (left) and experimental (right) results.

At $t = 2$ s, both CFCs are enabled and requested to set line current references $i_{12,+,\text{ref}}$ and $i_{12,-,\text{ref}}$ as follows:

$$\text{Experiment}: i_{12,+,\text{ref}} = i_{12,+} - \frac{\Delta_i}{100} = 0.7 - 0.125 = 0.575 \text{ p.u.}$$

$$\text{Simulation}: i_{12,+,\text{ref}} = i_{12,+} - \frac{\Delta_i}{100} = 0.75 - 0.15 = 0.6 \text{ p.u.}$$

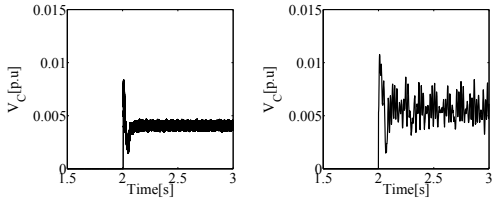
$$\text{Experiment}: i_{12,-,\text{ref}} = i_{12,-} + \frac{\Delta_i}{100} = 0.45 + 0.125 = 0.575 \text{ p.u.}$$

$$\text{Simulation}: i_{12,-,\text{ref}} = i_{12,-} + \frac{\Delta_i}{100} = 0.45 + 0.15 = 0.6 \text{ p.u.}$$

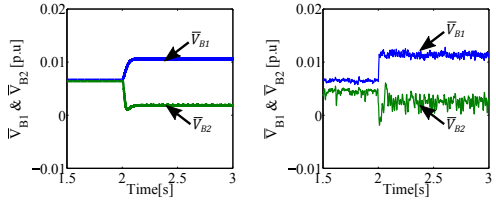
where, according to equation (11), $\Delta_i = \frac{i_m}{2}$, and $\Delta_i = 12.5\%$ for the experiment and $\Delta_i = 15\%$ for the simulation.

Following the activation of the imbalance controller, $i_{12,+}$ and $i_{12,-}$ are measured at 0.5756 p.u. and 0.5757 p.u. respectively; i.e. the imbalance has reduced below 0.01%. The additional voltage drop due to series tapping reduces the current through the negative pole of Line 12 from 0.7 to 0.45 p.u. During this period, a total power of 0.1215 p.u. is exported (dissipated). Following the activation of the CFC, current though Line 12 increases to 0.6 p.u. and, thus, a total power of 0.216 p.u. is exported. This demonstrates that a CFC could be used to increase the power though a series tap when the tapping device is operated at its maximum voltage.

Figs. 15 and 16 show the voltage profiles of the CFCs. In the experiment, the capacitor voltages are regulated to

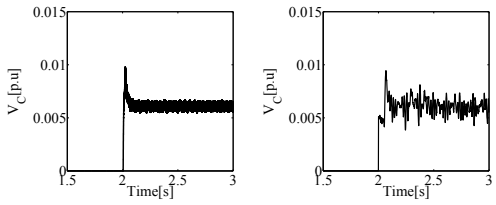


(a) capacitor voltage

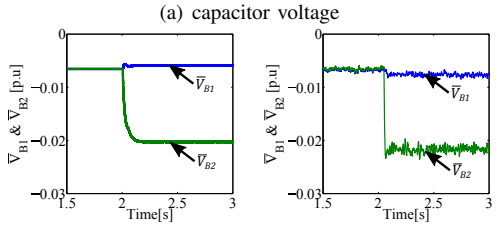


(b) inserted average dc voltages

Fig. 15. Response of the CFC located at the positive pole during dual-pole balancing: Simulation (left) and experimental (right) results.

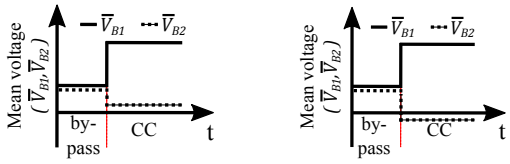


(a) capacitor voltage



(b) inserted average dc voltages

Fig. 16. Response of the CFC located at the negative pole during dual-pole balancing: Simulation (left) and experimental (right) results.



(a) (b)

Fig. 17. Inserted mean voltage in CC mode: (a) positive voltage injections; (b) complementary injection.

0.006 p.u., whereas in the simulations the values are different for each CFC: 0.004 p.u. for the positive and 0.006 p.u. for the negative pole (Figs. 15(a) and 16(a)). The mismatch is attributed to the semiconductor on-state voltage drop—resulting in different line current distributions. Figs. 15(b) and 16(b) show the average voltage injections in series with the positive and negative pole lines.

In scaled systems, the forward voltage drop on semiconductor switches imposes a significant challenge as it may be sufficient to modify the line current flow. Typically, power diodes exhibit an on state forward voltage drop of 0.7-1 V. During CC mode, a maximum of three diodes are inserted into the conduction path during the capacitor charging mode, resulting in a drop between 1.6-2.5 V. By taking the diode forward voltage V_f into consideration, (3) and (4) can be

modified as follows:

$$\begin{aligned}\overline{V}_{B1} &= \frac{V_{B1,\text{off}}T_{\text{off}} + V_{B1,\text{on}}T_{\text{on}}}{T_s} \\ &= \frac{(3V_f + \overline{V}_C)T_{\text{off}} + V_f T_{\text{on}}}{T_s} \\ &= (3V_f + \overline{V}_C)(1-D) + V_f D\end{aligned} \tag{12}$$

$$\begin{aligned}\overline{V}_{B2} &= \frac{V_{B2,\text{off}}T_{\text{off}} + V_{B2,\text{on}}T_{\text{on}}}{T_s} \\ &= \frac{V_f T_{\text{off}} + (V_f - \overline{V}_C)T_{\text{on}}}{T_s} = V_f - \overline{V}_C D,\end{aligned} \tag{13}$$

Equation (13) shows that $\overline{V}_{B1}$ is always greater than zero for the given point of operation. Conversely, $\overline{V}_{B2}$ could either be positive or negative.

Theoretically, if the diode voltage drop is zero (neglected in a high voltage system), when current flows from T_1 to T_2 and T_1 to T_3 (i.e. currents i_{12} and i_{13} are positive), the inserted dc voltages should have opposite polarities to satisfy the power balance between the bridges, where $\overline{V}_{B1} > 0$ and $\overline{V}_{B2} < 0$ (Fig. 17(a)) or vice versa. However, in a scaled system, $\overline{V}_{B2}$ changes between V_f and $-\overline{V}_C$ during CC mode as result of the diode voltage drop. Depending on the capacitor voltage, the inserted voltages could either have the same polarity or an opposite polarity (see Fig. 17(b)).

Since the voltage drop has a magnitude around 1-2% of the system voltage, this may be sufficient to significantly influence grid power flow. Thus, the required amount of capacitor voltage to achieve an optimum line current distribution could be very small. This would not be applicable to a high voltage system, where the impact of the diode's forward voltage drop on CFC operation could be neglected as the CFCs would be mostly operated around several hundreds of volts. Despite the differences previously discussed, it should be highlighted that the simulation and experimental results agree on well.

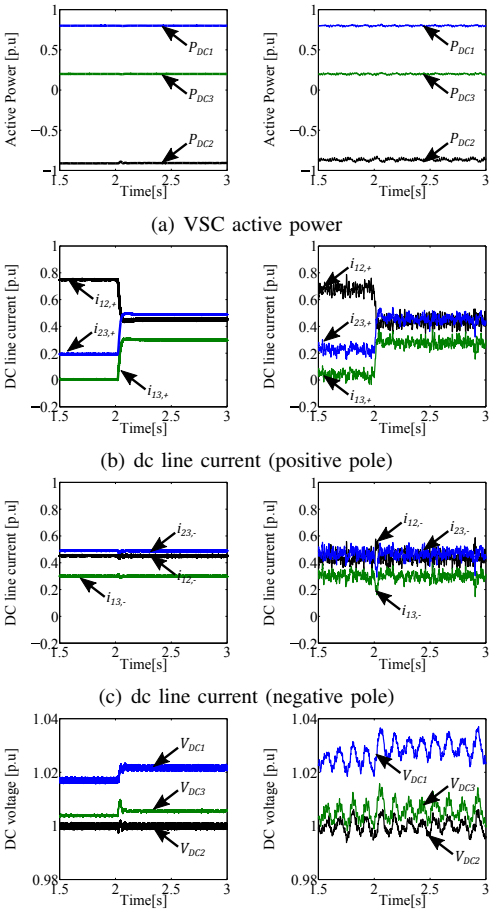
B. Pole Balancing – Uni-pole Compensation

A 1B-CFC with uni-pole compensation is used to eliminate an imbalance between positive and negative poles. Fig. 18 shows the dc grid response. Initially, both CFCs are by-passed and an imbalance of 25% is observed. At $t = 2$ s, the positive pole CFC is enabled only and is requested to maintain current $i_{12,+}$ at the same level as $i_{12,-}$. From Figs. 18(b) and 18(c), it can be seen that the imbalance is eliminated, with simulation and experimental results exhibiting good agreement.

For both the experiment and simulation, the required positive pole CFC capacitor voltage is maintained around 0.011 p.u. (see Fig. 19(a)). As shown in Fig. 19(b), average dc voltages $\overline{V}_{B1}$ and $\overline{V}_{B2}$ are inserted in series with lines L_{12+} and L_{13+}, respectively.

C. Line Overloading Elimination

In the previous test cases, the CFCs have been controlled using local measurements and the references have been set locally. In the test case presented in this section, a hierarchical control system is used to monitor grid power flow. The performance of positive and negative pole 1B-CFCs in the system shown in Fig. 11 is assessed following a line overloading condition resulting from a ramp change in power. The CFCs are assigned to separate LCs, but it is assumed that



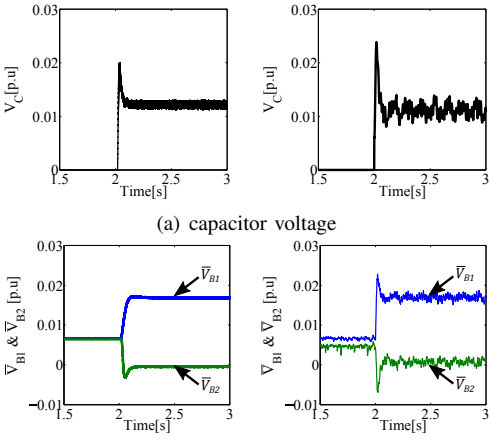
(a) VSC active power

(b) dc line current (positive pole)

(c) dc line current (negative pole)

(d) dc terminal voltage

Fig. 18. DC grid response during uni-pole balancing: Simulation (left) and experimental (right) results.



(a) capacitor voltage

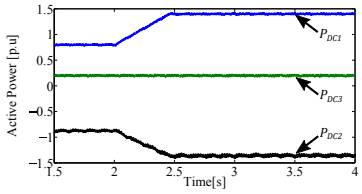
(b) inserted average dc voltages

Fig. 19. Response of the CFC located at the positive pole during uni-pole balancing: Simulation (left) and experimental (right) results.

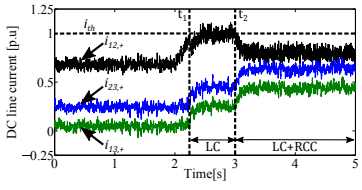
the communication between the RCC and the LCs fails. Due to space limitations only experimental results are presented.

Initially, the voltage source element is by-passed by turning on switches Q_1 and Q_2. At $t = 2$ s, the power generation in Grid 1 increases and VSC 1 adjusts its reference set-point accordingly to inject additional power into the MTDC grid (an additional 0.6 p.u. of power is ramped-up to 1.4 p.u. for 0.5 s, as shown in Fig. 20(a)). This causes the converter current i_1 to increase. Thus, line current $i_{12,+}$ exceeds the maximum ther-

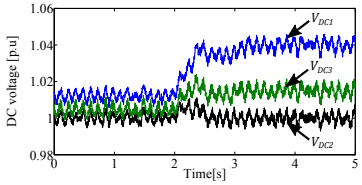
mal current limit $i_{th} = 1$ p.u. (see Fig. 20(b)). Following the overload detection at t_1, the LCs are automatically activated to maintain line currents $i_{12,+}$ and $i_{12,-}$ at i_{th} to avoid line overloading. At $t_2 = 3$ s, the communication between the LCs and RCC is restored and the CFCs are requested to reduce $i_{12,+}$ and $i_{12,-}$ to 0.8 p.u. As a result of series dc voltage injections, terminal voltages of VSCs 1 and 3 are increased to maintain the grid power balance (see Fig. 20(c)). Fig. 21 provides the voltage profiles of the CFC located at the positive pole. The required capacitor voltages are determined by the outer current control loop. As it can be observed, the positive pole capacitor voltage is regulated at 0.009 p.u. between t_1 and t_2. Following restoration of communication, the magnitudes of the capacitor voltage and inserted series dc voltages (as shown in Figs. 21(a) and 21(b), respectively) are increased further in response to the reduction in $i_{12,+}$ and $i_{12,-}$ (see Fig. 20(b)).



(a) VSC active power

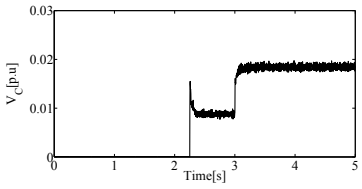


(b) DC line current (positive pole)

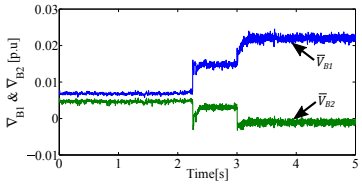


(c) DC terminal voltage

Fig. 20. DC grid response for a ramp change in power with embedded 1B-CFCs. Experimental results.



(a) capacitor voltage



(b) inserted average dc voltages

Fig. 21. Response of the 1B-CFC located at the positive pole for a ramp change in power. Experimental results.

In this test case, the CFC is placed on Line 12 as this line is more likely to become overloaded when compared to other lines. The placement of a CFC within a simple meshed MTDC grid (i.e. three-terminal grid) may be simple, but its placement inside a large dc grid is a non-trivial task. A CFC must be placed at an optimal point to achieve a high current variation capability. In a large dc grid, the adoption of a single CFC could offer a poor performance if the device is not directly connected at the overloaded cable. The required number of CFCs must be ideally defined during the network planning stage as certain lines could become overloaded more frequently when compared to other lines. The distributed CFC approach presented in [34] could reduce the device ratings while increasing the operational range.

Note: It should be emphasized that the benefits of using a CFC in dc grids goes beyond cable thermal management and pole balancing. A 1B-CFC could be used to minimize the wind power curtailment through the rescheduling of grid power flow and to isolate a dc line to facilitate its maintenance without interrupting the dc grid operation. Furthermore, a CFC can be incorporated into the initial network design as it could help to under-rate selected cables in the system.

D. Behavior Under a Pole-to-Pole Fault

Protection is an essential aspect in the design and development of a CFC as the protection scheme could be jeopardized by either system failure or a dc fault. In both cases, the device could experience overcurrent and overvoltage, which could lead to permanent failure. Since CFCs are series-connected devices, their failure would interrupt current flow and lead to system instability. Thus, additional measures must be implemented to avoid interruptions in the operation of a CFC-upgraded MTDC grid. Following this line, the performance of a 1B-CFC under a pole-to-pole fault is examined.

A communication-less single-ended protection strategy is used to detect the fault. Small-scale solid-state based DCCBs are installed at each end of line L_{12} to interrupt fault current (see Fig. 22). These devices are rated at 300 V and have the ability to break currents up to 20 A (*i.e.* 2.5 p.u). For the protection scheme, the DCCBs are set to open and by-pass switches to close if the rate of change in line current is > 800 p.u./s and if the line current magnitude is above 1.3 p.u. In addition, if the voltage across the CFC capacitor is 30% above its rated value, the CFC will be switched to a by-pass mode to protect it against overvoltage. Metal oxide varistors are connected across the by-pass switches and the CFC capacitor to protect the device against overvoltages.

Fig. 22 shows the CFC location. Modules Q_1 and Q_2 are placed in series with dc lines $L_{12,+}$ and $L_{13,+}$, respectively. Initially, the CFC is in CC mode and line current i_{13} is regulated at 0.5 p.u. A pole-to-pole fault is triggered at $t_0 = 2$ s. The fault currents through the CFC are shown in Fig. 23. Following the dc fault, $i_{12,+}$ increases while $i_{13,+}$ decreases. Hence, the CFC capacitor and bridge voltages increase as the CFC tries to maintain a constant line current (see Figs. 24 and 25, respectively). Following fault detection at $t = t_1$, the control signals are disabled and the CFC is switched to a by-pass mode; this way, the fault current is redirected to switches Q_1 and Q_2. The capacitor voltage remains constant as the H-bridge is by-passed. The fault current is interrupted at $t = t_2$ by opening the DCCBs. The system states during the fault are summarized in Table III.

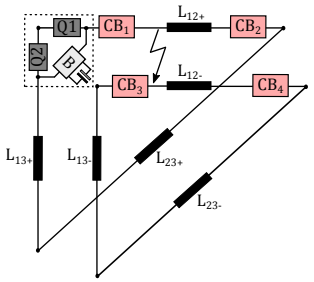


Fig. 22. Pole-to-pole fault location.

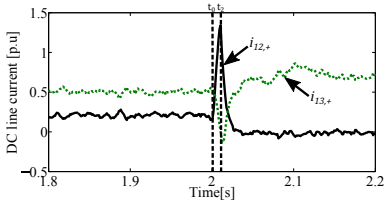


Fig. 23. Fault current through the 1B-CFC during a pole-to-pole dc fault (experimental results)

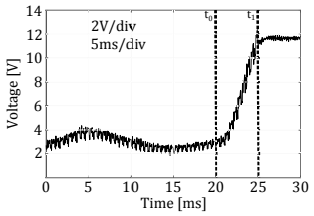


Fig. 24. 1B-CFC capacitor voltage during a pole-to-pole dc fault (experimental results).

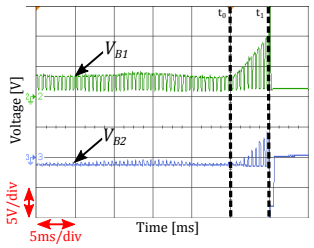


Fig. 25. Inserted dc voltages during a pole-to-pole dc fault (experimental results).

TABLE III
SYSTEM STATE DURING DC FAULT

Time	System state
t_0	Pole-to-pole fault applied
t_1	Fault detected by CFC, bypass switches activated and control signals disabled
t_2	Opening of DCCBs

In this test case, only the faulty line is isolated using four DCCBs. This configuration is sufficient to protect the experimental setup as the magnitude and rate of change of the fault current are limited. This follows the approach in [35], where each cable within a dc grid is equipped with circuit breakers to protect the CFC against any overcurrent or overvoltage. Despite its limitations, the experimental setup adopted in this work is adequate to study the effectiveness of the proposed CFC protection scheme under faulty conditions as demonstrated by the experimental results in this section.

E. Behavior Under a Pole-to-Ground Fault

For completeness, a further simulation is performed to assess the performance of the 1B-CFC under a pole-to-ground fault. Figs. 26 and 27 illustrate the current and voltage profiles of the device during the fault. The fault is applied on Line 12 at $t_0 = 1.5$ s. The system states during the fault are the same as in the pole-to-pole fault case (see Table III). A fault resistance of 0.5 Ω is adopted and the response time of the DCCB is assumed to be 2.5 ms. Initially, the CFC is operated under CC mode to regulate line current $i_{12,+}$ to 0.5 p.u. Following the dc fault at $t = t_0$, line current $i_{12,+}$ starts to rise while current $i_{13,+}$ starts to decrease. As the fault has not been detected by the CFC yet, the capacitor voltage increases as the CFC tries to maintain the line current at its reference value. Subsequently, bridge voltages V_{B1} and V_{B2} are increased. At $t = t_1$, the fault is detected by the CFC and the fault currents are completely redirected to switches Q1 and Q2 by operating the CFC under by-pass mode. The DCCBs are opened at $t = t_2$ and the fault current is interrupted.

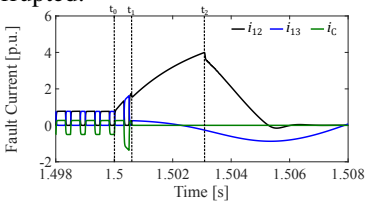


Fig. 26. Fault currents through the 1B-CFC during a pole-to-ground fault (simulation results).

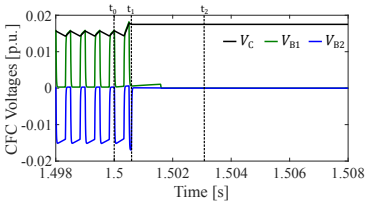


Fig. 27. CFC capacitor and bridge voltages during a pole-to-ground fault (simulation results).

F. A Note on Multi-Port CFC Devices

The operation of inter-dc grid power flow control devices can be affected by either external faults (as demonstrated in this section) or internal faults. Internal failures include semiconductor module failure, failure of gate drivers and mechanical failures. According to a survey conducted on 200 products from 80 companies, failure of a power electronic module due to semiconductor and soldering failures contributes 34% of the total system failures [36]. Although a two-port CFC can adjust the current flowing through uncompensated lines, failure of a port or dc line where the CFC is installed could force the device go offline, leading to unregulated line currents. Under such conditions, a multi-port CFC could offer a better solution in terms of control flexibility, reliability and cost. For instance, a 2B-CFC topology has been adopted in [37] to implement a multi-port CFC.

In a similar vein, the 1B-CFC topology can be extended to a multi-port controller. This idea is summarized in a schematic diagram in Fig. 28. This is a 1B-based multi-port CFC with n ports consisting of n anti-series connected IGBT switches Q_1, Q_2, , Q_n, n half bridges (B_1, B_2, , B_n) and one capacitor. A detailed assessment of this configuration requires further investigation that falls out of the scope of this paper.

VI. CONCLUSIONS

An inter-line CFC topology that effectively achieves line current regulation and redistribution in an MTDC grid has been presented in this paper. The modeling, operation and control

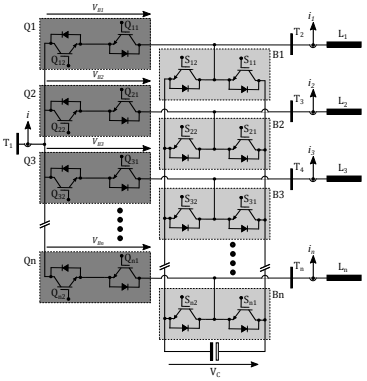


Fig. 28. Multi-port CFC with n ports.

of a 1B-CFC has been assessed under a single modulation scheme. Even when the current carrying capability of dc lines is restricted by their thermal and electric stress limits, it has been demonstrated, both through software simulation and real-time experiments, that the inclusion of a 1B-CFC increases the controllability and reliability of the MTDC grid.

A control method providing pole balancing services during imbalance conditions in upgraded-CFC MTDC grids has been proposed. It has been demonstrated that system performance is improved by balancing the voltages of negative and positive poles. Imbalance elimination is achieved by virtually altering the impedance of the dc lines. This approach may enable asymmetrical tapping of dc lines to power small loads.

The performance of the 1B-CFC has been assessed under pole-to-pole and pole-to-ground dc faults and a simple protection strategy based on DCCBs. As it has been observed, the by-pass switches of the CFC are able to hold fault currents—which is essential as the 1B-CFC is a series-connected device. It has been observed that CFC protection is determined by the response time of its by-pass switches and of the DCCBs.

APPENDIX

The PI controllers are represented in the form: $K(s) = K_p + K_i/s$.

VSCs: Current: $K_p = 45$, $K_i = 45000$. DC voltage: $K_p = 0.2$, $K_i = 20$. Active power: $K_p = 0.2$, $K_i = 20$. Reactive power: $K_p = 0.3$, $K_i = 10$.

1B-CFC: Current: $K_p = 9{\times}10^{-3}$, $K_i = 0.5$. Capacitor voltage: $K = 5.4$, $z_c = 200$, $p_c = 4762$, $z_p = 76.92$. Feedback loop gain: $K_f = 0.05$. CFC gain: $K_c = 5$.

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