Simplified analysis of the effect of load variation in common Doherty power amplifier architectures

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***Abstract*—This paper describes the effect of load variation on Doherty power amplifier performance. A simplified analysis that considers three common Doherty amplifier architectures allows the evaluation of how load variation translates into variation of load at the devices' current generator plane. Under the assumption that system counter-measures are used to avoid drain voltage clipping, the average efficiency and power are evaluated and compared among the different architectures. While, at the centre design frequency, similar results can be observed, it can be seen that an intrinsically broadband design leads to better average power and efficiency over frequency vs. load variation.**

***Index Terms*—Mobile communication, power amplifiers, antenna arrays.**

I. Introduction

Antenna arrays technologies have been used for decades in high frequency systems to increase the gain compared to the single antenna element, and to perform advanced functions such as electronically controlled beamforming or synthetic aperture radars. Future high frequency telecom systems, such as 5G and satellite communications, will use antenna arrays, but compared to past systems they will need to be more cost effective to be sustainable [1]. One consequence of the need of making active arrays cheaper is the acceptance that the bulk circulator (or isolator) at the output of each power amplifier will need to be removed to reduce cost, weight and size [2]. However, the circulator is specifically used to isolate the power amplifier from impedance variation of the antenna array element that might reduce performance in terms of output power, efficiency or linearity. This is particularly critical in active antenna arrays, where the cross-talk between array elements is not-negligible and the input impedance will depend on the dynamic active antenna status, i.e., the relative phase and amplitude setting of each element.

Systems such as 5G will make use of spectrum efficient signals with high peak-to-average ratio that will require advanced PA architectures to increase the average power efficiency to an acceptable level. In this framework, the Doherty PA (DPA) has been widely used to enhance PA efficiency when amplifying amplitude modulated signals, and some examples of DPAs for 5G applications have already been presented [3], [4], [5].

This paper presents a simplified study of the effect of load variation in some common DPA architectures. In particular, it shows how efficiency and output power are affected by load variation by assuming that clipping is avoided, i.e., avoiding strong non-linearity. Although some assumptions are made to simplify the analysis and make it sufficiently general, this study gives an insight on the mechanisms that lead to performance degradation and can be used to select the best DPA architecture.

II. Simulation setup and assumptions

The Doherty architectures considered are shown in Fig. 1. DPA(a) is the basic Doherty configuration where the impedance inverter is realized with a quarter-wave line, and the global output is realized with a quarter-wave line matching. The phase alignment is realized with a quarter-wave line at the auxiliary input. DPA(b) shows an alternative configuration the impedance inverter is realized with a quarter-wave line, the output global matching is obtained with a quarter-wave line matching, but a half-wavelength line is added on the auxiliary side to improve bandwidth. The phase alignment is realized with a quarter-wave line at the main input. DPA(c) is a similar

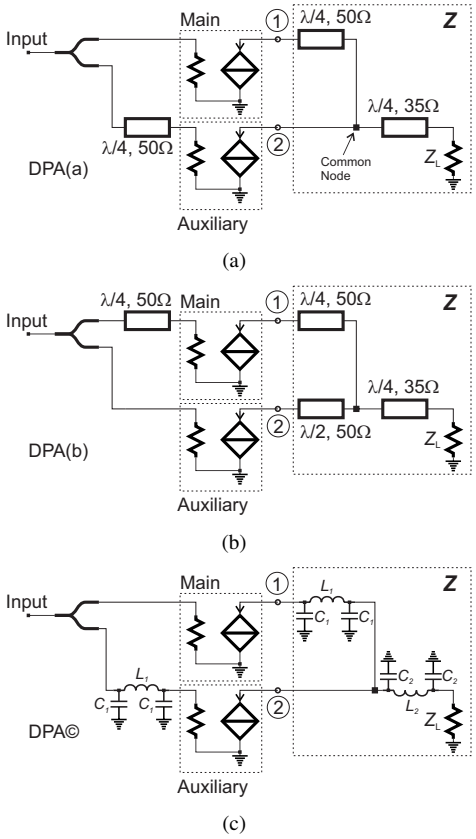

Fig. 1. Simplified Doherty schemes analysed in this paper. DPA(a): Basic Doherty with distributed element filters. DPA(b): Doherty with double inverter on auxiliary side. DPA(c): Basic Doherty with lumped elements low-pass filters.

architecture to DPA(a), but the impedance inverter and the other pieces of lines are realized by means of equivalent, low-pass, lumped element filters. This architecture allows to easily absorb the device output capacitance into the filter.

For simplicity, the devices are assumed to have ideal trans-characteristics with class B-like drain waveforms. Fundamental frequency only is considered. The maximum current I_{MAX} is chosen so that the optimum load for maximum power is $R_{\mathrm{opt}} = 2V_{\mathrm{MAX}}/I_{\mathrm{MAX}} = 50\,\Omega$. V_{MAX} is the maximum drain voltage swing applicable without drain current clipping, that we assume to be equal to the drain bias and set to 25 V for this analysis. With these choices, all the DPA architectures proposed would have, at centre frequency and with load impedance $Z_{\mathrm{L}} = 50\,\Omega$ a maximum output power of 12.5 W.

However, when either frequency or Z_L change, the DPAs do not operate in an ideal condition. The analysis proposed in [6] can be used to estimate the reduction in output power and efficiency, based on the assumption that clipping must be avoided to prevent strong-non-linearity. The output combiner of the Doherty is represented in terms of a **Z** matrix, and the drain voltage of the devices can be written as:

$$\begin{cases} V_{\mathrm{M}} = -Z_{1,1}I_{\mathrm{M}} - Z_{1,2}I_{\mathrm{A}} \\ V_{\mathrm{A}} = -Z_{2,1}I_{\mathrm{M}} - Z_{2,2}I_{\mathrm{A}} \end{cases} \tag{1}$$

where V_{M}, I_{M}, V_{A}, and I_{A} are the drain voltage and current for the main and auxiliary, respectively. It is important to notice that, by avoiding clipping, the description of the devices as current sources can be considered a good approximation. Clipping would occur if the magnitude of the voltage swing on either main or auxiliary exceeds V_{MAX}. In these cases, the input drive is backed-off of a quantity $\sigma = V_{\mathrm{MAX}}/V_{\mathrm{D}}$ to avoid clipping. The break-point is assumed at 6 dB input power back-off from the actual saturated output power, independently from the σ value. To give an example, DPA(a) is considered. At centre frequency, we evaluate the cases of $\Gamma_{\mathrm{L}} = 0$, +0.1, +j0.1, -0.1, -j0.1. The resulting σ values are 1, 0.692, 0.963, 1, and 0.963, respectively, while the calculated efficiency vs. output power curves are shown in Fig. 2. The case $\Gamma_{\mathrm{L}} = 0$ shows the

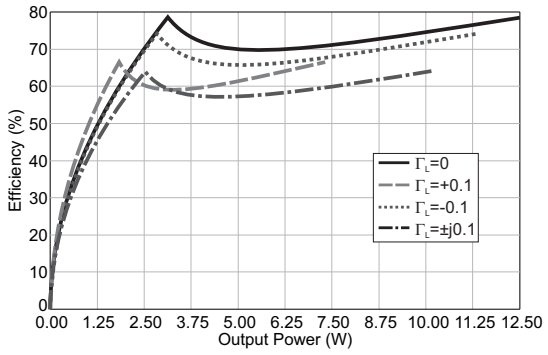

Fig. 2. Efficiency vs. output power for basic Doherty at different load conditions.

typical Doherty efficiency curve. The case $\Gamma_{\mathrm{L}} = +0.1$ is the most critical, since it leads to a large penalty in terms of both back-off power and efficiency. $\Gamma_{\mathrm{L}} = \pm j0.1$ brings to a mild reduction, while $\Gamma_{\mathrm{L}} = -0.1$ shows the least reduction since power, and consequently efficiency, reduction is only due to a lower voltage swing, not to the need of reducing the drive.

III. Load varation at device level

It is interesting to observe how the Γ_{L} variation reflects on the impedance measured at the devices' terminals. Fig. 3 reports the results of this simulation at the centre frequency when the Γ_{L} is swept within a maximum radius of 0.15, with 0.01 magnitude steps and 6 degrees phase steps. Firstly,

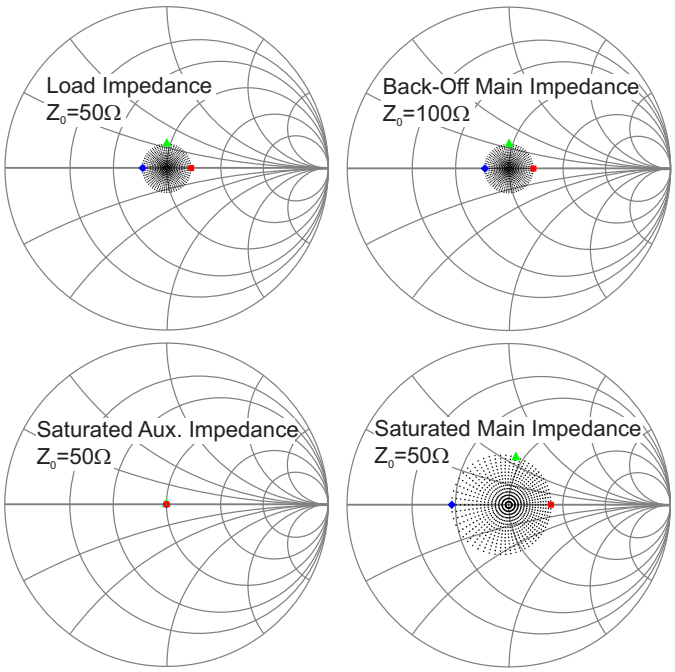

Fig. 3. Swept impedance points at load (top left) with maximum $|\Gamma_{\mathrm{L}}| = 0.15$. Resulting impedance points at back-off for the main device (top right), and at saturation for auxiliary (bottom left) and main (bottom right) devices.

the simulated impedance at the devices' drain terminals is identical for all DPA architectures. The main impedance at back-off is just scaled by a factor of 2 from Z_{L}, while the main impedance at saturation follows a more complex pattern, non-symmetrical around the optimum. Very interestingly, the auxiliary impedance does not vary with Z_{L}. One way of explaining this is by observing that the Doherty impedance inverter transforms the main device current generator into a voltage generator at the common node. This means that the impedance seen by the auxiliary device will be the common node voltage divided by the auxiliary current, both independent from Z_{L}. The half-wavelength line in the architecture of DPA(b) does not affect the validity of this observation.

IV. Average Performance vs. Frequency

To evaluate the average performance of the Doherty architectures vs. load variation, the saturated and 6 dB back-off output power and efficiency for each load condition is calculated and then averaging is applied. This means to

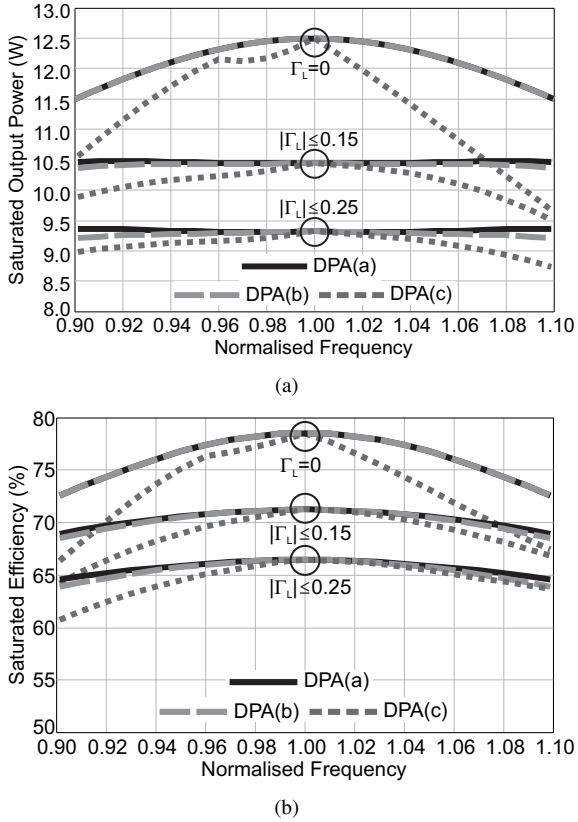

Fig. 4. Saturated output power (a) and efficiency (d) vs. normalised frequency. Comparison between fixed load and average with variable load with maximum $|\Gamma_{\mathrm{L}}|$=0.15 and 0.25, for the 3 considered DPAs.

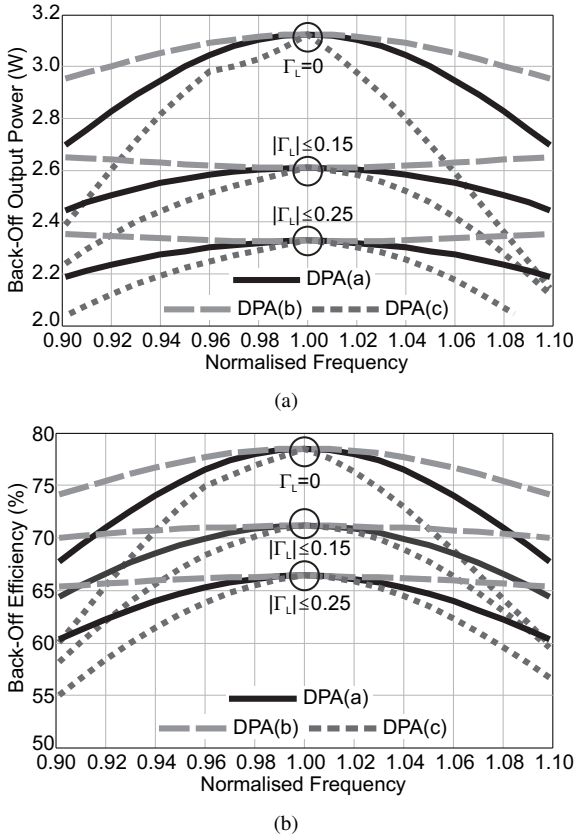

Fig. 5. Back-off output power (a) and efficiency (b) vs. normalised frequency. Comparison between fixed load and average with variable load with maximum $|\Gamma_{\mathrm{L}}|$=0.15 and 0.25, for the 3 considered DPAs.

assume that the loads have uniform probability; this can be refined if more detailed information on the active array behaviour is available. Two cases, maximum Γ_{L} of 0.15 and 0.25, are evaluated, with 0.01 magnitude and 6 degrees phase steps. While the proposed architectures behave identically at the centre frequency, they show different behaviour vs. frequency when simulated over a 20% bandwidth around the centre frequency. Fig. 4 shows the saturated output power and efficiency. The average performance vs. load variation is compared with the constant load condition. For example, at the centre frequency, the saturated output power is reduced to 10.4 W for $\Gamma_{\mathrm{L}} \leq 0.15$ and 9.2 W for $\Gamma_{\mathrm{L}} \leq 0.25$; larger load variation leads to lower average performance, as it could be expected. Very interestingly, the DPA(b) not only shows better bandwidth behaviour for constant load, but also in terms of average when the load varies. Fig. 5 compares the performance at back-off. At centre frequency, the back-off efficiency is reduced from 78.5% to 71% for $|\Gamma_{\mathrm{L}}| \leq 0.15$ and 66% for $|\Gamma_{\mathrm{L}}| \leq 0.25$; also in back-off, larger load variation leads to lower average performance, and again the DPA(b) shows better bandwidth behaviour.

V. Conclusion

This paper presented a simplified analysis of load variation effect in Doherty power amplifiers. While different architectures show similar behaviour at the centre frequency, intrinsically broadband Doherty architectures maintain a better average behaviour over frequency when the load varies. The proposed method can be used for an informed choice of power amplifier architectures for active arrays where cross-talk between array leads to impedance variation.

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