Protection of Single-Phase Fault at the Transformer Valve Side of FB-MMC-Based Bipolar HVdc Systems

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***Abstract*—Although the probability of occurrence of ac grounding faults at the valve side of the interface transformer of a high-voltage dc (HVdc) link is low, they may cause high risks to the converter when compared to grid-side ac faults. This article analyzes the characteristics of valve-side ac single-phase-to-ground faults in full-bridge modular multilevel converters (FB-MMCs)-based bipolar HVdc systems. Overcurrents in the converter arms are analyzed and it is shown that overvoltages in FB submodules occur without an appropriate protection in place. Two strategies are investigated to protect the FB-MMC during the fault and corresponding controllers are designed. The effectiveness of the presented strategies for the prevention of overcurrents and overvoltages, upon nonpermanent and permanent faults, and system postfault restoration is investigated. For completeness, the strategies are also verified by conducting simulations in PSCAD/EMTDC.**

***Index Terms*—Bipolar HVdc system, dc control, full-bridge modular multilevel converters (FB-MMCs) protection, thyristor branch, valve-side single-phase fault, zero-sequence current control.**

I. Introduction

VOLTAGE-SOURCE converter (VSC)-based high-voltage dc (HVdc) systems have drawn significant attention as the need for renewable energy integration increases [1], [2]. Among the available VSC topologies, half-bridge modular multilevel converters (HB-MMCs) have been mostly deployed in recent transmission projects due to their low-power losses and capital costs [3]–[5]. However, due to the freewheeling diodes within the submodules (SMs), these converters cannot interrupt dc fault currents [6]. AC-side circuit breakers (ACCBs) or dc-side circuit breakers (DCCBs) must be used in HB-MMC systems to clear dc short-circuit faults [7]. Alternatively, full-bridge MMCs (FB-MMCs) can block dc fault currents without the need for additional devices [8]. Therefore, the FB-MMC technology constitutes an attractive solution for overhead line-based HVdc systems, which are often subjected to nonpermanent dc faults [9].

Most of the existing VSC-based HVdc systems are monopolar. However, bipolar configurations have been adopted lately to satisfy the increasing power demands [10]. Significant research has been carried out on dc line faults for both monopolar and bipolar MMC-based HVdc systems [11]. Promising solutions have been investigated, such as employing DCCBs in HB-MMC systems or using FB-MMCs to handle dc faults [7], [12], [13]. However, station internal ac faults constitute one of the challenging issues that still needs to be addressed. One example of this type of faults is the wall bushing insulation failure, which may cause a single-phase-to-ground fault between the converter and the interface transformer (i.e., faults at transformer valve side) [14]. Both line commutated converter (LCC) and VSC-based systems have experienced such faults in practical HVdc projects [15]–[17].

Although its probability of occurrence is arguably low, a single-phase-to-ground fault at the valve side may have severe consequences for HVdc systems. For LCC topologies, commutation failure can be exhibited [15]. For MMC-based symmetrical monopolar systems, the fault can result in dc-bus voltage oscillations and the pole-to-ground voltage can reach a magnitude as high as 2 p.u. [18]. For MMC-based asymmetrical monopolar or bipolar systems based on HBs, the fault will generate large dc components in the grid-side currents. Grid-side ACCBs cannot isolate such faults due to the absence of zero-crossings [18], [19]. Additionally, overvoltages at the SMs will be exhibited by FB-MMC-based asymmetrical monopolar and bipolar systems [20]–[22].

A single-phase-to-ground fault at the valve side in a bipolar system generates notable zero-sequence currents in the converter arms [23]. The converter must be blocked once the fault is

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detected to prevent overcurrents. However, blocking the FB-MMC under this condition will result in SM overvoltage in the arms closest to the poles (i.e., the upper arm in the positive pole and the lower arm in the negative pole). In [20], SM overvoltage of FB-MMCs in a bipolar system has been analyzed under a single-phase-to-ground fault at the valve side of the positive pole. Results show that the voltages of SMs in the arms connected to the positive pole could be charged to nearly 2 p.u. of the rated voltage, which could potentially damage the converter unless it is designed to withstand such voltages. However, such an increase in rating would result in an unnecessarily high cost and additional power losses.

Protection methods aimed at reducing the overvoltage and at preventing damages arising from valve-side single-phase-to-ground faults in FB-MMC based bipolar systems have been proposed in the open literature. Surge arresters could be used to clamp the voltages of the arms connected to the positive and negative poles. However, these can only limit the voltage to around 1.7 p.u. and overvoltage would still exist [20]. Other protection measures should be considered before the fault is cleared permanently. In [21], a protection method preventing overvoltages was proposed for a point-to-point system. To this end, the FB-MMC is kept in operation during the fault event to regulate the dc-bus voltage to zero. However, this method may result in overcurrents during the transient regime. In [22], a hybrid MMC topology is presented, which uses HB SMs in the arms connected to the ground pole and FB SMs in the arms close to the positive and negative poles. Such a configuration can limit the overvoltage of SMs in the arms connected to the positive or negative pole. However, nonzero-crossing currents may still arise as in HB-MMC systems [24].

The existing protection methods reported in the literature have not effectively eliminated the SM overvoltages caused by valve-side single-phase-to-ground faults in FB-MMC-based bipolar systems and, thus, further investigation is required. This article bridges such a research gap by first analyzing the characteristics of the faults. To prevent the SM overvoltage, a thyristor branch is installed in the dc side of the FB-MMC and triggered during the fault. Following that, the converter is blocked and the grid-side ACCB is switched OFF for fault isolation purposes. To reduce the time for system restoration under a nonpermanent fault, an additional active protection strategy is included. The FB-MMC is kept in operation to rebuild its output voltages quickly once the fault disappears. For completeness, the effectiveness of the proposed strategies is supported by simulations conducted in PSCAD/EMTDC.

HB-MMCs exhibit a different fault behavior compared to FB-MMCs—for instance, no zero-crossings appear in the grid-side ac for HB topologies. These features demand a different protection philosophy. Given that the fault characteristics of HB topologies have been thoroughly analyzed in [18], with suitable protection schemes being proposed, the scope of this article is limited to FB-based configurations. It should be also highlighted that an experimental validation of the presented scheme, although highly desirable to verify its performance, falls out of the scope of this work.

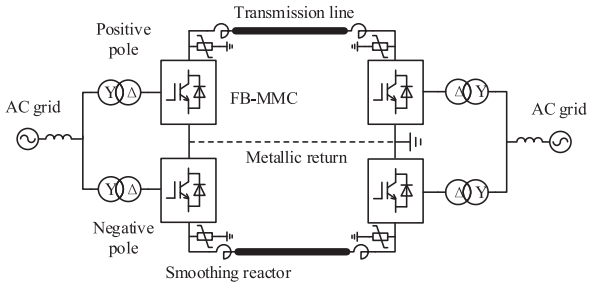


Fig. 1. FB-MMC-based bipolar HVdc system.

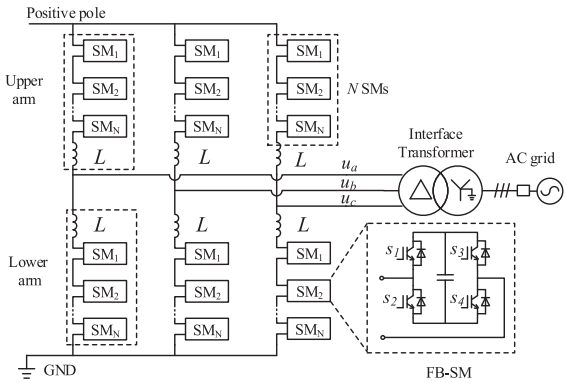


Fig. 2. FB-MMC at the positive pole.

II. Analysis of Valve-Side Single-Phase-to-Ground Faults

A. Bipolar FB-MMC-Based HVdc System Configuration

A point-to-point bipolar FB-MMC-based HVdc system is shown in Fig. 1. It consists of two independent asymmetrical systems with a dedicated metallic return. Since each pole can be controlled independently, only the positive pole is discussed. Fig. 2 shows the circuit diagram of an individual FB-MMC at the positive pole. There are six arms in the converter. Each arm contains N series-connected SMs and an arm inductor L. A star/delta (Y/Δ) transformer is adopted and the neutral grounding point is set at the grid side. This helps to isolate zero-sequence components under grid-side unbalanced conditions. This is discussed in the following section.

A single-phase equivalent circuit of a FB-MMC is shown in Fig. 3(a). The phase voltage waveforms are illustrated in Fig. 3(b) (phase a is shown as an example). The arm voltage modulated by the SMs is represented as a controlled voltage source. The ac-side output voltage is expressed as

$$u_x = \frac{1}{2}U_{\rm dc} + \sqrt{2}V_{\rm AC}\sin(\omega t + \varphi_x), \quad (x = a, b, c) \tag{1}$$

where u_x is the phase-to-ground voltage of the converter, $U_{\rm dc}$ the dc-bus voltage, $V_{\rm AC}$ the root mean square (rms) ac component of the phase voltage, and φ_x the phase angle.

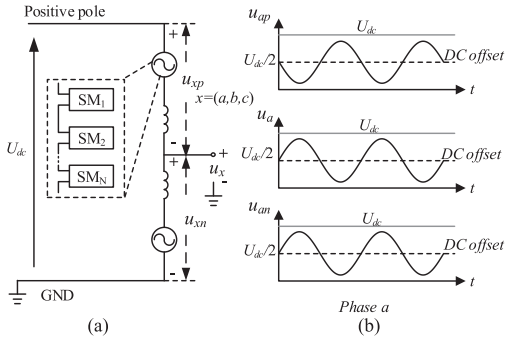


Fig. 3. Single-phase equivalent circuit of the FB-MMC ($x = a, b, c$) and its valve-side voltage waveforms. (a) Single-phase diagram. (b) Waveforms of phase *a*.

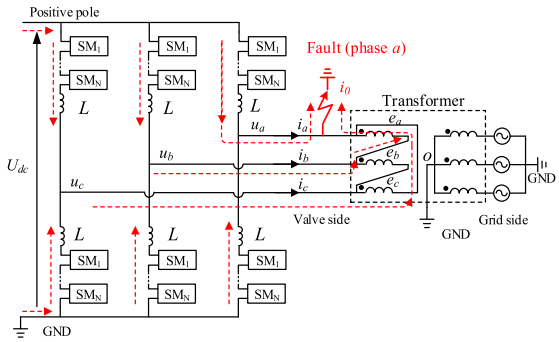


Fig. 4. Zero-sequence currents path during a single-phase-to-ground fault at the valve side of phase *a*.

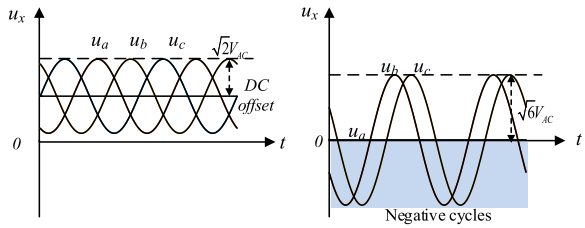


Fig. 5. Valve-side ac voltages due to a single-phase fault. Fault occurring at phase *a* as an example. (a) Prefault. (b) Postfault.

A modulation index m ($0 \leq m \leq 1$) for a FB-MMC is defined as the ratio between the ac-side and dc-side voltages, where

$$\frac{1}{2} m U_{\mathrm{dc}} = \sqrt{2} V_{\mathrm{AC}}. \tag{2}$$

Substituting (2) into (1) yields

$$u_x = \frac{1}{2} U_{\mathrm{dc}} \left(1 + m \sin(\omega t + \varphi_x)\right). \tag{3}$$

If only the fundamental component is considered, the voltages u_{xp} and u_{xn} produced by the upper and the lower arms in steady state, respectively, can be expressed as

$$u_{xp} = \frac{1}{2} U_{\mathrm{dc}} \left(1 - m \sin(\omega t + \varphi_x)\right) \tag{4}$$

$$u_{xn} = \frac{1}{2} U_{\mathrm{dc}} \left(1 + m \sin(\omega t + \varphi_x)\right). \tag{5}$$

As observed in (3)–(5), a dc offset voltage ($U_{\mathrm{dc}}/2$) exists for a bipolar configuration. Thus, the ac-side output voltages of the converter are always positive with respect to ground.

B. Zero-Sequence Current Analysis

A *Y*/Δ interface transformer is normally considered for MMCs-based HVdc systems and its grounding point is set at the grid side [25]. Zero-sequence currents can be isolated if a single-phase-to-ground fault happens at the grid side of the transformer since there is no path for them to flow to the valve side. However, if the fault occurs at the valve side instead, paths for zero-sequence currents will be created. Phase *a* is chosen as an example. This is shown in Fig. 4 (as red-dashed lines) for a *Y*/Δ transformer. A similar outcome occurs when a *Y*/*Y* transformer is used instead.

The magnitude of the zero-sequence currents arising once a valve-side grounding fault occurs is significant. As a result, these may, in turn, cause overcurrent in the converter arms. A simple way to limit this overcurrent and prevent semiconductor devices from overheating is achieved by blocking the FB-MMC (i.e., by switching OFF all transistors, such as insulated-gate bipolar transistor (IGBTs) following the fault. However, this approach may cause large SM overvoltage in the upper arms of the FB-MMC—especially in the nonfaulted phases. This will be analyzed in detail next.

C. SM Overvoltage Analysis

After the FB-MMC is blocked, the voltage of the faulted phase (a) will be zero. Conversely, the voltage magnitude of the nonfaulted phases (b and c) will increase to the magnitude of the line-to-line voltage (see Fig. 5)

$$u_x = \sqrt{3} \times \sqrt{2} V_{\mathrm{AC}} \sin\left(\omega t + \varphi_x + \Delta\varphi_x\right) \ (x = b, c) \tag{6}$$

where $\Delta\varphi_x$ is the phase angle variation due to the fault.

By comparing (6) with (1), it can be seen that the dc offset in the nonfaulted phase voltages disappears following the fault, which results in negative voltages with respect to the ground potential during their negative half-cycles, as shown in Fig. 5(b). These negative voltages will severely overcharge the upper arms SMs of the FB-MMC.

The voltages feeding the upper arms u_{xp} [see Fig. 6(a)] are expressed as

$$u_{xp} = U_{\mathrm{dc}} - u_x, \ (x = a, b, c). \tag{7}$$

Under normal conditions, since u_x is always positive with respect to ground, u_{xp} is smaller than U_{dc} according to (7). The total capacitor voltage of all the SMs in each arm $V_{c,\mathrm{sum}}$ equals U_{dc} before the fault [26]. However, since negative half-cycles for u_x will be present in the nonfaulted phases for single-phase-to-ground faults at the valve side, u_{xp} will be larger than U_{dc} after the fault when u_x is in its negative half-cycles. Fig. 6(a) shows the charging paths in the upper arms after the converter is blocked (as red-dashed lines). Although all the IGBTs have been switched OFF after the fault, the charging current will flow

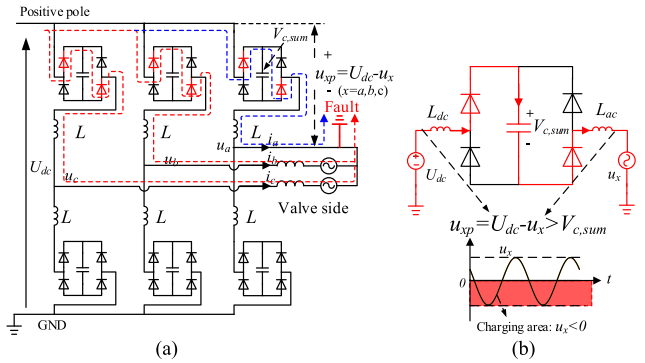


Fig. 6. Capacitor charging path of SMs in upper arms after the converter is blocked. (a) Charging path. (b) Equivalent circuit of charging path.

through the diodes of the SMs in the upper arms when u_{xp} is larger than $V_{c,\mathrm{sum}}$ [see Fig. 6(b)]

$$u_{xp} = U_{\mathrm{dc}} - u_x > V_{c,\mathrm{sum}}. \tag{8}$$

The upper arm SM capacitors will be charged until their total voltage $V_{c,\mathrm{sum}}$ reaches a maximum value

$$V_{c,\mathrm{sum}} = u_{xp\_\max} = U_{\mathrm{dc}} + \max|u_x| \tag{9}$$

where $\max|u_x|$ is the maximum amplitude of u_x.

It should be noticed that the energy stored in the inductance [i.e., dc and arm inductances in Fig. 6(b)] also contributes to the overvoltage of the upper arm SMs during the initial period of the fault. Thus, even when the faulted phase voltage is zero after the fault ($u_a = 0$), the SMs in phase a will still be overcharged. The blue-dashed line in Fig. 6(a) shows the charging path of the faulted phase during the initial period of the fault.

Due to the negative cycles of the phase voltages, the SM overvoltage exhibited by SMs in the nonfaulted phases will be worse than the overvoltage in the faulted phase. By substituting (2) and (6) into (9), the maximum voltage of the SMs in the upper arms of the nonfaulted phases is obtained as

$$V_{c,\mathrm{sum}} = u_{xp\_\max} = U_{\mathrm{dc}} + \sqrt{6}V_{\mathrm{AC}} = \left(1 + \frac{\sqrt{3}m}{2}\right) U_{\mathrm{dc}}. \tag{10}$$

According to (10), it can be seen that $V_{c,\mathrm{sum}}$ is determined by the amplitudes of the line-to-line ac voltage and the dc bus voltage and has a value of around $(1 + 0.886m)U_{\mathrm{dc}}$. Considering a 10% ripple during operation [26], this value may increase to $(1.1 + 0.886m)U_{\mathrm{dc}}$. The worst case will be experienced when the modulation index is $m = 1$, resulting in $1.986U_{\mathrm{dc}}$—reaching nearly 2 p.u. of the rated voltage. Such an overvoltage could damage the FB-MMC unless the SMs in the upper arms are designed to withstand a voltage of 2 p.u. An effective strategy is required to protect the FB-MMC under this condition.

III. Proposed Fault Protection Strategy

A valve-side single-phase-to-ground fault cannot be isolated simply by blocking the FB-MMC and, thus, additional protection measures are required. As shown in Section II, the SMs in the upper arms will be overcharged by the dc bus during the negative cycles of the phase voltages. To prevent the SM overcharge, either the dc-bus voltage could be reduced or the ac phase voltages disconnected. To avoid negative cycles in the phase voltages, the grid-side ACCBs could be switched OFF—however, the SMs of the FB-MMC may still be overcharged as removing the ACCBs from service may take several cycles [27]. In this section, a thyristor branch with a corresponding control strategy is presented to address the aforementioned problems.

A. Detection of Valve-Side Phase-to-Ground Faults

As the presence of zero-sequence current is an indication of a valve-side fault, this fact can be used for fault detection. The following criterion is defined:

$$i_0 = |(i_a + i_b + i_c)/3| \geq i_T \tag{11}$$

where i_0 is the zero-sequence current at the valve side of the FB-MMC and i_T is a threshold value. If the magnitude of the current i_0 is higher than the threshold, a fault is taking place.

B. Protection Strategy of the Faulted Converter

To protect the FB-MMC, a thyristor-based branch is installed at the dc terminals to clamp the dc-bus voltage following the fault. This is shown in Fig. 7. The branch is triggered when the valve-side fault is detected by the local protection system (discussed in Section III-A). Following that, the energy stored in the dc inductors and dc lines is released immediately through the thyristor branch instead of through the converter. The overvoltage in the SMs is avoided since the dc bus, which charges the SMs, is short circuited by the thyristor branch.

By using this approach, the FB-MMC is safely blocked without causing SM overvoltage. The grid-side ACCB can be then used to isolate the fault.

C. Protection Strategy of the Remote Converter

Although short circuiting the dc bus during the fault prevents SM overvoltages at the faulted converter, remotely located MMCs may exhibit overcurrents. Given that dc can be regulated by FB-MMCs during faults [9], a dc controller is incorporated to all FB-MMCs within the system to prevent the dc-side overcurrents.

A block diagram of a dc control loop based on a proportional integral (PI) controller is shown in Fig. 8. As it can be observed, this has been cascaded with an active power or dc voltage outer control loop. During normal operation, current reference i_{dcref} is generated from the outer loop and compared with the converter's dc i_{dc}. For all remote FB-MMCs, once the dc-bus voltage is lower than a preset limit (e.g., $U_{\mathrm{dc}} < U_{\mathrm{limit}} = 0.85$ p.u.), the reference is set to zero instead (indicated with red in Fig. 8). This reduces the current flowing through the thyristor branch to zero. Under this condition, the thyristor branch will be automatically turned OFF. After that, the fast disconnector at the faulted terminal will be used to isolate the faulted converter.

It should be noted that for point-to-point systems, the remote FB-MMC will work as a static synchronous compensator only

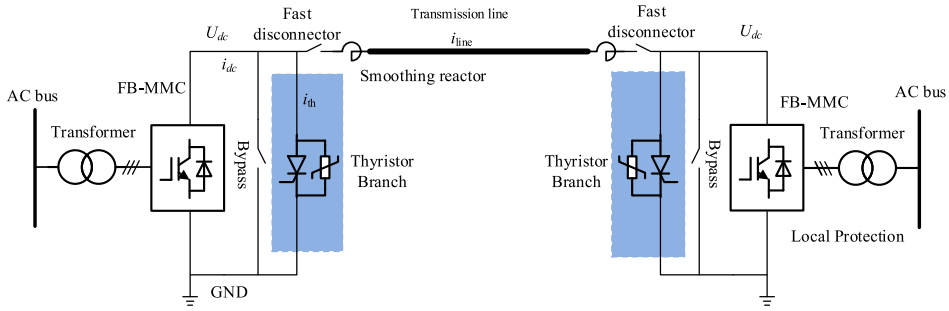


Fig. 7. Proposed protection thyristor branch.

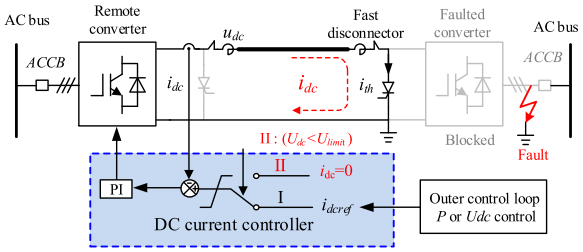


Fig. 8. Protection strategy of the remote converter.

due to the loss of the faulted terminal. However, in multiterminal systems, the status of the faulted terminal should be informed to all remote FB-MMCs by means of communications. Once the faulted terminal has been isolated, the whole system can begin to recover.

IV. Active Fault Protection Strategy

The protection strategy presented in Section III blocks the FB-MMC at the faulted terminal following fault detection. The grid-side ACCB can be then switched OFF to isolate the fault. This scheme is suitable for clearing a permanent valve-side fault, such as the insulation failure of a bushing. For a nonpermanent fault, such as a recoverable flashover, the FB-MMC should be reconnected to the ac grid following fault clearance to reduce the impact on the power transmission. However, reclosure of an ACCB takes time (e.g., several hundred milliseconds) [27], which could cause an undesirable long power transmission interruption. To prevent such shortcoming, an active fault protection strategy is presented in this section. The FB-MMC is kept in operation following the fault using a suitable controller that reduces the recovery time of the system following a nonpermanent fault.

A. DC-Side Control

SM overvoltage is avoided by triggering a thyristor branch to clamp the dc voltage when a valve-side fault is detected (see Fig. 7). A dc controller is used to prevent dc-side overcurrents, as shown in Fig. 9. The dc reference i_{dcref} is set to zero once the thyristor branch is triggered. This regulates the dc of the FB-MMC to zero, which will contribute to the reduction of the current of the thyristor branch.

B. AC-Side Control

As discussed in Section II-C, a valve-side single-phase-to-ground fault removes the dc offset at the ac voltage of the MMC. The dc offset ($U_{\mathrm{dc}}/2$) of the phase voltages disappears and negative cycles appear in the nonfaulted phases. Although this shortcoming cannot be handled by a HB configuration, the FB-MMC can be kept in operation during the fault and regulate its ac-side currents to zero since its SMs have the capability to generate negative voltages.

Large zero-sequence currents will be caused in the arms of the FB-MMC even when the dc voltage has been clamped to zero by the triggered thyristor branch. Given that conventional *dq*-frame-based control schemes cannot suppress zero-sequence currents, an additional control loop acting simultaneously with the thyristor branch is added. This is also shown in Fig. 9. The zero-sequence current controller is disabled during normal operation and the references for the *dq* current control $i_{d\mathrm{ref}}$ and $i_{q\mathrm{ref}}$ are generated from the outer control loop. When the fault is detected, the zero-sequence current controller is enabled and the references $i_{d\mathrm{ref}}$, $i_{q\mathrm{ref}}$, and $i_{0\mathrm{ref}}$ are all set to zero to regulate the ac-side current to zero.

As the zero-sequence component under a single-phase-to-ground fault exhibits the fundamental frequency, a proportional-resonant (PR) controller is adopted. A PR controller can suppress an ac at a specific frequency more effectively than a proportional or PI controller [28].

C. Fault-Type Discrimination and System Recovery

After both the dc-side and ac-side currents are reduced to zero, a nonpermanent fault disappears after some time. To effectively discriminate this type of fault from permanent faults, a small pulse (e.g., 0.2 p.u. rated dc for 10 ms) is added to the zero-sequence current reference $i_{0\mathrm{ref}}$ following a time delay (e.g., 30 ms). This is also shown in Fig. 9.

If no zero-sequence current is detected during the pulse injection period, it can be determined that the ac fault has been cleared. The zero-sequence controller can be then disabled to rebuild the normal ac-side voltage and the faulted FB-MMC can get recovered at its ac side. When the thyristor branch is turned OFF, the dc side of the system can also start its recovery process.

Conversely, if a zero-sequence current is still detected during the pulse injection period, the fault will be deemed as permanent. The FB-MMC will be blocked and the grid-side ACCB will be

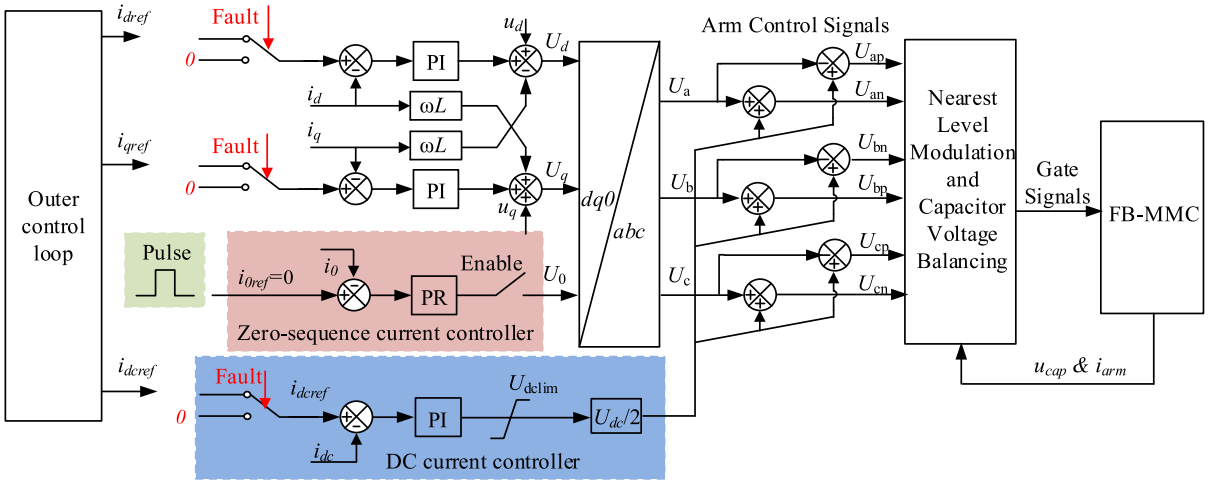


Fig. 9. Active protection strategy with corresponding controllers during the valve-side fault.

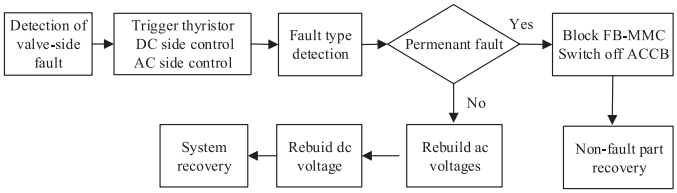


Fig. 10. Active protection strategy.

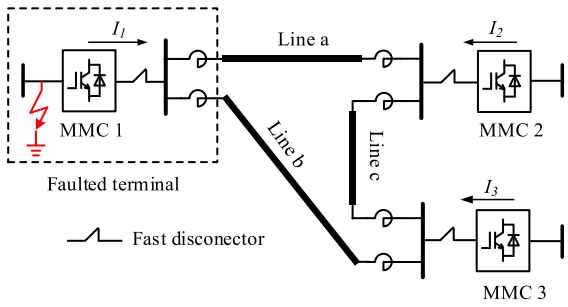


Fig. 11. Three-terminal HVdc test system (one pole is shown only).

switched OFF to isolate the fault. The other nonfaulted parts can then start their recovery process.

The protection procedure of the active protection strategy is summarized by the flowchart in Fig. 10.

V. Case Studies and Analysis

A bipolar point-to-point system and a meshed three-terminal FB-MMC HVdc system have been built in PSCAD to verify the analysis provided in Section II and the protection methods in Sections III and IV. The systems are implemented as in Figs. 7 and 11. The thyristor branch is installed at the dc terminals of each FB-MMC. System parameters are provided in Table I. Since each pole can be controlled independently, the valve-side phase-to-ground fault is analyzed on the positive pole. Phase *a* is chosen to simulate the fault—occurring at $t = 1$ s.

TABLE I
Parameters of the Simulated FB-MMC System of Each Terminal

Parameter	Value
Rated active power	2 × 1.5 GW
Rated dc voltage	± 500 kV
RMS ac voltage (line to line)	260 kV
Transformer capacity	2 × 1680 MVA
Transformer leakage inductance	0.15 p.u.
Transformer ratio	500 /260 kV
Arm inductance	60 mH
SM Capacitor	18 mF
Number of SMs in each arm	250
DC smoothing inductor	100 mH
Number of thyristors in each branch	350
Thyristor rating/peak surge current	6500 V/4250 A/64 kA
Thyristor I^2t capacity	20.48 MA^2-s

Different cases are assessed to verify the effectiveness of the proposed methods. To justify the inclusion of the thyristor branch, a comparison with schemes found in the literature is also conducted. Unless explicitly stated otherwise, the results on this section are for the bipolar point-to-point configuration.

A. Case I: Blocking the FB-MMC Only

When the fault is detected by the local protection system, the FB-MMC is blocked after a time delay (100 μs) without other protection measures being in place. Fig. 12 shows the simulation results. The valve-side ac voltages are given in Fig. 12(a). Following the fault, the dc offset of the phase voltages becomes zero and the magnitude of the phase voltages in the nonfaulted phases rises to a line-to-line value. The dc bus charges the SMs in the upper arms of the FB-MMC. The charging currents are shown in Fig. 12(b). Fig. 12(c) and (d) shows the SM capacitor voltages in the upper arms and lower arms of the FB-MMC after

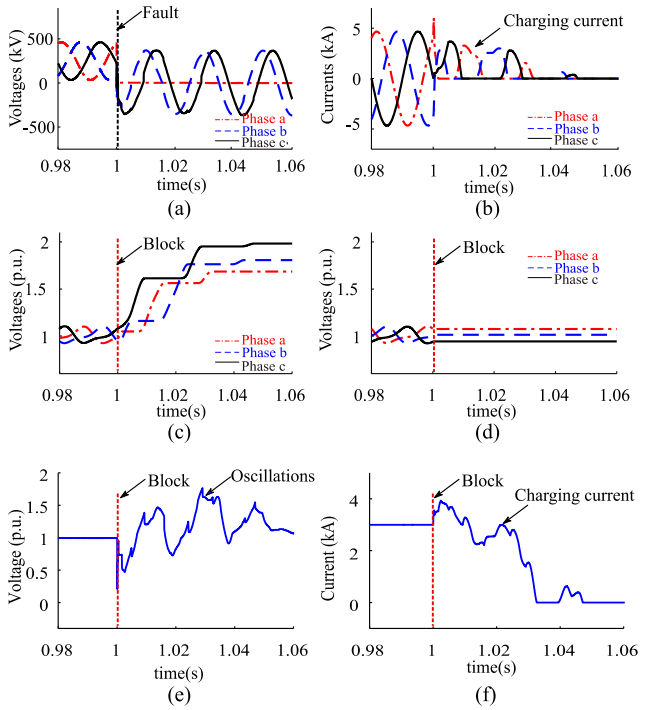


Fig. 12. Blocking the FB-MMC only for the phase-to-ground fault. (a) Valve-side ac voltages: u_x. (b) Valve-side ac currents: i_x. (c) Upper arm capacitor voltages: V_{cp}. (d) Lower arm capacitor voltages: V_{cn}. (e) DC voltage: u_{dc}. (f) DC current: i_{dc}.

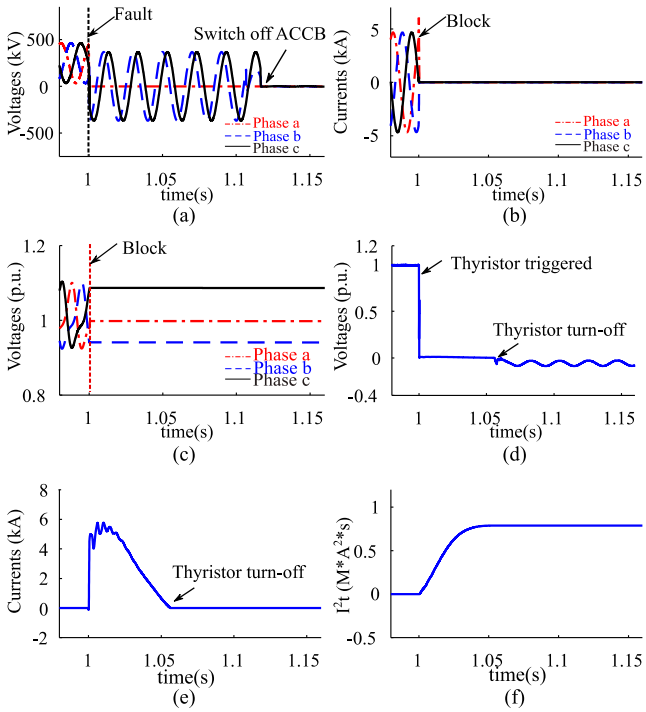


Fig. 13. Blocking the FB-MMC and triggering the thyristor simultaneously for the phase-to-ground fault. (a) Valve-side ac voltages: u_x. (b) Valve-side ac currents: i_x. (c) Upper arm capacitor voltages: V_{cp}. (d) DC voltage: u_{dc}. (e) Thyristor current: i_{th}. (f) I^2t of thyristor branch.

the fault, respectively. It can be seen that SMs in the upper arms are overcharged and the maximum voltage reaches nearly 2 p.u.

The phase voltages in the nonfaulted phases [phases *b* and *c* in Fig. 12(a)] exhibit negative cycles after the fault. As a result, the voltages of the SMs in the upper arm of the nonfaulted phases will have a higher magnitude than in the faulted phase (phase *a*). As a result of the energy stored in the inductors and transmission lines, the dc-bus voltage also sees a transient voltage during the initial stage when the converter is blocked [see Fig. 12(e)], which, in turn, also contributes to the SM overvoltages. It can be observed in Fig. 12(c) that the peak capacitor voltages in phases *b* and *c* are different. This occurs since the prefault instantaneous values of the phase voltage are different. When the dc-bus voltage reaches its peak value, the voltage of phase *c* is in its negative cycle (higher in magnitude than that of phase *b*) in this specific case. From these results, it can be concluded that blocking the converter only without considering additional protection means in place causes an overvoltage in the upper arms of the SMs.

B. Case II: Triggering the Thyristor Branch and Blocking the FB-MMC

When the fault is detected, the FB-MMC is blocked and the thyristor branch is triggered simultaneously. The valve-side ac voltages are shown in Fig. 13(a), which are similar as in Case I following the fault. However, by triggering the thyristor branch, there is no charging current flowing through the FB-MMC [see Fig. 13(b)] and no overvoltage occurring in the SMs of the upper arms [see Fig. 13(c)] since the dc voltage has been clamped to zero [see Fig. 13(d)]. The current of the thyristor branch and a plot for I^2t of the thyristor branch representing the thermal capability are shown in Fig. 13(e) and (f), respectively. The peak current is around 6 kA and I^2t is 0.8 MA^2s for this specific case, which is within the safe operation area of the selected thyristor (see Table I) [29]. The current flowing through the thyristor branch is reduced to zero as the remote FB-MMC regulates its dc to zero after the fault. After 100 ms (that is, five cycles of ac voltage emulating the operating time of ACCBs), the grid-side ACCB is switched OFF to isolate the fault. As it can be observed, the fault is isolated and no SM overvoltage is exhibited in the FB-MMC when this protection method is adopted.

C. Case III: Active Protection Method

When the fault is detected, the FB-MMC is kept in operation instead of being blocked and the thyristor branch is triggered to clamp the dc-bus voltage. The valve-side ac voltages are shown in Fig. 14(a). These are identical to those in Cases I and II immediately after the fault. As shown in Fig. 14(b), the ac-side currents are regulated to zero after the fault, which contributes to extinguishing the ac fault current. No overcurrents occur in the arms of the FB-MMC [see Fig. 14(g) and (h)]. There is no overvoltage occurring in the SMs of the upper arms [see Fig. 14(c)] since the dc voltage has been clamped to zero [see Fig. 14(d)]. The SM voltages are regulated by the voltage balance control loop of the FB-MMC. Through the active method, the dc of the FB-MMC, as shown in Fig. 14(f), is regulated to be zero.

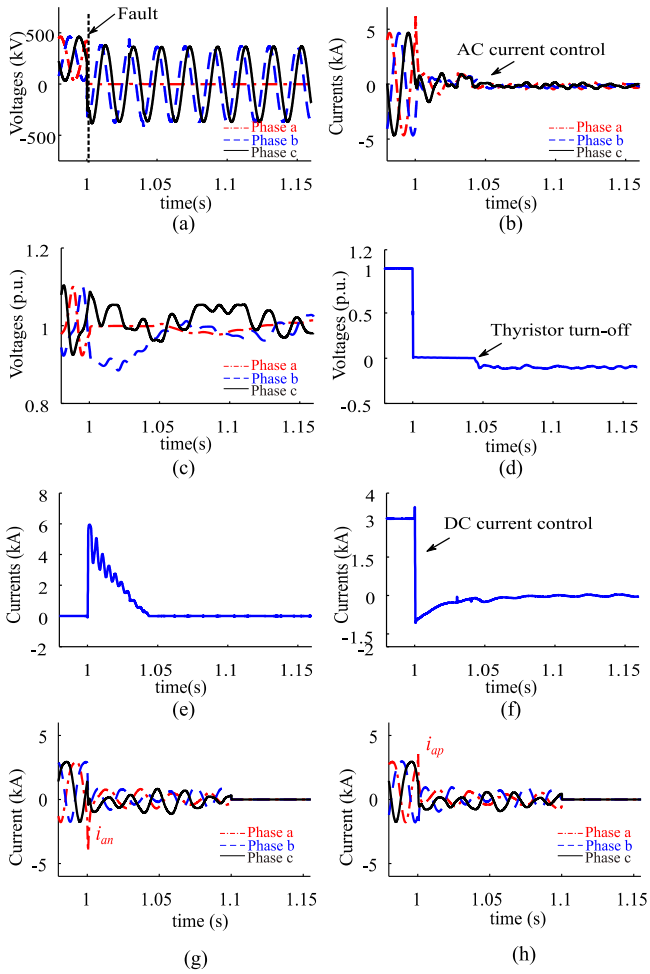


Fig. 14. Active protection for the phase-to-ground-fault. (a) Valve-side ac voltages: u_x. (b) Valve-side ac currents: i_x. (c) Upper arm capacitor voltages: V_{cp}. (d) DC voltage: u_{dc}. (e) Thyristor current: i_{th}. (f) DC current: i_{dc}. (g) Lower arm currents: i_{arm}. (h) Upper arm currents: i_{arm}.

This reduces the magnitude of the current flowing through the thyristor branch, as shown in Fig. 14(e). The thyristor branch is turned OFF when the current becomes zero.

D. Permanent Versus Nonpermanent Faults

As shown in Sections V-B and V-C, the ac-side currents can be reduced to zero regardless of whether this is achieved through the active control method or automatically.

Simulations are carried out to demonstrate the capability of the active protection method to discriminate between permanent and nonpermanent faults. To achieve this, a 10-ms pulse (0.2 p.u. of the rated dc) is added to the reference of the zero-sequence current controller (see Fig. 9). The pulse is injected with a 30-ms time delay following fault detection.

1) Permanent Fault: If the zero-sequence current can still be detected during the pulse injection period, as shown in Fig. 15(a), the fault is considered permanent. The grid-side ACCB is used to isolate the valve-side fault within 100 ms, as shown in Fig. 15(b).

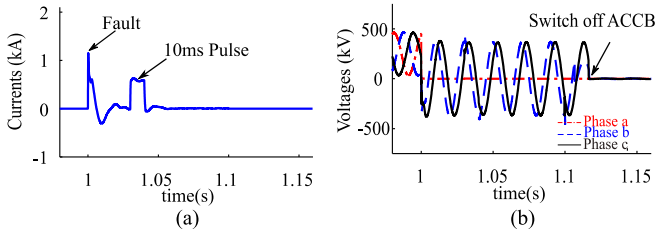


Fig. 15. Protection process of a permanent fault. (a) Zero-sequence current: i_0. (b) AC voltages: u_x.

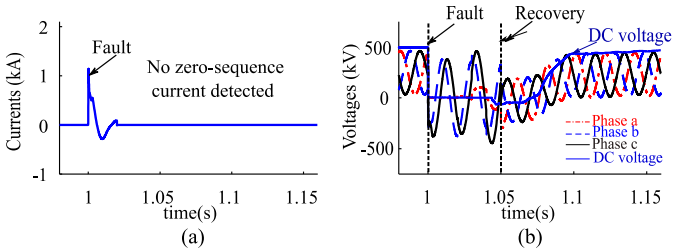


Fig. 16. Protection and restoration process of a nonpermanent fault. (a) Zero-sequence current: i_0. (b) AC voltages u_x and DC voltages u_{dc}.

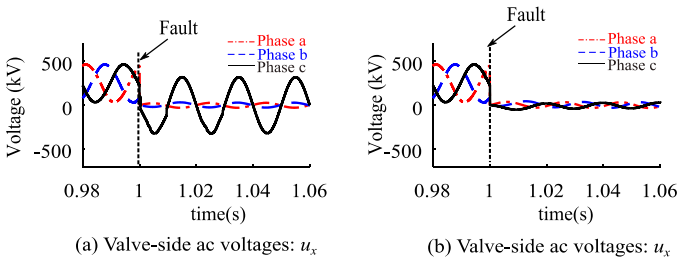
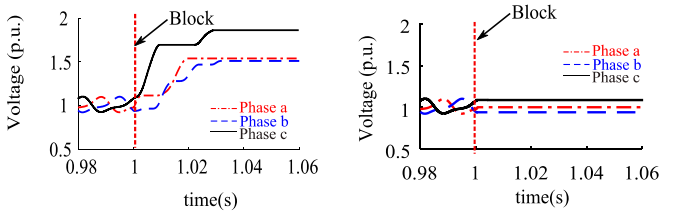


Fig. 17. Valve-side ac voltages after a grounding fault. (a) Two-phase fault. (b) Three-phase fault.

2) Nonpermanent Fault: If there is no zero-sequence current detected during the pulse injection period, as shown in Fig. 16(a), this indicates that the fault has disappeared. As it can be observed, the FB-MMC can rebuild its normal ac and dc voltages within 50 ms, as shown in Fig. 16(b). The active protection method contributes to reducing the recovery time of the whole system.

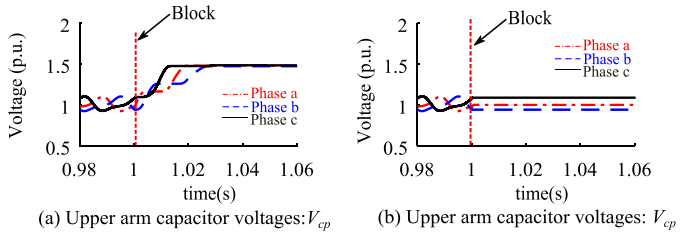
E. Performance Under Two- and Three-Phase Faults

To further verify the performance of the presented protection scheme, additional types of grounding faults are investigated. Fig. 17(a) and (b) shows the valve-side ac voltages following two-phase and three-phase faults occurring at $t = 1$ s into the simulation, respectively. As it can be observed, negative cycles in the phase voltages are still present under a two-phase fault. Similar to a single-phase fault, blocking the FB-MMC only upon two- and three-phase faults results in SM overvoltages in the upper arms following the faults [see Figs. 18(a) and 19(a)]. The overvoltages in the nonfaulted phase for a two-phase fault are more severe than in the faulted phases due to the presence of the negative cycles. Following a three-phase fault, the upper arm



(a) Upper arm capacitor voltages: V_{cp} (b) Upper arm capacitor voltages: V_{cp}

Fig. 18. Upper arm capacitor voltages following a two-phase fault. (a) Blocking the FB-MMC only. (b) Blocking the FB-MMC and triggering thyristor branch.



(a) Upper arm capacitor voltages: V_{cp} (b) Upper arm capacitor voltages: V_{cp}

Fig. 19. Upper arm capacitor voltages following a three-phase fault. (a) Blocking the FB-MMC only. (b) Blocking the FB-MMC and triggering thyristor branch.

SMs experience smaller overvoltages compared to a two-phase fault since no negative cycles appear in the phase voltages. However, the overvoltages are avoided altogether when the thyristor branch is triggered [see Figs. 18(b) and 19(b)]. These results show the effectiveness of the thyristor branch to protect the FB-MMC for different types of grounding faults.

F. Multiterminal System

The effectiveness of the presented method is verified for the three-terminal system in Fig. 11. Before the fault takes place, MMC2 regulates the dc voltage $U_{\rm dc}$ and reactive power Q_2. MMC1 and MMC3 regulate their active and reactive powers (P_1 and Q_1, and P_3 and Q_3, respectively). A permanent fault occurs at the terminals of MMC1, with results shown in Fig. 20. As shown by the FB-MMC ac in Fig. 20(a) and (b), no ac-side overcurrents are caused by the triggered thyristor branch since the converter can actively ride through a dc fault. Fig. 20(c) and (d) shows the dc-bus voltage and dc of the MMCs. Since MMC2 maintains the dc-bus voltage, its dc limit is set higher (e.g., 5 kA) than for the other two MMCs. Therefore, the dc-side current of MMC2 has a higher magnitude. However, its value is still within the safe operation region of the converter. After the faulted terminal is isolated safely around 100 ms following the fault, the remaining healthy converters rebuild the dc voltage at $t = 1.15$ s [see Fig. 20(c)] and restore to their prefault condition at $t = 1.25$ s [see Fig. 20(d)].

As opposed to a point-to-point system, the current stress of the thyristor branch is higher. This occurs since in the multiterminal configuration there are more than one lines injecting currents to the thyristor branch. The peak current and the I^2t of the branch

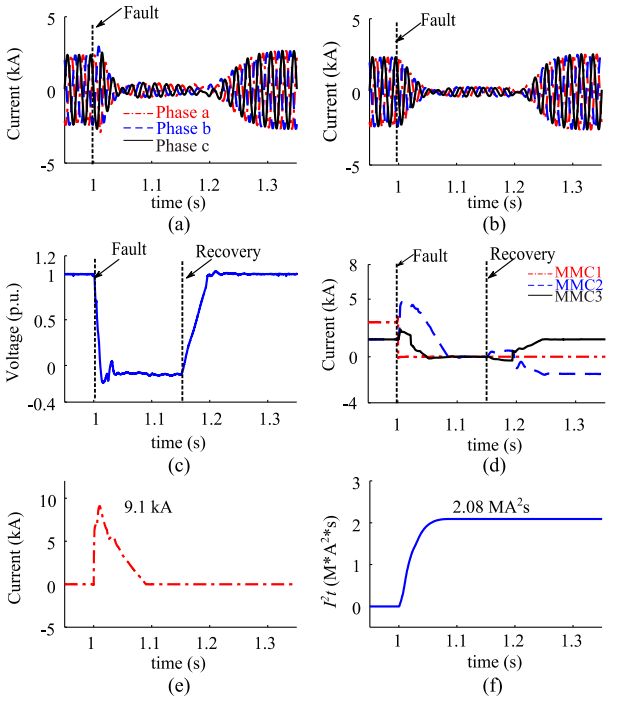
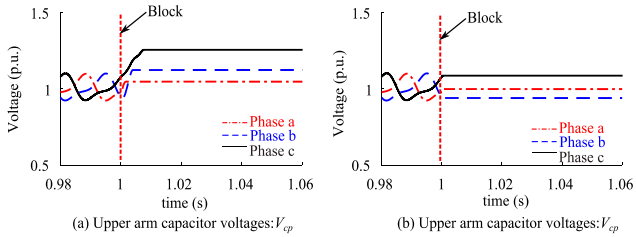


Fig. 20. Protection and restoration process in a multiterminal system. (a) AC currents of MMC2: i_x. (b) AC currents of MMC3: i_x. (c) DC voltage: u_{dc}. (d) DC currents i_{dc} of MMC 1, 2, 3. (e) Thysitor current: i_{th}. (f) I^2t of thyristor branch.



(a) Upper arm capacitor voltages: V_{cp} (b) Upper arm capacitor voltages: V_{cp}

Fig. 21. Protection performance against valve-side single-phase-to-ground faults. (a) With a hybrid DCCB. (b) With a thyristor branch.

are 9.1 kA and 2.08 MA^{2}s, respectively [see Fig. 20(e) and (f)], which is still within the safe operation area of the selected thyristor (64 kA/20.48 MA^{2}s, see Table I).

G. Thyristor Branch-Based Versus DCCB-Based Method

The thyristor branch-based method is compared to a scheme based on a hybrid DCCB to protect FB-MMCs under valve-side single-phase grounding faults. Simulation results are given in Fig. 21. When a hybrid DCCB is in place, the SMs are still charged to ≈1.3 p.u. [see Fig. 21(a)]. This occurs as it takes at least 3 ms to isolate the FB-MMC from the dc bus. Conversely, since no mechanical switches are required, the operation time of the thyristor branch is faster than that of a hybrid DCCB. As shown in Fig. 21(b), the thyristor branch-based method performs better as the dc voltage reduces to zero quickly.

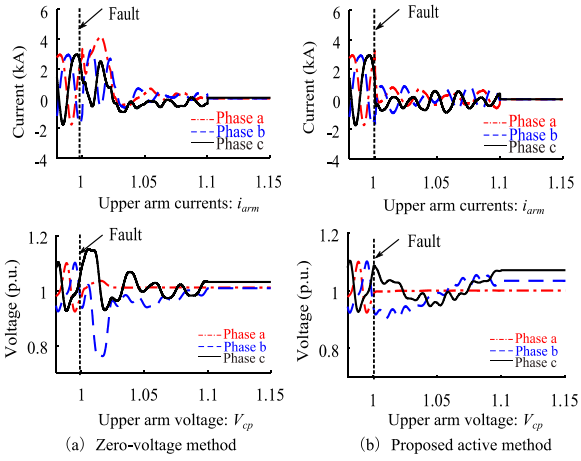


Fig. 22. Comparison of protection schemes in a point-to-point system. (a) Zero-voltage method. (b) Thyristor branch-based active method.

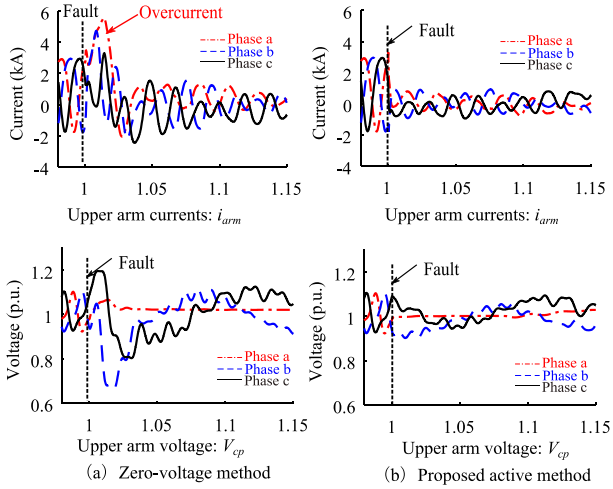


Fig. 23. Comparison of active protection schemes in a three-terminal system. (a) Zero-voltage method. (b) Thyristor branch-based active method.

H. Thyristor Branch-Based Versus Zero-Voltage Method

The performance of the thyristor-based active method is also compared with that of the zero-voltage method reported in [21] through simulations conducted in PSCAD. In the zero-voltage method, the dc-bus voltage is regulated to zero once the fault is detected. A point-to-point system and a three-terminal system are examined. An additional case is also carried out during the active protection process of both methods to justify the inclusion of a thyristor branch.

1) Point-to-Point System: Simulation results are given in Fig. 22, where it can be seen that both schemes can protect the FB-MMC's upper arm SMs from overvoltages, with no arm overcurrents being present. However, the thyristor branch-based method exhibits smaller current and voltage disturbances since the energy stored in the transmission lines is released to the thyristor branch instead of the FB-MMC.

2) Multiterminal System: Simulations have been also performed for a multiterminal system (see Fig. 11), with results given in Fig. 23. For the zero-voltage method, since there are more than one transmission lines injecting dc to the FB-MMC when its dc voltage is regulated to zero, an overcurrent occurs (with a peak value of 5.7 kA)—see the upper arm currents in Fig. 23(a). This current causes overheating of the IGBTs and triggers the overcurrent protection of the FB-MMC as the threshold value is 5 kA. In a real application, the FB-MMC would be blocked. As it can be observed from the upper arm currents in Fig. 23(b), the thyristor branch-based method performs better than the zero-voltage method, without exhibiting overcurrents, since the energy stored in the dc system is released to the thyristor branch instead of the FB-MMC—as in the point-to-point system.

3) Performance When the FB-MMC Is Blocked: An additional simulation is conducted to verify the performance of the two methods when the FB-MMC is blocked due to overcurrent. Fig. 24(a) shows that when the zero-voltage method is employed, the SMs exhibit overvoltages in the upper arms—failing to properly protect the FB-MMC.

Fig. 24(b) shows the performance for the thyristor branch-based protection method. In this case, the FB-MMC is intentionally blocked to conduct a fair comparison with the zero-voltage method given that no overcurrent occurs when the thyristor branch is employed. Blocking occurs 7 ms following the fault. As it can be observed, no overvoltages are exhibited as long as the thyristor branch is triggered.

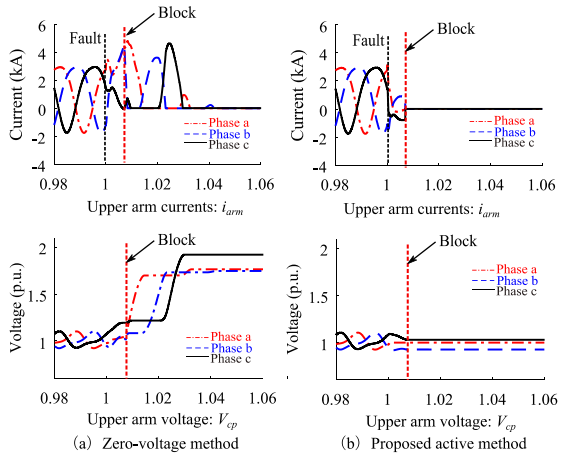


Fig. 24. Blocking of the FB-MMC during the active protection process. (a) Zero-voltage method. (b) Thyristor branch-based active method.

VI. Conclusion

Valve-side single-phase-to-ground faults may result in severe consequences in FB-MMC-based bipolar HVdc systems. In this article, theoretical analyses were conducted to investigate them. It was found that large zero-sequence currents cause overcurrents in arms of the FB-MMC following the fault. In addition, by simply blocking the FB-MMC in the faulted terminal, severe SM overvoltages (nearly 2 p.u.) in the upper arms of the FB-MMC may be exhibited. These overvoltages occur since the dc voltage will charge the SMs during the negative cycles of the ac voltages.

Two protection methods were investigated. In the first one, a thyristor branch-based scheme was employed to effectively eliminate the SM overvoltages. Thus, by blocking the converter and subsequently switching OFF the grid-side ACCB, the fault can be isolated. In the second one, termed active protection method, the FB-MMC is kept active following the fault. This reduces the recovery time of the system for non-permanent faults.

From the presented schemes, the first method investigated in Section III was recommended to isolate permanent faults since most of valve-side faults are permanent. However, additional flexibility was provided by the active protection method investigated in Section IV as it identified whether the fault was permanent or not. This was achieved by injecting a small pulse to the zero-sequence current reference. In the case of a nonpermanent fault, once it disappears, the FB-MMC can rebuild its output voltages quickly. Such a method is recommended to be adopted in systems which are vulnerable to nonpermanent faults and sensitive to the interruption time of power transmission.

The effectiveness of the presented protection methods against valve-side faults was verified through simulations conducted in PSACD both for point-to-point and multiterminal configurations based on FB-MMCs. Although most of the emphasis of this article was on single-phase-to-ground faults, simulations were also conducted for two-phase and three-phase grounding faults. The results illustrated that the schemes effectively protect the faulted FB-MMC after a fault takes place. The peak current and the thermal capacitor (I^2t) of thyristor branch obtained though simulation results can be used as reference to guide the design of the thyristor branch.

To further demonstrate the potential of the thyristor branch-based schemes, comparisons have been drawn against existing protection methods available in the open literature—notably outperforming them. Although adding a thyristor branch may increase the cost of the protection scheme, this would arguably be expected to be lower than that of incorporating additional protective devices such as hybrid DCCBs. Given that the proposed approach reduces the risks posed by overcurrents and is suitable for multiterminal configurations, it represents a cost-effective alternative to protect FB-MMC-based HVdc systems upon valve-side faults.

REFERENCES

[1] D. Jovcic and K. Ahmed, *High-Voltage Direct Current Transmission: Converter System and DC Grids*. Hoboken, NJ, USA: Wiley, 2015.

[2] G. Li, C. Li, and D. van Hertem, "HVDC technology overview," in *HVDC Grid: For Offshore and Supergrid of the Future*. New York, NY, USA: Wiley-IEEE Press, Apr. 2016, ch. 3, pp. 45–78.

[3] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Bologna Power Tech Conf.*, vol. 3, 2003, pp. 110–120.

[4] H. Rao, "Architecture of Nan'ao multi-terminal VSC-HVDC system and its multi-functional control," *CSEE J. Power Energy Syst.*, vol. 1, no. 1, pp. 9–18, Mar. 2015.

[5] G. Tang, Z. He, H. Pang, X. Huang, and X. P. Zhang, "Basic topology and key devices of the five-terminal DC grid," *CSEE J. Power Energy Syst.*, vol. 1, no. 2, pp. 22–35, Jun. 2015.

[6] R. Marquardt, "Modular multilevel converter: An universal concept for HVDC-networks and extended dc-bus-applications," in *Proc. Int. Power Electron. Conf.*, 2010, pp. 502–507.

[7] J. Hafner and B. Jacobson, "Proactive hybrid HVDC breaker—A key innovation for reliable HVDC grid," in *Proc. CIGRE Symp.*, Bologna, China, Sep. 2011, no. 264, pp. 1–9.

[8] D. Jovcic, W. Lin, S. Nguefeu, and H. Saad, "Full bridge MMC converter controller for HVDC operation in normal and DC fault conditions," in *Proc. Int. Symp. Power Electron.*, Novi Sad, Serbia, 2017, pp. 1–6.

[9] S. Wenig, M. Goertz, M. Suriyah, and T. Leibfried, "Active DC fault management of a bipolar full-bridge MMC-HVDC scheme with metallic return," in *Proc. IEEE Int. Energy Conf.*, Leuven, Belgium, 2016, pp. 1–6.

[10] Y. Xue and Z. Xu, "On the bipolar MMC-HVDC topology suitable for bulk power overhead line transmission: Configuration, control, and DC fault analysis," *IEEE Trans. Power Del.*, vol. 29, no. 6, pp. 2420–2429, Dec. 2014.

[11] E. Kontos, R. T. Pinto, S. Rodrigues, and P. Bauer, "Impact of HVDC transmission system topology on multi-terminal DC network faults," *IEEE Trans. Power Del.*, vol. 30, no. 2, pp. 844–852, Apr. 2015.

[12] S. Wenig, M. Goertz, C. Hirsching, M. Suriyah, and T. Leibfried, "On full-bridge bipolar MMC-HVdc control and protection for transient fault and interaction studies," *IEEE Trans. Power Del.*, vol. 33, no. 6, pp. 2864–2873, Dec. 2018.

[13] R. Marquardt, "Modular multilevel converter topologies with DC-short circuit current limitation," in *Proc. 8th Int. Conf. Power Electron.—ECCE Asia*, Jeju, South Korea, 2011, pp. 1425–1431.

[14] X. Li, Y. Liu, L. Yang, Z. Cai, and K. Han, "Research on single phase grounding fault at HVDC converter transformer valve side," in *Proc. 4th Int. Conf. Elect. Utility Deregulation Restruct. Power Technol.*, Shandong, China, 2011, pp. 471–476.

[15] J. Cheng and Z. Xu, "Analysis of AC faults in converter station and characteristics of its relay protection," *Proc. CSEE*, vol. 31, no. 22, pp. 88–95, Aug. 2011.

[16] N. Mei, Y. Li, D. Liu, X. Duan, C. Fu, and H. Rao, "Study on the operational equation for valve short circuit protections in HVDC projects," *Proc. CSEE*, vol. 29, pp. 40–47, Jan. 2009.

[17] J. Yang, J. Zheng, G. Tang, and Z. He, "Internal AC bus fault characteristics of VSC-HVDC system and protection coordination," *Proc. CSEE*, vol. 30, no. 16, pp. 6–11, Jun. 2010.

[18] G. Li, J. Liang, F. Ma, C. E. Ugalde-Loo, and H. Liang, "Analysis of single-phase-to-ground faults at the valve-side of HB-MMCs in HVDC systems," *IEEE Trans. Ind. Electron*, vol. 66, no. 3, pp. 2444–2453, Mar. 2019.

[19] Y. Zhou, Z. He, H. Pang, J. Yang, and Q. Li, "Protection of converter grounding fault on MMC based bipolar HVDC systems," *Proc. CSEE*, vol. 35, no. 16, pp. 4062–4069, Aug. 2015.

[20] T. Jonsson, P. Lundberg, S. Maiti, and Y. Hafner, "Converter technologies and functional requirements for reliable and economical HVDC grid design," in *Proc. CIGRÉ Conf.*, Calgary, AB, Canada, Sep. 2013, pp. 1–9.

[21] W. Yang, Q. Song, H. Rao, S. Xu, and Z. Zhu, "Converter side phase-to-ground fault protection of full-bridge modular multilevel converter-based bipolar HVDC," in *Proc. IEEE Ind. Electron. Soc.*, Beijing, China, 2017, pp. 185–189.

[22] A. Nami, J. Liang, F. Dijkhuizen, and P. Lundberg, "Analysis of modular multilevel converters with DC short circuit fault blocking capability in bipolar HVDC transmission systems," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, Geneva, Switzerland, 2015, pp. 1–10.

[23] L. Tang and B. T. Ooi, "Managing zero sequence in voltage source converter," in *Proc. Conf. Rec. IEEE 37th IAS Annu. Meeting Ind. Appl. Conf.*, Pittsburgh, PA, USA, vol. 2, 2002, pp. 795–802.

[24] G. Li, J. Liang, F. Ma, C. E. Ugalde-Loo, and H. Liang, "Analysis of single-phase-to-ground faults at the valve-side of HB-MMCs in bipolar HVDC systems," in *Proc. IEEE Energy Convers. Congr. Expo.*, Cincinnati, OH, USA, 2017, pp. 2659–2665.

[25] K. Sharifabadi, L. Harnefors, H. P. Nee, S. Norrga, and R. Teodorescu *Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems*. New York, NY, USA: Wiley, 2016.

[26] C. Zhao, Z. Wang, Z. Li, P. Wang, and Y. Li, "Characteristics analysis of capacitor voltage ripples and dimensioning of full-bridge MMC with zero sequence voltage injection," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 2106–2115, Sep. 2019.

[27] X. Li, Q. Song, W. Liu, H. Rao, S. Xu, and L. Li, "Protection of nonpermanent faults on DC overhead lines in MMC-based HVDC systems," *IEEE Trans. Power Del.*, vol. 28, no. 1, pp. 483–490, Jan. 2013.

[28] D. G. Holmes, T. A. Lipo, B. P. McGrath, and W. Y. Kong, "Optimized design of stationary frame three phase AC current regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2417–2426, Nov. 2009.

[29] *Datasheet: Phase Control Thyristor, 5STP 42U6500*, ABB, Zurich, Switzerland, 2018.

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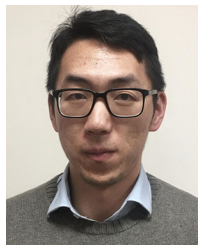

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