Applied Physics Letters

III–V nanowire array telecom lasers on (001) silicon-on-insulator photonic platforms

Cite as: Appl. Phys. Lett. **115**, 213101 (2019); https://doi.org/10.1063/1.5126721
Submitted: 05 September 2019 . Accepted: 08 November 2019 . Published Online: 19 November 2019

Hyunseok Kim, Ting-Yuan Chang, Wook-Jae Lee, and Diana L. Huffaker

Applied Physics Letters ARTICLE scitation.org/journal/apl

III–V nanowire array telecom lasers on (001) silicon-on-insulator photonic platforms

Cite as: Appl. Phys. Lett. **115**, 213101 (2019); doi: 10.1063/1.5126721
Submitted: 5 September 2019 · Accepted: 8 November 2019 ·
Published Online: 19 November 2019

Hyunseok Kim,[1,a)] Ting-Yuan Chang,[1] Wook-Jae Lee,[2] and Diana L. Huffaker[1,3,4]

AFFILIATIONS

[1]Department of Electrical and Computer Engineering, University of California, Los Angeles, Los Angeles, California 90095, USA
[2]Electronics and Telecommunications Research Institute, Daejeon 34129, South Korea
[3]School of Physics and Astronomy, Cardiff University, Cardiff, Wales CF24 3AA, United Kingdom
[4]California NanoSystems Institute, University of California, Los Angeles, Los Angeles, California 90095, USA

[a)]Electronic mail: hyunseokkim@ucla.edu

ABSTRACT

III–V nanowires have recently gained attention as a promising approach to enable monolithic integration of ultracompact lasers on silicon. However, III–V nanowires typically grow only along ⟨111⟩ directions, and thus, it is challenging to integrate nanowire lasers on standard silicon photonic platforms that utilize (001) silicon-on-insulator (SOI) substrates. Here, we propose III–V nanowire lasers on (001) silicon photonic platforms, which are enabled by forming one-dimensional nanowire arrays on (111) sidewalls. The one-dimensional photonic crystal laser cavity has a high Q factor >70 000 with a small footprint of ∼7.2 × 1.0 μm^2, and the lasing wavelengths can be tuned to cover the entire telecom bands by adjusting the nanowire geometry. These nanowire lasers can be coupled to SOI waveguides with a coupling efficiency > 40% while maintaining a sufficiently high Q factor ∼18 000, which will be beneficial for low-threshold and energy-efficient operations. Therefore, the proposed nanowire lasers could be a stepping stone for ultracompact lasers compatible with standard silicon photonic platforms.

Silicon photonics has been emerging as a promising platform for various applications, including chip-scale communications, optical computing, and chemical-, gas-, and biosensing.[1–3] Diverse components constitute silicon photonic chips, such as light sources, photodetectors, waveguides, couplers, and modulators, whereas light sources are regarded as one of the most challenging components to integrate since silicon does not efficiently emit light due to the indirect nature of the silicon bandgap. Because of this, III–V semiconductors with a direct bandgap at telecom wavelengths, such as InGaAs and InGaAsP, are typically integrated on silicon to form light sources. Wafer bonding and flip-chip bonding processes are the most extensively used methods to integrate lasers on silicon photonic chips. However, these processes are costly and time-consuming since small and expensive III–V wafers need to be transferred onto patterned silicon to fabricate laser architectures.[4–6] Another widely studied approach is directly integrating III–V materials on silicon by epitaxy techniques. Although direct growth does not require III–V substrates, directly grown III–V layers are typically defective with low quantum efficiency because of the lattice mismatch between III–V and silicon.[7–9]

Recently, epitaxy of III–V nanowires on silicon has shown promise in direct integration of high-quality III–V materials on silicon. The extremely small interface area between the nanowires and the substrate mitigates the strict requirement for lattice-matching, and thus, it is possible to grow threading dislocation-free nanowires on silicon.[10,11] Furthermore, such a small dimension of nanowires is ideal for fabricating ultracompact light sources on silicon, which can be effectively coupled to silicon waveguides.[12,13] However, one of the challenges in integrating nanowires on silicon chips is that nanowires typically grow only along the ⟨111⟩ directions due to the asymmetry in surface energy with respect to the crystal planes. Although controlled growth of nanowires along non-⟨111⟩ directions has been demonstrated by template-based approaches or by controlling the growth conditions,[14–17] this either requires additional time-consuming processes to make oxide tubes or can be applied only to certain material systems. Because current silicon photonic platforms typically adopt silicon-on-insulator (SOI) substrates with a ⟨001⟩ orientation and a 220 nm thickness silicon layer as a standard,[18] the capability to grow vertical nanowires only along the ⟨111⟩ direction seriously undermines the compatibility of nanowire-based approaches with current silicon photonics.

To overcome this issue, here we propose an alternative way to monolithically integrate III–V nanowire array lasers on SOI (001) and

coupled to silicon waveguides. One-dimensional (1D) photonic crystal laser cavities are formed by defining (111) sidewalls on 220 nm-thick SOI (001) layers and then growing 1D nanowire arrays on the (111) planes. These nanowire lasers can operate at telecom wavelengths such as 1310 nm and 1550 nm by tuning the cavity geometry and material composition. The lasers exhibit an extremely small footprint of $<9 \times 1\ \mu m^2$ and can be coupled to SOI waveguides with a high coupling efficiency >40%, suggesting that the proposed nanowire lasers could be utilized as ultracompact and efficient light sources for silicon photonics.

The schematic of the proposed lasers is depicted in Fig. 1(a). A standard 220 nm-thick SOI (001) is employed for the compatibility with silicon photonic platforms, and a silicon stripe with (111) sidewalls, which is inclined by 54.7° from the surface, is formed by wet chemical etching, as shown in Fig. 1(b). The other sidewall of the stripe is etched vertically with a 40 nm-thick silicon slab remaining on the buried oxide layer, which is for cointegration of waveguides, which will be discussed in the later part of this letter. A 1D nanowire array is integrated on the wet-etched sidewall, and since smooth (111) sidewalls can be obtained by controlling the wet etching condition, nanowires grow vertically with respect to the inclined sidewall. It should be noted that vertical growth of nanowires on wet-etched (111) sidewalls has been demonstrated by metal-catalyzed growth on III–V substrates[19] and by random growth on silicon,[20] substantiating the feasibility of this approach, while control of their positions on silicon platforms has not been demonstrated yet. Silicon dioxide shows high etch rate selectivity to silicon in KOH and TMAH solutions, and thus, the buried oxide layer will act as an etch-stop layer and ensure the formation of smooth (111) sidewalls.[21]

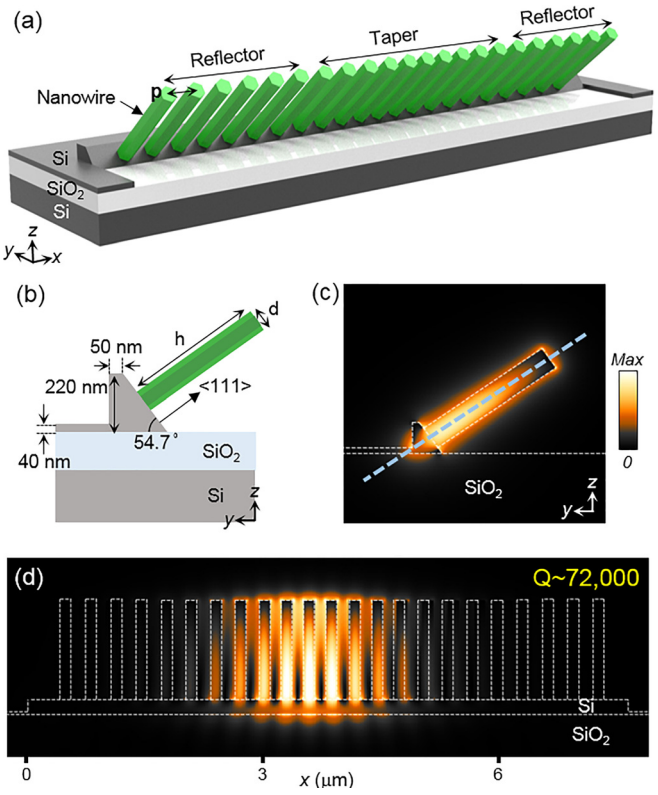

FIG. 1. (a) Schematic of the proposed nanowire array lasers on (111) sidewall of SOI (001) and (b) dimensions of the SOI structure. (c) Electric field profiles ($|E|$) of the yz-plane and (d) cross section along the dashed plane in (c), showing the tightly confined field in nanowires.

The nanowires ordered along the x-axis in Fig. 1(a) constitute a 1D photonic crystal. It has been already shown that 1D photonic crystals with artificial defects can exhibit high quality (Q) factors, for both hole-type[22] and rod-type[23] structures, while occupying very small device footprints. In our design, the pitch of nanowires in the center is tuned (tapered section) while keeping the pitch of the nanowires at the edges constant (reflector section) to make an artificial defect in a 1D resonator and form a high-Q mode in the photonic bandgap. Specifically, the tapered section of nanowires is composed of 11 nanowires, with the pitch decreasing linearly by 10 nm as it approaches the center, resulting in the pitch of nanowires in the center 50 nm shorter than the reflector section. The photonic bandgap enables optical confinement along the x-axis, and although nanowires are tilted from the substrate normal, total internal reflection still applies to the other axes via the nanowire/air interface and silicon/buried oxide interface, leading to high-Q values.

The cavity properties are studied in detail by three-dimensional finite-difference time-domain (3D FDTD) simulations (FDTD Solutions, Lumerical). In all simulations, the refractive index of nanowires is set to 3.62, assuming that InGaAs nanowires are employed, and the indices of silicon and silicon dioxide are adopted from Ref. 24. The Q factor is calculated from the rate of electromagnetic fields of the cavity mode decaying inside the cavity. The dimensions of cavity structures are shown in Fig. 1(b), and the nanowire height (h) is fixed to 1000 nm. Figures 1(c) and 1(d) show representative electric field profiles when the total number of nanowires (N) is 21 and the nanowire diameter is 170 nm. The cavity wavelength is 1306 nm, which is a technologically important telecom wavelength, with the Q factor around 72 000, corresponding to the spectral full-width at half-maximum (FWHM) linewidth of ~0.02 nm when the cavity is transparent. Besides the high Q factor, the electric field is tightly confined in the nanowires, resulting in an extremely small mode volume (V_{mode}) of [$V_{mode} = 0.86 \times (\lambda/n)^3$], which is on the subwavelength scale, and the confinement factor as large as 0.53. Such a high Q factor, small mode volume, and high confinement factor will all contribute to low-threshold lasing.[25] It is also worthwhile to mention that the footprint of the cavity is extremely small around $\sim 7.2 \times 1.0\ \mu m^2$.

Next, the effect of the cavity geometry is further explored by 3D FDTD simulations. The effect of the reflector size (i.e., the number of nanowires constituting the reflector) is first studied with the nanowire height and diameter fixed at 1000 nm and 170 nm, respectively [Fig. 2(a)]. When the total number of nanowires is 11, meaning that there is no reflector, the Q factor is small around ~260 due to the weak confinement along the x-axis. The Q factor rapidly increases as the number of reflector nanowires is increased and saturates around $N = 21$, meaning that other sources of loss mechanisms such as the phase mismatch and scattering at the interfaces start to dominate, while the cavity mode wavelength remains almost unchanged when the number of reflector nanowires is varied. For example, the silicon stripe with a trapezoid-shape cross section [Fig. 1(b)] is a source of loss since the refractive index of silicon is larger than the effective

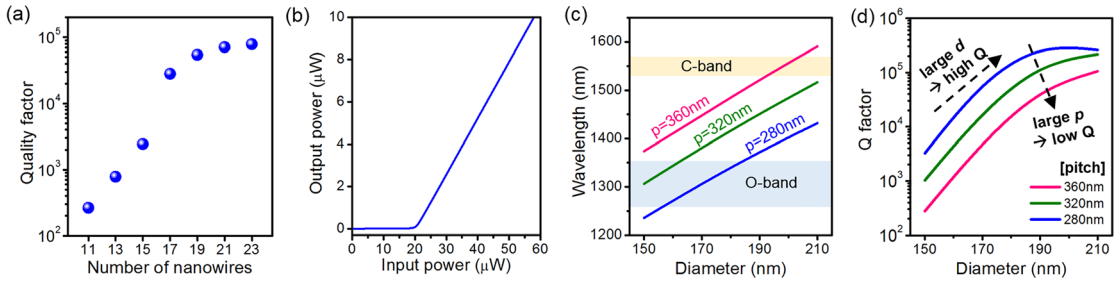

FIG. 2. (a) Cavity Q factor as a function of the number of nanowires. (b) L-L curve calculated from rate equations. (c) and (d) Cavity mode wavelength and Q factor as a function of the nanowire diameter, *d*, and the pitch, *p*.

index of the 1D nanowire array, resulting in a phase mismatch. Reducing the size of the silicon stripe therefore increases the Q factor, while this might increase the fabrication difficulty.

Based on the cavity geometry and cavity properties derived from FDTD simulations, lasing threshold of the proposed nanowire lasers operating at 1310 nm is calculated using rate equations when $N = 21$. The rate equations are modified to reflect optical pumping conditions,[12] and the material properties of InGaAs nanowires with their bandgap overlapping with the 1310 nm band are adopted from Ref. 26, assuming room-temperature operation. The calculated light-light (L-L) curve in Fig. 2(b) shows a clear kink at the input power of 20 μW, which indicates the lasing threshold of the proposed laser. Here, we note that the input power represents the power absorbed by nanowires, not the actual power of the pump beam, and thus, the ratio of output power and input power in Fig. 2(b) corresponds to the radiative quantum efficiency, not external quantum efficiency. While such a low lasing threshold has been achieved in air-hole type photonic crystal slab cavities,[27] lasing thresholds of nanowire-based lasers are typically much higher due to their low Q factor.[28,29] Therefore, the proposed design could bridge the gap and provide a path toward low-threshold and ultracompact monolithic lasers on silicon.

Another advantage of the nanowire array cavities is that the lasing wavelengths can be lithographically tuned by adjusting the pitch and diameter of nanowires, which has been experimentally demonstrated on (111) substrates.[26,30,31] Figure 2(c) shows that the fundamental peak wavelength of the cavity can be increased by either making the pitch larger or the nanowires fatter since the enlarged period in real space corresponds to a smaller period (longer wavelength) in k-space. This implies that there can be multiple combinations of pitches and diameters that exhibit an identical fundamental peak wavelength. In other words, the cavity wavelength can be kept constant by increasing (decreasing) the diameter and decreasing (increasing) the pitch, while it should be noted that the Q factor varies depending on the cavity geometry. In general, as shown in Fig. 2(d), the Q factor increases when the diameter is increased or the pitch is decreased. This is because the fill factor of the cavity (the portion of nanowire volume) increases in both cases, leading to a higher effective index of the cavity. The higher effective index corresponds to the higher index contrast of the cavity with the surrounding environment (cavity/air and cavity/silicon dioxide), and the higher index contrast increases the Q factor by reduced scattering due to the total internal reflection. The only exception shown in Fig. 2(d) is the decrease in the Q factor when the diameter is increased from 200 nm to 210 nm when the pitch is 280 nm. This is because the gap between nanowires gets extremely small in the tapered section (the distance is only 10 nm between the center nanowire and adjacent nanowires when the diameter is 210 nm and the pitch is 280 nm), and the offset of 10 nm in the tapered section induces a large phase-mismatch in this case. In short, the general design rule to realize high-Q cavities is employing fatter nanowires with narrower pitches.

It is possible to extend the cavity wavelength to another technologically important telecom band at 1550 nm by adjusting the cavity geometry, while the material composition of III–V nanowires needs to be tuned accordingly to match the optical gain with the cavity mode and achieve lasing.[26] Such a capability to tune the lasing wavelength could enable wavelength-division multiplexing (WDM) by integrating arrays of nanowire lasers with different dimensions on chip. In addition, the electric field of the cavity mode is aligned to the longitudinal direction of nanowires, which is rotated by 54.7° from the z-axis to the y-axis. We point out that the mixed TE-TM mode of the proposed laser cavity could potentially be utilized for a polarization-entanglement source that generates quantum-correlated photon pairs through spontaneous parametric downconversion in the III–V nanowires with a high second-order nonlinear optical response.[32]

Coupling of the on-chip laser with other components is a crucial requirement for practical applications. Here, we show an efficient coupling scheme to conventional rib waveguides. The waveguide is attached at the end of the cavity, as shown in Fig. 3(a). The width and height of the rib waveguide are 440 nm and 180 nm, respectively, which supports single mode at telecom wavelengths. The nanowire lasers coupled with waveguides can be fabricated by the processes shown in Fig. 3(b). First, an inclined (111) sidewall is exposed on SOI (001) by standard lithography and wet chemical etching. Next, a vertical sidewall on the other side of the stripe is patterned together with silicon waveguides by dry etching. A 40 nm-thick slab is left to form a rib waveguide and also potential for electrical connection on silicon photonic chips. A dielectric mask such as silicon nitride is then conformally deposited, followed by electron beam lithography and dry etching to expose nanoholes on (111) sidewalls as a nanowire growth template. Finally, nanowires are grown by selective-area epitaxy, and if necessary, the dielectric mask can be selectively removed by dry etching after the nanowire growth.

If a silicon waveguide is directly attached at the end of a nanowire array cavity when $N = 21$, the coupling efficiency is calculated to be only 0.23% because the high-Q cavity mode is strongly confined in the taper section and does not couple to the waveguide. Thus, the coupling

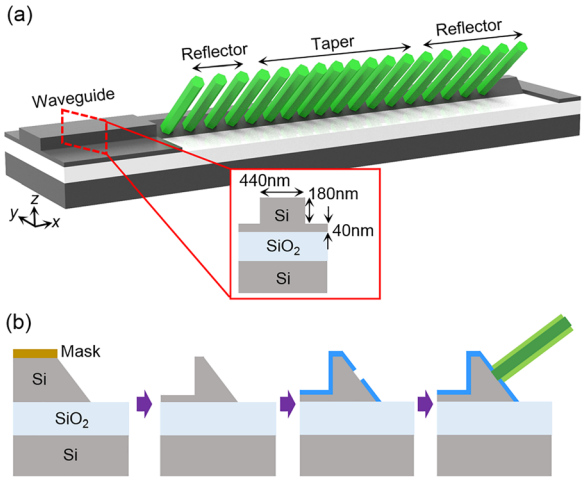

FIG. 3. (a) Schematic of waveguide-coupled nanowire array lasers. Inset: cross section of the waveguide. (b) Fabrication processes for waveguide-coupled nanowire lasers.

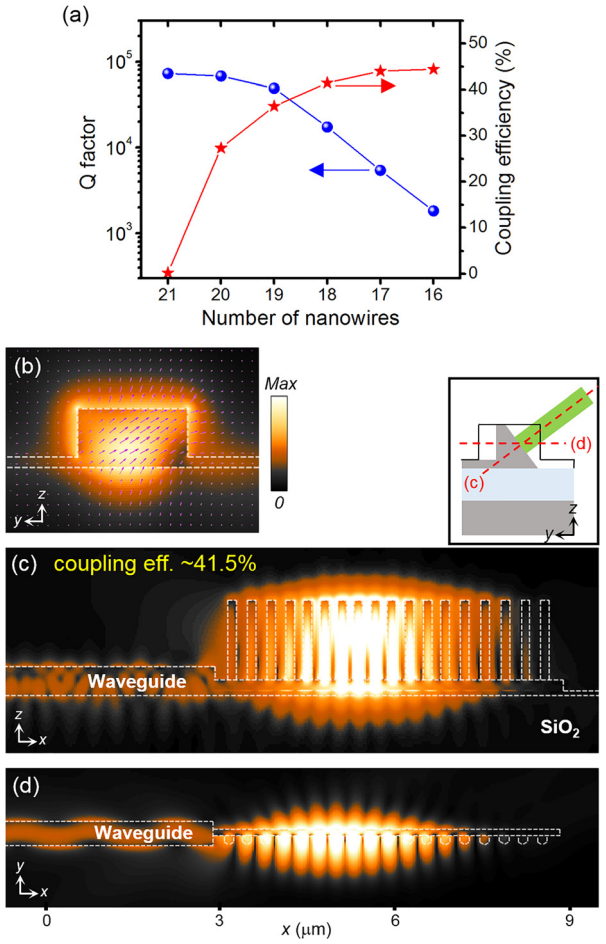

FIG. 4. (a) Change in the cavity Q factor and the coupling efficiency by removing nanowires. (b) Electric field (|*E*|) intensities and vector field (arrow) of the waveguide cross section. (c) and (d) Electric field (|*E*|) profiles plotted along the dashed line in the inset, showing the coupled mode profile with the SOI waveguide. The black line in the inset indicates the boundary of the silicon waveguide.

efficiency can be enhanced by making the cavity "leakier" toward the waveguide by removing some of the reflector nanowires between the taper section and the waveguide. As shown in Fig. 4(a), the coupling efficiency greatly enhances by removing the reflector nanowires and making the cavity asymmetric, while there is a trade-off between the coupling efficiency and the Q factor since efficient waveguide coupling means more energy loss from the cavity. Figures 4(b)–4(d) show the electric field profiles of waveguide-coupled cavity modes when three nanowires between the taper section and the waveguide are removed. We note that the position of the waveguide for butt-coupling to the silicon stripe is also optimized to maximize the coupling efficiency. As noted above, the electric field of the cavity mode is aligned to the longitudinal direction of nanowires, and this resulted in the electric field within the waveguide also being aligned to the same direction, as shown in the vector field in Fig. 4(b). The coupling efficiency is 41.5% under this condition, with the Q factor still sufficiently high around 18 000. A scattering at the cavity-waveguide interface is shown in Figs. 4(c) and 4(d), which implies that the coupling efficiency could be further improved without deteriorating the Q factor, for example, by employing the tapered waveguide or optimizing the geometry of the silicon stripe-waveguide junction. Another possible approach to realize high Q and high coupling efficiency simultaneously is to employ directional coupling by placing a waveguide in parallel to the 1D nanowire array, instead of the butt-coupling scheme shown here. Therefore, if the proposed laser is utilized in on-chip applications, its high coupling efficiency will be beneficial for energy-efficient operation, and its high Q factor will enable both energy-efficient and high-speed operation.[33]

However, for practical applications, electrical injection will be required in most cases, which is not demonstrated in this Letter. For current-injected nanowire lasers, p-i-n junctions with metal contacts are necessary, and this can be achieved by growing p-i-n nanowire heterostructures on doped substrates, followed by dielectric spacer formation and patterning of top metal contacts. Although these processes have already shown their effectiveness in fabricating nanowire-based optoelectronic devices,[34] additional challenges are expected in realizing electrically injected nanowire lasers. First, introduction of metal contacts and dielectric spacers will degrade the cavity Q factor due to lower index contrast between dielectric and air and also due to the absorption by metal, resulting in increased lasing threshold. Second, and more importantly, electrical injection typically induces additional loss of carriers by nonradiative recombination and Joule heating, compared to optical pumping, and thus, effective heat management is critical to achieve lasing at room temperature without thermal degradation. Therefore, careful design of cavity geometry including metals will be crucial for achieving electrical injection.

In conclusion, we have proposed nanowire array laser cavities on SOI (001) platforms, which can operate at telecom wavelengths and can be coupled to waveguides. By monolithically integrating nanowires on (111) sidewalls of SOI (001), which is exposed by wet chemical etching, 1D cavities with a high Q factor and compact sizes can be formed without the need for III–V wafer bonding processes. The operation wavelengths of the lasers can span a wide range by tuning the

cavity geometry, providing a path toward wavelength-division multiplexing. The proposed nanowire array laser cavities can be efficiently coupled to conventional waveguides on SOI chips while maintaining a high Q factor, suggesting that the proposed nanowire lasers could be a building block for monolithic light sources on silicon photonic platforms.

The authors acknowledge the generous financial support of this research by the Air Force Office of Scientific Research (AFOSR) (No. FA9550-15-1-0324), National Science Foundation (NSF) (No. ECCS-1711967), and Sêr Cymru grants in Advanced Engineering and Materials.

REFERENCES

[1]J. K. Doylend and A. P. Knights, "The evolution of silicon photonics as an enabling technology for optical interconnection," Laser Photonics Rev. **6**(4), 504–525 (2012).
[2]Y. Jiang, P. T. S. DeVore, and B. Jalali, "Analog optical computing primitives in silicon photonics," Opt. Lett. **41**(6), 1273–1276 (2016).
[3]N. A. Yebo, P. Lommens, Z. Hens, and R. Baets, "An integrated optic ethanol vapor sensor based on a silicon-on-insulator microring resonator coated with a porous ZnO film," Opt. Express **18**(11), 11859–11866 (2010).
[4]H. Park, A. W. Fang, S. Kodama, and J. E. Bowers, "Hybrid silicon evanescent laser fabricated with a silicon waveguide and III-V offset quantum wells," Opt. Express **13**(23), 9460–9464 (2005).
[5]S. Keyvaninia, M. Muneeb, S. Stanković, P. J. Van Veldhoven, D. Van Thourhout, and G. Roelkens, "Ultra-thin DVS-BCB adhesive bonding of III-V wafers, dies and multiple dies to a patterned silicon-on-insulator substrate," Opt. Mater. Express **3**(1), 35–46 (2013).
[6]A. W. Fang, H. Park, O. Cohen, R. Jones, M. J. Paniccia, and J. E. Bowers, "Electrically pumped hybrid AlGaInAs-silicon evanescent laser," Opt. Express **14**(2), 9203–9210 (2006).
[7]A. Y. Liu, S. Srinivasan, J. Norman, A. C. Gossard, and J. E. Bowers, "Quantum dot lasers for silicon photonics," Photonics Res. **3**(5), B1–B9 (2015).
[8]S. Chen, W. Li, J. Wu, Q. Jiang, M. Tang, S. Shutts, S. N. Elliott, A. Sobiesierski, A. J. Seeds, I. Ross, P. M. Smowton, and S. Liu, "Electrically pumped continuous-wave III–V quantum dot lasers on silicon," Nat. Photonics **10**, 307–311 (2016).
[9]Q. Li, K. W. Ng, and K. M. Lau, "Growing antiphase-domain-free GaAs thin films out of highly ordered planar nanowire arrays on exact (001) silicon," Appl. Phys. Lett. **106**(7), 072105 (2015).
[10]H. Kim, A. C. Farrell, P. Senanayake, W.-J. Lee, and D. L. Huffaker, "Monolithically integrated InGaAs nanowires on 3D structured silicon-on-insulator as a new platform for full optical links," Nano Lett. **16**, 1833–1839 (2016).
[11]H. Kim, D. Ren, A. C. Farrell, and D. L. Huffaker, "Catalyst-free selective-area epitaxy of GaAs nanowires by metal-organic chemical vapor deposition using triethylgallium," Nanotechnology **29**, 085601 (2018).
[12]H. Kim, W.-J. Lee, A. C. Farrell, J. S. D. Morales, P. Senanayake, S. V. Prikhodko, T. J. Ochalski, and D. L. Huffaker, "Monolithic InGaAs nanowire array lasers on silicon-on-insulator operating at room temperature," Nano Lett. **17**, 3465–3470 (2017).
[13]W.-J. Lee, H. Kim, A. C. Farrell, P. Senanayake, and D. L. Huffaker, "Nanopillar array band-edge laser cavities on silicon-on-insulator for monolithic integrated light sources," Appl. Phys. Lett. **108**, 081108 (2016).
[14]M. Borg, H. Schmid, K. E. Moselund, G. Signorello, L. Ginac, J. Bruley, C. Breslin, P. Das Kanungo, P. Werner, and H. Riel, "Vertical III-V nanowire device integration on Si(100)," Nano Lett. **14**, 1914–1920 (2014).
[15]Z.-A. Li, C. Moller, V. Migunov, M. Spasova, M. Farle, A. Lysov, C. Gutsche, I. Regolin, W. Prost, F.-J. Tegude, and P. Ericius, "Planar-defect characteristics and cross-sections of <001>, <111>, and <112> InAs nanowires," J. Appl. Phys. **109**, 114320 (2011).
[16]J. Wang, S. Plissard, M. Hocevar, T. T. T. Vu, T. Zehender, G. G. W. Immink, M. A. Verheijen, J. Haverkort, and E. P. A. M. Bakkers, "Position-controlled, [100] InP nanowire arrays," Appl. Phys. Lett. **100**, 053107 (2012).
[17]A. Cavalli, J. Wang, I. E. Zadeh, M. E. Reimer, M. A. Verheijen, M. Soini, S. R. Plissard, V. Zwiller, J. E. M. Haverkort, and E. P. A. M. Bakkers, "High-yield growth and characterization of ⟨100⟩ InP p-n diode nanowires," Nano Lett. **16**, 3071–3077 (2016).
[18]D.-X. Xu, J. H. Schmid, G. T. Reed, G. Z. Mashanovich, D. J. Thomson, M. Nedeljkovic, X. Chen, D. Van Thourhout, S. Keyvaninia, and S. K. Selvaraja, "Silicon photonic integration platform-have we found the sweet spot?," IEEE J. Sel. Top. Quantum Electron. **20**(4), 189–205 (2014).
[19]S. Gazibegovic, D. Car, H. Zhang, S. C. Balk, J. A. Logan, M. W. A. de Moor, M. C. Cassidy, R. Schmits, D. Xu, G. Wang, P. Krogstrup, R. L. M. Op het Veld, K. Zuo, Y. Vos, J. Shen, D. Bouman, B. Shojaei, D. Pennachio, J. S. Lee, P. J. van Veldhoven, S. Koelling, M. A. Verheijen, L. P. Kouwenhoven, C. J. Palmstrøm, and E. P. A. M. Bakkers, "Epitaxy of advanced nanowire quantum devices," Nature **548**, 434–438 (2017).
[20]F. Lu, T.-T. D. Tran, W. S. Ko, K. W. Ng, R. Chen, and C. C. Hasnain, "Nanolasers grown on silicon-based MOSFETs," Opt. Express **20**(11), 12171–12176 (2012).
[21]H. Kim, J. M. Kim, Y. S. Bang, E. S. Song, C. H. Ji, and Y. K. Kim, "Fabrication of a vertical sidewall using double-sided anisotropic etching of <100> oriented silicon," J. Micromech. Micromach. **22**(9), 095014 (2012).
[22]M. Notomi, E. Kuramochi, and H. Taniyama, "Ultrahigh-Q nanocavity with 1D photonic gap," Opt. Express **16**(15), 11095–11102 (2008).
[23]J. D. Joannopoulos, S. G. Johnson, J. N. Winn, and R. D. Meade, *Photonic Crystals: Molding the Flow of Light* (Princeton University Press, Princeton, 2008).
[24]E. D. Palik, *Handbook of Optical Constants of Solids* (Academic Press, Cambridge, 1998).
[25]J. T. Robinson, C. Manolatou, L. Chen, and M. Lipson, "Ultrasmall mode volumes in dielectric optical microcavities," Phys. Rev. Lett. **95**(14), 143901 (2005).
[26]H. Kim, W.-J. Lee, A. C. Farrell, A. Balgarkashi, and D. L. Huffaker, "Telecom-wavelength bottom-up nanobeam lasers on silicon-on-insulator," Nano Lett. **17**, 5244–5250 (2017).
[27]M. Nomura, S. Iwamoto, M. Nishioka, S. Ishida, and Y. Arakawa, "Highly efficient optical pumping of photonic crystal nanocavity lasers using cavity resonant excitation," Appl. Phys. Lett. **89**, 161111 (2016).
[28]D. Saxena, S. Mokkapati, P. Parkinson, N. Jiang, Q. Gao, H. H. Tan, and C. Jagadish, "Optically pumped room-temperature GaAs nanowire lasers," Nat. Photonics **7**, 963–968 (2013).
[29]T. Stettner, T. Kostenbader, D. Ruhstorfer, J. Bissinger, H. Riedl, M. Kaniber, G. Koblmüller, and J. J. Finley, "Direct coupling of coherent emission from site-selectively grown III–V nanowire lasers into proximal silicon waveguides," ACS Photonics **4**(10), 2537–2543 (2017).
[30]W.-J. Lee, H. Kim, J.-B. You, and D. L. Huffaker, "Ultracompact bottom-up photonic crystal lasers on silicon-on-insulator," Sci. Rep. **7**, 9543 (2017).
[31]H. Kim, W.-J. Lee, T.-Y. Chang, and D. L. Huffaker, "Room-temperature InGaAs nanowire array band-edge lasers on patterned silicon-on-insulator platforms," Phys. Status Solidi-RRL **13**, 1800489 (2018).
[32]A. Orieux, A. Eckstein, A. Lemaitre, P. Filloux, I. Favero, G. Leo, T. Coudreau, A. Keller, P. Milman, and S. Ducci, "Direct bell states generation on a III-V semiconductor chip at room temperature," Phys. Rev. Lett. **110**, 160502 (2013).
[33]H. Altug, D. Englund, and J. Vučković, "Ultrafast photonic crystal nanocavity laser," Nat. Phys. **2**, 484–488 (2006).
[34]A. C. Farrell, X. Meng, D. Ren, H. Kim, P. Senanayake, N. Y. Hsieh, Z. Rong, T.-Y. Chang, K. M. Azizur-Rahman, and D. L. Huffaker, "InGaAs–GaAs nanowire avalanche photodiodes toward single-photon detection in free-running mode," Nano Lett. **19**(1), 582–590 (2019).