Cardiff University

Technology Development for Nanoscale InSb Quantum Split-Gate Structures

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“Study hard what interests you the most in the most undisciplined, irreverent and original manner possible.”

– Richard Feynman

ABSTRACT

In this project some of the challenges of novel InSb based semiconducting material are investigated. Various features of electron transport in low dimensional semiconductors were studied for AlInSb/InSb quantum well (QW) two-dimensional electron gas (2DEG) heterostructures with an emphasis placed on realising one-dimensional systems (which exhibit quantum phenomena where the conductance takes on a discrete 'step-like' nature).

This material allows us to take advantage of very extreme material parameters such as light effective mass, the lowest binary material band gap, the highest electron mobility at room temperature, and an extremely large effective g-factor (with associated spin orbit coupling). However, this material still has significant challenges due to the large mismatch between the substrate GaAs and the QW, which produces threading dislocations that lead to limitations in mobility.

Surface roughness has been investigated as a result of shallow etching for Ohmic contact deposition on the AlInSb/InSb wafer. Both dry and wet techniques have been investigated, and their effect on the electron transport as a function of roughness, primarily using Transmission Length Measurement (TLM). In addition, the Ohmic contact resistivity was investigated as a function of depth over a wide range of temperatures to extract an effective contact barrier. The contact potential barrier was found to have a strong effect at low temperatures, which leads to a non-linear I-V characteristic.

Finally, this thesis studied different designs of nanoscale split gate structures that were fabricated on this state of the art InSb QW 2DEG material. This material was grown by collaborators at Sheffield University at the National Centre for III-V technologies. The devices were fabricated at Cardiff using photo-lithography and nanoscale electron beam lithography (EBL) using recipes tailored to this material.

DEDICATION

*I dedicate this work to my parents; **Ismael** and **Zainab**, to my brothers; **Qaiser**, **Khalid**, **Nashaat**, **Osama** and **Naseem**, to my wife; **Sally**, and to my children; **Teeba**, **Zainab**, **AbdurRahman** and **Alleen**, who are a constant source of motivation, and who inspire me to strive to be the best person I could possibly be. I could not have taken this opportunity if they had not helped me through the early stages of my education with patience and encouragement.*

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LIST OF ABBREVIATIONS

MBE	Molecular Beam Epitaxy
QW	Quantum Well
2DEG	2-Dimensional Electron Gas
DOS	Density of States
TLM	Transmission Line Model
LTLM	Linear Transmission Line Model
IFRS	Interface Roughness Scattering
XPS	X-ray photoelectron spectroscopy
EDX	Energy Dispersive X-ray Spectroscopy
AFM	Atomic Force Microscopy
EBL	Electron Beam Lithography
SEM	Scanning Electron Microscopy
PMMA	Poly (Methyl MethAcrylate)
IBM	Ion Beam Milling
FWHM	Full Width at Half Maximum
RMS	Root Mean Square
TDs	Threading Dislocations
TEM	Transmission Electron Microscope
RTA	Rapid Thermal Annealing
I-V	Current Voltage
FE	Field Emission
I-V-T	Current Voltage Temperature
MS	Metal Semiconductor
TE	Thermionic Emission
TFE	Thermionic Field Emission

Chapter 1

Introduction

1.1 Motivation

The semiconducting properties of indium antimonide (InSb) first became known in the early 1950s [1]–[4]. Numerous scientific investigations have since been performed on this material. However, even after 60 years of research, the growth of InSb crystals and their characterisation continues to evoke keen interest due to their innovative properties and their novel technological applications in areas such as thermal imaging and more recently nanoscale electronic devices [5]–[7].

Nanoscale quantum devices have attracted attention over recent years, and they have yielded some landmark fundamental studies of electronic states in matter, as well as potential applications in metrology and single electron sensing in quantum computing qubit implementations. A high-quality InSb quantum well (QW) two-dimensional electron gas (2DEG) is highly desired because of its unique and extreme properties compared to all other binary III-V compound semiconductors, having the narrowest band gap, lightest electron effective mass, largest Landé *g*-factor and highest intrinsic electron mobility amongst the currently known binary III-V compounds. These novel properties allow for a wide range of potential applications in nanoscale electronics and optoelectronics. This means that InSb QWs are an interesting material for fabricating high-speed and low power devices, spintronic devices, magnetic field sensors, middle-to-long wavelength photon detectors, and so on [8]–[13]. *Table 1.1* shows some of the fundamental properties of the intrinsic semiconductors Si and Ge, as well as III-V compound semiconductor materials. InSb is a direct bandgap semiconductor with energy band gap (E_g)=0.235 eV at low temperature because of its conventional negative temperature coefficient. The energy gap decreases to about 0.22 eV and 0.18 eV at 77K and room temperature, respectively [14]–[16].

InSb's mobility (μ_e =78000 $cm^2V^{-1}s^{-1}$) is the highest reported electron mobility at room temperature in comparison to any compound semiconductor. It has been reported to have mobilities in excess of (200000 $cm^2V^{-1}s^{-1}$) at 1.8K in two-dimensional electron gas (2DEG) channels [17]–[20], which is respectable, but still low in comparison to other materials, such as GaAs. This is due primarily to threading dislocations coming from lattice mismatch of the 2DEG and the substrate.

InSb exhibits the lightest electron effective mass ($m^*=0.014m_e$) at room temperature. The corresponding high-mobility possible allows for low power consumption devices to be realized [21]. Moreover, it can exhibit effects of quantisation phenomenon at higher temperatures than other materials, (following the Landauer equation [22]). Furthermore, the large *g*-factor makes its electron spin interaction extremely strong. This makes it an ideal material to study spin phenomenon and also facilitates potential exploitation in spintronics and quantum information control [23]–[25]. One of the aspects of potential qubit structures is the successful implementation of flexible surface gated split gate structures for charge sensing (in any spin to charge conversion scheme). Consequently, there is high potential in studying quantized conductance in this material system, and further investigation into the well-known 0.7 conductance anomaly in such a rich spin system may well yield interesting physics. Additionally, the realisation of a superconducting top gate offers the possibility of investigating Majorana physics [26] [27], as a result of the high g-factor.

Despite the apparent advantages of this materials system, significant challenges exist with the basic technology. In particular, ohmic contact technology is frequently inconsistent and with poor contact resistance. It is not well understood what causes this. Standard III-V NiGe:Ni:Au alloyed contacts will not work with this material due to thermal budgets (typical crystal growth temperatures are lower than traditional 385°C contact anneal temperatures. As a result of the variety of applications, there is a high-demand for accurate measurements to evaluate and optimize the contact resistance and specific contact resistance of metal/semiconductor contacts that limit device performance [28].

Table 1.1: Fundamental properties of some semiconductor materials, including direct energy band gap E_g, electron effective mass m, electron g-factor and electron mobility at 300K [11][15][17][29].*

System	Material	$E_g(\Gamma)$ (eV)	$m^*(m_o)$	g-Factor	μ_e ($cm^2V^{-1}s^{-1}$)
IV	Si	1.2	0.190	1.9	1450
	Ge	0.80	0.081	1.6	3900
III-V	GaAs	1.42	0.064	-0.4	8000
	InAs	0.35	0.023	-15.6	33000
	InSb	***0.18***	***0.014***	***-50.6***	***78000***

Despite these impressive features of InSb, many challenges remain. InSb QW growth on GaAs substrates with a large mismatch is an engineering challenge due to the significant strain in the crystal layers. This leads to the inevitable creation of high densities of dislocations, which adversely impact the mobility of the material and significantly degrade the performance of the device (such as gate leakage). This issue has led to a significant effort to eliminate the density of defects using for example super lattice layers, buffer layers, dislocations filtering, and decreasing the surface roughness to release the strain between the layers and improve the material's mobility [26][30]–[37]. Whilst not entirely solving the problems of mismatch, these improvements of the InSb material mobility have encouraged further investigations and applications, such as in high sensitivity magnetic field sensors, high frequency electronics and quantum computer technology [38]. Therefore, quantum devices that utilize the ballistic transport of the carriers will be very attractive for this purpose [39].

1.2 Thesis Outline

This research was performed at Cardiff University and it focused on characterising InSb QW 2DEG material, developing metal-semiconductor gate and Ohmic contact technology, and studying electron transport mechanisms and ballistic electron transport in InSb QW 2DEG split gate structures. This thesis is structured as follows.

Chapter 2 describes the physical concepts of the QW and low-dimensional electronic confinement in semiconductor heterostructure systems, specifically for aluminium indium antimonide/indium antimonide (AlInSb/InSb). The ballistic transport mechanism in 2DEG leading to quantisation conductance by using surface split gate

structures is then described. The electron transport mechanisms through metal-semiconductor (Ohmic) contacts are discussed using the "Transmission Line Model" (TLM) measurement technique.

Chapter 3 gives an overview of the structure of an InSb crystal, and in the case of the samples studied here, the epitaxial layers and its bandgap engineering, along with a description of the wafer fabrication and characterisation techniques. The split gate and TLM devices designs are described in detail, together with the techniques that were used in the fabrication process. Moreover, the sample packaging, wiring, electrical measurement techniques and variable low temperature set up are also described.

Chapter 4 describes the experimental study of the wafer surface roughness of AlInSb/InSb for a pristine sample and for a variety of surface etched samples. Wet and dry etching techniques are used to etch the Ohmic contact area over a range of depths into the QW layer and comparisons are made. An atomic force microscope (AFM) is used to create surface topography images of etched areas, which were then analysed mathematically using Python code.

Chapter 5 investigates metal-semiconductor contact resistance, sheet resistance and contact resistivity as a function of etching depth, with variable temperatures related to electron transport mechanisms, using the TLM technique.

Chapter 6 looks at different designs of surface metal gates and studies the transport that results in quantum conductance. The quantisation conductance is achieved by applying a source-drain voltage via Ohmic contacts and DC voltage on the top gate to increase the resistance, resulting in conductance steps. The results for a range of device designs at low temperature (2.7K) are given here.

Chapter 7 summarises the results from the research undertaken in this thesis, and it briefly discusses future possible research areas.

Appendix is included at the end of the thesis in which relevant addition details are provided for the simulations that were performed. Appendix A includes the theory concepts of an additional kind of TLM, which is a "circular" or "bullseye" CTLM.

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Chapter 2

Theory and Background

2.1 Introduction

Semiconductor materials that consist of two or more elements from the periodic table are known as compound semiconductors and they include binary compounds such as indium antimonide (InSb) and ternary alloys such as aluminium indium antimonide (AlInSb). Compound semiconductors that are derived of elements from group three and five of the periodic table are generally known as III–V semiconductors. Whilst it is not used widely, InSb has attractive semiconducting properties and this has led to interest in its uses in many electronic, optoelectronic and electromagnetic devices. This material can be grown by the molecular beam epitaxy (MBE) technique that can achieve high-quality semiconductor crystal growth and enables the growth of, for example, heterostructures and quantum wells (QWs) to be engineered. These dimensions possible for growth enables carrier quantisation effects to be achieved in real semiconductor devices.

InSb nanostructures may allow us to more easily study *ballistic transport* in QWs due to the large mean free path of electrons (as a result of the light electron effective mass). For devices this can result in electrons flow from the filled states one side of a device to flow to empty states without scattering. Consequently, this material should exhibit clear one-dimensional conductance quantization, an important mesoscopic phenomenon. However, in practice, the immature technology of things like the metal–semiconductor contact (Ohmic contact) plays a vital role in overall device performance and can dominate any observable effects.

This chapter begins with an overview of the basic principles of Ohmic contact formation, and the transmission line model technique will then be used to introduce the determination of specific contact resistance, which is the most important property

of Ohmic contacts, as well as the sheet resistance of the InSb QW samples used. Finally, electron scattering mechanisms will be introduced that have influence on the electron mobility, ballistic transport and ultimately observable conductance quantization.

2.2 Quantum Well

A QW is a series of semiconductor layers grown with a sandwich-like structure with a large difference in energy between the conduction bands of the bottom and top layers and the sandwiched intermediate layer. The electronic properties of InSb and AlInSb materials are well-suited to QW architecture [1]. Hence, the QW cladding layers (AlInSb layers (top and bottom) are thick or the conduction bands potential on both sides are sufficiently high, such that the electron tunnelling out can be considered negligible and the electrons will be confined in the growth direction (conventionally the z direction) and are free to move in the x and y plane of the QW [2]. The electronic states under this confinement are then quantised to a discrete number of energy levels, which are given by solutions of Schrödinger's equation.

The confining potentials in QW heterostructure devices are due to the band offsets (which will be discussed in more detail in Chapter 3) at the interfaces in double-junction QWs [2].

2.2.1 The Finite Quantum Well

The finite QW is sketched in *Figure 2. 1*, which explains the band diagram of an ideal QW with a finite potential barrier of height V_o at each interface such that.

$$V_o = \begin{cases} V_o & z < -\frac{L}{2} \\ 0 & -\frac{L}{2} \leq z \leq \frac{L}{2} \\ V_o & z > \frac{L}{2} \end{cases} \qquad \textbf{(2-1)}$$

The states are described by the time-independent Schrödinger equation: [3][4]

$$-\frac{\hbar^2}{2m*}\frac{d^2\Psi(z)}{dz^2} = E\,\Psi(z) \qquad \text{(within the QW)} \qquad \textbf{(2-2)}$$

$$-\frac{\hbar^2}{2m*}\frac{d^2\Psi(z)}{dz^2} + V_o\Psi(z) = E\,\Psi(z) \qquad \text{(within the barrier regions)} \qquad \textbf{(2-3)}$$

A finite number of states are confined in this region, which are labelled with a quantum number n: m^* is the particle effective mass, E is the energy and $\Psi(z)$ is the particle wavefunction.

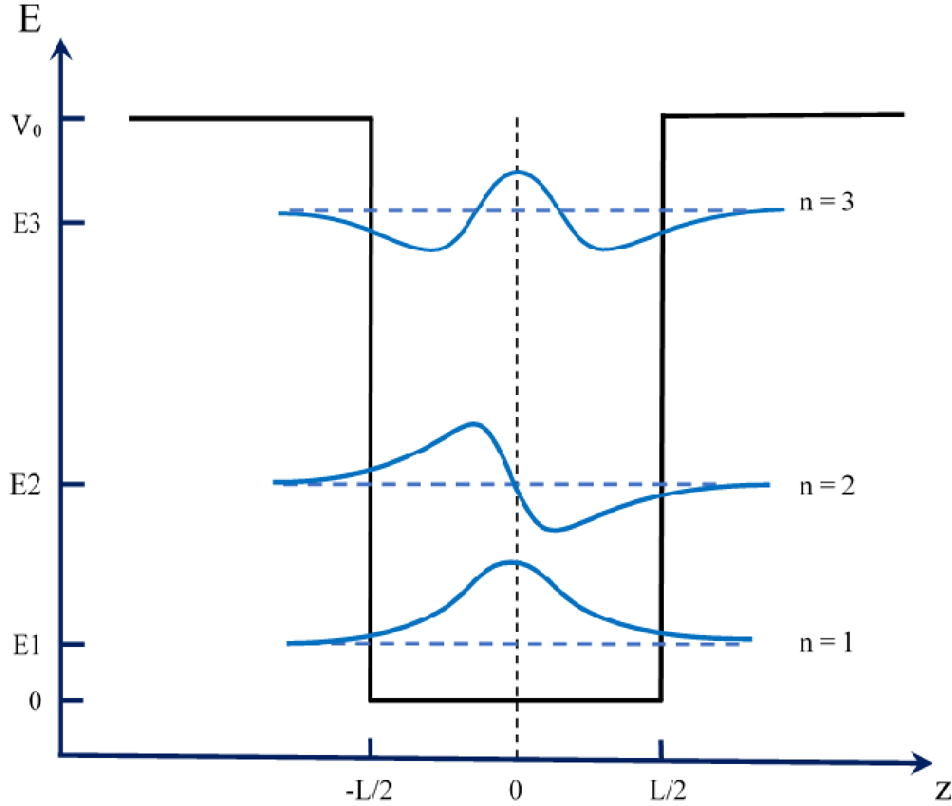


Figure 2. 1: A schematic energy-band diagram of a QW as a function of confinement direction, when E1, E2, E3 are the bound states in the finite quantum well as a function of the wave vector.

According to quantum theory, the wavefunction is non-zero at the barrier interface, which has to be considered with the solution of the following equation. Therefore, the wavefunctions within the QW can be written:

$$\Psi_w(z) = Asinknz \qquad (2\text{-}4)$$

$$\Psi_w(z) = Bcosknz \qquad (2\text{-}5)$$

for even and odd values of *n*. The wavefunction in the barrier region can be written in the form

$$\Psi_b(z) = Ce^{\mp kz} \tag{2-6}$$

where, A, B and C are constants. The states of the system can be described by two parameters: a quantum number *n* to indicate the energy level for the *z*-direction, and a wave vector *k* to specify the free motion in the *x, y* plane. The wavevector is

$$k_n = \left[\frac{2m_w^* E}{\hbar^2}\right]^{1/2} \tag{2-7}$$

Whereas, the wave vector value in the barrier region is

$$k_z = \left[\frac{2m_b^*(V_o - E)}{\hbar^2}\right]^{1/2} \tag{2-8}$$

where m_w^* and m_b^* denote the effective mass of the QW and the barrier material, respectively [5][6].

Using boundary conditions, by equating Ψ in the well and the barrier, considering $z = +L/2$ at the interface:

$$Bcos\left(\frac{k_n L}{2}\right) = Ce^{(-\frac{kL}{2})} \tag{2-9}$$

and equating the derivatives gives:

$$-kAsin\left(\frac{k_n L}{2}\right) = -kCe^{(-\frac{kL}{2})} \tag{2-10}$$

By dividing equation (2-9) equation (2-10) then gives:

$$-\frac{1}{k_n}Cot\left(\frac{k_n L}{2}\right) = -\frac{1}{k} \tag{2-11}$$

$$\therefore k_n \tan\left(\frac{k_n L}{2}\right) - k = 0 \tag{2-12}$$

Following through the same analysis as above gives the equation to be solved for the odd parity eigen energies also (but odd parity states would require the choice of wave function in the well region as a sine wave). This results in:

$$k_n \cot\left(\frac{k_n L}{2}\right) + k = 0 \tag{2-13}$$

Since both k_n and k are functions of the energy E, then equations (2-12) and (2-13) are also functions of E. These two equations can be solved numerically or graphically [6].

The wave vectors and decay constants in equations (2-12) and (2-13) normalized to obtain dimensionless values, $\upsilon = k_n L/2$ and $u = kL/2$ yielding

$$u = \upsilon \begin{cases} \tan \upsilon & (even\ parity) \\ -\cot \upsilon & (odd\ parity) \end{cases} \quad (2\text{-}14)$$

This expression can be written in terms of the variable υ by making further substitution $u_0^2 = \upsilon^2 + u^2$ such that:

$$\sqrt{u_0^2 - \upsilon^2} = \upsilon \begin{cases} \tan \upsilon & (even\ parity) \\ -\cot \upsilon & (odd\ parity) \end{cases} \quad (2\text{-}15)$$

So, u_0 value can be found by substituting in the definitions of u, υ, k_n and k:

$$u_0^2 = \upsilon^2 + u^2 = \frac{L^2}{4}\,(K_n^2 + k^2) \quad (2\text{-}16)$$

$$= \frac{2m^* L^2}{4\hbar^2}\,(E + V - E) \quad (2\text{-}17)$$

$$= \frac{m^* L^2 V}{2\hbar^2} \quad (2\text{-}18)$$

Therefore, the u_0 value contains all the structural information including effective mass, barrier height and well width for the finite well system.

Plotting barrier wave vector u as a function of well wave vector υ and the intersections (drawn as open circles) show the wave vectors of the bound states and the maximum possible wave vector in the well is denoted as υ_{max}.

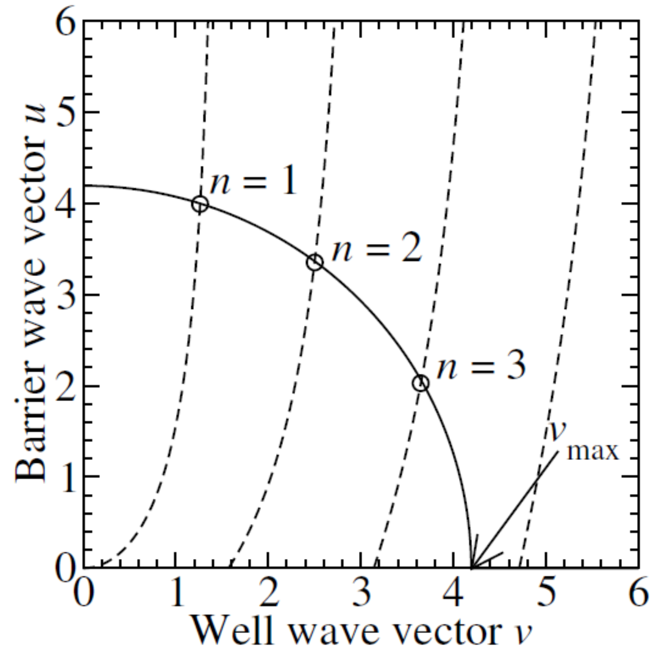


Figure 2. 2: Barrier wave vector as a function of well wave vector, when the left-hand side of equation (2-15) is plotted as a solid line and the right-hand side is plotted as a set of dashed lines.

Thus, each crossing point is a unique solution of k_n value and therefore unique value of energy as plotted in *Figure 2. 1*.

$$E_n = \frac{\hbar^2 k_n^2}{2m^*} \tag{2-19}$$

2.2.2 Density of States

The density of states is defined as the density of allowed energy states per unit volume/area/length depending on dimensionality. Electron states in structures are obtained by solving the wave equation for the potential distribution in the structure by using the bulk physical constants and by applying the so-called effective mass approximation, under which the electron energy can be written as follows:

$$E = \frac{\hbar^2 k^2}{2m^*} = \frac{\hbar^2 k_{x,y,z}^2}{2m^*} \tag{2-20}$$

and the solution of the electron wavefunction satisfies Schrödinger's equation and is of the form:

$$\psi_k(r) = U_k(r)e^{ik.r} \quad (2\text{-}21)$$

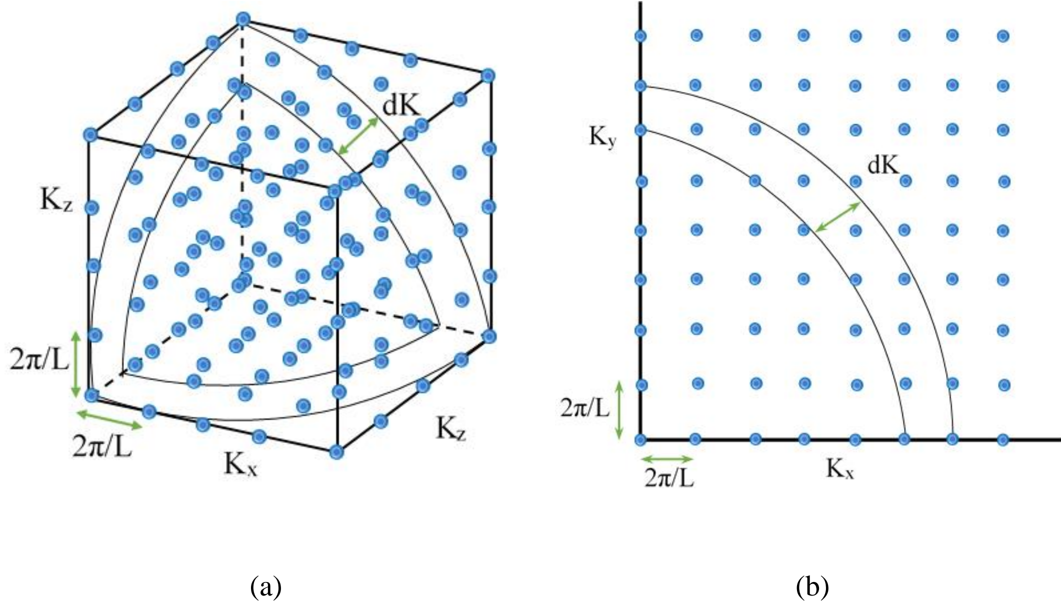
where $r = (x, y, z)$, $U_k(r)$ is a periodic function (Bloch function) and $exp(ik.r)$ is a plane wave.

Due to the periodicity of the lattice, the probability of finding an electron in one position is also periodic and, therefore, the wavevector will be:

$$k_x = \frac{2\pi n_{x,y,z}}{L} \quad (2\text{-}22)$$

where $n_{x,y,z}$ are integers. *Figure 2. 3* shows that an allowed state in the lattice exists in a k-space volume $(2\pi/L)^3$, so the total number of states up to the wavevector k is given by:

$$N_k = \frac{4}{3}\pi\left(\frac{kL}{2\pi}\right)^3 \quad (2\text{-}23)$$



(a) (b)

Figure 2. 3: Reciprocal lattice of a cubic lattice in 3D (a) and 2D (b).

Therefore, the density of states considering the spin degeneracy (spin up and spin down), such that:

$$g_{3D}(E) = 2dN_k = \frac{L^3k^2}{\pi^2}\,dk \quad (2\text{-}74)$$

By differentiating Equation 2-11, the density of states within an energy range $E+dE$, is then given by:

$$g_{3D}(E)dE = \frac{1}{2\pi^2\hbar^3}(2m^*)^{3/2}E^{1/2}\,dE \qquad (2\text{-}25)$$

The density of states of a two-dimensional (2D) system is a similar calculation in method as for three dimensions. However, the electrons are now confined in the z-direction and the volume $(2\pi/L)^2$ of the single energy state is considered in two-dimensional k-space (a circle), which results in:

$$g_{2D}(E)dE = \frac{m^*}{\pi\hbar^2}\,dE \qquad (2\text{-}26)$$

This shows that the density of states in two-dimensions does not depend on the energy. Consequently, a considerable number of states are available at the lowest energy, unlike the 3D case which builds parabolically. The total density of states has to be modified by taking into account the confinement energies in the QW and can be written as

$$g_{2D}(E)dE = \frac{m^*}{\pi\hbar^2}\sum_i \Theta(E - E_i)\,dE \qquad (2\text{-}27)$$

where $\Theta(E - E_i)$ is the Heaviside step function centred on the sub-band edge E_i, (this takes the value of zero if $E < E_i$ and one if $E \geq E_i$, where E_i is the energy of the ith level within the QW [2][7]–[11]).

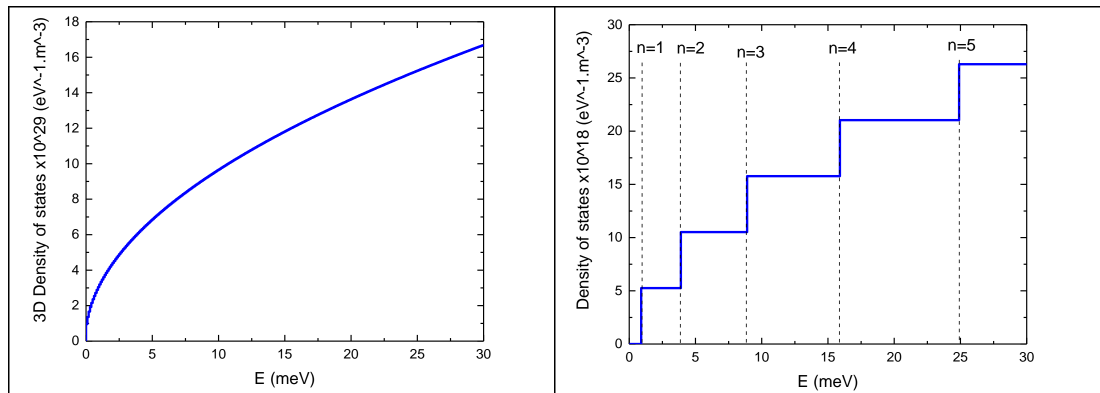


Figure 2. 4: InSb density of states (DOS) in 3D (a) using equation (2-25) and 2D QW (b) using equation (2-27) with quantised energy levels.

Figure 2. 4 compares the density of states (DOS) of InSb as a function of energy in 2D and 3D. The number of available states in 3D is dependent on $E^{1/2}$, whereas the quantization of the electron states in the 2D QW cause the DOS to become invariant with energy and increases in a step-wise way with the increasing number of sub-bands.

2.3 Electron Transport

2.3.1 Two-dimensional Electron Gas

Electron transport studies in narrow-gap semiconductors have recently attracted considerable attention because the confinement in a DEG provides a tool to create system with high-electronic mobility. It also permits electrons with a large mean free path to travel up to micrometres before scattering. Control of the mobility has important applications, such as in a magnetic sensor and ballistic transport [12][13].

One of the most significant developments in semiconductors from the point of view of physics and device development is the realisation of 2D structures, which means that electrons are trapped in a narrow potential well that restricts their motion in one dimension and modifies their available states to discrete energy levels. If the separation between these energy levels is large enough, then an electron will appear to be confined in the ground state of this potential well. The result for many electrons is a 2D electron gas (2DEG) [14]. The energy of an electron in a 2DEG according to solutions of Schrödinger's equation is

$$E = \frac{\hbar^2 k^2}{2m^*} = \frac{\hbar^2 (k_x^2 + k_y^2)}{2m^*} \tag{2-28}$$

2.3.2 Ballistic Transport

Semiconductor nanostructures are unique in offering the possibility to study quantum transport in an artificial potential landscape. Ballistic conduction is the transport of charge carriers in the active region of a 'device', which has negligible electrical resistance caused by scattering. Transport is described purely by Newton's second law in this scenario. Transport is confined to the conduction band above the Fermi energy where the energy states are not fully occupied. The transport properties can be tailored by geometric variations in the same way as tailoring the transmission properties of light in a waveguide [15]–[17].

If there is no barrier to transport, the current flows through the active region as a number of electrons (per unit time) from the source contact. If a barrier is present however a proportion of the injected electrons are reflected back into the source

contact and a fraction are transmitted across the barrier (which can take place by quantum tunnelling or by thermal activation say). Note that the charge fluctuations near the barriers may substantially affect the potential near the barriers and so modify the band structure. The transmission is then controlled by the quantization of conductance (for instance in split gates and quantum point contact devices that result from the discreteness of the number of electron wave energies [15][16][18]. The ballistic transport of an electron can be determined by the mean free path equation [19]:

$$\lambda = \frac{\hbar\sqrt{2\pi}}{e}.\sqrt{n}.\mu \tag{2-29}$$

where μ is the electron mobility. The ballistic transport for an InSb QW can be calculated as a function of temperature, from electron concentration (n) and mobility (μ) of a two-dimensional electron gas (2DEG). An example measurement of mean free path (deduced from Hall measurement) for a typical InSb 2DEG is shown in *Figure 2. 5*.

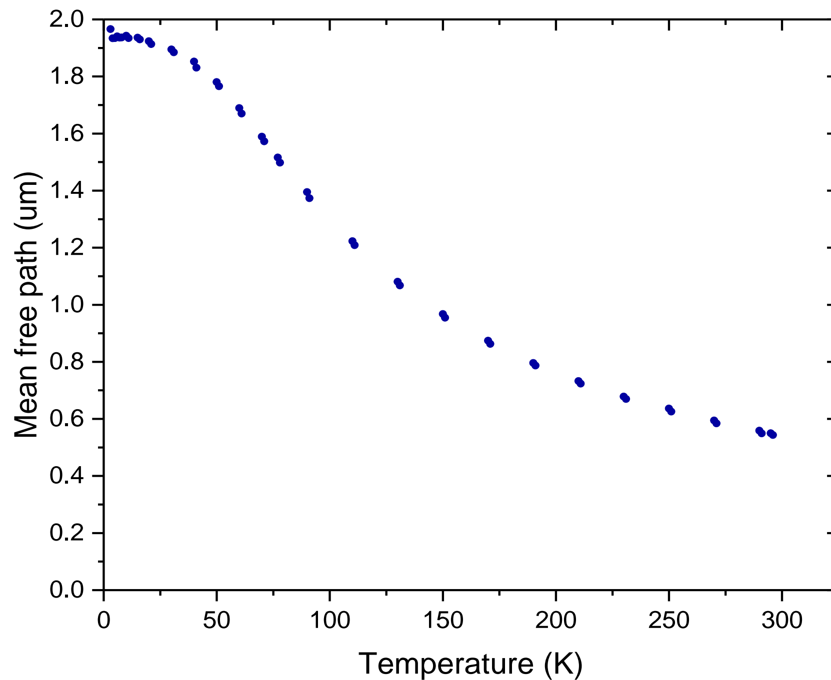


Figure 2. 5: Temperature dependence of the mean free path of InSb wafer (SF1258) as measured by the Hall effect.

2.3.3 Quantized Conductance

The one-dimensional conductance quantization phenomenon is probably one of the most important phenomena exhibited by mesoscopic conductors [18]. This phenomenon depends on the significance of the Landauer formula, which plays a central role in the study of ballistic transport because it expresses the conductance in terms of a Fermi level property of a system, such as a mesoscopic size system. Quantum tunnelling across a potential well produces a quantization of the conductance, as given by the Landauer formula [15][16]:

$$G = \left(\frac{e^2}{h}\right)T \tag{2-30}$$

where T is the electron transmission probability, e is electron charge and h is Planck's constant. This phenomenon was independently discovered by Van Wees et al. [20] and Wharam et al. [21] in the form of a sequence of steps in the conductance of a point contact using a GaAs 2DEG. These steps are nearly integer multiples of $2e^2/h$ ($\approx$ 13 $K\Omega^{-1}$). The principle of this effect relies on the fact that each 1D sub-band in the constriction contributes $2e^2/h$ to the conductance. Therefore, the conductance G is quantized and can be written in the form of [15]:

$$G = \left(\frac{2e^2}{h}\right)N \tag{2-31}$$

where N is the number of modes or channels participating in the conduction process. These elegant set of experiments and results were revealed by using very-high-mobility 2DEGs that formed at the interface between GaAs QW and the doped top cap (AlGaAs) layer. The conductance was measured between two reservoirs (*Ohmic contacts*) where electrons may travel ballistically between at low temperatures. A pair of surface metal gate electrodes are imposed on the top of the heterostructure material to create a *nanoscale constriction* between the two parts of the 2DEG by applying a negative potential on these electrodes, which repels the electrons and subsequently changes the current flow in the QW. These electrodes are electrically isolated from the 2DEG and form a short one-dimensional channel with allowed modes of propagation between the two parts of the broad-area electron gas depending on constriction size. The transmission coefficient is either 0 or 1, depending on whether the sub-band (mode channel) energy lies above or below the Fermi energy. The arrangement of sub-bands, Fermi energy and the bandgap of InSb structure are depicted in chapter 3.

Essentially, the gate bias is varied and the number of channels below the Fermi level is changed as the saddle potential between the gates is raised or lowered. Thus, in the case of a sufficiently large negative gate bias, all of the channels are pinched off and the conductance drops to zero. A simulation of the quantization conductance steps for InSb at a variety of temperatures are displayed in chapter 6. These results represent a very dramatic verification of the Landauer formula and ballistic transport in mesoscopic systems [16][18][22].

The degree of the plateaus 'flatness' and 'sharpness' varies among devices of identical design, indicating that the detailed shape of the electrostatic potential defining the constriction is significant. Whereas, there are many uncontrolled factors that affect this shape, such as changes in the gate geometry, variations in the Fermi level pinning at the QW, surface or at the interface with the gate metal, doping homogeneity in the heterostructure material and trapping of charge in deep levels in the top cap layer [15].

To model the quantization conductance electron energies in 2DEG of InSb heterostructure, the energy that corresponds to the nth level is given by:

$$E_n = \frac{\hbar^2 k_n^2}{2m^*} = \frac{\hbar^2}{2m^*}\left(\frac{n\pi}{d}\right)^2 \tag{2-32}$$

where m^* is effective mass and d is the electron path confined with QW [3]. While, the Fermi energy is giving by:

$$E_F = \frac{\hbar^2 \pi\, n_{2D}}{m^*} \tag{2-33}$$

where n_{2D} is the carrier density. Therefore, the quantized conductance of electrons in the case of many (n) channels is given by the Landauer equation [23]–[25]:

$$G = \frac{2e^2}{h} \; T \sum_{n}^{\infty}\left(\frac{1}{EXP\left[\frac{-(E_F - E_n)}{KT}\right] + 1} \right) \tag{2-34}$$

where T denotes the transmission probability of a single electron in the QW.

2.4 Metal–Semiconductor Contact

2.4.1 Ohmic Contacts

The metal–semiconductor contact system can either be rectifying such as a Schottky barrier or of broadly linear resistance which is known as an Ohmic contact. This in general depends on the material properties, preparation and characterisation of the contact which have major efforts in device fabrication. Therefore, the metal–semiconductor contact system can be defined as an *Ohmic contact* if has an insignificant junction resistance comparative to the entire resistance of the semiconductor device when the charge carriers flow in either direction without presenting any resistance at the interface. Low Ohmic contact resistance and the quality of Ohmic contacts are important and play a vital role in determining the performance limitations and reliability of many semiconductor devices [26], in particular devices like split gate structures. It is essential to understand the physical nature of Ohmic contacts and pave a way to determine some important basic quantities, such as specific contact resistance, the electron transmission length and the corresponding sheet resistance for the active material.

Essentially, a good Ohmic contact current-voltage characteristic displays a linear relationship and is symmetric with respect to the origin (if a potential barrier does not exist in between the semiconductor and the metal). Consequently, the contact resistance depends on parameters such as the contact size and geometry, the interface between the metal and the semiconductor, the regions immediately below and above the interface, and the uniformity of current within the contacted area [26]–[28].

Fabrication of Ohmic contacts relies on several theoretical and experimental concepts. The metal–semiconductor system is presented in *Figure 2. 6*, in two cases: Schottky and Ohmic cases, which depend upon the work functions for the metal and the semiconductor [28].

After the metal and semiconductor are brought into contact the charge carriers flow through the metal–semiconductor contact in either direction without any resistance (in theory). However, in practice, a potential barrier is formed at the interface. Fundamentally, the barrier arises from the difference in the metal and semiconductor

work functions. If the work function of the semiconductor is lower than that of the metal and $Em > Es$, then electrons will flow from the semiconductor to the metal until the Fermi levels in both materials reach equilibrium. The barrier height is then given by the band bending at the semiconductor surface E_{Bn}, which is reported by the Schottky–Mott equation in the theory of barrier formation:

$$E_{Bn} = E_m - \chi_{sc} \tag{2-35}$$

where χ_{sc} is the electron affinity of the semiconductor and W_m describes the barrier for electron flow from the metal to the semiconductor. For the reverse flow of electrons, from the semiconductor into the metal, the barrier will be

$$eV_{bi} = E_{Bn} - (E_C - E_F) \tag{2-36}$$

where the quantity V_{bi} denotes the diffusion potential, and E_C and E_F are the lower conduction band and the Fermi level, respectively [26].

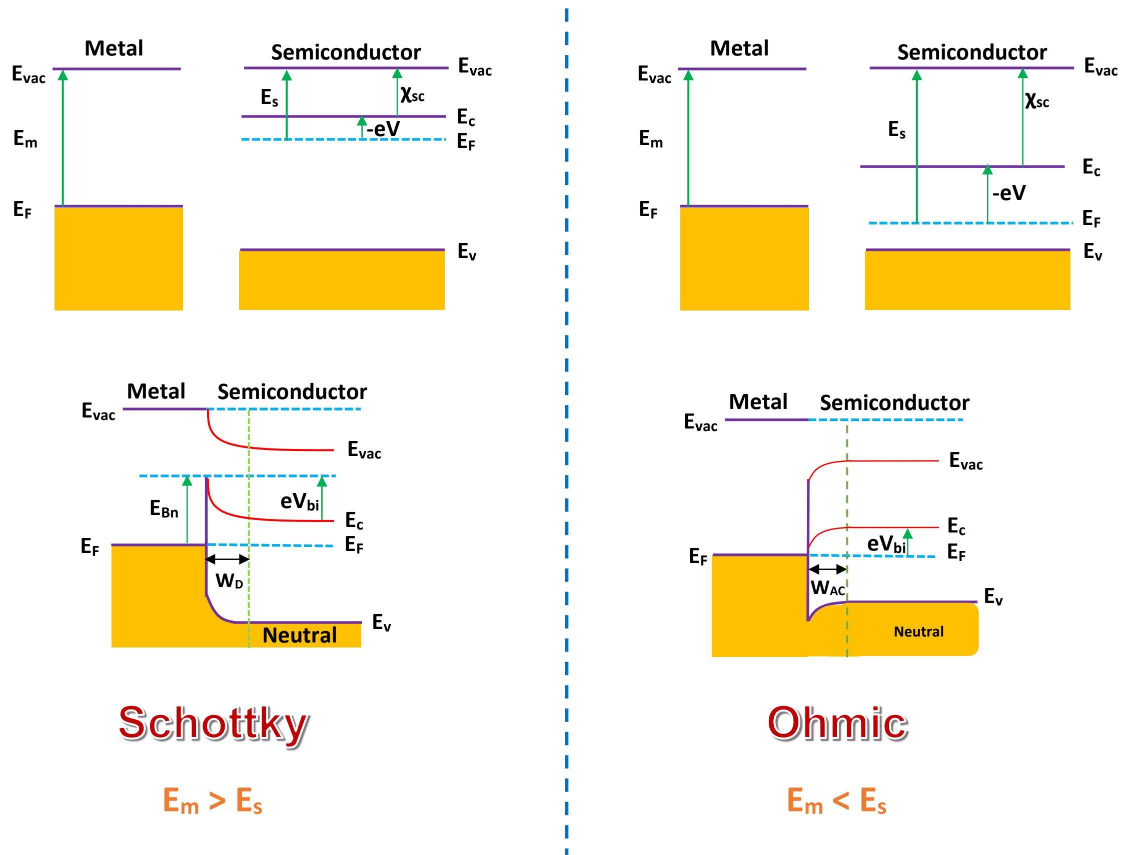


Figure 2. 6: Schematic band structure of a metal–semiconductor junction before and after contact for Schottky and Ohmic cases.

W_D and W_{AC} denote the width of the depletion and accumulation layers, respectively, E_{Bn} denotes the Schottky barrier height, and V_{bi} denotes the built-in voltage (here $V_{bi}>0$). Whereas, in the case where the work function of the semiconductor is higher in energy than that of the metal, $Em < Es$ electrons will flow from the metal to the semiconductor until the Fermi levels in both materials equilibrate. This results in band bending at the semiconductor surface. This is an Ohmic contact. However, experimentally fabricating Ohmic contacts can be more of an art than a science, and every laboratory has its own tailored recipe using particular metals or alloy systems, deposition methods, and heat treatments. All of these recipes depend on one or more of the following three principles [29]:

1. Depending on the Schottky–Mott (2-35), the contact behaves as an Ohmic with negative barrier height if the work function of the metal is less than that of the n-type semiconductor or greater than the work function of the p-type semiconductor, which allow carriers to transfer from the metal to the semiconductor.
2. A very heavy doping with a thin layer into the semiconductor immediately adjacent to the metal to obtain a very thin depletion region that allows electron transportation to take place with very low resistance contact at zero bias (transparent Schottky). *Figure 2. 7* explains the tunnelling electron transport through a thin barrier and both tunnelling electron and thermionic emission through a medium, whereas it is only thermionic in the case of a wide barrier, depending on the electron energy for both mechanisms.
3. Damaging the semiconductor surface by, for instance using ion beam milling technique, which forms crystal defects that act as efficient recombination centres. Consequently, the high density of these centres, means that the recombination in the depilation region will become the dominant conduction mechanism, causing an essential drop of contact resistance.

The current transport in a metal–semiconductor contact system has been studied by Schottky and Mott, who proposed models known as the diffusion theory and the thermionic transport theory [26]. Current transport in metal–semiconductor contact results from majority carriers, in contrast to *p-n* junctions, where the minority carriers are responsible. The mechanisms of current transport are [29][30]:

1. Emission of electrons from the semiconductor over the top of the barrier into the metal which depends on the barrier height and the thermal energy of an electron which must have a sufficiently high energy to overcome the potential barrier. The barrier width should also be significantly less than the mean free path of the electron in the semiconductor;

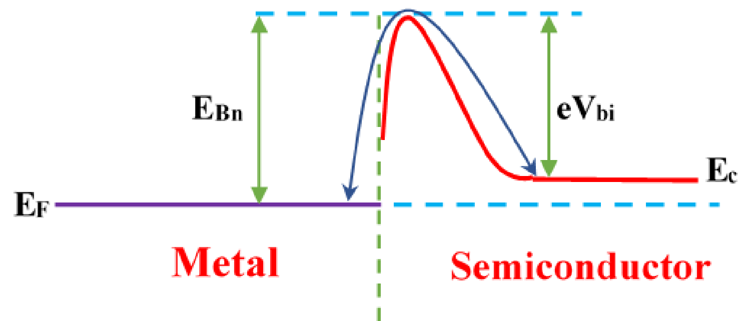
2. Quantum mechanical tunnelling of electrons from the semiconductor through the barrier into available states in the metal;

3. Recombination of electrons and holes in the depletion region; and

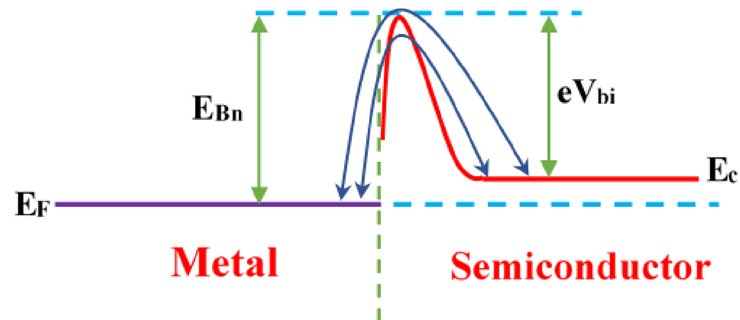
4. Recombination of electrons and holes in the neutral region ("hole injection").

These mechanisms are depicted in *Figure 2. 7*:

(a) Thermionic Emission



(b) Thermionic Emission & Tunnelling



(c) Tunnelling

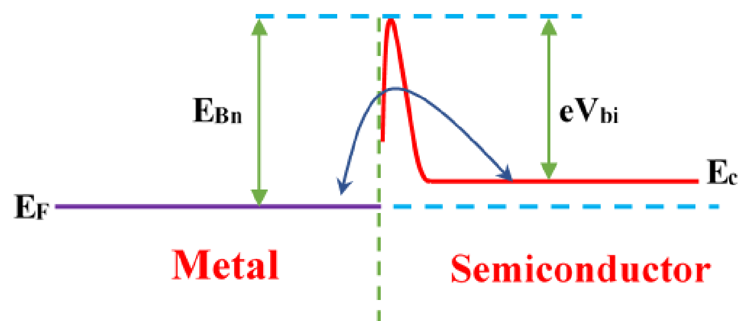


Figure 2. 7: Schematic diagram of the conduction mechanisms for different barrier widths: (a) wide barrier, (b) intermediate barrier width, and (c) thin barrier. The case of thermal activation and then subsequent tunnelling is sometimes referred to as a field emission mechanism.

2.4.2 Transmission Line Model

The Transmission Line Model (TLM) is one of the most common methods for quantitatively determining the performance of Ohmic contacts and assessing the intrinsic sheet resistance of the semiconductor material. This model has been widely used to extract the metal–semiconductor barrier resistance, in a form known as the specific contact resistance ρ_c (ohm-cm^{-2}), which is the most important property of Ohmic contacts [31]. The specific contact resistance is due to the potential barrier at the metal–semiconductor interface [32].

A TLM was originally proposed by Shockley [33] and it offered a convenient method for determining ρ_c for planar Ohmic contacts and experimentally by measuring the total resistance R_T between two contacts (of length d and width W separated by a space L). The total resistance can be plotted as a function of L and several other useful quantities can be obtained, including contact resistance R_C, transmission length of the electrons (L_T) and sheet resistance (R_{sh}) [34]–[38]. *Figure 2. 8* shows a schematic diagram of a typical TLM device, depicting the Ohmic contacts on the surface, distances (L_1, L_2, L_3), to a first approximation the contact resistances and the sheet resistances in the material.

TLM measurements can be carried out using a four-point probe technique or the Van der Pauw method. This technique uses two outer probes to pass the current (I) flow under and through the interface and two inner probes to measure the potential difference (V) determining the sheet resistance of the semiconductor.

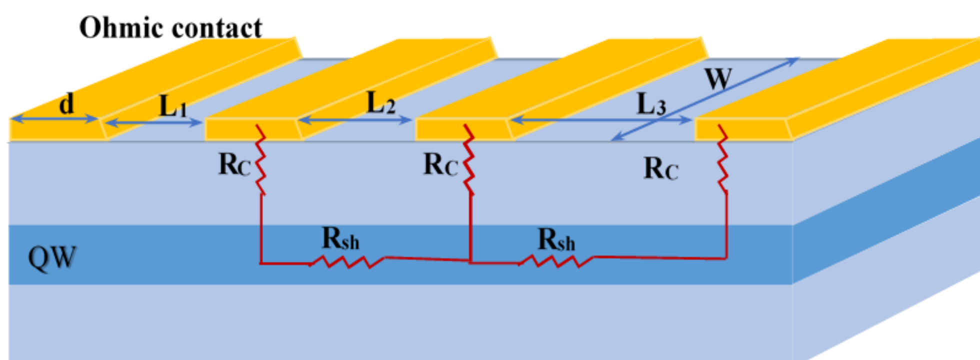


Figure 2. 8: A Schematic 3D representation of a typical transmission line model (TLM) device configuration showing the contributing contact resistance (R_C) and the effect of sheet resistance (R_s).

Therefore, this measures the resistance that is given by Ohm's law:

$$R = \frac{V}{I} \tag{2-37}$$

where R is the resistance. But this resistance is the total resistance, so R_T should be included, as in the following equation:

$$R_T = 2R_m + 2R_C + R_{semi} \tag{2-38}$$

where R_m is the resistance due to the contact metal, R_c is the metal–semiconductor interface of the single contact and R_{semi} is the usual semiconductor material resistance. However, in most situations, the resistivity of R_m is low compared to the others and, therefore, can be neglected. In addition, R_{semi} in a homogeneous material is given by:

$$R_{semi} = R_{sh}\left(\frac{L}{W}\right) \tag{2-39}$$

where R_{sh} is the semiconductor sheet resistance, L is the nominal length between contacts and W is the width of the contact, resulting in:

$$R_T = 2R_C + R_{sh}\left(\frac{L}{W}\right) \tag{2-40}$$

2.4.2.1 Linear Structure (LTLM)

The simplest and most used configuration of TLM is a linear array of Ohmic contacts, all of which are the same size but placed on the semiconductor surface at a variety of distances ($L1 < L2 < L3 < \ldots < Ln$). This configuration is often referred to as the linear transmission line method (LTLM) due to the linear arrangement of the Ohmic contacts. *Figure 2. 8* gives a schematic depiction of the LTLM configuration, which is in general isolated by mesa etching to restrict the current to flow only across the distances *Ln* and to prevent current spreading.

The LTLM configuration can be described by the following equations, when the total resistances R_{T1} and R_{T2} correspond to the contact separations L_1 and L_2, respectively:

$$R_{T1} = 2R_C + R_{sh}\left(\frac{L_1}{W}\right) \tag{2-41}$$

$$R_{T2} = 2R_C + R_{sh}\left(\frac{L_2}{W}\right) \qquad (2\text{-}42)$$

The contact resistance R_c can be calculated by measuring the total resistances R_{T1} and R_{T2}, and can be obtained by:

$$R_C = \frac{(R_{T2}L_1 - R_{T1}L_2)}{2(L_1 - L_2)} \qquad (2\text{-}43)$$

By plotting the total resistance as a function of the distance between several pairs of the planar contacts, R_c is determined by a linear extrapolation of the experimental points to L=0, which is shown in *Figure 2. 9*. Note that the probe metal's resistance is assumed to be negligible in this case of a four-point probe measurement technique. Whereas, the R_{sh} value can be calculated by the following formula:

$$\frac{\Delta R_T}{\Delta L} = \frac{R_{sh}}{w} \qquad (2\text{-}44)$$

The transmission length can be extrapolated on the x-axis when R_T is at zero from the R_T-L trend.

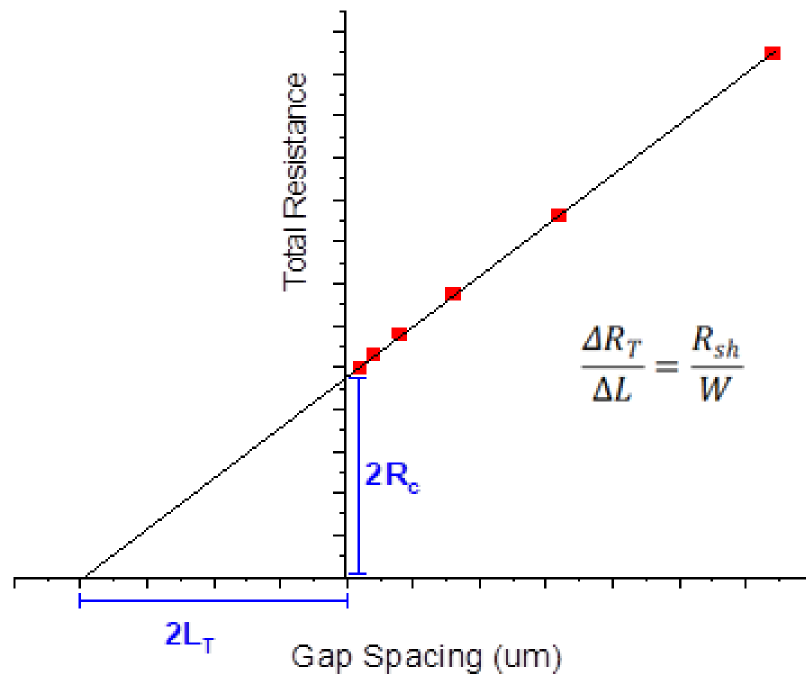


Figure 2. 9: A sketch of a typical plot of total resistance as a function of gap spacing between the planar Ohmic contacts in a TLM measurement.

2.5 Scattering

Electron transport in a heterostructure semiconductor in the QW scatters by interaction with the following excitations: polar phonons, acoustic phonons, background impurities, remote ionised impurities in the doping layer and QW interface roughness. The average of these mechanisms decreases the electron mobility by scattering events. The total electron mobility and the average mobility can be found by using Matthinessen's rule, which can be written as [12][13];

$$\mu = \frac{e < \tau >}{m *} \tag{2-45}$$

$$\frac{1}{\mu} = \frac{1}{\mu_{ac}} + \frac{1}{\mu_{po}} + \frac{1}{\mu_{bg}} + \frac{1}{\mu_{rii}} + \frac{1}{\mu_{int}} \tag{2-46}$$

where μ is the total mobility, e is the electron charge, $m*$ is electron effective mass, μ is average mobility, μ_{ac} is the acoustic mobility, μ_{po} is the polar phonon mobility, μ_{bg} is the background mobility, μ_{rii} is the remote ionised impurities mobility and μ_{int} is the interface roughness mobility.

Electrons can be scattered in an *inelastic* or *elastic* process, depending upon the collision transfer kinetic energy between the particles. For inelastic processes, there are acoustic and optical phonon scattering. The former plays a more effective role than the latter as temperature decreases. Therefore, at low temperatures, the optical phonon population in the crystal starts to vanish. Only at temperatures above 50 K do the effects of phonon scattering start to play a role. At temperatures approaching 300 K, the mobility is dominated by polar optical phonon scattering [39]. *Figure 2. 10* shows these types of scattering contributions and electron mobility in InSb QW as a function of temperature.

Whereas, for elastic processes, electrons can be scattered by ionised impurities or scattering from interface roughness. Both of these scattering events can even be effective and dominant at low temperatures, which is found to be independent of temperature in this regime. In addition, crystal dislocations can contain charge centres and thus act as scattering centres [17]. Nevertheless, even with a large spacer between dopant and QW in modulation-doped QWs, a heavy doping will raise the scattering rate [14][40]. The primary reason for the decrease of mobility with increasing doping level is the increasing role of remote ionised impurity scattering. At high-doping

levels, this can become more important at room temperature than phonon scattering [17][41].

The background density of neutral impurities is usually very small when compared with ionised impurities with a thin spacer layer thickness. However, when the thickness of the spacer layer is relatively large, the effect of remote ionised impurities is reduced and the background neutral impurity scattering becomes more important [42]. The net mobility in the AlInSb/InSb system increases with decreasing temperature due to impurities scattering.

Where surface roughness is one of the major scattering mechanisms, the low temperature mobility of 2D electrons in these layers is limited by the surface roughness scattering [43]. The effect of interface roughness on electron transport in semiconducting materials depends on the quality of the interfaces, which limits the electron mobility [44]. Interface roughness scattering has a very strong effect on electron mobility with the quantum width and becomes significant when $L < 25$nm in InSb QW [14][40][42]. Thus, the interface roughness scattering (IFRS) rate in narrow QW is high. Whereas, in wide QW width, the large mobility values indicate that scattering only comes from background impurities, which is small compared to the effect of (IFRS) in narrower wells. There are also some limitations for relative very wide thicknesses. For instance, nucleation of misfit dislocations in the QW layer due to the partial strain relaxation coming from lattice mismatch between QW and bottom layer. Moreover, the onset of intersub-band scattering is likely to come into play as the wells become wider. Therefore, there is a strong dependence on the well width and the optimum thickness of the QW, which should be checked for a particular material [45][46]. Therefore, roughness at the QW edge interfaces causes the energy of the confined states to change as the width of the confinement changes [39]. Furthermore, due to the narrow bandgap of InSb, the nonparabolicity effect with scattering can be strong.

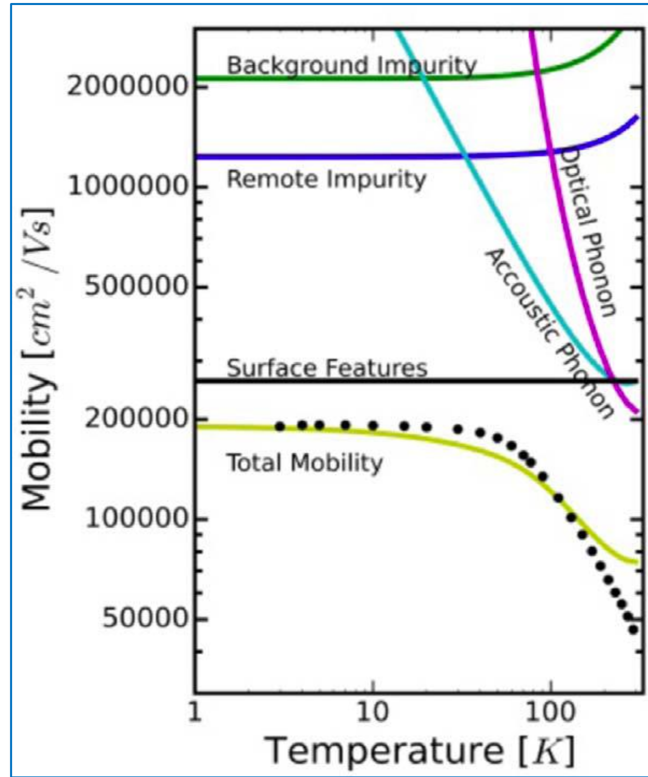


Figure 2. 10: A typical transport model of mobility (lines) using the relaxation time approximation, and measured data (symbols) versus temperature from [47].

Furthermore, structural defects, micro-twins and threading dislocations contribute to carrier scattering and decrease the mobility in the QWs, which is related to the defects density that arises from lattice mismatch with the substrate and growth process [47]–[50]. *Figure 2. 10* explains the electron mobility versus temperature for InSb and the scattering types.

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Chapter 3

AlInSb/InSb Heterostructure Wafers: Devices, Design and Fabrication

Fundamental studies of electronic transport, such as in heterostructure semiconductor devices, require high-quality fabrication and a clean environment for both material growth and device fabrication. A successful device requires fabrication in a clean room environment of class 1000 and 100 (or better), depending upon the stage of the process. However, the procedure steps that are required to fabricate a sample can affect the quality and definition of the device, such as the alignment of process steps and the quality of for example wet etching. In particular, the cleaning procedure is shown to be a very significant step during sample fabrication, which must clean and remove any resist remains from previous steps.

This chapter introduces the device structures and experimental techniques used in this work. It begins with a description of how the wafers were grown and it explains the materials that were used, along with the samples that were fabricated and prepared for measurement. This chapter also presents the experimental techniques and equipment that was used to characterize the material and collect data, including an outline of molecular beam epitaxy (MBE), X-ray photoelectron spectroscopy (XPS) energy dispersive X-ray spectroscopy (EDX), atomic force microscopy (AFM) and so on. The sample fabrication steps are illustrated in detail in this chapter, from lithography (photo and electron beam lithography (EBL)), to sample cleaving. Finally, this chapter introduces the sample characterisation, including scanning electron microscopy (SEM), electrical probe station, packaging and wire bonding, the low-tempoerature cryostat system and electric field measurement equipment.

3.1 Indium Antimonide Semiconductor Heterostructure

3.1.1 Crystal Structure

Nearly all III–V compound semiconductors, including InSb, crystallize with the zinc blende structure, which is a diamond-like structure that consists of two interpenetrating face-centred cubic (FCC) Bravais lattices with a lattice parameter of 6.47 Å at a temperature of 300K [1][2]. Each indium atom is tetrahedrally bonded in the solid to four antimony atoms, and vice versa. Figure 3.1 shows the structure of InSb. Indium and antimony are located on the (0,0,0) and (1/4,1/4,1/4) sites of the FCC structure, respectively. Therefore, the cation and anion sublattices are shifted with respect to each other by a quarter of the body diagonal of the FCC lattice [3][4].

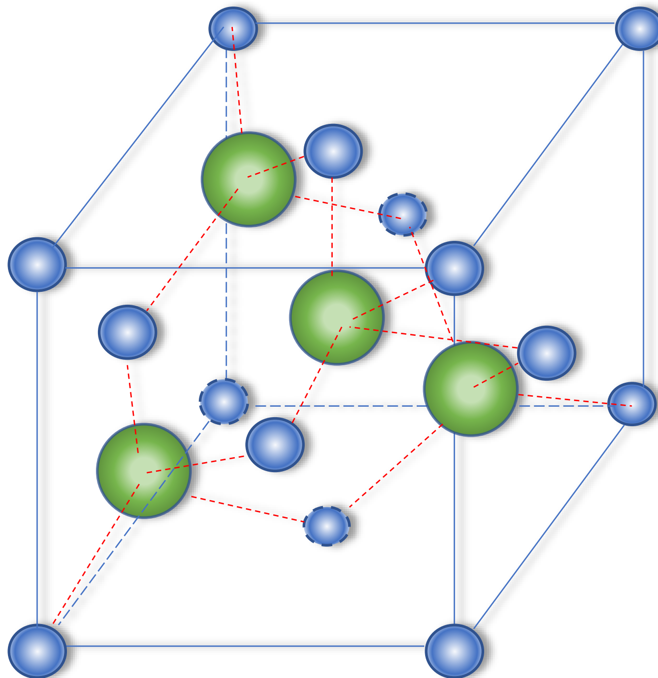


Figure 3.1: Zincblende structure (blue and green spheres denote the antimony and indium, respectively).

Impurities or vacancies can be included in the crystal, which can affect the crystal's band structure and states energies depending on the density.

3.1.2 Band Structure of an InSb QW 2DEG

The semiconductor heterostructures grown by MBE, which are structurally pure, although of varying composition and consequently of varying bandgaps. Structural purity is achieved by selecting different III–V semiconductors that have nearly the same lattice constant, which avoids or minimises defects due to any lattice mismatch with the accommodating growth surface. This is typically difficult for AlInSb basic materials because there is no common lattice matched III–V binary substrate material. The energy gap of the semiconductor band structure is defined as the energy between the valence and conduction band states, while the relative positions of the conduction band edges of the two-materials constitutes the band offset of any heterojunction. This depends not only on the properties of the bulk materials but also on the microscopic properties of the interface. In addition to any band offset, there may also be band bending as a result of free charge (e.g. from doping). At equilibrium, the Fermi levels of any two substances must ‘line up’. The Fermi level concept refers to the energy difference between the highest and lowest occupied states in a quantum system at absolute zero, where no electrons will have enough energy to rise above this level. In heterostructures, electron states are only altered from the bulk states by any confining potential profile, which results from the variation in the bandgap. Free charge redistribution takes place at interfaces by the net movement of charge from high to low energy states as a result of diffusion, which continues until the electrostatic field prevents further transfer and the Fermi level is at a constant value throughout the system. In the samples studied here, band bending depends on the modulation doping and width of the quantum well [5]. Therefore, the curvatures of the band bending are determined by the density of the fixed charges in the grown layers [5]–[7]. The conduction band potential profile of the typical InSb heterostructure that is studied in this thesis is shown in Figure 3.2. Good quality crystalline heterostructures can be grown with non-lattice matched compounds but only for very limited thicknesses. Although this is only possible for limited dimensions, it normally produces strain due to the lattice mismatch. The bandgap of III–V semiconductors is a function of the lattice parameter and so strain also naturally introduces a perturbation to the electronic states, and ultimately to the band structure. A plot of the relationship between bandgap and lattice constant is shown in Figure 3.2. The empirical lines reflect the heterostructures’ bandgap, depending on the combination of different III–V

semiconductors. For instance, InSb QWs grown on a GaAs substrate have a mismatch of about 0.8 Å, as shown in Figure 3.3. A mismatch in the lattice can affect the semiconductor through the heterostructure interface quality. The mismatched system for these grown semiconductors with strain energy is stored either in the epilayers or relaxed through a network of dislocations. These defects will modify the bandgaps and the characteristics of the electronic structure due to charge states, which lead to new physical effects that result from the band line-ups [8].

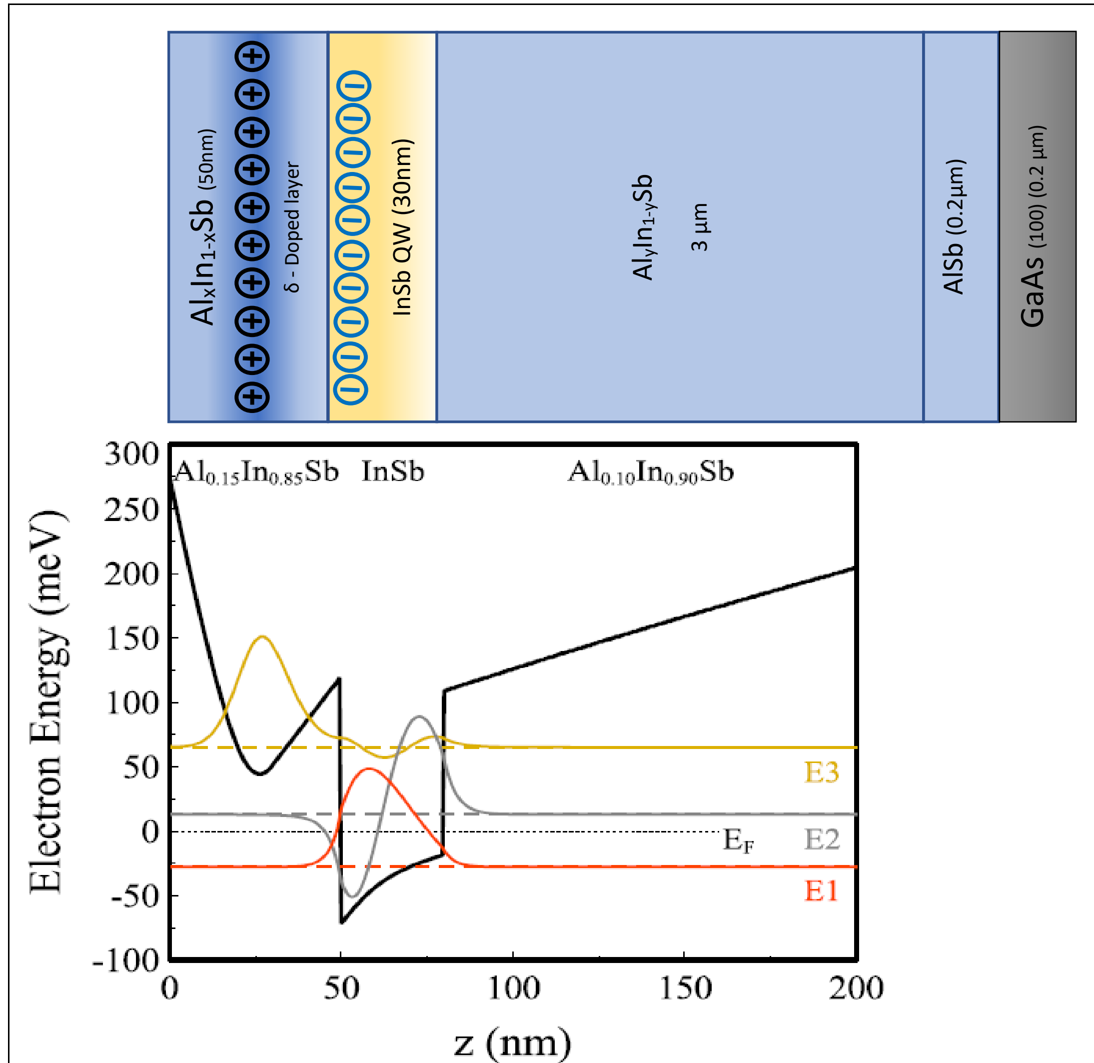


Figure 3.2: Typical description of an InSb QW heterostructure layers sequence and the conduction band profile with number of states, where the number of states and their positions are calculated using 1D Schrodinger-Poisson equations. The model has been coded by Christopher Mcindo using python.

InSb has an interesting and narrow bandgap value compared to other semiconductors of 0.17 eV and 0.235 eV at 300K and 1K, respectively. In fact, InSb has the smallest

bandgap among the III–V binary semiconductors, which is also a direct bandgap [2] [3]. This has made it a useful material for high-speed electronics and infrared imaging applications [9]–[11]. The temperature dependence of the bandgap in general comes from the change in interatomic spacing of the lattice with temperature, giving rise to a modified Bloch function associated with the lattice periodicity. The temperature dependence of the bandgap is governed by the electron energy in the atom related to the proton relation force and distance which lead to the thermal expansion of the lattice plays a minor role.

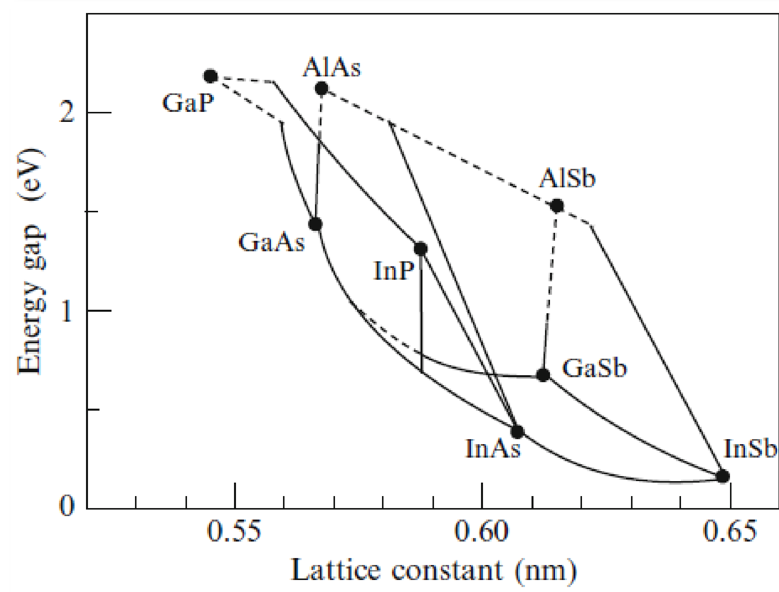


Figure 3.3: Lattice constants and bandgaps of some cubic semiconductors at 300K. Full lines indicate direct-gap materials; dashed lines indicate indirect-gap materials [6].

Among the empirical models, the widely quoted Varshni relation is given by [2][3]:

$$Eg(T) = Eg(0) - \frac{\alpha_E T^2}{T + \beta_E} \qquad \textbf{(3-1)}$$

where $E_g(0)$ is the extrapolated bandgap energy at absolute zero on a Kelvin scale for the material, and α_E and β_E are material specific constants (the volume coefficient of thermal expansion and the volume compressibility, respectively).

3.1.3 Molecular Beam Epitaxy

The InSb based heterostructures in this thesis were all grown by solid source molecular beam epitaxy (MBE) at the National Epitaxy Facility (Sheffield), or legacy samples grown similarly by solid source MBE at QinetiQ (Malvern) pre-2010. MBE is a versatile technique for epitaxial growth via the interaction of one or several molecular or atomic thermal beams. This technology is used for the deposition of thin film compound semiconductors, metals or insulators. MBE allows a precise control of compositional profiles by using a process far from the thermodynamic equilibrium with single thickness, which is as low as ~ 10 Å [8][12].

Advances in solid state device technology have established the III–V groups as a new class of semiconductors for highly efficient optical and high-speed microwave devices. These compound semiconductors usually consist of the group III elements, such as gallium (Ga) or indium (In), and the group V elements, such as arsenic (As) or antimony (Sb). These devices require precise layer thickness control in the growth process [12]. Theoretically, although MBE is a very simple crystal growth technique, it requires highly controlled evaporation in an ultra-high-vacuum (UHV) apparatus to grow semiconductor layers for electronic devices. Consequently, MBE uses only high-purity elemental sources to get the highest purity, growth process in a (10^{-11} Torr) chamber. In addition, the crystal structure, substrate surface quality, composition and growth process need to be monitored and controlled using analytical equipment, such as reflection high-energy electron diffraction (RHEED). Moreover, MBE needs extreme control of growth rate and composition or doping level to avoid any structural changes [13].

The MBE technique fabricates compound semiconductors by growing layers on the substrate surface in a desired stoichiometric composition that uses solid source effusion cells as a source of compositional atoms. These elementally pure material sources are heated for evaporation and controlled by temperature and by a mechanical shuttering system, which physically impedes the beam of atoms. This technique grows at very low rates and high-temperatures 550 ^{o}C, with a thickness control on the order of 5 Å, an interface width of <5Å and a dopant range of 10^{14}–10^{19} cm^{-3}[14][15]. The materials investigated in this thesis were grown either at QinetiQ (name Dalehead and Blencathra) or collaborators at the National Centre for III–V technologies at Sheffield

University (now the National Epitaxy Facility). The latter samples are denoted with numbers as opposed to names for the QinetiQ samples.

3.2 Device Design

3.2.1 Split Gate Devices

The split gate device consists of Ohmic metals, gates, and FEED pads with arms and MESA isolation designs. The gate structure and their taps need to be designed and tailored using EBL. The mask designs in general consist of 12 repeat fields that can be exposed on the wafer's surface. Each field consists of 30 devices, designed as five rows and six columns. There is then flexibility within these fields so they can be designed differently with a split gate design using EBL. Mesa isolation ranges from straight mesa's through to bulge, and even air bridge supporting islands (depicted later). The device consists of two pads of Ohmic metals, which are deposited in the first step of fabrication using optical lithography. Starting with a rectangular shape of $3\times24\mu m^2$, with a 2µm gap in between the pads. Then the Ohmic design was updated to 9, 12 and 14 µm width, and 2, 4, 6, 8 µm gap. The octagon shape was designed by EBL. The reason for the new design was to decrease the Ohmic resistance and avoid PMGI SF6 use. Figure 3.4 shows the Ohmic contacts in rectangular (a) and octagon (b) shapes, and their dimensions and gap distances are given.

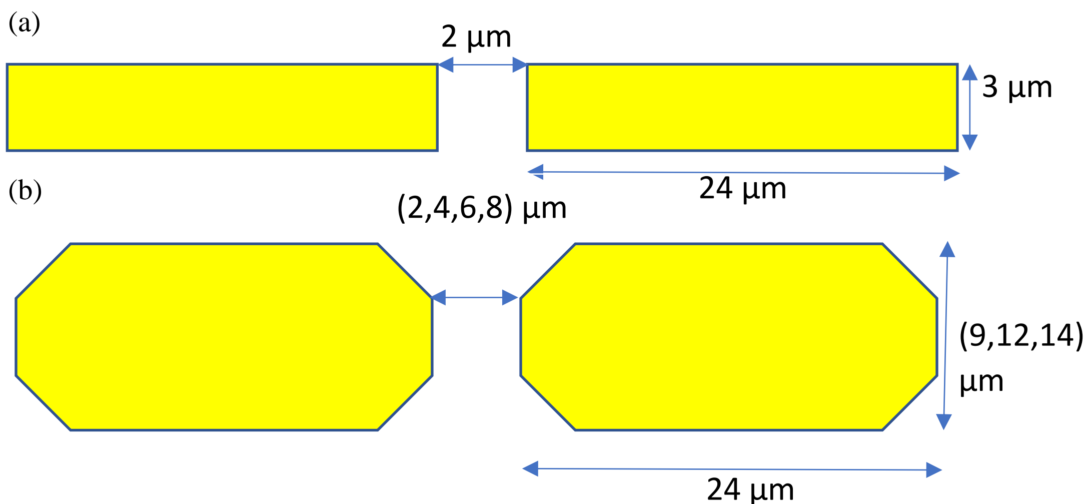


Figure 3.4: Ohmic contacts shape and dimensions: (a) rectangle shape produced by optical lithography, (b) octagon shape produced by E-line software.

The second step of fabrication was writing the gate structure by the EBL system using PMMA as a resist, followed by deposition a metals or oxide/metals. The first gates were written as three pairs of lines, of approximately 40–50 nm width. The width in general here depends on the beam dose and spot size quality. Between these lines, the gate separations (distance between lines) ranged from 150, 225, and 300 nm. These lines are connected to a bigger structure as taps and then arms, which are connected to FEED patterns. Later, two main gates were designed using EBL software. These gates are designed as a layer each and are then added to the main structure chip level file. The two main gate designs used are loop and solid structures (the former being a novel geometry to attempt to minimise current leakage), over a range of width/length ratios for gate designs. The gate length range is 100–600 nm, while the widths are 100nm and 200nm. Loops are designed as connected corner lines and non-connected corners with same length of lines in terms of overdose in critical places in gates area avoiding touching each other or making curved corners rather than normal square corners. The end of the written lines in the latter case is 30nm from the corner to achieve a square corner (due to proximity effects). Therefore, the real distance is 42.4nm, but is expected to be connected at the corner. According to the EBL images, the design has been enhanced to be only 10nm away from the corner for only one line. Since the length/width ratio of gate is influencing the quantization plateau shape, these variety dimensions have been used in order to find the best ratio. Whilst, the line and loop gate structures decrease the leakage current that applied on the gate in *Figure 3.5*: (a), (b) and (c). Where, solid gates have been used as successfully studied in literature studies considering the leakage current. Figure 3.5 presents the design of the gates and their dimensions, where: (a) shows a three pairs of line gate structure; (b) shows a loop gate structure (connected and non-connected corners); (c) shows another kind of loop and solid gate structures; (d) (e) and (f) are solid gate structures with different dimensions. Triangle structure helping the current to be directed by source-drain with (f) design; The three pairs of taps are connecting the gate structures and the FEED structure enabling for electric connection in (g) which shows the gate and its arms structures; and (h) is shows the gate length and width [16].

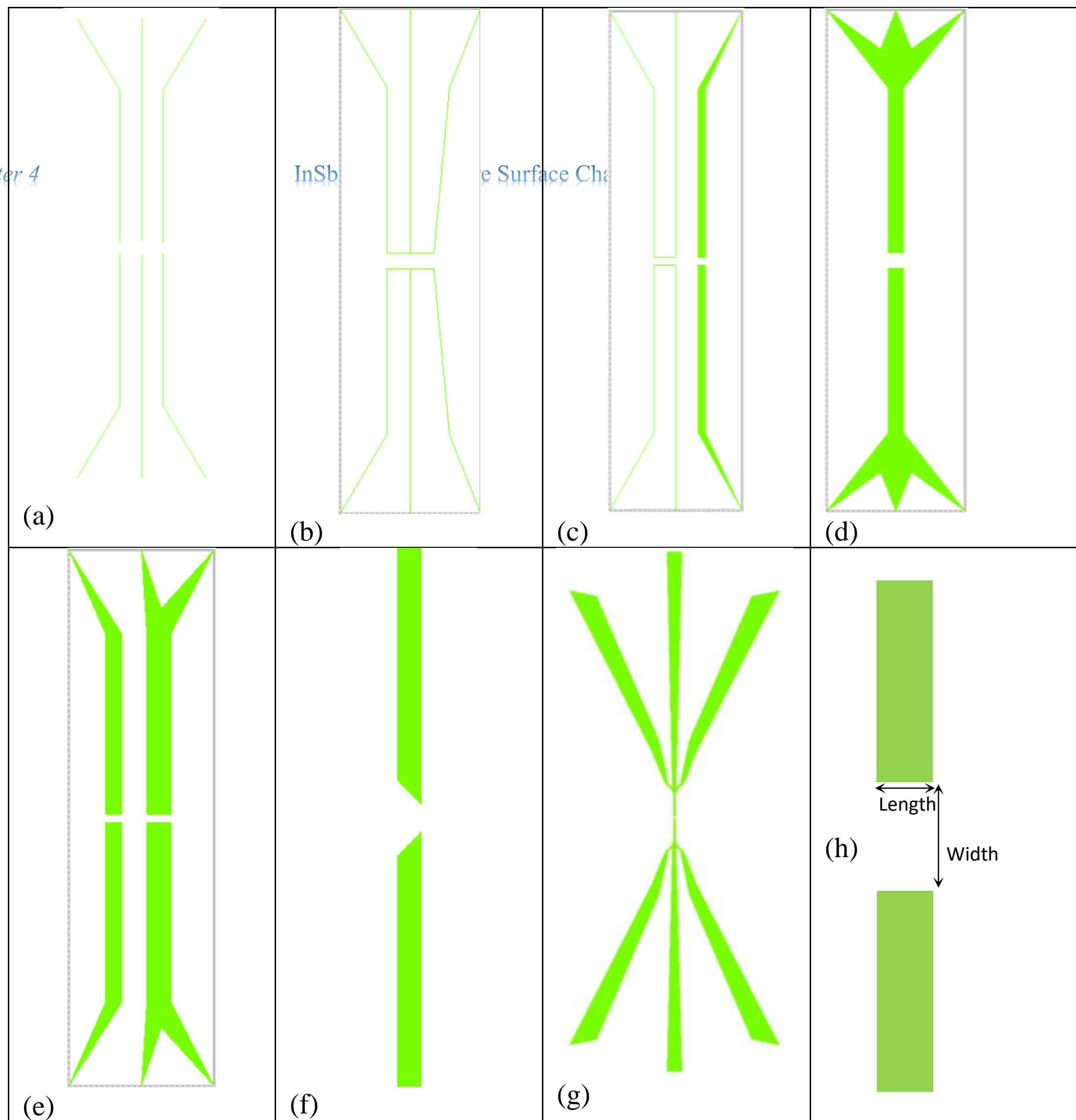


Figure 3.5: GDS file inputs for the active split gate structures designed using the E-beam software tool and the close proximity feed metal pattern (designed to contact to the larger photolithography feed metal and bond pad: (a) shows three pairs of thin (e-beam single pixel) line gate structures commonly used in chapter 6, (b) shows a pair of loop gate structures using e-beam single pixel line exposure but designed to minimise gate contact area , (c) shows one loop gate and one solid gate (exposed using both single pixel and solid raster write exposure, (d) shows a single solid gate, (e) shows a design with two pairs of solid gates, (f) shows wedge/triangle gate for electron focusing, (g) shows a more widely spaced gate feed metal pattern whilst (h) labels the dimensions of the gate.

Table 3.1 **shows the length and width of the loop split gates, their ratio and type of corner and its gap, corresponding to** *Figure 5. 3* **(b, c).**Table 3.2 **records the length and width of the line and solid split gates, and their ratio complementary to** *Figure 5. 3* **(a) for the line split gates and** *Figure 5. 3* **(c, d, e) for the solid split gates.**

Table 3.**3** records the triangle solid gate dimensions complementary to *Figure 5.* ***3*** (f).

Table 3.1: Loop split gates dimensions.

Length (nm)	Width (nm)	Corner type	Gap (nm)	Ratio
100	100	connected	-	1:1
200	100	connected	-	2:1
300	100	connected	-	3:1
200	200	connected	-	1:1
200	200	Non-connected	10	1:1
400	200	connected	-	2:1
400	200	Non-connected	10	2:1
600	200	connected	-	3:1
600	200	Non-connected	10	3:1

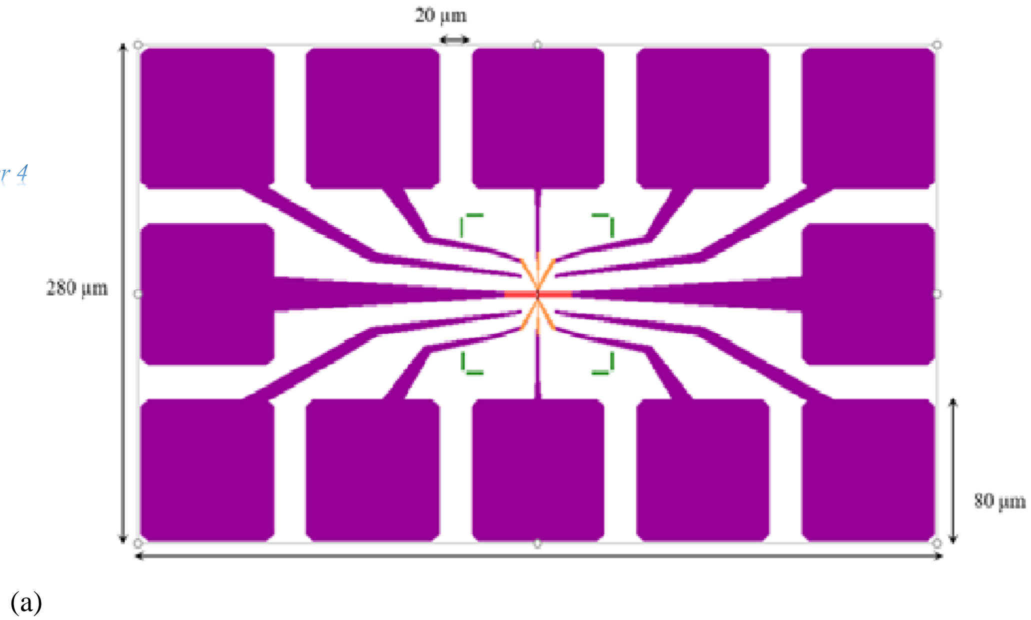
Table 3.2: Line and solid split gate dimensions.

Gate Type	Length (nm)	Width (nm)	Ratio
Line	40	150	1 : 3.75
	40	225	1 : 5.625
	40	300	1 : 7.5
Solid	100	100	1 : 1
	150	150	1 : 1
	300	150	2 : 1
	200	200	1 : 1
	400	200	2 : 1
	600	200	3 : 1
	200	100	2 : 1
	300	100	3 : 1
	300	200	1.5 : 1

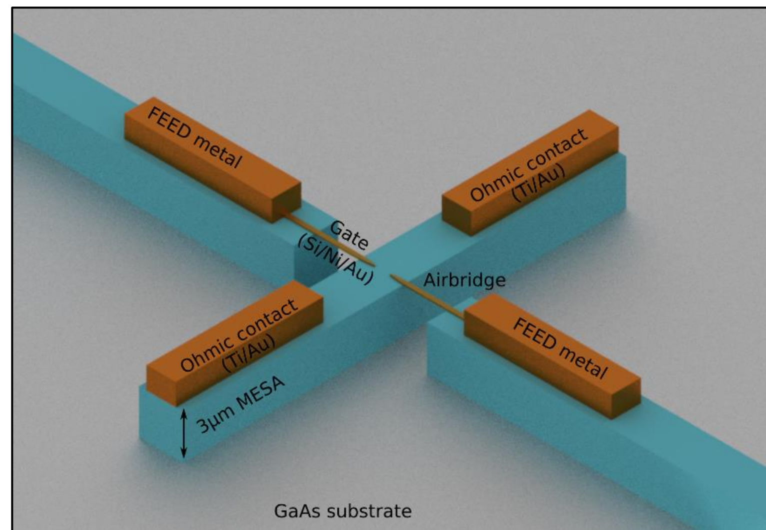
Table 3.3: Triangle solid gate dimensions.

Length	Width	Hypotenuse	Angle
300	300	460	40°

The FEED pattern is made using optical lithography and bilayer photoresists. Then, 50/300 nm of Ni/Au metals are deposited. These FEED pads are connected to the Ohmic contact pads and split gates structures by arms and then wire bonded with fine wire gold (17µm) to the ceramic package contacts for electric measurements. *Figure 3.6* shows the full device design, including Ohmic contact (pink colour), gate arms (orange), E-beam alignment marks (green) and FEED structure (purple) and its dimensions.



(a)



(b)

Figure 3.6: (a) The full design of the split gate device from the EBL GDSII software editor showing the active region and the feed metal leading to larger bond pads. These are sufficiently large to enable fine wire bonding using 17µm gold wire , (b) A 3D schematic representation of the active region of the device showing the Ohmic contacts and the gate structure with the free suspended air-bridge. Typically, the mesa depth is 3µm to allow for device isolation.

Figure 3. 7 presents the circuit used for the quantised conductance measurement. In this measurement both gates and Ohmics are connected to SMU channels, and both circuits are connected to one common earth.

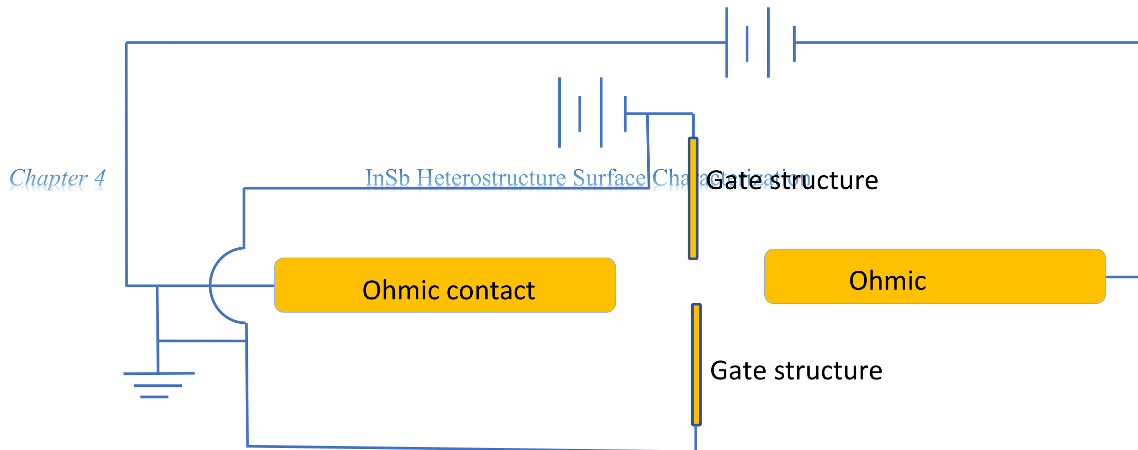


Figure 3. 7: Circuit of split gate device measurement. The source-drain for two Ohmic contacts and one channel for both gates is shown, with a common earth contact.

3.2.2 TLM Device Design

The Transmission Length Method or Transmission Line Measurement (TLM) structure designs include rectangular Ohmic pads with four rows for the devices in each field which mimic those which are suitable for quantum devices (in size and geometry). The length is 24 µm, with the range of widths for each row listed in Table 3.4. Each Ohmic pad is connected to two FEED connections as in Figure 3.8. The FEED pad dimensions are 80×120 μm^2. The Ohmic contacts are separated by 2, 4, 8, 16, 32, and 64 µm from left to right, as depicted in *Figure 3.8* and *Figure 3.9***.**

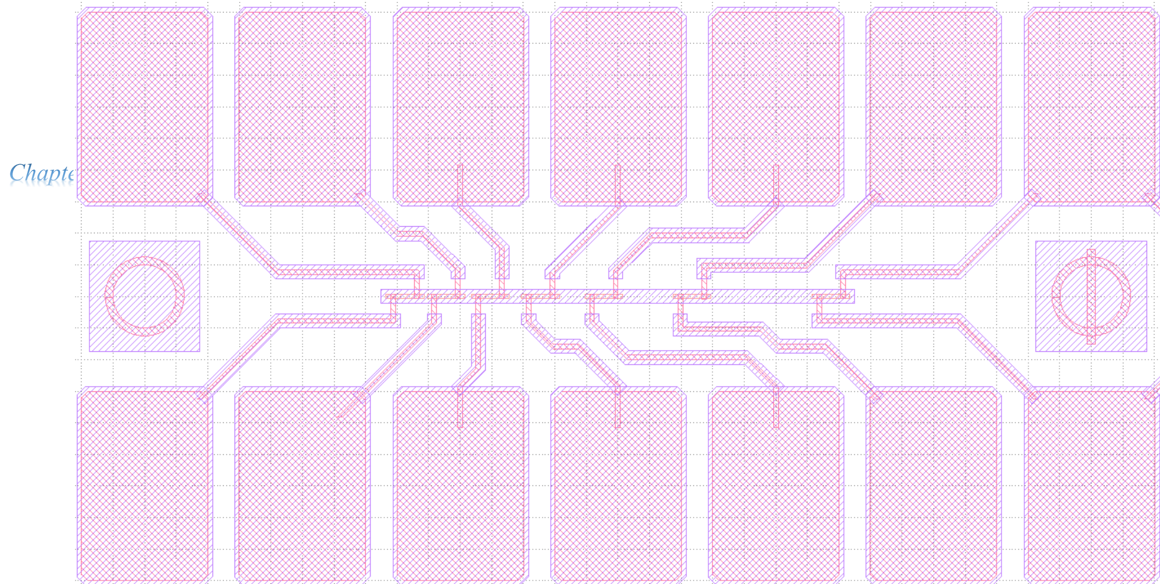


Figure 3.8: Whole TLM device design containing Ohmic pads in the middle connected to feed metal and bond pads. This also shows the active MESA area in the centre.

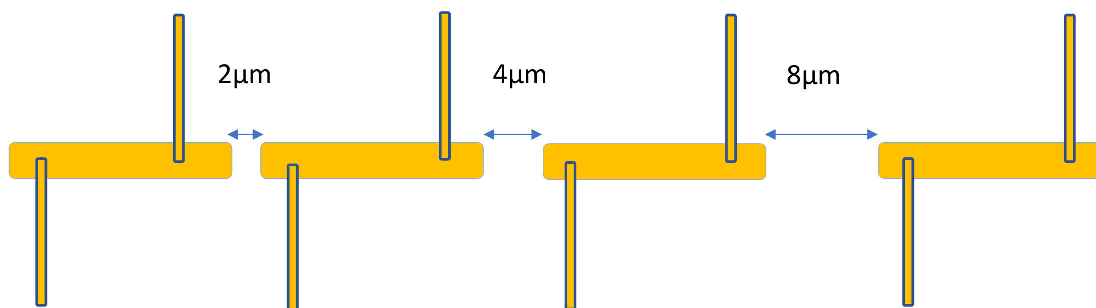


Figure 3.9: Schematic diagram of the TLM Ohmic pads design connected to two FEED pads each and their gaps. This feed arrangement enables four-point measurement for each contact 'gap' if required.

Table 3.4: The variety of width and length for the Ohmic contact pad TLM design.

Arrow number in field	Width (µm)	Length (µm)
1	3	24
2	9	24
3	27	24
4	81	24

3.3 Device Fabrication

Devices were fabricated in the Class 1000 clean room at Cardiff University, using photo lithography and nanoscale EBL and recipes tailored to this material. The process to make electrodes on the sample consists of six steps to get Ohmic contacts and split gates, with an air-bridge for electric measurements to avoid surface leakage. Surface cleaning is a very substantial step before spinning photoresist. A combination of PMGI-SF6/S1805 photoresists are spun as a bilayer on the sample surface to get an overall thickness of approximately 650nm. Then, the photolithography technique was used to expose for 5 seconds. A Suss Microtec MJB3 mask aligner was used to expose the photoresist with UV radiation, which was then developed with Rohm & Haas MF319 (Metal Free developer) to get the Ohmic pattern. This process was followed by evaporation to metallize zinc/gold with 10nm and 90nm, respectively, producing Ohmic contacts.

The second step started with spinning PMMA on the sample. The EBL technique was then used. The sample was loaded into a Raith E-line, using 10KV, with a 10µm aperture size, 100µm write field and 10mm working distance to expose the resist with a beam of electrons. Split gates and arms (taps) were written on the resist using some alignment marks on the sample for registration. A metallization process then deposited nickel/gold or titanium/gold with 10nm and 90nm thickness, respectively.

In the FEED step, a PMGI-SF6/S1813 bilayer of photoresist is spun onto the sample, followed with optical lithography and nickel/gold deposited with 50nm and 300nm thicknesses, respectively. In the MESA step, the semiconductor wafer layers are etched, except the substrate and pattern under Ohmic and FEED metal. The area under the gates is etched to make the air-bridges by spinning the sample with a resist and exposing it with UV using a suitable MESA mask for 8 seconds. Wet etching involves using lactic and nitric acids (50ml and 10ml ratios, respectively) etches down from the surface by approximately 2.5 µm to isolate the device electrically and form the air-bridge.

The MESA mask design produces a copy of the etching pattern of the active area bar, as in *Figure 3.10*: (a) bar area, (b) with two islands sporting tall gate arms, and island area in (c) without supporting island, considering leakage from gate arms to the active area.

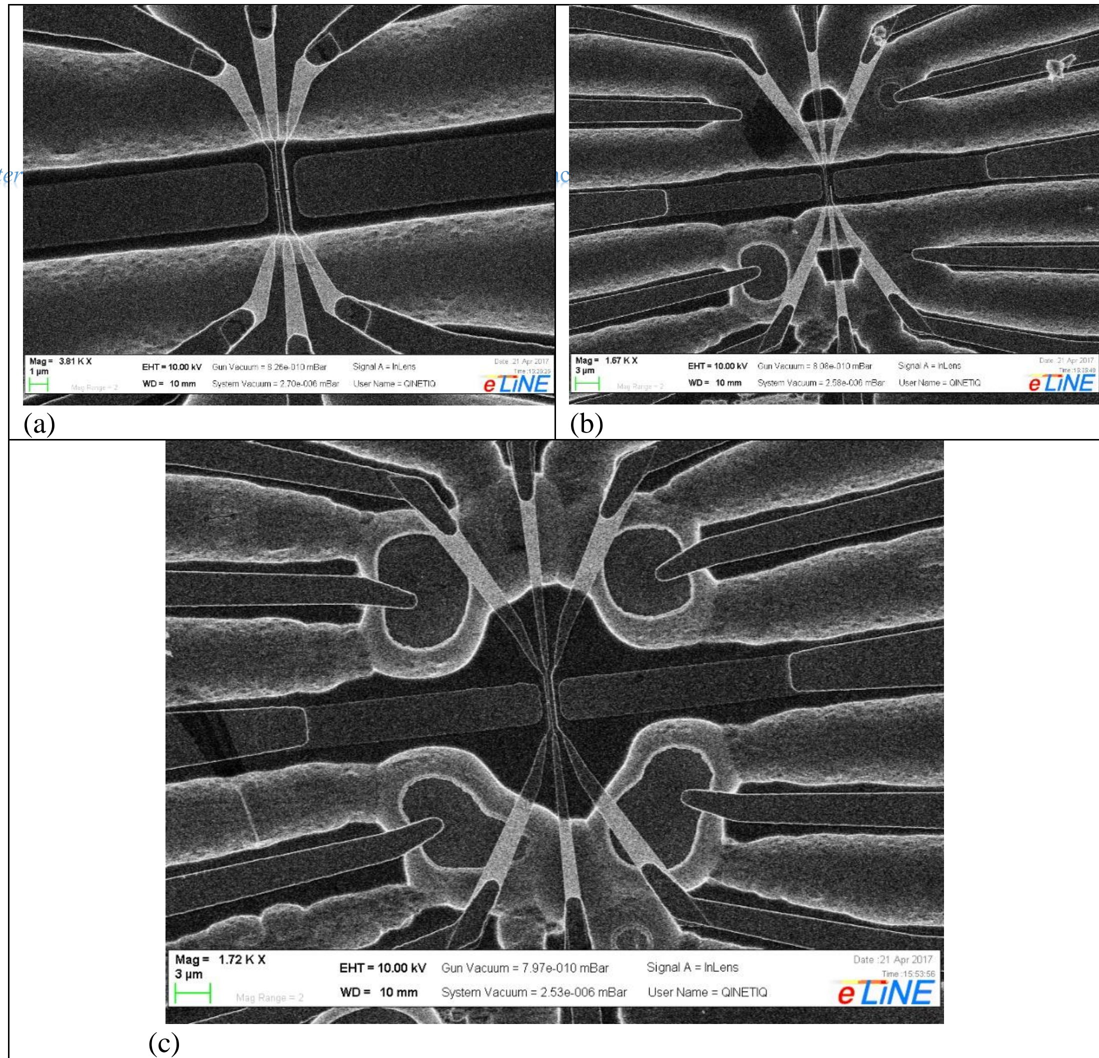


Figure 3.10: SEM images of the active region of the mesa. This highlights three kinds of non-etching areas; (a) only area between Ohmic contacts as a bar, (b) two small islands on the sides of Ohmic area, and (c) the area between Ohmic contacts as a big island.

3.4 Techniques

3.4.1 Lithography (Photo and EBL)

3.4.1.1 Photolithography

Photolithography uses ultra-violet (UV) light to interact with a light sensitive polymer, called *photoresist*, to produce a microstructure. This is the standard technique for the large-scale industrial production of these devices. Due to the light wavelength limitation in the research environment, a resolution of only around 1µm can be achieved [17]. The advantages of using photolithography at the research level include low price compared to EBL, which requires a high- vacuum, charged particles source, and a variety of lenses to focus and controlling the beam. [18]

Principally, optical lithography is photography of an original image to be copied using a photomask, which corresponds to a negative in photography, to get an image the same size as the original print on the mask. The photomask is aligned to the photoresist-coated wafer and exposed to UV radiation. UV exposure changes the photoresist's solubility, which enables selective removal of resist in the development step. In positive resists, the exposed areas become more soluble in the developer, and in negative resists the exposed parts become insoluble [17].

There are three elements in an optical lithography process. The first is the optics part, including radiation generation, propagation of radiation, light diffraction and interference at the resist layer. The chemistry part includes photochemical reactions in the resist and the development of the exposed photoresist. Finally, the mechanics part includes setting the mask to wafer alignment, and parallelism and focusing using lens settings. Image resolution is essentially determined by the pattern dimensions on the mask, although small patterns can in theory be made by pressing the mask into high contact with the resist surface, which is called vacuum contact. However, this will produce defects from the resist debris adhesion to the mask [19] and is a drawback of contact photolithography. The common subtractive patterning process shown in *Figure 3.11* involves three steps: first, deposition of a uniform film of photoresist on the wafer; second, lithography to create a positive image of the pattern that is desired in the film; and finally, develop to transfer that pattern into the wafer [20].

A Karl Suss MJB3 Contact Mask Aligner model MJB3 is used with a mercury discharge lamp UV radiation (~365nm), which is filtered and distributed uniformly over the wafer. The lithography system, which is inside a class 100 Nano-both within the main cleanroom, has a yellow light filter because the photoresist is only sensitive below 450 nm [19].

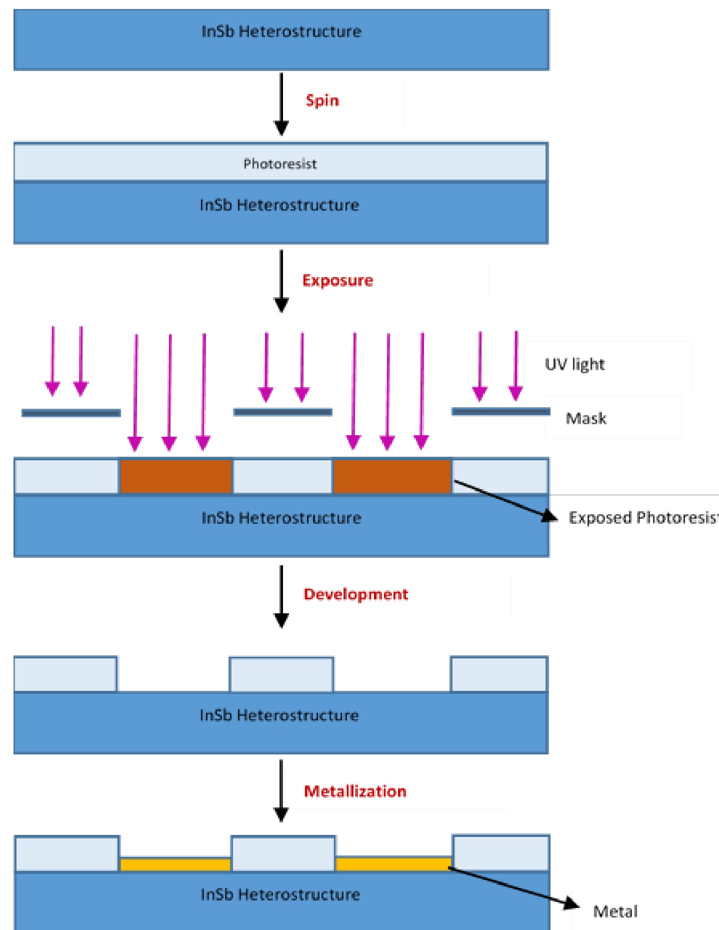


Figure 3.11: A schematic diagram showing typical photo lithography process steps (positive resist process).

3.4.1.2 Electron Beam Lithography

EBL is a fundamental technique of nanofabrication, which allows not only the direct writing of structures down to sub-10 nm dimension but can enable high-volume nanoscale patterning (unlike some other direct write techniques like FIB). In general EBL is necessary at the research level to define semiconductor structures with feature

sizes less than 1μm. The resolution of EBL is generally limited by scattering processes at the resist and substrate, although can be limited by the quality of column optics for most research systems. The lithographic process is essentially analogous and complementary to that of photolithography, whereas only the resist is sensitive to an electron beam, such as Poly (methyl methacrylate) (PMMA). The desired patterns are designed using specific computer software (generally GDSII) and written into the resist by a collimated beam of high-energy electrons, which are accelerated towards the sample. Typically, 10 keV has been used in this work in order to retain good beam resolution at the surface whilst providing a desirable exposure profile through the e-beam resist which is slightly undercut due to electron scattering. This greatly aids the lift off of the gate metal using a single resist layer, and avoids the use of a bilayer resist process and the therefore inevitable charge dispersal layer necessary to overcome sample charging. The beam position is controlled by magnetic fields (field coils) in the SEM column. Once developed, the exposed pattern is transferred onto the resist layer and can be used as a mask for subsequent metal deposition of small features, or for example etching (albeit with typically prohibitive erosion rates for EBL resists - Cross-linked PMMA is very often used as a high-resolution negative resist for EBL and physics applications for low-dimensional structures however with slower write times due to longer exposure).

A Raith E_line system with a minimum dimension demonstrated of ~20nm, was used to pattern the fine metal structures that define the split gate with a variety of designs that connects out to the features of the FEED metals. The gates and their arms are drawn using a GDSII editor within the E-line software. Overall, the dose used ranges from 0.7–1 with 0.1 steps for resist sensitivity was 165, to get best gate line quality and avoid over-exposure, which would produce a non-uniform shape (especially at the corners). The electron gun's aperture size is around 10μm. Whereas, the brightness and contrast ratios for indium antimonide topped with PMMA were 10% and 60% respectively. Whilst not critical, some samples have had the Ohmic patterns written by the E-line with new designs that have a wider contact.

3.5 Sample Cleaning

The normal procedure to clean the semiconductor wafer sample before starting sample processing is to soak the sample in NMP 1165 (mixture of organic compounds: 1-methyl-2-pyrrolidinone and Pyrrolidinone Compound) for 5 minutes in an ultrasonic bath and then soak it in acetone for 5 minutes in an ultrasonic bath. Finally, it is rinsed with Isopropanol. However, for some critical processes this has been shown to be insufficient, and for this material longer clean times or UV regimes have been used. It is essential to clean the sample after Ohmic deposition to remove the bilayer of photoresists. Two processes have been used: exposing the sample with UV for 30 seconds and then developing it with MF 319 for one minute, which is achievable and effective. A sample has been imaged with SEM in *Figure 3.12*: (a) before cleaning and (b) after cleaning.

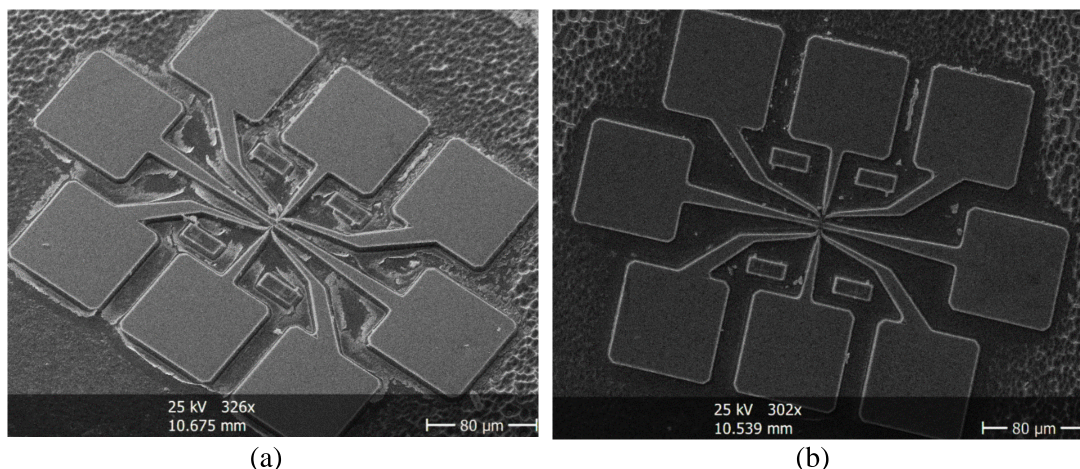
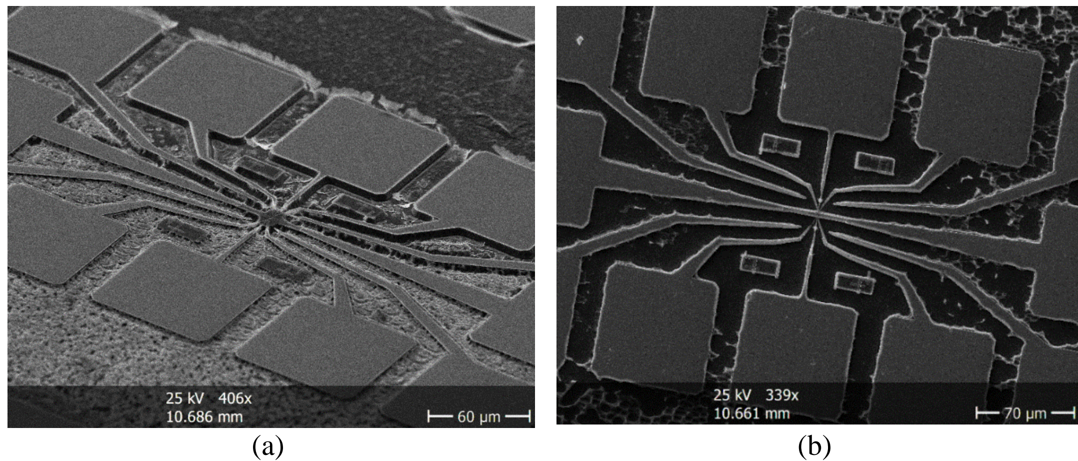


Figure 3.12: SEM images demonstrating the newly developed process of cleaning using UV exposure and development: (a) before cleaning, (b) after cleaning.

The second method is to soak the sample in hot NMP 1165 at 80 °C for 20 minutes, which is able to remove PMGI SF6 beyond detectable levels. The use of acetone in the left off process is unable to remove the SF6 photoresist, especially for PMGI-SF6 that has become solid and is difficult to remove after elevated temperature under high-vacuum from the deposition process for a relatively long time. A non-clean surface can lead to major problems in the device, even a thin layer of unremoved PMGI SF6 can result in high-Ohmic resistance, the lifting off metal pattern problem and can break the air-bridge gates due to non-even MESA etching. This residue is in general not a problem for conventional GaAs annealed contacts, and so these problems are specific

to narrow gap materials. This cleaning method enhances the etching process, even etching through the top layers down to the substrate. The SEM images in *Figure 3.13*(a) and (b) show how the new cleaning method enhances the etching process using the NMP 1165 hot remover.



(a) (b)

Figure 3.13: SEM images of device has been cleaned by the new process of the etching using NMP 1165 hot remover: (a) before cleaning, (b) after cleaning.

3.6 Wet Chemical Etching

The wet chemical etching technique can be used to remove material, depending on the material and the etchant. This technique is usually used in semiconductor device fabrication processes to remove undesirable material layers, such as electrical isolation or oxide removal. To remove an oxide layer for Ohmic contact pattern that has been pre-defined by photolithography, citric acid etchant is used to interact with the material and etch down at a rate of 2nm/min [21]–[24].

The last step of the sample fabrication is the MESA etching process. The MESA step is very important because it etches the semiconductor layers down to the substrate, except the area under the device, as an electron channel and produce an air-bridge under the gates to stop any current leakage from the arms or between the FEED pads. The MESA process spins the sample with a photoresist (S1813), which is not affected by acids, and then exposes the sample with UV using a MESA mask. The InSb wafer was etched with lactic and nitric acids with volume ratio 50ml to 10ml, respectively. The plan was to etch approximately 2.5 μm, approaching good isolation and air-bridge

formation. Comparatively, wet etching is an easy technique to apply but is hard to control, due to factors such as etchant PH, passivation, and the consistency of method of application by spin immersion and agitation [25]. *Figure 3.14* shows the spinning and etching process steps.

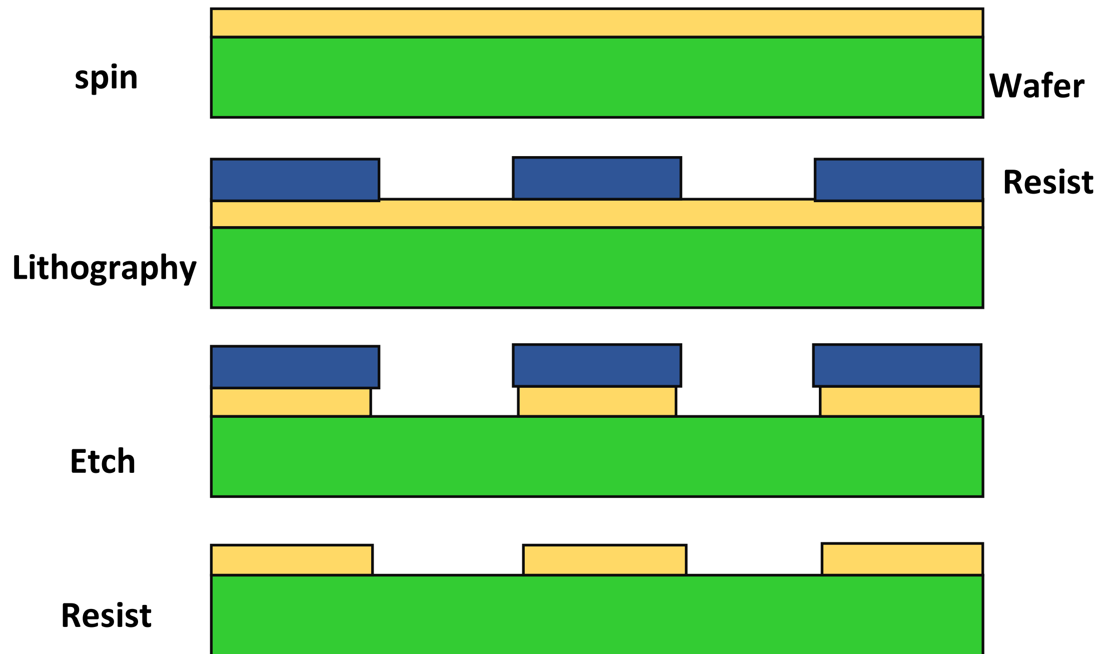


Figure 3.14: A schematic of the wet etching process steps with initial spin and bake, photolithography and wet chemical etching.

3.7 Plasma Ashing Technique

Plasma ashing causes degradation of the polymer surface and/or undesired creation of defects in the deposited films by ion bombardment with enough excessive kinetic energy to break the chemical bonds in the polymers [26]. The resist removal process has various demands. For instance, removal of any photoresist residual in the open windows and decreasing the thickness of photoresist on the top of pattern, which is a critical step to clean sample surface before metallization and avoids the lifting off of the metal pattern problem. Device performance and electric resistance is strongly dependent on the quality of the metal-semiconductor contact interface [27].

The ashing power that was used was 10 watts under 6×10^{-1} mbar of vacuum in an oxygen environment for 3 minutes with a rate of 10 nm/min for S1813 photoresist, before chemical etching and Ohmic metallization and longer for MESA etching [28] in terms of the PMGI-SF6 issue. Oxygen gas is used to avoid any contamination [29].

3.8 Wafer Surface Characterisation Techniques

3.8.1 Energy Dispersive X-ray Spectroscopy (EDX)

Energy dispersive X-ray spectroscopy (EDX) is a standard technique to identify and quantify elemental compositions in a very small area on the sample's surface, such as a few micrometres. The EDX technique detects and analyses surface elements by characterising a chemical composition of surface bonding and trace impurities using an electron beam to excite surface atoms and emit a specific wavelength of X-ray that is characteristic of the atomic structure of the elements [30].

Essentially, to successfully process and even before any metallization or chemical etching, the sample's surface is cleaned from any dirt or resist residue, even a very thin layer of dirt (few nanometres). The PMGI (SF6) usually sticks on the sample surface due to recycling of heating through post-baking and deposition, especially IBM deposition. The PMGI (SF6) layer cees or postpone the citric acid etching (The PMGI (SF6) residue impedes uniform the citric acid etching), which produce high-Ohmic contact resistance as well as destroying the device gate bridges through the MESA etching process. (PMGI resists consist of polydimethylglutarimide polymer with proprietary solvent blends). Contamination on the InSb surface can be observed in *Figure 3.15*. Image (a) shows a clean rectangle after E-beam exposure by the EDX technique on AlInSb/InSb surface (outside device), which clearly shows a thin layer of photoresist. Images (b) and (c) show a measurement on a surface between the device structure and the top of the FEED pad metal (Au), respectively. Both show a photoresist residue by characterising carbon and oxygen elements. Image (d) shows the etchant breaking through the thin layer of the photoresist and removal of some material and, interestingly, shows a circular broken portion of the photoresist residue (white colour). The characterised elements of (AlInSb/InSb) [31] image (d) were

O=6.49, C=3.15, In=8.52, Sb= 20.96, Al=2.15, Ga=31.38, As=27.35, as presented in *Figure 3.16*. The measurements were carried out at Cardiff University in the clean room using a Hitachi Regulus SU8230 ultra high-resolution SEM.

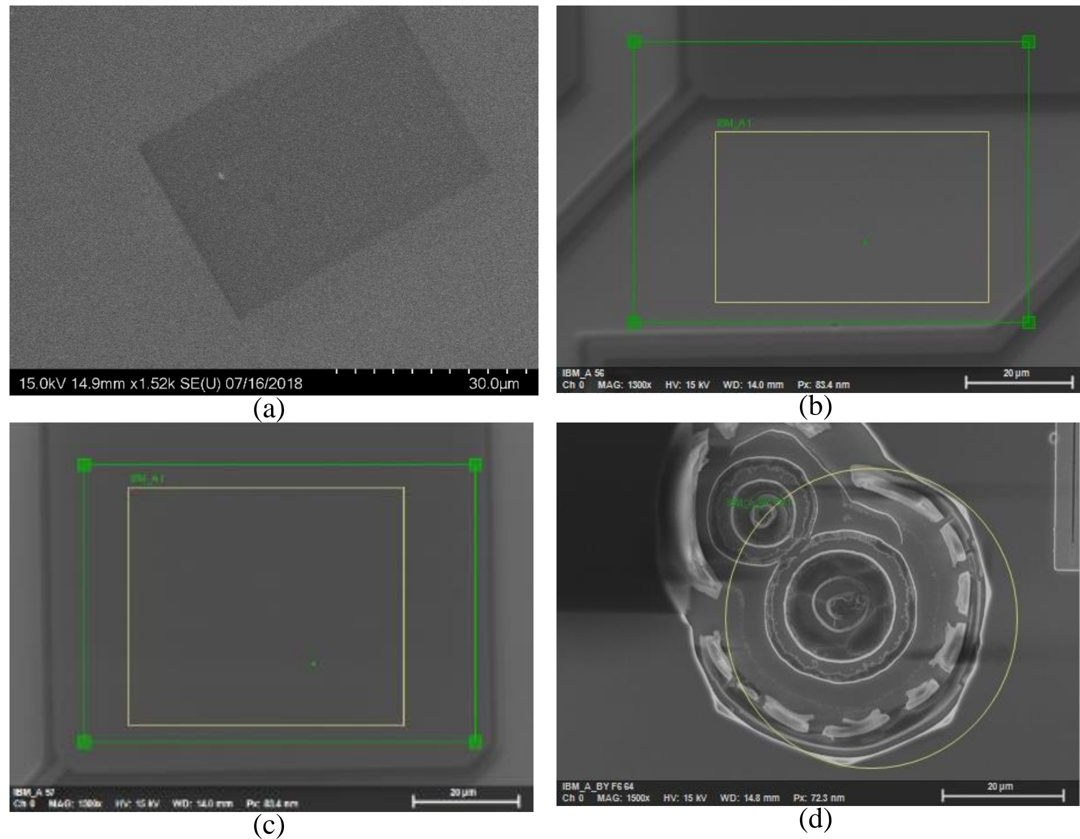


Figure 3.15: SEM images of a spilt gate device: (a) on AlInSb/InSb QW surface (outside device metal) exposed a rectangular area by e-beam and flake of photoresist as white colour, (b) measures area on AlInSb/InSb QW surface between a device metal structure, (c) measures on the top of FEED metal and (d) measuring an uneven etched area present the wafer layers.

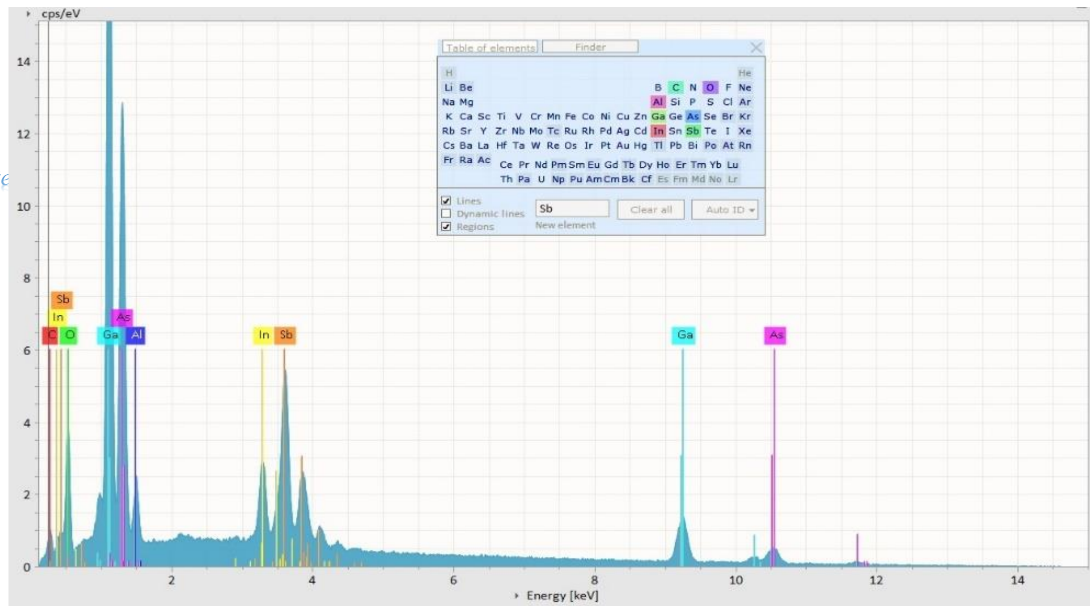


Figure 3.16: EDX spectrum and elemental quantitative data representative of AlInSb/InSb QW device for the etched area shown in Figure 3.15(d). This shows the constituents of the wafer and any contaminating elements (carbon and oxygen for example).

3.8.2 Atomic Force Microscopy

The atomic force microscope (AFM) is an effective tool for probing and investigating the ultra-small topographic features on the surface of solids using a specific tip. AFMs can be used to measure surfaces that may be either electrically conducting or insulating. The small forces can be scanned by a very flexible cantilever tip that has an ultra-small mass and sharp taper at the end (the tip). The scan moves the sample with a piezoelectric scanner on an X, Y, Z movement stage. Since the AFM operates in several modes—including contact, non-contact and tapping modes—in the initial contact, the atoms at the end of the tip experience a very weak repulsive force due to electronic orbital overlap with the atoms in the sample’s surface. The force acting on the tip causes a lever deflection, which is measured by an optical detection technique such as laser interferometry. AFM has become a popular surface profiling technique for microscale and nanoscale topography and is capable of producing very high-resolution in three-dimensional imaging of a sample’s surface up to atomic resolution [32]. This technique also gives an understanding of the fundamental nature of bonding

and interactions in materials, combined with advances in computer-based modelling and simulation methods that enable prediction of the nature of interfacial layers [33]–[36].

An AFM model Digital Instruments Veeco Metrology Group, Dimension™ 3100 has been used in tapping mode to determine the surface roughness and topography of the AlInSb/InSb heterostructures reported, both before and after etching of samples using wet and dry etching techniques. These form the basis of results in presented in Chapter 4. A schematic diagram of a typical AFM set-up is shown in *Figure 3.17*.

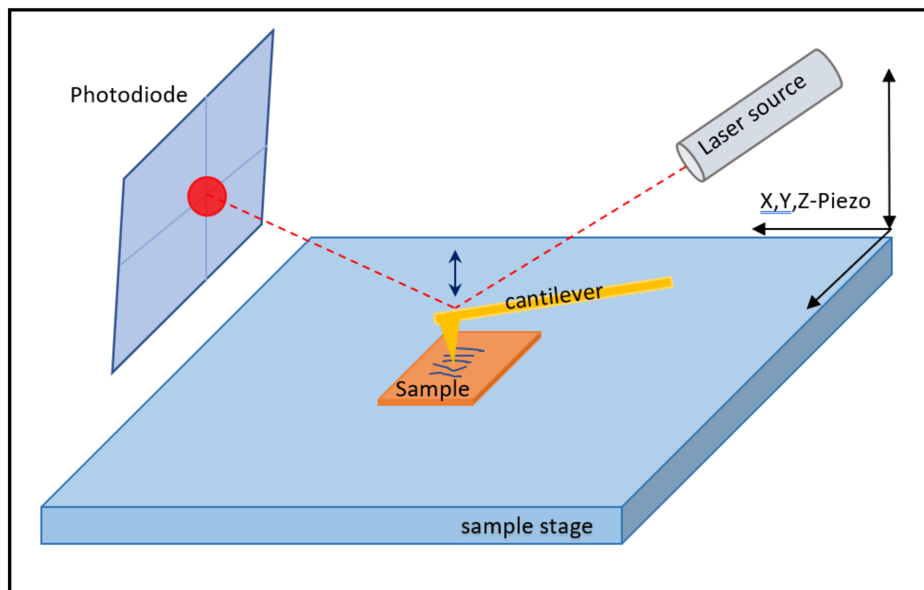


Figure 3.17: Principle of operation of the atomic force microscope, including cantilever moving up and down, photodetector with red spot and laser source.

3.9 Device Characterisation

3.9.1 Scanning Electron Microscope

The scanning electron microscope (SEM) is one of the most versatile instruments available for the examination and analysis of the material microstructure morphology and chemical composition characterizations. It is necessary to know the basic principles and fundamentals of electron microscopy. This microscope is consisting of

column and specimen chamber that can be under vacuum. At top of the column the electron gun has been located that produce the electron beam [38].

The electron, as a 'particle', can be accelerated, focused, and detected. As a 'wave' it has a shorter wavelength than visible light and can illuminate a specimen surface to higher resolutions than in an optical microscope. In principle, an electron beam can be produced by a scanning electron microscope (SEM) gun which is focused to a small spot and scanned in parallel linear scans over a specimen's surface. Electrons re-emitted or reflected from the surface can be detected simultaneously with an electron detector inside the specimen chamber [37] [39].

A SEM produces electrons typically with a thermionic, Schottky or field-emission cathode. These electrons are accelerated through a voltage difference between the cathode and an anode, that may be as high as 50KeV. The SEM can image and analyse a material's surface as a bulk specimen. These kinds of SEM systems operate with different beam cross-sections, which are produced by the gun with a diameter of around 1nm to 50 µm, depending on the design and the magnetic lenses system forming at the specimen surface, with currents of 10^{-9}–10^{-12} A [40].

With backscattered (reflected) and secondary electrons (essentially absorbed and re-emitted), a large variety of electron-specimen interactions can be exploited to form the image and to furnish qualitative and quantitative information. The magnification can be simply increased by decreasing the scan-coil current and keeping the image size [40].

SEM images reveal the physical quality of the devices though the fabrication process, helping to characterise the surface residue via EDX, metallization quality, distances between device structures, monitor etching depth and evaluation of the air-bridging by angled imaging. A Phillips Model XL-30 SEM is used for the majority of routine imaging in the clean room of the Physics and Astronomy School, Cardiff University, with high resolution and EDX being done using a Hitachi Regulus SU8230.

3.9.2 Room Temperature I-V Measurements

Local cleanroom measurement was done using a (gold tipped) needle probe station which gave an idea and initial characterisation of the Ohmic resistance of up to 30 devices at a time. This helped to choose some good (not broken) or low device

resistance devices for wiring. The tip arrangement consisted of four probes, but only two terminals are generally enough to get source and drain to apply voltage and measure the current. Whereas, four terminals are required for TLM devices. A Keithley model 2400 series meter was used to apply low DC voltage sweep of about -0.5 to +0.5 V and to measure the current in terms of heating and melting possibility of gates. The 2400 Keithley is interfaced with a computer to set the voltage and plot its current using in house software.

3.10 Packaging and Wire Bonding

Packaging and wire bonding are the final steps after cleaving. In general, the chip is cleaved into 12 fields before packaging, binding and measuring. Each good field can be mounted into a ceramic package (3.5×3.5 mm^2 inside) using GE varnish as a glue, which is left overnight to air dry before bonding. The sample is packaged in 20 pin dielectric and non-magnetic ceramic leadless chip carriers (LCC). An ultrasonic West-Bond 7400A Wedge wire bonder was used with 12.5 μm diameter Au wire to connect the device pads to the chip pins. A heated sample chuck (to around 100° C) was used in the wire bonding process. This is combined with manual pressure applied to the thermocompression process that provides a strong mechanical and electrical connection for the pad metal and the Au wire [30].

3.11 Low Temperature Measurement

Samples were cooled to a low temperature, which is necessary to achieve electric measurements whilst minimising scattering effects by phonon. Low temperature measurements were carried out using a liquid cryogen free cryostat system for AlInSb/InSb QW of TLM and split gate devices, (results presented in Chapters 5 and 6, respectively). The samples were mounted into 20 contact ceramic packages and mounted into a package holder on the cold-finger of an *Oxford Instruments Optistat* AC-V12 pulse tube system. The system consists of a *Cryomech, Inc* PT403 cold head, *Cryomech, Inc* CP830 helium gas compressor, which is cooled by a chiller using

water, and an *Oxford Instruments* Mercury iTC temperature controller. This system cools samples to a base temperature of 2.7K within approximately 90 minutes. The sample chamber of the PT403 cold head is held in a vacuum, discharged by an *aerlikon leybold vacuum* turbolab 80 basic turbomolecular pumping system with a dry compressing backing pump. These pumps work to get 5×10^{-5} mbar within approximately 15 minutes. The cryostat system is connected to an Agilent Technologies model (E5270B) precision current voltage analyser and an Agilent Technologies E5281B Medium Power Source Monitor Unit (MPSMU). The voltage, current and variable temperatures measurements are controlled via IEEE by in house written Python software. The software controls the voltage values, steps, time of measurement at a sweep of temperature after thermal stability with a typical time delay of 10min. *Figure 3.18* shows a schematic diagram of the main components of the cryostat system.

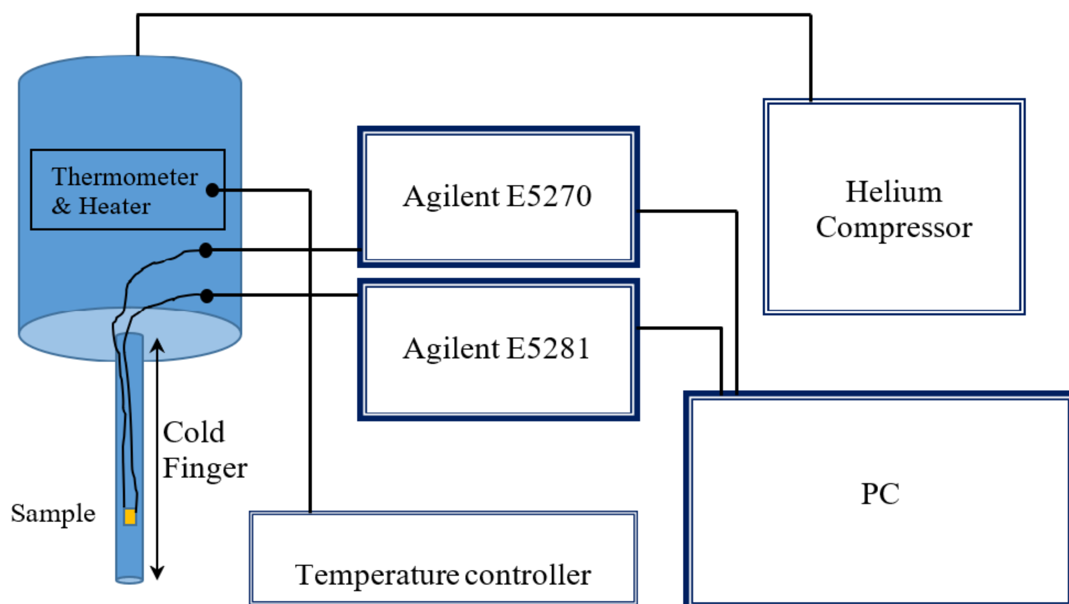


Figure 3.18: Schematic diagram of the main components of the low temperature measurement system by positioning the sample in the cold finger which connected to temperature controller and the sample to two Agilents.

3.12 Conclusion

This chapter presents the physics of the InSb crystal structure (zinc blende) and the growth onto GaAs substrates (considering lattice mismatch). InSb heterostructures studied here were grown by solid source MBE machine at the National Epitaxy Facility (Sheffield) and QinetiQ (Malvern). This heterostructure design which includes top cap layer doping results in band bending in the top cap and the embedded QW layer.

These InSb heterostructures have been used to fabricate split gate devices and TLM devices at Cardiff. Both designs are presented in this chapter with their typical active dimensions and some issues of device layout have been considered. There are many techniques required to fabricate devices, such as spinning, photolithography, electron beam lithography, plasma ashing and sample cleaning techniques. Ohmic contacts have been etched using dry and wet techniques aimed at investigating low contact resistance. Wafer characterization has been performed using EDX which has demonstrated surface photoresist residue and using the AFM technique to measure the surface roughness of the pristine surface and Ohmic contact after etching.

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Chapter 4

InSb Heterostructure Surface Characterization

4.1 Introduction

It is essential to understand the wafer surface when addressing the challenges of electrical contacting that would enable the optimum functioning of quantum devices such as split gates for charge sensing. The study in this chapter is important in characterising two possible contacting techniques for this narrow gap material that are not based on annealing and investigates the sample roughness as a figure of merit for the controlled etch techniques. A solid surface has a complex structure. Its properties depend on the nature of the solid, method of surface preparation, and the interaction between the surface and the environment. Surface interaction is extremely dependent on the properties of the surfaces. Properties that affect the real area of contact cause the effects of friction, wear and also lubrication. Moreover, surface properties can determine for instance optical and metallization properties, as well as for a lot of materials electrical and thermal performance.

The surface structure (oxide), morphology and roughness of an Ohmic contact is a major concern. This is because oxide and 'rough' surfaces can cause problems in later processing steps, primarily coating steps and electrical performance, potentially reducing device yield. There are many investigations on surface oxide and very few on the surface roughness of alloyed Ohmic contacts even though this is the common way of forming Ohmic contact to III-V materials. Good contacts without oxide by dry

and wet etching techniques with smooth surface morphology can be developed concerning any rough surface. But without annealing process, with concern that can be affected the InSb QW material in various ways by heating [1][2].

This chapter describes the surface oxide of AlInSb/InSb wafers fabricated at the III-IV Semiconductor Centre in Sheffield as pristine samples. The XPS technique has been used to investigate the surface oxide of the wafer (details of which can be found in chapter 3). The wafer surface oxide produces a high resistance (metal-semiconductor) contact that detriments device performance considerably to such an extent that only limited observation of quantised conductance could be observed. For this reason, the oxide needs to be controlled and/or removed. The chapter investigates the surface roughness of pristine wafers and etched AlInSb/InSb wafers using citric acid wet etching and Ion Beam Milling, two techniques that have been used in the formation of Ohmic contacts etching the top cap of the wafer.

Surface roughness data are analysed statistically for both the pristine and etched samples using AFM and considering the effects of image distortion by the measurement technique (such a scan direction and effective roughness length scale). Details of the XPS, AFM and IBM measurement techniques, and fabrication are explained in Chapter 3.

4.2 Surface Oxide Characterisation

The chemical nature of semiconductor surfaces can have an essential effect on the electrical performance of devices. So, the III-V semiconductor oxide layer can be unstable related to density of state in the band gap formed by the oxide capping which relevant to the interface of the compound. As well as, the spatial homogeneity of the interface (between the surface oxide and the unoxidized semiconductor) is also be subjected of electric variation. Therefore, the oxide property (chemical composition, texture, morphology, etc.) strongly influencing the kinetic energy of electron transfer through the interface. In the case of InSb Ohmic contacts, the carrier concentration of the material used, that its electron transport can be adversely affected by the presence of surface state of top cap layer. Therefore, the electron concentration reduces in the oxide and increases the interface barrier which lead to increase directly the contact

resistivity [3][4]. Therefore, to control the surface state is required a surface etching [5][6].

Moreover, oxide formation on the semiconductor surface material after exposing to air with an element, but with another free element will generate a conductive layer that lead to leakage current in the top cap and decreasing the resistance of the device, which effectively limit the device performance [7]. Consequently, it is necessary to remove the native oxide from the semiconductor surface before deposition process. Webb and his colleagues have cleaned the InAs/Insb nanowires using Atomic Hydrogen technique and characterised with XPS showing Sb_2O_3 before but not after cleaning process. This process has modified and increased the conductivity of 2 orders of magnitude but using 380°C temperature [8], which is not applicable for InSb QW. InSb wafer surface oxide has been examined and characterized its elements using X-Ray Photoluminescence Spectroscopy (XPS) technique [9][10] for sample dimensions (approximately 1×1 cm^2). *Figure 4. 1* shows the XPS result of sample covered with a photoresist. *Figure 4. 1* (a) shows that an obvious exist of carbon (red line) and oxygen (turquoise line) elements that belong to the photoresist layer. Then start with semiconductor layer consist of indium (green line) and antimony (grey line) elements layer. Moreover, in *Figure 4. 1* (b) shows obviously in between photoresist layer and semiconductor layer an Antimony oxide layer (black line) which calculated of approximately 3nm thickness or about five atomic layers which is with same thickness reported by Van in the room temperature [11].

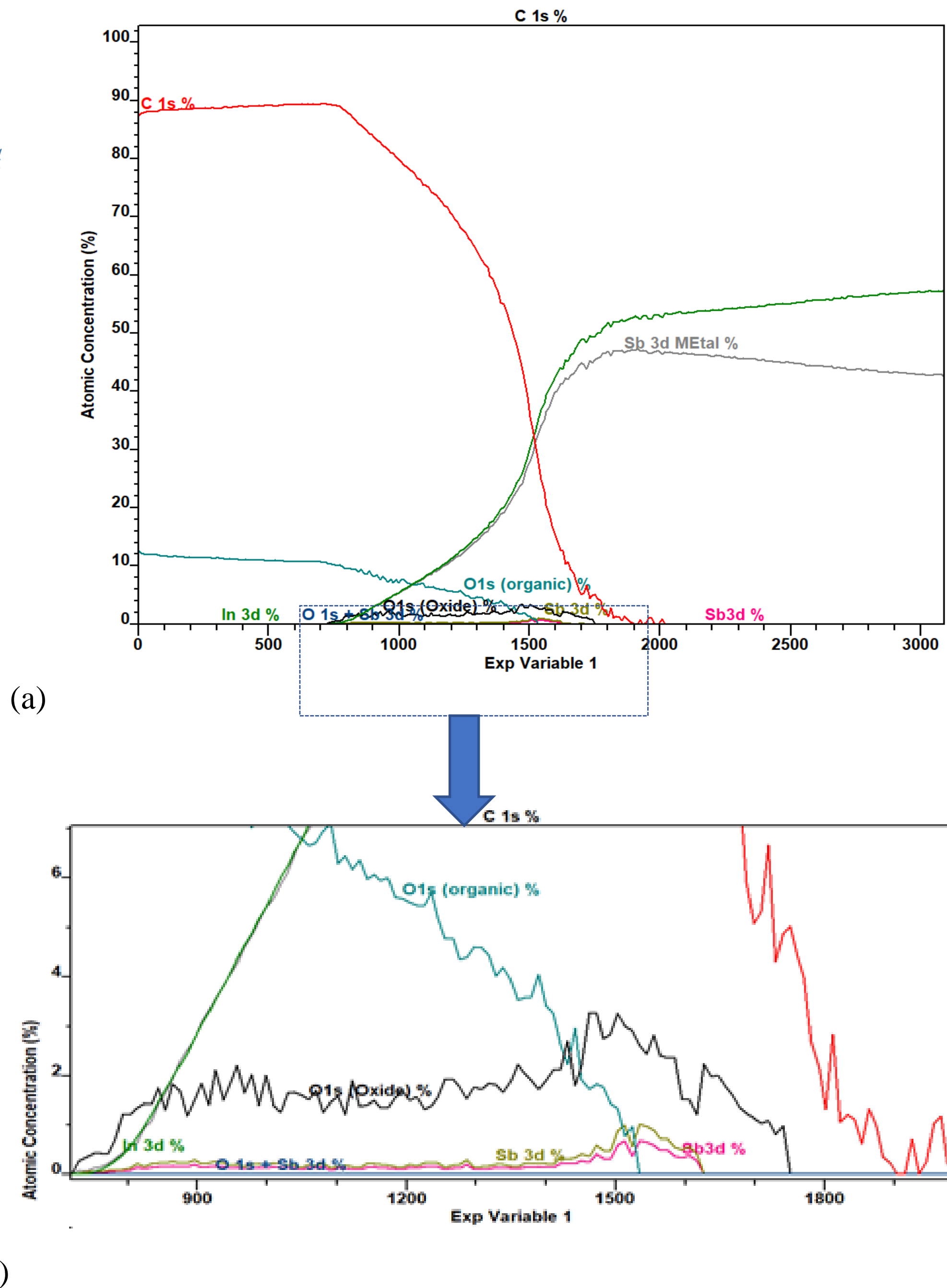

Figure 4. 1: shows the XPS analysis of AlInSb/InSb wafer; (a) for the wafer and the covered resist. The carbon 1s (red line) and oxygen 1s elements represent the resist layer up until the end of the semiconductor surface. This then continues with the observation of In 3d (green line) and Sb 3d (grey line). whereas, (b) the semiconductor surface start with oxide (black line), In (green line) and Sb 3d in (pink line). Note: the x-axis is representing time of etching with depth.

Figure *4. 3* shows that a typical diagram of InSb wafer layers covered by a resist and the first ~3 nm layer of the top cap has been oxidised that measurement by XPS and plotted in *Figure 4. 2*.

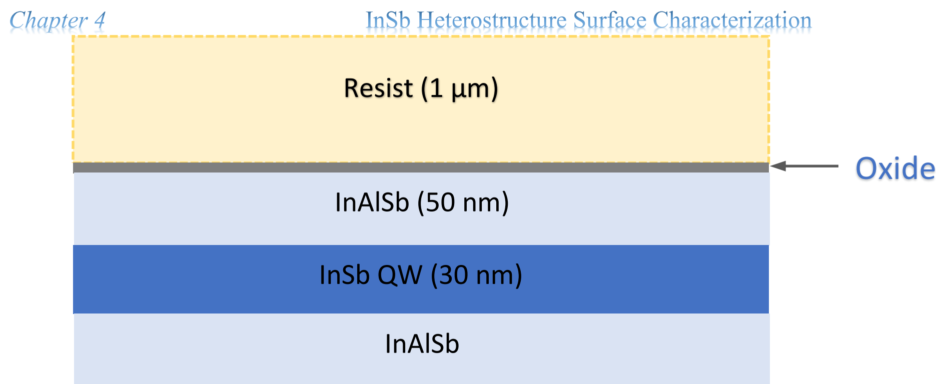

Figure 4. 3: Schematic diagram of InSb wafer presenting resist layer (yellow) on the top, surface oxide layer (grey) and InSb heterostructure layers (blue).

Figure 4. 4 shows XPS of the clean surface (without photoresist). Carbon element (green line) seems very thin layer which is a contamination layer. Whereas, the antimony oxide (black line) is clear in the semiconductor layer. XPS analysis shows aluminium element (red line) obviously in the top cap layer and stopped by the QW layer.

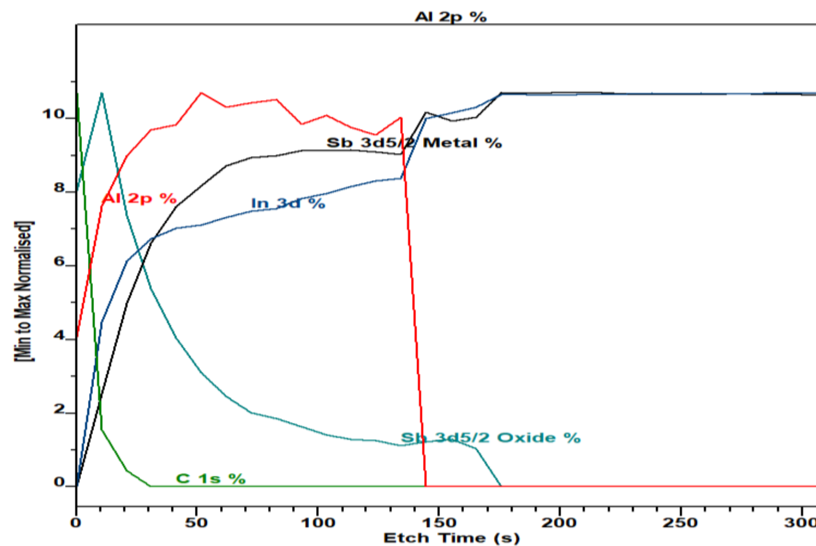

Figure 4. 4: shows the XPS analysis of AlInSb/InSb wafer of cleaned sample surface (without photoresist), starting with Al 2p (red line), Sb 3d (torques line) and (black line) and In 3d (blue line). At 150 second, the Al has stopped (top cap) and only In and Sb keep in high percentage in the QW.

The binding energy in the III-V crystal is much greater than that of many alloys. This high-binding energy causes the breaking of the crystal bonds to be a limiting step in the oxidation process [6]. Resulting less oxidization than other semiconductor materials, for instance GaSb [12].

4.3 Surface Roughness Characterization

Surface roughness commonly refers to the variations in the height of a surface relative to a reference plane. It is measured either along a single profile or along a set of parallel line profiles that form a three-dimensional topography of the surface. The measurement of the surface roughness is one of the most critical steps concerning the analysis of the contact between two surfaces. It is crucial for the quality control of the surfaces. Various alternatives in relation to the techniques for measuring surface roughness exist today, however Atomic Force Microscope is a good choice for surface analysis that can pick-up high-resolution topology in the order of nanometres. The solid surface comprises irregularities of various orders, ranging from shape deviations to irregularities of the order of interatomic distances. Any growth technique cannot produce a perfect atomically flat surface of a conventional material. Even the smoothest surfaces, such as those obtained by cleaving along a crystal plane comprise irregularities, the heights of which easily exceed interatomic distances.

Figure 4. ***5*** is a schematic diagram of a typical sample, showing an etch trench across the middle of the sample (typically 40microns wide) and the left and right sides which are typically 10microns wide. Furthermore, typical scan directions slicing in the horizontal and vertical axis of each part are shown. In each case, the line profile is measured and the RMS roughness for each slice in both directions is extracted.

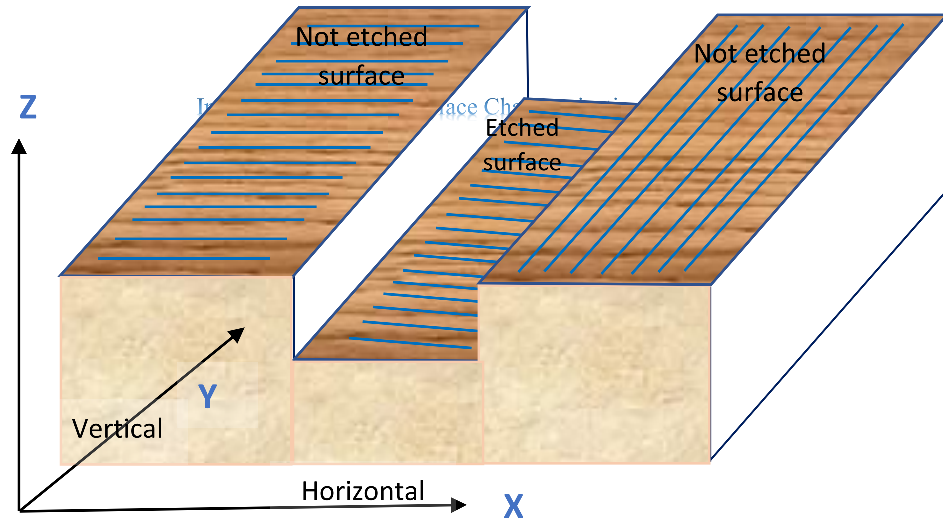

Figure 4. 5: A schematic diagram of the sample for the trench, and the left and the right surfaces. The stripes are a schematic representation of the horizontal and vertical scan directions (slices) dividing the surface. This is effectively the AFM tip direction in the x and y plane.

The RMS is the geometric average height of roughness irregularities over the sampling length, which is be given by

$$RMS = \sqrt{\frac{z_1^2 + z_2^2 + z_3^2 + z_4^2 \ldots \ldots . . + z_n^2}{n}} \qquad \ldots.. (4\text{-}1)$$

These height data (z_1, z_2, z_3) can usually be plotted as a Gaussian distribution, given that the roughness of the surface is often highly random.

The characterisation of surface roughness via a homogeneous and isotropic Gaussian distribution can be relatively straight forward but provides a good approximation and has become one of the mainstays of surface classification. The Gaussian probability distribution is given by

$$P(x) = \frac{e^{-\frac{(z-\mu)^2}{2\sigma^2}}}{\sigma\sqrt{2\pi}} \qquad \ldots.. (4\text{-}2)$$

where μ is the mean of the distribution, σ is the standard deviation and x is a continuous variable ($-\infty \leq x \leq \infty$). The position of the peak represents the value of the mean.

Figure 4. 6 represents a schematic diagram of surface roughness and its typical Gaussian distribution, as well as the mean and RMS roughness values.

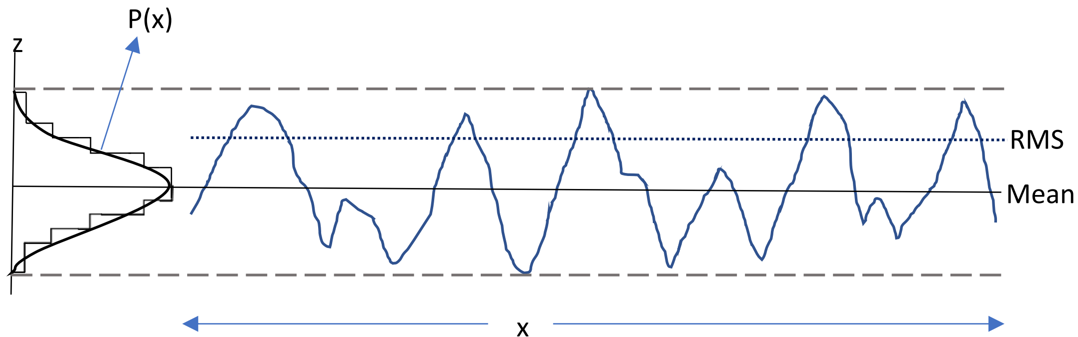

Figure 4. 6: Schematic diagram of surface roughness matching the height (Gaussian) distribution diagram with mean level and resulting in RMS roughness.

Where the median is a number of statistics that represents the middle of a dataset, the median formula is $\{(n+1)/2\}^{th}$, where n is the number of items in the set and th is the $(n)^{th}$ number. The Full width at half maximum (FWHM) is the width of a line shape at half of its maximum amplitude, as shown in *Figure 4. 7*. The technical term FWHM is used to describe the extent of the surface profile that can indicate the degree of the dispersion of the surface roughness height, which is an effective assessment parameter. The FWHM can cover most of the data of that extent, which is more than 68% of the most frequencies of roughnesses. Moreover, the FWHM can be calculated from the Gaussian distribution graph directly, as shown in *Figure 4. 7*, and is directly related to the standard deviation, which is given by the following expression [13];

$$FWHW = 2.355 \times \sigma \quad \text{…..} (4\text{-}3)$$

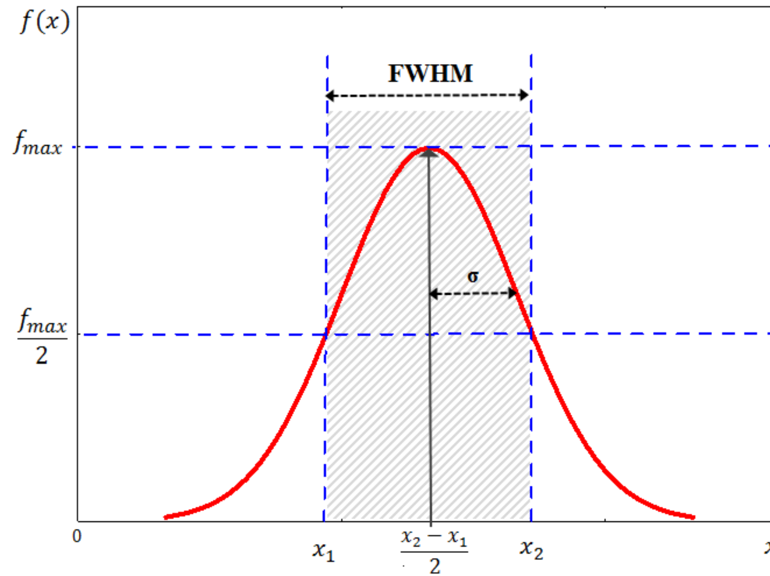

Figure 4. 7: Relationship between the standard deviation **σ** *and the full width at half-maximum (FWHM) of Gaussian distribution (frequencies of roughnesses).*

Since the surface texture is periodically, or random deviation from the nominal surface that forms the three-dimensional topography of the surface, the surface texture includes nano- and microroughness and waviness (macroroughness). The surface texture (roughness of area) derived from a typical AFM scan is displayed in *Figure 4. 8* for a real trench of an arbitrary sample surface and shows waviness (black surface roughness related to the red line along with different scales) and roughness (in local or short distance) in the profile. That is mean the roughness value is a relativity value which will be shown in *Figure 4. 11* and discussed in detail.

Sample surface roughness and etching depth, derived from sample images data analysis has been processed using Python code [(written by Chris McIndo) which checked by comparing with AFM Veeco software, Gwyddion, WSxM], Gwyddion, WSxM 4.0_Beta 8.5 (Windows Scanning × Microscopy where × if Force in AFM measurements) [14] and AFM Veeco software.

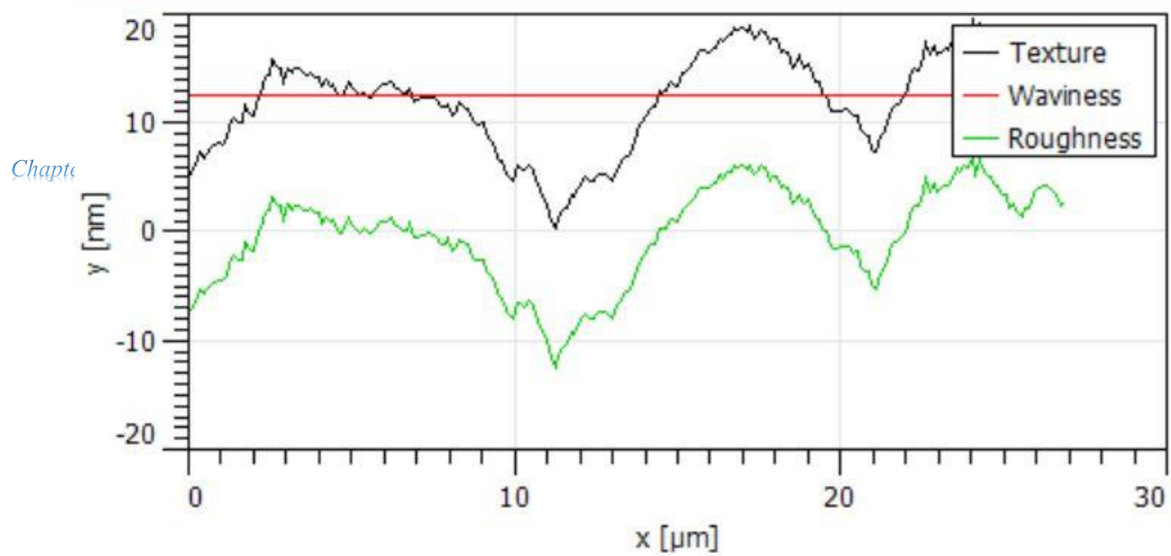

Figure 4. 8: Schematic diagram of the surface texture of types of roughness on a random InSb surface (captured from Gwyddion software), the 'waviness' shown by the undulations of the surface compared to the red line as a reference level.

4.3.1 Pristine wafer Roughness at zero and 90° degree

Figure 4. 9 (a) shows the three-dimensional topography of the pristine wafer of an AlInSb/InSb sample over a 40×40µm^2 area in an arbitrary direction approximately along a crystal axis. However, *Figure 4. 9* (b) illustrates the three-dimensional topography of the same area of the wafer, although in the 90-degree orientation (tip movement) of the AFM tip. The AFM tip movement can be set horizontally (X-direction) or vertically (Y-direction) in forward (trace) and backward (retrace) directions to obtain double measurements on the same line, with the aim of obtaining a precise profile of the 'mountains' and 'valleys' of the surface. I.e line scans along the x-direction and Y-direction result the same result, which is the aligned to lithography X/Y. Furthermore, the AFM software can set the tip velocity and set point value of the taping mode to determine the image resolution. Additionally, the AFM image size can be controlled by a span of a few micrometres, up to tens of micrometres.

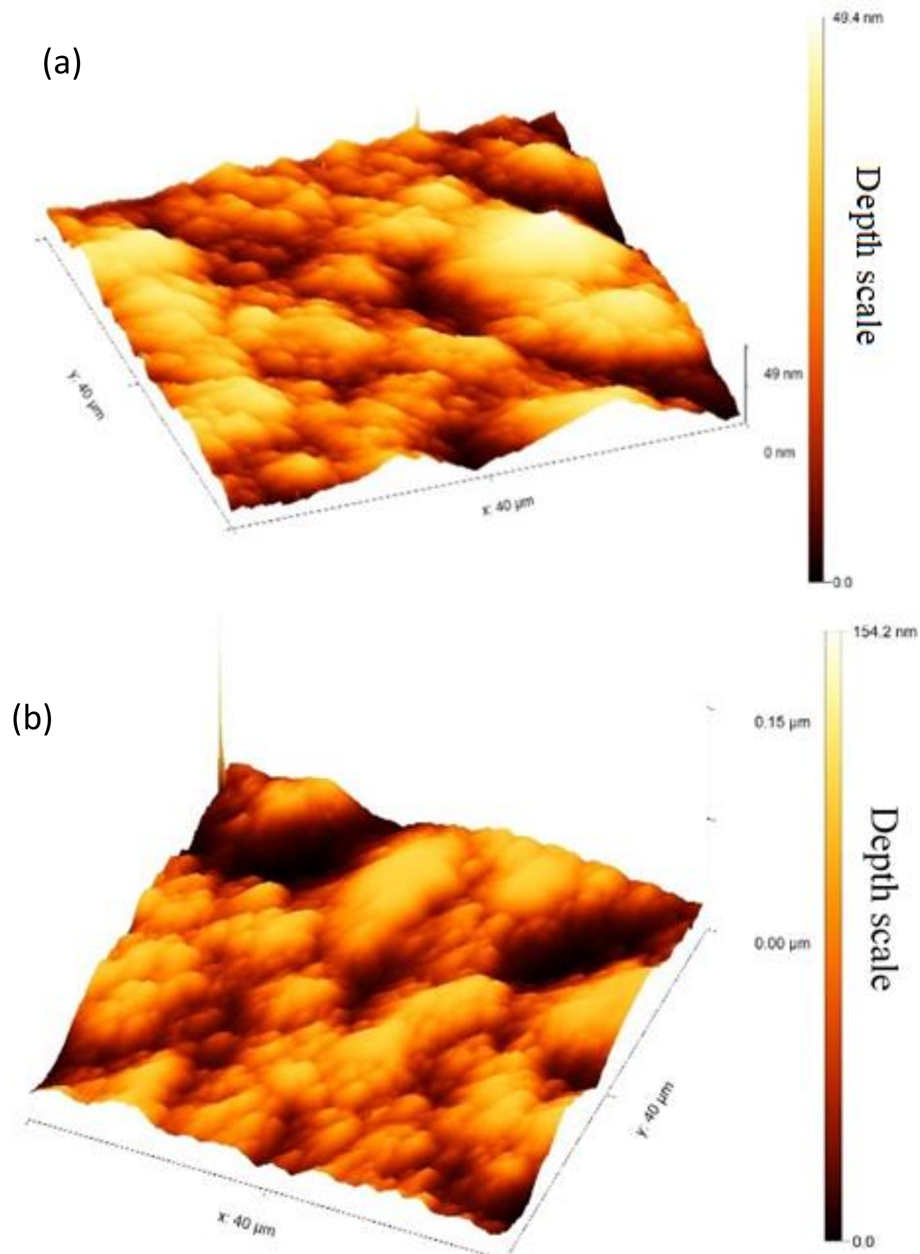

Figure 4. 9: AFM images of AlInSb/InSb wafer in three-dimensional profile; (a) at zero degrees on the wafer, and (b) at 90-degrees, the AFM tip measurement of the same area.

The reason for horizontal and vertical measurements is to check two points; specifically, the tip movement along the cantilever, and if there is a difference with regards to the laser spot reflection on the detector. This provides a good calibration of the measurements. Thus, the data analysis is plotted in the histogram in *Figure 4. 10*, as a Gaussian distribution, where the images are sliced in the horizontal and vertical

aspect and the 'Root Mean Square' roughness for each slice is measured depending on the data resolution.

The images in *Figure 4. 10* (a) and (b), reveal the maximum roughness and Gaussian distribution fit of the histograms which have been calculated by using equation 4.2 data that can be found in the range of 5nm for both zero and 90-degree angles. Moreover, the vertical slice data for the zero-degree angle reaches a frequency value of approximately 100, which agrees well with the horizontal data at 90-degrees. This represents the same values of surface roughness. Furthermore, both the horizontal data for the zero-degree angle and vertical data 90-degree angle is lower than the others with a different small value, seeing as the bars values and spreading away more than the others.

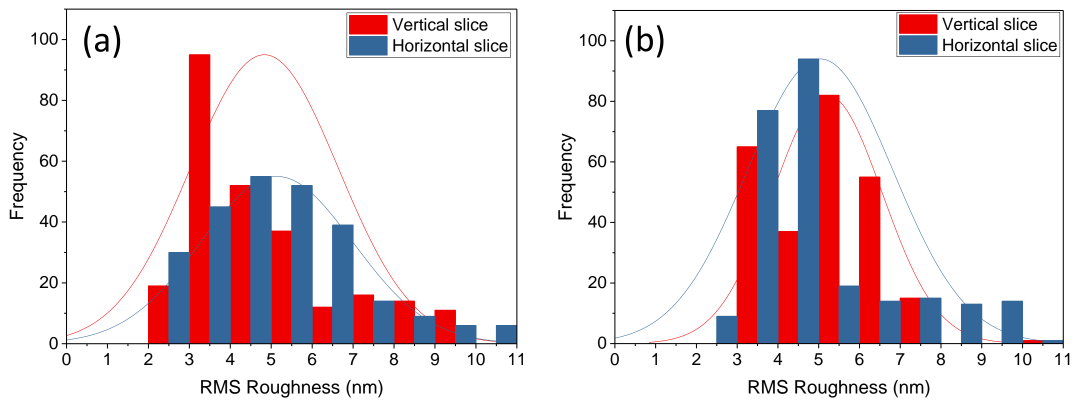

Figure 4. 10: Histogram of the pristine sample in vertical and horizontal slices with; (a) zero degrees and, (b) 90-degrees AFM tip direction measuring.

As a further investigation *Figure 4. 11* shows the RMS roughness of the surface for zero and 90-degree angles, as a function of the area size scanned. The zero-degree angle roughness as the solid curve, starting with ~ 1nm roughness and increases sharply. It begins to plateaux at ~ 4.5-5.0nm roughness and ends with a relatively steady value of ~6nm for a 30μm^2.

The 90-degree roughness presents behaviour that is comparable to that of zero-degrees, except for a slight dip at 25μm^2 scan size, which could be as a consequence of a change in the position of the small local 'mountain' observed between the two images, as can be seen in the AFM images in *Figure 4. 11*. These increasing trends suggest that the RMS roughness increases with the scale of the size of the scan area,

saturating in both cases above a scan size of 10-15μm^2. This mean the roughness can be in different value depend on the measurement scale, i.e roughness value is a relativity value which can enable to compare samples roughnesses with different scales, as well as, showing no difference between vertical and horizontal direction measurements.

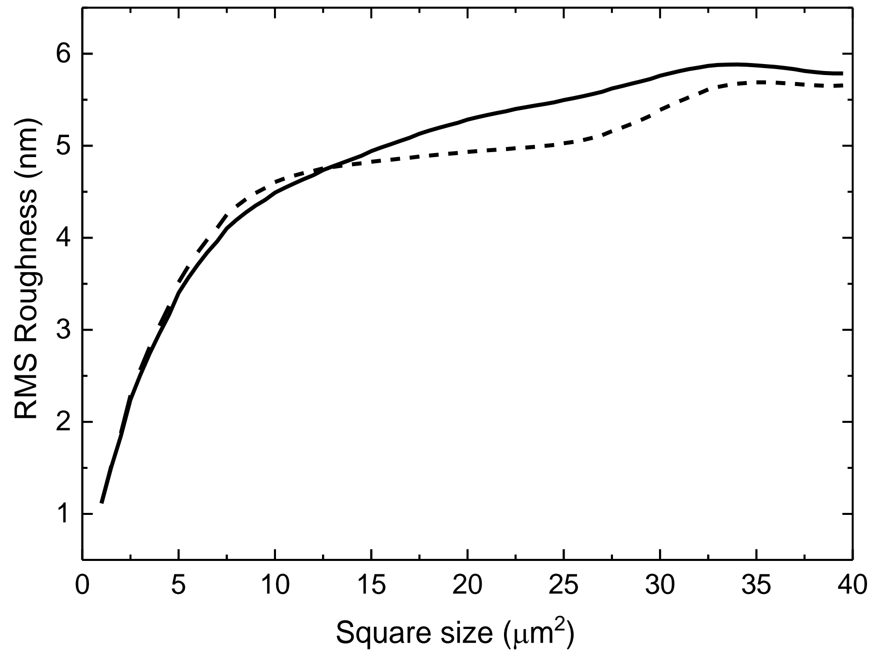

Figure 4. 11: RMS Roughness with square size for the pristine sample, a solid line for the zero-degree angle and dashed line for the 90-degree angle measurement.

Figure 4. 12 displays the mean and median of the horizontal and vertical slices of the image data for the zero and 90-degree angles. The mean values for vertical and horizontal slices are reasonably similar in the range of 5nm for both the zero and 90-degree angles, which is consistent with the histograms. However, the median value for zero-degrees for the vertical slice is just above 4nm and almost 5nm for the horizontal slice. The median values for 90-degrees are in reverse to the horizontal and vertical to zero-degree values, which is corresponds to the actual values of the surface roughness. The error bars indicate the standard deviation of the mean value and so from *Figure 4. 12* there is a high-degree of confidence that the mean and median are the same.

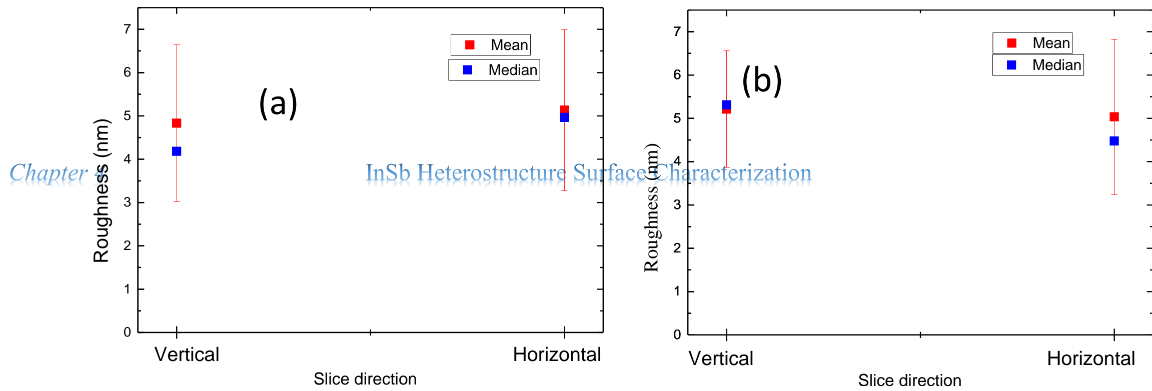

Figure 4. 12: Data analysis of the pristine sample in vertical and horizontal slices for; (a) zero angle measurement and (b) 90-degree angle AFM tip measuring. The error bar is the standard deviation.

These results of the pristine sample explain the wafer surface profile and the range of roughness in zero and 90-degrees of measurement for the same area, showing that RMS roughness for the square area, mean, median values and Gaussian distribution are virtually consistent with each other and establishes a well characterised benchmark for comparison. Additionally, the RMS roughness for the square area graph explains the saturation value of RMS roughness against the square size.

Measuring pristine sample as reference and give an idea before surface etching and comparing with surface roughness after using citric and IBM etching techniques. As well as, the AFM technique and its tip calibration is an important step by using it in different ways using horizontal and vertical direction measurements.

4.3.2 Citric Acid Etching for the AlInSb/InSb wafer

Citric acid ($C_6H_8O_7$) etching is a chemical interaction with the material surface of the wafer starting with the top cap, etching toward the quantum well (as outlined in Section 3.6) that is suitable for controlling the uniformity of array structure and proven the feasibility to bring superior etching process [15], which is reported also by Chang and his colleagues [16] and Aureau and his colleagues [17]. The used citric acid concentration is 1:2 ratio of granular citric (solid) and DI water. Furthermore, the surface roughness resultant by chemical etchant especially by citric acid is very

smooth [15]. An Ohmic pattern and standard photolithography was used to open windows in photoresist to allow the citric acid interaction and the etching of material. Oxygen plasma is used to ash these samples to remove any residue of the photoresist before etching, before samples are finally immersed in citric acid at a stable and controlled temperature (approximately 29°C) for a specific time and washed with deionized water.

Figure 4. 13 shows an example of the three-dimensional topography of the AlInSb/InSb wafer after Citric acid etching of a sample. Five samples were etched in the range of 5 - 25 minutes with 5-minutes steps. This is one of samples has been measured using AFM technique result in 3D image shows the trench depth (Ohmic contact etched area (black and red colour)) and non-etched area (yellow colour) on the left and right sides at a scale of 60×30μm^2 in the X (horizontal) and Y-axes (vertical) and depth in Z-axis for all studied samples.

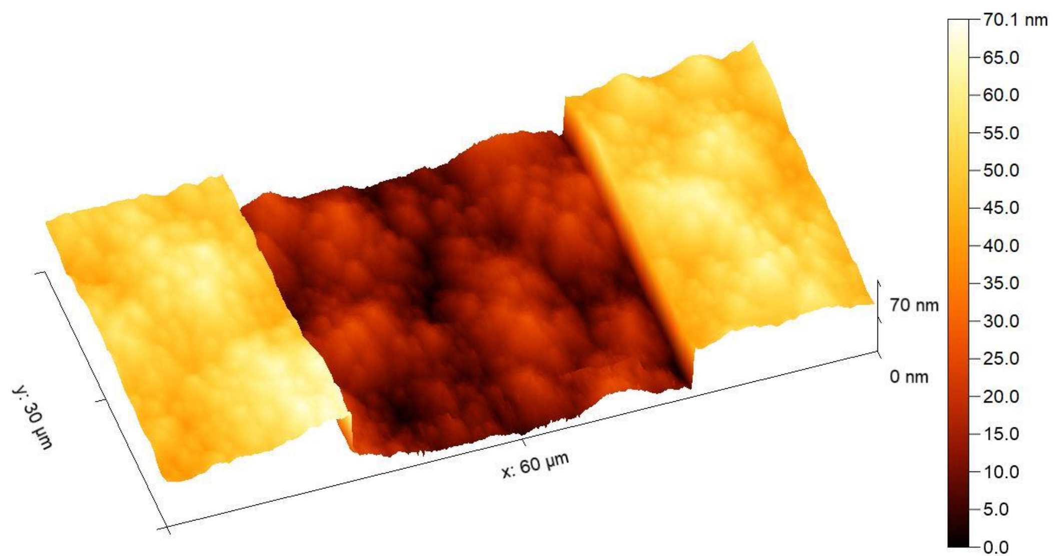

Figure 4. 13: An example AFM image in three-dimensional profile of the etched AlInSb/InSb wafer using citric acid.

The z-axis is the height range and is represented by the colour scale shown in the legend, for instance dark colours for valley as a trench that etched to a shiny colour on the top which is the non-etched area.

Figure 4. 14 confirms the relationship between the citric acid etching depth against etching time for different samples. Trench depth is measured by calculating the

difference between the mean value of the non-etched surface and the etched surface (trench). The graph shows there is clear increase in the experimental depth values against etching time with little of no induction phase at the start of the etch. The gradient of the linear fit to the data is calculated to be approximately 2.2 nm/min, which represent a good consistent etch rate for Citric acid etching of the AlInSb/InSb wafer.

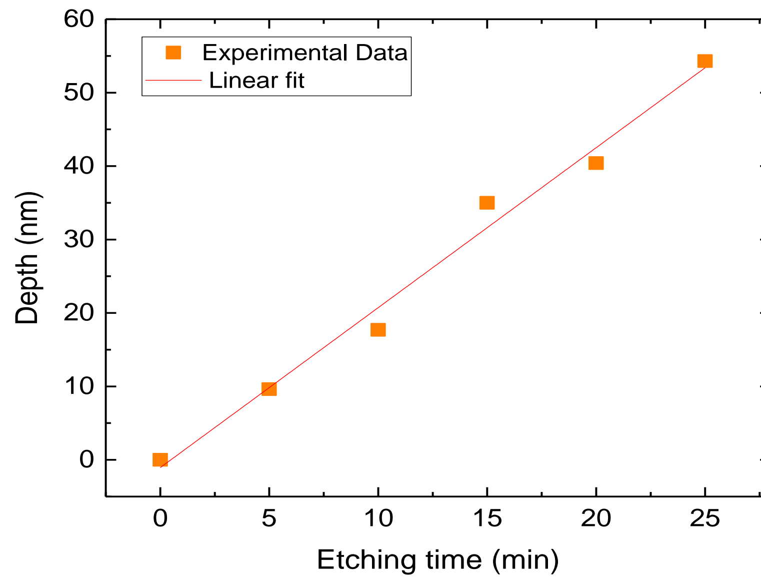

Figure 4. 14: Citric acid etching depth as a function of time.

The surface roughness data is analysed for the left, and right side of the trench top, and the trench bottom for all samples using both parallel and lateral slices to the trench geometry to investigate any symmetry bias. With respect to all samples, the results of the non-etched area (left and right sides) exhibit slightly more roughness than the previous pristine sample measured. A histogram of the non-etched (as a reference) sample and etched samples of 5min, 10min, 15min, 20min and 25min for trenches measured as vertical slices is shown in *Figure 4. 15*. Gaussian distributions of etched samples using citric acid are roughly identical in relation to the range of the RMS roughness values, with the exception of the 0 and 5 minute etched samples. Regarding the range of these samples investigated here, the measured RMS roughness varies between 1nm and 7nm and is approximately located in 3.5nm. However, the first sample (etched for 5 minutes) has greater roughness distribution and a wider range than the others. This is speculated to be due to some induction phase of the etch, and the origin of which is derived from a combination of the oxide on the surface and

possible residue of the resist after the developing process. This sample has a range of roughness between 3.5–10.5nm and a centroid that is approximately 7nm. Furthermore, the non-etched sample has significantly higher roughness than preceding samples with a 3.5-9.5nm range and centroid of virtually 7nm. An interesting indication which can be revealed, is that the citric acid etching process is generating minimal roughness and delivers decreased surface roughness.

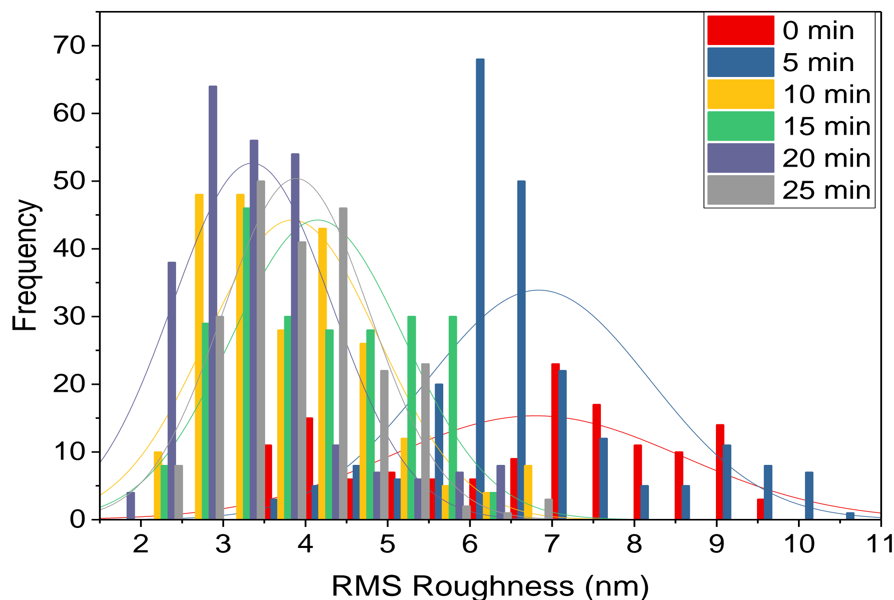

Figure 4. 15: Histogram for citric acid etched samples as a function of RMS Roughness in the vertical axis.

In terms of the horizontal axis slices for the trench areas, *Figure 4. 16* shows fitted Gaussian peaks to the distributions that are in general coincident to a first approximation in the location and peak range, except for those that fit the non-etched and 10- and 15-minute etched samples. The RMS roughness distribution range investigated in relation to the etched samples in 5, 20, 25 minutes, vary between only 1-6nm and the centroids are at approximately 3.8nm. The 15min etched sample has a marked narrower peak and also slightly shifted in the range of 3.7-6.5nm, whilst the peak centroid is very nearly 4.7nm. Additionally, the 10min etched sample has a wider range than previous samples, varying between 1.4-6.4nm and is located at 4.2nm. However, the non-etched sample reveals the widest distribution range which varies between 2-11.2nm, with the centroid at ~4.6nm.

The Gaussian distribution in *Figure 4. 16* indicates that the etched samples surfaces would appear to have RMS roughnesses which are lower in magnitude, and with a narrower range than the non-etched sample.

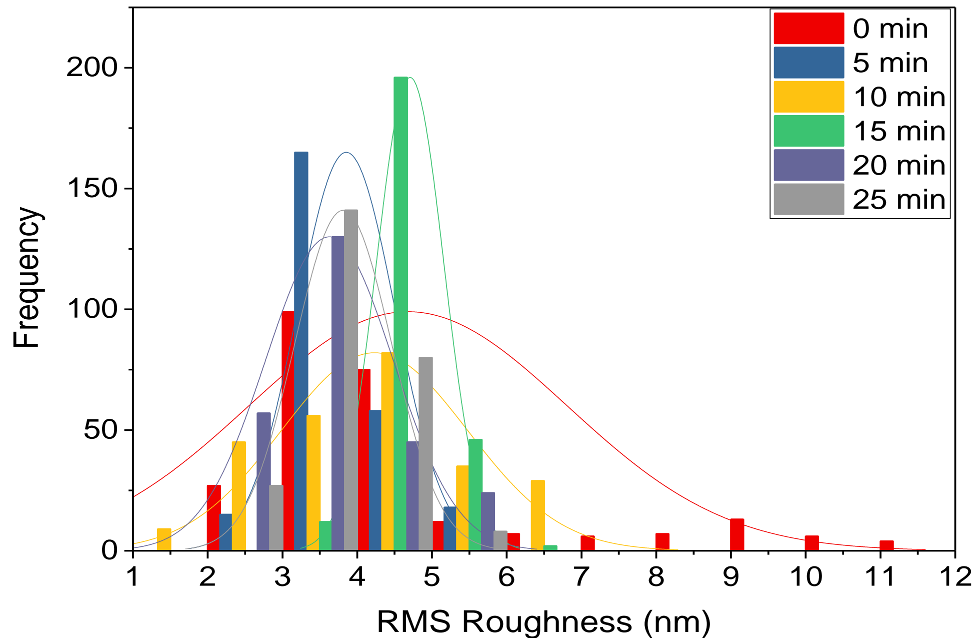

Figure 4. 16: Histogram for citric acid etched samples as a function of RMS Roughness in horizontal axis.

However, the RMS roughness can be seen to be rougher in the case of the vertical aligned slices, in contrast to the horizontal slices, due to the longer scale of roughness data which can be strongly dependent on the macro scale 'waviness' of the roughness. It should be noted that the frequency of the vertical slices is less than the horizontal slices, and so the absolute number of slices is fewer.

Given that the mean value represents the centroid of the Gaussian peak, *Figure 4. 17* explains the mean values of RMS roughness data in the vertical axis for etched samples using the citric acid. The error bars indicate the standard deviation of these data. Mean values of most of these samples are in the range of 3.5-4.5nm which is a difference of only 1nm, which is not significant compared to the magnitude of the uncertainty. However, this is not the case with regards to the non-etched and first etched samples (10nm depth), that have rougher surfaces for reasons speculated previously, related to the surface oxide and photoresist residue. Similarly, the citric

acid etching process provides considerable RMS roughness mean values which are less than the pristine surface.

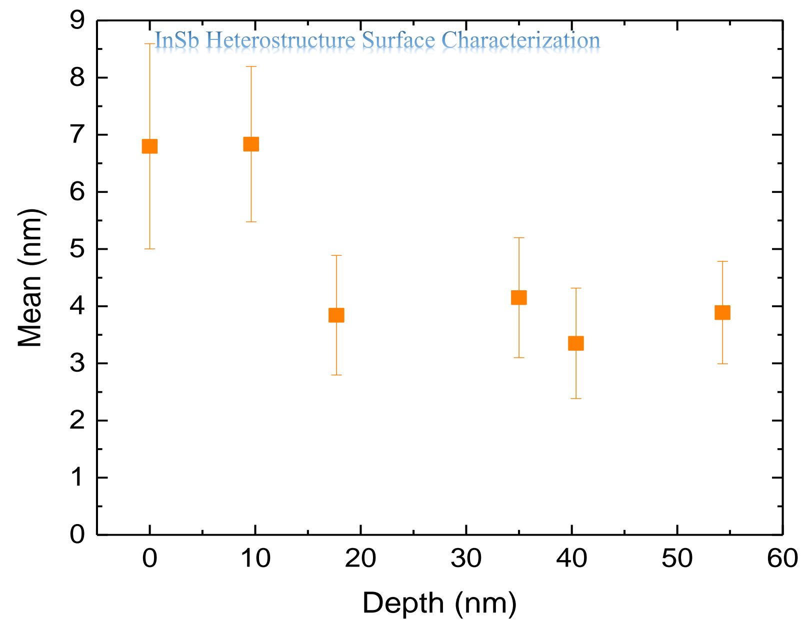

Figure 4. 17: Mean and standard deviation bars for Citric acid etched samples in the vertical axis as a function of etching depth.

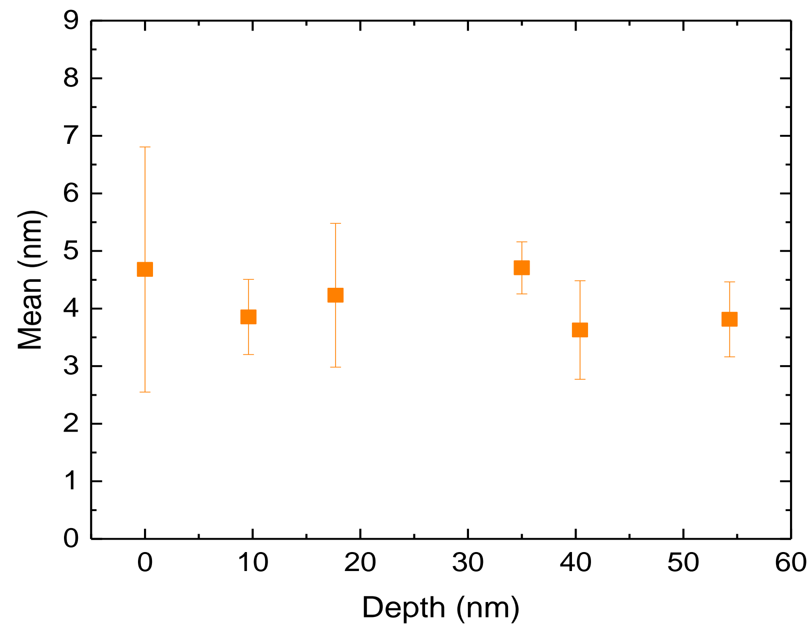

Figure 4. 18: Mean and standard deviation bars for Citric acid etched samples in the horizontal axis as a function of etching depth.

The mean values of the RMS roughness in the horizontal slices presented in *Figure 4. 18* display a range of 3.8-4.7nm, which is only a narrow difference of 0.9nm for all of the samples. These show low mean values and it appears that the etched samples mean values are less than the non-etched sample. Furthermore, the short (horizontally) slices of roughness reduce the difference value among them in comparison to the long (verical) slices.

The FWHM can be deduced from the data and is related to the sample standard deviation values as outlined in Equation (4 - 3). The FWHM values of the RMS roughness in the vertical slices is shown in *Figure 4. 19*, as a function of depth of trench which is explain the symmetry of Gaussian distributions of peaks. The graph shows that there is a narrowing in FWHM as a function of etch depth, starting from 4.2nm for the non-etched surface and drops steadily over the studied depth range, with the etching time reaching its lowest value at 2nm. Furthermore, the least squares linear fit shown in *Figure 4. 19* indicates the gradient of the FWHM values as a function of etching depth (which is similar to time). This therefore suggests that the Gaussian peaks will be thinner, and physically, the majority of RMS roughness ranges is modified into a smaller range. Specifically, this is an indication that the etching process is uniform and induces a smoother surface with time and depth.

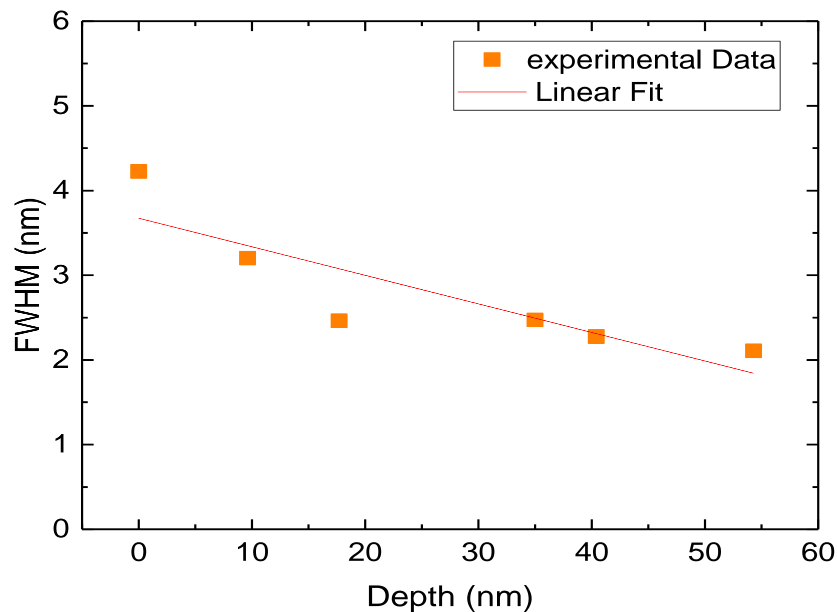

Figure 4. 19: Full Width at Half maximum value for citric acid etched samples in the vertical axis as a function of etching depth.

The FWHM values of RMS roughness shown in *Figure 4. 20*, presenting a fluctuation of values in the horizontal slices, comes predominantly from the effect of the 'waviness' of the surface, as shown in *Figure 4. 13* and explained in *Figure 4. 8*. Samples; 5 and 15 minutes etching that have less waviness induce a narrow range in relation to RMS roughness and therefore low value of FWHM for these two samples. However, the FWHM values and the linear fit show a gradient against the etching depth and time similar to the trend in the vertical case.

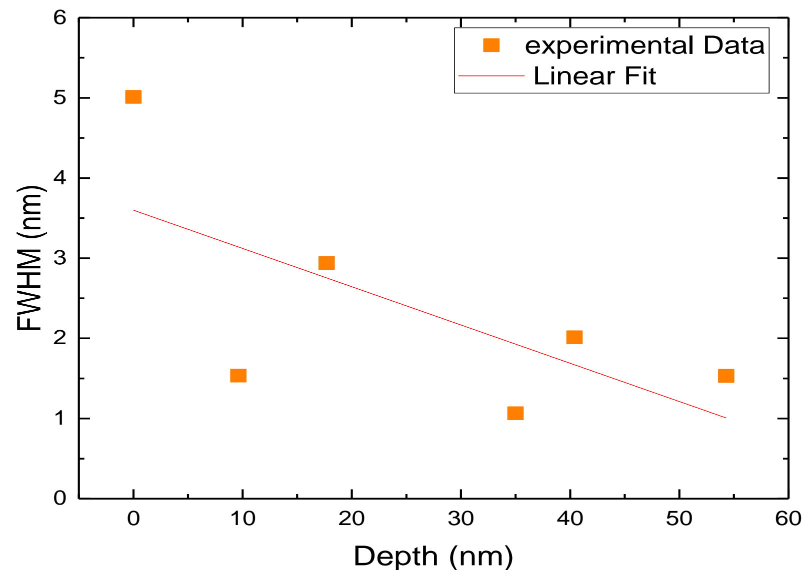

Figure 4. 20: Full Width at Half maximum value for citric acid etched samples in the horizontal axis as a function of etching depth.

The RMS roughness can be calculated and studied not only as slices, but also as areas. The RMS roughness of the surface area represents the combined roughness of the vertical and horizontal slices in the square area. *Figure 4. 21* shows the relationship between the RMS roughness in a square area and the area size. The RMS roughness has been analysed by taking a 1μm^2 square which is then shifted a small distance and the roughness recalculated repeatedly for the entire area. This process was repeated for 2 to 10μm^2 similarly to induce a trend of roughness as a function of template square area size. The RMS roughness is seen to increase proportionally with the area size due to the increasing scale of measurement on the surface which is related to the waviness of the surface roughness can be physically a valley and/or mountain. Likewise, the RMS roughness for all sample trenches using a small area of approximately 1μm^2 is roughly equal at just over 1nm.

The roughness values of different samples start to diverge against the area size when increasing the sample area size. For instance, the 5- and 10-minute etched samples start emerging in 7.5µm^2 size to the end. Whereas, the 15-minute etched sample exhibits much greater roughness in contrast to the etched samples. The 25-minute etched sample displays less roughness than the previous ones (0-15 minute samples). The most interesting roughness profiles are the 20-minute etched sample which exhibits the lowest roughness, whereas, the highest roughness is for the non-etched sample surface. These results correspond well to the mean values observed in the horizontal and vertical slice analysis.

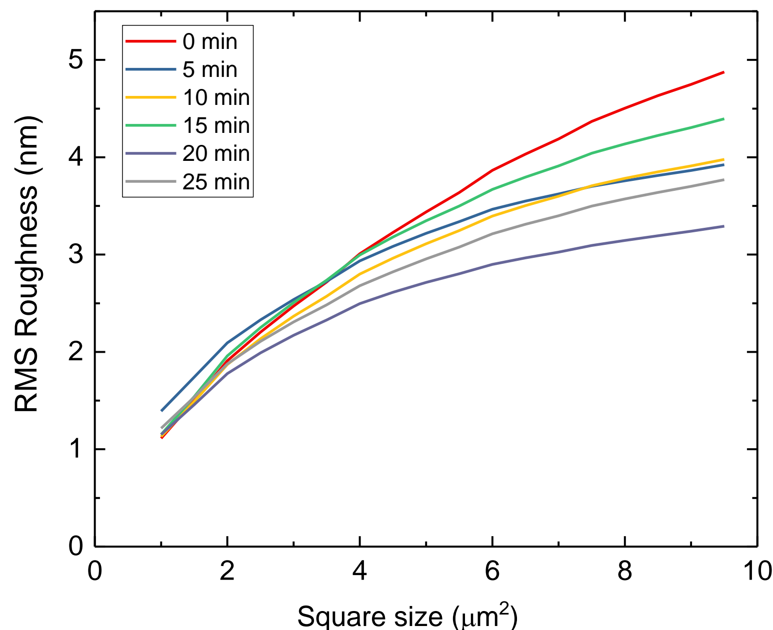

Figure 4. 21: RMS Roughness as a function of square size for the citric acid etched samples.

The full roughness of the trench samples can be analysed to cover the entire area with an equal area size of 700µm^2 for all the samples. *Figure 4. 22* depicts RMS roughness values of the entire area of the trench samples that are clearly decreasing with regards to time and depth of etching.

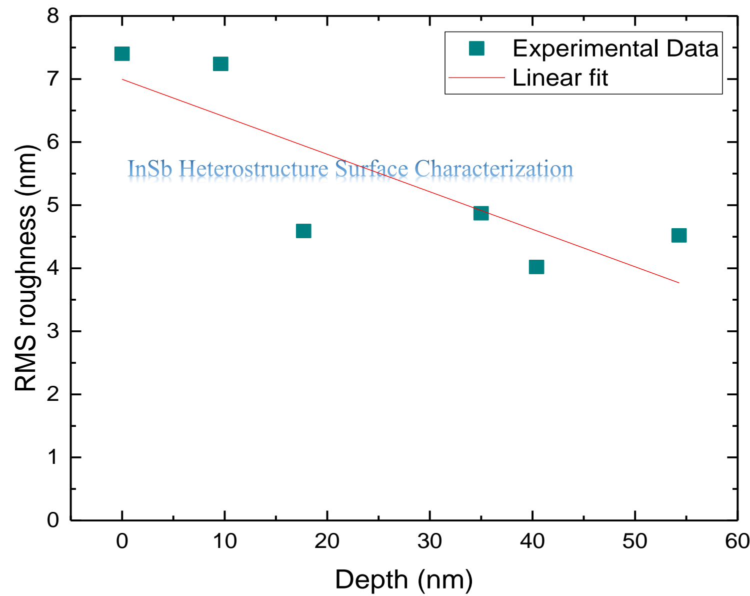

Figure 4. 22: RMS roughness for full trench area by Citric acid versus depth.

These results interestingly correspond to the mean and FWHM in the analysis of the vertical slice trends. The Citric acid etching technique results in less roughness than the pristine surface which is helping the Ohmic contact by removing the oxide layer and optimizing the metal-semiconductor contact, that leads to less contact resistance and modifies the device performance.

4.3.3 Ion Beam Milling for the AlInSb/InSb wafer

Dry etching technique is widely employed in III-V compound semiconductor technology for Ohmic contact [18], device isolation and several publications for InSb have been reported [19]–[21]. Eroding the semiconductor surface by argon ion beam bombardment has many advantages; remove defects and minimising surface damage, as well as, electrically, produce In-rich that create n-type layer [22]–[24] as reported by Jones and his group. IBM process has been used to prepare (etch) the top cap surface of the wafer by argon bombardment toward the quantum well. This has been done under high-vacuum (which is about 7.0×10^{-7} mbar approximately) with a discharge voltage of 200 V and discharge current of 1.0 A. The IBM technique removes oxidised surface before the deposition of metal that described in Section 3.3.2. By using the similar sample fabrication process as in the citric acid etching;

using S1805 photoresist, the Ohmic mask and photolithography technique to open windows for ion interaction. The etched sample can be presented as a three-dimensional topography of the AlInSb/InSb wafer surface after the IBM etching process. This is shown for 1, 2, 3 and 4 minute etches, in *Figure 4. 23*. This 3D image shows the trench depth and non-etched area to a scale of 60×30μm^2 in x and y for all of the samples studied. The size is kept the same in order to ensure consistent analysis, similarly the z axes scale.

Trench depth is calculated for the IBM samples using the same as method used to calculate the citric acid etch depth.

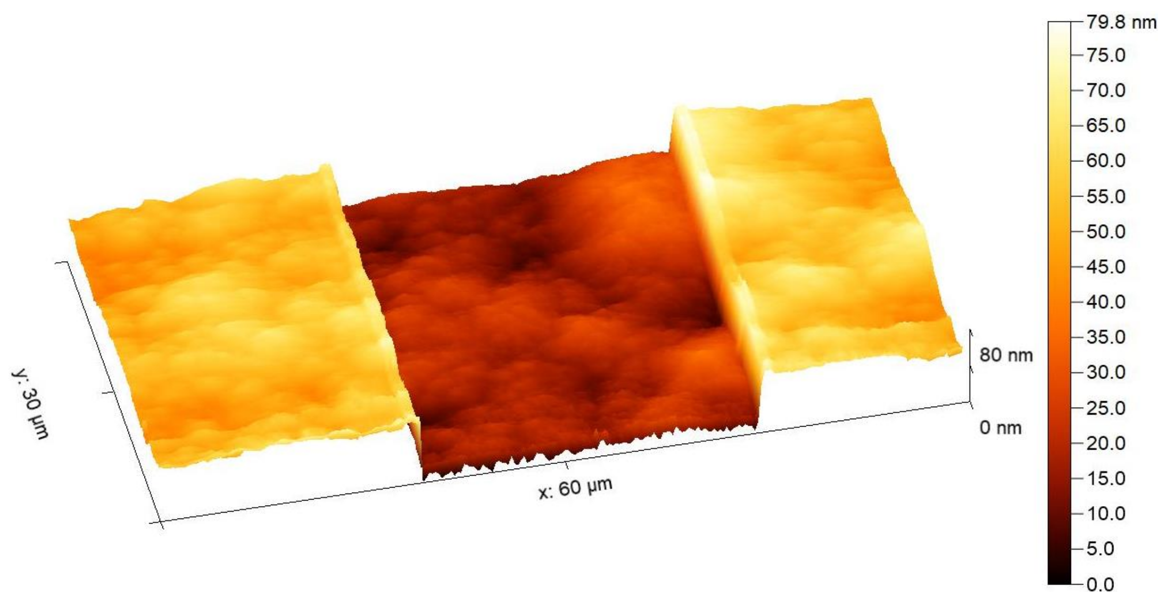

Figure 4. 23: AFM image in three-dimensional profile for the etched AlInSb/InSb wafer by means of IBM technique.

Figure 4. 24 illustrates that there has been a gradual increase in the trench depth as a function of etching time due to the increasing ion interaction (removal) with the surface material of the wafer with time. The experimental data related to trench depth is shown in *Figure 4. 23* demonstrating a linear fit for these samples. The gradient enables the rate of etching to be deduced which is approximately 7.7nm/min.

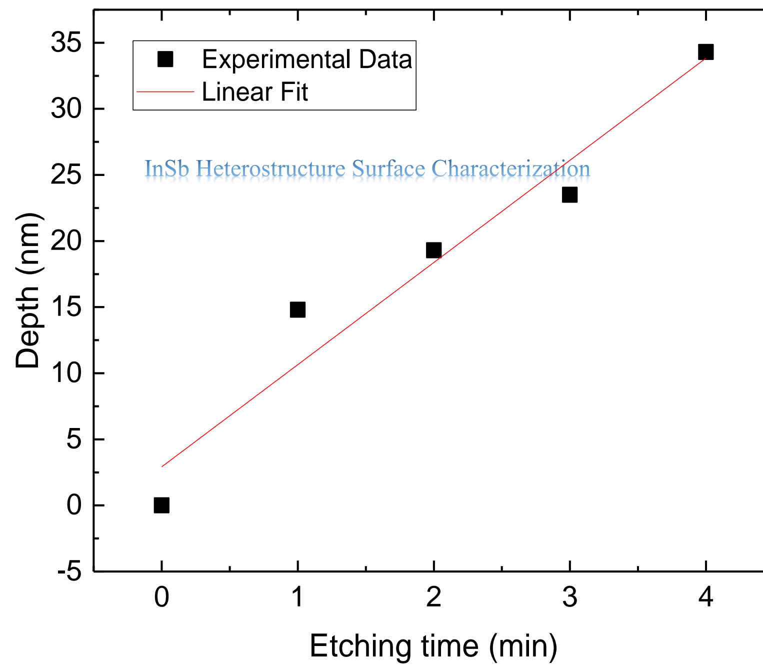

Figure 4. 24: Ion Beam Etching depth as a function of time.

The surface roughness of the etched area using IBM can be measured in the vertical and horizontal slices and presented statistically by Gaussian histograms as before. Non-etched (0 minute) and etched samples (0, 1, 2, 3 and 4 minutes) are presented in *Figure 4. 25*. Gaussian distributions for these samples are roughly identical in relation to the range of RMS roughnesses and locations, except the non-etched sample and the sample etched for 4 minutes. The range of RMS roughness of the etched samples varies between 1 and 7nm. The centroid is approximately 3.5 to 4nm. Moreover, the 4-minute etched sample has a slightly rougher and wider range in contrast to the etched samples, which has a range between 3–8.5nm and a peak centroid of 4.5nm. The non-etched sample has a roughness range of 2-6.5nm and a centroid value of 4.5nm.

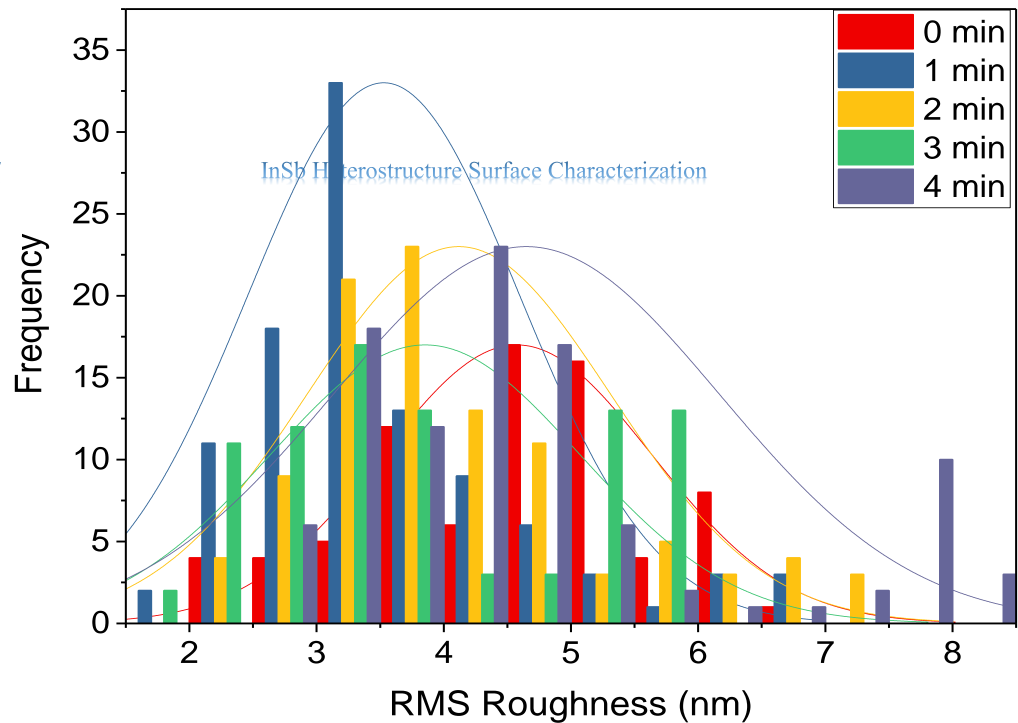

Figure 4. 25: Histogram for IBM etched samples as a function of RMS roughness in the vertical axis.

Gaussian distribution peaks in the horizontal slice axis can be presented for the trench areas in *Figure 4. 26*. Both samples (1 and 3 minutes) peak roughness are relatively similar in the centroid position and range of roughness. Regarding the range of samples investigated here, the measured RMS roughness varies between 2 and 5.5nm and is located at approximately 3.7nm. Additionally, the 2-minute etched sample has a slightly shifted distribution range which is approximately 2 to 7.2nm and has a centroid about 4.2nm. The non-etched and 4-minute etched samples have wider peaks roughness, mostly identical distribution ranges which is approximately 2 to 9.5nm and 5nm centroid. However, the maximum centroid difference is only roughly 1.3nm.

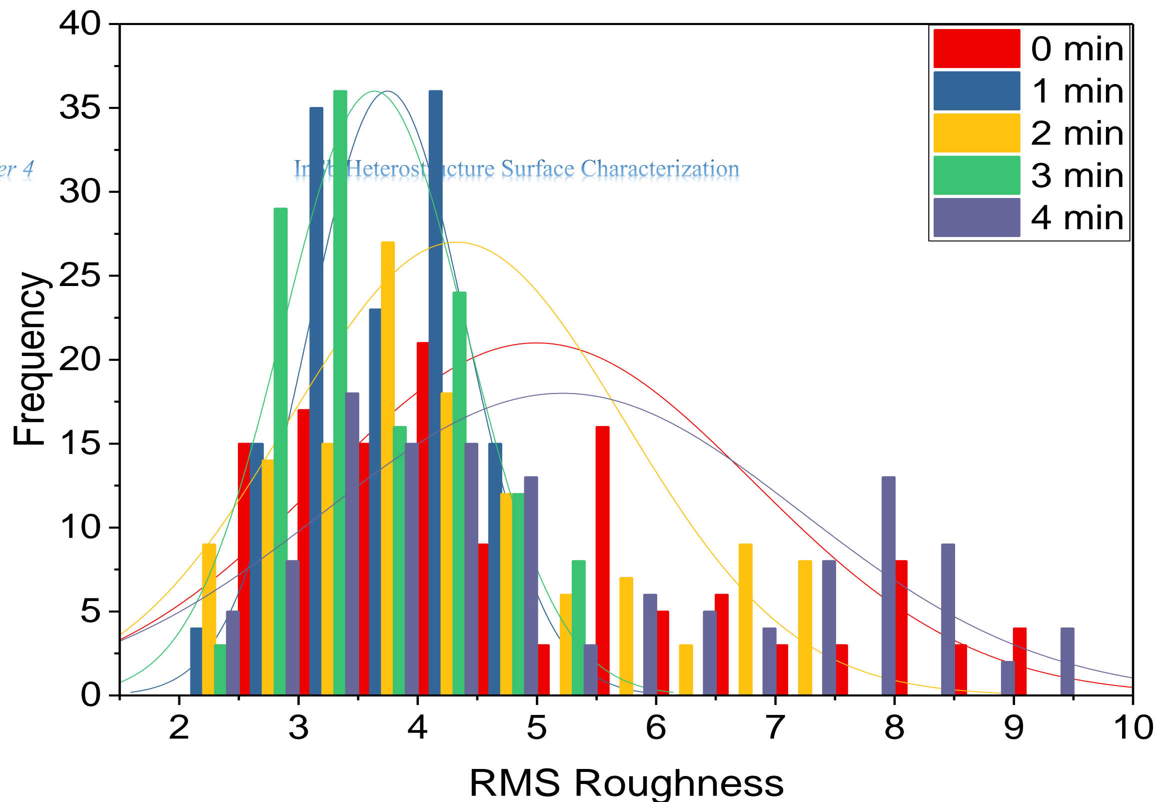

Figure 4. 26: Histogram for IBM etched samples as a function of RMS roughness in the horizontal axis.

Both the vertical and horizontal cases indicate that the IBM etching process seems to provide a lesser and more consistent surface roughness for most of the samples presented. The mean values of the RMS roughness in the vertical axis slices can be illustrated as a function of the depth of etching to study the effect of the wafer structure, surface oxide and/or dopant. *Figure 4. 27* illustrates the mean values for 0-4 minutes and does not exhibit a clear trend when considering the standard deviation values (The error bars represent the standard deviation value). However, the lowest values are for the etched samples of 1,2 and 3 minutes that have depths ranging from 14.8-23.5nm compared to the pristine and 4-minutes etching samples. Therefore, surface roughness of these samples mean values are less than the pristine surface (with the exception of the 4-minute sample (34.3nm depth)). The maximum difference in mean value is in the range of 1.1nm meaning that these results are extremely consistent.

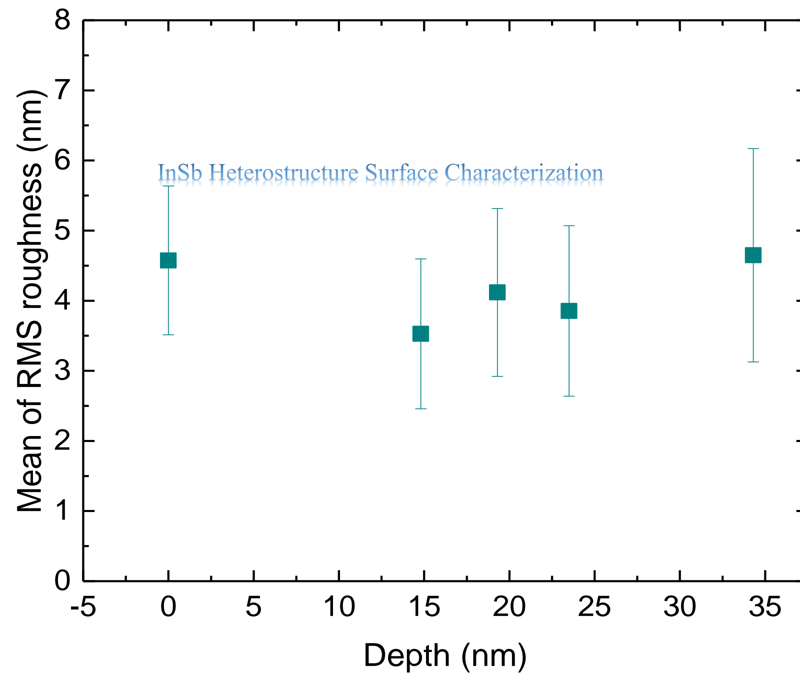

Figure 4. 27: Mean and standard deviation bars for IBM etched samples in the vertical axis as a function of etching depth.

In terms of the horizontal axis, the mean values of RMS roughness are illustrated as a function of the depth of the wafer etching in *Figure 4. 28*. Once again, the error bars represent the standard deviation. The graph reveals that there is no clear trend regarding the mean values against the depth, which is a similar conclusion to the vertical case. The mean values range between 3.6 and 5.2nm with a maximum difference in means of about 1.6nm. It should be noted that once again the mean values for the 1, 2 and 3 minute etches have an etch depth range of 14.8-23.5 nm and are lower than the pristine and 4-minute etched sample. This is consistent with the vertical slice case.

Both the vertical and horizontal slice analysis indicates that the IBM etching process provides roughly consistent surface roughness, which is actually lower than the pristine sample for the majority of samples studied.

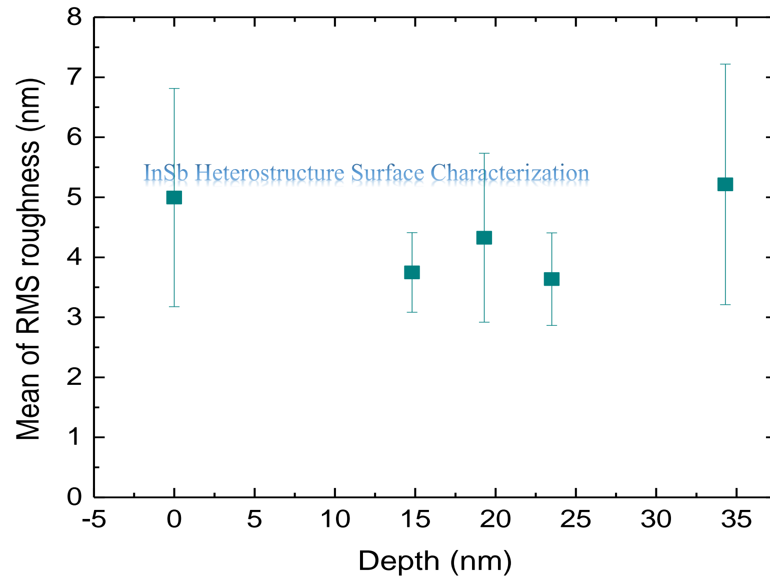

Figure 4. 28: Mean and standard deviation bars for IBM etched samples in the horizontal axis as a function of etching depth.

The FWHM values related to the RMS roughness in the vertical axis slices are presented in *Figure 4. 29*, as a function of trench depth. The graph shows that there has been a slight rise in FWHM over the studied depth range and etching time. However, the maximum variation between the zero and 35nm depth (4 minutes etching) is only 1.1nm on the scale of range.

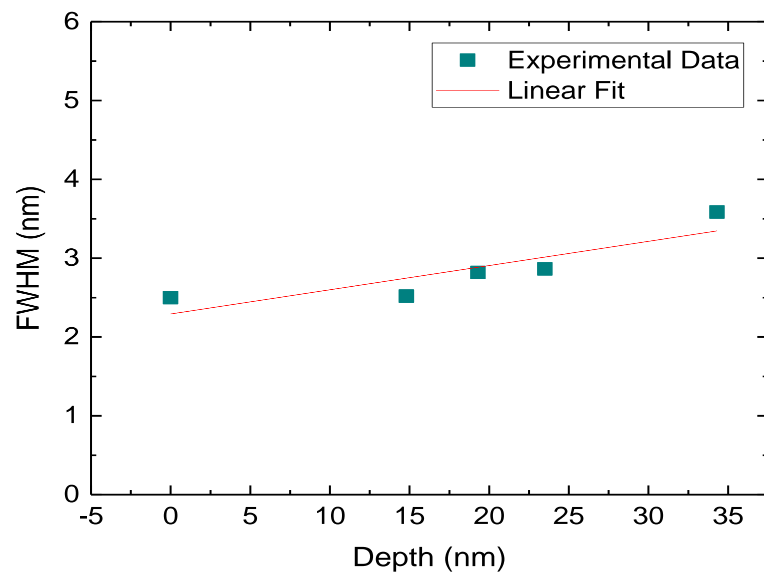

Figure 4. 29: Full Width at Half maximum value for IBM etched samples in the vertical axis as a function of etching depth.

Furthermore, the linear fit of the gradient of the FWHM value as a function of etching depth reveals the inverse trend compared to the citric acid in the vertical case. This suggests that the Gaussian peaks will be slightly wider, which was not expected as was the case with the citric acid case. However, this is only evident in sample (4-minute etching) via a depth of 34.3nm.

Conversely, the FWHM values of roughness in the horizontal slices are shown in *Figure 4. 30*. The graph illustrates that there is a relatively high-fluctuation as a function of depth and time etching. This can be as a result of the waviness effect of the surface as shown in *Figure 4. 13*, especially for the non-etched and etched sample for 4-minutes, that high-waviness induces a wide range of RMS roughness and therefore, FWHM of high-value for these samples.

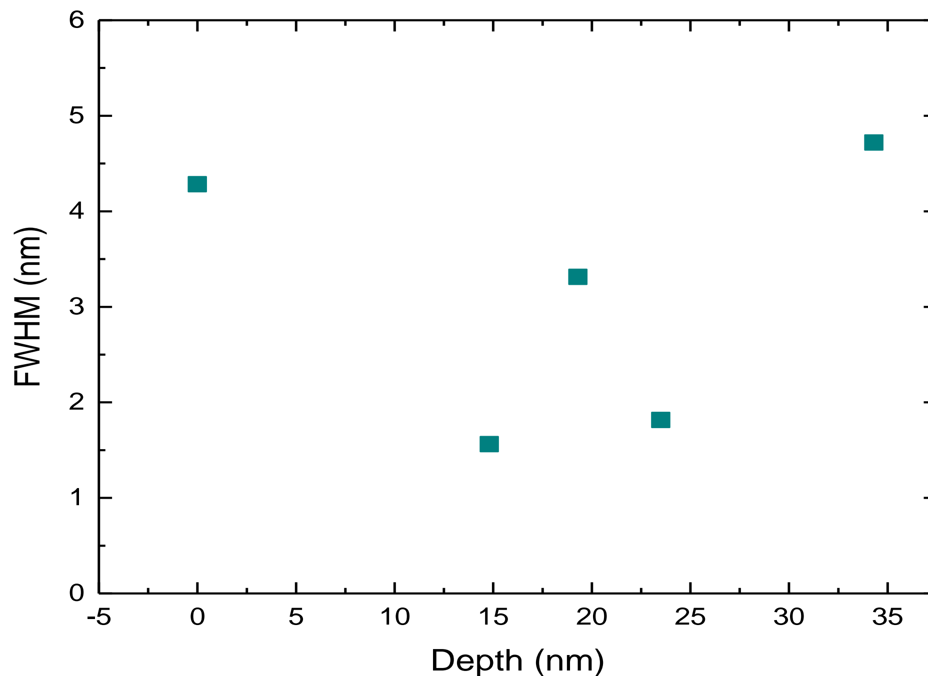

Figure 4. 30: Full Width at Half maximum value for IBM etched samples in the horizontal axis as a function of etching depth.

However, the FWHM values demonstrate an unclear relationship concerning the depth and etching. Nevertheless, the interesting point is that the FWHM values for the etched samples are less than the non-etched sample, (with the exception of the 4-minute etched sample).

The RMS roughness using a square area of all the IBM sample trenches has been calculated to be the same as in the citric acid case. *Figure 4. 31* reveals the relationship between the RMS roughness values and the square size. The RMS roughness values of 1µm² square areas are roughly equal, which is also virtually equal to the citric acid samples. However, the roughness values start to diverge with increasing area size (beyond 4µm², towards the end of the area size (9.5µm²)). The non-etched sample exhibits the highest values of roughness, approximately 4.8nm for analysis on a square size of 9.5µm². The samples that are 1 and 3 minutes etched reveal the lowest roughness and are practically similar, (at approximately 3.2 and 3.3nm respectively using analysis from the maximum square size). The maximum difference in roughness (at maximum analysis size) is of the order of 1.6nm.

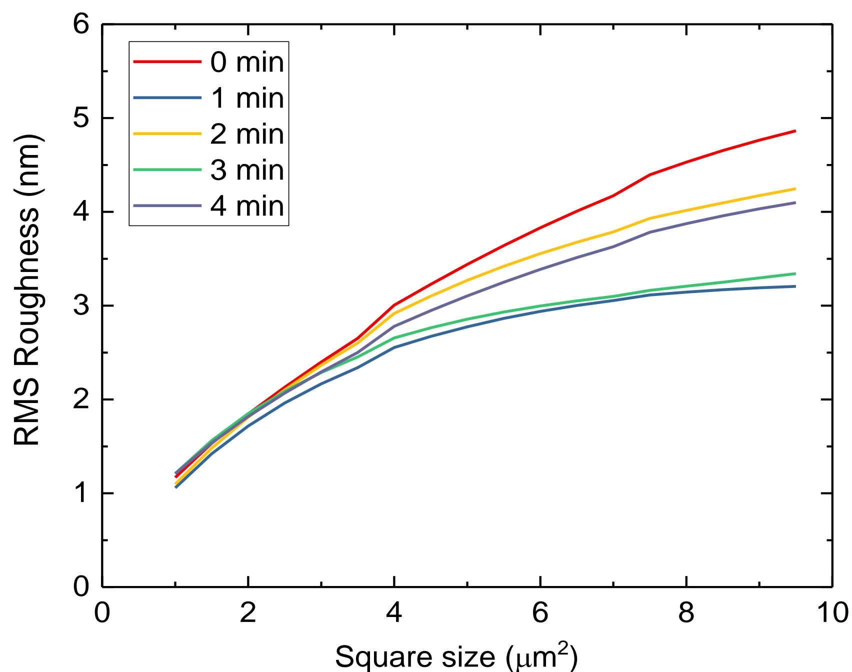

Figure 4. 31: Square area average RMS roughness for only IBM etched areas.

The RMS roughness of the samples trench can be measured for the entire area that has been analysed with normalised area size for all samples, which is roughly 700µm² and illustrated in *Figure 4. 32*. This graph reveals that there is a remarkable narrow in RMS roughness values as a function of etch depth/time, which is indicated by the linear fit applied to the graph. These results interestingly have a similar trend to the mean values.

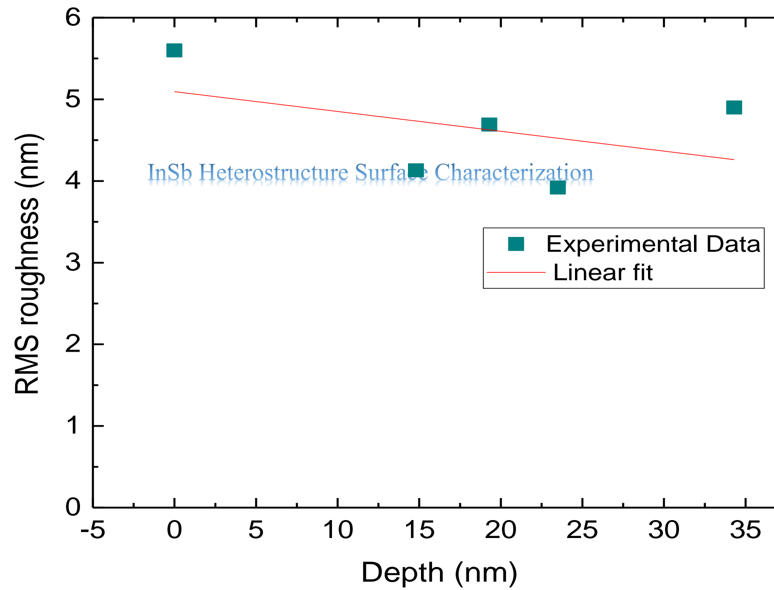

Figure 4. 32: RMS roughness for full trench area by IBM versus depth.

4.4 Conclusion

This chapter has presented a detailed surface oxide of pristine AlInSb/InSb wafer surface and roughness analyses for pristine wafer surfaces and etched surfaces by means of citric acid wet etching and argon beam milling. The XPS proves the existence of surface oxide with thin thickness that need to remove to improve dive performance. These two techniques have removed the oxide and modified the Ohmic contact in terms of resistivity which studied and substantiation in chapter five. Etch depths characterised are critical for Ohmic contact and gate technologies in this material. The RMS surface roughness analysis has been described with respect to two different orientations of zero and 90° degree AFM tip scan directions which proof of systematic in Gaussian distributions of RMS roughness. Furthermore, from this study it has been observed that the RMS roughness values vary with square area starting from approximately 1nm to less than 6nm, with a saturation value analysed to be with an approximately 30µm^2 square area. There is high-consistency for the trends in RMS roughness analysis against square size and furthermore, mean and median values are a substantiation of directions consistency for RMS roughness. Therefore, it can be concluded that the effect of AFM tip orientation or the crystal structure on the surface roughness measurements is negligible.

The most significant results were demonstrated by the citric acid etching, finding that the etching depth (proportion with time) has a rate of approximately 2.2 nm/min. Whereas, IBM etch in rate of approximately 7.7nm/min. This rapid etching is as a result of the high energetic ion that interacts with material. Therefore, wet chemical etching is less invasive compared to the dry etching [25]. The etched samples by both techniques that were studied here in general showed less RMS roughness than the pristine wafer surface. This implies that the etching process interacts reasonably uniformly with this material. This is also confirmed by the RMS roughness peak FWHM, mean, square size and full area roughness values. It is important to state that the effect of the surface oxide and residue of resist on the first etched sample depth value and surface roughness is clear, that slows down the etching acting as a barrier layer [17].

It should be noted that there are some fluctuations in values in the case of the IBM samples that are different to the citric acid results. This can be attributed to the nature of interaction of the applied ion and acid, as well as, the velocity of etching. Consequently, the high ion energy can generate unpredicted or slightly rougher roughness. Furthermore, it is shown that using citric acid and IBM techniques are modifying the roughness which not affecting the Ohmic contacts resistance and therefore, does not affect the performance of the quantum device.

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Chapter 5

AlInSb/InSb QW: Contact Improvement Using the Transmission Line Model (TLM) measurement technique

5.1 Introduction

A common challenge in developing technology in new materials is how to modify the surface or interface layer properties in a controlled manner to achieve successful Ohmic or desirable rectifying behaviour. As the device size is reduced, the surface properties of InSb increasingly affect the performance of the device. One of the major challenges with InSb surface bonds, and in general semiconductor surfaces, is their uncontrolled reaction with the environment. In particular, InSb surfaces can become oxidised spontaneously, which is often driven by humidity. It is therefore difficult to avoid the formation of surface native oxides on InSb based material, particularly surfaces based around the alloy AlInSb. Consequently, the presence of this interfacial oxide layer as well as electronic defects at the interface alters the energy band diagram. These two factors can effectively influence the performance of the device by obstructing the electron transport [1]. Modification of the InSb crystal surface has been investigated here to try to enhance the operation of future devices. In particular developing a low resistance Ohmic contact is an essential part in the development of any high-performance electronic device and reliably measuring the contact resistivity is a high-priority [2][3].

The AlInSb/InSb wafers studied here have been characterised by XPS and EDX techniques, (presented in Chapters 3 and 4 respectively). To avoid AlInSb–oxide

interface structures, this chapter presents an approach where the AlInSb surface is etched/treated using two techniques: wet etch (citric acid ($C_6H_8O_7$)) and dry (Argon ion beam milling), prior to for metal deposition [4]–[9]. The transmission line model (TLM) that was proposed by Shockley is the most commonly used technique to investigate Ohmic contact performance [10].

In this study, TLM devices are fabricated by photolithography using a Cardiff TLM mask design (for further details, see Chapter 3). Ohmic contacts are etched and deposited with Ti/Au, with thicknesses 10 and 90 nm, respectively.

5.2 Total Resistance

The total resistance has been measured for linear TLM devices over a range of distances between the contact pads. Citric acid sample etching time and subsequent depths are depicted in *Figure 5. 1*, and listed in Table 5.1. Ion beam milling times and subsequent depths are depicted in *Figure 5.* ***2*** and listed in Table 5.2. These depictions are shown with the QW (blue layer) and the δ-doping layer (green dots) position relative to the etched surface. *Figure 5. 3* shows a SEM image of a linear TLM (LTLM) device design after MESA etching and fine wire bonding.

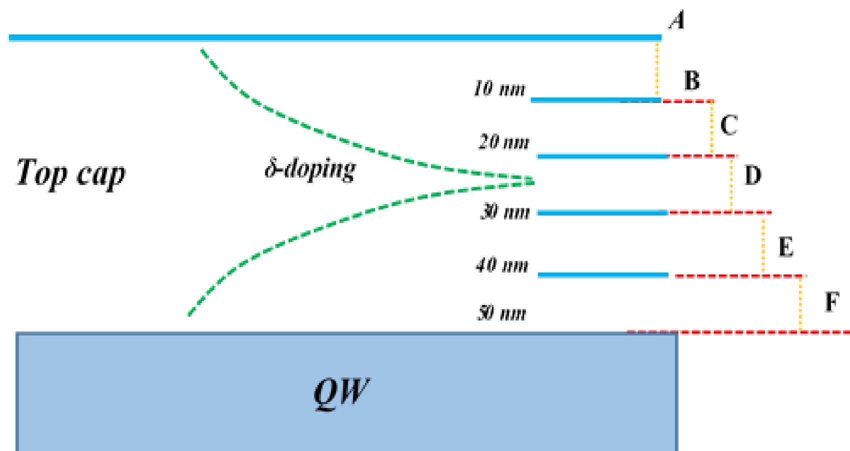

Figure 5. 1: AlInSb/ InSb wafer etching depth using citric acid for samples A–F.

Table 5.1: Citric acid samples with etching time and etching depth.

Sample number	**Etching time (minute)**	**Etching depth (nm)**
A	0	0
B	5	10
C	10	20
D	15	30
E	20	40
F	25	50

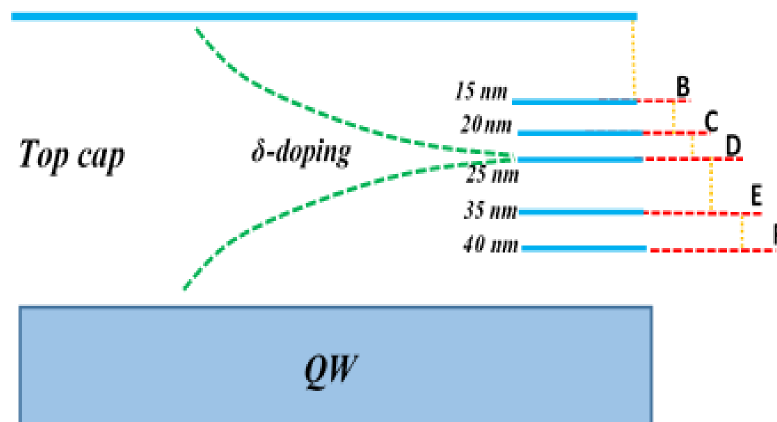

Figure 5. 2: AlInSb/ InSb wafer etching depth using IBM for samples A–F.

Table 5.2: Ion beam milling samples with etching time and etching depth

Sample number	Etching time (minute)	Etching depth (nm)
A	0	0
B	1	15
C	2	20
D	3	25
E	4	35
F	5	39

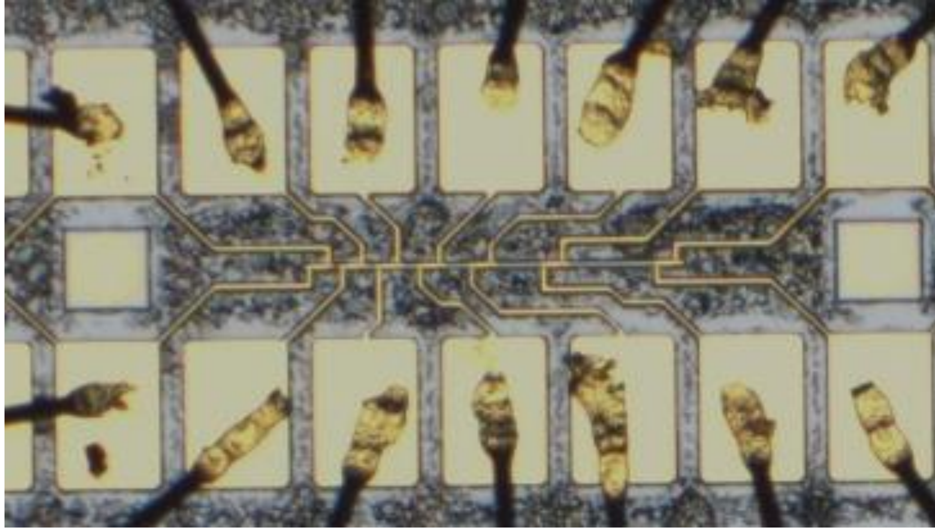

Figure 5. 3: LTLM device with gold wires connected to FEED pads measuring resistance for 2–64 µm distances.

Four terminal I-V measurements are taken over a range of temperatures. An example of raw I-V-T data from a ~2.5µm etch (MESA) depth LTLM is presented in *Figure 5. 4*. Both types of etched samples are measured at room and low temperatures by applying voltage and measuring current. The linear I–V characteristic indicates that both contacts form good Ohmics (metal/semiconductor).

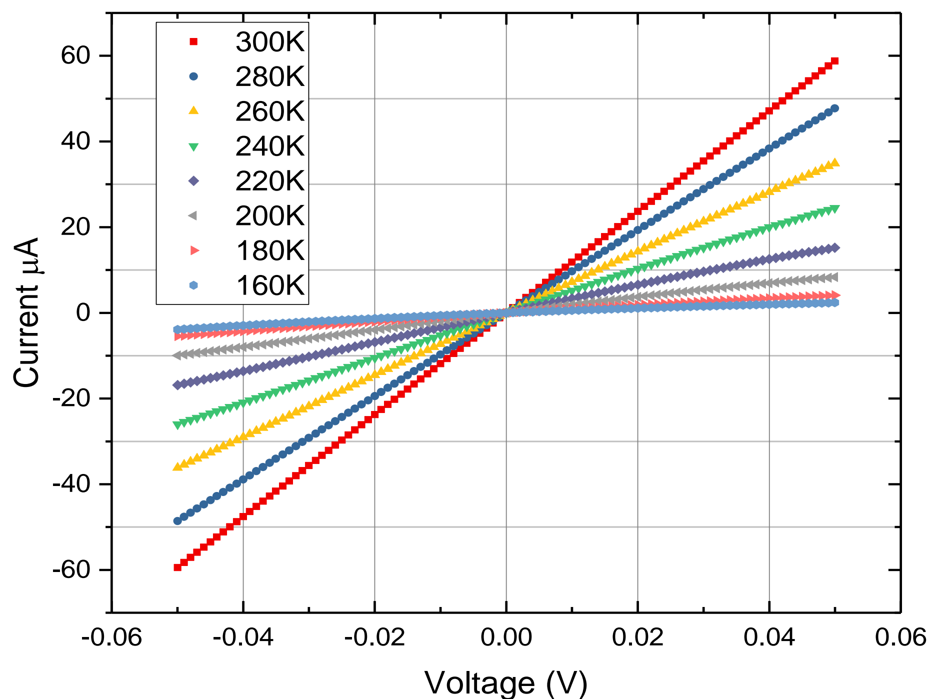

Figure 5. 4: I–V characteristics of LTLM contacts for InSb 2DEG over a range of temperatures.

The total resistances are deduced from linear fits to the I-V curves at low voltage for the citric and IBM samples, which are extracted as a function of the distance between contacts, as shown in *Figure 5. **5*** and *Figure 5. **6***, respectively. It is reasonably clear that the etching process decreases the total resistance significantly when compared to unetched contacts in Sample A (zero depth) in both cases (i.e. citric and IBM). Interestingly, the lowest resistance has been achieved for Sample B (relatively shallow 10nm depth), which decreased 86% on average for all contact separations in the case of citric acid when compared to the untreated Sample A. Similarly, in the case of IBM, Sample B's (relatively shallow 15nm depth) resistance decreased about 89% on average for all contact separations when compared to Sample A. This most likely happens because, as mentioned earlier, native oxides are formed on the AlInSb/InSb surface even during very short exposure to air, within 80 seconds for the first monolayer and ~20 minutes for 3nm [11]. This tends to inhibit the formation of good Ohmic contacts [12] in the case of the untreated samples.

The sequence of citric acid and IBM samples resistances is essentially identical because Sample B has lower resistance for all contacts separations—in the range of 3–9KΩ and 3.9–10.4 KΩ, respectively—then sample C, which has higher resistance. Whereas, Samples E and F are almost in the same range of resistances and higher than Sample C. Sample D has the highest resistance among the etched samples. Finally, Sample A (non-etched sample) has the highest resistance in both cases (citric and IBM), in the range of 30–53KΩ and 45.6–70.5 KΩ, respectively.

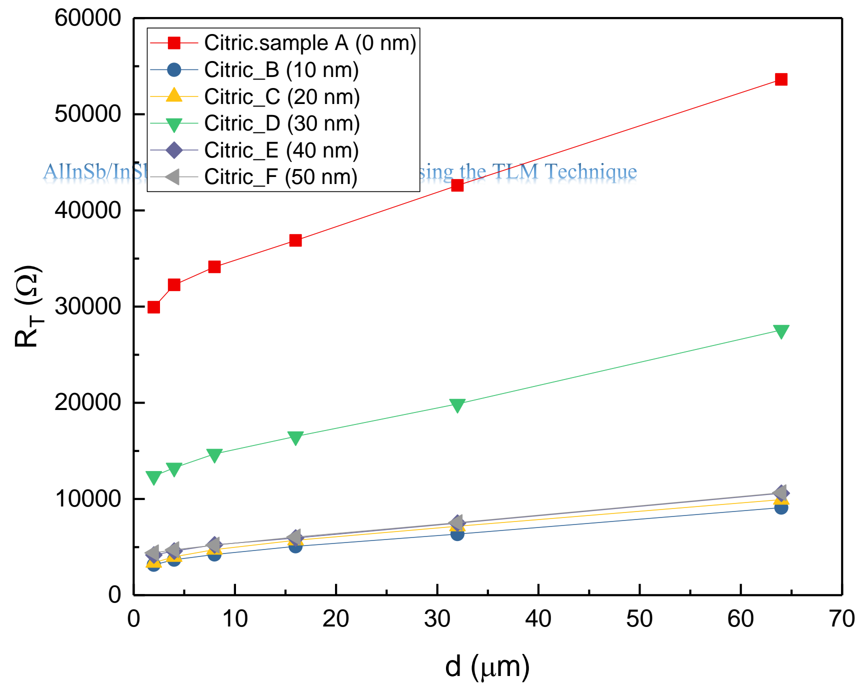

Figure 5. 5: Total resistance of contacts of LTLM device versus distance with different citric etching depths at room temperature using SF1258 wafer.

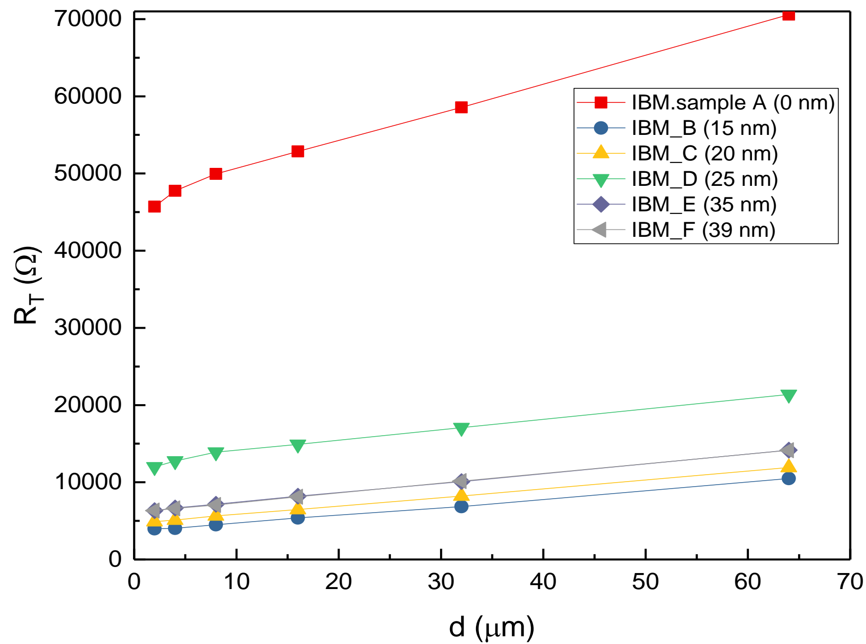

Figure 5. 6: Total resistance of contacts of LTLM device versus distance with different IBM etching depths at room temperature using SF1251 wafer.

A bending of total resistance curves occurs at short contact separations which comes from essentially lower resistances than the fit line. This phenomenon is attributed to the leakage current at the top cap layer, which contributes to the current flow and results in lower resistance. This is confirmed by Hall bar measurements, which show that there are two carriers within the top cap (the QW and some other unidentified carrier which is either attributed to the second sub-band of the QW or charge remaining within the delta doped layer – this is dependent on design). This is shown in *Figure 5. 7*. The current flow in two conducting layers has been investigated intensively by Look et al using the TLM technique [13][14] and by Ando et al [15]. Furthermore, there is potential for leakage current on the top of the surface when Sb is oxidised and then leaves the In, which can behave as a (albeit thin) metal conductor [16]. However, at low temperatures, the resistance for the top cap layer is much higher than the QW. This happens because the electron scattering on the top cap AlInSb and at the doping layer can dominate at low temperatures, and also because of the low electron activation energy [17].

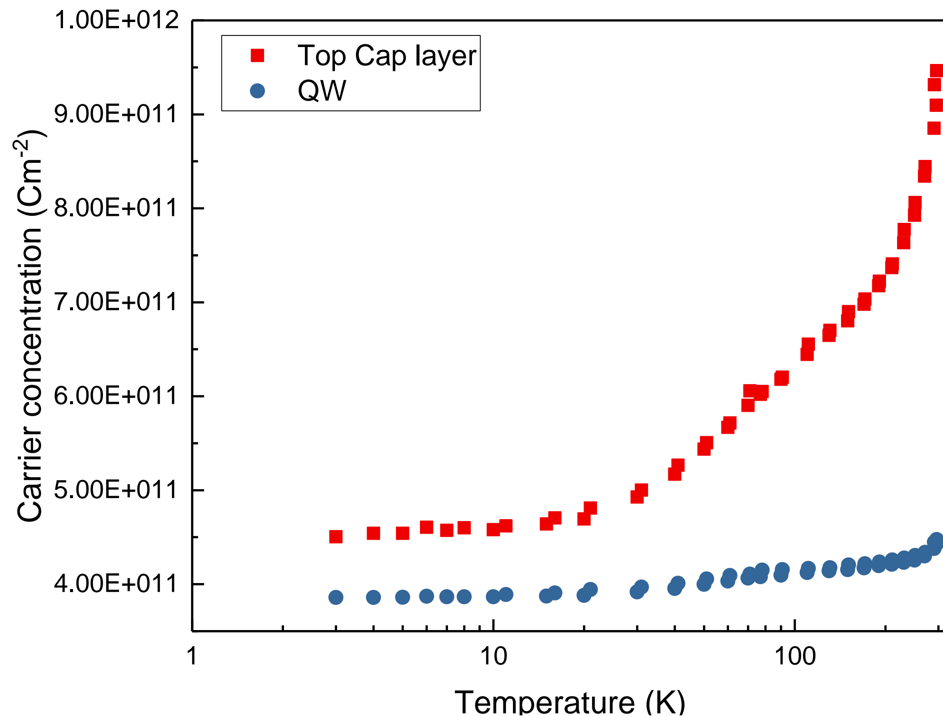

Figure 5. 7: Carrier concentration in the top cap layer and QW of AlInSb/InSb wafer, measured by the Hall technique using bar device in ratio 1/5 dimension.

5.3 Temperature Dependence of the Contact Resistivity

The metal-semiconductor contact can be deduced by assuming that both contacts are identical, and both have linear I-V characteristics. The contact resistance for each sample can extrapolated from the total resistance curve intercept with the Y axis; as shown theoretically in *Figure 5.* ***8*** and measured experimentally by *Figure 5.* ***5*** and *Figure 5.* ***6***. Similarly, the value of the contact resistance for each temperature for citric and IBM are extracted and calculated. The contact resistivity [18] is then given by

$$\rho_c = R_c \times L \times W \qquad 5\text{-}1$$

where L is the contact pad length and W is the contact pad width. The contact resistivity for citric and IBM are presented in *Figure 5.* ***8*** and *Figure 5.* ***9***, respectively. These figures show that the etching process drops the contact resistivity significantly when compared with the unetched contacts in Sample A (zero depth) in both cases (i.e. citric and IBM) and for all temperatures. At room temperature, Sample A's (not etched) and Sample B's (10nm depth) contact resistivity are 13.06 mΩ.cm^2 and 1.46 mΩ.cm^2, respectively, which is decreased about 9 times in the case of citric acid. In the same way for IBM, Sample A's (not etched) and Sample B's (15nm depth) contact resistivity are 19.55 mΩ.cm^2 and 1.52 mΩ.cm^2, respectively, which is decreased about 13 times. It is worth noting at this point that the trends for citric acid etching and etching via IBM are remarkably similar. Sample C, E and F in both cases (i.e. citric and IBM) have relativity low contact resistivity compared to Sample A. Only Sample D in both cases (i.e. citric and IBM) has relativity high-contact resistivity compared to the etched samples. This may be due to the scattering at the interfacial layer and dopant layer for example, but it is not conclusive.

These figures also show that the contact resistivity increases exponentially as temperature goes down in both cases (i.e. citric and IBM). Hence, some form of thermionic emission is the dominant current mechanism at room temperature, while quantum mechanical tunnelling most likely dominates at low temperatures. Furthermore, the presence of an interface barrier between the metal and the semiconductor increases insulation as temperature decreases, which reduces the carrier transmission and increases the barrier height concomitantly. In addition, the barrier height can be increased with decreasing temperature due to the increasing the

band gap of the material, depending on Varishni's equation [19]–[21]. The typical barrier height value of a sample is approximately 150 meV, as calculated by the Arrhinias method.

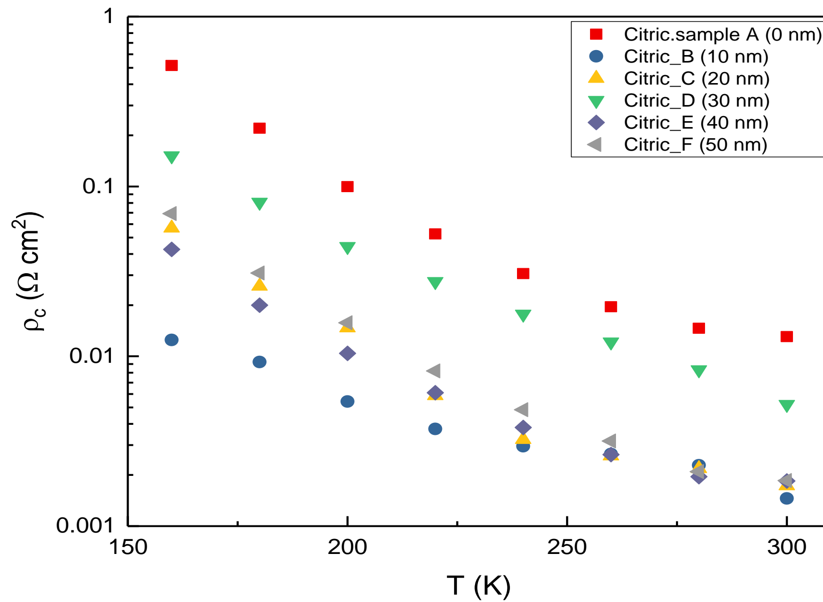

Figure 5. 8: A semilog contact resistivity versus temperature for contacts etched by citric acid over a range of depth.

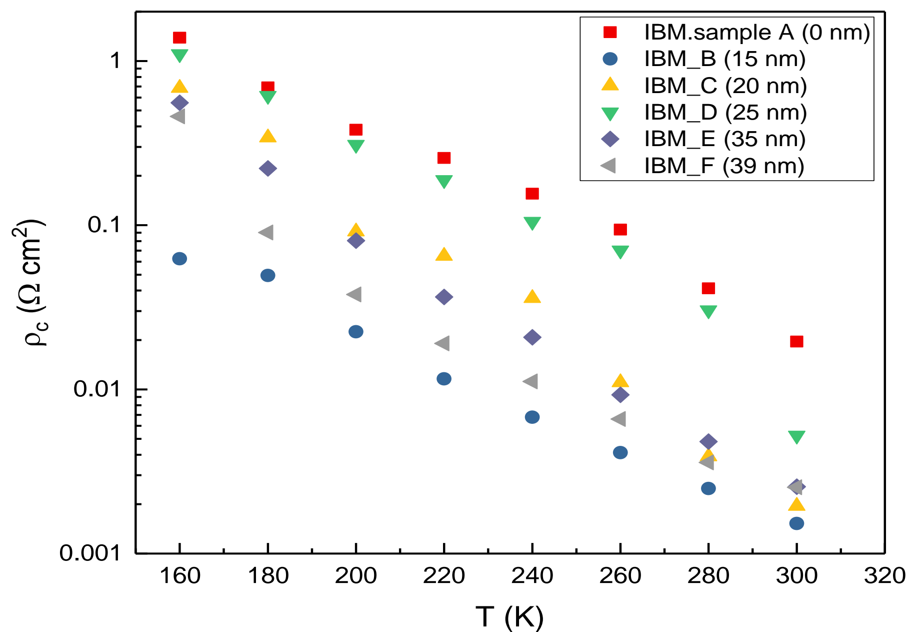

Figure 5. 9: A semi-log contact resistivity versus temperature for contacts etched by IBM over a range of depth.

The charge trapping effect is a significant factor that can affect the MS contact by obstructing the carrier transition. Trapping charge can influence electron tunnelling through the barrier and has been intensively investigated in the case of metal-oxide-semiconductor (MOS) structures with an ultra-thin oxide layer [22][23]. Essentially, the oxide layer has a different bonding state, which disrupts the symmetry and increases the energy level that may lie within the semiconductor's bandgap at the interface [3][24] where a positive surface state charge is exhibited [25]. In addition, structural defects can behave as a 'hole' that enhances the charge trapping [26][27], which has been investigated in this type of material by Shi and Christopher [28][29].

It is worth mentioning that trapping of the charge inside the barrier can cause non-linearity of the I-V characteristics by shifting the forward bias away from the backward bias [30]–[32], as shown in *Figure 5. 10* for example citric and IBM samples at room temperature. These figures show that the differential resistance at low voltage can greater than at higher voltages. However, the shift in the citric sample is larger than that in the IBM sample case, probably because the etching by IBM occurs under vacuum inhibiting oxide formation compared to citric acid etch, which is dried and exposed to air before metal deposition.

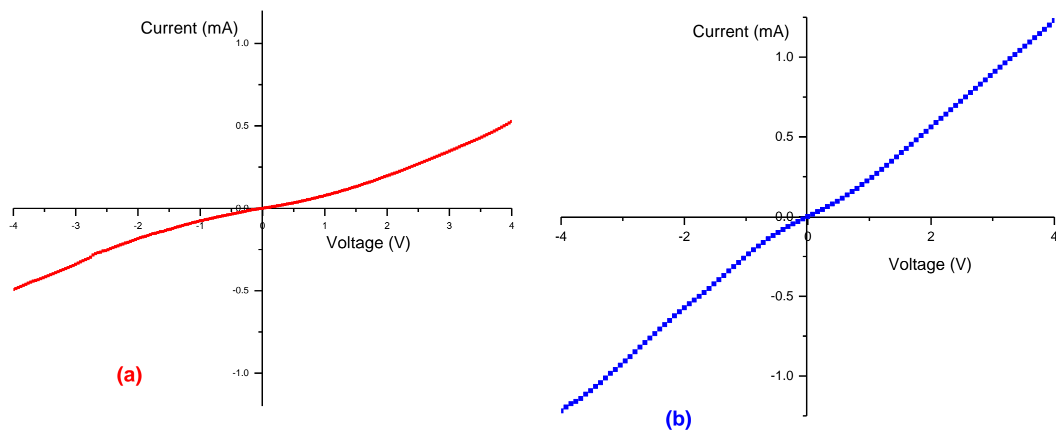

Figure 5. 10: I-V characteristics shifting at room temperature in forward and backward of (a) citric acid (using SF1258 wafer) and (b) IBM samples (using SF1251 wafer).

Figure 5. 11 displays the measurements in the range of (2) - (-2) volts and demonstrates that the barrier is maintained at low temperatures [21][33]. These results indicate that the barrier effect may have a more significant influence at low temperatures.

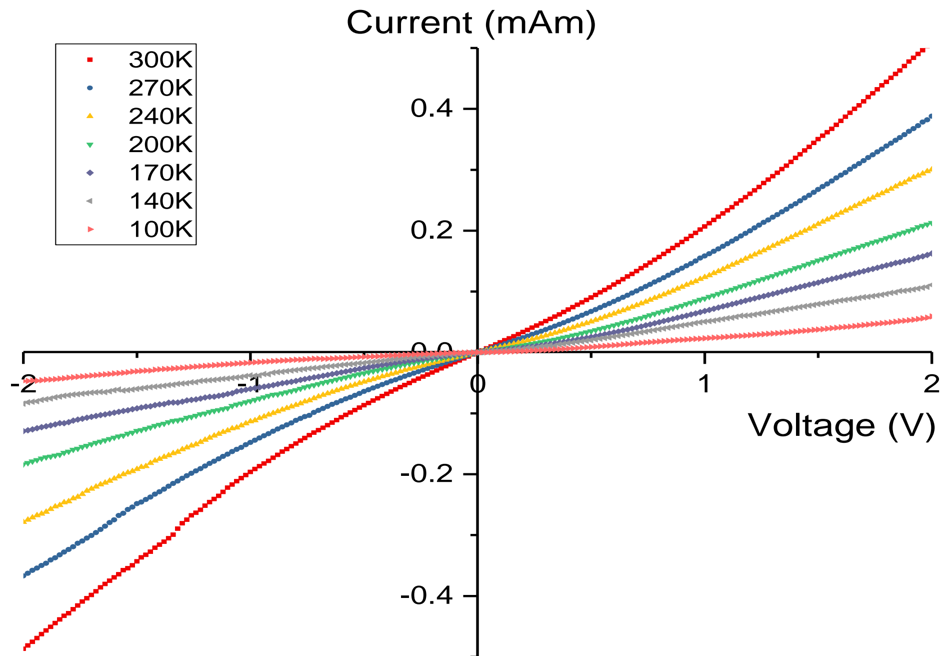

Figure 5. 11: I-V characteristics shifting forward and backward in a range of temperatures for IBM sample.

5.4 Temperature Dependence of the Sheet Resistivity

The sheet resistivity of the etched surface is determined for the AlInSb/InSb QW based LTLM structures and was carried out in the temperature range (160-300) K, which is represented in a semilogarithmic plot for citric acid and IBM samples and is shown in *Figure 5. 12* and *Figure 5. 13*, respectively. It is apparent that, in both cases, the etching process affects the sheet resistivity values in terms of different etching depths. Moreover, the sheet resistivity values clearly increase exponentially with a decrease of temperature. The typical sheet resistivity values at room temperature are acceptable and match the Hall bar measurements for the same material. Whereas, as the temperature falls, the sheet resistivity values increase. This behaviour is the inverse of the expected results. The reason for this can be revealed by measuring the Hall bar

device on any of these samples. It is noticeable from *Figure 5. 14* that the carrier concentrations of citric and IBM samples (red dots) are lower than the normal, more common wafers studied (blue dots) and they decrease sharply at temperatures ~<120K rather than gradually for temperatures >77K for a typical wafer. The main reasons for the low carrier concentration are affective carrier trapping inside the barrier and structural defects, especially at low temperatures. In addition, the wafer doping may have been low through fabrication process by MBE, or the dopant atoms may have defused away from the middle of the top cap layer or trapped in the structural defects. Furthermore, structural defects, micro-twins and threading dislocation in InSb QW have fundamental effects on electron mobility at room temperature [28][34] and low temperatures, and it is not clear that these aren't the same as the more commonly studied samples (compared to sample studied for example by Hayes et al, and Orr et al [35][36].

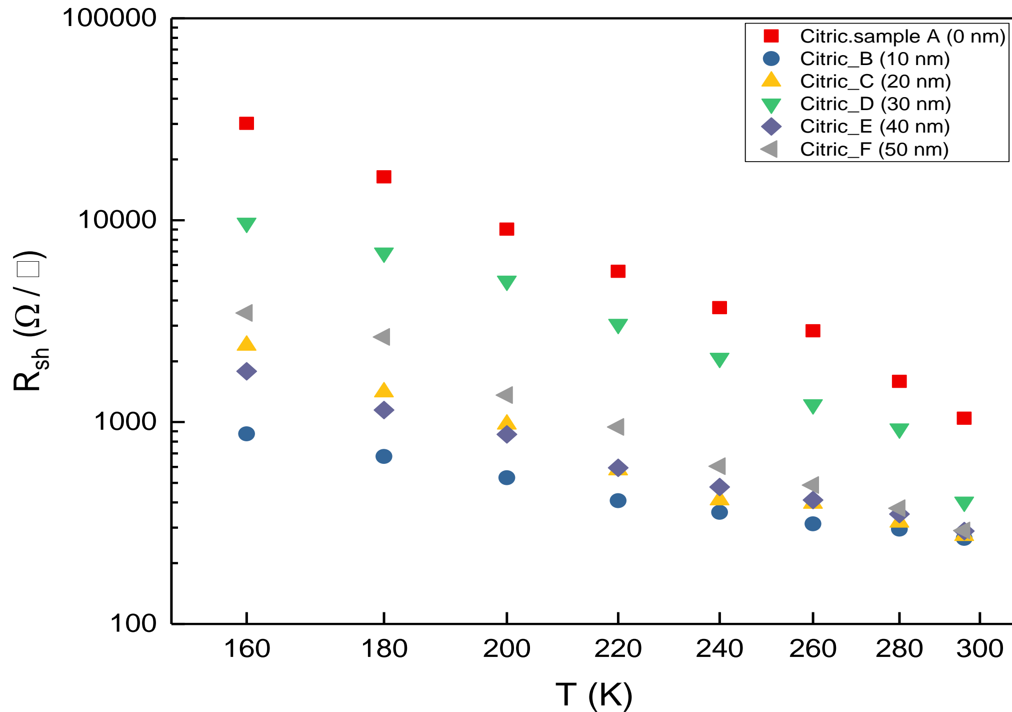

Figure 5. 12: A semilog plot of the sheet resistivity for AlInSb/InSb QW 2DEG of citric samples.

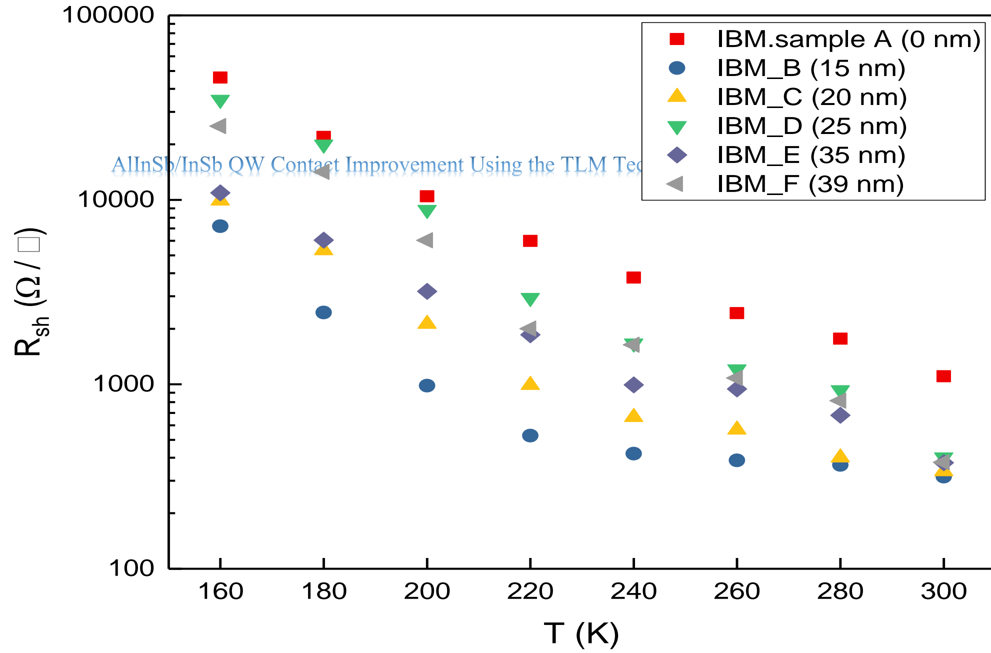

Figure 5. 13: A semilog plot of the sheet resistivity for AlInSb/InSb QW 2DEG of IBM samples.

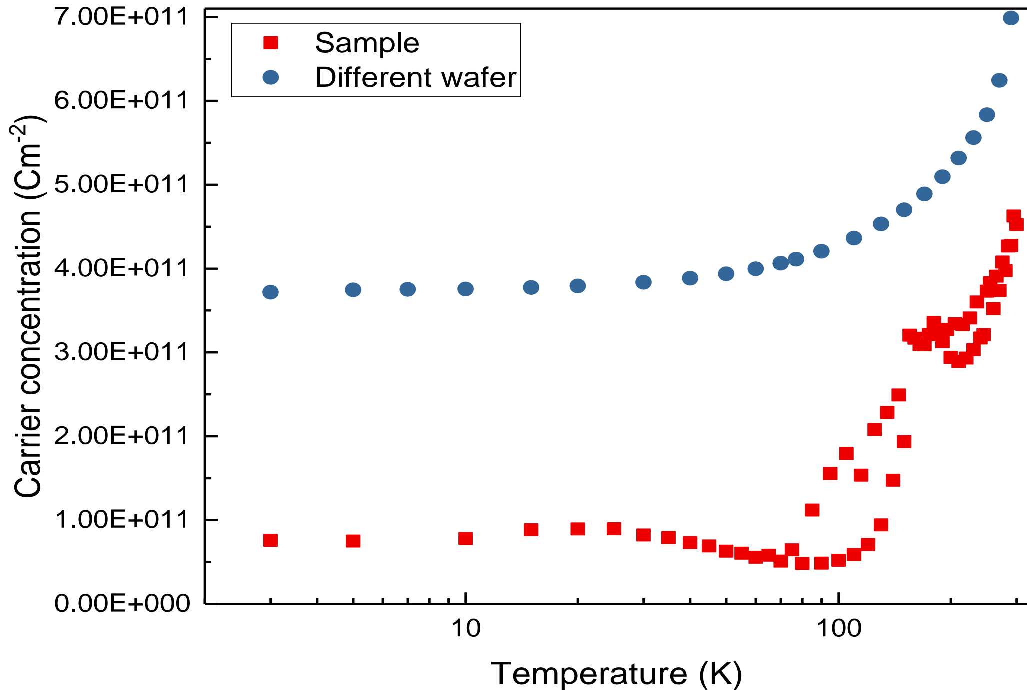

Figure 5. 14: A semilog plot of the carrier concentration as a function of temperature for typical AlInSb/InSb QW (blue dots) and one of the samples (red dots) conducted by hall bar devices. Low carrier density data beyond 70K is unreliable due to inconsistent Hall data (high resistivity).

5.5 Etching Depth Dependence Contact Resistivity

Due to the importance of contact resistivity, it is interesting to present and discuss it as a function of etching depth into the top cap layer of the wafer. As previously described, there are two significant aspects: the oxide layer on the semiconductor surface and δ-doping layer nominally in the middle of the top cap layer. As shown in *Figure 5. 15*, the MS contact resistivity was achieved at 300K as a function of etching depth displaying the contact position. For example, Sample A's contact is directly set on the oxide, which results in the highest resistivity among the etched samples in both cases (i.e. citric and IBM). This can be attributed to the insulating effect, which influences current transportation at the interface. Whereas, the MS contact at 10–20nm depth has a significant decrease in resistivity, due to the removal of the oxide layer. However, at the δ-doping layer, the resistivity value has increased slightly. This can be attributed to a combination of electron scattering directly by the MS interface barrier and the δ-doping layer simultaneously [37][38].

The roughness behaviour as a function of depth in Chapter 4 for citric and IBM etching—as shown in *Figure 4.21* and *Figure 4.31*, respectively—has almost the same behaviour as contact resistivity at 300K. This may indicate that the wafer surface roughness before and after etching is related to the carrier transmission, even at a few nanometres.

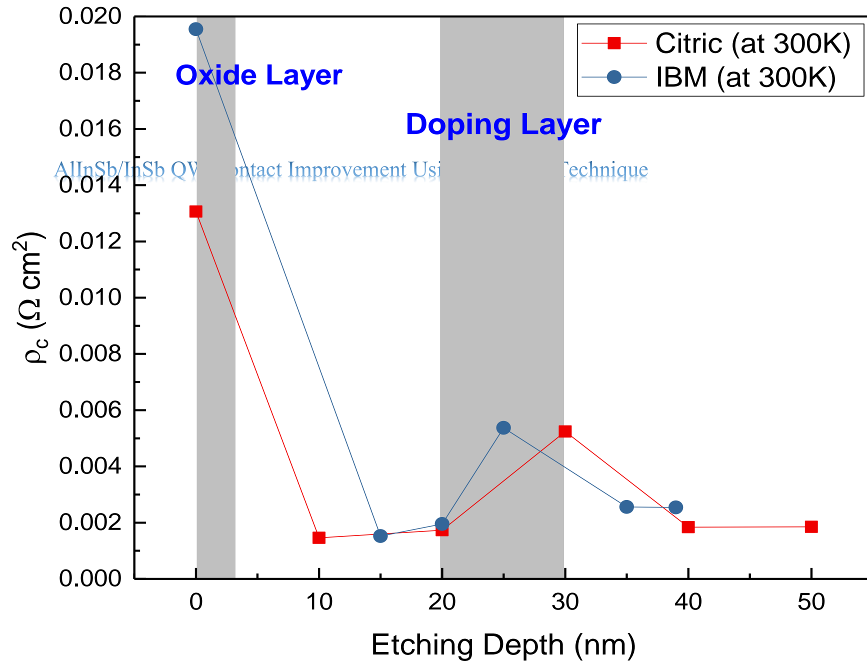

Figure 5. 15: Contact resistivity as a function of citric acid and IBM etching depth into top cap layer (AlInSb) at 300K. This curve shape is important and shows a significant improvement within the region just short of the delta doping plane. This is effectively the first rigorous confirmation of what has been done through anecdotal speculation previously.

Contact resistivity has been measured over a wide range of temperatures and can be translated to a function of depth. This is shown in *Figure 5. 16* and *Figure 5. 17* for citric and IBM, respectively, as semilogarithmic plots. The contact resistivity behaves the same as temperature falls, except that the contacts for 20nm etch depth starts increasing comparatively more than the others in the citric acid case at temperatures ≤ 220K. This can be attributed to the vicinity of the contact interface to the δ-dopant layer. Meanwhile, in the case of IBM, this phenomenon can be realized for contacts at 20nm and 35nm depths with temperatures ≤ 280K, which similarly is likely due to the effect of the δ-dopant layer.

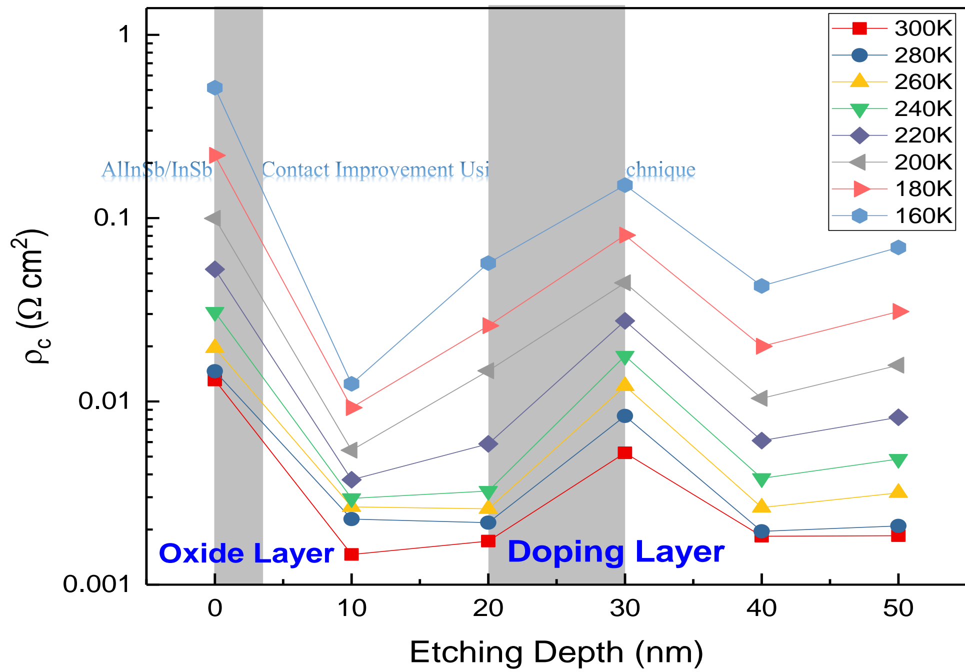

Figure 5. 16: A semilog of the contact resistivity as a function of citric acid etching depth into top cap layer (AlInSb) over a range of temperatures, once again showing clear enhancement of contact conductivity over the region of the delta doped layer.

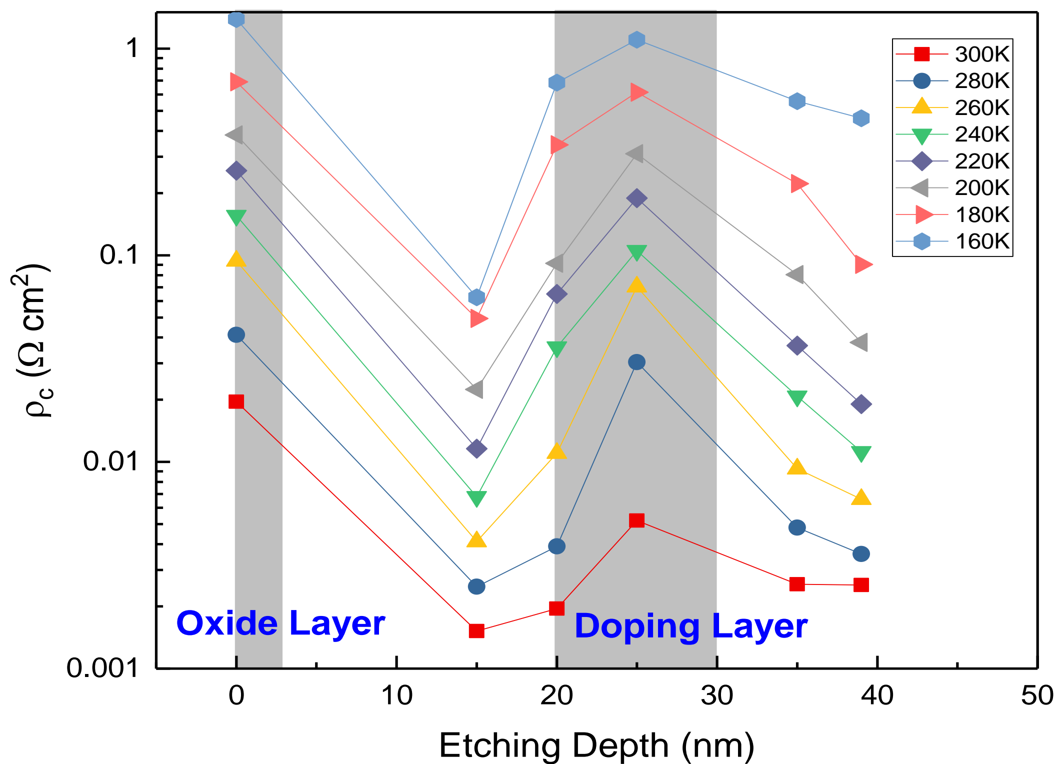

Figure 5. 17: A semilog of the contact resistivity as a function of IBM etching depth into top cap layer (AlInSb) over a range of temperatures.

5.6 Conclusion

In conclusion, a systematic study of etch depth for commonly used contacting techniques for InSb/AlInSb QW heterostructures has been performed. The MS contacts have been described before and after wet and dry etching using the TLM technique. This has been used to investigate the contact resistivity as a function of the temperature and etching depth, and sheet resistivity as a function of temperature.

The results show a drastic decrease of the contact resistivity as a function of the depth compared to the non-etched sample in both cases (i.e. citric acid and IBM), which is mainly due to the removal of the oxide layer. In addition, the contact resistivity is increased exponentially as temperature decreases in both cases (i.e. citric acid and IBM), which is attributed to electron activation energy and the presence of a barrier in the conduction band of the material. The doping layer and surface roughness play a role in affecting the electron transport through the contact position at the dopant layer, which can come from scattering. In these samples cases the sheet resistivity increases as temperature decreases due to a very low carrier concentration and very low doping concentration. Consequently, there may be a charge trapping effect between the barrier, and the presence of significant structural defects.

Finally, these results contribute toward the use of crystalline oxide passivation to develop electron transportation and enhance device performance. Moreover, surface roughness is related to the carrier transmission, even at a few nanometres and at low temperatures.

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Chapter 6

Quantum Transport in InSb Nanoscale Split-Gate Structure

6.1 Introduction

It has been shown that perfectly good two-dimensional electron gases can be formed in narrow gap InSb QWs (Chapter 5). They are assessed as a promising candidate for conductance quantization (nanowires), nanosails and quantum point contact device investigations [1]–[8]. However, InSb QWs have substantial challenges because of the crystal structure defects, and also from the ambient environment and device fabrication which limits contact resistance. As a result, to date, there is only one rather unconvincing conference proceedings report of surface gated InSb split gate operation in the literature [9].

Surface gating is essential if a truly scalable quantum technology based on planar semiconductor qubits is to be realised (either charge or spin based). Whilst in plane gates have successfully demonstrated the potential for this material [7], surface gating remains elusive in part due to the thermal budgets for processing which inhibit truly leak free dielectrics. However, it is not just qubit and entanglement-based quantum computation that is the driver for this work, but the rich spin-based physics that can be investigated in extremely high g-factor material.

Electron transport behaviour in these materials dramatically changes when the conduction is restricted to two-dimensions, as discussed in Chapter 2. The

conductance cannot be described on a macroscopic scale when the length scales are of the order of the Fermi wavevector because these dimensions are often smaller than the ballistic mean free path. Consequently, scattering in the QW cannot play a role in the transport process and, generally, transport equations for the microscopic must be derived. Semiconductor materials are an effective tools to characterize the electron transport in this aspect because the energy separation between transverse modes in a low-dimensional semiconductor device are always inversely proportional to the effective mass, in the same way as for sub-bands in a parabolic potential [10].

In this chapter, a range of device geometries are fabricated to investigate ballistic transport of electrons in low-dimensional InSb structures using surface gated devices to restrict the degrees of freedom (dimensionality) of the active conducting channel. In the devices reported here, the source-drain contact design is relatively small at 3x24μm with two different etching techniques over a range of depths. Different designs of gates (line, loop and solid discussed later) have been used over a range of gate dimensions. Consistent measurement of quantised conductance would be promising for both low power electronics and low temperature transport physics where split gates are typically used for charge sensing.

This chapter presents the best experimental results of quantization conductance obtained for the different geometries of gate, and some model consideration of the implications of the material choice. Interestingly a possible 0.7 anomaly was observed with a loop gate structure, the study of which was the initial aim of this project. Section 6.3 will describe the influence of various scattering mechanisms and main physical limitations on conductance quantization in the 2DEG.

The wafers used in this research are grown in Qinatiq including Dealhead and Blencathra and SF wafers in Sheffield III-V centre with their mobility and carrier density. These wafers have been fabricated and tested at Cardiff university using Hall bar measurement. These wafers information is reported in *Table 6.1*.

Table 6.1: The used wafer including names, carrier density and electron mobility at 3K measurements.

Wafer name	Carrier density n_{2D} (cm^{-2})	Mobility μ (cm^2/Vs)
Daelhead	3.96×10^{11}	130300
Blencathra	4.86×10^{11}	126200
Sheffield (SF0900)	4.11×10^{11}	223000
Sheffield (SF0901)	4.44×10^{11}	203791
Sheffield (SF0965)	3.04×10^{11}	203945
Sheffield (SF0968)	2.2×10^{11}	147000
Sheffield (SF1054)	3.75×10^{11}	244465
Sheffield (SF1055)	3.06×10^{11}	234666
Sheffield (SF1056)	2.14×10^{11}	195320
Sheffield (SF1057)	4.24×10^{11}	231192
Sheffield (SF1258) (TLM-citric)	4.87×10^{11}	201903
Sheffield (SF1251) (TLM-IBM)	7.56×10^{10}	147708

Because of the PMGI residue on the sample surface and uneven MESA etching, the number of nonbroken sample is few and less for good ones but increased with developing the sample process fabrication. So, the nonbroken or measurable are only 0.38% device compare to fabricated devices. Whereas, the good devices are only 10% from the measured which is only 0.038% from the fabricated devices. *Figure 6. 1* shows the evaluation way and random distribution of broken and non-broken devices using SEM for all devices in different magnifications, checking the FEED pads, arms, gate structure, gate bridges and isolation in between the device structures after MESA etching.

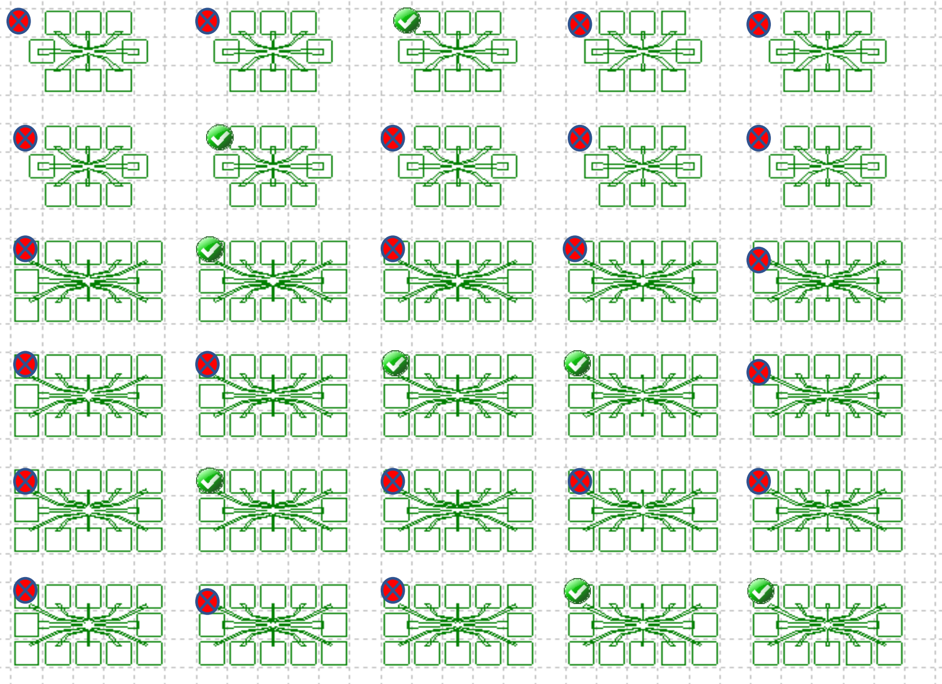


Figure 6. 1: Schematic diagram of one field of 12 fields as one sample. So, each sample contents 360 device.

6.2 InSb 2DEG Quantized Conductance

The quantized conductance of an AlInSb/InSb QW 2DEG was measured using split gates devices at a temperature of 2.7K. The distance between the Ohmic contacts for all devices was ~2µm, while the gates were a range of designs and dimensions as reported in Chapter 3. *Figure 6. 2* shows the used gates and the novel loop gate. The SEM images in *Figure 6. 3* show the top view of the whole device structure. Image (a) shows the FEED pads for wiring and their arms, which are fanned out from the central island. This island is the effective active area of the 2DEG. Image (b) shows the air bridge arms of the gate structures. This airbridge technique is designed to inhibit the leakage current coming from the gate arms by minimising the area of contact. Finally, image (c) shows three pairs of line structures, where each gate has approximately 100nm length (line width) and 250nm width (gap) (see chapter 3 *Figure 3.5*) on the island surface. The MESA etching is problematic and inconsistent, as can be observed in *Figure 6. 3* (a). In general, this is believed to be due to issues with

residue from the PMGI (SF6) photoresist process; however, etching is well defined around the island in some devices.

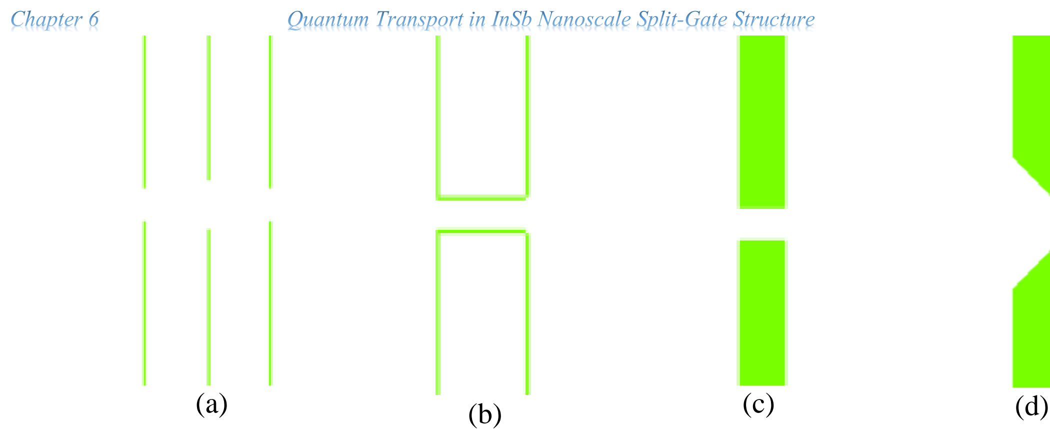
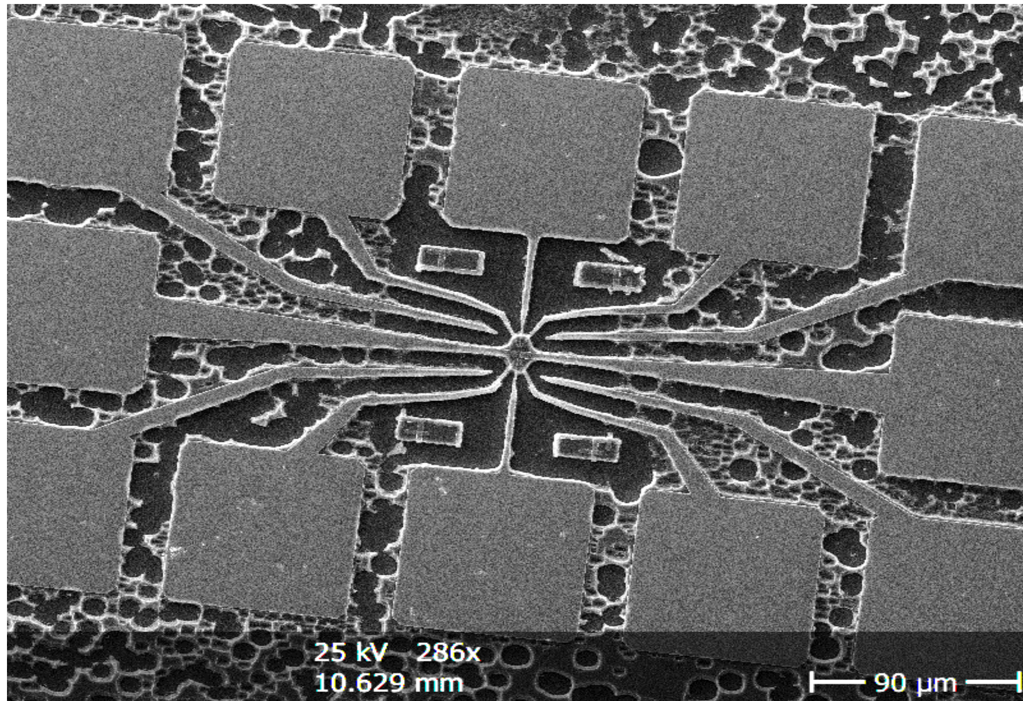
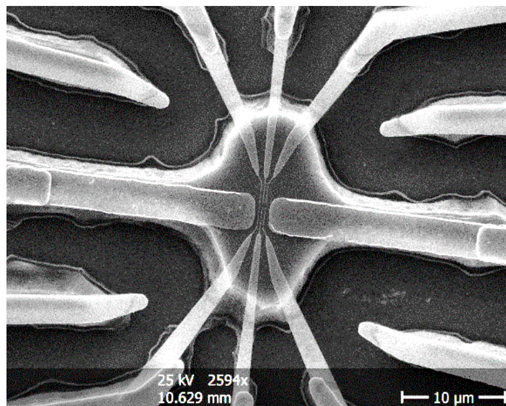


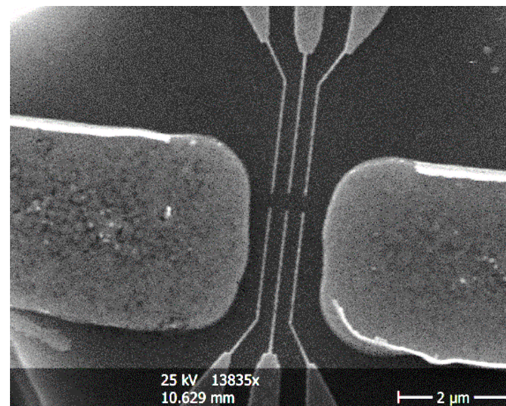
Figure 6. 2: Schematic diagram from the e-beam GDSII files of some of the gate structures including; 3 pairs of straight forward (e-beam single pixel) line gates, novel loop gates that minimize contact area, and solid gates including funnel gates that minimize back scattering within the emitter contact.



(a)



(b)



(c)

Figure 6. 3: SEM images of a split-gate device: (a) the whole device including bond pads, (b) small Ohmic contacts, three pairs of air bridge structures and the middle island, and (c) high-magnification of the three-line gate structure.

Measurement proceeds by applying AC voltage on the source-drain contacts (in order to measure conductance) and DC voltage on the surface gate, in order to increase the potential above the Fermi level and form a constriction in the 2DEG between the source-drain contacts, which will increase the resistance. *Figure 6. 4* shows a

simulation of the potential of a typical surface split-gate structure and the applied voltage modulated as a function of the dimensions. The constriction is formed in the 2DEG at its maximum gap width, which is approximately equal to the e-lithographic width of the opening in the gate. Lowering the gate voltage Vg, the constriction width is reducing until it fully pinches off. This phenomenon can be observed through measurement of the I-V characteristic gradient change over the gate voltage in *Figure 6. 5*. This figure shows the gate leakage current with a maximum value of (2.90×10^{-4}) mA at zero bias which corresponds to the maximum applied gate voltage and maximum resistance.

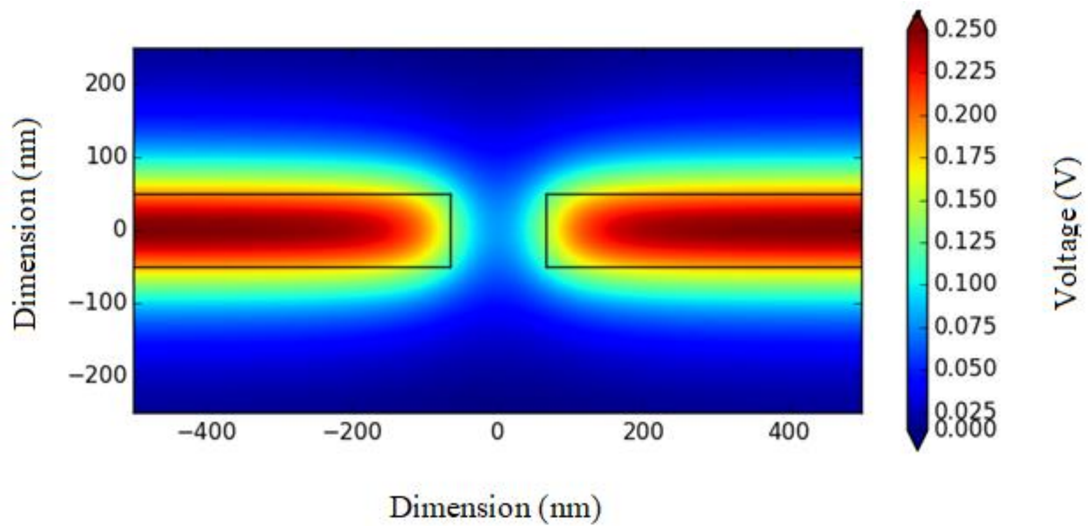


Figure 6. 4: Split-gate structure on the 2DEG Surface with applied voltage scale as a function of lithography dimensions.

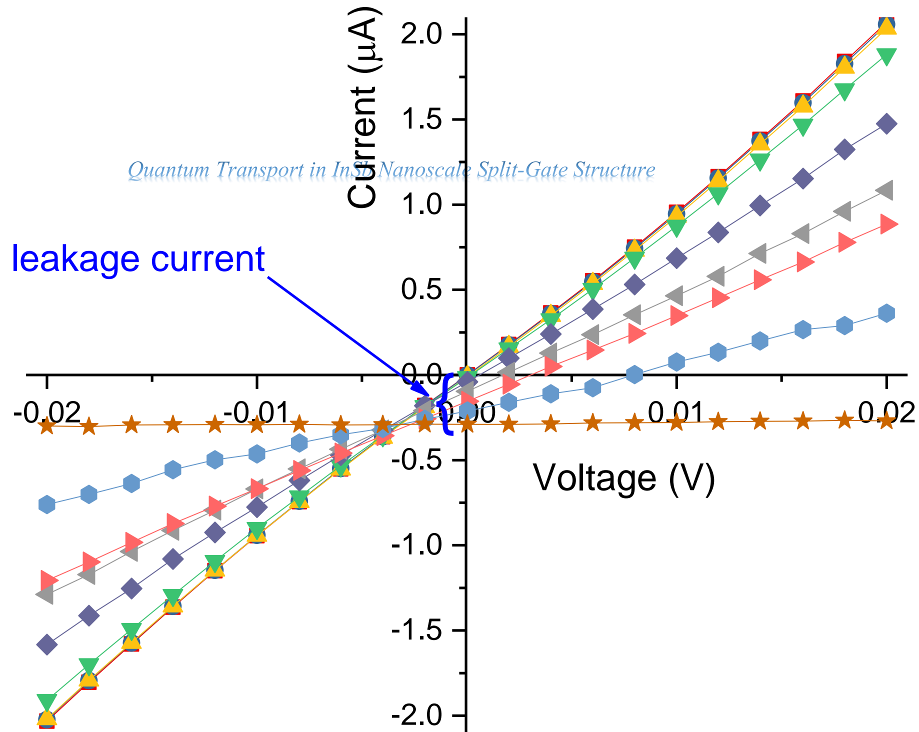


Figure 6. 5: Source-drain I-V characteristic over a range of gate voltages of split-gate device for AlInSb/InSb QW 2DEG, with shifting towards negative voltage of current value at zero bias as a leakage current.

Figure 6.6 (a) shows a theoretical plot of the energy of three sub-bands as a function of wave vector (k), while *Figure 6.6* (b) explains the theoretical modulation of conductance quantization plateaus of an InSb QW 2DEG (using equation 2-25) at four different temperatures. This model has considered a temperature dependence of the bandgap according to the Varshni's equation (2-1), tending toward more accurate results. Increased temperature causes thermal activation, which leads to smearing out of the plateaus, which disappear completely at elevated temperatures. However, this is extreme for InSb due to the light mass particle which results in large energy sub-band separation (In fact smearing happens when the thermal energy becomes comparable to the sub-band splitting). This can be also, understood by the Fermi-Dirac distribution [11],

$$f(E-E_F) = \left[1 + e^{(E-E_F)/K_B T}\right]^{-1} \tag{6-9}$$

where E is the band energy, E_F is the Fermi energy, K_B is Boltzmann constant and T is the temperature.

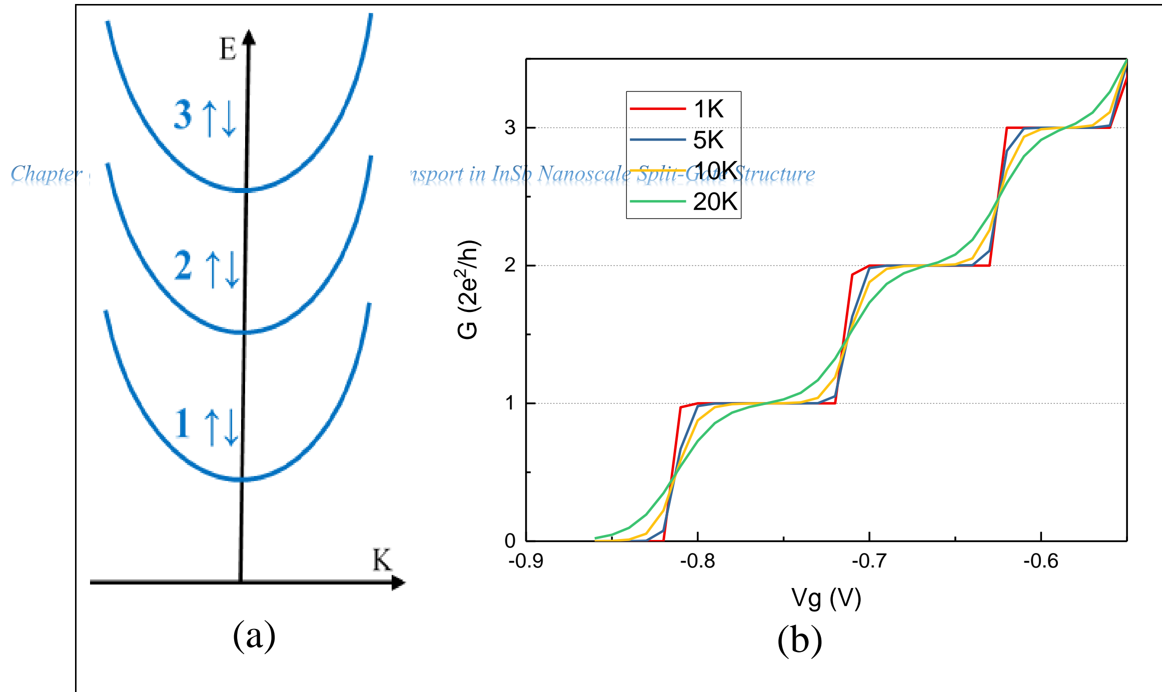


Figure 6.6: Theoretical conductance quantization in InSb QW 2DEG: (a) the energy of three energy sub-bands as a function of wave vector (k) and, (b) quantization plateaus corresponding to these energy sub-bands as a function of the gate voltage at four different temperatures.

Conductance can be calculated from the measured resistance as a function of gate voltage. *Figure 6.7* shows the quantized conductance plateaus of two steps in units of $2e^2/h$ measured as a function of the voltage applied to one set of the line-gate structure shown in the previous SEM image (*Figure 6. 3*). These results are produced by using an applied source-drain voltage range of -20 to +20 mV and a gate voltage (on a single pair in the range of 0 to -3 V). The device was made from a 'Blencathra' wafer 2DEG with 30nm QW layer thickness. The device contact resistance is about 10kΩ, at 2.7K and without applying gate voltage. As the gate voltage increases further, the conductance reduces until the channel is completely pinched off at -3 V. The quantized conductance is pinched off whenever the Fermi level is at the band bottom of the (n +1)th transverse sub-band $G = n\,(2e^2/h)$ [12].

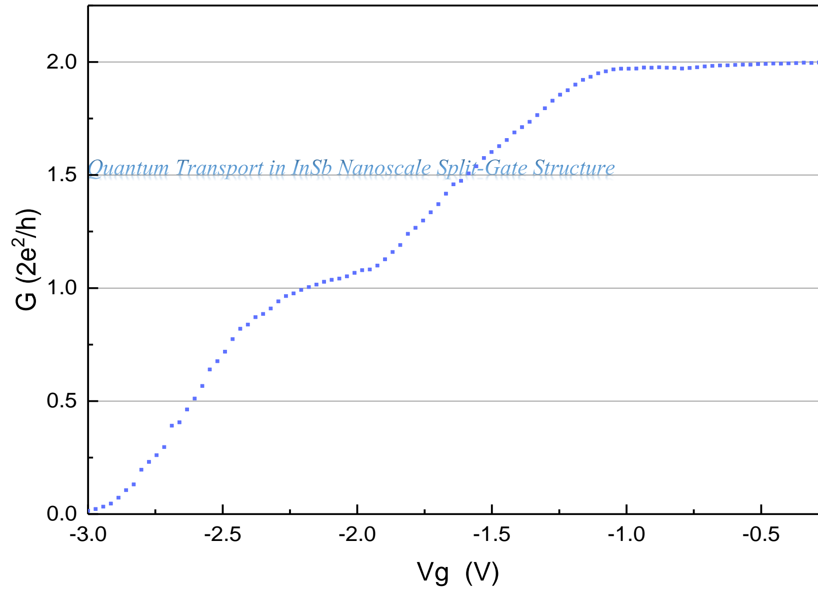


Figure 6.7: Quantized conductance of a simple split-gate device for an AlInSb / InSb 2DEG with island mesa design.

In this figure it can be seen that the gate structure pinches off the quantized conductance. This even happens with the presence of leakage current in the top cap layer that contributes to current, the effect of which has been previously investigated in heterostructure materials by Feuer [13].

The second device is a split line gate device with Ohmic contacts of the same design but with a (smaller area) bar active region and two small isolated islands mechanically supporting the air bridges, as presented in the SEM images in *Figure 6.8*.

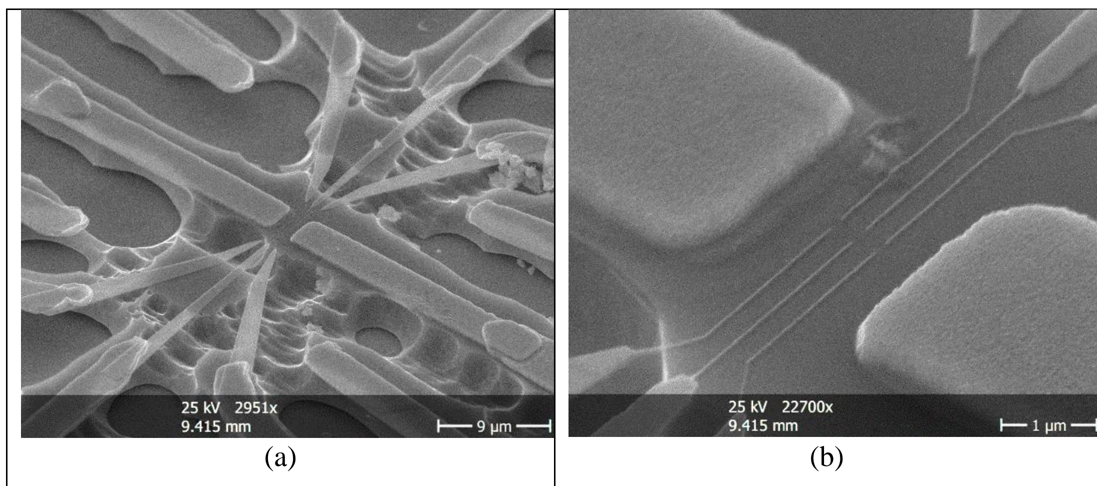


Figure 6.8: SEM images of the split-gate device: (a) Ohmic contacts, three pairs of air bridge structures; and (b) three-line gates structure.

The applied voltage on the source-drain contacts range from -4 to +4 mV and the gate voltage from 0 to -0.8 V, which is less than the previous island mesa case. This can be attributed to the gate structure quality, which could depend on the Schottky barrier magnitude or on the PMGI photoresist residue issue under the gate. This device has a resistance of about 35kΩ, at 2.7K without applying gate voltage. *Figure 6.9* shows a set of four albeit poor quality steps of N ($2e^2/h$), with one step smeared out or disappearing at 3N. The smearing of this step is likely due to scattering as a result of the high-resistance of the contacts, which produces scattering near the channel and can exhibit an oscillation [14].

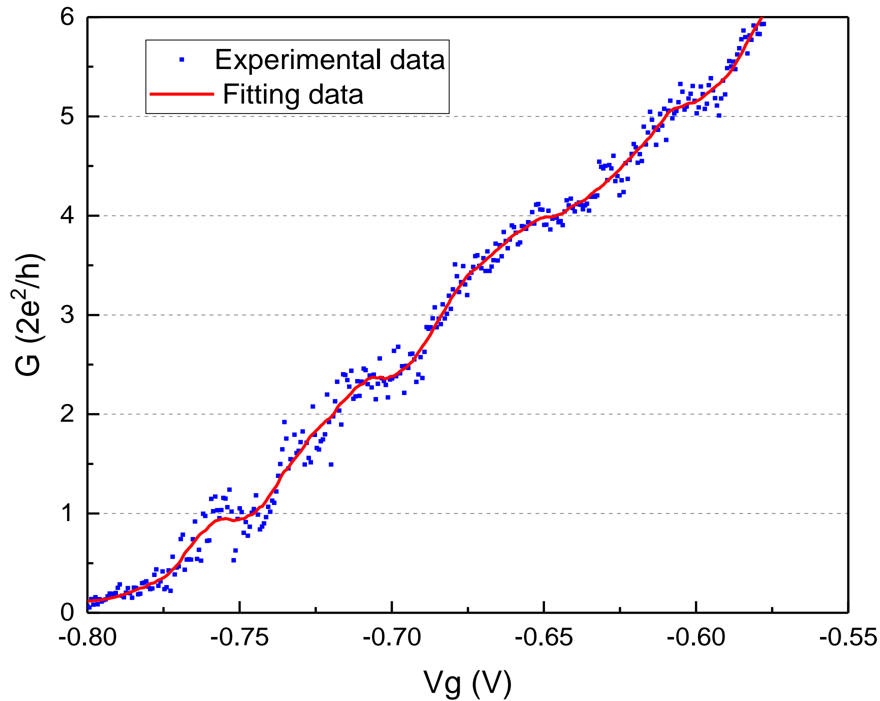
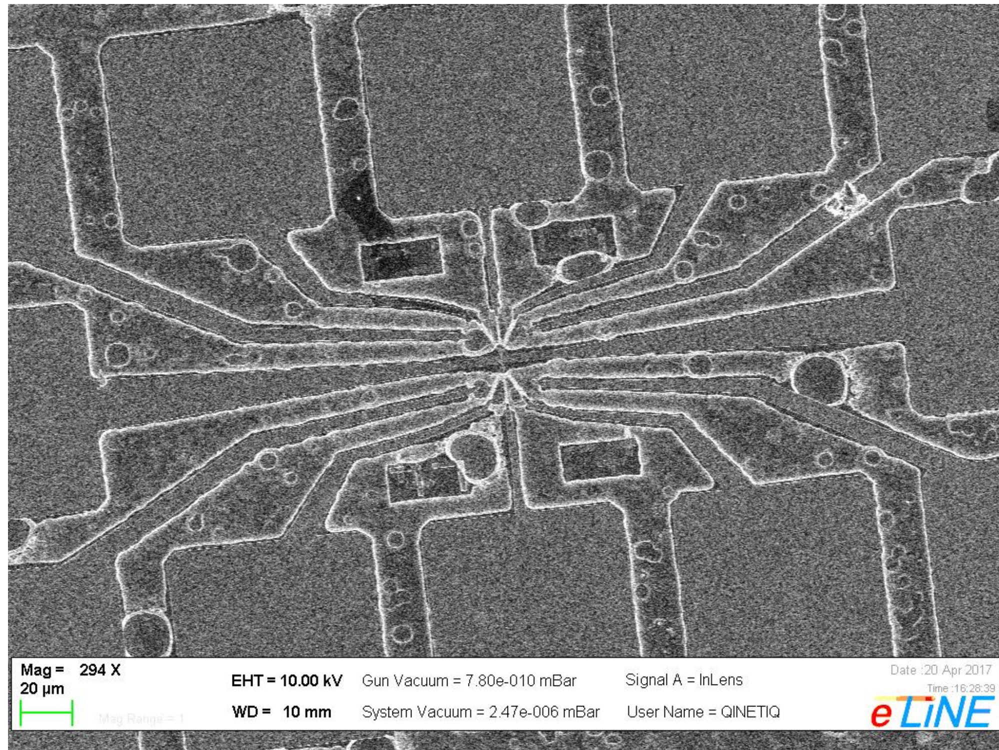
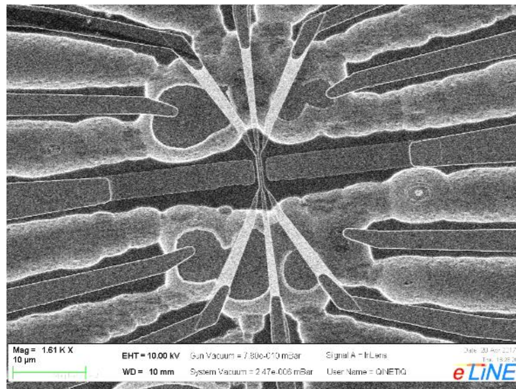


Figure 6.9: Quantized conductance of split-gate device for AlInSb / InSb 2DEG for bar design with island supported bridges measured at 2.7K.

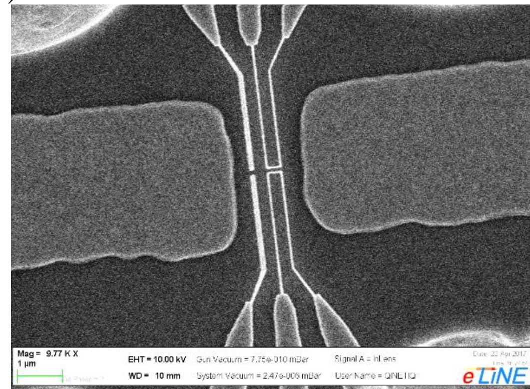
The third device studied here is a split solid and loop gate device, whose gate is 100nm in length and 100nm in width for the solid, and 300nm in length and 100nm in width for the loop structure. In this instance, the gate structure has been deposited with a 30nm silicon dioxide (SiO_2) layer as an insulator beneath the Ni/Au to reduce the leakage current. The device structure is shown in the SEM images in *Figure 6.10*.



(a)



(b)



(c)

Figure 6.10: Progressive magnification of SEM images of split-gate device: (a) the whole device, (b) Ohmic contacts, three pairs of air bridge structures and the middle island, and (c) high-magnification, two (solid and loop) gate structures.

Due to the oxide layer of the gate structures, the applied effective gate voltage is much greater than without an oxide layer; as shown in *Figure 6.11*, which exhibit a low leakage current. However, some samples exhibit a leakage current through their gates when a high- voltage is applied. The gate used in this particular measurement is the solid line structure. The resistance is approximately 3 kΩ, at 2.7K without applying a gate voltage. This happens because the etching of the Ohmic contact with IBM for 30 sec decreases the contact resistance. *Figure 6.11* just shows the results of two

quantized conductance steps, with a pinch off at 6.5V gate voltage, which is relatively high due to the oxide layer under the gate metal.

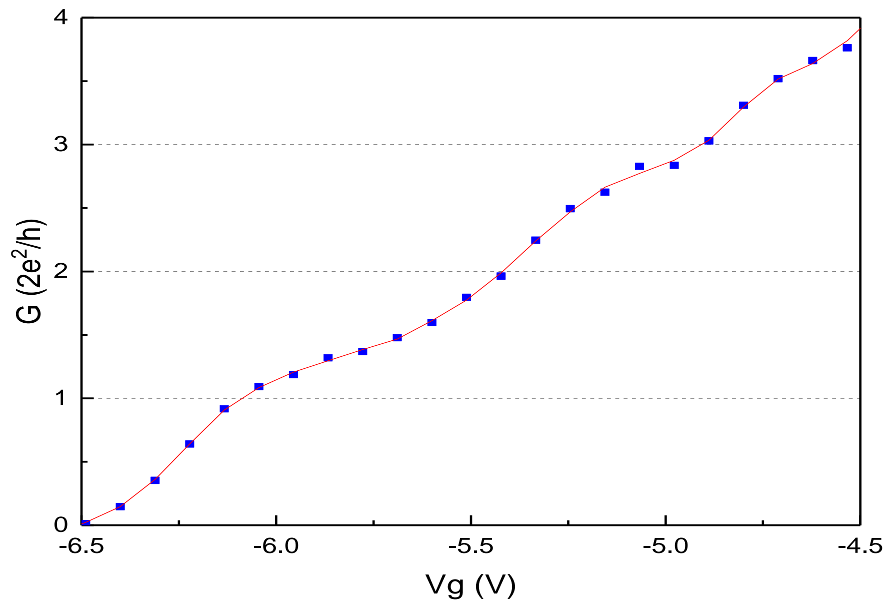
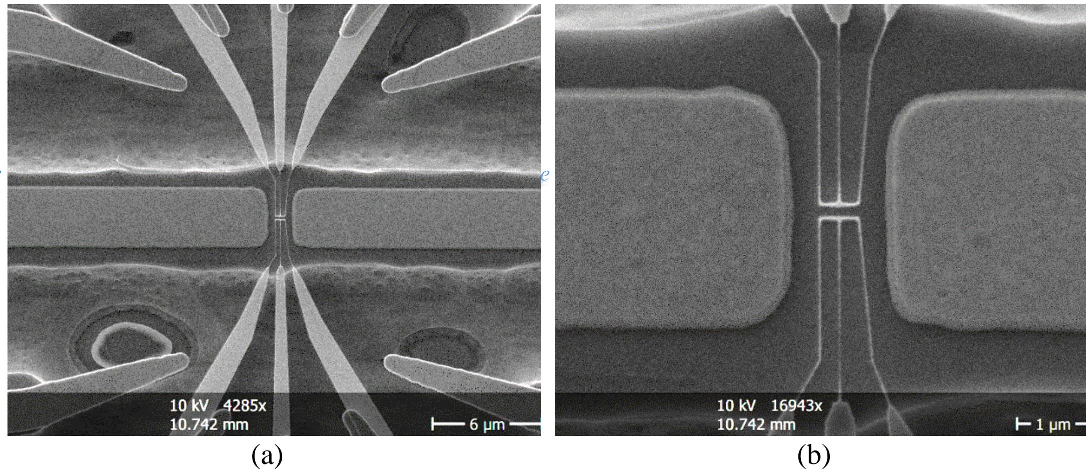


Figure 6.11: Quantized conductance of split-gate device for AlInSb/InSb 2DEG, after series resistance subtraction.

The fourth device design studied is a split loop gate device with a ratio (length/width) of two (for 600nm and 200nm loop structure). They are also deposited with a silicon dioxide layer (SiO_2) under the gate metal (Ni/Au). (n.b. This gate design allows the use of any pair of six connections to apply the gate voltages in case of any breaking issue with some of the air bridges). The successful gate structure fabrication and definition using E-beam lithography and deposition of the device is presented in *Figure 6.12* using SEM.



(a) (b)

Figure 6.12: SEM images of split-gate device: (a) Ohmic contacts, three pairs of air bridge structures and the middle small island, and (b) loop gate structure.

This gate structure needs a high- voltage to constrict the current in the QW, due to the oxide layer of the gate as shown in *Figure 6.13* and *Figure 6.14*. Meanwhile, *Figure 6.13* shows results of two clear quantized conductance steps. Interestingly, the first after series resistance correction is at 0.7 ($2e^2/h$) conductance. This could be attributed to a commonly observed transport anomaly [15][16]. The main plateau after correction is at ($2e^2/h$), with pinching off with nearly zero conductance at ~5.5 volts by the gate. Non-zero conductance in this case could be due to a leakage current transport from the gate structure. The conductance is correlated to the split-gate length/width ratio [17] whereas, 0.7 anomaly reduces as the curvature of the potential barrier becomes shallower. When the confinement becomes shallower, the sub-band spacing becomes closer [18]. In addition, the 0.7 anomaly can disappear below at a specific temperature but can be enhanced by an external magnetic field, considering the g-factor of material [19]. Furthermore, the plateau’s flatness depends on the gate length and width of the 1D channel [20].

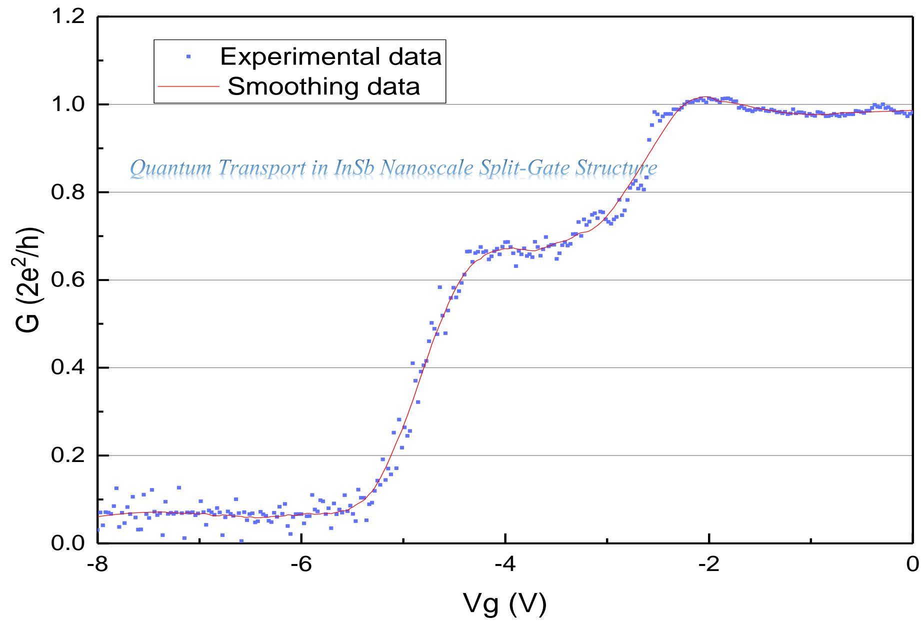


Figure 6.13: Quantized conductance of split-gate device for AlInSb / InSb 2DEG for island design at 2.7K.

Figure 6.14 shows two obvious quantized conductance steps at one and two ($2e^2/h$) and an unclear 0.7 conductance anomaly (at ~ -4.6V), after subtraction of series resistance with a pinch off at ~ -5.3 volts [21].

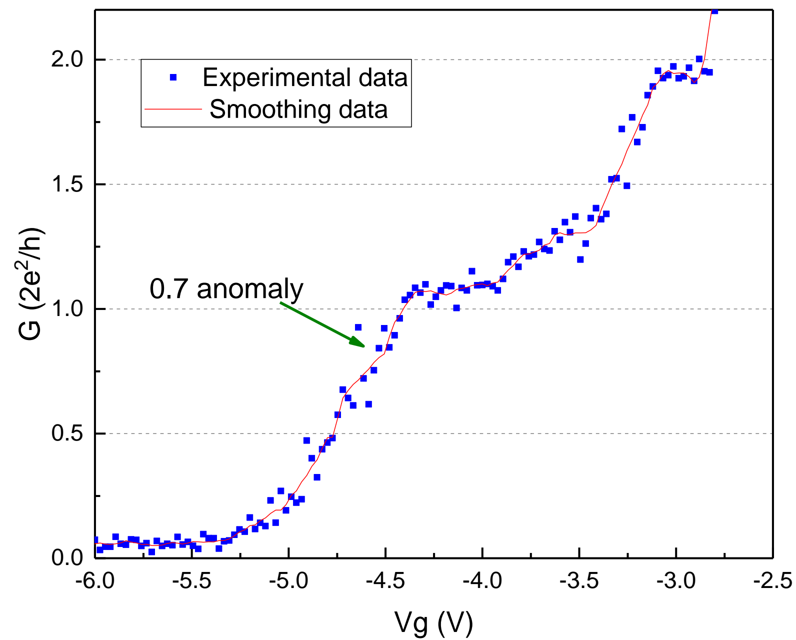


Figure 6.14: Quantized conductance of split-gate device for AlInSb/InSb 2DEG, after series resistance subtraction at 2.7K.

The oscillations on the conductance plateaus in *Figure 6.9*, *Figure 6.13* and *Figure 6.14* are due to a transmission probability that is associated with reflections at the entrance and exit of the channel constriction [11]. In addition, the shape and strength vary from device-to-device, depending on the uncontrolled variations in the confining potential, such as a quantum interference effect associated with electron backscattering that is caused by impurities or defects near the constriction [11]. A MS contact barrier will result in additional backscattering events, which exhibits a further smearing out of the quantized conductance plateaus.

6.3 Limitations of Conductance Quantization

Many factors can affect the quantized conductance plateaus. In fact, threading dislocations (TDs) can significantly affect these by carrying an electrical potential due to accumulation of dopant or the presence of charged traps [22]. The leakage by TDs and carrier hopping between these traps can also significantly degrade the device's performance [23][24]. In particular, TDs enhance the conduction on the surface [25], which exhibits device-to-device variability due to formation of multiple parallel paths of current with different conductivity [26]. Furthermore, the TDs severely reduce the carrier mobility in QW due to the scattering process, which affects the conductance plateaus [27]–[30].

The quantized conductance plateaus can be smeared out and disappear due to scattering by impurity and/or TDs, either inside or near the constriction [12][31]. Also, the presence of a contact barrier near the ballistic channel, distorts the plateau's structure at interface scattering [14][32][33]. Electron scattering formed at the interface of AlInSb/InSb heterojunctions layer has been investigated by Nash [1][34]. The source-drain contacts interface barrier and it's high-resistance increase exponentially as temperature decreases, which has been discussed in detail in Chapter 5. Furthermore, surface roughness and dopant scattering (discussed in Chapter 5) can affect the mobility and the conductance plateau's structure, especially due to the roughness of the etched side walls [35][36].

The presence of dangling bonds at the semiconductor surface is responsible for the main leakage current on [37] the top cap, especially in short distance between the

source-drain contacts (as discussed in Chapter 5). This contributes to the drain current and affects the plateau structure.

These AlInSb/InSb QW 2DEG devices remain challenging because of the high-density of dislocations within the $Al_xIn_{1-x}Sb$ buffer layer, starting from the substrate to the wafer surface, as measured by Transmission Electron Microscope (TEM). *Figure 6.15* shows a cross-sectional micrograph of AlInSb/InSb wafer with 4.2x10^9 cm^{-2} defect density for AlSb layer on the substrate (GaAs), 6.0x10^9 cm^{-2} for buffer layer and 1.0x10^9 cm^{-2} for cap layer that positioned on top of the QW layer.

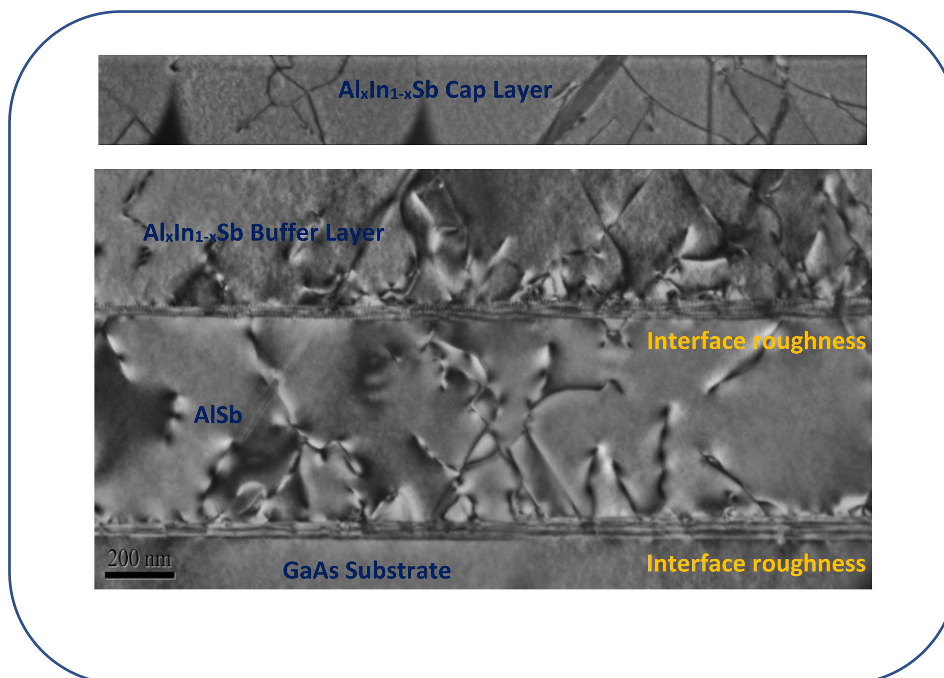


Figure 6.15: Cross-sectional TEM image of an AlInSb/InSb wafer explaining why a high- density of TDs are propagating through the structure with the growth direction. Courtesy of Dr Richard Beanland – Warwick University.

Figure 6.16 shows a schematic diagram the main scattering processes can be presented in AlInSb/InSb split-gate devices, including scattering at: source-drain contacts, dopant scattering, threading dislocations in the QW, reflections at the entrance and exit of the channel constriction and presence of charged traps. In addition to the leakage by TDs and dangling bonds on the surface.

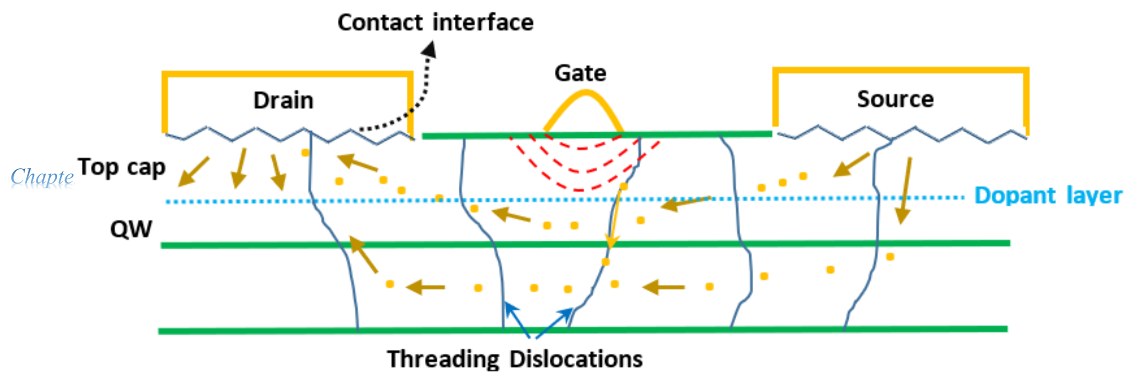


Figure 6.16: A schematic diagram main scattering process elements can be presented in AlInSb/InSb split-gate devises. These scattering elements; Ohmic contacts in both sides with electron reflection, doping layer and TDs scattering in the QW and top cap.

6.4 Conclusion

In conclusion, conductance quantization has been observed and investigated in AlInSb/InSb 2DEG QW heterostructures using electrostatic confinement by different designs of split-gate structures. Measurements of quantized conductance in the split-gate device are direct evidence of ballistic transport and controlled mode occupation.

A split-gate device fabrication process has been developed. However, even when using chemical cleaning and ashing techniques resists residue has proved to be problematic resulting in low device yield, increasing the number of broken devices. By etching the AlInSb/InSb contacts using wet and dry techniques, the source-drain contact resistance is significantly decreased, and this enhances the device's performance enough to observe conductance quantization. At the commencement of this thesis work it was impossible to see conductance quantization steps due to prohibitively large ohmic contact resistance (which was greater than the quantised unit of conductance for these devices). Development of the contact resistance has enabled rudimentary observation. In some cases, it is still necessary to subtract the contact resistance to see these plateaus which loses definition (and effectively data). Furthermore, using a cold deposited oxide layer deposition for the gate structure has been shown to reduce leakage current. In addition to the variety of gate structure designs, the airbridge technology helps to decrease the leakage current by decreasing the active contact area. These results show that the AlInSb/InSb QW 2DEG wafers

with 30nm QW can be used to investigate conductance quantization further, although with some fundamental physical limitations related to structural defects and the fabrication process.

Furthermore, the 0.7 conductance anomaly has been observed using a split-gate device with a novel loop structure in the ratio of 2 for length/width with (600nm and 200nm) deposited with a silicon dioxide layer (SiO_2). This emphasis that the 0.7 anomaly conductance is correlated to gate's dimensions.

Finally, these results need further investigation depending on the characterizations and developments in Chapters three, four and five, which will enhance the device's performance and the electron population in the QW.

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Chapter 7

Conclusion and Future investigation

Conclusion and Future Investigation

The potential for this material is in spin-based physics and the possibility of developing all electrical spin-based qubit systems for quantum information. However, the technology is immature in the extreme, and basic knowledge of issues such as ohmic contacting and gate technology hold progress back. This thesis has been concerned with material characterisation, device component design, fabrication, measurement, and basic modelling of InSb/AlInSb 2DEG heterostructures for use in such quantum systems. A number of electronic transport phenomena have been studied over a wide range of temperatures using 30nm InSb quantum wells that are modulation doped, with the aim of extracting material parameters pertinent to electron transport mechanisms in metal/semiconductor contacts and ballistic transport in conducting 1D channels. The main fields of investigation and outcomes discussed in the previous chapters can be summarised as follows:

i. *Wafer Characterisation*

   Material characterisation was performed of the active layers of AlInSb/InSb QW 2DEG wafers, including electrical assessment, AFM, EDX, and basic XPS. The wafer and active device surfaces have been characterised using EDX, observing the surface elements and contamination layers coming through various processing steps. In addition, the surface roughness of the wafer has been characterised and analysed using AFM to evaluate any effect of roughness on the Ohmic contact stack and its resistivity before and after two key etching techniques (Dry and wet etch).

ii. *Cleaning and etching*

A cleaning process was developed as a result of EDX outcomes, while the wet and dry etching techniques that have been used resulted from XPS outcomes. The etching area was characterised in terms of surface roughness that effected directly the contact resistivity. The surface roughness along with recess depth into QW layer has been investigated in relation to the dopant layer and the QW.

iii. *Metal-semiconductor contact resistivity evaluation*

TLM measurement has been shown to be a good technique which offers a good understanding of the electron transport mechanisms of the MS interface and for evaluating the contact resistivity. Ohmic contact resistivity has been investigated as a function of etching depth over a wide range of temperatures in order to understand and optimize the resistivity.

iv. *Quantization of conductance in InSb QW 2DEG with a variety of gate designs.*

InSb QWs were used to study the quantization of conductance by electron ballistic transport. This was done with limiting Ohmic contact resistivity and in some cases significant gate leakage, however conductance quantisation was observed regardless of crystal structural defects. Several surface metal split gate devices were designed to attempt to minimise leakage currents including novel loop gate structures. Many trials were performed using different fabrication processes to develop the fabrication process and produce good devices with low contact resistance, good lift off, and non-broken air-bridges gates.

Broadly, the investigations in Sections i, ii, iii and iv are described in detail in Chapters 3, 4, 5 and 6, respectively. This chapter briefly summaries the main results of these studies and it makes some recommendations for further investigations.

7.1 Conclusions

There are three areas of significant advancement in this work. Firstly, hard fought process development for nonstandard processing. This includes new cleaning and dry ashing techniques which were used to remove photoresist residue on surfaces, previously plaguing device realisation, which come from the sample fabrication processing steps and has been observed on the wafer and samples previously limiting

for example MESA isolation and gate operation. The development of more successful cleaning routines has resulted in modified (and more consistent) contact resistance, increases the number of non-broken air-bridge gates, and produces more uniform MESA etching. Wet and dry etching techniques were used to remove the 3nm thick observed oxide layer on the AlInSb/InSb wafer surface (Chapter 4). The etching was achieved for different depths towards the QW, while observing any change in RMS roughness affecting the contact roughness and resistivity. The RMS surface roughness analysis was described for both techniques that were studied in Chapter 4 (dry and wet etch) and showed less RMS roughness than the pristine wafer surface. This indicates that the etching process interacts reasonably and uniformly with this material which is also confirmed by the RMS roughness peak FWHM, mean roughness and full normalised area roughness values. In addition, it is important to state that the effects of the surface oxide and resist residue on sample etch depth and surface roughness are clear. The resist residue obstructs the etching, which acts as a barrier layer. Furthermore, both etching techniques modified the roughness, which decreased the Ohmic contacts resistance and ultimately enhanced the performance of the quantum device.

The metal-semiconductor contact resistance, resistivity and the InSb QW sheet resistance were evaluated using the TLM technique after removing the oxide layer and using new cleaning techniques. The source-drain (I-V) characteristic of the Ohmic contact showed an interfacial barrier that increases the resistivity at both room temperature and low temperature for all etched samples and which was more obvious for non-etched samples. The TLM technique evaluated and showed a drastic decrease of the contact resistivity as a function of the recess depth compared to the non-etched sample in both cases (i.e. citric acid and IBM), which is mainly due to the removal of the oxide layer and new cleaning techniques. In addition, the contact resistivity is increased exponentially as temperature decreases in both cases, which is attributed to some electron activation energy and the presence of a barrier. The doping layer and surface roughness play a role in affecting the electron transport through the contact position at the dopant layer, which can come from scattering. Furthermore, the roughness has an indirect effect, the low roughness decreases the density of defects created through wafer growth. Meanwhile, the sheet resistivity increases as temperature decreases, due to a very low carrier concentration and very low doping

concentration. Consequently, there may be a charge trapping effect in the barrier and structural defects. These results contribute toward developing electron transportation and enhance device performance.

Many trials were performed using different fabrication processes in order to develop new fabrication processes for this material and produce good devices with low contact resistance (using the results in Chapter 5), good lift off, non-broken air-bridges gates, eliminate leakage current through the gates, and even MESA isolation. Chemical cleaning and ashing techniques were substantial steps to develop for the fabrication process however using an oxide layer deposition for the gate structure significantly reduced the gate leakage current.

Several thousand split gate devices have been fabricated, but only ~0.038% devices can be measured in low temperature at (2.7K) to obtain the quantization conductance. Quantisation conductance steps have been observed in InSb-based heterostructures with electrostatic confinement by surface metal split gates. This has only been reported once in the literature, with very poor form for the I-V. The low temperature ballistic transport length has been shown elsewhere (Chapter 4) to be sufficiently large for the gate dimensions used, and this has been confirmed by the presence of transport effects consistent with discrete quantised states. Therefore, quantized conductance measurements in the split-gate device are direct evidence of ballistic transport and controlled mode occupation. The 0.7 conductance anomaly has possibly been observed using a novel loop split-gate device in the ratio of 2 for length/width which was deposited with an insulator layer. These gate devices show great promise for maximising channel length but holding gate leakage to a minimum as a result of reduced surface area contact with the active layer.

7.2 Future work

All the results of characterizations and developments presented in Chapters 3, 4, 5 and 6, would benefit from further study to enhance the device's performance, contact resistivity, electron mobility, ballistic transport and the electron population in the QW. It is imperative for InSb technology that routine processes must be as reliable or better

than standard GaAs material. These further investigations would likely focus on several key areas:

1. Development of AlInSb wafer growth by using interlayers or superlattice buffers, decreasing the surface roughness, or using a different substrate that has less mismatch with the AlInSb material to eliminate or prevent the production of threading dislocations that decrease scattering mechanisms, enhance ballistic transport and yield improving electron mobility in this more promising material than GaAs.
2. Development of the Ohmic contact resistivity by rapid thermal annealing (RTA) technique or heating up the sample to less than 180°C for long time can help to diffuse Ohmic contact metals down towards the first semiconductor layer (AlInSb/InSb), which can eliminate the interfacial layer and remove the potential barrier and enhance the linearity of the I-V characteristic [1]. So far rapid thermal annealed contacts for this material have eluded the community.
3. A low IBM etching rate can be used by decreasing the etching power (discharge voltage and current), which might be able to remove surface defects, minimising the RMS surface roughness. This may reduce and modify the contact resistivity [1].
4. Split gate devices can be fabricated without using bilayer (containing PMGI (SF6)), especially with Ohmic contacts fabrication by using alternative photoresist or spin thick layer of (S1805) photoresist, because of the difficulties of cleaning after heat has been applied through the fabrication process steps.
5. The quantization conductance should be measured using a range of space between Ohmic contacts and at a wider range of sample temperatures to observe step fluctuations or smearing, which can be enhanced by applying a magnetic field [2][3].
6. It would be beneficial for these devices to be measured with a vertical magnetic field, which should allow the investigation of the large Zeeman spin-splitting of confined states predicted using the large g-factor of InSb. The 0.7 conductance anomaly requires further investigation using split gate devices that have a range of gate sizes, temperatures and magnetic fields.

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Appendix

A.1 Circular Structure (CTLM)

Study of Ohmic contacts can be achieved by alternative geometry of TLM in circular structure, which is abbreviated to CTLM. This geometry only requires one lithography step without a mesa etching step. Thus, excluding them could simplify the fabrication process. Consequently, the use of a CTLM structure can reduce the errors that are introduced by the lateral current crowding and this can achieve a more symmetrical current flow pattern by eliminating the edge effects that are always present in linear TLM structures [1]–[4].

This structure is important in enabling a quick experiment with III-V heterostructure material [5]. A typical planar structure is shown in *Figure A.* ***1***, which describes a geometry with one disc and one ring.

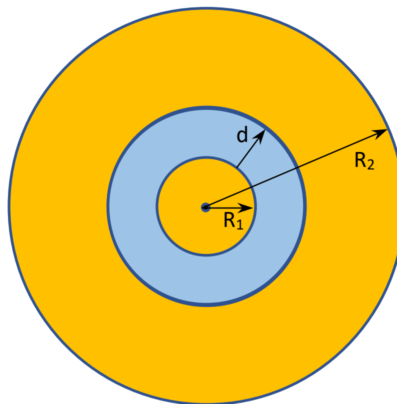

Figure A. 1: Top view of typical CTLM structure explaining the radii of the inner disk, outer ring and the gap in between them.

This geometry involves a current flow under and through the interface of the contacts. The resistance R between contacts for the circular configuration follows the equation [3][6]:

$$R = \frac{R_{sh}}{2\pi}\left[\ln\frac{R_2}{R_2 - d} + L_T\left(\frac{1}{R_2 - d} + \frac{1}{R_2}\right)\right] \qquad \text{(A-1)}$$

where R_{sh} is the sheet resistance of the material, R_2 is the radius of the outer circular contact, d is the gap spacing and LT is the transfer length.

The nonlinear relationship between resistance and the gap distance is apparent with CTLM because of the geometry. When the ring radius to gap ratio is large, the ring contact geometry reduces to the standard TLM structure that has a linear relationship by normalising the data with a correction factor for each gap spacing [7]. These correction factors are essential to compensate for the difference between the TLM and ring layouts to get a linear fit to the data. Without the correction factors, the specific contact resistance would be underestimated [8]. The equation describing these correction factors is described by [9]:

$$C = \frac{R_1}{d}\ln\frac{[R_1 + d]}{R_1} \qquad \text{(A-2)}$$

where R_1 and d are the disk radius and the gap spacing, respectively. The experimental CTLM data is divided by the calculated correction factors to arrive at values that can be used to compare to a linear fit. Figure A.2 shows a typical measured resistance as a function of the gap spacing, with nonlinear curve (red squares), which can be transformed into a linear relationship using the correction factors (blue circles). Therefore, from this linear fit, the specific contact, sheet resistance and so on can be calculated properly [9].

The results of the CLTM structure not very good and need more analysis or fabrication new devices to be considered.

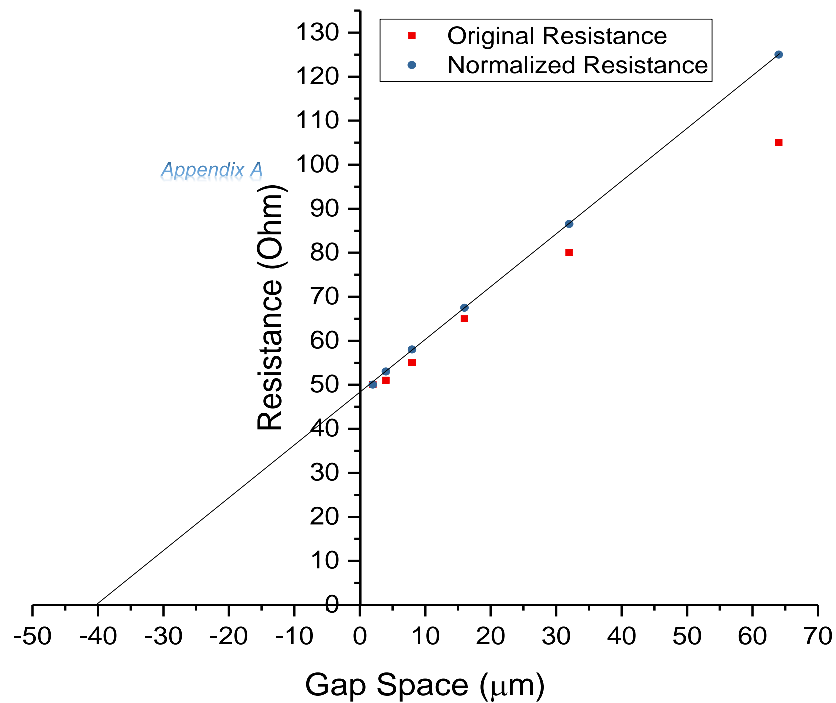

Figure A. 2: The resistance for circular structure versus gap spacing before and after applying the correction factors.

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