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Low threshold quantum dot lasers directly grown on unpatterned quasi-nominal (001) Si

Yating Wan, Chen Shang, Justin Norman, Bei Shi, Qiang Li, Noelle Collins, Mario Dumont, Kei May Lau, Arthur C. Gossard, John E. Bowers

***Abstract*—We report electrically pumped, continuous-wave (cw) InAs/GaAs quantum dot (QD) lasers directly grown on quasi-nominal Si (001) substrates with offcut angle as small as 0.4°. No GaP, Ge buffer layers or substrate patterning is required. An anti-phase boundary free epitaxial GaAs film was grown by metal-organic chemical vapor deposition (MOCVD) with a low threading dislocation density of 3×10^{7} cm^{-2}. Room-temperature cw lasing at ~1.3 µm has been achieved, with a minimum threshold current density of 34.6 A/cm^{2} per layer, a maximum operating temperature of 80 °C, and a maximum single facet output power of 52 mW. A comparison of various monolithic III-V hetero-epitaxy on Si solutions is presented. Direct growth on unpatterned quasi-nominal (001) Si may yield the best material quality at the lowest lifecycle cost.**

***Index Terms*— Integrated optoelectronics, quantum dots, wafer scale integration**

I. Introduction

Optical interconnects are superior to electronic interconnects through their high bandwidth capability, immunity to electromagnetic interference, and minimum attenuation and dispersion at 1.3 and 1.55 µm wavelengths. This technology replaced electrical wires several decades ago in long-haul telecommunications and is now taking shape, with a similar trend, at increasingly short lengths in datacom and high-performance computing (HPC) [1]. As cost is a fundamental design criterion, the development of optoelectronic integration with complementary metal-oxide-semiconductor (CMOS) electronics would obviously boost the adoption of photonics for post-Moore performance scaling of electronic systems [2]. A complete suite of photonic devices is needed, with passive optical components on the silicon-on-insulator (SOI) platform, high-speed modulators based on silicon PN junctions, high-speed photo detectors (PDs) based on epitaxially grown germanium films [3, 4], and integrated lasers. While the realization of a laser based entirely on a Si-like nonpolar group IV material system could be an enabler for the implementation of on-chip light sources, the best Group IV laser has threshold current density around 300 kA/cm^{2} [5], which is ~3000 times higher than that of the state-of-the-art III-V laser (with a typical number of ~0.1 kA/cm^{2}).

Heterogeneous silicon photonics via wafer bonding high quality III-V layers onto a Si substrate is now reaching maturity [6, 7], with commercial products shipped in volume for the data center market [8]. However, the use of III-V substrates for the laser growth can be costly. Absent any III-V substrate reclamation processes, over 95% of the III-V material is wasted in the process (only 1-2 µm of the epi material is used, the 500 µm substrate is etched away). As an alternative, direct growth of high gain III-V laser material onto large area, low cost Si substrates is well suited for high volume applications. This research field was boosted by using a quantum dot (QDs) active region in place of traditional quantum wells (QWs), giving rise to lower thresholds and better reliability [9-11]. To date, tremendous advancements have been made in blanket hetero-epitaxy of III-V compound semiconductors on Si substrates, including scaling III-V integration up to 300-mm Si wafers [12, 13], overcoming the antiphase boundary (APB) problem on exact (001) oriented Si [13-17], and exceptional laser performance with continuous-wave (cw) threshold currents below 1 mA [18], single-side output power of 175 mW [19], near zero linewidth enhancement factor [20], isolator-free stability at optical feedback levels of up to 90% [21], and extrapolated mean time to failure of more than 10,000,000 hours at 35 °C [22].

For III-V/Si integration to be compatible with CMOS processing, microelectronics-standard nominal (001) Si substrates with a miscut angle less than 0.5° are preferred. However, except for the use of a thin GaP buffer layer, conventional hetero-epitaxy on planar Si wafers generally requires a 4°–6° offcut angle to form a prominent double-stepped Si surface so that APB formation can be prevented [23]. Recently, there has been notable progress to achieve APB-free III-V epilayers on on-axis (001) substrates. Chen *et al.* [13]

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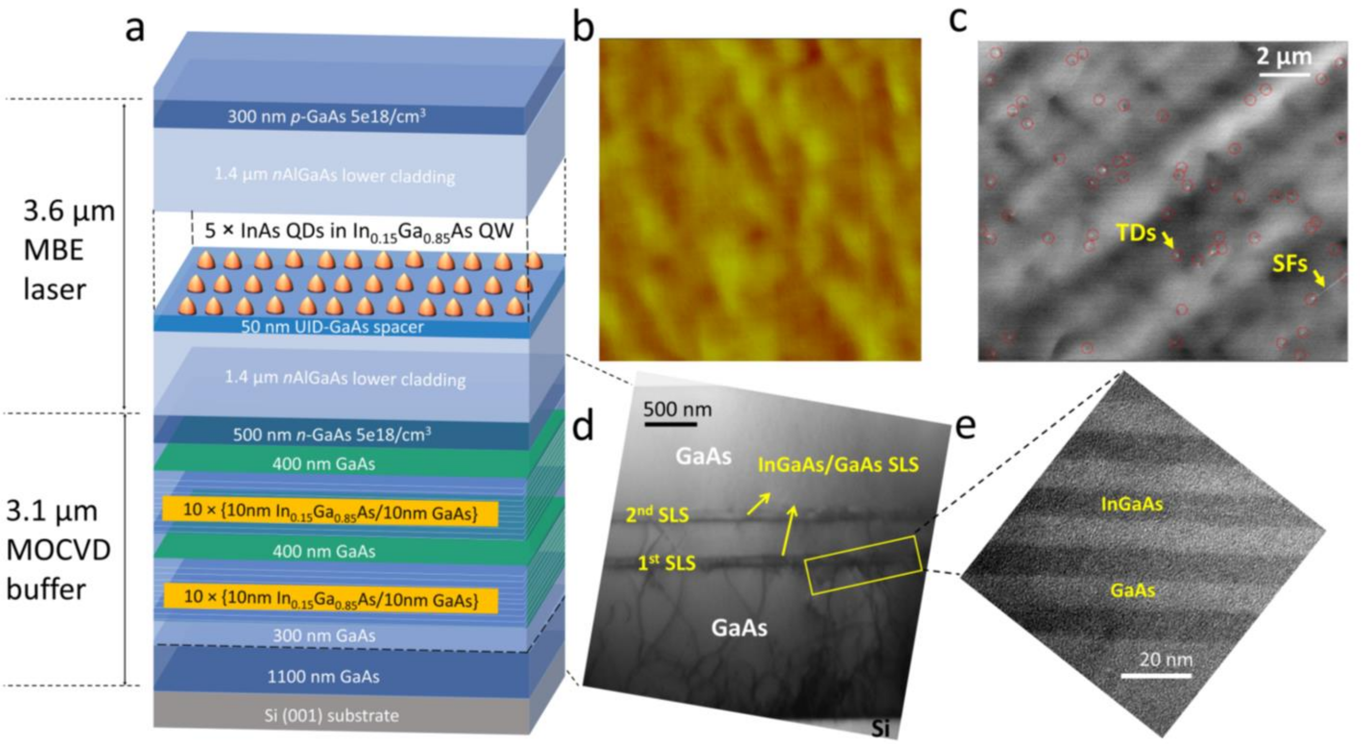

Fig. 1. (a) Schematic image of the buffer structure by MOCVD and the full stack of a standard QD laser structure by MBE. (b) Atomic force microscopy image of the sample surface, with a RMS value of 2.26 nm. The image has a size of 10 × 10 µm^2. (c) Plan-view ECCI image of the buffer structure, showing that the TDD is as low as 3×10^7 cm^{-2}. (d) and (e) Cross-sectional TEM images of the SLS structure, showing stacking faults termination effects.

reported electrically pumped 1.3 µm InAs/GaAs QD lasers directly grown on microelectronics-standard (001) Si substrates with unpatterned surface using a sophisticated Si surface preparation step. However, there has been observed degradation in laser performance, including higher threshold current densities and poorer T_0, compared to lasers directly grown on offcut Si substrates [24]. Norman *et al.* [25] uses selective patterning of an on-axis (001) silicon substrate to simultaneously circumvent the issue of antiphase domains and reduce the dislocation density in a coalesced GaAs buffer layer. By growing III/V in trenches with a V-shaped bottom consisting of two {111} facets, anti-phase disorder can be avoided with no specific surface treatment required [26, 27]. However, if the trenches are very narrow and deep, it becomes more difficult to achieve perfectly clean {111} Si facets, which might degrade the yield to some extent. Wei *et al.* [17] initialized a quite unique way to achieve high-quality III-V layers on Si via homo-epitaxially grown (111)-faceted Si hollow structures by in-situ hybrid epitaxy. In addition to the APB annihilation and threading dislocation termination effects through the in-situ (111)-facet, the hollow structures can effectively reduce the thermal stress. This is very beneficial to alleviate microthermal cracks from thermal expansion mismatch between III-V and Si, though only optically pumped devices have been demonstrated so far [28]. Kwoen *et al*. [16, 29] reported all molecular beam epitaxy (MBE) grown high-quality InAs/GaAs QD lasers on on-axis Si (001) substrates without using patterning and intermediate layers of foreign material. Though buffer-layer threading dislocation density (TDD) value is approximately eight times higher than that for the QD lasers on on-axis GaP/Si [19], high-temperature (over 100°C) cw operation was achieved with threshold current density as low as 370 A/cm^2 and a maximum net modal gain centered around 1225 nm [29].

Compared to MBE, III-V buffers grown by metal organic chemical vapor deposition (MOCVD) may have advantages in terms of high growth rates in volume production requirements. While most III/V-on-Si buffers were grown using MBE, in this work, we achieved a high crystalline quality GaAs buffer by MOCVD with a TDD of 3×10^7 cm^{-2}. This value is over 3 times smaller than that of the recent TDD for MBE grown GaAs buffer on (001) Si [29] and closes the gap relative to the TDD of the state-of-art lasers on Si with intermediate GaP buffers [19]. Furthermore, the InAs/GaAs QD lasers were grown on quasi-nominal (001) Si without any Ge/GaP buffers or substrate patterning. This waives the trouble of selective etching of the patterned Si, the cost of growing a well-engineered thin GaP/Ge layer on Si, the substrate offcut, still producing ultra-low thresholds (34.6 A/cm^2 per layer) with reasonable output powers (up to 52 mW) and a maximum cw operating temperature of 80 °C. These encouraging results provide prospect to generate high-quality III/V-on-Si buffers with the smallest compromise for the requirement of CMOS-standard on-axis Si (001). Finally, a benchmark of various monolithic III-V hetero-epitaxy on Si solution is presented. Ultimately, this technology is agnostic to what the initial buffer approach is. Whichever solution yields the best material quality at the lowest lifecycle cost shall be used.

II. Experimental Procedure

The III-V buffer layer growth was carried out by MOCVD and the active device layers of the QD lasers were grown by MBE, as shown in Fig. 1(a). Quasi-nominal Si (001) substrates with offcut angle as small as 0.4° are used to achieve APB-free

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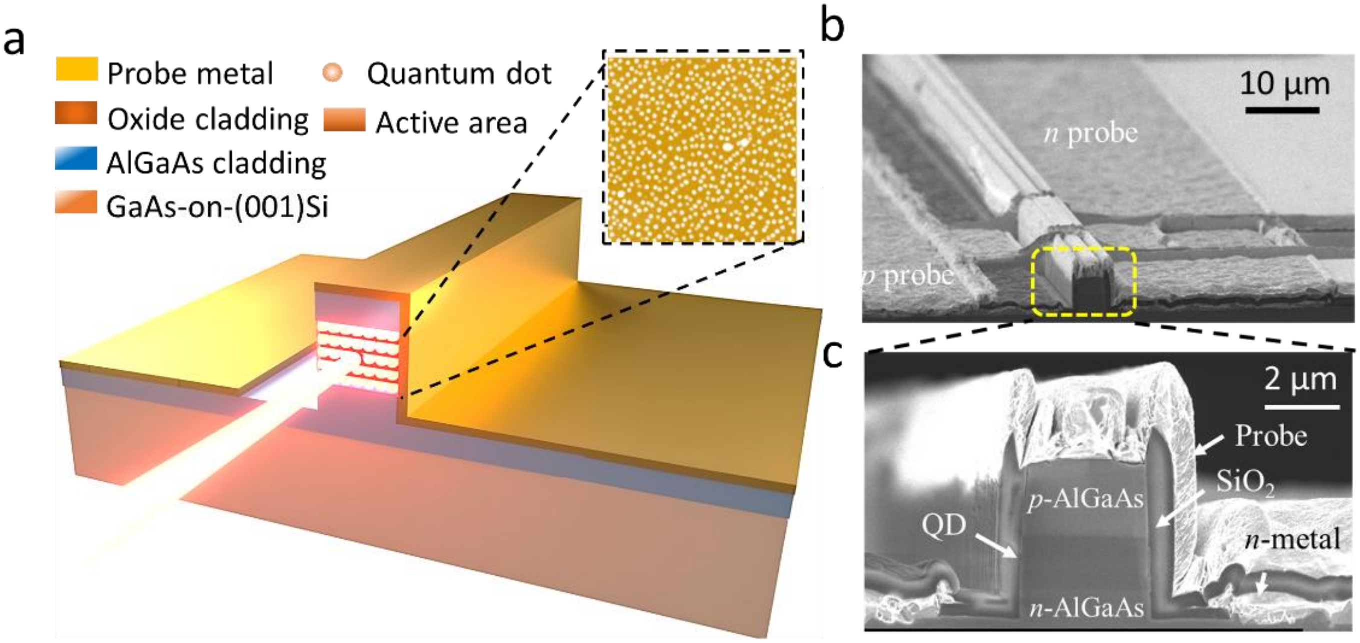

Fig. 2. (a) Schematic image of the laser cross-section, revealing the geometry of the contact and probe metals. Inset: AFM of the dot morphology, showing a dot density of 5×10^{10} cm^{-2}. The image has a size of 1 × 1 μm^2. (b) and (c) SEM image of the cross-section of an as-cleaved laser, tilted at 75º.

GaAs. Further surface treatment with H_2 ambient is expected to reduce the offcut angle to 0.15°[12]. A GaAs nucleation layer was first deposited at a temperature of 400 °C, followed by a 1.1 µm thick GaAs buffer grown at step increased temperatures from 550 to 600 °C. While APBs still appeared at the early stage of the GaAs/Si hetero-epitaxy, they completely vanished with ~300 nm GaAs overgrown layer on Si [30]. This result coincides with the experimental observation from Alcotte *et al.* that APB-free III-V epilayers can be grown on Si (001) substrates by careful treating of Si (001) with a slight misorientation (< 0.5°) prior to III-V nucleation [12]. Thermal cycle annealing was then introduced, where cycling stresses promote dislocations to glide and increase the likelihood of interaction with neighboring dislocations and annihilation. To further reduce the dislocations, two sets of strained-layer superlattices (SLSs) consisting of ten periods of 10-nm $In_{0.15}Ga_{0.85}As$/10-nm GaAs were inserted, separated by a 400 nm GaAs spacer. The SLS drive TDs to form misfit segments and glide along the strained interface. This effect is shown in the cross-sectional transmission electron microscopy (XTEM) image in Fig. 1(d). An atomic force microscopy (AFM) image of the 3.1-µm MOCVD buffer is shown in Fig. 1(b), showing a root-mean-square (RMS) value of 2.26 nm across a scan area of 10 × 10 µm^2. Electron channeling contrast imaging (ECCI) was used to assess the defect densities, as shown in Fig. 1(c). In the image, the pinpoints of bright contrast indicate threading dislocations intersecting the surface. By counting the defects, a low TDD of 3×10^7 cm^{-2} was obtained.

After the ECCI measurement, the template was loaded back to the MBE chamber to grow a $GaAs/Al_xGa_{1-x}As$ graded index separate confinement heterostructure (GRINSCH) laser with five stacks of QD layers as the active region [25]. An AFM image of the uncapped InAs QDs is shown in the inset in Fig. 2(a), showing a dot density of 5×10^{10} cm^{-2}. This corresponds to only one threading location per 1667 QDs, and thus only a limited amount of QDs are directly affected by the contact with the TDs. The as-grown material was then processed into deeply etched ridge waveguide lasers with varying stripe widths using standard dry etching and metallization techniques. Right after the ridge was patterned, the sample went through the first passivation step consisting of 12 nm atomic-layer deposited (ALD) Al_2O_3 and 500 nm plasma enhanced chemical vapor deposition (PECVD) SiO_2. After the metal-contact area was opened, a Pd/Ti/Pd/Au *p*-contact was deposited on top of the etched mesa, and an Pd/Ge/Au *n*-contact metal was deposited on the exposed *n*-GaAs layers. The device then went through a second passivation step with PECVD SiO_2 as an electrical isolation layer. Vias were subsequently opened to the contacts prior to the deposition of Ti/Au probe metal. After thinning the silicon substrate to ~120 µm, the laser facets were formed by cleaving with no facet coating applied to the surface. Schematic and scanning electron microscope (SEM) images of the cleaved cross-section of the finished devices are shown in Fig. 2. The devices were then mounted on copper heatsinks and all laser

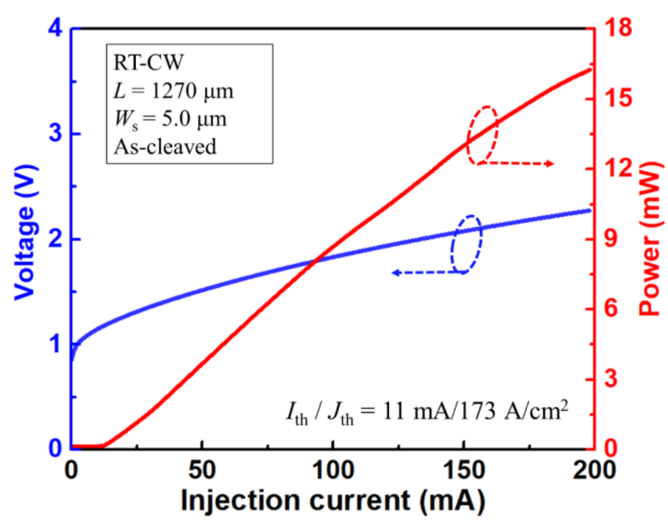

Fig. 3. Typical L-I-V characteristics of an as-cleaved laser with a cavity length of 1270 µm and a ridge width of 5 µm.

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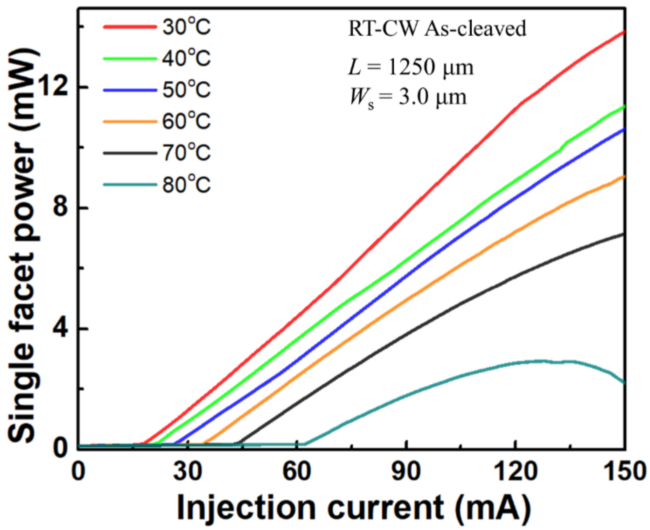

Fig. 4. High temperature measurements of a device with 3×1250 μm^2 cavity, showing lasing up to 80 °C under cw operation.

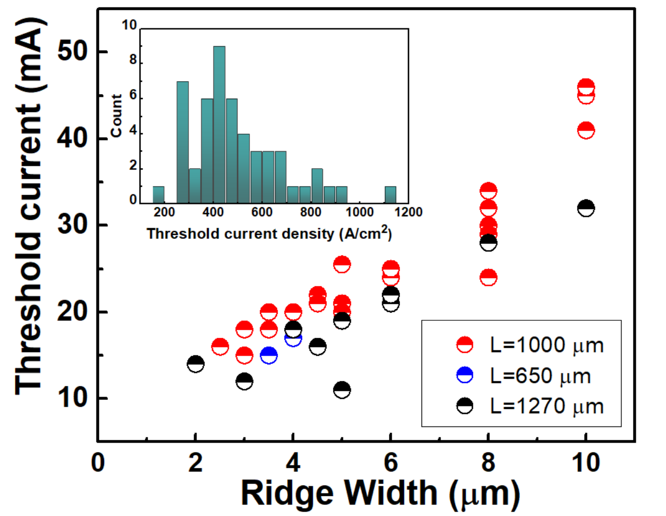

Fig. 6. Threshold current for all lasers of varying ridge width and length is plotted. A continuous decrease of threshold current with reduced ridge width is observed, indicating good suppression of side-wall recombination. Inset: current density distribution histogram for all measured lasers. The smallest value is 173 A/cm^2.

performance measurements described in this report were carried out in the cw mode.

III. Results and Discussion

Fig. 3 shows representative light–current–voltage (LIV) characteristics of a laser with a 1270 μm cavity length and 5 μm ridge width. A threshold current of 11 mA was measured and the device shows a continuous wave operation to current values as high as 18 times threshold, with no sign of performance degradation and power roll-off. The low threshold current density of 173 A/cm^2, which corresponds to 34.6 A/cm^2 for each of the five QD layers, is comparable to the best reported values of QD lasers grown on on-axis (001) Si (33 A/cm^2 per layer for a four-QD-layer lasers [19]), and QD lasers grown on native substrates (32.5 A/cm^2 per layer for a three-QD-layer lasers [32] and 10.5 A/cm^2 per layer for a single-QD-layer laser [33]).

For most datacom applications, it is desirable for the laser to achieve efficient continuous wave operation at room temperature and above (up to 80 °C), with low thresholds (down to a few to tens of mA), and reasonable output powers (1–10 mW) [34]. A device with 3×1250 μm^2 cavity was tested at elevated temperatures as shown in in Fig. 4. The laser was able to function up to 80 °C under cw operation, still producing an output power of 2.8 mW. This result matches that of our lasers on V-grooved Si templates [25], outperforms other 1.3 μm lasers grown directly on (001) Si (operate up to 36°C under cw injection [13]), represents the highest demonstrated O-band cw lasing temperature of epitaxial laser grown directly on Si without a Ge or GaP interlayer, miscut or otherwise, and compares favorably to the best heterogeneously integrated QD lasers on Si without packaging, which operate cw up to 100°C [35]. This demonstrates that QD lasers grown on unpatterned quasi-nominal (001) Si could potentially compete with those grown on more complicated designs, waiving the trouble of selective etching the patterned Si or the cost of growing a well-engineered thin GaP or Ge layer on Si.

The slope efficiency and natural logarithm of threshold current versus stage temperature for the same device is shown

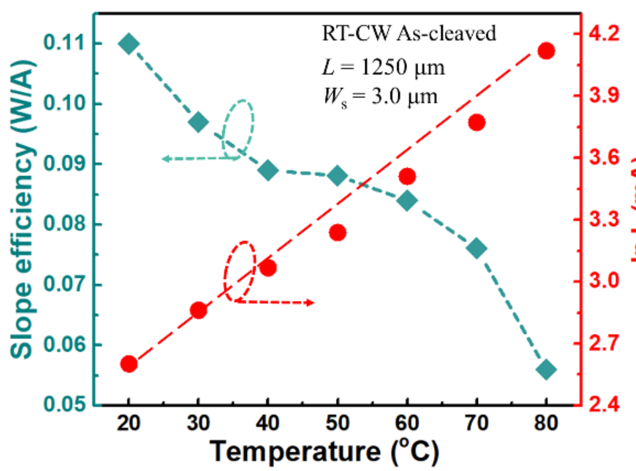

Fig. 5. Slope efficiency and natural logarithm of threshold current versus stage temperature of a device with 3×1250 μm^2 cavity. The dashed red line represents linear fitting to the experimental data.

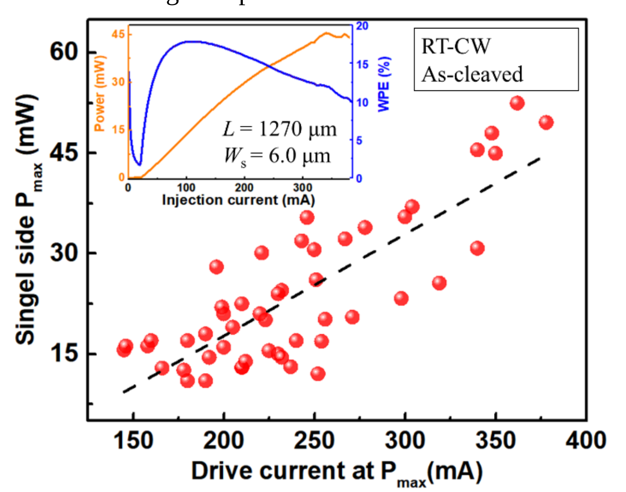

Fig. 7. Maximum cw output power versus corresponding drive current. The dashed line represents the best fit with slope of 0.153 W/A.

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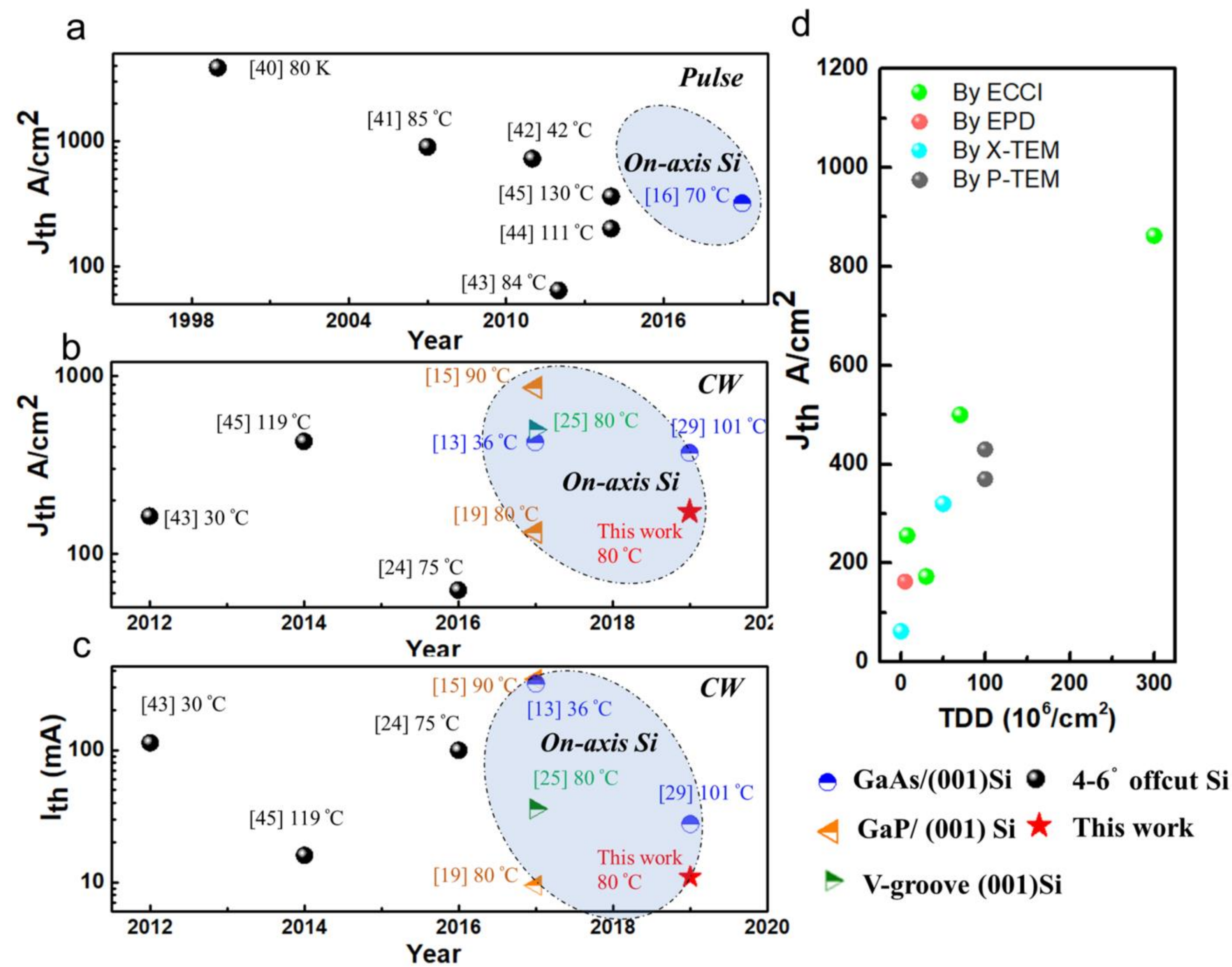

Fig. 8. (a) Chronological evolution of InAs/GaAs quantum dot lasers epitaxially grown on Si in terms of threshold current density reduction and increase in maximum lasing temperature. (b) The dependency of threshold current density on TDD for cw lasers.

in Fig. 5. The dependence of threshold current on temperature follows the exponential function of $I_{th} \propto \exp\left(\frac{T}{T_0}\right)$. The characteristic temperature is 41 K, which is typical for an undoped active region [24, 25]. Note that the T_0 here was extracted under cw excitation, and thus is an underestimated value due to self-heating effects. To date, temperature invariant operation ($T_0 = \infty$) in a range of 5-70 °C [36] and maximum operating temperature up to 220 °C [37] have been demonstrated for the state-of-art native III-V QD lasers. It is anticipated that well-established approaches using modulation *p*-doping of the QDs [20], tunnel-injection designs [38], and hard soldering the laser to a high-thermal-conductivity heatsink will further reduce the temperature sensitivity and improve the extraction of heat from the active region.

Fig. 6 shows a continuously decreasing trend of threshold current as the ridge width narrows over the entire range of ridge widths studied. In the inset of Fig. 6, threshold current density is plotted for all devices as a histogram, showing a peaked distribution around 350-450 A/cm^2 and a lowest value of 173 A/cm^2. By utilizing a QD active region instead of its QW counterpart, the carrier diffusion length is reduced from 3 to 5 μm to below 1 μm. The same property that reduces sensitivity to dislocations during III-V/Si epitaxy, also reduces sensitivity to recombination at device sidewalls [39]. As devices shrink, the effects of surfaces, which act as extended planar defects, won't serve as strongly as a detrimental effect allowing further reduction of device size for the realization of low cost, size, weight, and power (cSWaP) photonic integrated transmitters.

In Fig. 7, the maximum single-side peak output power (the roll-over inflection point in the LI curve) is plotted as a function of corresponding drive currents. Devices of all sizes routinely put out a few tens of milliwatts of output power, with a maximum single-side output power of 52 mW achieved by an 8×1000 μm^2 ridge, and a maximum wall-plug-efficiency (WPE) of 17.8% by a 6×1270 μm^2 ridge (inset in Fig. 7). The slopes of the best fit line of 0.153 W/A acts as a conservative estimate of the average slope efficiency for our devices. It should be mentioned that appropriate dielectric coatings and facet passivation can further increase the output power of the device.

Fig. 8 (a)-(c) and Table 1 present the recent progress in threshold current/current density reduction as well as maximum lasing temperature improvement for Fabry-Perot type lasers with a QD active region grown on Si. The performance of III–

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TABLE I
BENCHMARKING OF VARIOUS MONOLITHIC III-V HETERO-EPITAXY ON SI

	Year	**I_{th}(mA)/ J_{th}(A/cm^2)**	**Max T (^{o}C)**	**Size (μm^2)**	**Laser type**	***TDD* *(cm^{-2})***	**λ (μm)**	**substrate**	**Ref**
	1999	788/3850	NA	800×50	FP(pulse, as cleaved)	*NA*	1	**2° offcut**	[40]
	2007	432/900	85	600×80	FP(pulse, as cleaved)	*2-5×10^7 (X-TEM)*	1	**4° offcut**	[41]
pulse	**2011**	1087.5/725	42	3000×50	FP(pulse, as cleaved)	*NA*	1.3	**4° offcut**	[42]
	2012	45/64.3	84	3500×20	FP(pulse, as cleaved)	*5×10^6 (EPDs)*	1.28	**6° offcut with Ge buffer**	[43]
	2014	150/200	111	3000×25	FP(pulse, as cleaved)	*3-5×10^6 (EPDs)*	1.25	**4° offcut**	[44]
	2014	18/362	130	(700-1200)×(4-12)	FP(pulse HR coated)	*~10^8 (P-TEM)*	1.25	**6° offcut with Ge buffer**	[45]
	2012	114/163	30	3500×20	FP(cw, as cleaved)	*5×10^6 (EPDs)*	1.28	**6° offcut with Ge buffer**	[43]
	2014	16/430	119	(700-1200)×(4-12)	FP(cw, HR coated)	*~10^8 (P-TEM)*	1.25	**6° offcut with Ge buffer**	[45]
	2016	100/62.5	75	3200×50	FP(cw, as-cleaved)	*~10^5 (X-TEM)*	1.3	**4° offcut**	[24]
	2017	345/862	90	2000×20	FP(cw, as-cleaved)	*3×10^8 (ECCI)*	1.28	**on-axis Si with GaP buffer**	[15]
	2017	36/500	80	1200×6	FP(cw, HR coated)	*7×10^7 (ECCI)*	1.25	**on-axis Si with v-grooves**	[25]
	2017	9.5/256 27.5/132	80	1485×2.5 2600×8	FP(cw, HR coated)	*7.3×10^6 (ECCI)*	1.27	**on-axis Si with GaP buffer**	[19]
On-axis	**2017**	319/425	36	3000×25	FP(cw, as-cleaved)	*NA*	1.29	**Planar on-axis Si with no interlayer**	[13]
	2019	512/320	70	2000×80	FP(pulse, as-cleaved)	*5×10^7 (X-TEM)*	1.25	**Planar on-axis Si with no interlayer**	[16]
	2019	27.6/370	101	1100×7	FP(cw, as-cleaved)	*1×10^8(P-TEM)*	1.22	**Planar on-axis Si with no interlayer**	[29]
	2019	11/173	80	1270×6	FP(cw, as-cleaved)	*3×10^7 (ECCI)*	1.27	**Nominal (001) Si with planar surface with no interlayer**	This work

V QD lasers grown on silicon is progressing rapidly leading to impressive results in material quality and record setting device performance: cw lasing up to 119°C and threshold current density down to 62.5 A/cm^2, exceeding what has been achieved through heterogeneous integration without packaging. Starting from 2016, efforts have doubled down on developing CMOS compatible, epitaxial material platforms on Si. Of all the lasers grown directly on on-axis (001) Si, the threshold current density of laser in this work stays among the lowest values. In Fig. 8(d), threshold current density of lasers operated under cw injection is plotted as a function of TDD and are classified in three groups depending on the characterization methods: cross-sectional/plan-view TEM, ECCI, and etch pit density (EPD). While the threshold current density shows correlation with TDD, the dependency becomes less strong when TDD is below 1×10^8 cm^{-2}. Concerns of direct epitaxy schemes shall be focused more on the economic cost and CMOS compatibility of the substrate type. Since the direct growth of GaAs on unpatterned quasi-nominal (001) Si technique eliminates the necessity of using intermediate GaP/Ge buffer layers, substrate patterning, or offcut, this epitaxial scheme can potentially yield the best material quality at the lowest lifecycle cost.

IV. CONCLUSION

In conclusion, we demonstrate APB-free epitaxial GaAs film directly on unpatterned quasi-nominal (001) Si. Room-temperature cw lasing at ~1.3 μm has been achieved, with a minimum threshold current density of 34.6 A/cm^2 per layer, a maximum cw operating temperature of 80 °C, and single facet output power of 52 mW. Compared to other monolithic III-V hetero-epitaxy schemes on Si, the direct growth on unpatterned quasi-nominal (001) Si technique gives rise to exceptional device performance without Ge or GaP interlayers, substrate patterning, miscut or otherwise, and compare favorably to the best heterogeneously integrated quantum dot lasers on Si [35]. These devices are scheduled for aging at elevated temperatures and current densities to directly evaluate their suitability in realistic datacenter and HPC environments. The unpatterned growth technique shall significantly de-risk the technology from a performance standpoint, warranting discussion for more advanced photonic integration.

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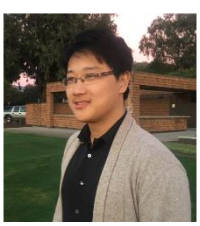

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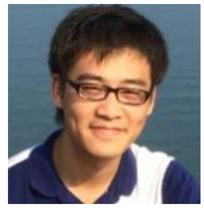

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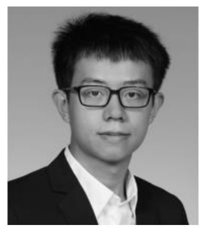

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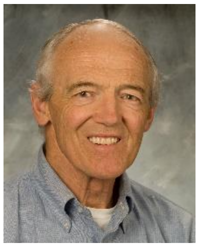

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