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Protection for Submodule Overvoltage caused by Converter Valve-Side Single-Phase-to-Ground Faults in FB-MMC based Bipolar HVDC Systems

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***Abstract*—One of the most critical faults affecting modular multilevel converter (MMC) based bipolar high-voltage direct-current (HVDC) transmission systems is the single-phase-to-ground (SPG) faults between the converter transformer and the valve. However, half-bridge (HB) and full-bridge (FB) based MMCs exhibit a different behavior following such a fault and, thus, converter protection should be addressed in a different manner for each configuration. For HB-MMCs, an SPG fault at the valve-side leads to a severe overvoltage on the submodule (SM) capacitors in the converter upper arms and to grid-side non-zero crossing currents. Although FB-MMCs only exhibit overvoltage, these are more severe than for their HB counterparts. To address this problem, this paper presents a protection strategy considering thyristor bypass branches placed in parallel with upper arms of FB-MMCs. By employing this configuration, the upper arm overvoltage in the faulted converter is mitigated and remote converters can be quickly blocked using their local protection schemes. For completeness, the effectiveness of the strategy is verified through time-domain simulations in PSCAD/ EMTDC. The studies in this paper demonstrate the effectiveness of the presented protection scheme for station internal faults occurring in FB-MMCs in bipolar HVDC systems.**

***Index Terms*—Modular multilevel converter, high-voltage direct-current systems, converter valve-side fault, single-phase-to-ground fault, overvoltage, protection, thyristors.**

I. Introduction

In recent years, the voltage source converter (VSC) based high-voltage direct-current (HVDC) technology, especially the modular multilevel converter (MMC) based HVDC, has attracted considerably more attention for renewable energy integration and multi-terminal applications compared to line commutated converter (LCC) based HVDC [1]-[3]. Thanks to their distinctive features, such as the modularity and scalability to different voltage/power levels, high efficiency, and superior harmonic performance [4]-[6], the MMC-HVDC technology has been planned for systems of high capacity and high dc voltage level. Examples include the Zhangbei four-terminal ±500 kV HVDC grid [7] and the Kun-Liu-Long three-terminal ±800 kV hybrid LCC/MMC ultra HVDC project [4].

Although the MMC-HVDC technology has achieved a high degree of maturity, system protection and fault tolerant operation remain as outstanding challenges [8]-[9]. However, significant research has been conducted in these areas to facilitate its widespread deployment. For instance, various HVDC circuit breakers (DCCBs) [10] and MMC topologies with dc fault blocking capability [11]-[12] have been developed to isolate faulted dc zones. DC fault protection methods for MMC-HVDC systems have been proposed in [1], [13]-[14]. The modeling and control of MMCs subject to unbalanced ac faults at the converter grid-side have been investigated in [15]-[16]. Despite such valuable contributions to the open literature, the protection for converter valve-side single-phase-to-ground (SPG) faults in bipolar MMC-HVDC systems has not attracted sufficient attention. Although the probability of the occurrence of this type of faults is low, their severe consequences should be considered in the design of protection schemes.

Valve-side SPG faults are normally permanent as they are usually caused by insulation failure and flashover of converter ac bus wall bushings [17]-[18]. In half-bridge (HB) MMC based bipolar systems, this type of faults will lead to overvoltage in the submodule (SM) capacitors in the upper arms of the converter and to grid-side non-zero crossing currents [19]-[22]. The upper arm SM capacitors are charged under the dc voltage and the negative half-cycles of the valve-side post-fault ac voltages. The non-zero crossing currents are caused by the constant uncontrolled coupling of the dc-side to the ac-side via the free-wheeling diodes of the arms connecting to the ground. In [21], an *LR* parallel circuit is employed as a converter dc-side grounding to relieve the issues associated with non-zero crossing currents. However, FB-based MMCs require an alternative solution as their fault characteristics differ from HB-based MMCs.

FB-MMC based bipolar HVDC systems do not exhibit grid-side non-zero crossing currents. This is because all the diodes

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in the lower arms will be reversed-biased thanks to the configuration of the FB-SMs. However, the FB-MMC will also suffer from the upper arm overvoltage problem—which is more severe than for HB-MMC topologies because of the higher valve-side post-fault ac voltages [19], [23]. Such an overvoltage may threaten the insulation of the SM devices. To address this issue, reference [19] recommends increasing the voltage rating of FB-SMs to withstand the overvoltage. However, such an approach would increase capital costs, while the devices would still face risks associated with overcurrent and overvoltage.

Surge arresters can be deployed in parallel with each arm to clamp the overvoltage. However, these devices can only limit the voltage to around 1.7 p.u. and overvoltage may still exist [19]. A protection strategy for FB-MMCs that regulates the dc terminal voltage to zero to relieve the overvoltage has been proposed in [23]. However, as an SPG occurs close to the valve, the arm currents will immediately increase to intolerable levels. In this scenario, the insulated-gate bipolar transistors (IGBTs) will be quickly blocked by their internal overcurrent protection. Therefore, this protection strategy may damage the IGBTs before completing the fault discrimination process and triggering the control strategy. Although the remote converter may be able to switch to regulate the dc voltage to zero to alleviate the overvoltage, the control signal must be based on the communication system—which cannot be achieved if the communication system is out of service.

Converter-embedded devices, such as bypass thyristors installed with HB-SMs, have been employed in real industrial applications to protect the HB-MMCs upon dc-side faults [1], [24]-[25]. In [26], a double-thyristor branch is installed in each arm of FB-MMCs to achieve high-efficient operation and dc fault protection capability. However, the use of the thyristor bypass branches to protect the overvoltage caused by valve-side SPG faults in FB-MMCs is still an under-researched topic.

This paper bridges the aforementioned research gap by analyzing in detail the effect of valve-side SPG faults in FB-MMC bipolar configurations. Emphasis is made on the overvoltage exhibited by the SM capacitors in the upper arms. A protection strategy employing double-thyristor bypass branches is presented. The thyristors are installed in the terminals of each upper arm and will be triggered once the converter is blocked following the detection of the fault. This way, the upper arms are bypassed and the overvoltage can be eliminated. Although a dc terminal short-circuit is created, the short-circuit current will only flow through the triggered thyristors. This is not an issue as thyristors can withstand large surge currents. Moreover, a remote converter can detect this dc short-circuit and block its IGBTs immediately using its local protection instead of depending on communication.

The protection strategy presented in this work has been assessed via time-domain simulations conducted in PSCAD/EMTDC. Results show that the protection strategy works effectively to eliminate the overvoltage.

II. Analysis of Valve-Side SPG Faults

For the work carried out in this paper, it is assumed that both poles of a bipolar MMC-HVDC system are symmetrical and controlled independently [27]. Findings and conclusions are made for the positive pole only but are equivalently applicable to the negative pole.

A. Upper Arm Overvoltage

Fig. 1(a) shows the positive pole of a bipolar FB-MMC system. Each phase of the converter consists of one upper and one lower arm. Each arm has N series-connected FB-SMs and one inductor L. The equivalent circuit resistance is represented by resistor R. Each SM contains four IGBTs, four diodes and one capacitor. Since a delta/star transformer connection with a grid-side neutral grounding is widely used in HVDC systems [28]-[29], this type of transformer is adopted in this paper.

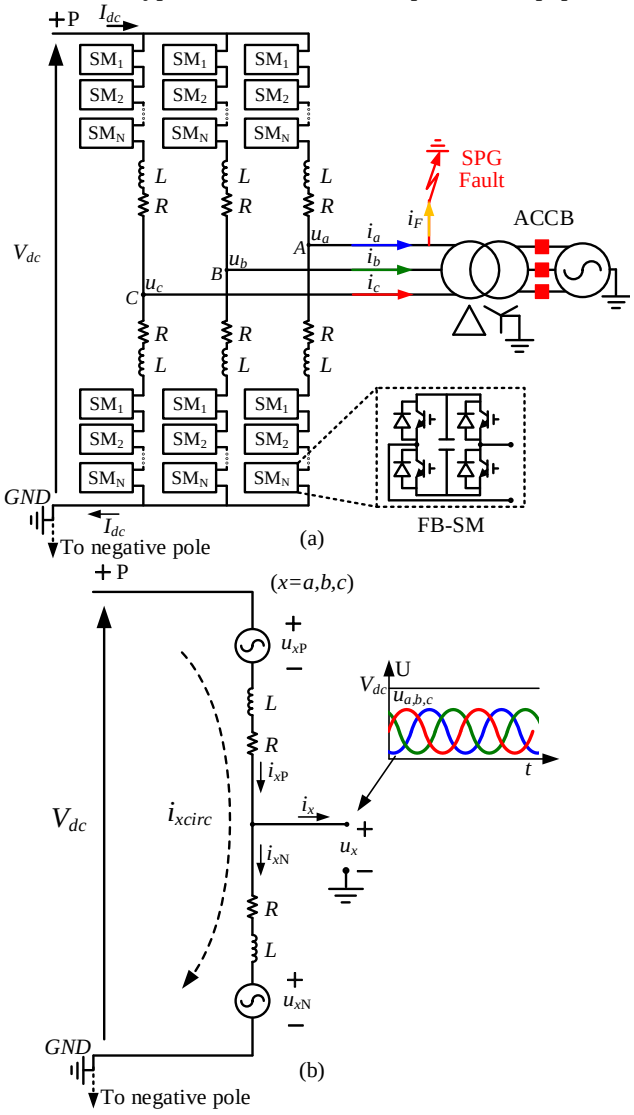

Fig. 1. Positive pole of a bipolar FB-MMC. (a) Converter topology. (b) Single-phase equivalent circuit.

Fig. 1(b) illustrates the single-phase equivalent circuit of the converter, where V_{dc} is the dc voltage, u_x the valve-side phase-to-ground voltage, i_x the phase current, u_{xP} and u_{xN} the voltages produced by SMs in the upper and lower arms, i_{xP} and i_{xN} the arm currents, and i_{xcirc} the circulating current, which can be reduced to a very low value using damping controllers [30]. If the circulating current i_{xcirc} is ignored, the valve-side ac phase voltages can be expressed as:

$$u_x = -\frac{1}{2}L\frac{di_x}{dt} - \frac{1}{2}Ri_x + \frac{u_{x\mathrm{N}} - u_{x\mathrm{P}}}{2} + \frac{1}{2}V_{dc}, \quad (x = a,b,c) \quad (1)$$

The voltage produced by the upper and lower arms $u_{x\mathrm{P}}$ and $u_{x\mathrm{N}}$ can be expressed as:

$$\begin{cases} u_{x\mathrm{P}} = \frac{1}{2}V_{dc}m[\sin(\omega t + \theta_x) + 1] \\ u_{x\mathrm{N}} = \frac{1}{2}V_{dc}m[1 - \sin(\omega t + \theta_x)] \end{cases}, \quad (x = a,b,c) \quad (2)$$

where θ_x is the phase angle and m is the modulation index. The following equation can be obtained by substituting (2) into (1) and ignoring the voltage drop in the arm inductor and resistor:

$$u_x \approx \frac{1}{2}V_{dc}\left[1 - m\sin(\omega t + \theta_x)\right], \quad (x = a,b,c; 0 < m \le 1) \quad (3)$$

It can be seen from (3) that the ac phase voltages are always positive during normal operation, as illustrated by $u_{a,b,c}$ in Fig. 1(b). The reason behind this phenomenon is that the valve-side voltage reference is clamped by the dc grounding of the converter. If the converter is over-modulated (i.e. $m > 1$), the ac phase voltages will show negative values. However, there is still a large dc component in the voltages.

As the SPG fault occurs close to the valve, the IGBTs will immediately experience large fault currents. To protect the converter, the IGBTs will be blocked by the local protection scheme of the converter. As a result, the converter becomes an uncontrollable diode bridge, as shown in Fig. 2.

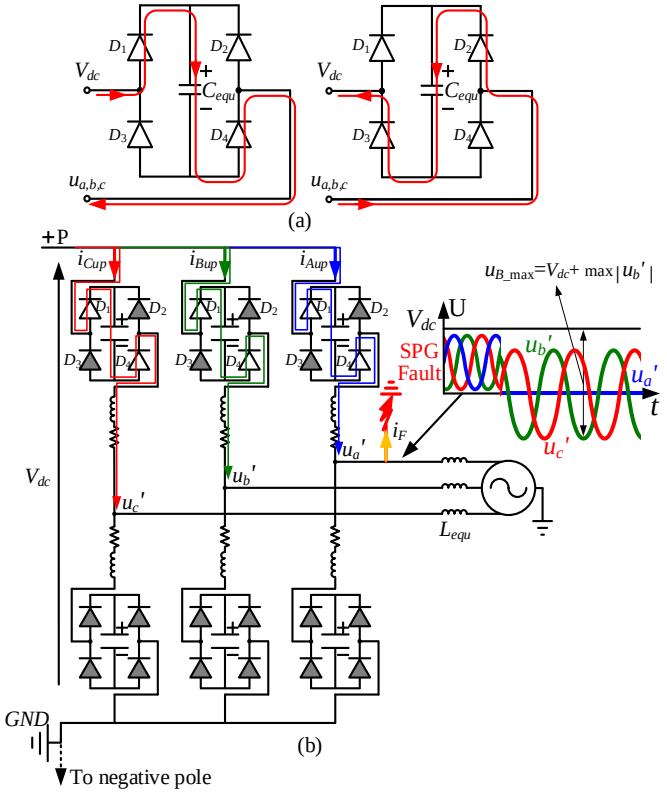

Fig. 2. Equivalent circuits of a blocked FB-MMC in the positive pole. (a) Possible current paths in a blocked FB-SM. (b) Single-phase equivalent circuit.

Fig. 2(a) illustrates the equivalent circuit of one arm of the blocked FB-MMC, where C_{equ} is the equivalent capacitor of all SM capacitors in the arm. It can be observed that C_{equ} cannot discharge when the converter is blocked; however, it can be charged by bidirectional currents.

Fig. 2(b) illustrates the equivalent circuit of a blocked converter during a valve-side SPG fault occurring at phase *A*. It should be emphasized that, as the three phases are symmetrical, the analysis presented for a fault at phase A would also apply to the other two phases should the fault occur in any of them. The faulted phase voltage drops to zero immediately after the fault. Due to the valve-side delta connection of the transformer, the voltages of the two non-faulted phases become the line voltages. Moreover, before blocking the converter, the sum of the total voltage of all SM capacitors in each arm is approximately equal to V_{dc}, which is a higher value compared to the valve-side line voltages, as shown in Fig. 2(b). Therefore, all the diodes in the lower arms will be reversed-biased and there will be no fault current in the lower arms. In addition, as the ac buses are isolated from the dc grounding by the blocked lower arms, the dc offset in the two non-faulted phases will no longer exist.

The valve-side post-fault voltages (u_a', u_b' and u_c') are illustrated in Fig. 2(b). It can be seen that the SPG fault results in a zero voltage ($u_a' = 0$ kV) in phase *A*. Since the dc voltage V_{dc} is higher than u_a', diodes D_2 and D_3 will become reversed-biased once the converter is blocked. Diodes D_1 and D_4 will conduct if V_{dc} experiences overvoltage. For instance, a transient overvoltage can be caused in the dc-side of the converter once it is blocked due to the SPG fault. Diodes D_1 and D_4 will be reversed-biased if the dc terminal voltage becomes equal or lower than the total capacitor voltage in the upper arm. Consequently, all upper arm diodes in the faulted phase will be reversed-biased and the capacitor voltages will remain constant.

Similarly, as the post-fault voltages of the two non-faulted phases (u_b' and u_c') are lower than the total capacitor voltage in the two upper arms, diodes D_2 and D_3 in the two non-faulted phases will be reversed-biased as well. However, D_1 and D_4 may conduct during the negative half-cycles of the post-fault ac voltages.

Taking phase *B* as an example, the upper arm capacitors will stop being charged once their total voltage reaches a maximum value, given by

$$u_{B_\max} = V_{dc} + \max|u_b'|, \quad (4)$$

where $\max|u_b'|$ is the peak value of the valve-side post-fault voltage u_b'. Assuming the magnitude of the transformer's valve-side pre-fault phase voltage is U_b, then

$$\max|u_b'| = \sqrt{3}\times\sqrt{2}U_b. \quad (5)$$

The converter modulation index m is defined as

$$m = \frac{2\sqrt{2}U_b}{V_{dc}}. \quad (6)$$

The following equation can be obtained by substituting (5) and (6) into (4):

$$u_{B_\max} = \left(1 + \frac{m\sqrt{3}}{2}\right)V_{dc}. \quad (7)$$

It can be seen from (7) that the SM capacitors in the upper arms of phase *B* will exhibit a large overvoltage. The other non-faulted phase *C* will experience the same overvoltage. Taking

m = 0.9 as an example, the maximum SM voltage will be 1.8V_{dc} approximately, which represents a serious overvoltage magnitude for the devices.

It should be mentioned that the above analysis assumes that the dc terminal voltage of the faulted converter remains constant during the fault. However, the SM overvoltage can be more severe when the dc terminal voltage experiences overvoltage during the transient process caused by the fault.

B. Impact of the Remote Converter on the Faulted Converter

The above discussion does not consider the impact that the remote converter has on the overvoltage seen by the faulted converter. As valve-side SPG faults are usually permanent, the faulted converter needs to be isolated by tripping its grid-side ac circuit breaker (ACCB). The remote converter can be shut down and then switched to a static synchronous compensator (STATCOM) mode. However, the time it would take to stop the power being transmitted from the remote converter will affect the upper arm overvoltage in the faulted converter.

Let us assume that the SPG fault occurs at a power-receiving converter and that the power transmitted from the power-sending converter (i.e. the remote converter) is P. If the power-sending converter takes Δt to block the IGBTs based on either its local protection or a blocking signal received from the faulted converter through communications [31], the voltage change ΔV_{dc} of the upper arm SM capacitors in the faulted converter can be obtained using the following equation:

$$P\Delta t = \frac{3}{2}C_{equ}(V_{dc}+\Delta V_{dc})^2 - \frac{3}{2}C_{equ}V_{dc}{}^2 . \tag{8}$$

As $\Delta V_{dc} << V_{dc}$, the second order terms in (8) can be neglected. Therefore,

$$\Delta V_{dc} = \frac{P\Delta t}{3C_{equ}V_{dc}} . \tag{9}$$

It can be observed from (9) that the higher the transmitting power (P) and the longer the time (Δt) it takes to stop transmitting such power are, the higher the voltage increase of the SM capacitors will be. However, the remote converter may not be able to detect the fault quickly as the overcurrent or voltage change experienced by it may not be enough to reach its protection thresholds—especially for long-distance systems. Under these circumstances, the SM capacitor voltages in the upper arms may reach intolerant levels. Moreover, the system may face the risk of communication failure. A reliable solution is thus needed to successfully relieve this overvoltage problem without relying on communications.

C. Impact of Converter Grounding Schemes on Fault Characteristics

Converter grounding schemes constitute an important aspect of MMC-HVDC transmission systems. Due to the dc offset of the valve-side voltages, an ac-side grounding scheme using a star-point reactor [32] is not suitable for a bipolar configuration. The converter station in bipolar systems can be solidly grounded or grounded through the dc-side impedance [33]. As it can be seen from Fig. 3, there is no current flowing through the lower arms. Therefore, the converter grounding will not affect the fault characteristics.

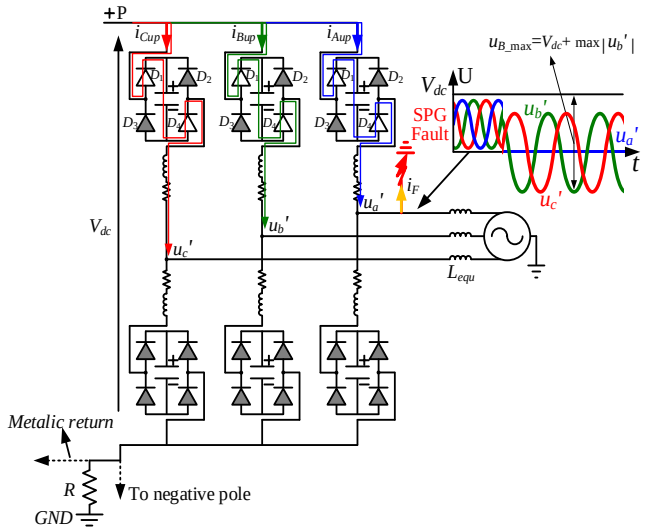

Fig. 3. A blocked converter with a dc-side impedance grounding and a metallic return.

D. Comparison with the Mixed-cell MMC

In [18], a mixed-cell MMC has been proposed to mitigate the SM overvoltage caused by valve-side SPG faults. It uses FB-SMs in the upper arms and HB-SMs in the lower arms, as shown in Fig. 4(a). The equivalent circuit after blocking all IGBTs is shown in Fig. 4(b).

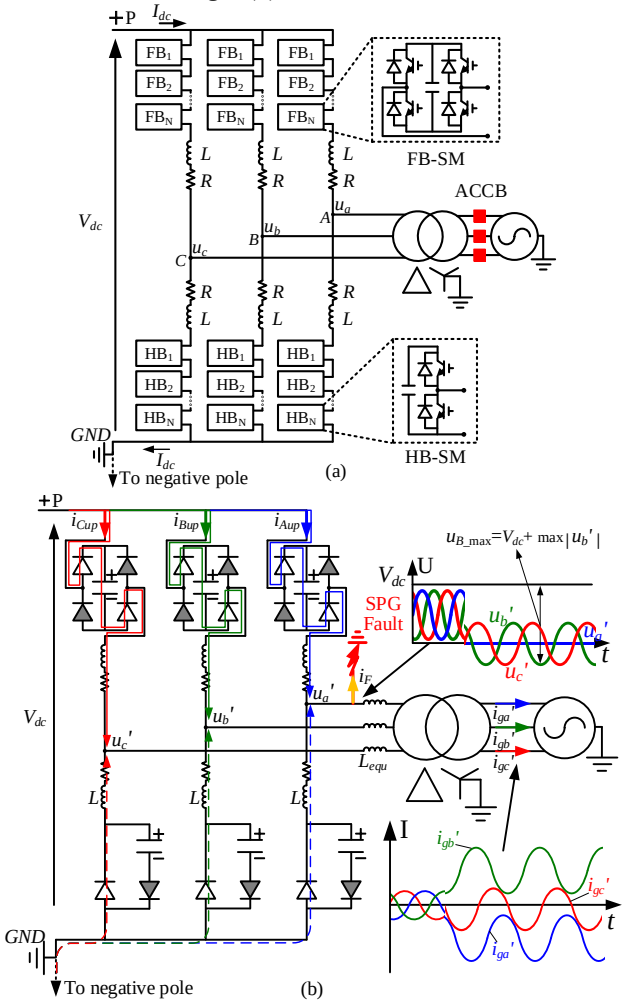

Fig. 4. Topology and equivalent circuit of a mixed-cell MMC. (a) Converter topology. (b) Equivalent circuit of the blocked converter.

Due to the freewheeling diodes in the lower arm HB-SMs, there will be fault currents during every negative half-cycle of the two non-faulted phases. Taking phase b as an example, the peak value of the valve-side post-fault voltage u_b' can be estimated by:

$$\max |u_b'| \approx \sqrt{3}\times\sqrt{2}U_b\times L/(L+L_{equ}). \quad (10)$$

where L_{equ} is the total equivalent reactance of the transformer and the grid-side reactance referred to the valve-side. Then, equation (7) becomes

$$u_{B_\max} \approx \left(1+\frac{m\sqrt{3}}{2}\cdot\frac{L}{L+L_{equ}}\right)V_{dc}. \quad (11)$$

Assuming $L_{equ} \approx 2L$ and $m = 0.9$, the maximum upper arm SM voltage will be $1.26V_{dc}$ approximately. It means that the upper arm overvoltage is reduced from $1.8V_{dc}$ thanks to the deployment of the lower arm HB-SMs, i.e. the same overvoltage level as a conventional HB-MMC [18].

Although this topology can mitigate the presence of overvoltage, it has some inherent drawbacks when compared with the method presented in this paper. For instance, it sacrifices the flexible controllability of an FB-MMC, e.g. the non-blocking dc fault ride-through capability [34]. Furthermore, the constant uncontrolled coupling of the dc-side to the ac-side via the free-wheeling diodes of the lower arm HB-SMs will result in grid-side non-zero-crossing currents, which in turn would need to be mitigated by involving additional devices [20]-[22]. Last but not least, the upper arm capacitors would still face a risk of suffering severe overvoltage.

III. Thyristor-based Protection Strategy

Based on the analysis presented in Section II, a thyristor bypass branch-based protection strategy is presented in this section. The anti-parallel series thyristors-based bypass branches are installed in parallel with converter upper arms, as shown in Fig. 5(a). Press-pack thyristors can be utilized due to their excellent capability to withstand surge currents [24]. As discussed previously, there will be no current in the blocked lower arms. Therefore, thyristors are not required in the lower arms.

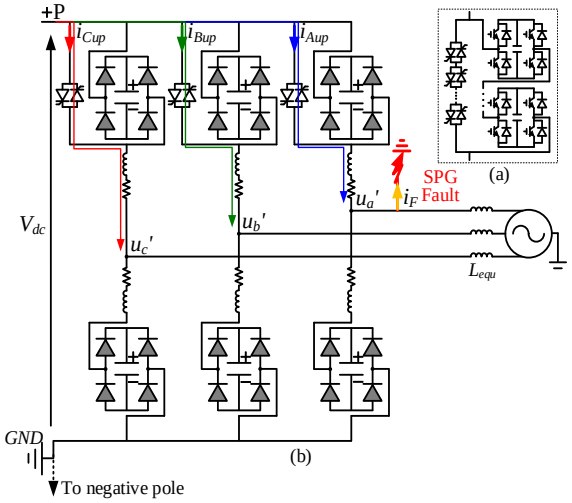

Fig. 5. Topology and equivalent circuit of the proposed FB-MMC. (a) FB-SM with a separate thyristor valve. (b) Equivalent circuit of the blocked converter.

The bypass thyristors are in off-state during normal operation. Once a valve-side SPG is detected, the IGBTs will be blocked immediately. Then, the thyristors will be triggered once fault discrimination is completed. The upper arms will be bypassed immediately once the thyristors are triggered.

The equivalent circuit after triggering the thyristors is illustrated in Fig. 5(b). All the upper arm SMs are bypassed by as a result. Therefore, the overvoltage will no longer exist. However, the triggered thyristors create a three-phase short-circuit at the dc terminal of the converter, as shown in Fig. 5(b).

As the SPG fault has led to a zero voltage in the faulted phase, the triggered thyristors will also create an equivalent pole-to-ground fault at the converter dc terminal. However, the surge currents will only flow through the thyristors—which are able to withstand large currents. It should be also noted that the inductance of the arm inductors and the transformer will limit the overcurrent and the voltage drop in the valve-side and, in turn, in the ac grid. These adverse issues, though, are removed quickly following the triggering of the grid-side ACCB. As suggested in [35], the ACCB interrupting time can be 2-5 line-frequency cycles. In this paper, a conservative 5-cycle (100 ms) has been chosen, which is commonly used in the open literature to test the effectiveness of protection methods (e.g. [1] and [36]). The duration of the created ac short-circuit can be reduced by utilizing an ACCB with a fast fault current interrupting capability. Moreover, as mentioned in Section II-C, there is no fault current flowing through the lower arms and, therefore, the converter grounding will not affect the proposed solution.

To limit the dc short-circuit current caused by the pole-to-ground fault at the faulted converter, the remote converter should be blocked as fast as possible. As this converter is an FB-MMC, its dc-side will be blocked from its ac-side once it is blocked. The dc-side short-circuit current will then stop increasing and will start to decay naturally. Thanks to the voltage drop caused by the triggered thyristors, the remote converter will be able to quickly detect the dc voltage drop or dc overcurrent and then block the IGBTs. A blocking signal will also be sent from the faulted converter to the remote converter through communications to ensure the remote converter can be blocked quickly. It can then switch to a STATCOM mode when it is disconnected from the dc line.

It should be emphasized that the presented method will not affect the high level control strategy (e.g. energy based control or circulating current suppression control) as it will only be triggered once an SPG fault is detected. The protection strategy presented in this section is summarized in Fig. 6.

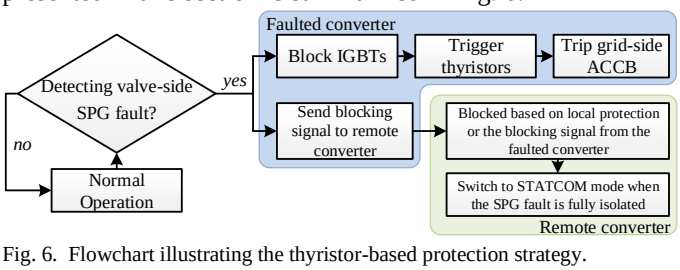

Fig. 6. Flowchart illustrating the thyristor-based protection strategy.

IV. Simulation and Analysis

The analysis and the thyristor-based protection strategy presented in previous sections are verified through simulations in PSCAD/EMTDC.

A. System Modelling

The FB-MMC based bipolar HVDC link shown in Fig. 7 has been implemented in PSCAD. The converter parameters are obtained from the Zhangbei four-terminal ±500 kV HVDC project [7]. Parameters of the overhead line (OHL) model are taken from [37]. The parameters and dimensions of the OHL model are given in the Appendix. The ac systems are modeled as ideal ac sources with short-circuit impedances $R_S + jL_S$. The X_S/R_S and the ac system short-circuit ratio are assumed to be 10. System parameters are provided in Table I. In the system, MMC1 operates in a dc voltage and reactive power control mode and MMC2 operates in an active and reactive power control mode.

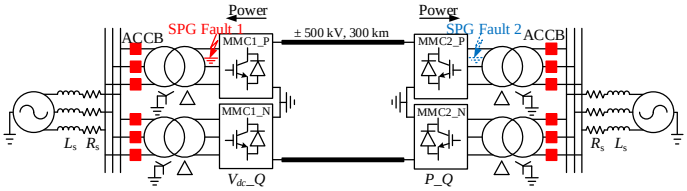

Fig. 7. Bipolar FB-MMC HVDC link.

TABLE I
Parameters of the Bipolar FB-MMC HVDC Link

Parameters	Values
Capacity of each pole (MW)	1500 (1 p.u.)
Rated dc voltage (kV)	±500 (1 p.u.)
Rated ac voltage (kV)	230 (1 p.u.)
AC grid frequency (Hz)	50 (1 p.u.)
Transformer ratio (kV/kV)	260/230 (1.13/1 p.u.)
Transformer leakage reactance (p.u.)	0.15
Number of SMs in each arm	40
DC terminal inductor (H)	0.15
SM capacitance (mF)	2.5
Arm inductance L (H)	0.04 (0.206 p.u.)
Arm resistance R (Ω)	0.1 (0.001 p.u.)
AC system equivalent resistance R_S (Ω)	0.35092 (0.005 p.u.)
AC system equivalent reactor L_S (H)	0.01117 (0.057 p.u.)
Length of the OHL (km)	600

B. Case Studies

1) Upper arm overvoltage

As discussed before, the upper arm overvoltage will be worse if the valve-side SPG fault occurs in a power-receiving converter than in a power-sending converter. However, a power-receiving converter can be in either dc voltage control or power control mode. To investigate the fault characteristics and test the worst possible conditions, valve-side SPG faults are separately set at phase *A* of the positive poles of MMC1 and MMC2 (MMC1_P and MMC2_P) when they operate as the power-receiving end. This is shown in Fig. 7

To show the fault responses under the worst case, a small fault resistance $R_F = 0.001$ Ω is assumed. The SPG fault occurs at t = 2 s. The faulted converter employs an overcurrent protection strategy: the IGBTs will be blocked once any arm current exceeds 4.5 kA. The remote converter remains unblocked.

Fig. 8 illustrates the SM capacitor voltages in the upper and lower arms and valve-side post-fault voltages when the SPG fault occurs at the power-controlling converter (MMC2_P). A full power of 1500 MW is transmitted from MMC1_P to MMC2_P. It can be seen from Fig. 8(a) that the upper arm SM capacitors start being charged once the converter is blocked. The valve-side post-fault voltages u_b' and u_c' exhibit a magnitude of the line voltage (1.73 p.u.). Taking phase *B* as an example, the upper arm SM capacitors are charged during the first two negative cycles of u_b', as illustrated in Fig. 8(a) and 7(c). The voltage stops increasing as it has reached its maximum value (once it is higher than or equal to the voltage difference between the dc terminal and the valve-side post-fault voltage). The upper arm SM capacitors in the faulted phase *A* are also charged as the dc terminal voltage experiences overvoltage. The maximum overvoltage reaches 2.07 p.u. in phase *C*. All lower arm SM voltages remain constant once the converter is blocked, as shown in Fig. 8(b).

Fig. 9 shows the results when the SPG fault occurs at the dc voltage-controlling converter (MMC1_P). A full power of 1500 MW is transmitted from MMC2_P to MMC1_P. Similar to the results shown in Fig. 8(a), the SM voltages start to increase once the converter is blocked [see Fig. 9(a)]. However, the SM voltage keeps being charged. The reason behind this behavior is that although the dc controlling-converter is blocked, the remote power-controlling converter is still able to transmit power to the faulted converter. As discussed in Section II-B, the power transmitted from the remote converter will keep charging the upper arm SM capacitors through the uncontrollable diode bridge. Therefore, the exhibited overvoltage in this case is more severe. For instance, the overvoltage of phase *C* has reached 2.77 p.u. at t = 2.2 s. The voltages will keep increasing if the power transmitted from the remote converter is not stopped. Therefore, the remote converter should be blocked as soon as possible. The lower arm capacitors are not affected by the remote converter and their voltages remain constant once the converter is blocked, as shown in Fig. 9(b).

2) Verification of the proposed protection strategy

To relieve the overvoltage problem experienced upon SPG faults, the double thyristor-based protection strategy has been applied in the two converters of the system shown in Fig. 7—bearing in mind that a detailed algorithm for the discrimination of the discussed SPG fault is out of scope of the paper.

The double thyristors are fired 0.5 ms after blocking the converter to emulate the fault discrimination time. Such a time (within a millisecond) is much shorter than the opening time (in tens milliseconds) of the grid-side ACCB. Therefore, the time delay will not affect the effectiveness of protecting the SM capacitors and the opening of the grid-side ACCB. A tripping signal is also sent to the grid-side ACCB when the converter receives its blocking signal. A 100 ms time delay is used to emulate the operating time of the ACCB [36]-[35]. To investigate the effectiveness of the presented strategy, the blocking signal is not sent to the remote converter through communication. The remote converter is blocked instead using its local protection: a blocking signal will be generated when

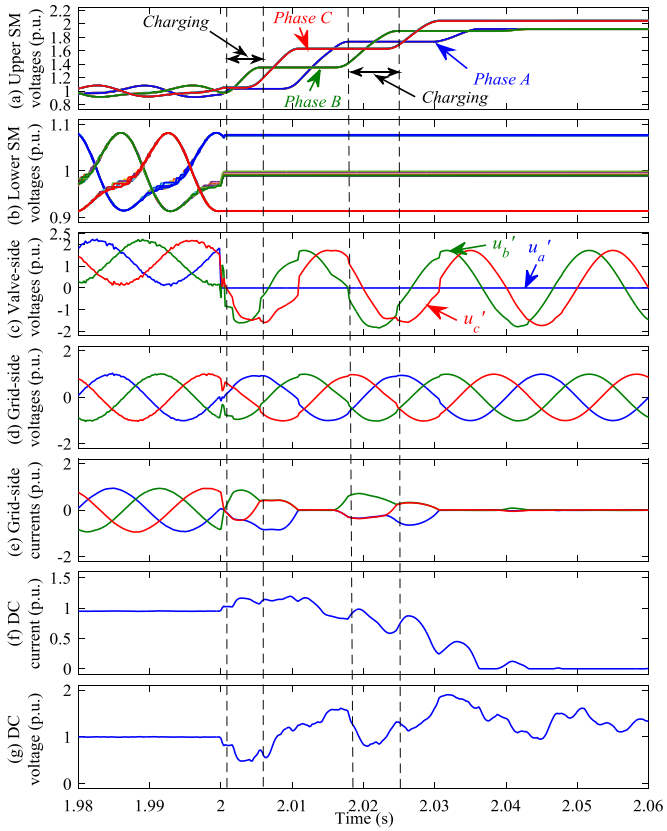

Fig. 8. Fault responses during an SPG fault at MMC2_P. (a) Upper SM voltages; (b) Lower SM voltages; (c) Valve-side voltages; (d) Grid-side voltages; (e) Grid-side currents; (f) DC current; (g) DC voltage.

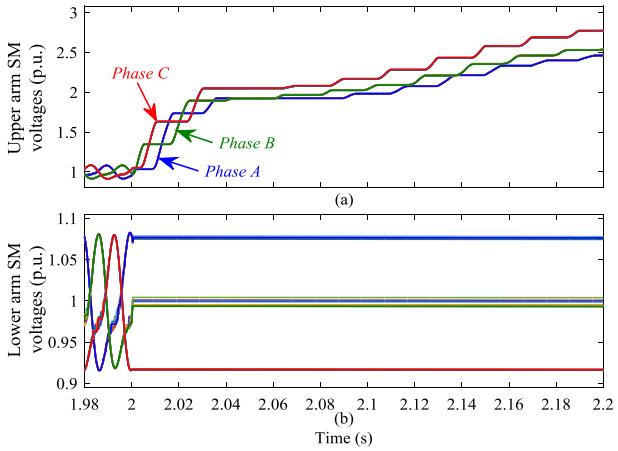

Fig. 9. The SM capacitor voltages during an SPG fault at MMC1_P: (a) Upper arm SM voltages; (b) lower arm SM voltages.

either any arm current exceeds 5 kA or the converter dc terminal voltage is less than 0.8 p.u. or higher than 1.2 p.u. of the rated dc voltage.

As studied previously in Section IV-B, the most serious upper arm overvoltage occurs at the dc voltage-controlling converter when it operates as a power-receiving end. Therefore, results for MMC1_P during a valve-side SPG fault are presented only. Before the fault, MMC1_P receives 1500 MW transmitted from MMC2_P. Relevant plots are shown in Fig. 10.

It can be seen from Fig. 10(a) that the upper arm overvoltage is effectively eliminated by the protection strategy. Although

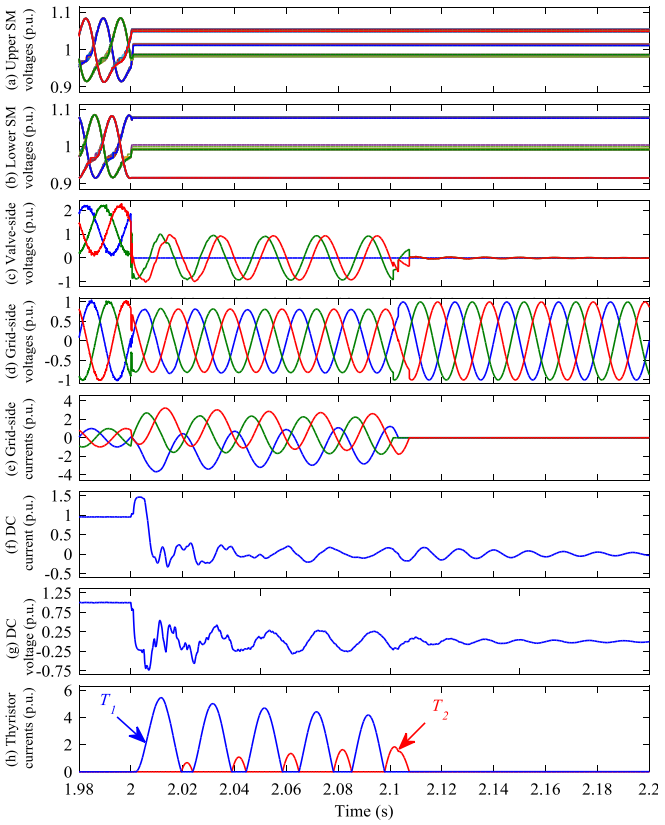

Fig. 10. Simulation results of MMC1_P during an SPG fault when the proposed protection strategy is employed. (a) Upper SM voltages; (b) Lower SM voltages; (c) Valve-side voltages; (d) Grid-side voltages; (e) Grid-side currents; (f) DC current; (g) DC voltage; (h) Thyristor currents.

the triggered thyristors in the upper arms create a three-phase short-circuit at converter valve-side, due to the transformer and the arm inductances, the valve-side post-fault voltages of the two non-faulted phases only drop to 0.92 p.u. [see Fig. 10(c)]. As shown in Fig. 10(d) and Fig. 10(e), the ac grid experiences a voltage drop to 0.82 p.u. and an overcurrent to 3.68 p.u.

However, these are removed quickly once the grid-side ACCB is tripped. Although the triggered thyristors create an equivalent dc-side pole-to-ground fault, the fault current has been limited within 1.46 p.u. [see Fig. 10(f)] as there is no power source once the remote converter is blocked. Then, the dc current naturally decays to zero quickly. Fig. 10(g) shows the currents flowing through the double thyristors in phase *C*. The maximum surge current reaches to 5.45 p.u. in thyristor T_1. These results are relevant as they can be used to select thyristors with suitable I^2t.

3) Comparison with the Mixed-cell MMC

To compare the performance of the method presented in this paper with that implemented for a mixed-cell MMC in [18], the system has been built in PSCAD using the same parameters in Section IV-A. FB-SMs and HB-SMs are used in the upper and lower arms, respectively. The same fault condition as the one studied in Fig. 8 has been tested in the system. Simulation results are shown in Fig. 11.

It can be seen from Fig. 11(a) that the upper arm overvoltage has been mitigated when compared to the results shown in Fig.

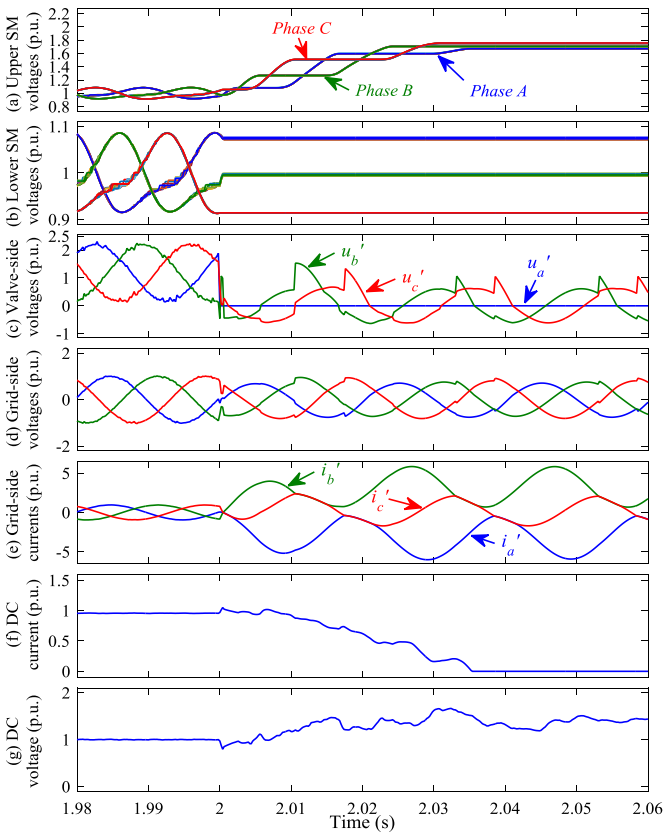

Fig. 11. Fault responses during an SPG fault at MMC2_P of the Mixed-cell MMC. (a) Upper SM voltages; (b) Lower SM voltages; (c) Valve-side voltages; (d) Grid-side voltages; (e) Grid-side currents; (f) DC current; (g) DC voltage.

8(a) due to the lower valve-side post-fault voltages [as shown in Fig. 11(b)]. However, it is observed in Fig. 11(c) that two phases of the grid-side fault currents contain large dc components and exhibit non-zero-crossing. Additional actions should be taken to address this undesirable problem. Otherwise, the grid-side ACCB might not be able to clear such fault currents and in fact may become damaged if no corrective actions are undertaken [21], [38].

V. Conclusion

The converter valve-side SPG fault is one of the most critical faults affecting bipolar HVDC systems. However, its inherent characteristics and corresponding protection against it have not been extensively addressed in the open literature. This paper bridges such research gap by investigating the characteristics of SPG faults at the valve-side of FB-MMCs in bipolar HVDC systems. The studies show that an SPG fault leads to severe overvoltage on the SM capacitors in the upper arms of the converter. Moreover, a power-receiving converter exhibits a more severe overvoltage than a power-sending converter.

To address such issues, a protection strategy using thyristor bypass branches has been presented. The exhibited overvoltage can be effectively eliminated by utilizing the investigated solution—which has been verified through simulations conducted in PSCAD. Although an equivalent dc-side short-circuit is created by the triggered thyristors, the remote converter can be blocked immediately by sensing the short-circuit using its local protection. Since the presented strategy works without relying on communication, this represents an important merit towards its practical deployment.

Appendix

The parameters and dimensions of the OHL used in this paper are shown in Fig. 12.

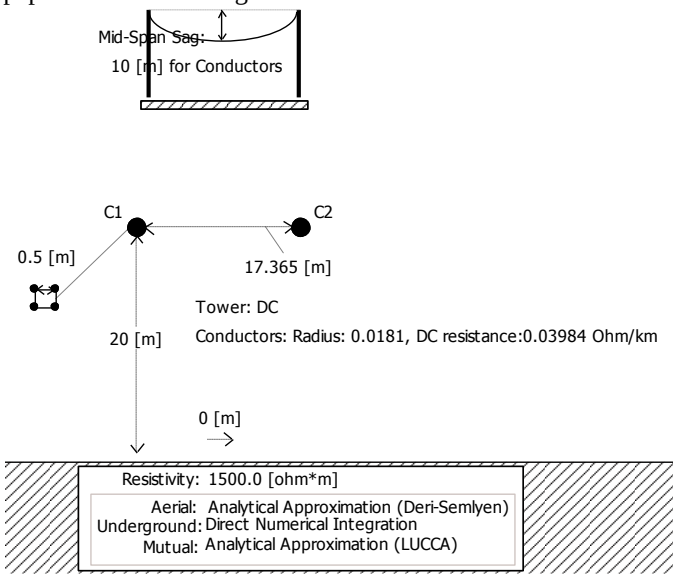

Fig. 12. OHL configuration and dimensions.

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