A Monopolar Symmetrical Hybrid Cascaded DC/DC Converter for HVDC Interconnections

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***Abstract*—With the rapid development of voltage source converter (VSC) based high voltage direct current (HVDC) transmission, it is an irresistible trend that HVDC grid will come into being. High-voltage and high-power DC/DC converters will serve as DC transformers in HVDC grid to interconnect DC lines with different voltage ratings. This paper proposes a monopolar symmetrical DC/DC converter which is composed of cascaded half-bridge sub-modules (SMs) and series-connected IGBTs. This hybrid topology features low capital costs, high efficiency, small footprint, and bidirectional power transfer capability. Operation principle, parameter design, and the control strategies of this topology are introduced. A 480MW, ±500kV/±160kV monopolar symmetrical DC/DC converter is simulated to verify its performance and evaluate the efficiency. In addition, a downscaled prototype rated at 2.4kW, ±300V/±100V has been built and tested. Experimental results further validate the effectiveness of the proposed DC/DC converter.**

***Index Terms*—Monopolar symmetrical DC/DC converter, hybrid topology, DC transformer, HVDC grid.**

I. Introduction

As a milestone achievement in power electronics, modular multilevel converter (MMC) has significantly facilitated voltage source converter (VSC) based high voltage direct current (HVDC) transmission technology [1]-[3]. In the last decade, dozens of MMC-HVDC projects with different voltage ratings have been constructed worldwide. For flexibility and reliability purposes, multi-terminal and meshed HVDC grids have been getting widespread attention of the academia and industry [4]-[9]. In such a trend, DC/DC converter for matching different voltage ratings will be one of the most crucial devices in future HVDC grids.

With regard to HVDC interconnections, DC/DC converters should be scalable up to hundreds of kilovolts and hundreds of megawatts [10]-[12]. Facing the problems of limited semiconductor voltage rating, high d*v*/d*t*, high losses, and large filter size, most of the classic DC/DC converter topologies are not qualified for this application. Enlightened by the MMC concept that using series connection of sub-modules (SMs) to realize efficient high-voltage high-power conversion, modular DC/DC converter topologies have been proposed which can solve the problems. In terms of whether there is galvanic isolation between the DC input and output, these modular DC/DC converters are classified into two categories, namely isolated types [13]-[17] and non-isolated types [18]-[31].

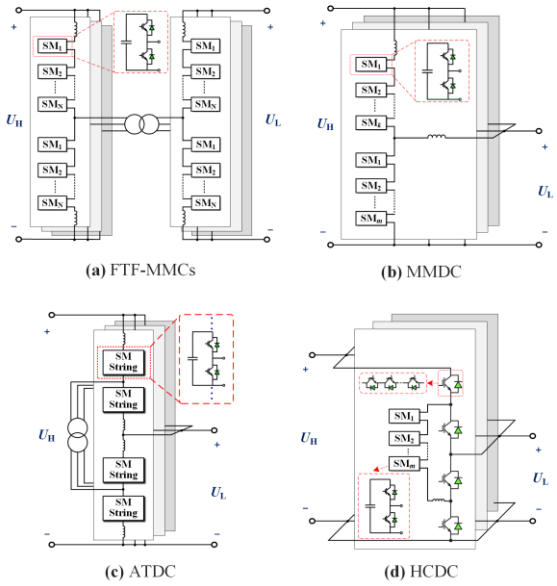

Fig. 1. The existing modular DC/DC topologies for HVDC interconnections.

The most common isolated topology is the front-to-front (FTF)-MMCs shown in Fig. 1(a), which consists of two MMCs and an AC link transformer [13]-[17]. It inherits the distinctive features of MMC and presents good scalability of voltage and power rating. However, there are two power conversion stages, thus it exhibits significant large number of semiconductors, which causes high losses, and requires a full power AC transformer. Using medium-frequency (several hundred Hz) transformer [13]-[14] or trapezoidal-waveform transformer [15]-[17] can help shrink the size and weight of the AC transformer, but this is at the expense of much more difficult insulation and cooling design on account of the induced eddy-current losses in magnetic core as well as the windings. In summary, the FTF-MMCs are not suitable for HVDC interconnections with similar voltage rating but more viable for conversion between high-voltage and medium-voltage systems which has a high DC voltage ratio [10].

As for low (1<ratio≤1.5) and medium (1.5<ratio≤5) voltage ratio connections, non-isolated topologies are more attractive. Compared with the FTF-MMCs, modular multilevel DC/DC converter (MMDC) topologies [18]-[24] have been proposed which have only one conversion stage and do not need the AC link transformer. As shown in Fig. 1(b), part of its SMs can be

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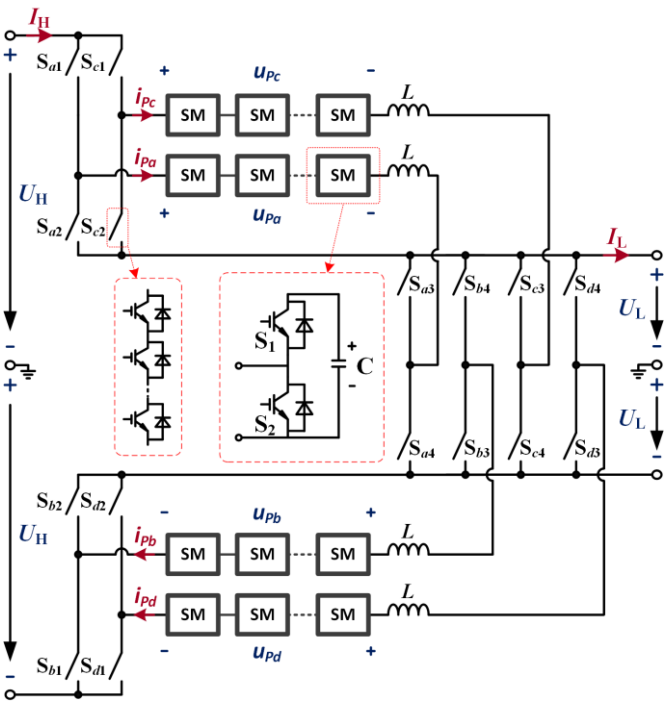


Fig. 2. Configuration of the proposed monopolar symmetrical hybrid cascaded DC/DC converter (MS-HCDC) topology.

utilized by both of the high-voltage (HV) and low-voltage (LV) DC sides, so the number of the semiconductors can be reduced. However, in order to maintain the power balance of the SM capacitors, AC voltages and currents must be injected. As a result, the current stress and power losses are both significant and a large reactor is required at the DC output to filter the injected AC voltages. To avoid using the reactor, additional SM strings have been utilized in [23] and [24] to actively attenuate the injected AC voltages, but this is at the expense of higher semiconductor count and power losses.

Another non-isolated topology is the auto-transformer principle based DC/DC converter (ATDC), as shown in Fig. 1(c), which is composed of two MMCs connected in series on the DC ports, and a partial-power AC transformer is utilized to link the AC ports [25]. Since a portion of power can be transferred directly through the DC path, the power losses and rating of the AC transformer can be reduced. In addition, ATDC can be conveniently extended to a multiport topology [26]. However, the AC transformer in ATDC should be designed to withstand large DC offset voltage stress across the windings, which will significantly increase costs and size compared to a conventional transformer of equivalent power rating [27]. In [28] and [29], the flying capacitors have been utilized to replace the AC transformer in ATDC, but the flying capacitors should accommodate large DC voltage rating and high current stress, which increases weight, volume and manufacture difficulty. In [30], additional SM strings, rather than the flying capacitors, have been used, which will obviously increase the semiconductor count and add to capital costs and power losses of the converter.

In order to avoid using large AC transformer or filtering reactor, a novel hybrid cascaded DC/DC converter (HCDC) has been proposed in [31]. As shown in Fig. 1(d), the HCDC has three phases, each of which consists of four branches of series-connected insulated-gate bipolar transistors (IGBTs), a string of cascaded half-bridge SMs, and one buffering inductor. By controlling the IGBT branches, the SM string can be connected in series between the two DC sides to make the SM capacitors charged/discharged and then switched to the LV DC side to make the SM capacitors discharged/charged. In this way, the DC/DC conversion can be realized through the repeated charging and discharging of the SM capacitors. The three phases operate in an interleaving mode to avoid the currents of the two DC sides being discontinuous. Since all the SMs can be utilized by both of the two DC sides, the HCDC has the highest utilization rate of the SMs compared to the above-mentioned topologies. Hence, it features less semiconductors, higher efficiency, and small footprint.

On the other hand, note that all the aforementioned DC/DC topologies are monopolar asymmetrical structure; however, most of the existing VSC-HVDC projects adopt monopolar symmetrical configuration [32]. Therefore, for practical interconnections between monopolar symmetrical HVDC systems, two HCDC converters in cascade are required [19], [23], [29]. However, in this paper, by further effectively utilizing the SM strings by both of the positive and negative DC poles, the HCDC can be integrated into a novel monopolar symmetrical configuration so that the phase number can be reduced from six to four.

The rest of this paper is organized as follows. In Section II the monopolar symmetrical DC/DC converter and its operating principle are illustrated. This is followed by the circuit analysis and parameter dimensioning in Section III. Further, Section IV discusses the control schemes developed for this monopolar symmetrical DC/DC topology. Simulation results are provided in Section V to demonstrate validity of the topology and control schemes, which is followed by experimental results in Section VI. A further discussion and efficiency evaluation are provided in Section VII, and finally the conclusion is given in Section VIII.

II. Monopolar Symmetrical Hybrid Cascaded DC/DC Converter

A. Circuit Configuration

Circuit configuration of the proposed monopolar symmetrical hybrid cascaded DC/DC converter (MS-HCDC) is shown in Fig. 2. It consists of four phases (j=a, b, c, d); each phase is composed of four branches of IGBTs in series connection (S_{j1}, S_{j2}, S_{j3}, S_{j4}) and a string of cascaded half-bridge SMs and one buffering inductor L. U_H is the voltage of the HV DC side while U_L is the LV DC side voltage. I_H and I_L are the currents of the HV and LV sides, respectively. i_{Pj} is the SM string current, and u_{Pj} is the SM string voltage.

B. Operation Principle of One Phase of the MS-HCDC

Operation principle of one phase of the MS-HCDC is shown in Fig. 3, in which phase a is taken as an example and the power is transferred from the HV side to the LV side. u_{Sa1} ~ u_{Sa4} are the voltages of the IGBT branches, u_L is the voltage across the buffering inductor, and T_h is the operation cycle.

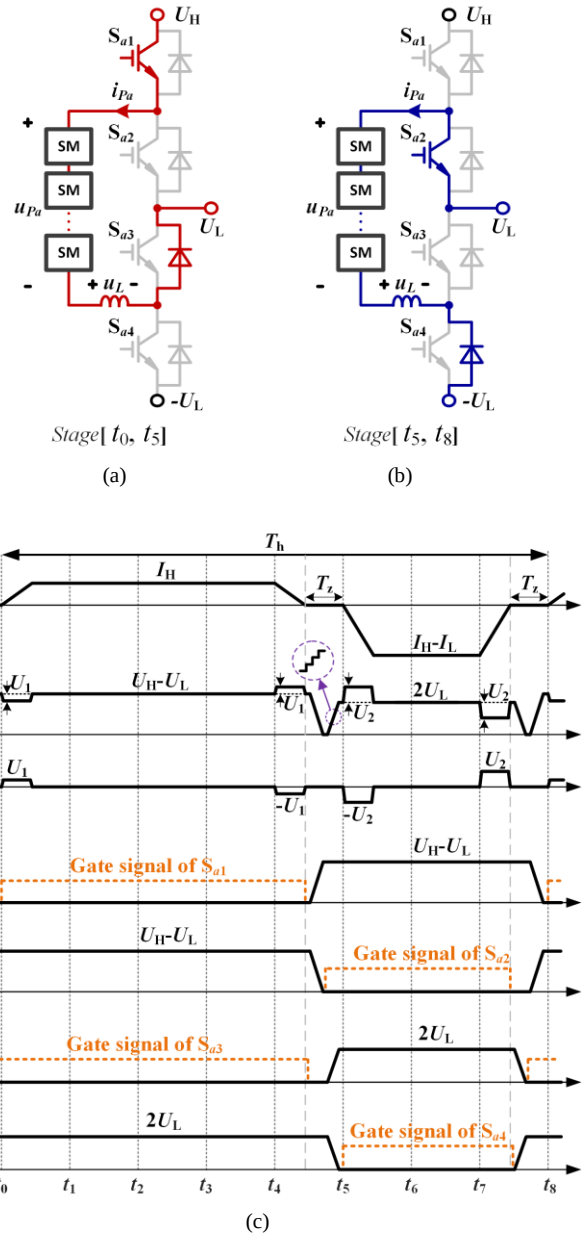


Fig. 3. Operation principle of phase *a* of the MS-HCDC. (a) Circuit during [t_0, t_5]. (b) Circuit during [t_5, t_8]. (c)Waveforms.

During [t_0, t_5], S_{a1} and S_{a3} are in on state while S_{a2} and S_{a4} are in off state, thus the SM string is inserted between the positive poles of the HV and LV DC sides, as shown in Fig. 3(a). The string voltage u_{Pa} accommodates U_H-U_L to control the string current to flow through S_{a1} and S_{a3}, and the SM capacitors are charged. As shown in Fig. 3(c), i_{Pa} is regulated as a trapezoid waveform whose amplitude is I_H. During i_{Pa} rising/falling process, u_{Pa} should be adjusted to impose a positive/negative current driving voltage U_1 across the buffering inductor. Capacitors of the SMs in the string are charged and the total energy absorbed by the SM string during [t_0, t_5] can be derived as

$$\Delta E_{\text{charge}} = \int_{t_0}^{t_5} u_{Pa} i_{Pa} \mathrm{d}t = \int_{t_0}^{t_4} \left(U_H - U_L\right) I_H \mathrm{d}t = \frac{1}{2} T_h I_H \left(U_H - U_L\right) \quad (1)$$

During [t_5, t_8], S_{a2} and S_{a4} are in on state and S_{a1} and S_{a3} are in off state. The SM string is connected in parallel with the LV DC side, as shown in Fig. 3(b). u_{Pa} is controlled to match $2U_L$ and i_{Pa} flows through S_{a2} and S_{a4} which discharges the SM capacitors. As shown in Fig. 3(c), i_{Pa} is controlled as a trapezoid waveform with amplitude of I_H-I_L. A negative/positive current driving voltage U_2 is imposed across the buffering inductor during i_{Pa} falling/rising process. In [t_5, t_8], the SM capacitors get discharged and the total energy released by the SM string is

$$\Delta E_{\text{discharge}} = \int_{t_5}^{t_8} u_{Pa} i_{Pa} \mathrm{d}t = \int_{t_5}^{t_7} 2U_L \left(I_H - I_L\right) \mathrm{d}t = \frac{1}{2} T_h U_L \left(I_H - I_L\right) \quad (2)$$

Summation of (1) and (2) yields the energy variation of the SM string in a cycle, that is

$$\Delta E = \Delta E_{\text{charge}} + \Delta E_{\text{discharge}} = \frac{1}{2} T_h \left(U_H I_H - U_L I_L\right) \quad (3)$$

where $2U_H I_H$ and $2U_L I_L$ represent the HV side and LV side DC power of the MS-HCDC, respectively, and when neglecting the converter losses, they are equal. Hence ΔE is zero, which means the absorbed and released energy over one cycle are balanced. In practice, the amplitudes of the string current during charging and discharging stages are controlled independently. One amplitude is used to regulate the power of the converter, and the other amplitude is adjusted to ensure the absorbed energy somewhat higher than the released energy so as to compensate power losses of the converter.

In addition, during the transition between the stages [t_0, t_5] and [t_5, t_8], an interval T_z is designed where the i_{Pa} is kept zero. It can be observed in Fig. 3(c) that S_{a1} ~ S_{a4} are all switched within T_z, so that the zero-current switching (ZCS) for the IGBT branches is guaranteed. Moreover, by appropriately adjusting the string voltage u_{Pa}, the voltages across S_{a1} ~ S_{a4} (u_{Sa1} ~ u_{Sa4}) can be controlled to be zero as well for achieving zero-voltage switching (ZVS). For instance, when switching off S_{a1} and S_{a3}, the u_{Pa} voltage can be kept at U_H-U_L, thus u_{Sa1} and u_{Sa3} are maintained zero. On the other hand, before switching on S_{a2}, u_{Pa} is decreased to zero, as a result u_{Sa2} becomes zero and ZVS turn-on of S_{a2} is realized. Afterwards, u_{Pa} is increased to match $2U_L$, u_{Sa4} drops to zero accordingly and S_{a4} also turns on at ZVS condition. Likewise, when switching on S_{a1} and S_{a3} while switching off S_{a2} and S_{a4}, the ZVS condition can also be created. Therefore, the variation of string voltage u_{Pa} is U_H-U_L+$2U_L$=U_H+U_L during T_z, whose length should be designed to limit dv/dt, i.e., (U_H+U_L)/T_z.

In summary, all the IGBT branches can be switched on and off under the zero voltage zero current switching (ZVZCS) condition. Besides, to avoid causing excessive dv/dt in the waveform of u_{Pa}, the SMs in the string are switched sequentially, which results in a staircase-shaped transition waveform [17], as shown in Fig. 3(c).

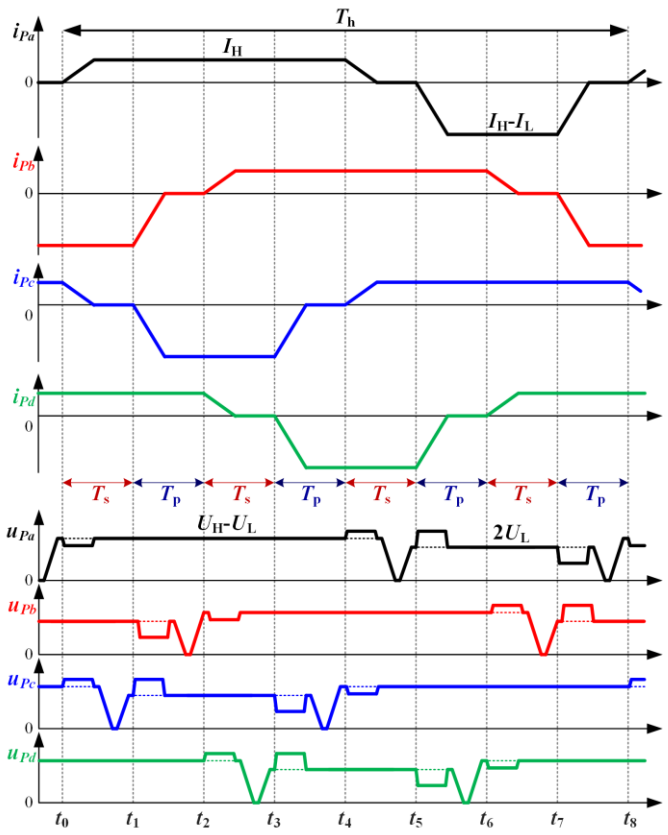
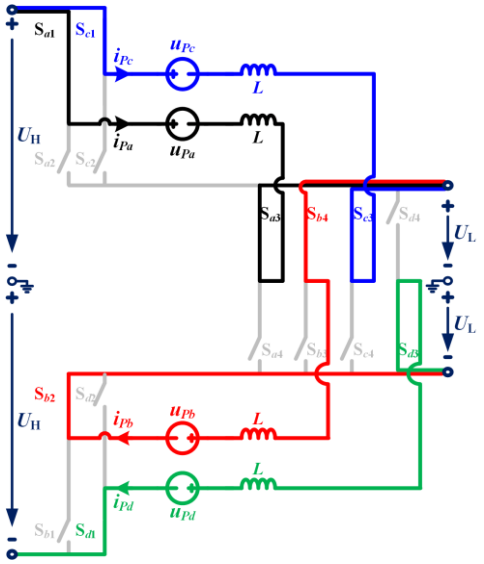


Fig. 4. Operation waveforms of the MS-HCDC.

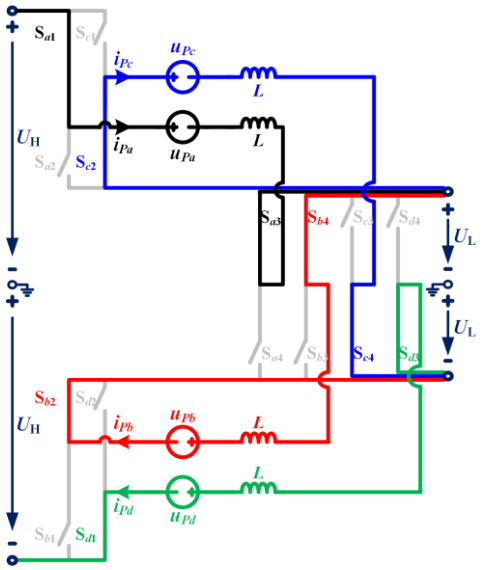
C. Operation Principle of the MS-HCDC

Based on the above discussion of each phase, operation waveforms of the complete MS-HCDC with four phases are further shown in Fig. 4. Actually, the current and voltage waveforms of the four phases are identical but interleaved with 90° electrical angle. In each cycle T_h, it can be divided into eight intervals. During interval [t_0, t_1], the circuit configuration is shown in Fig. 5(a), where string *b* (coloured red) is in parallel with the LV side, string *d* (coloured green) is inserted between the negative poles of HV and LV sides, and strings *a* and *c* (coloured black and blue, respectively) are both inserted between the positive poles of HV and LV sides. During this interval, i_{Pb} remains invariant at I_H-I_L and i_{Pd} remains I_H, respectively. However, current commutation happens between i_{Pa} and i_{Pc}. i_{Pa} increases from 0 to I_H whereas i_{Pc} decreases from I_H to 0, and they have the same changing rate. As a result, for the HV side, current of the positive pole, which is i_{Pa}+i_{Pc}, and current of the negative pole, which is i_{Pd}, are both maintained to be a constant DC value, i.e., I_H. With regard to the LV currents, which is i_{Pa}+i_{Pc}-i_{Pb} for the positive pole and i_{Pd}-i_{Pb} for the negative pole, ensure to be constant I_L.

On the other hand, during the next interval [t_1, t_2] as shown in Fig. 5(b), stings *b* and *c* are connected in parallel with the LV DC side, and strings *a* and *d* are inserted between the positive poles and negative poles of HV and LV sides, respectively. In this case, i_{Pa} and i_{Pd} remain I_H thus the current of HV side is constant I_H. Meanwhile, the current commutation happens between string *b* and *c*, that i_{Pb} changes from I_H-I_L to 0 whereas i_{Pc} changes from 0 to I_H-I_L at the same rate, thus summation of



(a) [t_0, t_1]



(b) [t_1, t_2]

Fig. 5. Circuits of the MS-HCDC during [t_0, t_1] and [t_1, t_2].

i_{Pb} and i_{Pc} is kept as I_H-I_L. Consequently, for the LV side, current of the positive pole, which is i_{Pa}-i_{Pb}-i_{Pc}, and current of the negative pole, which is i_{Pd}-i_{Pb}-i_{Pc}, are both maintained to be a constant DC value, i.e., I_L.

As shown in Fig. 4, the time length of [t_0, t_1] is denoted as T_s and that of [t_1, t_2] is denoted as T_p. The following six intervals are very similar, with T_s and T_p arranged alternately. In T_s, the commutation happens between the two strings which are simultaneously inserted between the positive/negative poles of the two DC sides. In T_p, the current commutates between the two strings that are paralleled with the LV side. By this means, the currents of the two DC sides can always keep continuous and the power balance of the SM capacitors in each string is also guaranteed. In addition, no matter during T_s or T_p, the output voltage of the proposed MS-HCDC is always supported by one or two strings. Consequently, the output voltage quality would not be affected although the proposed MS-HCDC has fewer phases than the traditional HCDC.

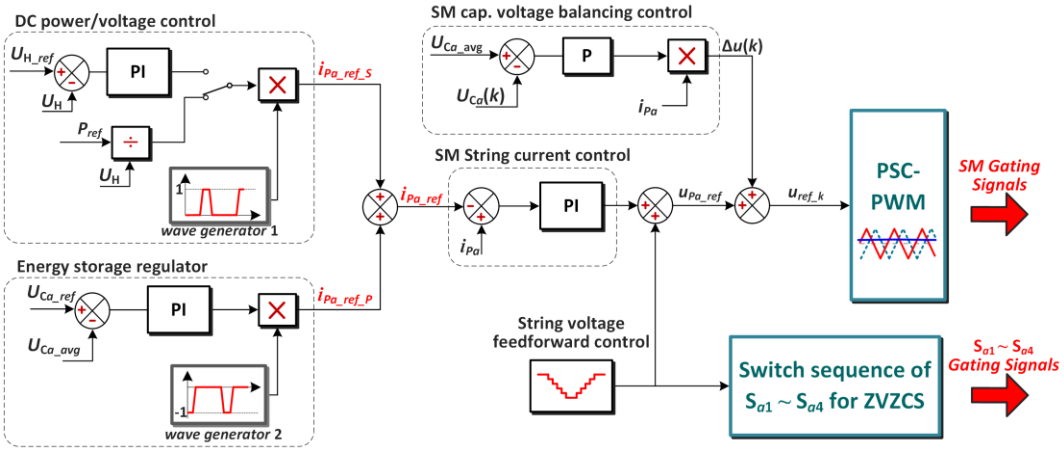


Fig. 6. Control block diagrams for the MS-HCDC.

It is worth noting that, the basic idea of this topology actually lies in the fully utilization of the connectivity of each string, making it able to be parallel with the LV side, inserted between the positive poles, and inserted between the negative poles of two DC sides. On this basis, two traditional HCDCs are integrated into the proposed MS-HCDC. As consequence, four phases of circuit are sufficient to maintain continuous DC currents and it is not necessary to have a total of six phases of circuit as in the conventional HCDC to realize the monopolar symmetrical DC/DC conversion. A large amount of SMs and IGBTs can therefore be saved and the conversion efficiency is improved.

III. Circuit Analysis and Design

A. Sub-Modules

For each SM string, summation of the SM output voltages should be able to provide the required maximum value for matching U_H-U_L or $2U_L$ plus an extra current driving voltage U_1 or U_2. Note that U_1 and U_2 can be determined based on the voltage-second relation of the buffering inductor, that is

$$\begin{cases} U_1 = L\dfrac{I_H}{T_s - T_z} \\ U_2 = L\dfrac{I_L - I_H}{T_p - T_z} \end{cases} \tag{4}$$

where T_s-T_z and T_p-T_z are the corresponding time durations for current rising/falling. As shown in Fig. 4, T_h is equal to $4(T_s+T_p)$, so larger U_1 and U_2 are required if T_h is reduced.

Therefore, taking no account of redundancy, the required number of SMs in each SM string can be then calculated as

$$N = \frac{max\left[U_H - U_L + U_1,\ 2U_L + U_2\right]}{U_C} \tag{5}$$

where U_C is the nominal capacitor voltage of SMs.

Thus, the total number of IGBTs in each SM string of the MS-HCDC is $2N$. The current stress of the IGBTs in SMs depends on the maximum value of the string current, which is

$$I_{stress} = max\left[I_H, I_L - I_H\right]. \tag{6}$$

B. SM Capacitance

The SM capacitors should be designed to withstand the energy fluctuations of each SM string. The maximum energy variation of one SM string can be evaluated by the energy absorbed by the SM string in a cycle, as presented in (1). This energy variation will be buffered by the N SM capacitors in the string, hence the following equation can be obtained:

$$\Delta E_{charge} = \frac{1}{2}NC\left(U_{C,max}^2 - U_{C,min}^2\right) = NC\varepsilon U_C^2 \tag{7}$$

where ε is the specified relative voltage ripple of the SM capacitor. By substituting (1) into (7), the required SM capacitance can be derived as

$$C = \frac{T_h I_H \left(U_H - U_L\right)}{2N\varepsilon U_C^2}. \tag{8}$$

C. Series-Connected IGBTs

For realizing high-voltage switch (several hundred kV), the IGBT branches must be composed of series-connected IGBTs. According to Fig. 3, the IGBT branches S_{j1} and S_{j2} should withstand the voltage of U_H-U_L, while S_{j3} and S_{j4} should withstand the voltage of $2U_L$. Therefore, the number of series-connected IGBTs can be expressed as

$$\begin{cases} N_{1,2} = \dfrac{U_H - U_L}{\lambda_d U_B} \\ N_{3,4} = \dfrac{2U_L}{\lambda_d U_B} \end{cases} \tag{9}$$

where $N_{1,2}$ and $N_{3,4}$ represent the required number of series-connected IGBTs in S_{j1} and S_{j2}, and S_{j3} and S_{j4}, respectively, U_B is the rated blocking voltage of each single IGBT, and λ_d is the voltage derating factor in terms of series connection, which ensures voltage margin for a single IGBT [33]. In practice, λ_d is selected for example 56% in the ABB design [34] and 57% in the GE design [35]. It is noteworthy that the ZVZCS of the IGBT branches can significantly ease the technical difficulty of series connection of IGBTs.

As for the current stress of the series-connected IGBTs, according to Fig. 3, the current stress of S_{j1} and S_{j3} is I_H, and the current stress of S_{j2} and S_{j4} is I_L-I_H, respectively.

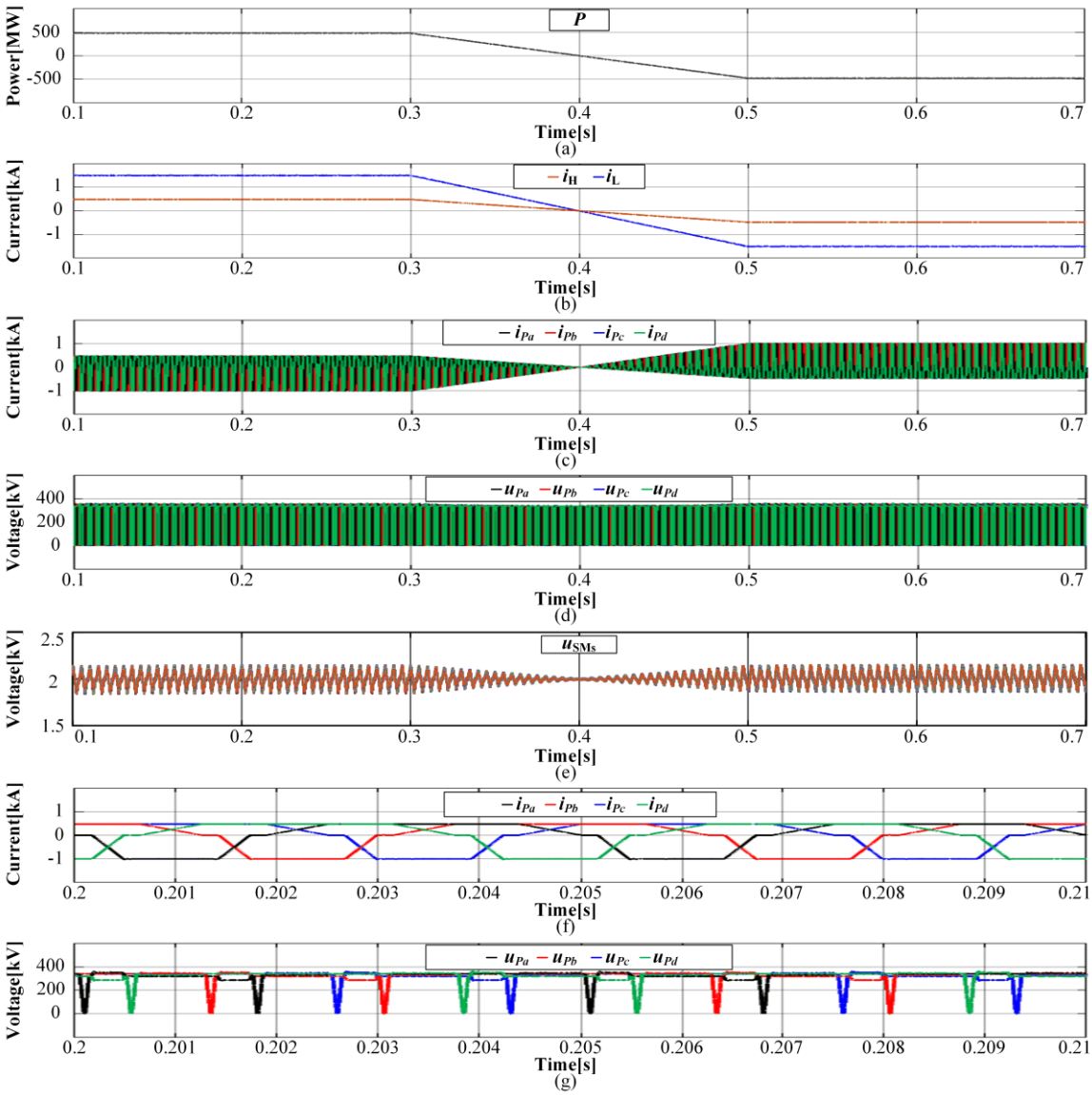


Fig. 7. Simulation results of the MS-HCDC.

D. String Inductance

The string inductors should be designed according to the requirement of switching ripple of the string currents, which satisfy

$$\Delta i = \frac{U_C}{2LNf_c} \tag{10}$$

where Δi is the switching ripple of string current, f_c is the carrier frequency of the phase shifted carrier pulse-width modulation (PSC-PWM) and Nf_c is the equivalent switching frequency of string voltage u_{Pj}.

IV. Control Schemes

Appropriate control schemes for the MS-HCDC topology are developed in Fig. 6, in which phase *a* is taken as an example. The control system is mainly composed of DC power/voltage control, energy storage regulator, SM string current control, string voltage feedforward control, SM capacitor voltage balancing control and PSC-PWM.

There are two control modes in the proposed control schemes, namely DC power control mode and DC voltage control mode. Whether to control DC power or DC voltage depends on the requirement of the HVDC system [36]. When the DC power control mode is desired, the amplitude of the SM string referenced current $i_{Pa\_ref\_S}$ when inserted between the HV and LV sides is given as P_{ref}/U_H, where the P_{ref} is the transmission DC power command. On the other hand, when the DC voltage control mode is required, the amplitude of $i_{Pa\_ref\_S}$ is generated by proportional-integral (PI) controller acting on the error between the reference HV side DC voltage U_{H_ref} minus the measured HV side voltage U_H. Note that the DC power or DC voltage control should coordinate with the HVDC system. To be specific, if the HV and LV side are both connected with DC grids whose voltages are controlled by AC/DC converters, the DC/DC converter should operate in DC power control mode. Otherwise, the DC/DC converter should operate in DC voltage

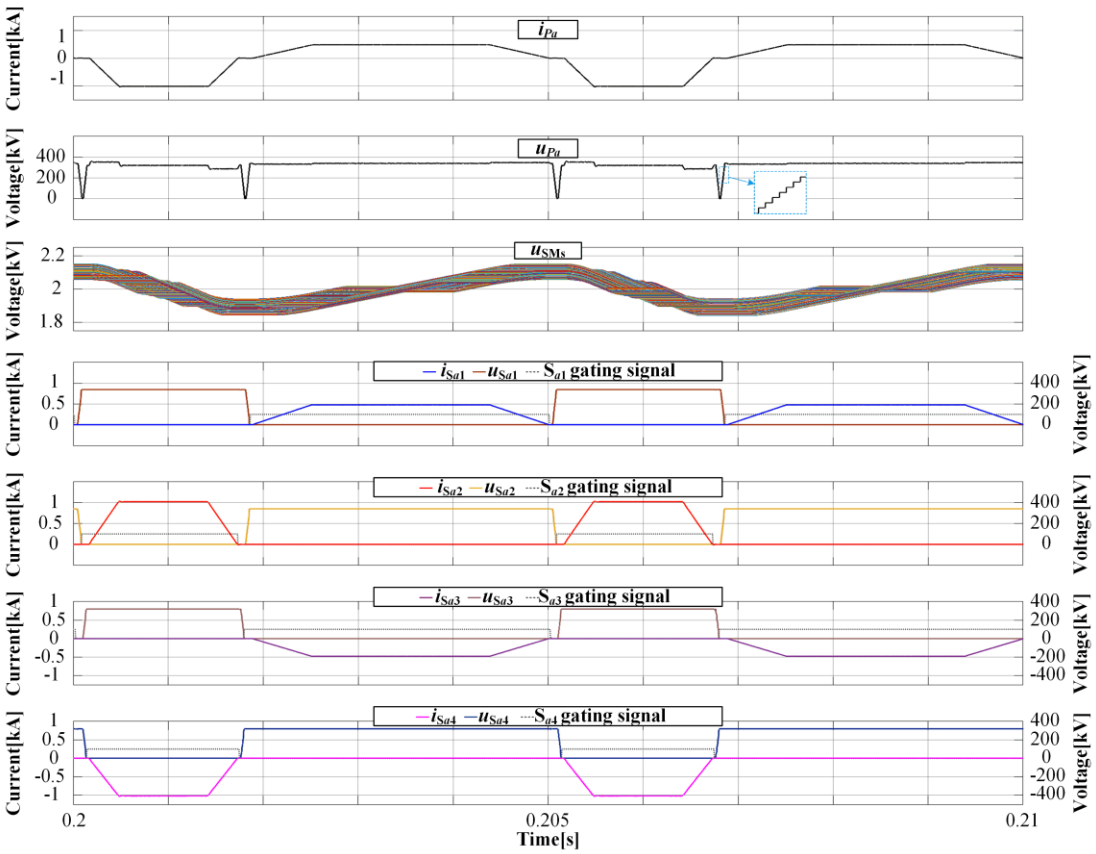


Fig. 8. Detailed simulation results of phase *a* of the MS-HCDC when rated DC power is transmitted from the HV side to the LV side.

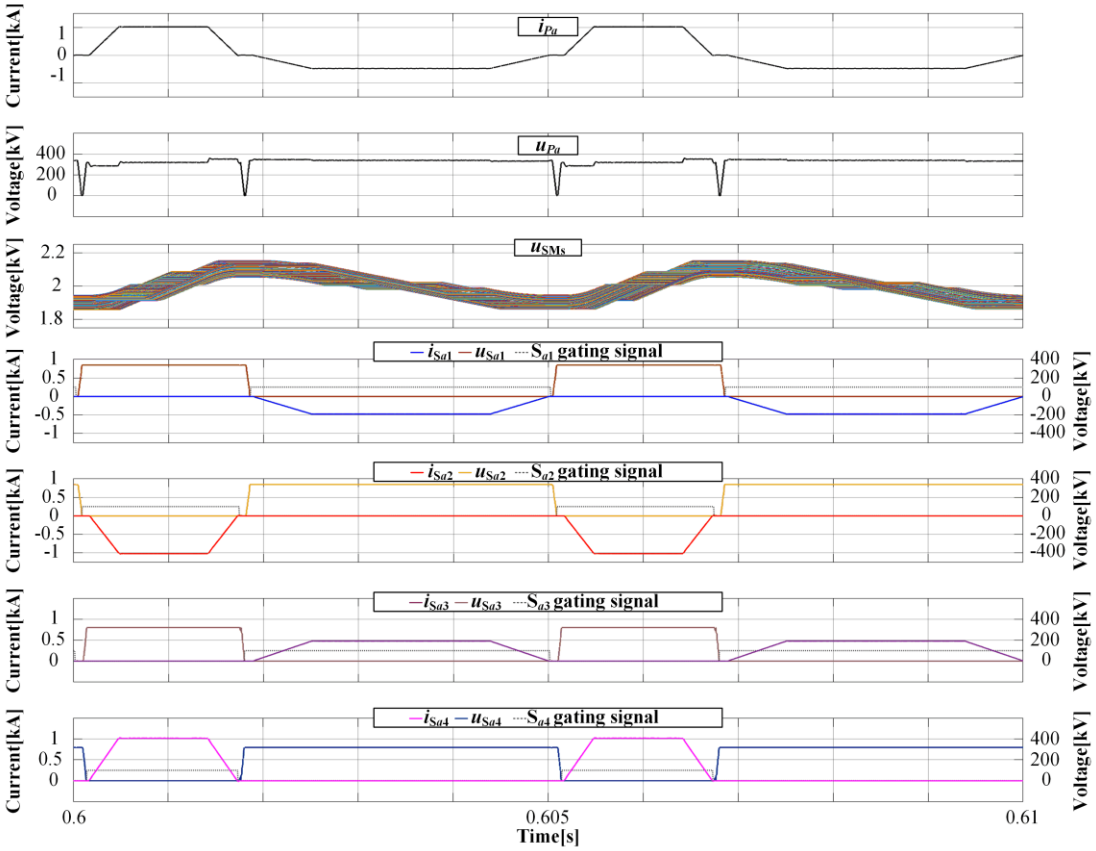


Fig. 9. Detailed simulation results of phase *a* of the MS-HCDC when rated DC power is transmitted from the LV side to the HV side.

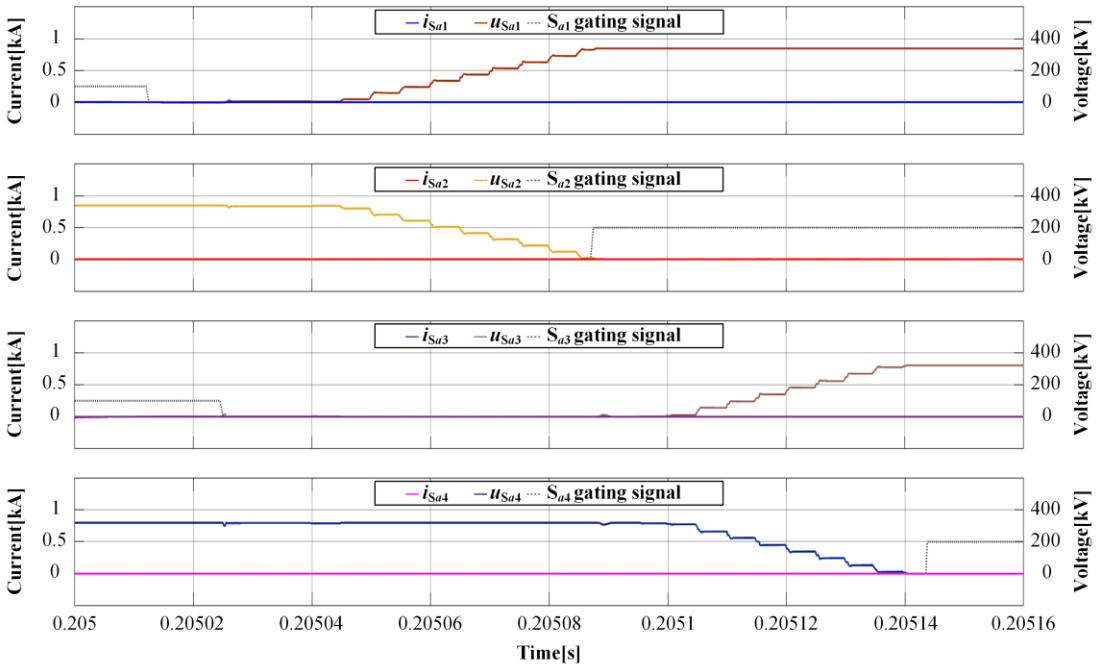


Fig. 10. Simulation results of soft switching process of the IGBT branches.

control mode. For controlling U_H, it is effective in the HVDC system where the AC/DC converter at the HV side controls the power and the AC/DC converter at the LV side stabilizes U_L. The trapezoidal shape of $i_{Pa\_ref\_S}$ is decided by the *wave generator* 1, which will generate a trapezoidal waveform with amplitude of 1 during [t_0, t_5] in Fig.3.

The energy storage regulator is used to achieve balance of the stored energy in the string through adjusting the string current when it is connected in parallel with the LV side (indicated as $i_{Pa\_ref\_P}$). The amplitude of $i_{Pa\_ref\_P}$ is generated by PI controller acting on the error between the reference capacitor voltage U_{Ca_ref} minus the measured average voltage of the SM capacitors U_{Ca_avg}. When this error deviates from zero, it signifies an imbalance in the energy of the string, thus the PI controller regulates the amplitude of $i_{Pa\_ref\_P}$ to reestablish the balance. The trapezoidal shape of $i_{Pa\_ref\_P}$ is decided by the *wave generator* 2, which will generate a trapezoidal waveform with amplitude minus 1 during [t_5, t_8] in Fig.3.

Afterwards, the string current reference i_{Pa_ref} can be obtained by adding $i_{Pa\_ref\_S}$ and $i_{Pa\_ref\_P}$. An inner-loop string current control is then used to adjust the string voltage u_{Pa_ref} in order to make i_{Pa} follow its reference.

The string voltage feedforward control is applied during T_z in Fig. 3. u_{Pa} is gradually decreased from U_H-U_L or $2U_L$ to zero, and then recovers to $2U_L$ or U_H-U_L, to create the ZVZCS condition for the IGBT branches. And a staircase-shaped waveform of string voltage is utilized to avoid excessive dv/dt in the way of inserting (or bypassing) the SMs one by one.

Finally, the string voltage reference u_{Pa_ref} is sent to the PSC-PWM which synthesizes the SM gating signals. In order to balance the SM capacitor voltage, a controller is utilized for each SM. The error between the capacitor voltage of the kth (k=1, 2,…, N) SM $U_{Ca(k)}$ and the average voltage of all the SM capacitors in this string U_{Ca_avg} is inputted into a proportional controller. Moreover, in consideration of the direction of the string current, the output of the proportional controller is further multiplied by i_{Pa} to generate the $\Delta u(k)$. Therefore, if the string current charges the SMs (namely, i_{Pa}>0), a positive $\Delta u(k)$ will be generated for the kth SM once its capacitor voltage $U_{Ca(k)}$ is below the average value U_{Ca_avg}. Afterwards, the voltage reference correction $\Delta u(k)$ is added to the string voltage reference u_{Pa_ref}, which gives the reference voltage of the kth SM u_{ref_k}, and this can be expressed as

$$u_{ref\_k} = u_{Pa\_ref} + \Delta u(k) = u_{Pa\_ref} + K_p\left(U_{Ca\_avg} - U_{Ca(k)}\right) \times i_{Pa} \quad (11)$$

where K_p represents the proportional balancing gain. u_{ref_k} is compared with the triangular carrier of PSC-PWM and finally generates the gating signal of the SM IGBTs. Under this balancing mechanism, the SMs with higher voltage will absorb less energy (or release more energy), and vice versa [37].

As for the other three phases, the only difference is that each of the *wave generators* is lagged 90° electrical angle compared with its previous phase. As a result, continuous HV and LV DC currents can be obtained.

TABLE I
SIMULATION PARAMETERS

Converter Parameters	Values
Rated DC power	P=480MW
HV DC voltage	$\pm U_H$=±500kV
LV DC voltage	$\pm U_L$=±160kV
No. of SMs in each string	N=200
Nominal SM capacitor voltage	U_C=2kV
SM capacitance	C=5.1mF
SM capacitor voltage ripple	ε=10%
PSC carrier frequency	f_c=550Hz
Operation cycle	T_h=5ms
Buffering inductor	L=10mH

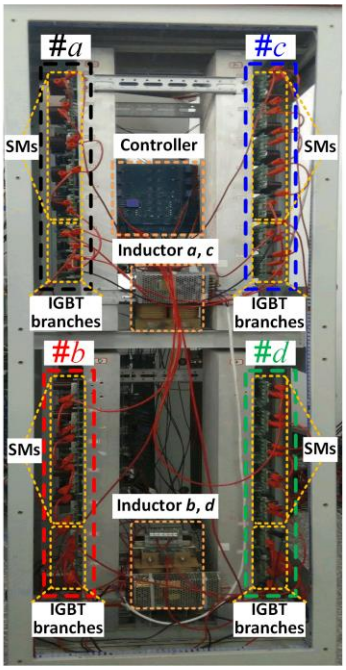


Fig. 11. Photograph of the laboratory MS-HCDC prototype.

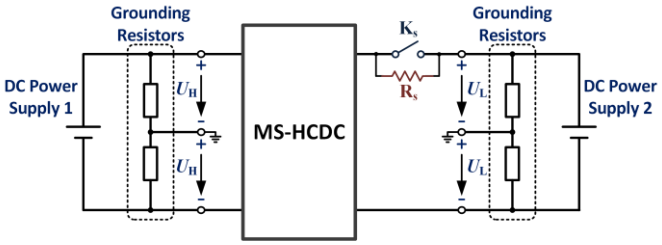


Fig. 12. Configuration of the experimental circuit.

V. Simulation Study

In order to verify feasibility of the proposed topology, a 480MW, ±500kV/±160kV simulation model of the MS-HCDC is performed in MATLAB/SIMULINK. Detailed parameters are listed in Table I. In each SM string, there are 200 SMs and each of them is rated at 2kV.

Fig. 7 presents the bidirectional power flow response of the MS-HCDC. As shown in Fig. 7(a), in the beginning, the converter transmitted rated DC power from the HV side to the LV side; then between 0.3s and 0.5s, the DC power was ramped from +480MW down to -480MW; afterwards, the power was maintained -480MW, meaning the power flow was reversed completely. Fig. 7(b) shows the currents (i_H and i_L) of the two DC sides. The currents (i_{Pa}, i_{Pb}, i_{Pc}, i_{Pd}) and voltages (u_{Pa}, u_{Pb}, u_{Pc}, u_{Pd}) of the four SM strings are displayed in Figs. 7(c) and (d), respectively. In addition, the capacitor voltages of the 200 SMs in phase *a* are shown in Fig. 7(e), which were kept well balanced during the whole simulation process. Zoomed currents and voltages of the four SM strings are displayed in Fig. 7(f) and (g). As can be observed, although the shapes and amplitudes of the four SM string currents and voltages are identical, they are interleaved with 90° electrical angle. Therefore, the currents of the two DC sides maintain continuous

TABLE II
Experimental Parameters

Converter Parameters	Values
Rated DC power	P=2.4kW
HV DC voltage	$\pm U_H$=±300V
LV DC voltage	$\pm U_L$=±100V
No. of SMs in each string	N=5
Nominal SM capacitor voltage	U_C=50V
SM capacitance	C=3mF
PSC carrier frequency	f_c=3kHz
Operation cycle	T_h=10ms
Buffering inductor	L=2mH

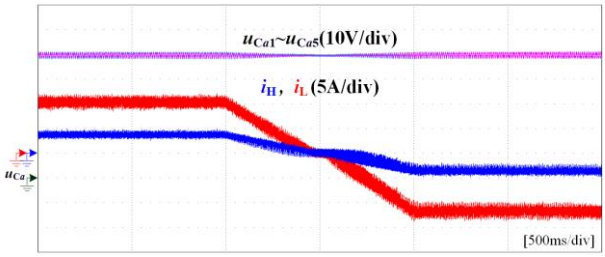


Fig. 13. Experimental results of the MS-HCDC under power reversal: currents of the two DC sides; capacitor voltages of the SMs u_{Ca1} ~ u_{Ca5}.

as shown in Fig. 7(b). These results verified the validity of the MS-HCDC and the control schemes.

Fig. 8 further shows the detailed waveforms of phase *a* when the power flow is from the HV side to the LV side, which agree well with the theoretical waveforms in Fig. 3(c). i_{Pa} appears trapezoidal waveform with positive amplitude of I_H to charge the SMs in the string and with negative amplitude of I_L-I_H to discharge them. The SM capacitors are designed according to (8), in which SM capacitor voltage ripple ε is equal to 10%. Besides, the SM capacitor voltages are well balanced, but it can be observed that in each cycle there are slight differences among them, this is due to the low switching frequency of each SM. Furthermore, the staircase-shaped waveform can be observed during the rising and falling transitions of u_{Pa}, in which way the dv/dt value is limited.

Fig. 9 displays the detailed waveforms of phase *a* when the power flow is from the LV side to the HV side. The SM string is charged by the current I_L-I_H, and discharged by I_H, thus i_{Pa} seems upside down compared with that in Fig. 8, and so do the currents of the IGBT branches.

Fig. 10 further shows the zoomed current, voltage, and gating signals of the IGBT branches. It can be observed that the gating signals are applied when the switch voltages and currents are both zero, which demonstrates the ZVZCS of S_{a1} ~ S_{a4}.

VI. Experimental Verification

A downscaled prototype of the MS-HCDC rated at 2.4kW, ±300V/±100V has been built in the authors' laboratory, as shown in Fig. 11. Each of the four SM strings is composed of five half-bridge SMs. The test configuration is shown in Fig. 12, two regenerative DC power supplies with grounding resistors are connected with the MS-HCDC to emulate the monopolar

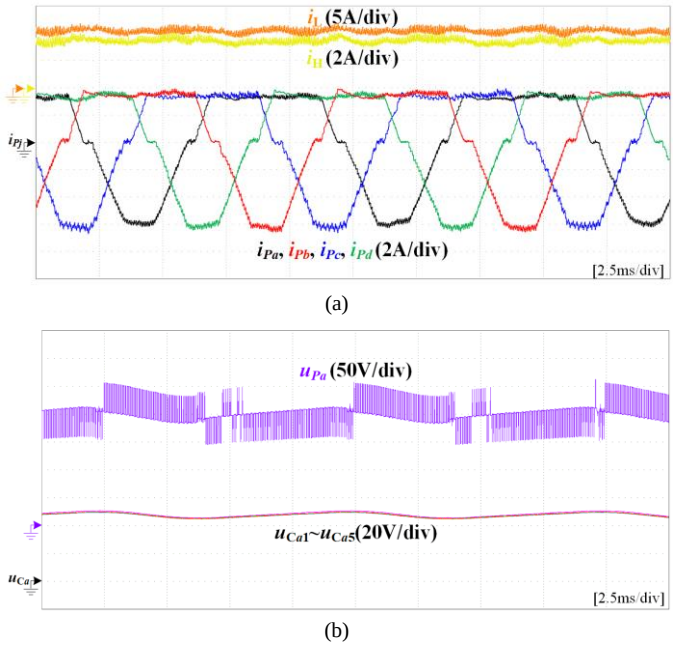


Fig. 14. Experimental results of the MS-HCDC when power is transmitted from the HV side to the LV side. (a) Currents of the two DC sides; currents of the SM strings; (b) String voltage u_{Pa}; capacitor voltages of the SMs u_{Ca1} ~ u_{Ca5}.

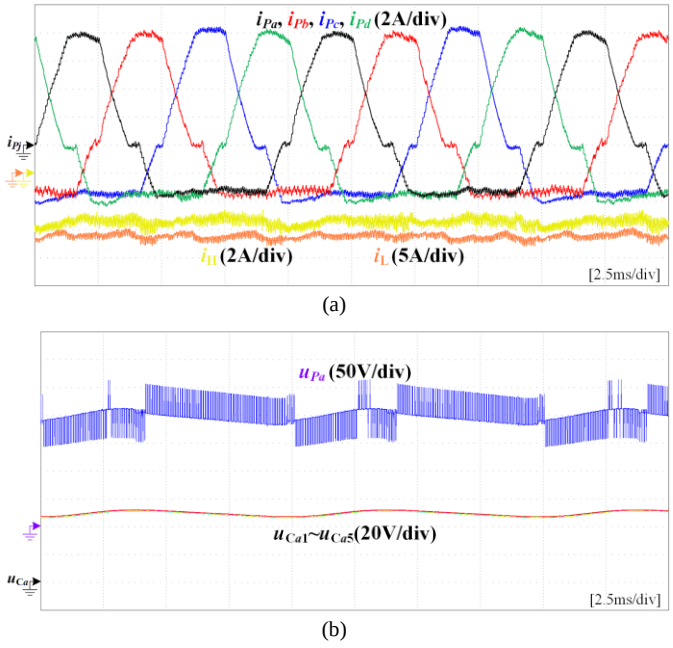


Fig. 15. Experimental results of the MS-HCDC when power is transmitted from the LV side to the HV side. (a) Currents of the two DC sides; currents of the SM strings; (b) String voltage u_{Pa}; capacitor voltages of the SMs u_{Ca1} ~ u_{Ca5}.

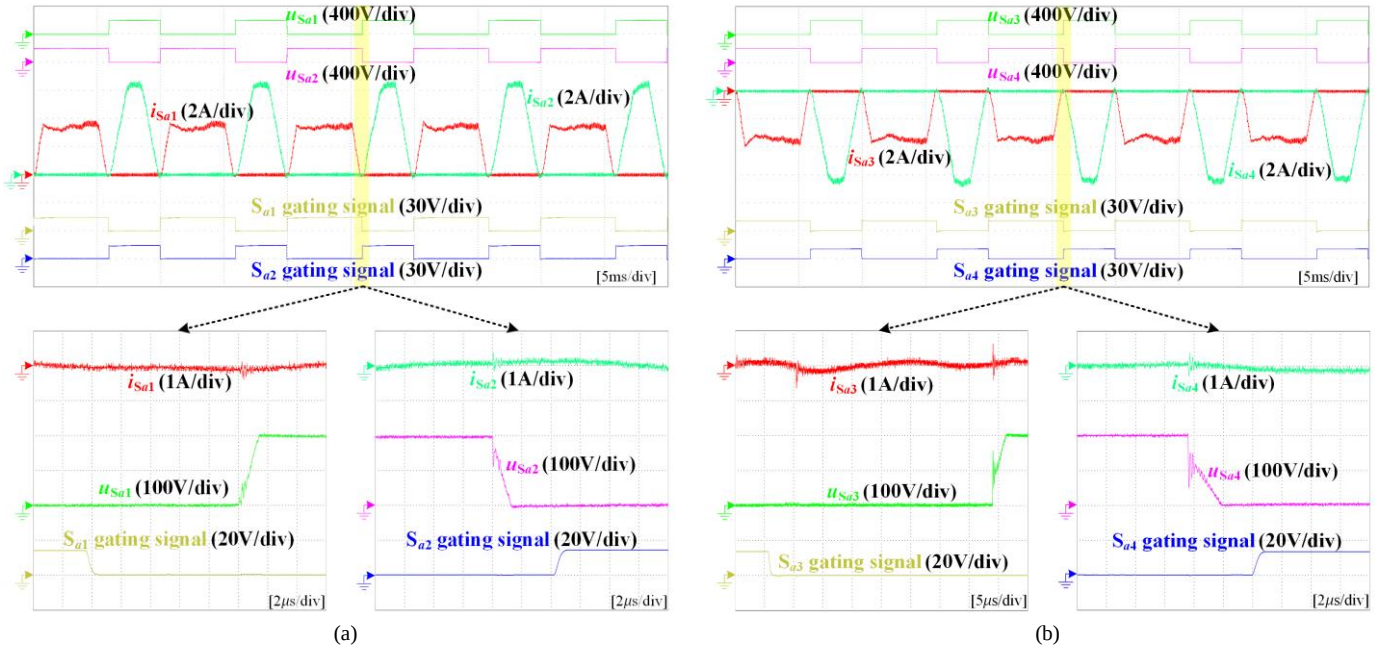


Fig. 16. Experimental results of the soft switching process of the IGBT branches. (a) S_{a1} switching OFF and S_{a2} switching ON; (b) S_{a3} switching OFF and S_{a4} switching ON.

symmetrical HVDC systems with different voltage ratings and a limiting resistor R_s with bypass contactor K_s is installed in series with the LV DC side of the proposed MS-HCDC, which is utilized to limit the inrush current into the capacitors during the start-up process of the MS-HCDC. The main circuit parameters are given in Table II. A digital signal processor TMS320F28377D DSP is employed to realize the control algorithms, and each SM is controlled by an independent EPM570T100 CPLD.

Fig. 13 presents the bidirectional power transfer performance of the MS-HCDC. At the beginning, the MS-HCDC transmitted 2.4kW power flow from the HV side to the LV side, and then the power flow was ramped down and kept reversed. In the whole process, the DC currents i_H and i_L followed the references and maintained stable. Nevertheless, some visible harmonics existed. This is due to the limited number (only five) of SMs in each string. For practical application with hundreds of SMs, the current harmonics would become negligible as a result of the sufficiently high number of levels in the string voltage. In addition, it can be observed the SM capacitor voltages were

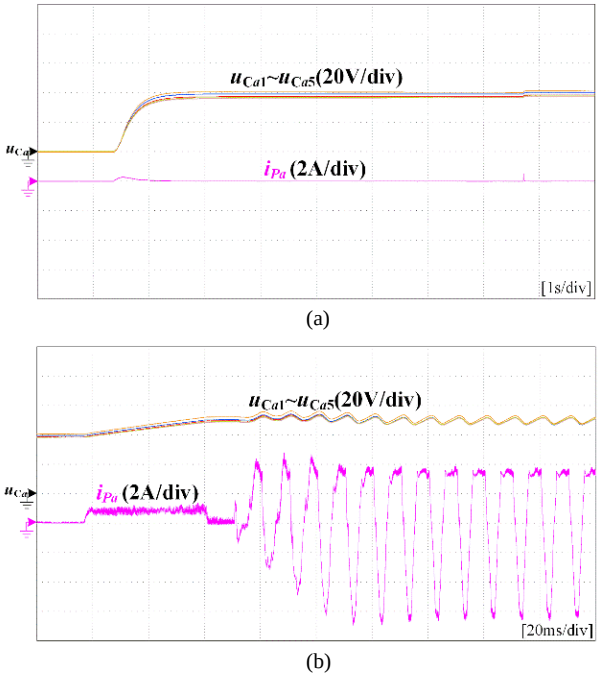


Fig. 17. Experimental results of the start-up process of the proposed MS-HCDC. (a) Uncontrolled precharge stage; (b) Closed-loop precharge stage.

well balanced around 50V during the entire power reversal process.

Fig. 14 presents the detailed steady-state waveforms of the MS-HCDC when power flow was transferred from the HV side to the LV side. The SM string current waveforms of the four phases were almost identical but interleaved with 90° electrical angle, which generated continuous HV and LV DC currents i_H and i_L. In addition, the peak-to-peak value of the SM capacitor voltages is about 5V, which agrees with the theoretical result in (8). On the other hand, Fig. 15 shows the detailed steady-state waveforms when power flow was transferred from the LV side to the HV side. The string current waveforms in Fig. 15(a) seem upside down compared with those in Fig. 14(a), meaning that the direction of the power flow was reversed. These results confirmed the effectiveness of the MS-HCDC topology and the proposed control schemes.

Fig. 16 displays the soft switching process of the IGBT branches. As shown in Fig. 16(a), S_{a1} was switched off before u_{Sa1} began to rise from zero, and S_{a2} was switched on after u_{Sa2} fell to zero. As shown in Fig. 16(b), S_{a3} was switched off before u_{Sa3} started to rise, and S_{a4} was switched on after u_{Sa4} dropped to zero. Meanwhile, i_{Sa1} ~ i_{Sa4} were basically zero during this process, thus S_{a1} ~ S_{a4} can all be switched under ZVZCS condition. However, some resonant spikes are visible which are caused by the interaction between buffering inductance and parasitic capacitances, as well as the excitation of one voltage step of the u_{Pa} waveform (i.e., one SM voltage). As a result, this voltage spike cannot be higher than one SM voltage, hence it would not be a severe problem in the practical application with hundreds of SMs.

Fig. 17 shows the experimental results of the start-up precharge process of SM capacitors, in which phase *a* is taken as an example. Fig. 17(a) shows the waveforms of the first uncontrolled precharge stage, during which the SM capacitors

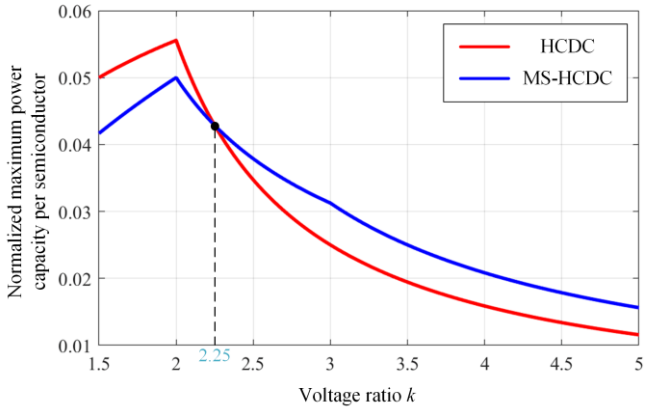


Fig. 18. The maximum power capacity per semiconductor of the traditional HCDC and the proposed MS-HCDC (normalized by $U_{rated}I_{rated}$).

TABLE III
COMPONENT COUNTS OF THE PROPOSED MS-HCDC AND THE HCDC

Quantity	HCDC topology [31]	Proposed MS-HCDC
No. of SMs	200×6=**1200**	200×4=**800**
No. of SM IGBTs	1200×2=**2400**	800×2=**1600**
No. of series-connected IGBTs	318×6=**1908**	420×4=**1680**
No. of buffering inductors	6	4

can be precharged to about 40V through the 40Ω limiting resistor. Fig. 17(b) shows the waveforms of the further controlled precharge stage. The charging current is closed-loop regulated as 1A by adjusting the string voltage. Once the SM capacitors are fully charged to their rated capacitor voltage 50V, the proposed MS-HCDC turns into normal operation as the string current becomes trapezoid waveform.

VII. DISCUSSIONS

A. Comparison with the traditional HCDC

In order to fairly compare the proposed MS-HCDC with the traditional HCDC, the maximum power capacity per semiconductor is used in this paper. It is assumed that the identical IGBTs are used and redundancy is not taken into consideration. According to (6), the maximum capacity of both the traditional HCDC and the proposed MS-HCDC can be expressed as

$$P_{max} = U_H I_H = \begin{cases} U_H I_{rated} & \text{if } k \le 2 \\ \dfrac{U_H I_{rated}}{k-1} & \text{if } k > 2 \end{cases} \tag{12}$$

where I_{rated} is the rated current of the IGBTs and k=U_H/U_L is the voltage ratio.

As for the traditional HCDC, the required number of SMs in each SM string is

$$N_{HCDC} = \frac{max\left[U_H - U_L, U_L\right]}{U_{rated}}. \tag{13}$$

where U_{rated} is the rated voltage of the IGBTs and the extra current driving voltage U_1 and U_2 are ignored because they are relatively small compared to U_H and U_L.

And the number of series-connected IGBTs in each IGBT branch of the traditional HCDC can be calculated as

$$\begin{cases} N_{1,2\_\mathrm{HCDC}} = \dfrac{U_{\mathrm{H}} - U_{\mathrm{L}}}{U_{\mathrm{rated}}} \\ N_{3,4\_\mathrm{HCDC}} = \dfrac{U_{\mathrm{L}}}{U_{\mathrm{rated}}} \end{cases}. \tag{14}$$

Therefore, the maximum power capacity per semiconductor of the traditional HCDC can be derived as

$$\begin{aligned} M_{\mathrm{HCDC}} &= \frac{P_{max}}{6\times\left(2N_{\mathrm{HCDC}}+2N_{1,2\_\mathrm{HCDC}}+2N_{3,4\_\mathrm{HCDC}}\right)} \\ &= \begin{cases} \dfrac{k}{12(k+1)}U_{\mathrm{rated}}I_{\mathrm{rated}} & \text{if } k\le 2 \\ \dfrac{k}{12(k-1)(2k-1)}U_{\mathrm{rated}}I_{\mathrm{rated}} & \text{if } k>2 \end{cases}. \end{aligned} \tag{15}$$

Likewise, the maximum power capacity per semiconductor of the proposed MS-HCDC can be expressed as

$$M_{\mathrm{MS\text{-}HCDC}} = \begin{cases} \dfrac{k}{8(k+3)}U_{\mathrm{rated}}I_{\mathrm{rated}} & \text{if } k\le 2 \\ \dfrac{k}{8(k+3)(k-1)}U_{\mathrm{rated}}I_{\mathrm{rated}} & \text{if } 2<k<3 \\ \dfrac{1}{16(k-1)}U_{\mathrm{rated}}I_{\mathrm{rated}} & \text{if } k\ge 3 \end{cases}. \tag{16}$$

According to (15) and (16), Fig. 18 further shows the comparison results of maximum power capacity per semiconductor of the traditional HCDC and the proposed MS-HCDC, which are normalized by $U_{\mathrm{rated}}I_{\mathrm{rated}}$. It is shown the maximum power capacity per semiconductor changes along with the voltage ratio k. The traditional HCDC has larger maximum power capacity per semiconductor if the voltage ratio is smaller than 2.25. On the contrary, the proposed MS-HCDC is better if the voltage ratio exceeds 2.25. Larger maximum power capacity per semiconductor indicates higher utilization of semiconductors, so the proposed MS-HCDC is superior when the voltage ratio is larger than 2.25.

B. Specific case

The simulated DC/DC conversion application in Section V (480MW, ±500kV/±160kV) is further studied to make a comparison between the proposed MS-HCDC and the traditional HCDC. The identical half-bridge SMs are chosen in the MS-HCDC and the traditional HCDC, whose nominal SM capacitor voltage is U_{C}=2kV. For the MS-HCDC and the traditional HCDC, the numbers of half-bridge SMs in one phase are the same, which is 200 in this case study. However, the MS-HCDC needs only four phases, while the traditional HCDC needs six phases in total (three phases for each pole). Thus, the number of SMs and SM IGBTs in the MS-HCDC can be reduced by 1/3, as shown in Table III. However, it should be noted that the total energy stored in the SM capacitors in the proposed MS-HCDC is equal to that of the traditional HCDC, as then number of SMs is reduced, the SM capacitance of the proposed MS-HCDC should be 1.5 times that of the traditional

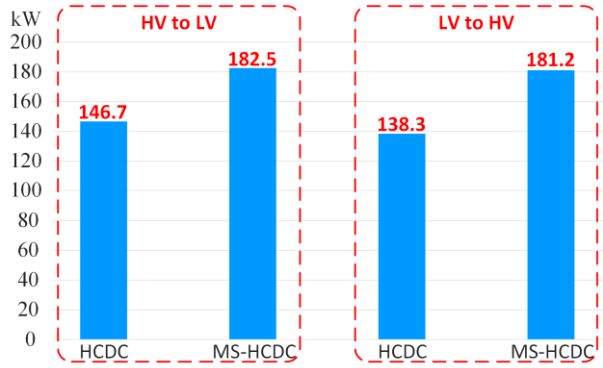


Fig. 19. Summation of the conduction losses of four IGBT branches in one phase in the traditional HCDC and the MS-HCDC.

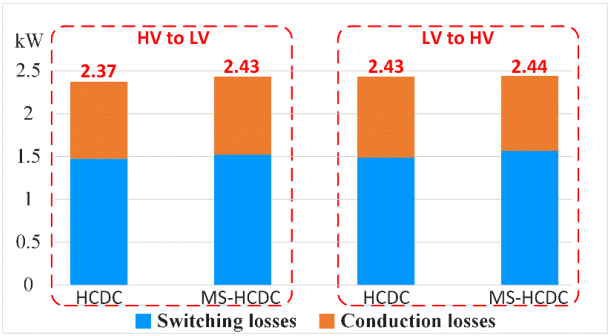


Fig. 20. Losses of each SM in the traditional HCDC and the MS-HCDC.

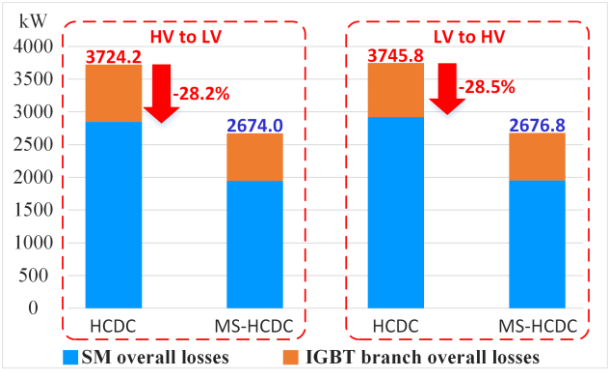


Fig. 21. Overall converter losses comparison.

HCDC. Consequently, compared to the traditional HCDC, the cost and volume corresponding to capacitors in the proposed MS-HCDC remain the same. However, since the number of SMs in the proposed MS-HCDC can be reduced significantly, the cost and volume corresponding to semiconductors and their auxiliary components (drivers, sensors, cooling devices, etc.) are saved. Therefore, the proposed MS-HCDC in general presents lower capital costs and smaller footprint.

The numbers of the series-connected IGBTs are also shown in Table III. The voltage rating of S_{j1} and S_{j2} in the MS-HCDC is the same with that in the HCDC, while the voltage rating of S_{j3} and S_{j4} is twice that in the HCDC. Therefore, for a single phase, the MS-HCDC needs more series-connected IGBTs. However, since the number of phases is less, the MS-HCDC needs less series-connected IGBTs in total. It can be observed that the number of series-connected IGBTs in the MS-HCDC can be reduced by 12% compared with the traditional HCDC.

In addition, the MS-HCDC requires only four buffering inductors, compared to the traditional HCDC which needs six.

Furthermore, the power losses of the proposed MS-HCDC and the traditional HCDC in the 480MW, ±500kV/±160kV DC/DC conversion application are evaluated by co-simulation between MATLAB/SIMULINK and PLECS software. For the IGBT branch, ABB 4.5kV/2kA press-pack IGBT module "5SNA2000K450300" is employed, and the ABB 3.3kV/1.5kA IGBT module "5SNA1500E330305" is used in the half-bridge SMs. For 5SNA 2000K450300 IGBT module, the junction-to-case and case-to-heatsink thermal resistances are 0.004K/W and 0.001K/W, respectively, which are obtained from the datasheet [38]. For 5SNA 1500E330305 IGBT module, the IGBT junction-to-case and case-to-heatsink thermal resistances are 0.0085K/W and 0.009K/W, respectively, and the diode junction-to-case and case-to-heatsink thermal resistances are 0.017K/W and 0.018K/W, respectively, which are obtained from the datasheet [39]. The cooling water temperature of 40°C and heatsink-to-water thermal resistance of 5K/kW are assumed [40].

Fig. 19 demonstrates the summation of the power losses of four IGBT branches in one phase of the traditional HCDC and the MS-HCDC, respectively. Since the IGBTs operate under ZVZVS condition, only the conduction losses are taken into consideration. The conclusion can be drawn that the power losses of IGBT branches in a single phase of the MS-HCDC are higher than those of the HCDC. However, the MS-HCDC requires less phases, so the total losses of IGBT branches of the MS-HCDC are 82.94% of those of the HCDC when power is transmitted from the HV side to the LV side, and 87.35% in the reversed direction.

Fig. 20 presents the average losses of each SM in the traditional HCDC and the MS-HCDC, respectively. It is shown that for a single SM in the traditional HCDC and the proposed MS-HCDC, the power losses are similar. Whereas, the total power losses of SMs in the MS-HCDC are much lower because the number of SMs in the MS-HCDC is only 2/3 of that of the traditional HCDC.

Adding the power losses of IGBT branches and all the SMs, the overall converter losses can be calculated, as shown in Fig. 21. As the power of the converter is 480MW, the overall efficiency of the traditional HCDC is 99.22%, while efficiency of the MS-HCDC is about 99.44%. To summarize, compared with the traditional HCDC, the MS-HCDC can reduce the overall power losses by more than 28.2%.

VIII. Conclusion

A monopolar symmetrical hybrid cascaded DC/DC converter (MS-HCDC) is proposed in this paper for interconnections of HVDC systems with different voltage ratings. The SM strings can be utilized by both of the positive and negative DC poles, thus only four phases are required compared to the traditional HCDC, which results in reduction of capital cost, power loss and footprint of the converter. Compared to the traditional HCDC, the proposed MS-HCDC has larger maximum power capacity per semiconductor when the voltage ratio is larger than 2.25, which means the proposed MS-HCDC should be selected to obtain higher utilization of the semiconductors in this case. The operation principle and control strategies are discussed. Simulation and experimental results are performed which confirmed the validity and effectiveness of the MS-HCDC. The proposed MS-HCDC can be a promising "DC transformer" solution in the future monopolar symmetrical HVDC interconnections.

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