Operation and Control of an HVDC Circuit Breaker with Current Flow Control Capability

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***Abstract*—Deployment of dc circuit breakers (DCCBs) will help to isolate dc faults in dc systems. Conversely, current flow controllers (CFCs) will be employed in dc grids to balance currents among transmission lines. However, the inclusion of these devices may incur significant capital investment. A way to reduce costs is by integrating current control capabilities into DCCBs. This paper presents a new device, the CB/CFC, which combines a multi-line DCCB with a half-bridge based CFC. The operating principles of the device are analyzed and its operating modes are classified. A level-shift modulation method ensuring that a single bridge of the CB/CFC is modulated for each operating mode is considered. This simplifies the control scheme for CFC operation. For completeness, the CB/CFC is compared with other alternatives available in the literature. It is shown that the presented device reduces the number of semiconductor components compared to other solutions. DC fault isolation and current flow control are verified through simulations conducted in PSCAD.**

***Index Terms*—HVDC system, dc circuit breaker, current flow controller, level-shift modulation, dual-loop control.**

I. Introduction

Compared to high-voltage direct-current (HVDC) point-to-point links, meshed HVDC grids are attractive solutions for bulk power transfer due to their enhanced flexibility and reliability [1], [2]. However, the installation of dc circuit breakers (DCCBs) and current flow controllers (CFCs) will be required to quickly isolate faults and fully control current flow in dc grids [3]-[6]. The capital costs of a dc grid may increase significantly by adding these devices and, thus, their integration into a single device to reduce costs while fulfilling the same operating requirements is worth to be investigated.

The current flow within a meshed multi-terminal dc (MTDC) grid is dominated by the resistance of the transmission lines and cannot be fully regulated by converter terminals [7], [8]. In meshed dc grids, parallel paths for power flow exist. Under some operating conditions, one conduction path may reach its full power capacity (thermal limit), whereas other paths may not be fully utilized. These unbalanced current flows may either cause transmission line overloadings or transmission bottlenecks when system operating conditions change. Thus, CFCs are needed in MTDC grids for power flow balancing, pole balancing, and thermal management and, this way, to fully use the capacity of the transmission network. In addition, they can be used for maintenance of dc lines without the need for putting out of service the whole MTDC grid [9], [13].

Different configurations achieving current flow control have been investigated in the literature [6]-[14]. Among the possible alternatives, passive resistor-based CFCs generate considerable power losses and large cooling systems are required to dissipate the excess heat [6], [8], [10]. To prevent large losses, external voltage source-based CFCs may be used, which exchange power with nearby ac or dc lines. However, this device requires a large isolation transformer, increasing its footprint and capital costs [6], [8], [11]. To solve the above problems, interline CFCs have been proposed [12]-[15]. By using series dc/dc converters within a dc grid, interline CFCs exchange power between transmission lines without incurring large losses and avoiding the use of isolation transformers [12], [13].

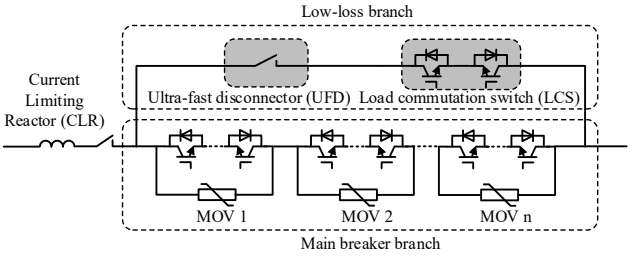

Fig. 1. HCB topology proposed in [19].

In an MTDC grid, the propagation of a dc fault is fast due to the small impedance exhibited by dc transmission lines [17]. DCCBs are required to interrupt the fault currents within a few milliseconds to maintain the normal operation of the remaining healthy parts of the grid [18]. Fig. 1 shows the topology of a hybrid DCCB (HCB), consisting of a low-loss branch and a main breaker (MB) branch [19]. Current flows through the low-loss branch under normal conditions. When a dc fault is detected, the fault current is commutated to the MB branch for fault interruption. Fault energy is absorbed by metal oxide varistors (MOVs) across the MB branch.

By integrating mechanical and semiconductor switches, HCBs achieve a high interruption speed while exhibiting low power losses. However, the capital cost of the device is a major concern. Alternative HCB topologies have been proposed by different manufacturers [5], [20]. However, these also present a similar problem: the MB contains a large number of semiconductor switches (i.e. IGBTs) to be able to withstand around 1.5 to 2 p.u. of the rated dc bus voltage [18], [19].

The use of HCBs sharing MB branches to reduce the number of semiconductor switches when multiple dc lines are connected to one terminal has been proposed [21]-[24]. Diode and thyristor-based solutions have been examined as their costs are relatively lower compared to those of an IGBT-based

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topology [5], [25]. However, only selected references have assessed the integration of current flow control into HCBs, which would further reduce costs. In [26], the low-loss branches of different HCBs are connected together to operate as an H-bridge CFC. Both current regulation and dc fault isolation are implemented and the semiconductor switch count reduced by eliminating the need for a separate CFC. To further reduce the number of semiconductor switches, the MBs can be shared [27]. This way, a large number of components can be avoided since the MB dominates the number of switches of an HCB.

Although [26] and [27] represent noteworthy attempts to integrate CFC and HCB capabilities, the control and modulation methods for CFC operation have not yet been analyzed in detail. A simple and reliable control method not requiring the detection of instantaneous current directions to generate control signals is still required [14]-[16].

To bridge the aforementioned gaps, an integrated device, the CB/CFC, is presented in this paper. This consists of a half-bridge based CFC and a multi-line HCB incorporated into a single device, thereby providing current flow control and dc fault isolation capabilities. A level-shift modulation method is adopted, which ensures that a single bridge is regulated by modulating signals under a specific operating mode, and that the transition to different modes does not rely on the detection of the direction of instantaneous currents. It is shown that the number of semiconductor switches in a CB/CFC can be further reduced compared to existing solutions. For completeness, the functionality of a CB/CFC and its corresponding control methods are verified through simulations conducted in PSCAD.

II. Topology of the CB/CFC

The CB/CFC configuration is shown in Fig. 2. It integrates a half-bridge based CFC [6] with multi-line HCBs [22] to reduce the number of semiconductor switches. Besides the low-loss and MB branches, a capacitor branch is included for current flow regulation. The series connected mechanical switch U_c and the semiconductor switch S_c are used to isolate the capacitor following a dc fault. It should be noticed that the stray inductances in high voltage systems could be quite large due to the considerable distance between devices compared to medium voltage or low voltage systems. Larger stray inductances within the commutation loop of the low-loss branch will lead to higher voltage stresses and higher switching losses for the IGBTs. Therefore, a symmetrical mechanical layout is recommended to be used in practical implementations of the CB/CFC so as to reduce the values of the stray inductances.

Fig. 3(a) shows a simple schematic of a dc terminal equipped with three HCBs and one CFC. Fig. 3(b), in turn, shows the use of a CB/CFC for the same dc terminal. Fig. 4(a) shows a meshed MTDC grid with four dc terminals and five transmission lines. Within such a dc grid, the dc current between converter terminals can flow through different paths. Overloading may occur when the current flows are not regulated properly. To fully manage the current flows in the grid and utilize transmission lines within their capability, two CB/CFCs are required to be installed in the dc terminals.

Fig. 4(b) shows a three-terminal meshed MTDC grid, which could be seen as part of the network of Fig. 4(a) (with T_4 and associated transmission lines being removed). Within such a grid, only one CB/CFC is needed to fully regulate the current flows. For the sake of simplicity, the MTDC grid shown in Fig. 4(b) is adopted in the paper to analyze the operating principles of the CB/CFC and to demonstrate its functionality.

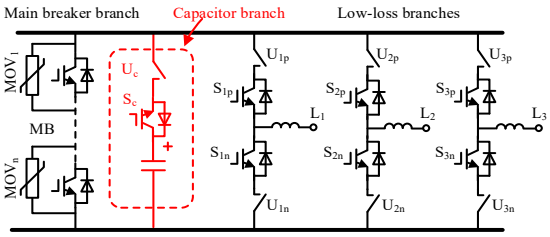

Fig. 2. Topology of the CB/CFC.

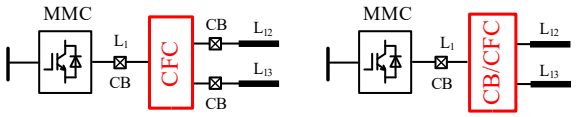

Fig. 3. HCBs with a CFC in one terminal of an MTDC system. (a) Separate HCBs and CFC. (b) Integrated device.

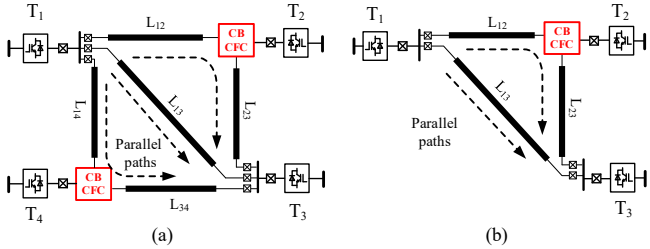

Fig. 4. Meshed MTDC grid with parallel paths. (a) Four terminals and five transmission lines. (b) Three terminals and three transmission lines.

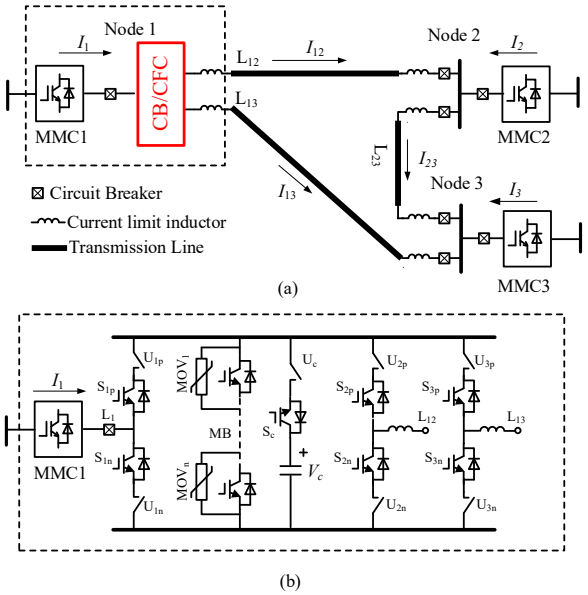

Fig. 5. System configuration with the presented CB/CFC in one terminal. (a) Meshed HVDC system. (b) Detailed configuration with the CB/CFC.

The use of the CB/CFC in the MTDC system is shown in Fig. 5. A bipolar system is employed, with only one pole being shown. Modular multilevel converters (MMCs) are adopted. The detailed CB/CFC configuration is given in Fig. 5(b). Converter MMC1 and transmission lines L_{12} and L_{13} are connected to the middle points of each low-loss branch.

During normal operating conditions, the CB/CFC operates as a CFC and, thus, regulates the currents of L_{12} and L_{13} to optimize system current flows. Once a dc fault is detected, the CB/CFC would operate as an HCB to interrupt fault currents.

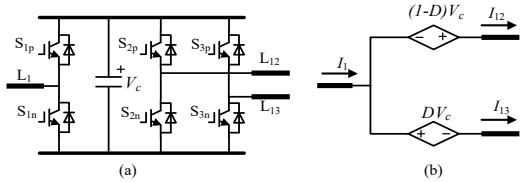

Fig. 6. Simplified CB/CFC circuit. (a) CFC operation. (b) Equivalent circuit.

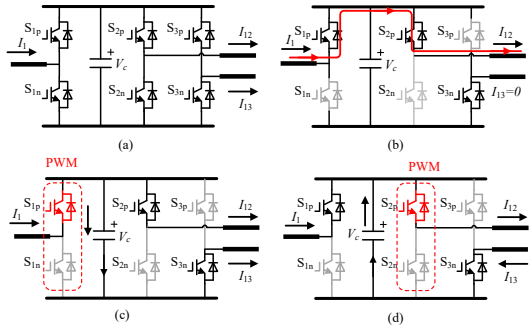

Fig. 7. Operating modes for CFC operation: (a) Bypass; (b) current nulling; (c) current sharing; (d) current reversal.

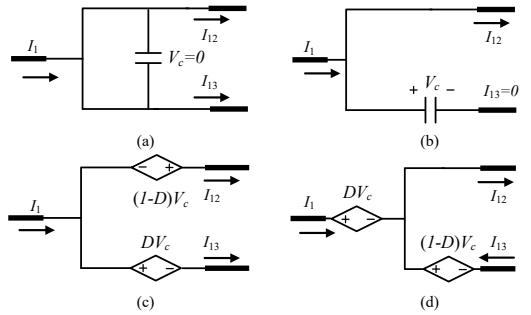

Fig. 8. Equivalent circuits under different CFC operating modes: (a) Bypass; (b) current nulling; (c) current sharing; (d) current reversal.

III. Current Flow Control Function

Fig. 6(a) shows the simplified circuit of the CB/CFC when the device operates as a CFC. In this case, mechanical switches U_c and $U_{ip,n}$ (i=1,2,3) are kept in an on-state and the MB is kept in an off-state. The capacitor is incorporated into the circuit by switching on S_c. By applying suitable control signals (i.e. PWM) to switches $S_{ip,n}$ (i = 1, 2, 3), the capacitor is selectively inserted in series with the transmission lines. This way, controllable dc sources are placed in series with L_{12} and L_{13} which, in turn, helps to regulate the current in these lines. This is shown in the equivalent circuit of Fig. 6(b).

A. CFC operating modes

Based on the relationship between the node current I_1 and the transmission line currents I_{12} and I_{13}, the half-bridge CFC has four operating modes, which will be discussed next.

1) Bypass mode

The CB/CFC operates in this mode when all switches $S_{ip,n}$ are kept in an on-state [see Fig. 7(a)], which bypasses the CFC capacitor. An equivalent circuit is shown in Fig. 8(a). In this mode, the CFC does not influence the current flows within the dc network. These are instead determined by the resistance of the transmission lines and the system's operating point, with

$$I_1 = I_{12} + I_{13} \tag{1}$$

The bypass mode can reduce switching losses of the CB/CFC when no demand for current regulation is needed.

2) Current nulling mode

The CB/CFC operates in this mode when the capacitor is fully inserted into one of the transmission lines; e.g. when S_{1p}, S_{2p}, and S_{3n} are kept in on-state and the other switches are in off-state [see Fig. 7(b)]. An equivalent circuit for this mode is shown in Fig. 8(b). By fully inserting the capacitor into L_{13}, I_{13} will be reduced to zero, and I_1 will flow through L_{12} only:

$$I_{12} = I_1, \quad I_{13} = 0 \tag{2}$$

This operating mode is useful whenever maintenance for a transmission line is required. Given that there is no need to switch off the corresponding HCBs to interrupt the current, surge energy in-rush to the HCBs is avoided.

3) Current sharing mode

The CB/CFC operates under this mode when the bridge connected with MMC1 (i.e. S_{1p} and S_{1n}) is regulated by a PWM signal [see Fig. 7 (c)]. When S_{1p} is on, the capacitor is inserted into L_{13} with a positive voltage V_c and it is charged by I_{13}. When S_{1n} is on, the capacitor is inserted into L_{12} with a negative voltage V_c and it is discharged by I_{12}. This way, two controllable dc sources are inserted into the two transmission lines.

An equivalent circuit is shown in Fig. 8(c). The average values of the dc voltages are determined by the duty cycle of the PWM signal. Considering the energy balance of the capacitor, the average current (charging and discharging) flowing through the capacitor within a period of the PWM should be zero in steady-state conditions:

$$I_{13}DT - I_{12}(1-D)T = 0 \tag{3}$$

where T is the period and D is the duty cycle of the PWM. Calculating (1) and (3), the line currents are derived as

$$I_{12} = I_1 D \tag{4}$$

$$I_{13} = I_1(1-D) \tag{5}$$

From (4) and (5), it can be seen that the line currents are regulated by D. Since D has a value between 0 and 1, I_{12} and I_{13} have a magnitude lower than the magnitude of I_1.

The current sharing mode can be used to distribute the node current between different transmission lines.

4) Current reversal mode

The CB/CFC operates in this mode when one of the bridges connected with the transmission lines is regulated by PWM. To explain the operation, the bridge connected with L_{12} is taken as an example [see Fig. 7(d)]. When S_{2n} is on, the capacitor is inserted to the node with a positive voltage and charged by node current I_1. When S_{2p} is on, the capacitor is inserted into L_{13} and discharged with current I_{13} (reversed direction).

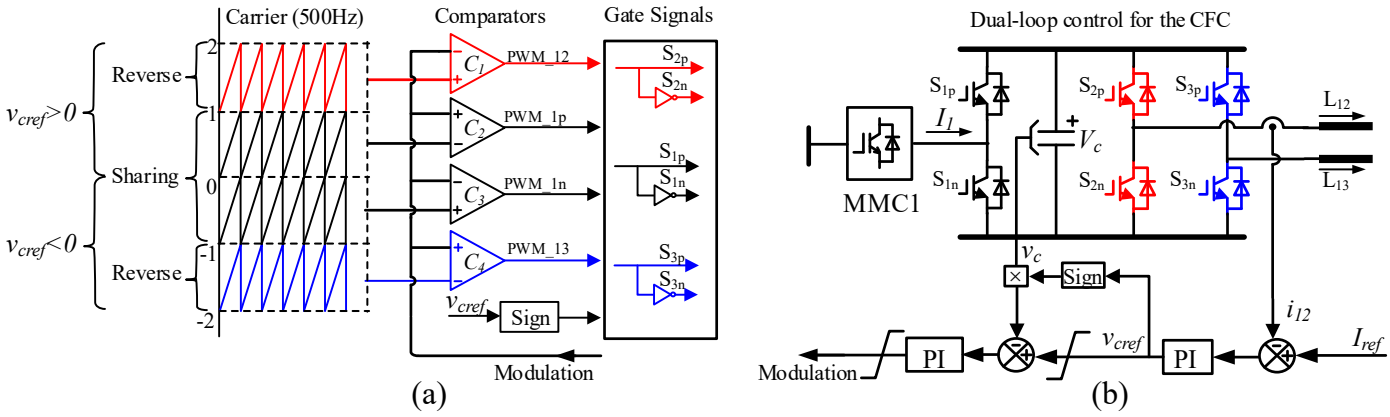

Fig. 9. Modulation and control for CFC operation. (a) Level-shift modulation. (b) Dual-loop control.

An equivalent circuit is shown in Fig. 8(d). Considering the energy balance of the capacitor, the following relationships are obtained:

$$I_1(1-D)T + I_{13}DT = 0 \tag{6}$$

$$I_{12} = I_1 / D \tag{7}$$

$$I_{13} = -I_1(1-D)/D \tag{8}$$

From (7) and (8), it can be seen that the line currents are regulated by D and, since D has a value between 0 and 1, I_{12} has a greater magnitude than that of I_1 and current I_{13} is reversed. Reversal of I_{12} is achieved instead when PWM is applied to the bridge connected with L_{13}.

The current reversal mode can be used to reverse the current flow in one of the transmission lines which, in turn, could prevent overloading of other transmission lines within a dc grid.

B. Modulation and control method

1) CFC Modulation

From Section III-A, it can be concluded that the current sharing and reversal modes can be implemented by applying a single PWM signal to a specific bridge of the CB/CFC. In line with this observation, a level-shift modulation method is adopted for a three-port configured CB/CFC.

Fig. 9 shows the modulation philosophy and its control diagram. The high frequency carriers used to generate PWM signals are level-shifted with each other to avoid interactions [see Fig. 9(a)]. This way, the modulation signal is compared with a single carrier in one specific area. Therefore, only one bridge is regulated by PWM signals. This can reduce switching losses compared to dual modulation methods as in [15].

2) Control method

Fig. 9(b) shows the dual-loop control for the CB/CFC. Line current I_{12} is fed back to its outer control loop and compared with its reference I_{ref}. Through a PI controller, the outer current control loop generates a voltage reference v_{cref} for the inner control loop. The capacitor voltage v_c is fed back and compared with v_{cref} to generate the modulation signal, thus, generate the duty cycles

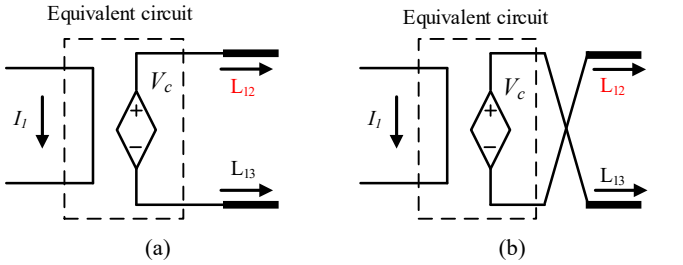

Fig. 10. Equivalent circuit of the CB/CFC when: (a) $v_{cref} \geq 0$; (b) $v_{cref} < 0$.

It should be noticed that the capacitor voltage V_c of the CFC cannot be regulated to a negative value due to the anti-parallel free-wheeling diodes within the semiconductor switches (i.e. IGBTs). However, if current I_{12} should be reduced, a negative voltage would be needed for current flow regulation. To solve this issue, a scheme based on the sign detection of the voltage reference v_{cref} is adopted [Fig. 9(b)]. When a negative v_{cref} is generated by its outer control loop, the on/off logic of the semiconductors switches is reversed; i.e. the positions of L_{12} and L_{13} are exchanged. This change produces an equivalent negative voltage, as shown by the equivalent circuits in Fig. 10. This transition process can be implemented by modifying the PWM signals based on the sign of v_{cref}.

To show the relation between the duty cycle and the control parameters, an equivalent system-level diagram with the CB/CFC is given in Fig. 11. Since the dynamics of current flow control are in the timescale of seconds, the transmission networks are represented by their equivalent inductances and resistances in series (capacitances are eliminated since they dominate the characteristics in a higher frequency range). The MMCs are represented by current and voltage sources. However, the PWM modulation of the CB/CFC is a nonlinear process when regulating current flows. To analyze the dynamic behavior of the CFC, a state-space averaging method is used to linearize the process to obtain the small-signal models [28]. Since there are two active operating modes (i.e. the current sharing and current reversal modes), separate transfer functions are obtained.

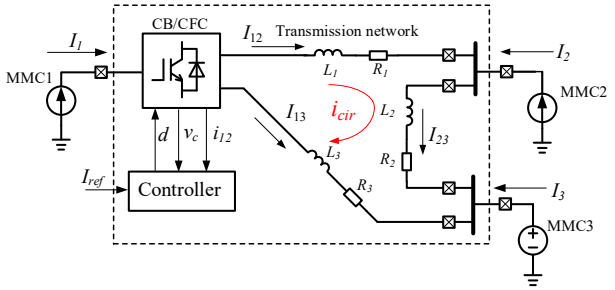

Fig. 11. Equivalent system-level diagram with the CB/CFC.

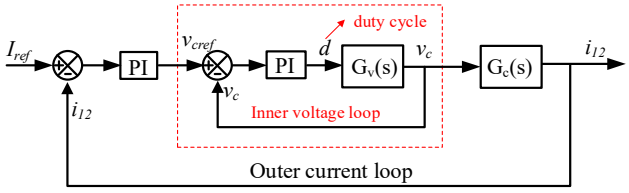

Fig. 12. Block diagram of the dual-loop control.

Under the current sharing mode, the transfer function $G_v^s(s)$ between the duty cycle d and the capacitor voltage v_c, and the transfer function $G_c^s(s)$ between v_c and output current i_{12}, are derived as:

$$G_v^s(s) = \frac{v_c(s)}{d(s)} = \frac{I_1(Ls+R)}{LCs^2+RCs+1} \tag{9}$$

$$G_c^s(s) = \frac{i_{12}(s)}{v_c(s)} = \frac{1}{Ls+R} \tag{10}$$

where C is the CFC capacitor, L the total inductance of the network (i.e. $L = L_1+L_2+L_3$), and R the total resistance of the network (i.e. $R = R_1+R_2+R_3$) [see Fig. 11].

Under the current reversal mode, the transfer function $G_v^r(s)$ between d and v_c, and the transfer function $G_c^r(s)$ between the v_c and i_{12}, are derived as:

$$G_v^r(s) = \frac{v_c(s)}{d(s)} = \frac{(Ls+R)I_{12}+(1-D)V_c}{LCs^2+RCs+(1-D)^2} \tag{11}$$

$$G_c^r(s) = \frac{i_{12}(s)}{v_c(s)} \approx \frac{D}{Ls+R} \tag{12}$$

where D and V_c are the steady-state values of the duty cycle and of the CFC capacitor voltage at a specific linearized operating point, respectively.

For clarity, the block diagram of the dual-loop control is given in Fig. 12. However, since the transfer functions of the CB/CFC under the two operating modes are different, both conditions need to be considered when designing the control system.

IV. DC Fault Isolation Function

The CB/CFC operates as an HCB when a dc fault is detected. A flow chart is given in Fig. 13 to clearly show the operation sequence of the fault isolation process. A fault occurring at L_{13} is taken as an example [see Fig. 14]. Waveforms for a typical fault interruption are given in Fig. 15.

1) *Pre-fault* (t_0-t_1)

Before the fault is detected, the CB/CFC operates as a CFC. The MB is kept in off-state and the mechanical switches are in on-state. Switches $S_{in,p}$ are regulated by their corresponding PWM. Currents can flow through both positive and negative buses. Fig. 14(a) shows the current path before a dc fault.

2) *Current commutation* (t_1-t_4)

When the fault occurs at $t = t_1$, the current in the faulted line L_{13} rises rapidly. At $t = t_2$, current i_{13} reaches the protection threshold:

$$i_{13}(t_2) = I_{13} + \frac{V_{dc}}{L_e + L_{CLR}} \times (t_2 - t_1) \tag{13}$$

where I_{13} is the initial current before the fault, V_{dc} is the rated dc voltage of the HVDC system, and L_e and L_{CLR} are the equivalent inductances of the VSC and of the current limiting reactor of the HCBs, respectively. When the fault is detected, S_c is switched off first to avoid discharging the CFC capacitor. After a short time delay (e.g. 100 μs), the MB is switched on to prepare for the current commutation process. After that, $S_{ip,n}$ are used to re-arrange the currents within the CB/CFC. For a fault at L_{13}, S_{3p} is switched off to force the current of the faulted line to flow through the negative bus only. At the same time, S_{1n} and S_{2n} are switched off to force the currents of the healthy lines to flow through the positive bus only [see Fig. 14(b)]. The process can be completed in hundreds of microseconds. At $t = t_3$, the fault current is fully commutated into the MB branch and its magnitude can be approximated with

$$i_{13}(t_3) = I_{13} + \frac{V_{dc}}{L_e + L_{CLR}} \times (t_3 - t_1) \tag{14}$$

In (14), the closest MMC (MMC1) is assumed to dominate the increment of fault current during the initial stage of the fault.

After the commutation processs, the mechanical switches U_{1n}, U_{2n}, U_{3p}, and U_c are switched off to isolate the low-voltage semiconductor switches to prepare for the fault interruption, as shown in Fig. 14(b). The mechanical switches are fully opened at $t = t_4$.

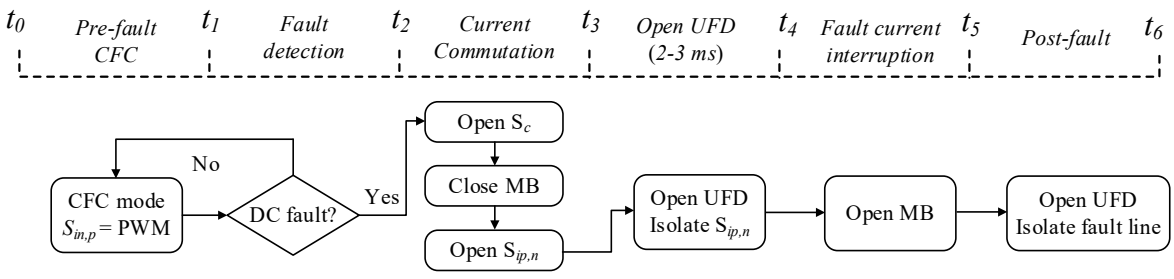

Fig. 13. Sequence of dc fault isolation for a CB/CFC.

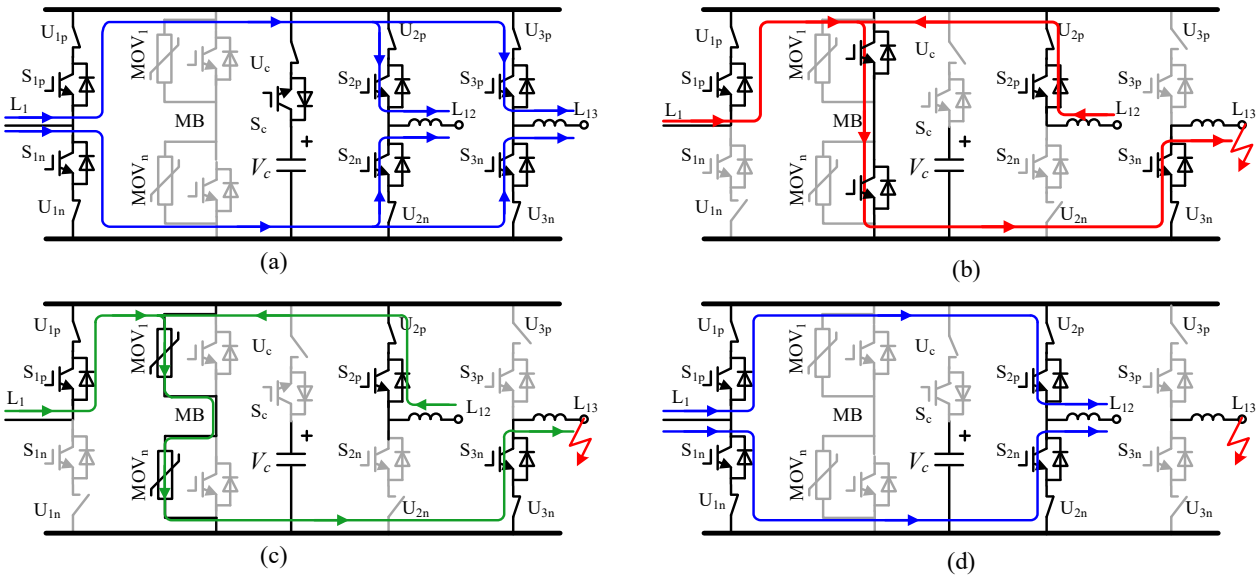

Fig. 14. Fault isolation process. (a) Pre-fault: (t_0-t_1). (b) Current commutation (t_1-t_4). (c) Fault current interruption (t_4-t_5). (d). Post fault (after t_5).

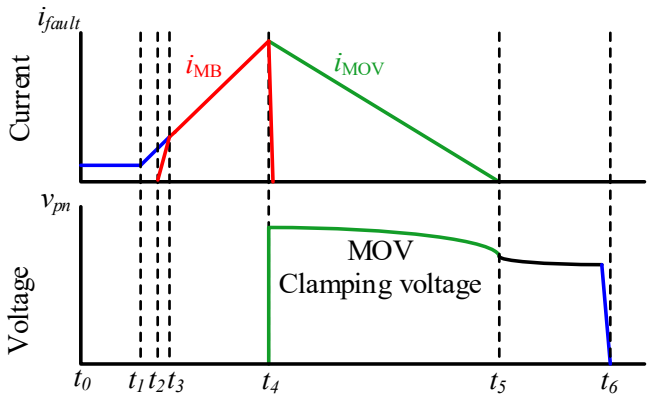

Fig. 15. Typical fault interruption fault current and voltage waveforms.

The maximum current in the MB is estimated as:

$$i_{13}(t_4) = I_{13} + \frac{V_{dc}}{L_e + L_{CLR}} \times (t_4 - t_1), \quad (15)$$

which can be used to select the current capability of the HCB (i.e. the maximum cut-off current of the CB/CFC). A worst case scenario should be considered for a practical project.

3) Fault current interruption (t_4-t_5)

The MB is switched off at $t = t_4$ after the mechanical switches are in their open-state. When the MB is switched off, the fault current is then transferred into the MOVs. Since the clamping voltage of the MOVs is higher than the rated dc bus voltage (normally 1.5 to 2 p.u.), the current in the MB will decrease to zero rapidly (at $t = t_5$, as shown in Fig. 15). The energy will be dissipated by the MOVs from t_4 to t_5. The energy rating of the MOVs may be estimated with

$$E_{MOV} = V_{MOV} \times I_{peak} \times \frac{(t_5 - t_4)}{2}, \quad (16)$$

where V_{MOV} is the residual voltage of the MOV and I_{peak} is the maximum cut-off current of the HCBs. It should be highlighted that the peak current, the residual voltage of the MOVs and the energy rating of the MOVs are the main parameters that should be considered when designing an HCB. As with the current capability, a worst case scenario should be considered for a practical project. However, given that the main focus of the paper is to analyze the principles and control of the CB/CFC, an optimal parametric design is not here considered.

4) Post fault (after t_5)

When the fault current reduces to zero at $t = t_5$, U_{3n} is switched off to permanently isolate the faulted line from the negative bus, as shown in Fig. 14(d). After this, the healthy line can be restored to its normal condition. The CB/CFC is ready to protect other lines against dc faults.

V. Simulations and Analysis

A. System Configuration in PSCAD

The meshed three-terminal MTDC system in Fig. 5(a) has been built in PSCAD/EMTDC to verify the operation and performance of the CB/CFC. Since the positive and negative poles in a bipolar system can be controlled independently, only one pole is simulated. Solid dc-side pole-to-ground faults are studied to verify dc fault isolation. The transmission lines are modelled as π sections in series and the maximum current capability of each line is assumed as 1.5 kA.

MMC1 regulates the dc voltage V_{dc} and its reactive power Q_1. MMC2 and MMC3 regulate their active and reactive powers (P_2 and Q_2, and P_3 and Q_3, respectively). The parameters of the dc grid are given in Table I. The parameters of the CB/CFC are given in Table II. The switching frequency of the CB/CFC is set as 500 Hz and a 10 mF capacitor is used. The rated voltage of the CFC is 5 kV. It should be noted that this value should be high enough in a practical application to complete the commutation process when isolating a dc fault, where current transfers from the low-loss branches to the MB branch. The voltage spike generated by the stray inductances should be also accounted for. In addition, since the CB/CFC injects a circulating current to the meshed grid, a higher resistance of the transmission lines will lead to a higher voltage rating. Therefore, the parameters of the CFC should be calculated accordingly in practical projects.

TABLE I
MTDC SYSTEM PARAMETERS

Parameter	Value
Rated dc voltage	500 kV
Rated power MMC1, 2, 3	1000 MW,1000 MW, 1500 MW
Transformer rated capacity	1200 MVA,1200 MVA,1800 MVA
Transformer ratio	500 kV/260 kV
Transformer leakage inductance	0.15 p.u.
Arm inductance	60 mH
SM Capacitor	18 mF
Number of SMs in each arm	250
DC current limiting inductor	300 mH /100 mH
Pi-section (per 40 km)	0.38 Ω, 84.4 mH, 0.46 μF
Capability of transmission line	1.5 kA
Length of Line 12, Line 13, Line 23	200 km, 200 km, 200 km

TABLE II
PARAMETERS OF THE CB/CFC

Parameter	Value
Maximum current interruption capability	20 kA
Maximum LCS current	20 kA
Rated CFC voltage	5 kV
Rated voltage of MBs/clamping voltage of MBs	500 kV/900 kV
Opening time of UFDs	2 ms
Switching frequency	500 Hz
Sampling frequency	20 kHz
Capacitor in the CB/CFC	10 mF

TABLE III
OPERATING POINTS OF THE MTDC SYSTEM

Operating point	Parameters	MMC1	MMC2	MMC3
Point A	Active power	500 MW	500 MW	–1000 MW
	Node current	1 kA	1 kA	–2 kA
Point B	Active power	1000 MW	500 MW	–1500 MW
	Node current	2 kA	1 kA	–3 kA
Point C	Active power	500 MW	1000 MW	–1500 MW
	Node current	1 kA	2 kA	–3 kA

B. Current Flow Control

Fig. 16 shows waveforms under the current sharing mode of the CB/CFC. The operating conditions are given in Table III. The system initially operates at point A and CFC functionality is not in service. MMC1 and MMC2 provide 1000 MW in total to MMC3. (i.e. $I_1 = 1$ kA; $I_2 = 1$ kA; $I_3 = -2$ kA). At $t = 3$ s, the system moves to point B. The active power of MMC3 increases from −1000 to −1500 MW and of MMC1 from 500 to 1000 MW [see Fig. 16(a)]. The converter currents are given in Fig. 16(b) and the currents of the transmission lines in Fig. 16(c). From Fig. 16(c), it can be seen that after the system changes its operating condition, I_{13} increases from 1 to 1.7 kA, which exceeds the capability of the transmission line (1.5 kA). At $t =$ 5 s, current flow regulation is enabled and I_{13} is regulated to 1.5 kA by the CB/CFC [see Fig. 16(c)]. Notice that the currents of the converters are not affected [see Fig. 16 (b)]. The additional current is transferred to L_{12} and L_{23} by the CB/CFC to balance the current flow.

As the direction of I_{12} and I_{13} is the same as that of node current I_1 and their magnitudes are smaller than that of I_1, the CB/CFC operates in a current sharing mode (Section III-A-3). The modulation and carrier signals are given in Fig. 16(d). As it can be observed, a single PWM signal is generated, which verifies the analysis in Section III.

An additional simulation is done to demonstrate the current reversal mode, with results shown in Fig. 17. As in the previous simulation, the system initially operates at point A and the CFC is out of service. At $t = 3$ s, the system moves to point C [see Fig. 17(a)]. The currents of the converters and of the lines are given in Figs. 17(b) and (c), respectively. It can be seen that following the change in operating point, I_{23} increases to 1.7 kA —exceeding the transmission line capability. At $t = 5$ s, current flow control is enabled and I_{23} is regulated to 1.5 kA, while the currents of the converters are not affected. The additional current is transferred to L_{12} and L_{13} to reduce the load of L_{23}.

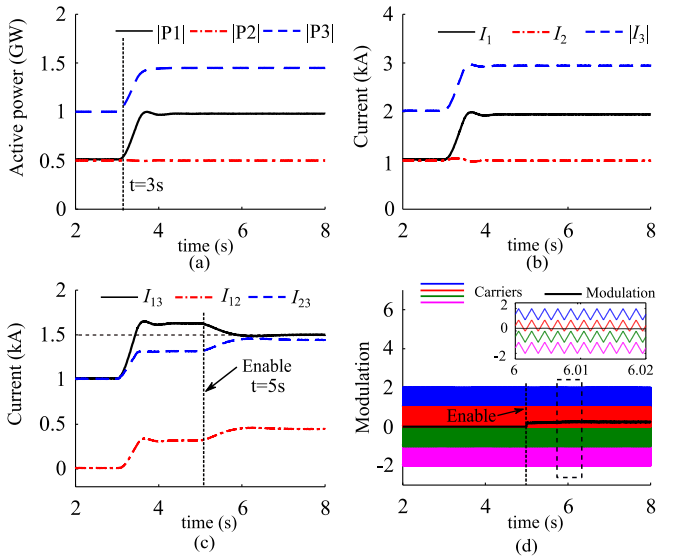

Fig. 16. Current sharing mode for CFC operation. (a) Active power of converters. (b) DC currents of converters. (c) Currents of transmission lines. (d) Modulation and carrier signals.

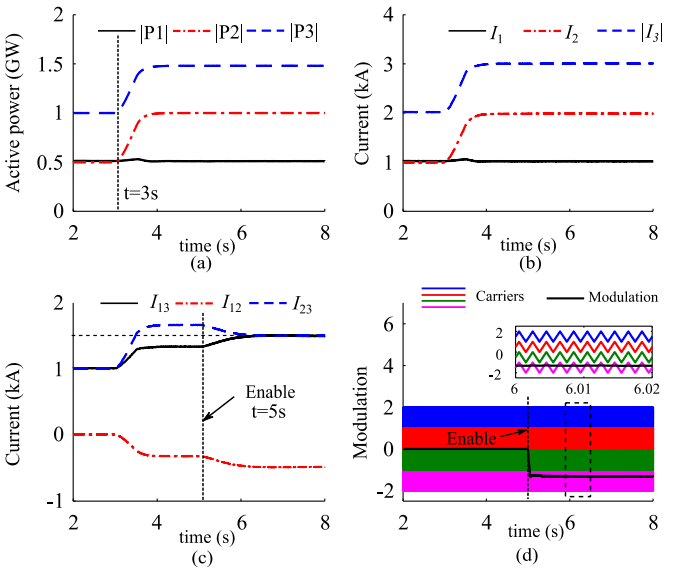

Fig. 17. Current reversal mode for CFC operation. (a) Active power of converters. (b) DC currents of converters. (c) Currents of transmission lines. (d) Modulation and carrier signals.

As the direction of current I_{12} is different from that of I_1 and the magnitude of I_{13} is higher than that of I_1, the CB/CFC operates in the current reversal mode (Section III-A-4). The modulation and carrier signals are given in Fig. 17(d). As it can be seen, a single PWM signal is generated.

C. DC Fault Isolation

To assess the operation of the CB/CFC for fault isolation, the system initially operates at point B in a current sharing mode (see Table II) before a dc fault occurs at $t = 3$ s. MMC1 exports 1000 MW to MMC3, and MMC2 sends 500 MW to MMC3.

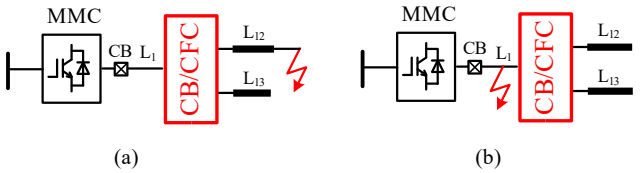

Fig. 18. Location of dc faults. (a) At the dc line. (b) At the dc terminal.

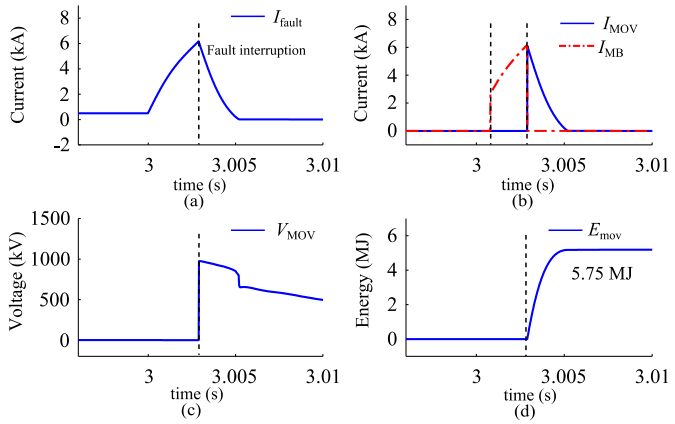

Fig. 19. Protection of dc faults at transmission lines. (a) Fault current. (b) Currents of MB and MOV. (c) Voltage of MB. (d) Energy absorbed by the CB/CFC.

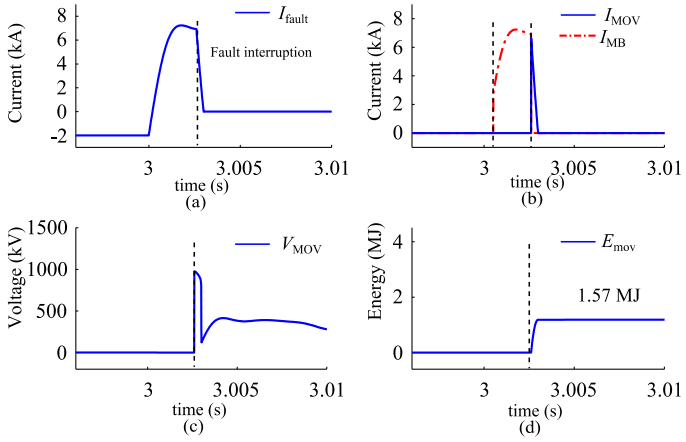

Fig. 20. Protection of dc faults at the terminal. (a) Fault current. (b) Currents of MB and MOV. (c) Voltage of MB. (d) Energy absorbed by the CB/CFC.

Fig. 19 shows the simulation results for a solid pole-to-ground fault at L_{12} [see Fig. 18(a)]. The current of the faulted line rises rapidly [see Fig. 19(a)]. When the current magnitude is over the protection threshold, the CB/CFC starts the fault interruption process. The fault current is transferred to the MB at $t = 3.0008$ s [see Fig. 19(b)]. After that, the corresponding ultra fast disconnectors (UFDs, see Fig. 1) are switched off within 2 ms to isolate the semiconductor switches. At $t \approx 3.0029$ s, the MB is switched off to interrupt the fault current (6.025 kA). The energy is absorbed by the parallel MOVs. As it can be observed, the fault current is reduced to zero at $t = 3.0052$ s. The voltage of the MOVs and energy absorbed by the MOVs are given in Figs. 19(c) and (d), respectively.

Fig. 20 shows the simulation results for a solid fault taking place at the terminal of Node 1 [see Fig. 18(b)]. As it can be seen, the current of the faulted line quickly increases [see Fig. 20(a)]. The CB/CFC starts the fault interruption process once the current magnitude is above the protection threshold. The fault current is commutated to the MB at $t = 3.0005$ s [see Fig. 20(b)], and the corresponding UFDs are switched off within 2 ms so as to isolate the semiconductor switches. At around $t = 3.0025$ s, the MB is switched off to interrupt the fault current (6.92 kA) and the parallel MOVs absorb the energy. This way, the fault current is reduced to zero at $t = 3.003$ s. Figs. 20(c) and (d) show, respectively, the voltage of the MOVs and the energy absorbed by the MOVs, for completeness.

The results presented in this section show that faults at a dc line and at a converter terminal can be successfully isolated using the presented CB/CFC.

VI. Comparison of Three Different Schemes

The CB/CFC presented in this paper is compared with two schemes available in the open literature which also integrate current flow regulation and dc fault isolation. Fig. 21 shows a schematic for each configuration.

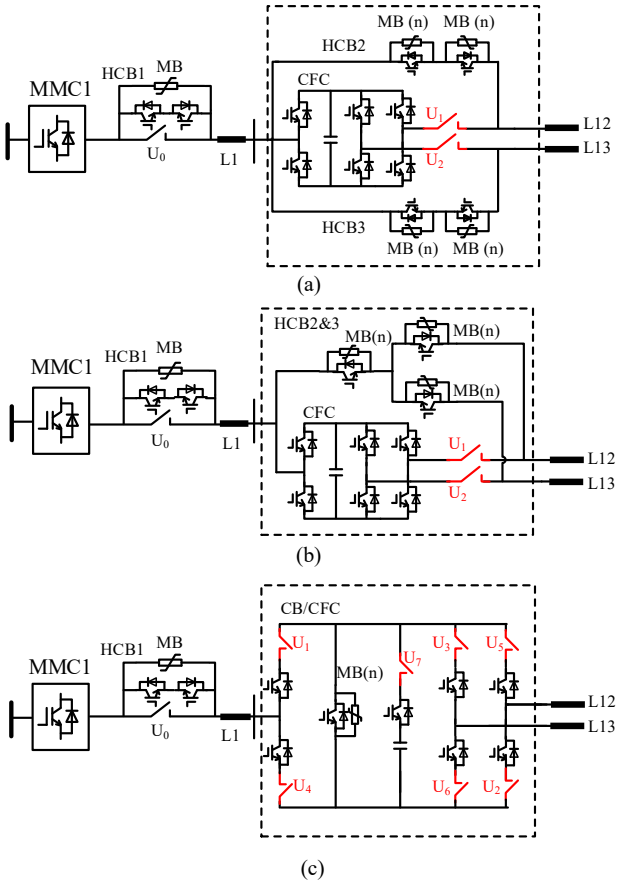

Fig. 21. Integrated schemes of CFC with HCB. (a) Scheme I: Sharing LCSs. (b) Scheme II: Sharing LCSs and MBs. (c) Scheme III: CB/CFC.

A. High Voltage Components

The scheme presented in [26] is shown in Fig. 21(a), where the LCSs of the two HCBs are combined to operate as a CFC. Compared to a traditional scheme with separate devices, the number of components can be reduced as there is no need to install a new CFC for current flow regulation. Fig. 21(b) shows instead the scheme presented in [27], where the MBs are also shared by the two HCBs in addition to the LCSs, which can further reduce around 25% of the total number of IGBTs. The CB/CFC scheme is given Fig. 21(c). Since the CFC and HCB are integrated into a single device, the MB is shared by three bridges and the use of a uni-directional branch is sufficient.

Based on the previous observations, the CB/CFC scheme can further reduce the number of IGBTs by approximately 50% when compared to a traditional scheme. This is complemented by Table IV, which summarizes the number of components for each configuration. It should be noted that, as opposed to the other two schemes, the CB/CFC uses additional mechanical switches (UFDs) to reduce the number of IGBTs. However, given that mechanical switches are much economic than MBs (which contain hundreds of IGBTs), the CB/CFC scheme renders a cost-effective and promising alternative for current flow regulation and dc fault protection.

TABLE IV
NUMBER OF HIGH VOLTAGE COMPONENTS

Scheme	No. of IGBTs	No. of UFD Units	No. of MOV Units
I	$4n$+6×4	2	4
II	$3n$+6×4	2	3
III	n+7×4	7	1

Note: n is determined by the residual voltage of MOVs and the cut-off current of the HCBs and n is in the level of hundreds for a 500 kV HCB [29].

B. Costs and Power Losses of MB Branch

1) Costs

To compare the three schemes, a 500 kV system is adopted as an example and the number of IGBTs and their costs calculated. Similar IGBTs are used in all cases. The price of a single IGBT rated at 4.5 kV/3 kA (5SNA 3000K452300) with its gate driver and snubber RCD circuit is assumed to be $9,000 [5], [29]. Table V shows the number of IGBTs and the projected cost of the MBs for each scheme. As it can be observed, Scheme III has the lowest cost, with a considerable reduction compared to Schemes I and II.

TABLE V
COST CALCULATION OF THE MB BRANCH FOR A 500 KV SYSTEM

Scheme	No. of MB units	No. of IGBTs	Costs (Million)
I	4	800×4 = 3200	$ 28.8
II	3	800×3 = 2400	$ 21.6
III	1	800×1= 800	$ 7.2

Note: 400 IGBTs are in series to withstand a transient voltage of 900 kV and 400 IGBTs are in parallel to withstand the fault current. Therefore, 800 IGBTs are considered per MB unit.

2) Power losses

Scheme III reduces the number of IGBTs in the MBs, which in turn do not generate conductive power losses as they are kept in an off-state under normal conditions. Thus, the switching losses and conduction losses for all three schemes are the same. However, since the number of the IGBTs is significantly reduced, the total power supply (static power supply, such as gate drivers, condition monitoring and communication system) to the MB's IGBTs is also reduced.

The power supply to each IGBT is assumed to be 5 W. Table VI summarizes the power supply to the MBs for each scheme. It can be observed that Scheme III requires the least amount.

TABLE VI
POWER LOSS EVALUATION OF MB BRANCHES

Scheme	No. of IGBTs	Power supply (Per IGBT)	Power supply (Total)
I	3200	5 W	16 kW
II	2400	5 W	12 kW
III	800	5 W	4 kW

C. DC Terminal Fault Isolation Process

When a dc fault occurs at the dc terminal, as shown in Fig. 22, Scheme III exhibits a different behavior from the other two schemes. For Schemes I and II, both MBs and UFDs connected with L_{12} and L_{13} should open to isolate the fault. L_{12} and L_{13} are also disconnected from each other and the current flow between them is interrupted [see Fig. 22(a)]. Conversely, only the faulted line L_1 is isolated following the fault in Scheme III. L_{12} and L_{13} are still connected and keep carrying the grid's current, which reduces the fault influence on the whole dc system [see Fig. 22(b)]. To verify the previous observations, a fault at the dc terminal for the three schemes is simulated at t = 3 s into the simulation, with results shown in Fig. 23.

Fig. 23(a) shows relevant waveforms for the fault isolation process of Schemes I and II. The fault current is reduced to zero at around t = 3.003 s. Soon after, the currents in L_{12} and L_{13} are also interrupted (and become zero). Fig. 23(b) shows the results for Scheme III. The fault current is reduced to zero at around t = 3.003 s as in the other two schemes. However, L_{12} and L_{13} still carry the grid's operating current (500 A) [see Fig. 23(b)]. The healthy part of the grid is thus less influenced when Scheme III is adopted compared to when Schemes I or II are used.

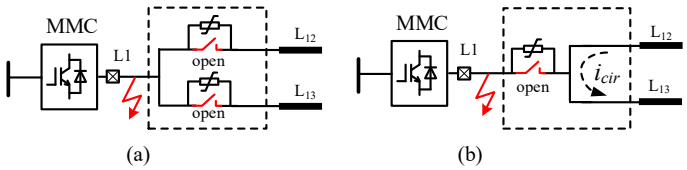

Fig. 22. Fault isolation at the dc terminal. (a) Schemes I and II. (b) Scheme III.

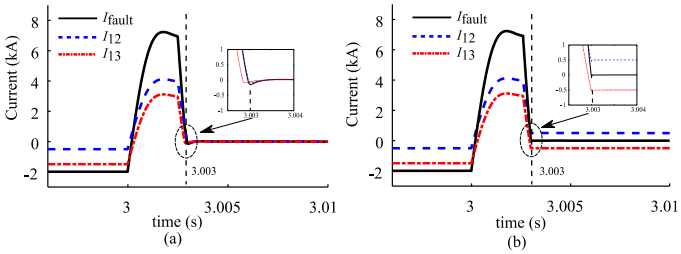

Fig. 23. DC terminal fault isolation waveforms. (a) Schemes I and II. (b) Scheme III.

D. Reliability Considerations

Although HCBs achieve a high interruption speed while exhibiting low power losses, reliability is an essential aspect to be considered as these devices comprise a large number of IGBTs (both in series and parallel) and several mechanical switches (UFDs). As shown in [30], Markov chains and an iteration method can be used to evaluate the reliability of such a device. A general analysis has been undertaken in this section to discuss reliability; however, a detailed assessment is not included and falls out of the scope of the paper.

1) Reliability of the MB branch

MB branches consist of hundreds of IGBTs in series and parallel to withstand high voltage and current following a fault, respectively. Such a large number of switches makes reliability a key feature to be considered when designing an HCB. The CB/CFC in Scheme III, given that it uses fewer IGBTs in its MB branch compared to the other two schemes, is thus more reliable when the IGBT's failure rate is considered only.

One way to increase the reliability of the IGBT-based MB branches is to use press-pack IGBTs (short-circuit failure mode) to keep the MB branch operating correctly under the failure of a single component. Meanwhile, redundant IGBTs (e.g. 10% redundant switches) could also be used to increase the reliability of the device.

2) Reliability of the low-loss branch

This should be considered since failure in the fault isolation process would be present when the UFD in the faulty line refuses to open [31]. Scheme III uses more mechanical switches (7 UFDs) than the other two schemes (only 2 UFDs) and, thus, has more chance to fail if one of the UFDs in the low-loss branches does not open following a fault. The other branches are not redundant in this case.

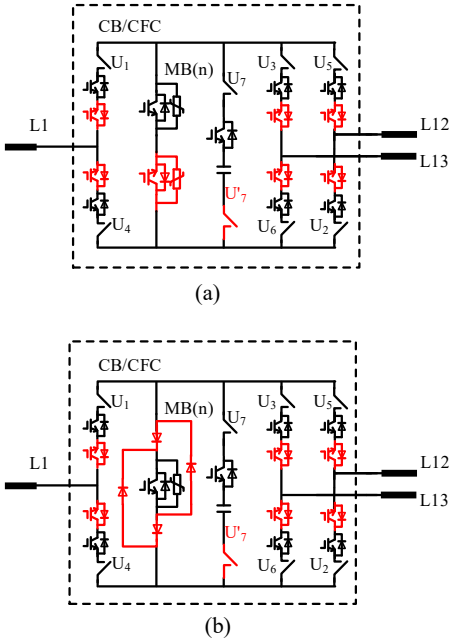

Fig. 24. Modified topologies of Scheme III with additional devices. (a) IGBT-based topology; (b) diode-based topology.

Modified topologies aimed to increase the reliability of the CB/CFC are given in Fig. 24. As shown in Fig. 24 (a), anti-series IGBTs (with red color) are added to ensure that the MB have the capability to interrupt bi-directional currents. This enables the other branches to be redundant following a single line fault. For instance, when a fault occurs at L_1, either opening U_1, U_6, U_2 or U_4, U_3, U_5 can isolate the fault, which provides further redundancy.

Although the number of IGBTs used in the modified topology shown in Fig. 24(a) is doubled compared to the original CB/CFC, this number is still less than that for the other two schemes. To further reduce the IGBT count, a diode-based topology is presented in Fig. 24 (b). A diode bridge is used to ensure that the MB has the capability to interrupt bi-directional currents. This topology would have a reduced cost as the price of diodes is much lower than that of IGBTs [25].

VII. Conclusion

Current flow regulation and dc fault protection remain important challenges restricting the widespread deployment of MTDC systems. In this paper, a power electronics based configuration addressing such issues has been presented. The CB/CFC integrates a multi-line HCB with a half-bridge based CFC into a single device. Such DCCB and CFC configurations have been chosen as they share similar topologies—facilitating their integration into a simple configuration which, in turn, leads to a reduction in the number of semiconductor switches. In addition, flexible controllability is enabled by the half-bridge topology of the CFC.

Simulation studies conducted in PSCAD demonstrate the successful performance of the integrated device. It has been shown that the CB/CFC has the capability of isolating dc faults either in transmission lines or directly at the node terminal where it is installed. To ensure an adequate current flow regulation functionality, a level-shift modulation and control method has been adopted. A significant benefit obtained from it is the possibility of current regulation irrespective of the direction of the current at interfacing transmission lines. This simplifies the overall control strategy of the device.

To show the advantages of the CB/CFC in terms of the semiconductor component count (and thus cost), a comparison was made with two other alternatives available in the open literature. Given the reduction in the number of IGBTs for a CB/CFC, the presented device represents a good option to achieve current flow regulation and dc fault protection—using a single integrated power electronics device.

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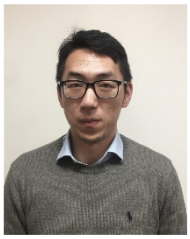

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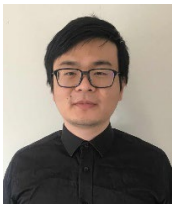

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