A Multi-Port Current-Limiting Hybrid DC Circuit Breaker

Jianzhong Xu, *Senior Member, IEEE*, Bingqian Song, Yu Lü, Chengyong Zhao, *Senior Member, IEEE*, Gen Li, *Member, IEEE*, and Jun Liang, *Senior Member, IEEE*

***Abstract*- Recently the hybrid multi-port DC circuit breaker (MP-DCCB) is becoming popular in protecting HVDC grids, thanks to their reduction of power electronics devices. In this paper, an enhanced multi-port current-limiting DCCB (MP-CLCB) for multiple line protection is proposed. The integrated fault current limiter (FCL) inside the MP-CLCB can clear the fault faster with slightly increased costs. To reduce the energy dissipation requirement for the surge arresters caused by the newly added current-limiting path, an energy transfer path which provides a loop with the inductors during the current decay stage is designed. The theoretical analysis of the pre-charging, current-limiting, fault interruption and energy dissipation of the MP-CLCB is carried out. Moreover, the design principles of the energy dissipation and the key parameters of the MP-CLCB are provided. The proposed approaches are verified through simulations in PSCAD/EMTDC. The results show that the MP-CLCB can replace multiple DCCBs, accelerate the fault current interruption and reduce the energy dissipation requirement for the surge arresters.**

Index Terms—HVDC grid; multi-port DC Circuit Breaker (MP-DCCB); fault current limiter (FCL); energy dissipation.

NOMENCLATURE

MP-CLCB	Multi-Port Current-Limiting Circuit Breaker
UFD	Ultra-Fast Disconnector
LCS	Load Commutation Switch
NCP	Nominal Current Path
MBP	Main Breaker Path
MBU	Main Breaker Unit
CLP	Current-Limiting Path
CPP	Capacitor Pre-charging Path
ETP	Energy Transfer Path

I. INTRODUCTION[1]

Recently, the modular multilevel converter (MMC) based high voltage direct current (HVDC) grid, which is formed by interconnecting multiple converter stations, is becoming popular due to their flexible operation and control in achieving a high penetration of renewable energy [1]-[3]. However, a DC grid has low inertia and impedance at the DC side, which results in its fast dynamic response [4]. DC fault currents may increase quickly following a DC short-circuit in the HVDC grid, which may damage the converters and other equipment.

Compared to the DC fault ride-through scheme using MMCs with self-blocking sub-modules (SMs), the DC circuit breaker (DCCB) based protection can ensure the selectivity of clearing the DC fault and a fast system restoration [5]-[7]. Hence, DCCBs may have a broad prospect in HVDC grids. Hybrid circuit breakers (HCBs) have lower on-state losses than solid-state DCCBs and faster fault current interrupting speed than mechanical DCCBs [8]-[9]. One of the classical configurations is ABB's HCB which consists of two paths: the nominal current path (NCP) and main breaker path (MBP) [10]. However, the extensive capital cost will be the bottleneck if DCCBs are installed at all lines connecting to a common DC bus [11].

Integrating the HCBs into one multi-port DCCB (MP-DCCB) can reduce the use of power electronic devices [12]-[15]. An interlink HCB for unidirectional and bidirectional interruption has been proposed in [12], which features its reduced sizes and costs. In [13], an integrated DCCB for meshed HVDC grids has been proposed, wherein the breakers connected to the same DC bus are merged into the proposed integrated DCB. However, they do not have the current limiting capability. The MP-DCCB in [14] utilizes the characteristics of HCB and reduces the number of components. However, overcurrent may be observed when the fault current flows through the lower arm of the faulty line. The MP-DCCB proposed in [15] embeds current limiting inductors and can effectively limit the rate-of-change of the DC fault currents. However, the remaining energy in the inductor may slow down the decay of the fault current and increase the energy dissipated by surge arresters (SAs).

It may take several milliseconds for MP-DCCB to interrupt the fault current. The rapid development of fault current may result in a large overcurrent. A fault current limiter (FCL) can limit the rate-of-change of the fault current and therefore, reduce the burden of DCCBs. The FCL based on power electronics devices can be classified into solid and hybrid categories [16], [17]. The solid FCL has high on-state losses and limited capacity. The hybrid FCL combines the advantages of power electronics and mechanical switches. Thanks to their fast development, hybrid DCCBs with current limiting capability are emerging. Reference [18] proposes an HCB that has different current limiting function for protecting permanent

This work was supported in part by National Key R&D Program of China under grant 2018YFB0904600 and in part by National Natural Science Foundation of China under grant 51607065 and 51777072.

J. Xu, Y. Lü and C. Zhao are with the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University (NCEPU), Beijing 102206, China.

B. Song is with the State Grid Nanjing Power Supply Company, Nanjing, China, 210000.

G. Li and J. Liang are with the School of Engineering, Cardiff University, Cardiff, CF24 3AA.

Corresponding authors: Gen Li*, LiG9@cardiff.ac.uk; Jun Liang*, LiangJ1@cardiff.ac.uk.

and temporary DC faults. However, this type of DCCB can only operates in low voltage DC systems.

The paper proposes a novel topology of the multi-port current-limiting DCCB (MP-CLCB) which combines the multi-port DCCB and FCL. The current-limiting path (CLP) uses high rating thyristors which are durable and economical as the main switch. The free-wheeling path proposed in [19] has been employed to accelerate the current decay in the SA. In the proposed MP-CLCP, an energy transfer path (ETP) by adding additional thyristors and capacitor to the path is employed to bypass the inductors and accelerate the fault current decay. The current commutation path in the proposed MP-CLCB shares the similar concept with ABB's hybrid breaker [20]. The main innovation of the proposed topology is to enhance the performance of such type of hybrid breakers through proposing the current limiting path which can reduce the fault current and the ETP which can dissipate energy in inductors [21]-[22]. In this case, the shunt columns of SA can be reduced, which is beneficial to the manufacture and its cost. Moreover, reducing the dissipated energy of the SA is very important to reduce the shunt columns of SA and therefore, will be beneficial to the manufacture and its cost. The operation principle of the proposed MP-CLCB is provided and its effectiveness is verified through simulations in PSCAD/EMTDC.

II. Topology and Operational Mechanism of the Proposed MP-CLCB

A. Existing Multi-Port DCCB

Fig. 1 shows the topologies and configurations of the conventional DCCB and the existing MP-DCCB [14] in a DC grid. It is shown that an MP-DCCB protects *n* lines connected to the same DC bus.

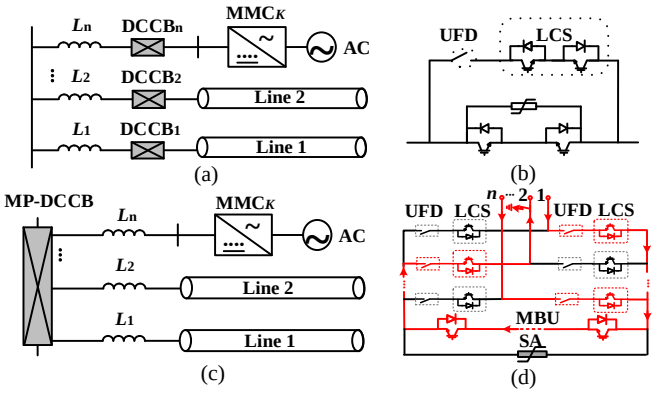

Fig. 1. Configuration of DCCBs and the MP-DCCB: (a) deployment of conventional DCCBs; (b) topology of the conventional HCB; (c) deployment of the MP-DCCB; (d) topology of existing MP-DCCB.

The current transfer process of the MP-DCCB [14] installed in Fig. 1(c) is shown in Fig. 1(d) in case of a fault in Line 2. During normal operation, current flows through both the upper and lower arms, which is equivalent to a parallel connection of the upper and lower arms. Thus, the on-state losses are less than the conventional DCCB. However, due to the lack of current-limiting capability, similar to the HCB, the MP-DCCB needs to interrupt a large fault current. To handle this issue, a DCCB with embedded FCL has been proposed in [20], which can limit the rate-of-change of the fault current and therefore, reduce the energy dissipated in the SA and the interruption time.

B. Topology of the Proposed MP-CLCB

The proposed MP-CLCB is shown in Fig. 2. The breaker consists of two main parts: the NCP and the main branch shared by all connected branches. Each NCP consists of an ultra-fast disconnector (UFD) and a load commutation switch (LCS). The UFD and diodes with large current ratings are connected between each NCP and the main branch. The main branch is composed of an MBP, a CLP, a capacitor pre-charging path (CPP) and an ETP.

The function of each path is: **CPP**- Charging capacitor C_{CLP}, which is required for current commutation among branches during current interruption; **ETP**- Improving dissipation energy in L_{dci} and L_{FCL} when the main breaker unit (MBU) is turned off; **MBP**- Commutating and interrupting fault current to help UFD_i and LCS_i turn off; **CLP**- Commutating current into the current-limiting inductor L_{FCL}.

The CPP, which is composed of resistor R_g, capacitor C_g and thyristor T_g, is to pre-charge the high-voltage capacitor under the DC voltage. As C_{CLP} and C_g will remain charged for a long time, resistive grounding preventing leakage currents is needed to clamp their voltages. The thyristor T_{g2} is applied to discharge C_g through the R_g. The utilization of T_{g2} might increase cost and size. However, the size and cost can be minimized by optimizing the system dimension and design.

The ETP consists of three parts: 1) Thyristor T_d, which is used to form a loop with the inductor. 2) Pre-charged capacitor C_{ETP}, whose discharging process provides a reversed turn-off voltage for T_d. Before operation, C_{ETP} will be pre-charged to about 1 kV through a power source, e.g. the laser energy charging technology. 3) Resistor R, which absorbs the energy of the capacitor. The MBP consists of an IGBT group and a SA group.

The CLP has three parts: 1) The thyristor valve group T_a, which is used to rapidly transfer the fault current to ensure the UFD can open at zero current. 2) The branch with parallel connected T_b and T_{g1}, and the pre-charging capacitor C_{CLP} with a paralleled surge arrester, which overall ensures the turn-off of T_a. Moreover, the reverse charging of the capacitor can store partial energy and limit the rate-of-change of the current. 3) The branch with the thyristor valve group T_c and the current limiting inductor L_{FCL}. As the line current limiting inductor L_{dci} (i=1, 2, …, n) may affect the dynamic characteristics of the DC system, L_{FCL} will not be inserted into the circuit during normal operation and will be inserted into the main path to suppress fault currents. L_{FCL} is used to limit the rate-of-rise of the fault current and therefore, reduce the voltage-of-rise of the capacitor C_{CLP}. In fact, the MP-DCCB could operate without L_{FCL}, as many DCCBs with parallel capacitors have been reported in the open literature. However, the DCCB without the FCL may cause overvoltage on C_{CLP}. To avoid the overvoltage, the capacitance of the C_{CLP} should be increased. However, this solution would in turn increase the volume and

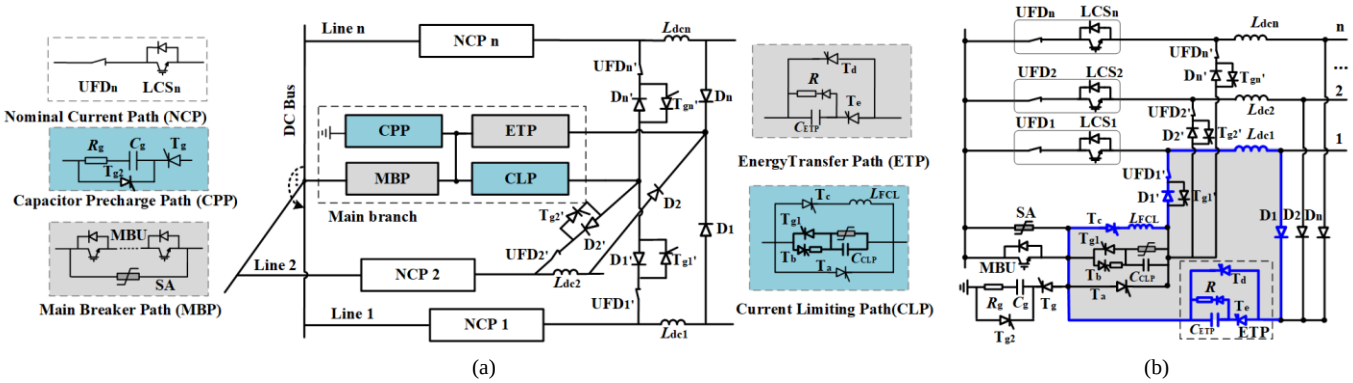

Fig. 2. Topology of the proposed MP-CLCB: (a) Modular view; (b) Detailed view.

cost. Therefore, the insertion of the L_{FCL} is an effective alternative solution. The selection of the DC reactance (L_{FCL} and L_{dci}) should be determined based on the overall system requirement and case-by-case, which needs an optimal design to minimize their volume [19]. For instance, the ratio of L_{FCL}/L_{dci} can be 1~3.

C. Operating Principle of the Proposed MP-CLCB

The operating principle of the MP-CLCB is illustrated in Fig. 3: (a) C_{CLP} and C_{ETP} are charged during normal operation. (b) The fault occurs at t_0; MBU operates at t_1; C_{CLP} begins to discharge at t_2; the voltage of C_{CLP} is reduced to zero at t_3; L_{FCL} is completely inserted into the circuit at t_4,. (c) At t_5, MBU is turned off. (d) At t_6, the current of the faulty line drops to zero and C_{ETP} starts to discharge; At t_7, the voltage of C_{ETP} is reduced to 0; At t_8, the energy stored in the inductors are completely dissipated. The four operating stages of the MP-CLCB are detailed as follows:

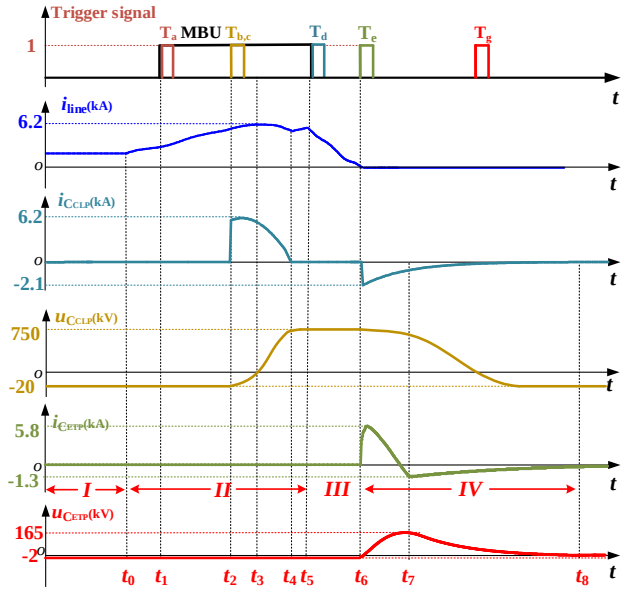

Fig. 3. The time sequence of the MP-CLCB.

a. Stage I (Normal operation)

In normal operation, all UFDs and LCSs are closed, MBP and ETP are bypassed, UFD$_i$' is closed to protect D_i' from overvoltage under DC faults, T_g, T_{g1} and T_{g1}' are turned on, C_g and C_{CLP} are charged. T_{g2}'…T_{gn}' are in backup modes in case that Line1 is out of service. For CPP and CLP, the currents through T_g and T_{g1} will reduce to zero when the charging process of C_{CLP} is completed. Then, the thyristors will turn off. C_{CLP} can remain its pre-charge voltage because T_{g1} and T_b are off.

b. Stage II (Current-limiting)

The processes are illustrated as the red solid lines and red dotted lines in Fig. 4(a). If a DC fault occurs on Line 1 at t_0, IGBTs in MBP and T_a of CLP will be turned on when the fault is detected at t_1'. The current flows through D_1'. After a short time delay, at t_1", a turn-off signal will be given to LCS_1 and UFD$_i$' (i=2,3...,n) of other branches. Then, the current in LCS_1 drops rapidly. At t_1, UFD_1 starts to open when the current in it is fully transferred to the MBU. To simplify the derivations in the theoretical analysis, it is assumed that t_1' = t_1" = t_1 because the turn-off time of IGBTs are short and can be ignored.

The operation of CLP is shown in Figs. 4(b)-(e). At t_2, UFD_1 is fully opened. Triggering signals will be kept sending to T_b and T_c until the thyristor is turned on. T_b is turned on due to the forward-biased voltage of the pre-charged capacitor. At the same time, C_{CLP} starts to discharge and T_a has to withstand the reversed voltage. T_a can be turned off after a short delay, as shown in Fig. 4(c). At t_3, the capacitor voltage reduces to 0, and then C_{CLP} is reversely charged. T_c is turned on due to the forward-biased voltage. The current flows through C_{CLP} begins to decrease when the voltage of C_{CLP} is higher than the DC voltage. At t_4, when the current flowing through the capacitor drops to zero, T_b will be turned off and L_{FCL} will be inserted into the circuit.

c. Stage III (Fault current decay)

At t_5, the current in the faulty line is measured. Then, the circuit status will be discriminated to determine if the breaker will keep open or return to normal operation. If the fault still exists, the MBU will be turned off at t_5, D_1 and T_d of ETP will be turned on at the same time. Then, the inductor current will be quickly transferred. The fault current will gradually decrease when the SA operates. The process is shown in the red solid and blue solid lines in Fig. 4(a).

d. Stage IV (Energy dissipation process)

The current path of this process is shown in Fig. 5. At t_6, T_e will be turned on when the current in the faulty line drops to

zero. Then, the pre-charged capacitor C_{ETP} starts to discharge. At the same time, T_d withstands a reversed voltage and will be is off after a short delay.

The current paths are shown in Fig. 5(b). At t_7, the capacitor voltage drops to zero. Then, the inductors form a loop with R and C_{ETP} wherein the capacitor is charged. The energy is dissipated through R. Thanks to the capacitor, the energy is rapidly transferred from the inductors, as shown in Fig. 5(c).

At t_8, the inductor current drops to zero. Then, D_1 and D_1' turn off and the energy stored in the inductors is completely dissipated. Finally, the capacitor dissipates the energy through the resistance, as shown in Fig. 5(d).

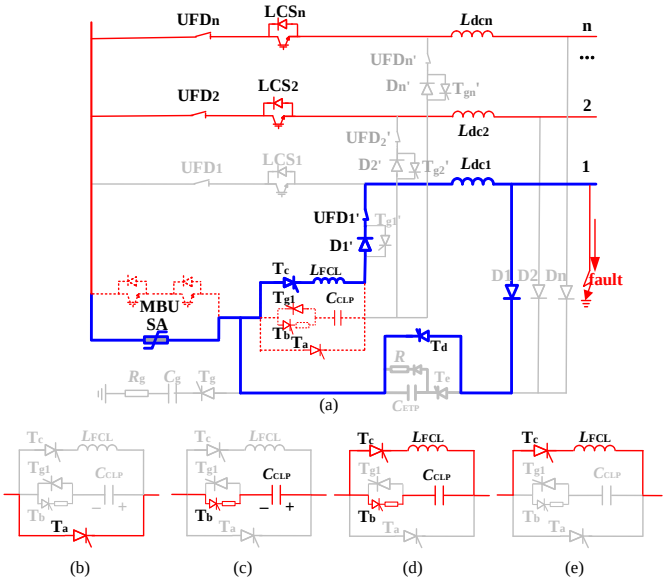

Fig. 4. Current paths of fault current limiting and decay processes: (a) t_1~t_6, (b) t_1~t_2, (c) t_2~t_3, (d) t_3~t_4, (e) t_4~t_5.

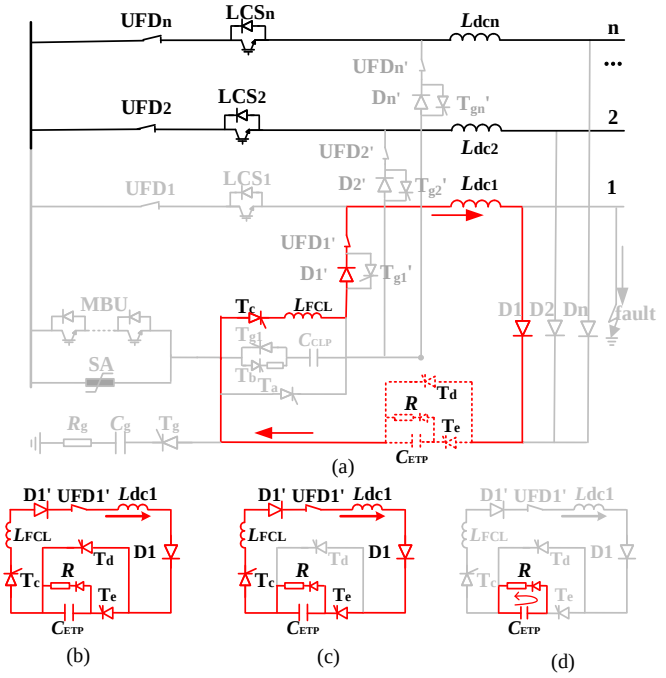

Fig. 5. Current path of the energy dissipation process: (a) t_6~t_9, (b) t_6~t_7, (c) t_7~t_8, (d) t_8~t_9.

D. Analysis of Multiple Fault Types and Reclosing Process

In Fig. 1, MMC_K is the converter station connected to the DC bus. Herein, the DC bus is defined as bus_K and the breaker is defined as MP-$CLCB_K$. If a pole-to-ground fault occurs on bus_K, the MP-$CLCB_K$ cannot clear the fault. Then, the faulty pole of the nearest converter station MMC_K will be blocked. Then, the backup protection should be activated and the lines 1 to n-1 will be interrupted by remote breakers MP-$CLCB_j$ (j=1, 2, ..., K-1) to interrupt all lines connected to bus_K. At the same time, the output power of MMC_K is reduced by a half, and the healthy pole remains operating. If the fault occurs on $line_n$, the $line_n$ should be interrupted by MP-$CLCB_K$ and MMC_K should be blocked. If faults occur on multiple lines (for example, lines i and j), the positive sides of the diodes (D_i and D_j) will withstand the bus voltage, and the negative sides of the diodes (D_i and D_j) will withstand the fault voltage. Then, the diodes (D_i and D_j) on the branches of the faulty lines will turn on. Differing from the single-line fault, during multi-line faults, multiple fault currents will flow into the MBU, which increases the level of its maximum current. Yet, the voltage across MBU does not change. Therefore, a parallel IGBT group connected with the MBU can be designed to protect multi-line faults.

Comparing with conventional HCBs, the multiport circuit breaker features in handling complex bus faults. It is because the DC bus is embedded in the MP-CLCB, which reduces the probability of a bus fault. Moreover, a DC bus fault can still be protected with the help from remote MP-CLCBs which can isolate the lines connected to the faulty bus. As for the remote MP-CLCBs, the fault on the faulty bus can be seen as a ground fault on the lines connected to the bus. Therefore, their primary protection will operate once the fault is detected. No backup protection is required.

The charging time for C_{CLP} is about 50 ms and the charging time for C_{ETP} is about 20 ms. Therefore, from the fault occurrence to the completion of energy dissipation, it takes 100 ms until the MP-CLCB can protect next fault. However, an important requirement of reclosing is that the UFD has been deionized, which takes about 200 ms [21]. This period is long enough for MP-CLCB to be initialized. Therefore, the proposed break would need roughly 200 ms to be ready for protecting next fault.

It is necessary to ensure that the mechanical switch UFD_1 is turned on at a low voltage [22]. Thus, the MBU and D_1' are turned on firstly. The voltage on NCP is then lowered after 2.5 ms when the UFD_1 starts to close. After 1 ms, when UFD_1 closes successfully, the LCS_1 will be turned on and the MBU will be turned off. Therefore, the mechanical operation time of the MP-CLCB is 3.5 ms.

Moreover, improving the reliable triggering of thyristors is a matter of concern. This issue relies on the industrial design and manufacture and may be addressed, for example, by optimization and/or employing special signal channels [23].

III. Theoretical Analysis of the Operation Process

A. Theoretical Model and Current Stress

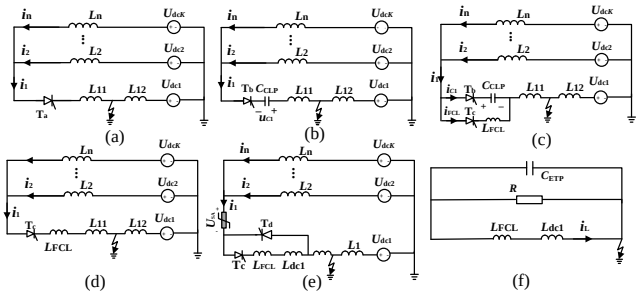

Fig. 6. Equivalent circuits during the current interrupting process: (a) t_0~t_2, (b) t_2~t_3, (c) t_3~t_4, (d) t_4~t_5, (e) t_5~t_6(f), t_6~t_8.

The stage-by-stage equivalent circuits during the fault interruption process are shown in Fig. 6.

In Fig. 6, L_i (i=2, 3…,n) is the sum of all inductances between the near converter to the remote DC bus. It includes the equivalent inductance of MMC$_K$, inductance of $L_{\mathrm{dc}i}$, and the equivalent line inductance of the lumped parameters of the transmission line model. L_{11} is the equivalent inductance from the fault point to the remote DC bus. L_{12} is the equivalent inductance from the fault point to the MMC$_K$. L_{FCL} is the inductance of CLP, and L_{dc1} is the line current limiting inductor. Each converter station is equivalent to a DC voltage source whose voltage is $U_{\mathrm{dc}i}$ (i=1, 2, …, K). Resistance of converters and lines, and the on-state voltage drop of each power electronics device are ignored as they are relatively small.

a. Analysis of stage I

During the steady-state, T_g and T_{g1} are on and the DC grid pre-charges the commutation capacitor. The thyristor is automatically turned off once the current drops to zero and the pre-charging process ends. The initial pre-charging voltage u_{10} can be adjusted by setting the parameter of C_g:

$$u_{10} = \frac{C_g}{C_g + C_{CLP}} u_{dc} . \tag{1}$$

b. Analysis of stage II

1) t_0~t_2

During the period of t_0~t_2, the fault current continues to rise through T_a in CLP, as is shown in Fig. 6(a). The steady-state current of the faulty DC Line 1 is denoted as $I_{1\mathrm{N}}$. Based on KCL and KVL, the fault current i_1 is expressed as:

$$i_1 = I_{1\mathrm{N}} + \frac{\Sigma_2}{1 + L_{11}\Sigma_1}(t - t_0) \tag{2}$$

where $\sum_1$ and $\sum_2$ are defined as:

$$\begin{cases} \Sigma_1 = \sum_{j=2}^{n} 1 / L_j \\ \Sigma_2 = \sum_{j=2}^{n} U_{\mathrm{dc}j} / L_j \end{cases}$$

2) t_2~t_3

At t_2, the capacitor C_{CLP} begins to discharge, and the faulty line current will be quickly transferred from T_a to C_{CLP}. The equivalent circuit diagram is shown in Fig. 5(b). The dynamic process of C_{CLP} discharge is described as:

$$\begin{cases} U_{\mathrm{dc}j} = L_j \dfrac{\mathrm{d}i_j}{\mathrm{d}t} - u_{C_{\mathrm{CLP}}} + L_i \dfrac{\mathrm{d}i_i}{\mathrm{d}t} \quad (j = 1...n, j \neq i) \\ i_i = -C_{\mathrm{CLP}} \dfrac{\mathrm{d}u_{C_{CLP}}}{\mathrm{d}t} \\ i_i = \sum_{j=1, j\neq i}^{n} i_j \end{cases}$$

Ignoring the time that the current through T_a drops to zero, and assuming that the current is transferred to the commutating capacitor immediately at t_2. Substituting t_2 into (2), it is obtained that $i_{C\mathrm{CLP}}(t_2)$=$i_1(t_2)$=I_2, then

$$\begin{cases} u_{C_{\mathrm{CLP}}} = \sqrt{A_1^2 + B_1^2}\sin(\beta(t - t_2) + \varphi_1) + D_1 \\ i_i = -\beta C_{\mathrm{CLP}}\sqrt{A_1^2 + B_1^2}\cos(\beta(t - t_2) + \varphi_1) \end{cases} \tag{3}$$

where all the variables are defined as:

$$\begin{cases} \beta = \sqrt{\Sigma_1 / C_{\mathrm{CLP}}(1 + L_{11}\Sigma_1)} \\ A_1 = \Sigma_2 / \Sigma_1 + U_0 \\ B_1 = -I_2 / C_{\mathrm{CLP}}\beta \\ \tan\varphi_1 = A_1 / B_1 \\ D_1 = -\Sigma_2 / \Sigma_1 \end{cases}$$

When designing the initial voltage and capacitance of the capacitor, the discharging process of (3) should be considered to ensure that $u_{C\mathrm{CLP}}$>0. This is to make sure that the reversed voltage is continuously applied on T_a until it is completely turned off.

3) t_3~t_4

At t_3, $u_{C\mathrm{CLP}}$ =0, the reverse charging of C_{CLP} starts, then T_c is turned on due to the forward voltage. The equivalent circuit diagram is shown in Fig. 6(c). The initial conditions are $u_{C\mathrm{CLP}}(t_3)$=0, $i_{C\mathrm{CLP}}(t_3)$ =$i_1(t_3)$=I_3, based on KVL, then:

$$\begin{cases} u_{C_{\mathrm{CLP}}} = \xi\sin(\gamma(t - t_3) + \varphi_2) - A_2 \\ i_{C_{\mathrm{CLP}}} = -\gamma C_{\mathrm{CLP}}\xi\cos(\gamma(t - t_3) + \varphi_2) \\ i_{\mathrm{FCL}} = (\xi\sin(\gamma(t - t_3) + \varphi_3) + A_2\gamma(t - t_3) + B_2) / L_{\mathrm{FCL}}\gamma \\ i_1 = i_{C_{\mathrm{CLP}}} + i_{\mathrm{FCL}} \end{cases} \tag{4}$$

where variables are defined as:

$$\begin{cases} A_2 = \Sigma_2 / [(L_1\Sigma_1 + 1) / L_{\mathrm{FCL}} + \Sigma_1] \\ B_2 = I_3 / C_{\mathrm{CLP}}\gamma \\ \xi = \sqrt{A^2 + B^2} \\ \tan\varphi_2 = A_2 / B_2 \\ \tan\varphi_3 = -B_2 / A_2 \\ \gamma = \sqrt{\dfrac{1}{C_{\mathrm{CLP}}}\left(\dfrac{1}{L_{\mathrm{FCL}}} + \dfrac{1}{C_{\mathrm{CLP}}(1/\Sigma_1 + L_{11})}\right)} \end{cases}$$

4) t_4~t_5

As C_{CLP} is charged, u_{C1} will gradually increase, and i_{C1} will

gradually decrease. When u_{C1} equals the system voltage, the line current begins to decrease, and u_{C1} will gradually rise above the system voltage. At t_4, i_{C1}=0, C_{CLP} is charged to the highest voltage, T_b turns off and the capacitor is thus disconnected.

After t_4, the fault current completely flows through the current limiting inductor, based on (4), $i_1(t_4)=I_4$. The equivalent circuit diagram is shown in Fig. 6(d). After t_4, the faulty current i_1 is expressed as:

$$i_1 = I_4 + \frac{\Sigma_2}{1+(L_{11}+L_{FCL})\Sigma_1}(t-t_4) \tag{5}$$

Compared with (2), the insertion of the current limiting inductor reduces the rate-of-rise of the DC fault current.

c. Analysis of stage III

At t_5, the MBU is turned off, and the T_d of ETP is turned on. When SA operates, and the fault current is gradually reduced. At time t_6, the fault current drops to zero, and the decay time of current is defined as Δt_{break}.

The faulty line current $i_1(t_5)=I_5$ can be obtained from (5), and the voltage during the operation of the SA is U_{SA}. During the decay of current:

$$i_1 = I_5 + \frac{\Sigma_2 - \Sigma_1 U_{SA}}{1+(L_{11}-L_{dc1})\Sigma_1}(t-t_5) \tag{6}$$

$$\Delta t_{break} = I_5 \cdot \frac{1+(L_{11}-L_{dc1})\Sigma_1}{\Sigma_1 U_{SA} - \Sigma_2} \tag{7}$$

The energy that the SA needs to be dissipated is:

$$E_{SA} = \frac{I_5^2 U_{SA}}{2} \cdot \frac{1+(L_{11}-L_{dc1})\Sigma_1}{\Sigma_1 U_{SA} - \Sigma_2} \tag{8}$$

The equivalent circuit is shown in Fig. 6(e). When the current begins to decay, I_5 is smaller than that without CLP. As can be seen from (7) and (8), the reduction of I_5 reduces the interruption time and energy dissipation of SA. Additionally, the ETP forms a loop with the inductors which results in the reduction of the interruption time and dissipated energy.

d. Analysis of stage IV

At t_6, the capacitor C_{ETP} of ETP starts to discharge. Ignoring the time that T_d's current drops to zero, then the DC inductor current is immediately transferred to the commutation capacitor at time t_6. It is obtained that $i_{C2}(t_5)=i_1(t_5)=I_5$, $u_{CETP}(t_6)=-u_{cETP,pre}$, $L_d=L_{dc1}+L_{FCL}$, the time interval from t_6 to the time when the voltage is zero at t_7 is Δt_{OFF}, and the time interval from t_6 to t_8 when the inductor current decays to zero is Δt_{att}. According to the equivalent circuit diagram shown in Fig. 6(f), it can be obtained:

$$\begin{cases} i_L(t) = I_5 \cos\dfrac{t-t_6}{\sqrt{C_{ETP}L_d}} + u_0\sqrt{\dfrac{C_{ETP}}{L_d}}\sin\dfrac{t-t_6}{\sqrt{C_{ETP}L_d}} \\ u_{C_{ETP}}(t) = I_5\sqrt{\dfrac{L_d}{C_{ETP}}}\sin\dfrac{t-t_6}{\sqrt{C_{ETP}L_d}} - u_0\cos\dfrac{t-t_6}{\sqrt{C_{ETP}L_d}} \\ \triangle t_{OFF} = \sqrt{C_{ETP}L_d}\tan^{-1}\left(\dfrac{u_0}{I_2}\sqrt{\dfrac{C_{ETP}}{L_d}}\right) \\ \triangle t_{att} = \sqrt{C_{ETP}L_d}\left(\pi + \tan^{-1}\left(-\dfrac{I_2}{u_0}\sqrt{\dfrac{L_d}{C_{ETP}}}\right)\right) \end{cases} \tag{9}$$

The total energy stored in inductors is:

$$W_L = \frac{1}{2}L_d I_5^2 \tag{10}$$

At t_7, u_{C2}=0, the discharge of C_{ETP} is completed. Then, the DC reactor starts to reversely charge the capacitor. When designing the initial voltage and capacitance of the capacitor, discharge process based on (9) needs to be considered. The interval Δt_{OFF} from t_6 to t_7 needs to be greater than the turn-off time of the thyristor to ensure that u_{C2} is over zero until T_d is turned off.

At t_8, the inductor current drops to zero, D_1' turns off and the capacitor C_{ETP} voltage rises to the maximum value. Then the resistor dissipates the residual energy. According to (9) and (10), the smaller the capacitance, the shorter the charging time and the faster the DCCB recovers. However, the maximum voltage across the capacitor increases accordingly. Hence, the capacitor parameters need to be properly designed.

B. Analysis of Voltage Stress

For each power electronic device, the LCS and the diodes are connected in series with the UFD, so the voltage is small. The maximum voltage U_{Tamax} of T_a is the forward voltage, which is equal to U_{C1max} of C_{CLP}. The maximum voltage U_{Tbmax} of T_b is the reversed voltage which is equal to the total voltage of U_{C1max} and the voltage across the current-limiting inductor. The voltage of T_c is small. The voltage across the MBU is up to the value of U_{SA}. Specifically:

$$U_{T_a max} = -U_{C1max} = -u_C(t_4) \tag{11}$$

$$U_{T_b max} = \left| U_{C_1 max} + \frac{L_{FCL}(\Sigma_2 - \Sigma_1 U_{SA})}{1+(L_{11}-L_{dc1})\Sigma_1} \right| \tag{12}$$

The voltage of ETP mainly depends on the inductance and capacitance. The maximum voltage U_{TDmax} of T_d is equal to the maximum voltage of the capacitor C_{ETP}, then

$$U_{C_2 max} = u_{C_2}(t_8) = I_5\sqrt{\frac{L_d}{C_2}}\sin\frac{t_8-t_6}{\sqrt{C_2 L_d}} - u_0\cos\frac{t_8-t_6}{\sqrt{C_2 L_d}} \tag{13}$$

Using the above equations, the next section will analyze the voltage and current stresses of the proposed MP-CLCB under specific parameters.

IV. Parameter Design and Economic Analysis

A ±500 kV four-terminal bipolar HVDC grid using half-bridge MMCs shown in Fig. 7 is used for the test. Eight MP-

CLCBs are deployed. L_{dci} (i=1, 2, …, n)= L_{FCL} = 0.15 H. C_{CLP} = 10 μF. The line inductance is 1.287 mH/km. The grid parameters are shown in Fig. 7. The t_{det} = 1 ms is the fault detection time, t_{UFD} =2 ms is the action time of UFD, and T_{off} = 60 μs is the turn-off time for T_a and T_d.

From the view of MP-CLCB1, the rated current of Line 12 is the largest among the three lines. The pole-to-pole fault marked in Fig. 7 is simulated. I_{12N} represents the pre-fault current of line 12, substituting DC grid parameters into the power flow calculation, it is obtained that: U_{dc1} = 512 kV, U_{dc2} = 501 kV, U_{dc3} = 514 kV, U_{dc4} = 500 kV, I_{12N} = 1.78 kA.

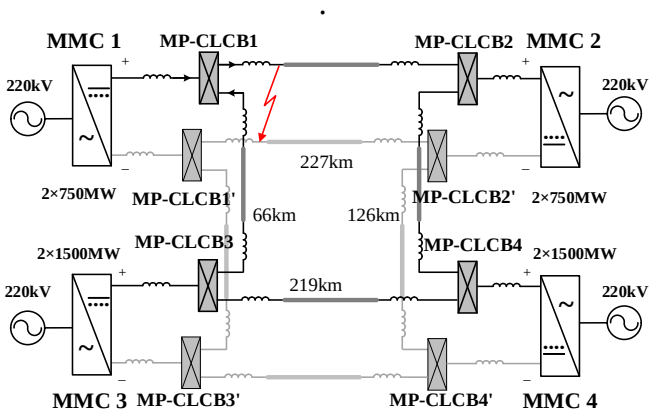

Fig. 7. Test system and locations of MP-CLCBs.

The number of IGBTs in MBP is determined by the maximum voltage and current. The 4.5 kV/3 kA high-power IGBT devices are selected. It is known from (7) and (8) that the larger the U_{SA}, the faster the current interruption and the smaller the energy dissipation of SA. However, the larger the U_{SA}, the more IGBTs are needed. In this paper, it is given that U_{SA}=800 kV. Considering 10% of voltage margin, the number of IGBTs in series for MBP is 196.

At t=t_0=0 s, the fault occurs. The time interval from t_0 to t_3 is the sum of t_{det}, t_{UFD} and T_{off}, i.e., t_3=t_0+t_{det}+t_{UFD}+T_{off}=3.6 ms. The capacitor discharge process has little effect on the fault current. Substituting t_0, t_3 and I_{12N} into (2), it is calculated that I_3=6.23 kA. Substituting I_3 to (4) and (5), it is obtained that I_5=5.82 kA. As the surge rating for a duration in the single digit millisecond range can be expected upwards 20 kA, the number of IGBTs in parallel with MBP is 1.

For DCCBs and MP-DCCBs, the required numbers of IGBTs are determined by the maximum current and voltage [24]. For both DCCBs and MP-DCCBs, the maximum voltage is 800 kV which is the same as MP-CLCB. The fault current calculated from (2) indicates that the current reaches the maximum value of 8.93 kA at time t_5. Considering the margin, the number of parallel IGBTs (4.5 kV/3 kA) is 1 and the number in series is 196. Therefore, the MBP of MP-DCCB needs 1×196 IGBTs. Taking the reversed fault current direction into consideration, the number of IGBTs for MBP of the DCCB is 1×196×2×n. Moreover, as shown in Fig. 1, a DCCB needs n UFDs and 2n LCSs, and a MP-DCCB needs 2n UFDs and 2n LCSs, where n is the branch number. The above comparison of the required IGBTs of each topology is given in Table I.

TABLE I
COMPARISON OF REQUIRED IGBTS

Items		DCCB	MP-DCCB	MP-CLCB
NCP	Parallel	3×n	2×3×n	3×n
	Series	2×3	3	3
MBP	Parallel	1×n	1	1
	Series	196×2	196	196
In total		410n	196+18n	196+9n

Compared with the conventional DCCB, the number of IGBTs saved by MP-CLCB is 401n-196. When n=2, the number of IGBTs is saved by 75.56%. When n=3, the number of IGBTs is saved by 81.87%. Compared with the MP-DCCB proposed in [14], the number of IGBTs saved is 9n. When n=2, the number of IGBTs is saved by 7.76%. When n=3, the number of IGBTs is saved by 10.80%, this comes at the cost of additional components.

According to (9), the value of C_{ETP} and the pre-charge voltage $u_{cETP,pre}$ will affect the capacitor discharge time Δt_{OFF}, the current-limiting inductor current decay time Δt_{att}, the thyristor maximum voltage U_{Tdmax}, the current-limiting inductor current i_L, and the capacitor voltage u_c. In order to visually show the influence of the two parameters, firstly, C_{ETP} is set as 500μF. Based on (9) and (13), the variations of each item under different values of $u_{cETP,pre}$ is shown in Fig. 8.

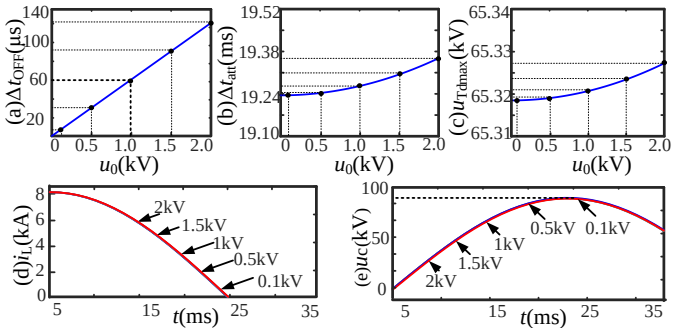

Fig. 8. Effect of $u_{cETP,pre}$: (a) Δt_{OFF}: time of the capacitor discharging, (b) Δt_{att}: decay time of inductor current, (c) U_{Tdmax}: maximum voltage of the thyristor T_d, (d) i_L: the current-limiting inductor current, (e) u_c: the capacitor voltage.

Figs. 8(a) to (c) illustrate the variation of Δt_{OFF} (discharge time of capacitor), Δt_{att} (decay time of inductor's current), U_{Tdmax} (maximum voltage of the T_a) with the pre-charge voltage $u_{cETP,pre}$. Figs. 8(d) and (e) show i_L (current of inductor) and u_C (voltage of the capacitor) when $u_{cETP,pre}$ is 0.1, 0.5, 1.0, 1.5 and 2.0 kV. Δt_{OFF}, Δt_{att} and U_{Tdmax} increase with the increase of $u_{cETP,pre}$. As i_L and u_C are less affected by the pre-charge voltage, the time for T_d to turn off plays a major role. Since T_{OFF}=60 μs, the capacitor discharge time is at least 60 μs, from Fig. 8(a), $u_{cETP,pre}$ needs to be over 1.0 kV.

Given that $u_{cETP,pre}$ is 2.0 kV, the values of each item are calculated based on (5), then the effect of C_{ETP} is shown in Fig. 9. Figs. 9(a) to (c) illustrate that the variation of Δt_{OFF}, Δt_{att}, U_{Cmax} (the maximum voltage of the capacitor) varies with the value of capacitor C_{ETP}. Figs. 9(d) and (e) visually show that the development of i_L and u_C when the capacitor value is 100, 200, 300, 400 and 500 μF. As the capacitance increases, Δt_{OFF} and Δt_{att} increase. Therefore, C_{ETP} cannot be too large.

However, as the capacitance value decreases, U_{Cmax} increases, and the requirement of the voltage capability of T_d and C_{ETP} increases. Based on Fig. 9(c), the smaller the capacitance value, the larger increase rate of the maximum voltage will be. Therefore, the capacitance value should be selected in the range of 250-350 μF.

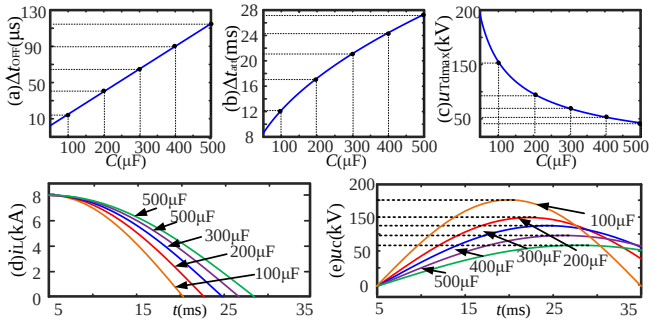

Fig. 9. Effect of C_{ETP}: (a) Δt_{OFF}: time of the capacitor discharging, (b) Δt_{att}: decay time of inductor current, (c) U_{Tdmax}: maximum voltage of the T_d, (d) i_L: the current-limiting inductor current, (e) u_c: the capacitor voltage.

In this paper, the capacitance of C_{ETP} is 300 μF, the pre-charge voltage $u_{cETP,pre}$ is 2 kV, and the maximum current of ETP is close to the initial value of I_5. At time t_7, the inductor current drops to 0, D_1 turns off, and the voltage of C_{ETP} rises to the maximum value. Substituting the parameters into (9) and (13), the maximum current of the energy transfer path is 5.83 kA and the maximum voltage is 165.3 kV.

Further, according to (8) and (10), when the current is interrupted, the energy that the SA dissipates is about 10.97 MJ. The energy that ETP absorbs is 29.05 MJ. It indicates that the proposed MP-CLCB reduces the SA capacity by 72.59%. As the large capacity of SA requires a large number of insulator columns in series and parallel, the problem of voltage and current equalization in the complex electromagnetic transient process is one of the bottlenecks [22] that limit the capacity increase of the SA. Moreover, the introduction of the energy transfer path can effectively extend the service life of the SAs. It can be seen that, compared with the existing MP-DCCB proposed in [14], the MP-CLCB not only saves the number of IGBTs but also effectively reduces the capacity of the SA at the cost of additional components.

For D_1'- D_n' and D_1- D_n, the diode model is D2601N90T whose rated voltage is 9 kV and design voltage is 4.5 kV. For CLP and ETP, 5STB18U6500 thyristor is adopted in MP-CLCB [25]. Its rated voltage and current are 6.5 kV and 1.5 kA. It can withstand 29 kA maximum surge current for not more than 10 ms. Taking the voltage margin into account, the design voltage of the thyristor is 3.25 kV [12]. As is given in Table II, the number and requirement of each component are given based on its voltage and current need to withstand.

TABLE II
REQUIREMENT OF THE MAIN COMPONENT

Components	Voltage	Current	Number	Total
D_1'- D_n'	10 kV	6.2 kA	3*n*	Diode
D_1- D_n	10 kV	5.8 kA	3*n*	6*n*
T_a	750 kV	6 kA	230	Thyristor 263
T_b	20 kV	6.2 kA	6	
T_c	20 kV	6.2 kA	6	
T_d	65.3 kV	6.2 kA	20	
T_e	2 kV	5.8 kA	1	
C_{CLP}	Value: 50μF; Voltage requirement: 750 kV.			
C_{ETP}	Value: 300μF; Voltage requirement: 165.3 kV.			
R	Energy dissipation requirement: 31.05 MJ.			

V. Simulation and Verification

The system shown in Fig. 7 is used in the simulation, the parameters and scenarios are the same as Section III.

A. Verification of Current Suppression

Currents of the lines connected to the MP-CLCB1 are shown in Fig. 10. In steady state, MMC2 and MMC3 work in the rectifier mode, and MMC1 receives power. As the healthy Lines 2 and 3 are far away from the fault point, the fault current rises slowly. Therefore, the currents of Lines 2 and 3 are only slightly limited by using MP-CLCB. The current of Line 1 is cleared after effective fault current limiting. Fig.10 shows 3 cases: (a) the MP-CLCB operates; (b) only the circuit breaker operates without triggering the current limiting function; (c) the circuit breaker does not operate. Compared with the case where the circuit breaker does not operate, the fault is cleared very fast. Compared with the case where only the circuit breaker operates, the maximum value of the fault current is reduced.

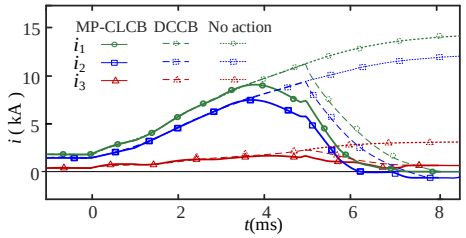

Fig. 10. Line currents of MP-CLCB ports.

The currents flow through the paths of the MP-CLCB and the voltage of main components are shown in Fig. 11. At time t_0=1.5s, the fault occurs, and the fault line current i_1 rises rapidly. After 1 ms, T_a and the IGBTs of the main breaker path are turned on. After a delay of 100μs, at time t_1"=1.1 ms, LCS_1 is turned off, the current in LCS_1 drops rapidly. At time t_1= 1.2 ms, the current is less than the residual current of the corresponding UFD, and UFD_1 starts to open. The red dotted line in Fig. 11 shows that the results calculated in MATLAB match well with the simulation results. It can be seen from Fig.11(e) that, after the fault has been cleared, the system will recover to a new steady state in about 150 ms which is faster than the case where only the regular DCCB operates. Fig.11(f) shows the voltage of C_{CLP}, the voltage that C_{CLP} needs to withstand is about 750 kV. Fig.11(g) shows the voltage of C_{ETP}, when the current in the inductor drops to 0, the voltage of C_{ETP} is the largest, about 165.3 kV.

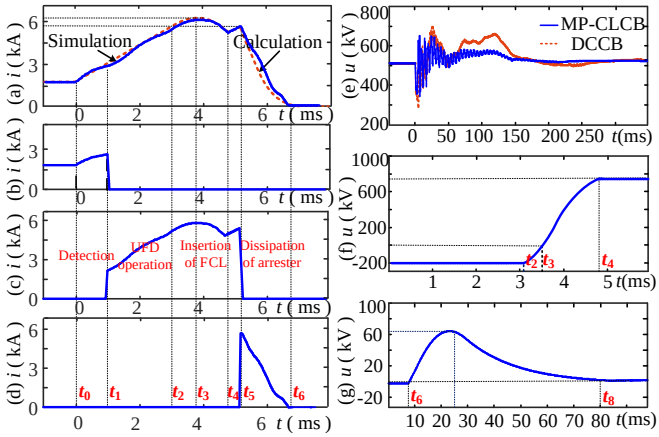

Fig. 11. Current and voltage of main components of MP-CLCB: (a) Line 1, (b) NCP, (c) MBU, (d) SA, (e) DC Bus, (f) C_{CLP}, (g) C_{ETP}.

B. Verification of Current Decay Process

The current of the inductors and the capacitor of ETP is shown in Fig. 12. At time t_2=3.2 ms, the UFD_1 is fully open, T_b and T_c receive turning-on signals. T_b is turned on due to the forward voltage. The capacitor C_{CLP} starts to discharge and then is reversely charged. At time t_4=4.8 ms, the capacitor current drops to 0, and L_{FCL} is completely inserted into the faulty circuit. At time t_5=5.3 ms, SA operates, L_{FCL} and L_{dc1} are bypassed. The fault line current is reduced to 0 and the system fault is cleared at time t_6=6.7 ms. The capacitor of ETP begins to absorb the inductor energy after a short period of discharging for 60 μs. At time t_7=28 ms, the inductor current drops to 0, CLP returns to the initial state. At time t_8=80 ms, the energy dissipation stage is completed.

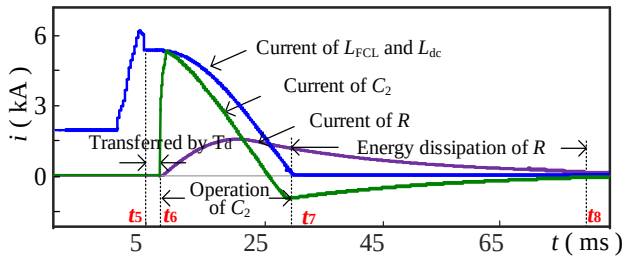

Fig. 12. Internal current of ETP.

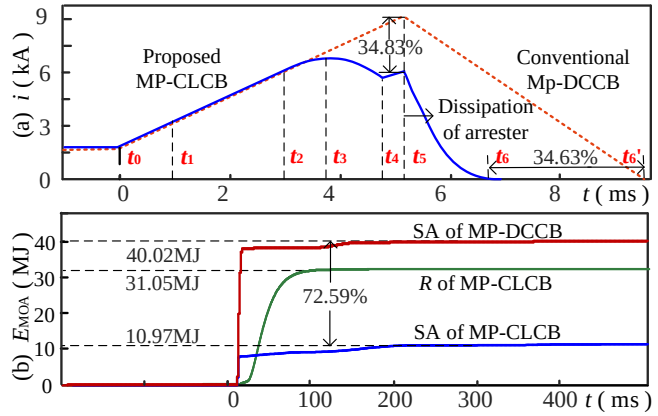

Fig. 13. Comparison of the existing MP-DCCB and MP-CLCB: (a) fault current of line1, (b) energy dissipation of SA and *R*.

In order to verify the effectiveness of current limiting and energy dissipation of the proposed MP-CLCB, the results are compared with the MP-DCCB proposed in [14]. The comparison of the fault current and the energy dissipation of the SA is shown in Fig. 13.

As seen in Fig. 13(a), compared with the MP-DCCB proposed in [14], the proposed MP-CLCB can reduce the fault current by 34.83% when the SA starts to operate, which can significantly reduce the current stress on each device. The time from when the fault occurs until the faulty line current drops to zero is shortened by 34.63%. As shown in Fig. 13(b), the overall energy dissipation from MP-CLCB's SA and R is similar to the energy dissipated by MP-DCCB's SA. The additional dissipated energy in MP-CLCB is caused by the deployment of the L_{FCL} which also stores energy. The proposed MP-CLCB reduces 72.59% of the energy to be absorbed by R, which can also reduce the energy consumption requirement of SA. Thanks to the installation of the ETP, the energy dissipation of the inductors is independent from the operation of the grid. The energy dissipation of inductors will also not influence the isolation processes of the faulty line. It is because that the fault isolation process of the breaker is much faster than the period of the energy dissipation. Thus, compared with the complete dissipation in the SA, the fault current on the line decays more quickly, enabling the faulty line to be removed from the system faster. Thus, the system can restore more quickly.

C. Verification of Reclosing Process

The charging time for C_{CLP} is about 50 ms and the charging time for C_{ETP} is about 20 ms. From the fault occurrence to the completion of energy dissipation, it takes 100 ms until the MP-CLCB is able to interrupt next fault current. The deionization time of the MP-CLCB is about 200 ms. In the simulation, the reclosing process after clearing the fault is verified as shown in Fig. 14.

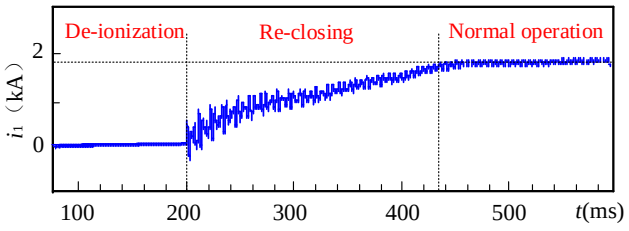

Fig. 14. Line current during the post-fault restoration.

At time *t*=200 ms, the MBU and D_1' on the branch are firstly turned on. The voltage on NCP is lowered after about 2.5 ms, at that time UFD_1 starts to close. After about 1 ms, when UFD_1 closes successfully, the LCS_1 is turned on and the MBU is turned off. At *t*=435 ms, the NCP and Line 1 are restored to the rated operating state. Then, the insulation level of the faulty line is restored. No overcurrent flows through the MBP and the MP-CLCB completes the reclosing process successfully.

VI. Conclusions

In this paper, a multi-port current-limiting DC circuit breaker (MP-CLCB) is proposed. The topology, operation process, parameter design and economic analysis are provided. Conclusions are drawn as follows:

By using the main breaker path, the MP-CLCB can reduce the number of DCCBs and FCLs on healthy lines. Compared with the conventional DCCB, the MP-CLCB reduces at least 75.56% of IGBTs at the cost of additional components. In a four-terminal MMC-HVDC system, when the SA starts to operate, the faulty line current is reduced by 34.83% compared with the existing MP-DCCB.

The overall energy dissipation by the SA and *R* of the MP-CLCB and by the SA of the MP-DCCB is very similar. However, as the energy dissipation of the SA is assisted by the ETP, the energy dissipation of the SA is reduced by 72.59% compared with the existing MP-DCCB, which significantly reduces the demand for the capacity of SA. The time used to clear the fault is reduced by 34.63% compared to MP-DCCB, which increases the fault current interruption speed. The MP-CLCB needs 80 ms to be ready for the next fault clearance and can reclose within 3.5 ms after the de-ionization process.

Although the proposed MP-CLCB can save numerous IGBTs, it does involve additional components such as capacitors and thyristors which may increase the capital cost. In addition, the added subsystems may influence its reliability in terms of malfunction and wrong signal. Hence, it is worthy of figuring out the trade-off of cost, complexity and reliability without sacrificing the fault protection capability. Moreover, it should be also highlighted that the impact of the triggering delays of different stages and the thyristor recovery behavior on the performance of the topology, although highly desirable to verify its robustness, falls out of the scope of this paper. Last but not least, the internal signal communication of the proposed breaker should be properly designed to avoid the malfunction of power electronics devices and therefore improve its reliability. It would be the future work of the optimal design of the proposed circuit breaker.

References

[1] C. Li, C. Zhao, J. Xu, Y. Ji, F. Zhang and T. An, "A Pole-to-Pole Short-Circuit Fault Current Calculation Method for DC Grids," *IEEE Trans. Power Syst.*, vol. 32, no. 6, pp. 4943-4953, Nov. 2017.

[2] G. Li, J. Liang, F. Ma, C. E. Ugalde-Loo and H. Liang, "Analysis of Single-Phase-to-Ground Faults at the Valve Side of HB-MMC in HVDC Converter Stations," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2444-2453, March 2019.

[3] Y. Wang *et al*., "Generalized protection strategy for HB-MMC-MTDC systems with RL-FCL under DC faults," *IET Gen. Transm. Distrib.*, vol. 12, no. 5, pp. 1231-1239, 13 3 2018..

[4] S. Wang, C. Li, O. D. Adeuyi, G. Li, C. E. Ugalde-Loo and J. Liang, "Coordination of MMCs With Hybrid DC Circuit Breakers for HVDC Grid Protection," *IEEE Trans. Power Del.*, vol. 34, no. 1, pp. 11-22, Feb. 2019.

[5] R. Li, L. Xu and L. Yao, "DC Fault Detection and Location in Meshed Multiterminal HVDC Systems Based on DC Reactor Voltage Change Rate," *IEEE Trans. Power Del.*, vol. 32, no. 3, pp. 1516-1526, June 2017.

[6] A. Jamshidi Far and D. Jovcic, "Design, Modeling and Control of Hybrid DC Circuit Breaker Based on Fast Thyristors," *IEEE Trans. Power Del.*, vol. 33, no. 2, pp. 919-927, April 2018.

[7] B. Li, F. Jing, B. Li and W. Wen, "Research on the Parameter Matching Between Active SI-SFCL and DC Circuit Breaker in DC systems," *IEEE Trans. Appl. Supercond.*, vol. 29, no. 2, pp. 1-5, March 2019.

[8] W. Wen, Y. Huang, B. Li, Y. Wang and T. Cheng, "Technical Assessment of Hybrid DCCB With Improved Current Commutation Drive Circuit," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 5456-5464, Sept.-Oct. 2018.

[9] W. Sima et al., "A Novel Active Mechanical HVDC Breaker With Consecutive Interruption Capability for Fault Clearances in MMC-HVDC Systems," *IEEE Trans. Ind. Electron.*, vol. 66, no. 9, pp. 6979-6989, Sept. 2019.

[10] Magnus Callavik, Anders Blomberg, et al. "The hybrid HVDC breaker: An innovation breakthrough enabling reliable HVDC grid, " *ABB Grid Systems, Technical paper*, Nov, 2012.

[11] R. Majumder, S. Auddy, B. Berggren, G. Velotto, P. Barupati and T. U. Jonsson, "An Alternative Method to Build DC Switchyard With Hybrid DC Breaker for DC Grid," *IEEE Trans. Power Del.*, vol. 32, no. 2, pp. 713-722, April 2017.

[12] C. Li, J. Liang and S. Wang, "Interlink Hybrid DC Circuit Breaker," in IEEE Transactions on Industrial Electronics, vol. 65, no. 11, pp. 8677-8686, Nov. 2018.

[13] H. Xiao, Z. Xu, L. Xiao, C. Gan, F. Xu and L. Dai, "Components Sharing Based Integrated HVDC Circuit Breaker for Meshed HVDC Grids," in IEEE Transactions on Power Delivery, early access.

[14] E. Kontos, T. Schultz, L. Mackay, L. Ramirez-Elizondo, C. Franck, and P. Bauer, "Multi-line breaker for HVDC applications," *IEEE Trans. Power Del.*, vol. 8977, no. c, pp. 1–8, 2017.

[15] A. Mokhberdoran, D. V. Hertem, N, Silva, H. Leite, and A. Carvalho, "Multiport hybrid HVDC circuit breaker", *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 309–320, Jan. 2018.

[16] Fereidouni A R，Vahidi B，Mehr T H．"The impact of solid state fault current limiter on power network with wind-turbine power generation", *IEEE Smart Grid*，4(2)：1188-1196，2013.

[17] Keshavarzi D，Farjah E，Ghanbari T, "Hybrid DC circuit breaker and fault current limiter with optional interruption capability", *IEEE Trans. Power Electron*，33(3)：2330-2338， 2018.

[18] J. Xu, X. Zhao, N. Han, J. Liang and C. Zhao, "A Thyristor-Based DC Fault Current Limiter With Inductor Inserting–Bypassing Capability" *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 7, no. 3, pp. 1748-1757, Sept. 2019.

[19] J. Xu, S. Zhu, C. Li and C. Zhao, "Dc fault current calculation method in MMC-HVDC grid considering current-limiting devices", The Journal of Engineering, vol. 2019, no. 16, pp. 3188-3195, 3 2019.

[20] J. Hafner and B. Jacobson, "Proactive Hybrid HVDC Breakers - A key innovation for reliable HVDC grids," *Cigré International Symposium*, 2011.

[21] A. Jehle, K. Pally, and J. Biela, "Comparison of Energy Dissipation Concepts for DC Circuit Breakers," *20th European Conference on Power Electronics and Applications*, 2018

[22] Magnusson J， Saers R，Liljestrand L，et al. "Separation of the energy absorption and overvoltage protection in solid-state breakers by the use of parallel varistors," *IEEE Trans. Power Electron.*，29(6)：2715-2722，2014.

[23] Y. Hu, J. Chen, C. Zou *et al.*, "Experimental Investigation on Communication Link Delay of Valve Control System of Ultra high-voltage VSC-HVDC," Journal of Global Energy Interconnection, 3(2): 190-198, 2020.

[24] W. Liu, F. Liu, Y. Zhuang, X. Zha, C. Chen and T. Yu, "A Multiport Circuit Breaker-Based Multiterminal DC System Fault Protection," *IEEE J. Emerg. Sel. Topics Power Electron*, vol. 7, no. 1, pp. 118-128, March 2019.

[25] ABB Semiconductor, Lenzburg, Switzerland. 5STB18U6500 data sheet. (Jul. 2015). [Online]. *Available: http://www.abb.com.*

Jianzhong Xu (M'14-SM'19) was born in Shanxi, China. He received the B.S. and Ph.D. degrees from North China Electric Power University (NCEPU) in 2009 and 2014 respectively. Currently, he is an Associate Professor and Ph.D. Supervisor of the State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University, China, where he obtained his Ph.D. degree in 2014. From 2012 to 2013 and 2016 to 2017, he was a visiting Ph.D. student and Post-Doctoral Fellow at the University of Manitoba, Canada. He is an Associate Editor of the CSEE Journal of Power and Energy Systems. He is now working on the Electromagnetic Transient (EMT) equivalent modelling, fault analysis and protection of HVDC Grids.

Bingqian Song was born in Jiangsu, China. She received the B.S. and M.S. degrees in power system and its automation from North China Electric Power University (NCEPU) in 2017 and 2020, respectively. Currently, she is working in the State Grid Nanjing Power Supply Company, Nanjing, China. Her research interests include HVdc grid operation and protection.

Yu Lü was born in Zhejiang, China. She received the B.S. degree in power system and its automation from North China Electric Power University in 2018, where she is currently working toward her master degree. Her research interests include HVdc grid operation and protection.

Chengyong Zhao (M'05-SM'15) was born in Zhejiang, China. He received the B.S., M.S. and Ph.D. degrees in power system and its automation from NCEPU in 1988, 1993 and 2001, respectively. He was a visiting professor at the University of Manitoba from Jan. 2013 to Apr. 2013 and Sep. 2016 to Oct. 2016. Currently, he is a professor at the School of Electrical and Electronic Engineering, NCEPU. His research interests include HVDC system and DC grid.

Gen Li (M'18) received the B.Eng. degree in Electrical Engineering and its Automation from Northeast Electric Power University, Jilin, China, in 2011, the M.Sc. degree in Power Engineering from Nanyang Technological University, Singapore, in 2013 and the Ph.D. degree in Electrical Engineering from Cardiff University, Cardiff, U.K., in 2018.

From 2013 to 2016, he was a Marie Curie Early Stage Research Fellow funded by the European Union's MEDOW project. He has been a Visiting Researcher at China Electric Power Research Institute and Global Energy Interconnection Research Institute, Beijing, China, at Elia, Brussels, Belgium and at Toshiba International (Europe), London, U.K. He has been a Research Associate at the School of Engineering, Cardiff University since 2017. His research interests include control and protection of HVDC and MVDC technologies, power electronics, reliability modelling and evaluation of power electronics systems.

Dr. Li is a Chartered Engineer in the U.K. He is an Associate Editor of the CSEE Journal of Power and Energy Systems. He is an Editorial board member of CIGRE ELECTRA. His Ph.D. thesis received the First CIGRE Thesis Award in 2018.

Jun Liang (M'02-SM'12) received the B.Sc. degree in Electric Power System & its Automation from Huazhong University of Science and Technology, Wuhan, China, in 1992 and the M.Sc. and Ph.D. degrees in Electric Power System & its Automation from the China Electric Power Research Institute (CEPRI), Beijing, in 1995 and 1998, respectively.

From 1998 to 2001, he was a Senior Engineer with CEPRI. From 2001 to 2005, he was a Research Associate with Imperial College London, U.K. From 2005 to 2007, he was with the University of Glamorgan as a Senior Lecturer. He is currently a Professor in Power Electronics with the School of Engineering, Cardiff University, Cardiff, U.K. He is the Coordinator and Scientist-in-Charge of two European Commission Marie-Curie Action ITN/ETN projects: MEDOW (€3.9M) and InnoDC (€3.9M). His research interests include HVDC, MVDC, FACTS, power system stability control, power electronics, and renewable power generation.

Prof. Liang is a Fellow of the Institution of Engineering and Technology (IET). He is the Chair of IEEE UK and Ireland Power Electronics Chapter. He is an Editorial Board Member of CSEE JPES. He is an Editor of the IEEE Transactions on Sustainable Energy.