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ORIGINAL ARTICLE

Flexible cascaded multilevel inverter with multiple operation modes

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Abstract
In this paper, a flexible cascaded multilevel inverter is proposed with a wide operational range. The inverter can change its topology structure to operate in three modes by a bidirectional switch unit. The nine-level or five-level mode of the inverter is adopted to optimize the output waveform when the input power is low. To decrease power losses, the three-level mode of the inverter is adopted to reduce the number of active switch devices when the input power is high. The topology and modulation strategy of the proposed inverter are presented and analyzed. The total losses and current THD of the inverter are calculated. In addition, simulations and experiments are conducted. The obtained simulation and experimental results indicate the correctness and feasibility of the proposed inverter and its modulation strategy.

Keywords Photovoltaic generation · Multilevel inverter · Multiple modes · Modulation strategy

1 Introduction

Nowadays, photovoltaic systems are becoming more popular due to their advantages in terms of unlimited reservation, pollution-free and convenient utilization [1]. As a core piece of equipment for photovoltaic systems, inverters play an important role in reducing output harmonics and improving system efficiency [2]. Compared with traditional two-level inverters, multilevel inverters are more suitable for PV systems due to their unique characteristics [3–5]. Multilevel inverters come with the benefits of reduced du/dt, reduced device voltage stress, improved output waveform quality and smaller filter inductance [6–8]. These benefits make it easier to meet the demands in photovoltaic applications.

There are a few classics multilevel inverter topologies. These classes are the neutral point clamped topology (NPC) [9–11], the flying capacitor topology (FC) [12, 13], and the cascaded H-bridge topology (CHB) [14–16]. NPC inverters are widely used in photovoltaic systems due to their characteristics of low switch losses, and freedom from common-mode leakage current. However, all of the NPC inverters need to solve the problem of capacitor voltage balance on dc side. CHB inverters can heighten the voltage rank by series connections. However, CHB converters require multiple sets of isolated dc sources, which is a main drawback of this topology.

Topologies with the multilevel structure have good output characteristics due to their ability to produce staircase-like voltage waveforms. However, multilevel inverters exhibit an important limitation. For an increased number of output levels, they require many power switches, which increases the cost, control complexity and the losses of devices [17]. In photovoltaic applications, the output power of PV cells spans a wide range and varies greatly [18–21]. Due to the wide input range of inverters, the power levels of the power devices and filter inductor are selected from the maximum output power. This leads to high device cost, high losses and low system utilization.

There is a contradiction between achieving a wide operational range and reducing power losses [22, 23]. For the past few years, efforts have been directed to reduce the cost and losses in multilevel inverters, and many topologies have appeared. In [24] and [25], a T-type inverter with a significant reduction in the number of power devices was described. In addition, this topology can be applied to any number of voltage levels within the switch maximum voltage. The losses are decreased since higher voltage rated

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switches operate at the fundamental frequency in this topology. In [26], a multilevel inverter using the series/parallel conversion of dc voltage sources was proposed. When the capacitors are connected in series, the voltage of devices is reduced, as well as the total losses of the devices. In [27], a flying capacitor clamped inverter based on a switched-capacitor was proposed. Its modulation strategy reduced the losses of the switch devices by curtailing the switch frequency of certain switches. In [28], an H-bridge inverter with dc side switches was proposed and applied to a PV system. In this topology, the bridge arm switches operate at a low frequency, which reduces the switch losses. The above inverter topologies reduced losses by optimizing the topology structure. However, all of the switches are always under operating state, and the total losses are still large.

Considering the actual conditions in a PV system, the operational range of an inverter should be wide. Different output characteristics of an inverter are needed under different conditions. This paper proposes a cascaded multilevel inverter. Based on a wide operational range, the inverter can provide different output characteristics to adapt to different conditions. Using a bidirectional switch unit, the proposed inverter can change its topology structure to operate in three modes: nine-level mode, five-level mode and three-level mode. When the dc input power is low, the nine-level or five-level mode can provide more output levels to improve the quality of the output waveform. When the dc input power is high, the three-level mode can reduce the number of active switch devices to decrease the inverter losses.

This paper is organized as follows. Section 2 introduces the topology of a cascaded multi-mode inverter, and modulation methods of the three modes are described in detail. In addition, the capacitor voltage balance on the dc side is analyzed. Section 3 analyzes and calculates the losses and the current total harmonic distortion of the inverter during the three modes. Section 4 offers simulation and experimental results. Section 5 provides some conclusions for this paper.

2 Cascaded multimode inverter and its modulation strategy

2.1 Topology structure

The topology of the proposed cascaded multilevel inverter is presented in Fig. 1a. It consists of twelve switches S_1–S_{12}, and a bidirectional switch unit S_0. In addition, it also contains four clamping diodes D_1–D_4, four clamping capacitors C_1–C_4, and two dc voltage sources. By the bidirectional switch unit, the proposed inverter can change its topology structure to operate in three operation modes. According to different working conditions, different operation modes can be applied.

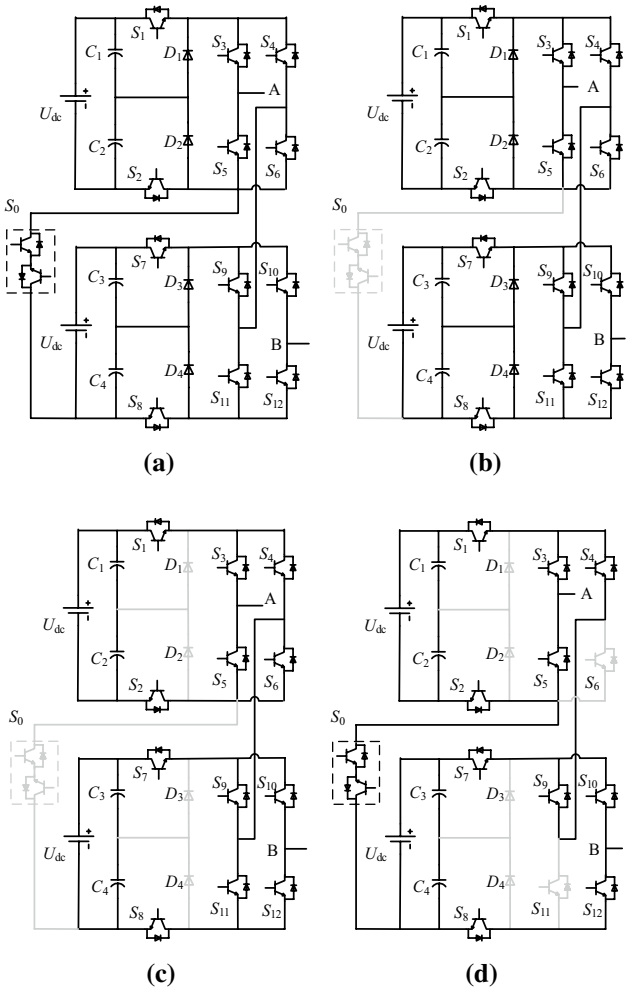

Fig. 1 Diagrams showing: **a** topology of the proposed inverter; **b** nine-level mode; **c** five-level mode; **d** three-level mode

The three working modes are presented as follows. (1) Keep the bidirectional switch S_0 off, and the topology is a cascaded nine-level inverter. This mode is called the nine-level mode, as shown in Fig. 1b. (2) Keep the bidirectional switch S_0 off, keep the switches S_1, S_2, S_7 and S_8 on, and the topology is a cascaded five-level H-bridge inverter. This mode is called the five-level mode, as shown in Fig. 1(c). (3) Keep the bidirectional switch S_0 as well as the switches S_1, S_2, S_4, S_7, S_8 and S_9 on. Meanwhile, keep switches S_6 and S_{11} off. The topology becomes one H-bridge inverter composed of the switches S_3, S_5, S_{10} and S_{12}. With the switches S_1, S_2, S_4, S_7 and S$_9$ and the bidirectional switch S_0 kept on, two dc sources are connected in parallel. This mode is called the three-level mode, as shown in Fig. 1d.

2.2 Modulation strategy

When the proposed inverter operates in the nine-level mode, the switches connected to the dc side (S_1, S_2, S_7, S_8) are

controlled to output required waveforms, and the bridge arm switches (S_3–S_6, S_9–S_{12}) are controlled to change the polarity of output waveforms. Therefore, the dc side switches act at a high frequency while the bridge arm switches act at a low frequency. Taking the upper half of the topology as an example, the voltage of each capacitor is $0.5U_{dc}$. When S_1 and S_2 are switched on, the clamping capacitors C_1 and C_2 are in the discharge state, and the output voltage is U_{dc}. When S_1 is on and S_2 is off, or when S_1 is off and S_2 is on, only one capacitor discharges. Thus, the output voltage is $0.5U_{dc}$. When both S_1 and S_2 are switched off, none of the capacitors discharge. Thus, the output voltage is 0.

The modulation strategy of the nine-level mode of the proposed inverter is shown in Fig. 2. It requires eight carriers (Tri_1–Tri_8) and one reference signal (T_{ref}) to generate original waveforms. The amplitude of each carrier is 1, the frequency is the same, and the phase difference between adjacent carriers is 90°. Depending on modulation ratio M_1, the amplitude of the reference signal T_{ref} changes between 0 and 1. Eight sets of rectangular pulse signals are obtained by comparing the carriers and the reference signal, to control the dc side switches. In addition, the switches (S_3–S_6, S_9–S_{12}) are controlled by the reference signal polarity.

Moreover, the capacitors (C_1–C_4) clamp the dc voltage when the proposed inverter operates in the nine-level mode. The inverter can output a nine-level voltage when all the capacitor voltage is $U_{dc}/2$. Thus, it is of great importance to keep the voltage balance of the capacitors. When the inverter outputs a voltage of $\pm U_{dc}/2$, $\pm U_{dc}$, $\pm 3U_{dc}/2$, only parts of the capacitors discharge. As a result, the capacitor voltage balance was broke. The key to achieving voltage balance is to make all of capacitors output the same energy in one cycle.

Figure 3 shows the discharge states of four capacitors, and the colored squares mean the discharge time of each capacitor. Since the carrier frequency is much higher than the modulation frequency, the reference signal in Fig. 3 can be seen as a horizontal line. The amplitude of the carriers is 1. When the reference signal is in the interval of [0, 0.25], the inverter outputs a voltage of 0 or $U_{dc}/2$. As a result, there are 0 or 1 capacitor discharges at the same time, as shown in Fig. 3a. Similarly, when the reference signal is in the interval of [0.25, 0.5], there are 1 or 2 capacitors discharged at the same time, as shown in Fig. 3b. When the reference signal is in the interval of [0.5, 0.75], there are 2 or 3 capacitors discharged at the same time, as shown in Fig. 3c. In addition, when the reference signal is in the interval of [0.75, 1], there are 3 or 4 capacitors discharged at the same time, as shown in Fig. 3d. Therefore, whatever the value of the reference signal, four capacitors can take turns discharging, and the discharge times of all the capacitors are equal. As a result,

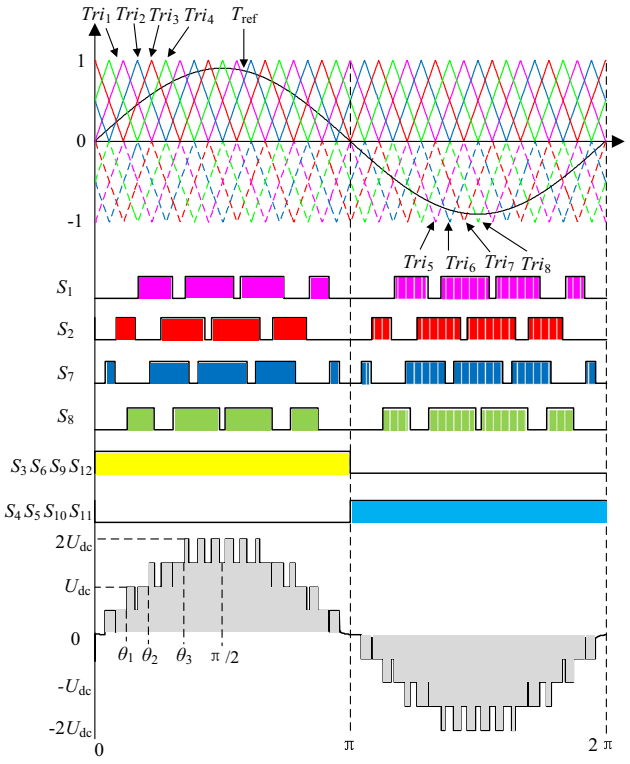

Fig. 2 Modulation strategy for the nine-level mode

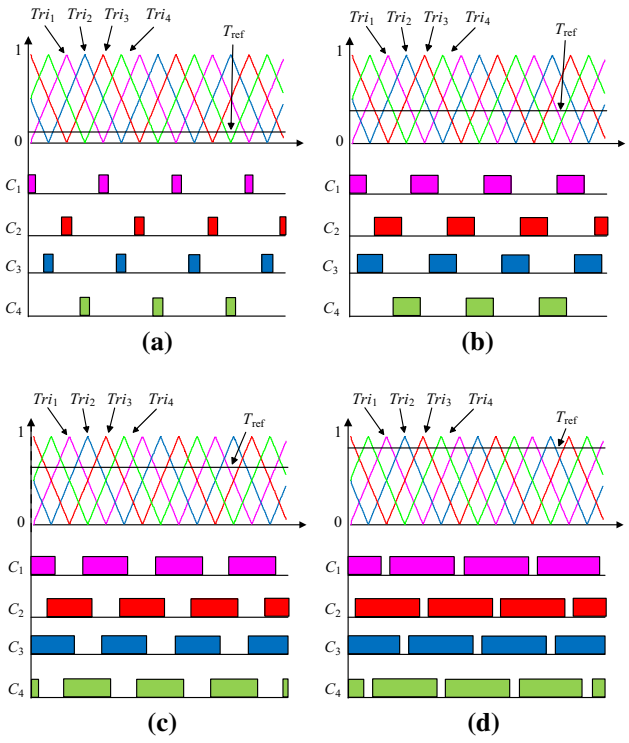

Fig. 3 Capacitor states under different reference signal amplitudes: **a** $T_{ref} \in [0, 0.25]$; **b** $T_{ref} \in [0.25, 0.5]$; **c** $T_{ref} \in [0.5, 0.75]$; **d** $T_{ref} \in [0.75, 1]$

each of the capacitors output the same energy, and voltage balance of capacitors is achieved under the carrier frequency. The number of voltage level changes when the modulation ratio M_1 changes, and the capacitor voltages are always balanced. Compared with voltage balance strategies under the modulation frequency, the voltage balance strategy proposed in this paper has a smaller voltage ripple and a more stabilized voltage value. Thus, the quality of the output waveform is better.

When the proposed inverter operates in the five-level mode, the dc side switches (S_1, S_2, S_7, S_8) are kept on, and the bidirectional switch S_0 is kept off. Then the topology of the proposed inverter changes into a cascaded H-bridge inverter.

The modulation strategy of the five-level mode of the proposed inverter is shown in Fig. 4a. Four carriers (Tri_1, Tri_3, Tri_5, Tri_7) and one reference signal (T_{ref}) are required to generate original waveforms. The phase difference between adjacent carriers is 180°. Four sets of rectangular pulse signals are obtained by comparing the carriers and the reference signal, to control the bridge arm switches (S_3–S_6, S_9–S_{12}).

When the proposed inverter operates in the three-level mode, only four bridge arm switches (S_3, S_5, S_{10}, S_{12},) participate in the modulation process. In addition, the topology changes into a three-level H-bridge inverter.

The modulation strategy of the three-level mode of the proposed inverter is shown in Fig. 4b. Two carriers (Tri_1, Tri_5,) and one reference signal (T_{ref}) are required to generate original waveforms. Two sets of rectangular pulse signals are obtained by comparing the carriers and the reference signal, to control bridge arm switches (S_3, S_5, S_{10}, S_{12}).

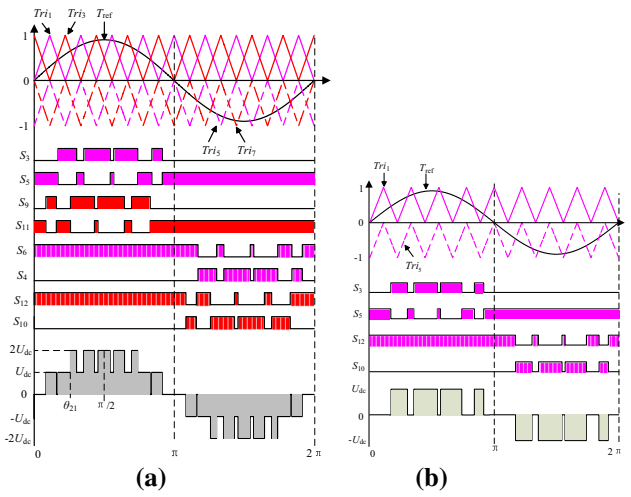

Fig. 4 Modulation strategy for: **a** five-level mode; **b** three-level mode

3 Calculations and analysis of losses and current THD

As can be seen from the analysis in Sect. 2, the quality of output waveforms and the losses are quite different when the proposed inverter operates in different modes. In this section, the total losses and current THD of the proposed inverter are calculated and compared under the three modes.

3.1 Calculations of losses

The inverter losses mainly include the conduction losses, the switching losses and the losses of the filter inductor. Since a multilevel inverter has an advantage in terms of reducing the filter inductor, the losses of the inductor are ignored in this paper.

The conduction losses of the proposed inverter are derived first. The conduction losses of one MOSFET device can be approximately calculated as:

$$\begin{aligned} P_{\mathrm{con\_M}} &= (U_{\mathrm{M}} + R_{\mathrm{M}} I)I \\ &= U_{\mathrm{M}} I_{\mathrm{m}} \sin \omega t + R_{\mathrm{M}} I_{\mathrm{m}}^2 \sin^2 \omega t \end{aligned} \tag{1}$$

where U_{M} is the conduction voltage drop of the MOSFET (V); R_{M} is conduction resistance (Ω); and I is the current (A), which can be expressed as: $I = I_{\mathrm{m}} \sin \omega t$.

Similarly, the conduction losses of one diode can be approximately calculated as:

$$\begin{aligned} P_{\mathrm{con\_D}} &= (U_{\mathrm{D}} + R_{\mathrm{D}} I)I \\ &= U_{\mathrm{D}} I_{\mathrm{m}} \sin \omega t + R_{\mathrm{D}} I_{\mathrm{m}}^2 \sin^2 \omega t \end{aligned} \tag{2}$$

where U_{D} is conduction voltage drop of the diode (V); and R_{D} is the conduction resistance of the diode (Ω).

The losses of the proposed inverter under the nine-level mode are analyzed first. The number of output levels changes as the modulation radio M_1 varies from 0 to 1. When $M_1 \in [0.75, 1]$, the inverter can output a nine-level voltage wave. Since the output waveforms of the inverter have periodic symmetry, the output characteristic can be analyzed in the interval of $[0, \pi/2]$. Depending on the voltage of a waveform, three angles are defined to differentiate the output voltage intervals. In a modulation cycle, when the voltage level reaches $U_{\mathrm{dc}}/2$ for the first time, the corresponding angle is defined as θ_1. The definitions of θ_2 and θ_3 are similar to that of θ_1. The three angles are defined as:

$$\theta_1 = \arcsin \frac{1}{4M_1}, \theta_2 = \arcsin \frac{1}{2M_1}, \theta_3 = \arcsin \frac{3}{4M_1} \tag{3}$$

In the above four intervals, the duty cycles of the switches are different. The duty cycles D_{11}–D_{14} in the four intervals are expressed as:

$$\begin{aligned} D_{11} &= 4M_1 \sin\omega t \quad \omega t \in [0, \theta_1] \\ D_{12} &= 4M_1 \sin\omega t - 1 \quad \omega t \in [\theta_1, \theta_2] \\ D_{13} &= 4M_1 \sin\omega t - 2 \quad \omega t \in [\theta_2, \theta_3] \\ D_{14} &= 4M_1 \sin\omega t - 3 \quad \omega t \in [\theta_3, \pi/2] \end{aligned} \tag{4}$$

Moreover, in the four intervals above, the conduction losses are different when the inverter output voltage changes. To calculate the conduction losses, the number of conductive switch devices with different output voltages is analyzed, as shown in Table 1.

According to (1), (2), (4) and Table 1, the conduction losses of a MOSFET in the nine-level mode ($P_{\text{con\_M9}}$) and the conduction losses of a clamp diode in the nine-level mode ($P_{\text{con\_D9}}$) can be obtained as:

$$\begin{aligned} P_{\text{con\_M9}} &= \frac{2}{\pi}\left\{\begin{array}{l} \int_0^{\theta_1} [4P_{\text{con\_M}}(1-D_{11}) + 5P_{\text{con\_M}}D_{11}]\mathrm{d}\omega t \\ + \int_{\theta_1}^{\theta_2} [5P_{\text{con\_M}}(1-D_{12}) + 6P_{\text{con\_M}}D_{12}]\mathrm{d}\omega t \\ + \int_{\theta_2}^{\theta_3} [6P_{\text{con\_M}}(1-D_{13}) + 7P_{\text{con\_M}}D_{13}]\mathrm{d}\omega t \\ + \int_{\theta_3}^{\frac{\pi}{2}} [7P_{\text{con\_M}}(1-D_{14}) + 8P_{\text{con\_M}}D_{14}]\mathrm{d}\omega t \end{array}\right\} \\ &= \left(\frac{8}{\pi} + 2M_1\right)U_{\text{M}}I_m + \left(2 + \frac{16M_1}{3\pi}\right)R_{\text{M}}I_m^2 \end{aligned} \tag{5}$$

$$\begin{aligned} P_{\text{con\_D9}} &= \frac{2}{\pi}\left\{\begin{array}{l} \int_0^{\theta_1} [4P_{\text{con\_D}}(1-D_{11}) + 3P_{\text{con\_D}}D_{11}]\mathrm{d}\omega t \\ + \int_{\theta_1}^{\theta_2} [3P_{\text{con\_D}}(1-D_{12}) + 2P_{\text{con\_D}}D_{12}]\mathrm{d}\omega t \\ + \int_{\theta_2}^{\theta_3} [2P_{\text{con\_D}}(1-D_{13}) + P_{\text{con\_D}}D_{13}]\mathrm{d}\omega t \\ + \int_{\theta_3}^{\frac{\pi}{2}} [P_{\text{con\_D}}(1-D_{14})]\mathrm{d}\omega t \end{array}\right\} \\ &= \left(\frac{8}{\pi} - 2M_1\right)U_{\text{D}}I_{\text{m}} + \left(2 - \frac{16M_1}{3\pi}\right)R_{\text{D}}I_{\text{m}}^2 \end{aligned} \tag{6}$$

Then the switching losses in the nine-level mode are calculated. The switching losses are caused by the non-ideal state of the switch device. It takes time for the switch device to go from fully on to fully off, and this process produces losses. The switching loss of one MOSFET in a single switch motion can be calculated as:

$$E_{\text{s}} = \frac{1}{2}V_{\text{D}}I_{\text{D}} \times (t_{\text{S(on)}} + t_{\text{S(off)}}) \tag{7}$$

where E_{s} is the energy of the switching loss of one switch motion (J); V_{D} is the voltage stress of the switch (V); I_{D} is the conduction current of the switch (A); and $t_{\text{S(on)}}$ and $t_{\text{S(off)}}$ are the on delay time and the off delay time of the switch (s).

When the proposed inverter operates in the nine-level mode, there are 12 switches participate in modulation. S_1, S_2, S_7, S_8 operate at the carrier frequency in one cycle. The bridge arm switches act only one time in one cycle, and can be ignored. The total switching losses can be obtained by summing the losses of all the switches.

$$\begin{aligned} P_{\text{sw\_9}} &= \frac{1}{T}\sum_{s=1}^{12} E_{\text{s}}f_{\text{s}} \\ &= \frac{2}{T}f_{\text{c}}I_{\text{out}}U_{\text{dc}} \times (t_{\text{S(on)}} + t_{\text{S(off)}}) \end{aligned} \tag{8}$$

where, $P_{\text{sw\_9}}$ is power of the switching losses (W); T is the modulation period (s); f_{s} is the motion frequency of one switch (Hz); and f_{c} is the carrier frequency (Hz).

To sum up (5), (6), (8), the total losses of the inverter in the 9-level mode is:

$$P_9 = P_{\text{con\_M9}} + P_{\text{con\_D9}} + P_{\text{sw\_9}} \tag{9}$$

Similarly, the losses of the proposed inverter under the five-level mode is calculated. The conduction losses of the MOSFET ($P_{\text{con\_M5}}$) and the conduction losses of the antiparallel diode ($P_{\text{con\_D5}}$) can be expressed as:

$$\begin{aligned} P_{\text{con\_M5}} &= \frac{2}{\pi}\left\{\begin{array}{l} \int_0^{\theta_1} [2P_{\text{con\_M}}(1-D_{21}) + 5P_{\text{con\_M}}D_{21}]\mathrm{d}\omega t \\ + \int_{\theta_1}^{\frac{\pi}{2}} [5P_{\text{con\_M}}(1-D_{22}) + 8P_{\text{con\_M}}D_{22}]\mathrm{d}\omega t \end{array}\right\} \\ &= \left(\frac{4}{\pi} + 3M_2\right)U_M I_{\text{m}} + \left(1 + \frac{24M_2}{3\pi}\right)R_M I_{\text{m}}^2 \end{aligned} \tag{10}$$

$$\begin{aligned} P_{\text{con\_D5}} &= \frac{\pi}{2}\left\{\begin{array}{l} \int_0^{\theta_1} [2P_{\text{con\_D}}(1-D_{21}) + P_{\text{con\_D}}D_{21}]\mathrm{d}\omega t \\ + \int_{\theta_1}^{\frac{\pi}{2}} P_{\text{con\_D}}(1-D_{22})\mathrm{d}\omega t \end{array}\right\} \\ &= \left(\frac{4}{\pi} - M_2\right)U_D I_{\text{m}} + \left(1 - \frac{8M_2}{3\pi}\right)R_{\text{D}}I_{\text{m}}^2 \end{aligned} \tag{11}$$

The total switching losses in the five-level mode can be expressed as:

Table 1 Number of conductive switches of the nine-level mode

Output voltage level	Number of conductive MOSFET	Number of conductive clamp diode
$2U_{\text{dc}}$	8	0
$3U_{\text{dc}}/2$	7	1
U_{dc}	6	2
$U_{\text{dc}}/2$	5	3
0	4	4

$$P_{\text{sw\_5}} = \frac{1}{T}\left(\sum_{s=3}^{6} E_s f_s + \sum_{s=9}^{12} E_s f_s\right) = \frac{2}{T} f_c I_{\text{out}} U_{\text{dc}} \times (t_{\text{S(on)}} + t_{\text{S(off)}}) \tag{12}$$

To sum up (10), (11), (12), the total losses of the inverter in the five-level mode is:

$$P_5 = P_{\text{con\_M5}} + P_{\text{con\_D5}} + P_{\text{sw\_5}} \tag{13}$$

The losses of the proposed inverter under the three-level mode are calculated as follows. The conduction losses of the MOSFET ($P_{\text{con\_M3}}$) and the conduction losses of the antiparallel diode ($P_{\text{con\_D3}}$) can be expressed as:

$$P_{\text{con\_M3}} = \frac{2}{\pi}\int_0^{\frac{\pi}{2}} [2P_{\text{con\_M}}(1 - D_{31}) + 5P_{\text{con\_M}} D_{31}]\mathrm{d}\omega t = \left(\frac{4}{\pi} + \frac{3M_3}{2}\right) U_M I_m + \left(1 + \frac{4M_3}{\pi}\right) R_M I_m^2 \tag{14}$$

$$P_{con\_D3} = \frac{\pi}{2}\int_0^{\frac{\pi}{2}} [2P_{con\_D}(1 - D_{31}) + P_{con\_D} D_{31}]\mathrm{d}\omega t = \left(\frac{4}{\pi} - \frac{M_3}{2}\right) U_D I_m + \left(1 - \frac{4M_3}{3\pi}\right) R_D I_m^2 \tag{15}$$

The total switching losses under the three-level mode can be expressed as:

$$P_{\text{sw\_3}} = \frac{1}{T}\left(E_{s3} f_{s3} + E_{s5} f_{s5} + E_{s10} f_{s10} + E_{s12} f_{s12}\right) = \frac{1}{T} f_c I_{\text{out}} U_{\text{dc}} \times (t_{\text{S(on)}} + t_{\text{S(off)}}) \tag{16}$$

To sum up (14), (15), (16), the total losses of the inverter in the three-level mode is:

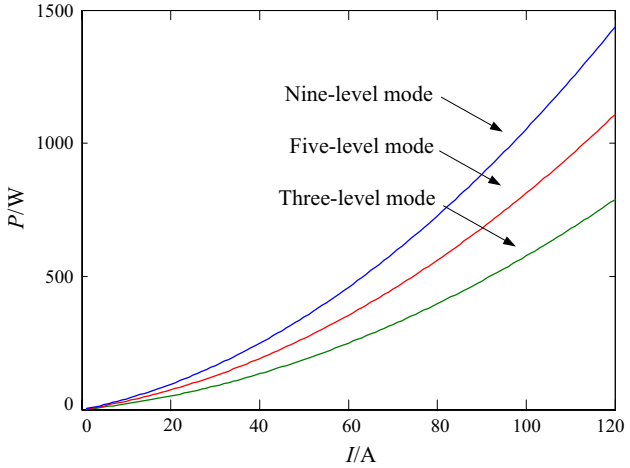

Fig. 5 Total losses of the three modes

Table 2 Parameters used in the calculations

Parameters	Value	Parameters	Value
L	0.3 mH	ω	314 rad/s
T	0.02 s	f_c	1 kHz
U_I	2.09 V	R_I	0.16 Ω
U_f	2.1 V	R_D	0.025 Ω
I_c	10.7 A	V_{cc}	650 V
$t_{s(\text{on})}$	10 ns	$t_{s(\text{off})}$	67 ns

$$P_3 = P_{\text{con\_M3}} + P_{\text{con\_D3}} + P_{\text{sw\_3}} \tag{17}$$

To analyze and compare the losses under different modes, specific data was substituted into the equations and a function diagram was obtained, as shown in Fig. 5. To simplify the calculations, the parameters of the antiparallel diode and the clamping diode are the same. The parameters used in the calculation are shown in Table 2.

As can be seen from Fig. 5, the total losses increase with an increase of the current. When the current is the same, the losses of the nine-level mode are the largest, and the losses of the three-level mode are the lowest. The larger the current is, the more obvious the difference is. An increase of the level number leads to an increase of the losses.

3.2 Calculations of current THD

Total harmonic distortion (THD) plays an important role in the detection and evaluation of a power system. It is an important index to evaluate the characteristics of an inverter. It is not easy to calculate the current THD by its definition. However, the output current of an inverter can be seen as a combination of the current fundamental wave and the current ripple. Therefore, the current ripple can be approximately regarded as the sum of harmonic currents. Thus, the current THD is approximately expressed by the ratio of the current ripple to the fundamental wave as:

$$\text{THD} \approx \frac{\Delta I_{\text{RMS}}}{I_1} = \frac{\sqrt{2}\Delta I_{\text{m}}}{2\sqrt{3} I_{\text{M}}} \tag{18}$$

where ΔI_{RMS} is the RMS value of the current ripple (A); ΔI_{m} is the peak–peak value of the current ripple wave (A); and I_{M} is the peak value of the output current fundamental wave (A).

When the proposed inverter operates in the nine-level mode, the current ripple in different intervals is calculated first. Following the rules in Sect. 2.1, interval [0, π/2] is divided into four parts. Thus, the peak–peak values of the current ripple in the four intervals are:

$$\begin{cases} \Delta I_{\mathrm{m91}} = \frac{1}{4Lf_{\mathrm{c}}}\left(\frac{U_{\mathrm{dc}}}{2} - U_{\mathrm{out}}\right)(4M_1 \sin \omega t) \\ \Delta I_{\mathrm{m92}} = \frac{1}{4Lf_{\mathrm{c}}}(U_{\mathrm{dc}} - U_{\mathrm{out}})(4M_1 \sin \omega t - 1) \\ \Delta I_{\mathrm{m93}} = \frac{1}{4Lf_{\mathrm{c}}}\left(\frac{3U_{\mathrm{dc}}}{2} - U_{\mathrm{out}}\right)(4M_1 \sin \omega t - 2) \\ \Delta I_{\mathrm{m94}} = \frac{1}{4Lf_{\mathrm{c}}}(2U_{\mathrm{dc}} - U_{\mathrm{out}})(4M_1 \sin \omega t - 3) \end{cases} \tag{19}$$

RMS values of the current ripple are obtained by integrating the peak–peak values of the current ripple in the four intervals. Thus, the RMS values of the current ripple in the nine-level mode are expressed as:

$$\Delta I_{\mathrm{RMS9}} = \frac{1}{2\sqrt{3}}\sqrt{\frac{2}{\pi}\left(\begin{array}{l}\int_0^{\theta_1} \Delta I_{\mathrm{m91}}^2 \mathrm{d}\omega t + \int_{\theta_1}^{\theta_2} \Delta I_{\mathrm{m92}}^2 \mathrm{d}\omega t \\ + \int_{\theta_2}^{\theta_3} \Delta I_{\mathrm{m93}}^2 \mathrm{d}\omega t + \int_{\theta_3}^{\pi/2} \Delta I_{\mathrm{m94}}^2 \mathrm{d}\omega t\end{array}\right)} \tag{20}$$

Hence, the current THD of the proposed inverter in the nine-level mode is obtained as:

$$\mathrm{THD}_9 = \frac{\sqrt{2}\Delta I_{\mathrm{RMS9}}}{I_{\mathrm{M}}}, \quad M_1 \in [0.75, 1] \tag{21}$$

Similarly, when the inverter operates in the five-level mode, the interval [0, π/2] is divided into two parts. In addition, the peak–peak value of the current ripple in the two intervals are:

$$\begin{cases} \Delta I_{\mathrm{m51}} = \frac{1}{4Lf_{\mathrm{c}}}(U_{\mathrm{dc}} - U_{\mathrm{out}})(2M_2 \sin \omega t) \\ \Delta I_{\mathrm{m52}} = \frac{1}{4Lf_{\mathrm{c}}}(2U_{\mathrm{dc}} - U_{\mathrm{out}})(2M_2 \sin \omega t - 1) \end{cases} \tag{22}$$

The RMS value of the current ripple in the five-level mode can be obtained as:

$$\Delta I_{\mathrm{RMS5}} = \frac{1}{2\sqrt{3}}\sqrt{\frac{2}{\pi}\left(\int_0^{\theta_{21}} \Delta I_{\mathrm{m51}}^2 \mathrm{d}\omega t + \int_{\theta_{21}}^{\pi/2} \Delta I_{\mathrm{m52}}^2 \mathrm{d}\omega t\right)} \tag{23}$$

Thus, the current THD of the proposed inverter in the five-level mode is expressed as:

$$\mathrm{THD}_5 = \frac{\sqrt{2}\Delta I_{\mathrm{RMS5}}}{I_{\mathrm{M}}}, \quad M_2 \in [0.5, 1] \tag{24}$$

In a similar way, when the inverter operates in the three-level mode, the peak–peak value of the current ripple in the interval [0, π/2] is:

$$\Delta I_{\mathrm{m31}} = \frac{1}{2Lf_{\mathrm{c}}}(U_{\mathrm{dc}} - U_{\mathrm{out}})(M_3 \sin \omega t) \tag{25}$$

The RMS values of the current ripple in the three-level mode is calculated as:

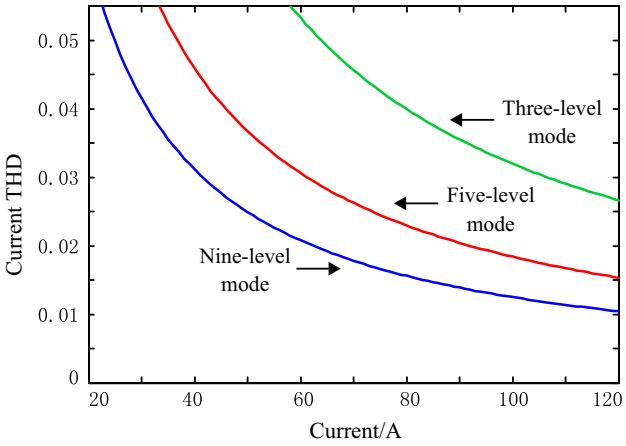

Fig. 6 Current THD of the three modes

Table 3 Simulation and experimental parameters

Parameters	Values
dc source/V	60
Capacitor/μf	2200
Load resistance/Ω	25
Load inductance/mH	18
Switching frequency/Hz	1000
Modulation frequency/Hz	50

$$\Delta I_{\mathrm{RMS3}} = \frac{1}{2\sqrt{3}}\sqrt{\frac{2}{\pi}\left(\int_0^{\pi/2} \Delta I_{\mathrm{m31}}^2 \mathrm{d}\omega t\right)} \tag{26}$$

The current THD of the proposed inverter in the five-level mode is expressed as:

$$\mathrm{THD}_3 = \frac{\sqrt{2}\Delta I_{\mathrm{RMS3}}}{I_{\mathrm{M}}}, \quad M_3 \in [0, 1] \tag{27}$$

To intuitively analyze the difference of the current THD in the three modes, specific data was substituted into the above equations. Take a grid-connected application as an example, 'U_{out}' in (19), (22) and (25) is replaced with 'E_{m} sinωt', and its value is 311 V. For comparison purposes, U_{dc} in both the nine-level mode and the five-level mode is 200 V; and U_{dc} in the three-level mode is 400 V. The other parameters used in the calculations are shown in Table 2. Figure 6 shows different current THDs under the three operation modes. As can be seen from Fig. 6, the current THD decreases along with the increase of the current. When the current is the same, the current THD of the nine-level mode is the lowest, and that of the three-level mode is the highest.

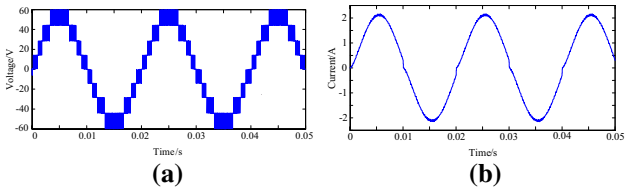

Fig. 7 Simulation waveforms of the nine-level mode: **a** output voltage; **b** output current

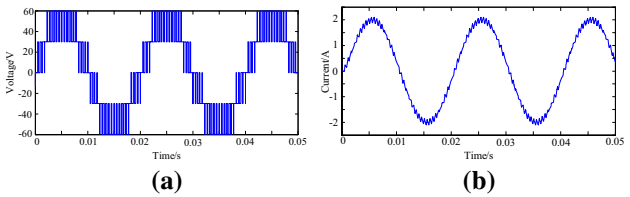

Fig. 8 Simulation waveforms of the five-level mode: **a** output voltage; **b** output current

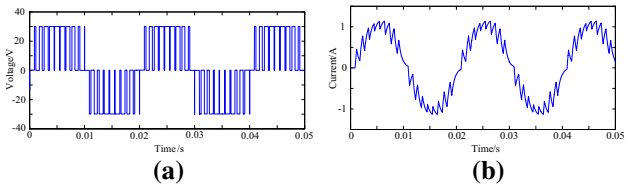

Fig. 9 Simulation waveforms of the three-level mode: **a** output voltage; **b** output current

4 Simulation and experimental results

4.1 Simulation results

To verify the correctness and feasibility of the proposed inverter, simulation models are established on a MATLAB/Simulink platform. The parameters used in the simulations are shown in Table 3.

The steady-state performance of the inverter under each mode was simulated first. The proposed inverter has three modes. Simulation results of the nine-level mode are shown in Fig. 7. Figure 7b shows the current waveform with a 25 Ω resistive load and an 18mH inductive load. It can be seen from Fig. 7 that the inverter can output a nine-level voltage waveform with a frequency of 50 Hz as required.

Simulation results of the five-level mode are shown in Fig. 8. Figure 8b shows the output current with the same load as the nine-level mode. The inverter can output a five-level voltage waveform and the switching frequency of the output voltage is halved when compared with Fig. 7a.

Simulation results of the three-level mode are shown in Fig. 9. Comparing the above three simulation results, the quality of the output current under the nine-level mode is the best, and the quality of the output current under the three-level mode is the worst. Simulation results can confirm the theoretical analysis in this paper.

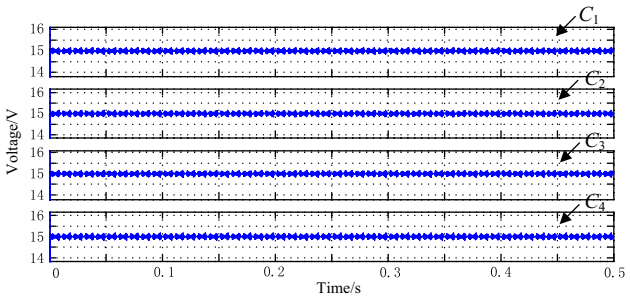

Fig. 10 Voltage waveforms of four capacitors

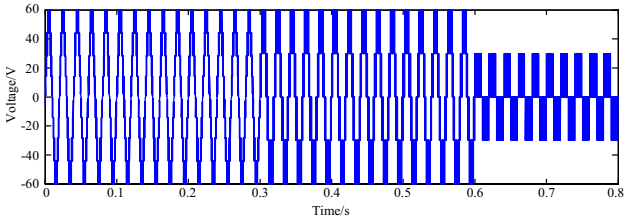

Fig. 11 Voltage waveform among the different modes

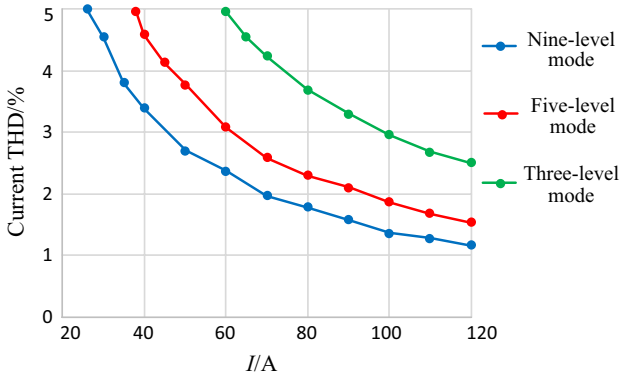

Fig. 12 Simulation curves of the current THD

When the inverter works in the nine-level mode, the capacitor voltage must be balanced. Figure 10 shows the voltage waveforms of the four capacitors. The obtained simulation results indicate that the voltages of the four capacitors are well balanced under the modulation strategy proposed in this paper.

The dynamic performance of the proposed inverter was also simulated. Figure 11 shows the simulation results of the online transition process with different modes. With the given control signals at 0.3 s and 0.6 s, the inverter

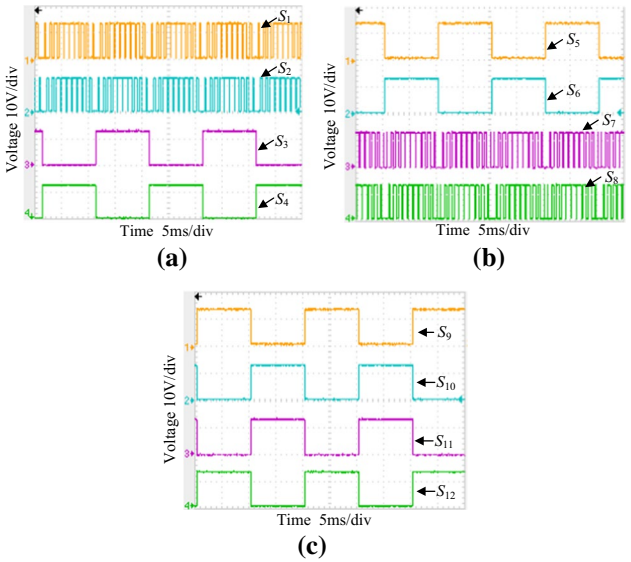

Fig. 13 Switching signals of the nine-level mode: **a** signals of S_1–S_4; **b** signals of S_5–S_8; **c** signals of S_9–S_{12}

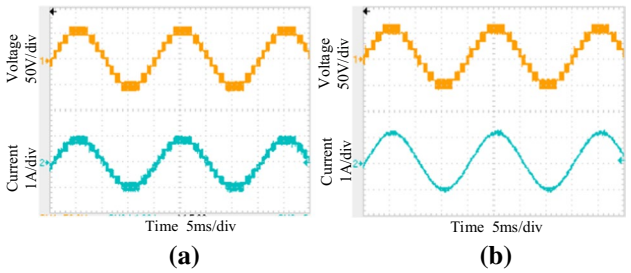

Fig. 14 Output waveforms of the inverter in the nine-level mode: **a** resistive load; **b** inductive load

changes from the nine-level mode to the five-level mode at 0.3 s, and from the five-level mode to the three-level mode at 0.6 s. The output waveform is correct and good during the transition process.

Simulation results of THD corresponding to different currents are obtained by an FFT analysis. In addition, simulation results of the current THD curve are obtained, as shown in Fig. 12. The colored points are simulation values of different currents. By comparing the THD simulation results with the THD calculation results in Fig. 6, it can be seen that the simulation results are in accord with the calculation curves, which verifies the correctness of calculations in this paper.

4.2 Experimental results

An experimental platform was implemented to further validate the proposed inverter and its modulation strategy.

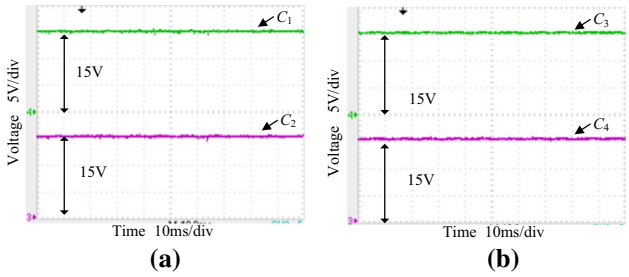

Fig. 15 Capacitor voltage waveforms: **a** voltage of C_1 and C_2; **b** voltage of C_3 and C_4

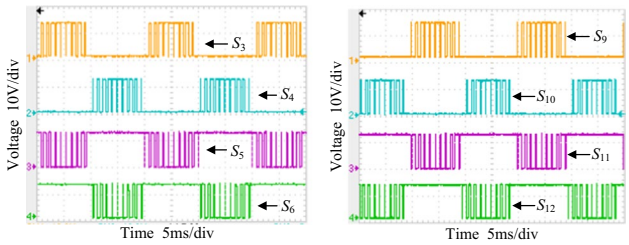

Fig. 16 Switching signals of the five-level mode: **a** signals of S_3–S_6; **b** signals of S_9–S_{12}

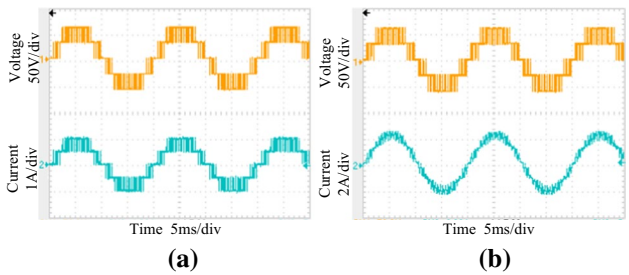

Fig. 17 Output waveforms of the inverter in the five-level mode: **a** resistive load; **b** inductive load

The parameters in the experiment are the same as those used in the simulation, as shown in Table 3.

Firstly, the steady-state performance of the inverter was tested. Experiments of the inverter working in different modes were conducted, and output voltage and current waveforms were observed. Figure 13 shows signal waveforms of twelve switches in the nine-level mode. It can be seen from this figure that the four dc side switches work at a high frequency and the eight bridge arm switches work at a low frequency. The obtained experimental signals are consistent with modulation signals.

Figure 14 shows output voltage waveforms and current waveforms of the proposed inverter in the nine-level mode. Figure 14a shows output waveforms with a 60 Ω resistive

load, and Fig. 14b shows output waveforms with a 25 Ω resistive load and an 18mH inductive load.

Figure 15 shows dc side capacitor voltage waveforms when the inverter works in the nine-level mode. It can be seen from this figure that the voltage of each capacitor is half of the dc side voltage. The voltage values are stable and the voltage ripple is small. This shows that the voltage balance strategy in this paper is effective.

Figure 16 shows switching signal waveforms of the five-level mode. As can be seen, eight switches participated in the modulation. The obtained experimental switching signals are consistent with the modulation signals.

Figure 17 shows output voltage waveforms and current waveforms of the proposed inverter in the five-level mode. Figure 17a shows output waveforms with a 60 Ω resistive load, and Fig. 17b shows output waveforms with a 25 Ω resistive load and an 18 mH inductive load.

Figure 18 shows switching signal waveforms of the three-level mode. Four bridge arm switches participated in the modulation. The obtained experimental switching signals are consistent with the modulation signals.

Figure 19 shows output voltage waveforms and current waveforms of the proposed inverter in the five-level mode. Figure 19a shows waveforms with a 60 Ω resistive load, and Fig. 19b shows waveforms with a 25 Ω resistive load and an 18mH inductive load. It can be observed from Figs. 14, 17 and 19 that the inverter has the best output characteristics under the nine-level mode, and that the voltage waveform has the highest switching frequency. With the same load, the output characteristics under the three-level mode are the worst. The obtained voltage waveform has a lower switching frequency. These experimental results are consistent with the theoretical analysis and simulation results in this paper.

Then the dynamic performance of the proposed inverter was tested. The inverter changes its working modes online by given control signals. Figure 20 shows experimental

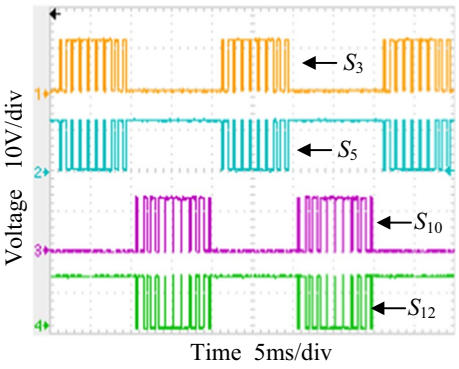

Fig. 18 Switching signals of the three-level mode

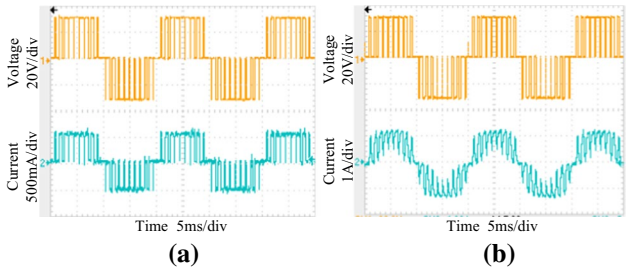

Fig. 19 Output waveforms of the inverter in the three-level mode: **a** resistive load; **b** inductive load

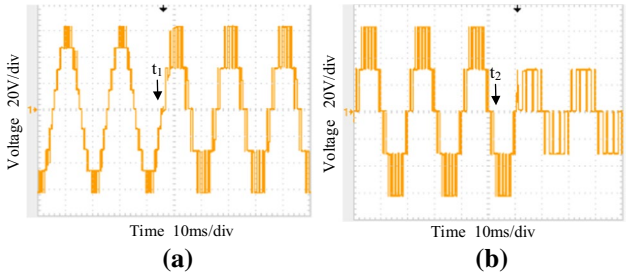

Fig. 20 Output voltage waveforms with inverter mode transitions: **a** nine to five-level mode; **b** five to three-level mode

results of an online transition between the different modes of the inverter.

In Fig. 20a, the inverter changes from the nine-level mode to the five-level mode, and t_1 is the moment to give a switch signal. In Fig. 20b, the inverter changes from the five-level mode to the three-level mode, and t_2 is the moment to give a switch signal. Since the circuit structure changes from cascade to parallel, the output voltage of the three-level mode is halved. The obtained experimental results are in agreement with simulation results. It can be seen from these results that the working modes can switchover online and that the output waveforms is good during the transition process.

5 Conclusions

To achieve a wide operational range and to reduce the power losses, a flexible cascaded multilevel inverter is proposed in this paper. According to the actual working conditions, the inverter can change its topology structure to work in three modes. The proposed inverter can reduce the number of active switch devices to decrease the inverter losses in the three-level mode. In addition, the inverter can provide more output levels to improve the quality of its output waveforms in the nine-level mode.

Furthermore, its modulation strategies and voltage balance method were analyzed. Simulations and experiments were conducted. The obtained results indicate that the topology and modulation strategy of the inverter are correct and valid. In addition, the online transition process between the different modes is effective and favorable. The proposed inverter can achieve a wide operational range and decreased total losses.

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