# An Improved Bipolar-Type AC-AC Converter Topology Based on Non-Differential Dual-Buck PWM AC Choppers

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***Abstract*—A novel single-phase pulse width modulation (PWM) direct ac-ac converter based on two-level non-differential dual-buck ac chopper legs with inverting and non-inverting operations is first proposed in this paper. It has the ability to resolve both voltage sag and swell problems at the same time when used as distributed flexible voltage conditioner (DFVC). Compared to the traditional ac-ac converter, it has much enhanced system reliability thanks to no shoot-through problems even when all switches of each ac chopper legs are turned on, and therefore, the PWM dead-time is not needed leading to improving the utilization of the duty cycles. Only half of the switches in the proposed converter are switched at high frequency during a switching period at most, which significantly reduces the total switching loss. In particularly, the converter has two greatest advantages that it retains the common sharing ground of the input and output and has the same buck/boost operation process for non-inverting and inverting modes. In order to fully testify the performance of the proposed converter, a 500W experimental prototype is built and tested at different conditions.**

***Index Terms*—AC-AC converter, bipolar voltage gain, non-differential AC chopper, voltage sag and swell, buck/boost operation process.**

## I. INTRODUCTION

THE parameters of electrical energy, such as supply voltage amplitude, has a great influence on both the operation of the power grid and the use of the load side [1]. With the continuous access of distributed generation, the voltage quality becomes worse. Among the many power quality problems, the sag and swell in supply voltage are the main problems. Voltage sag and swell will do a great deal of harm to the end-user, especially from the viewpoint of the sensitive loads such as hospitals, data centers, etc. In the case of big plants and factories, voltage sags and swells may cause financial losses [2].

In order to fully mitigate unwanted effects of supply voltage, mainly voltage sags and swells, various types of devices have been developed in recent literature. These devices are primarily referred to as voltage sag/sell compensators [3]-[4], ac voltage regulators [5], ac stabilizers [6], ac voltage sag supporters [7], voltage conditioners [8], dynamic voltage restorers (DVR) [9]-[12], distributed flexible voltage conditioner (DFVC) [13], etc. Either of these devices can be designed with a voltage source inverter (VSI) or a direct PWM ac-ac converter. AC voltage compensator based on VSI can be divided into two main types. One of the types is adopting dc-ac converters, which requires independent external energy storage systems such as batteries, capacitors, super magnetic energy storage, and so on. This feature determines that it is not capable of compensating deep and long-duration voltage sags or swells, and its magnitude and ride-through capability depend on the size and capacity of the storage systems [14]. Therefore, ac voltage compensator adopted dc-ac converters is not suitable for high power applications. The other ac voltage compensator based on ac-dc-ac converters does not need to use external energy storage systems, but it adds one ac-dc power processing stage with bulky DC link. These facts will reduce the efficiency of the whole systems and add to the maintenance burden. If the ac voltage compensator implements the direct ac-ac converters, the DC-link will be saved, the whole systems will be improved, and no external energy storage systems will be required, the devices volume and cost also will be reduced. Specially, the direct ac-ac converters are more attractive in applications where only need to maintain the grid voltage amplitude without changing phase shift and frequency at the same time. Under this motivation, the direct ac-ac converter is to be studied continuously [15]-[16].

The simplest and most basic ac-ac converters including buck, boost, buck-boost topologies, etc. These converters inherit the merits of simple structure, uncomplicated control, and high conversion efficiency, but they have common commutation problems due to using ac switches [17]-[18]. To overcome commutation problems, RC buffer circuit and the soft commutation strategies are the two commonly used methods. However, these two methods have some shortcomings, such as the commutation strategy cannot guarantee the zero-crossing reliable commutation, and the output voltage waveforms are distorted because energy is dissipated in the RC snubber circuits. Recently, a novel single-phase PWM ac-ac converters solving commutation problem without using RC snubber circuits or soft commutation strategies is presented in [19]-[21].

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These converters, while effectively solving the commutation problems, all suffer from a unipolar voltage gain range, which, in use of the grid-voltage compensation, restricts them to mitigate either voltage sag or swell but not both [22].

To overcome this constraint of ac-ac converter applications, a cost-effective ac voltage stabilizer based on ac-ac converters is proposed in [23], as shown in Fig. 1 (a). It can output bipolar voltage by adding a mechanical switch, but there are some shortcomings in mechanical switches such as slow response speed, voltage step change, etc. In [24], a Z-source PWM ac-ac converter is presented to achieve the bipolar voltage gain through an additional impedance network. However, the sharp rise and fall in its gain during the non-inverting buck operation are quite challenging for the controller. Another Z-source ac-ac converter is analyzed in [25], it is able to output bipolar voltage, but it requires a new commutation strategy to achieve safe commutation. The topology shown in Fig. 1(b) is a unified non-inverting and inverting PWM ac-ac converter capable of obtaining bipolar voltage gains [26]. But the converter may have commutation problems due to employing bidirectional switches, which decreases the reliability of the systems. Hence, it also needs to adopt a safe commutation strategy to address commutation problems [27]. Recently, a novel bipolar-type direct ac-ac converter is presented in [13], as shown in Fig. 2(c). This converter not only resolves the commutation problem, but also retains the common sharing ground of the input and output. Especially, the main advantage is that the converter has the same buck/boost operation process for non-inverting and inverting modes. However, it is necessary for this converter to set a dead-time to solve the shoot-through problems due to the two active switches in each legs of the converter, which reduces utilization of the duty cycles. A buck-boost ac-ac converters adopting switching cell structured and coupled inductor is proposed in [28], as shown in Fig. 1(d). This converter effectively solves the commutation problem and does not need to set dead-time. But it needs more numbers of passive components, which increases the volume of the devices in high-power applications. Moreover, similar to the converter proposed in [29]-[32], the converter has not the same buck/boost operation process for non-inverting and inverting modes and have not the common ground on input and output. In addition, a high-frequency isolated AC-AC converter with bipolar voltage gain is proposed in [33]-[34]. However, this converter has some drawbacks, such as a converter proposed in [34] needs to a safe-commutation strategy, which reduces its reliability.

To overcome above constraints, this paper investigates a novel single-phase ac-ac converter based on two-level non-differential dual-buck ac chopper legs with bipolar voltage gains. The DB-AC has the following advantages:

1) It can achieve continuous and bipolar voltage transfer without drastic changes and the combination of multiple PWM modulation modes increases the degree of freedom of control. It employs less passive devices, thus reducing footprint of the converter.

2) By adopting dual-buck ac chopper legs, it does not need to set dead-time, which increases the utilization of the equivalent pulse width-modulated voltage, and leads to output waveform distortions and less energy transfer. Partial free-wheeling diodes can be chosen independently with fast reverse recovery features to minimize switching loss.

3) The limiting inductors of each ac choppers are replaced by separated inductors instead of coupled inductors, which effectively decreases the magnetic volume and improves the ability to deal with power density. The limiting inductors also contributes to the inductance of the output filter inductor, which is conducive to reducing volume of the output filters.

4) The common ground between the input and output ports is retained, the feature that output can reverse or maintain phase angle with input is supported well. Additionally, it has the same buck/boost operation process for non-inverting and inverting modes, which ensures the continuously average current supply to the output side without a high-value capacitor to supply power.

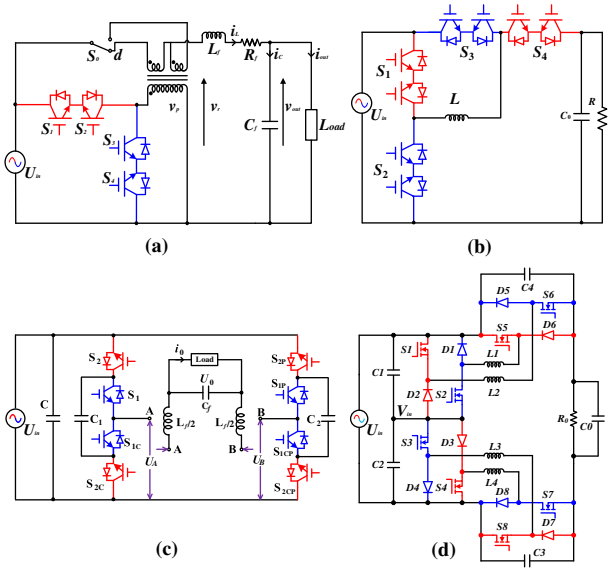



Fig. 1 Four types of bipolar AC-AC converters.

The paper is arranged as follows. The description of the proposed topology and PWM modulation principles are described in section II. Section III investigates the operation states of the ac-ac converter. Section IV discusses the design of the converter parameters. Experimental results illustrating the performance of the converter are presented in Section V. Finally, the conclusions are highlighted in Section VI.

## II. Description Of The Proposed Topology And PMW Modulation Principles

### *A. Topology of the Proposed Converter*

The novel bipolar-type dual-buck PWM AC-AC converter (DB-AC) proposed is expressed in Fig. 2. As shown in Fig. 2, the topology structure of the DB-AC is consisted of two dual-buck ac chopper legs with two separation inductors that are defined as IP-Leg (in-phase leg) and OP-Leg (out-of-phase leg) respectively, both of which are two-level non-differential ac choppers. Hence, the polarity of the output port voltage $v_{AB}$ is determined by the voltage difference between the two legs, that is $v_{AB}=v_A-v_B$, where $v_A$ and $v_B$ are IP-Leg and OP-leg voltage respectively. Four insulated gate bipolar transistor (IGBT) that two of the IGBT contain antiparallel body diodes, and the other two do not contain, two fast recovery diodes, two inductors and one capacitor are contained in each leg, and the

connected relation of the components and parts is shown in Fig. 2. The diodes $D_1$, $D_{1c}$ and $D_{1p}$, $D_{1cp}$ in each leg are fast recovery diode, which validly relieves the problems of high loss and slow turn-off of bulk diode. On the other hand, in order to reduce the influence of the source voltage, an input capacitor is added at input side. Additionally, the two legs retain a common ground connection with the input side.

The proposed DB-AC can effectively deal with the commutation problem without bulky and lossy resistor-capacitor (RC) snubbers circuits or soft commutation strategies, which obviously improves the reliability of the systems. The bipolar output voltage can be ensured by IP-Leg and OP-leg voltage, and it is precisely because of the two controllable objects of the topology that the flexibility and diversity of the proposed DB-AC can be improved commendably. With the common sharing ground of the input and output, the feature that output can reverse or maintain phase angle with input is supported well. Meanwhile, no dead time is required, which increases the utilization of the equivalent pulse width-modulated voltage, and leads to output waveform distortions and less energy transfer. The particularly outstanding superiority is that the proposed DB-AC has the same buck or boost running process for non-inverting and inverting modes, so there is no need to design high-value capacitors to ensure that the average current of the outside continuously.

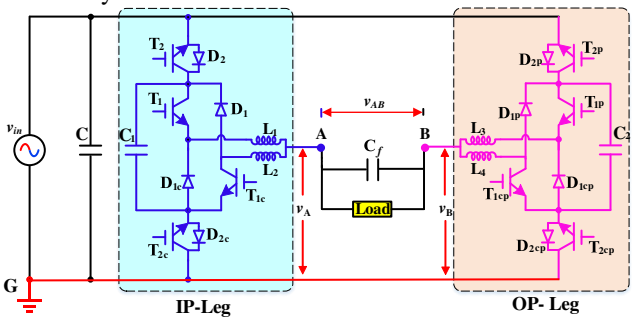



Fig. 2. Schematic of the proposed DB-AC.

### *B. PWM Modulation Principles*

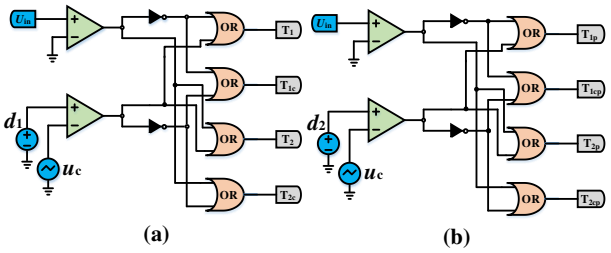



Fig. 3. PWM modulation principles.

The PWM modulation principle with zero vector coupling of the proposed DB-AC is shown in Fig. 3. A square wave signal is generated by a comparison of $v_{in}$ and zero potential. Besides, the converter flexibility is improved with two duty cycles, where $d_1$ and $d_2$ are the duty cycles of IP-Leg and OP-Leg, respectively, and $u_c$ is a triangular carrier with a scope value of 0 to 1. Compared with the interleaved PWM strategy used in [19], the proposed PWM strategies reduce partial circulation due to the absence of the mode in which all switches are turned on simultaneously. Additionally, the proposed converter has the least number of switches to do high-frequency switching in a switching period through using the proposed PWM strategies, which further reduces the total switching loss and improves the efficiency of the converters. In order to further understand the DB-AC, the comparative analysis between it and previously published bipolar voltage gain ac-ac converters is shown in TABLE I.

## III. Operation Of The Proposed Converter

According to the analysis of the PWM strategies mentioned above, the input voltage in the positive and negative half-wave has a direct effect on the working process of the converters. Considering the proposed topology is a novel bidirectional AC-AC converter and in order to analysis the working process of it in detail, the buck operation mode is clearly divided into in-phase and out-of-phase in TABLE II with the interrelation between input and output voltage.

According to the work pattern shown in TABLE II, the proposed DB-AC has a variety of operation modes. Regardless of the operating mode, the relationship between input voltage $v_{in}$ and output voltage $v_o$ is as follows.

$$v_0 = v_A - v_B = (d_1 - d_2)v_{in} \tag{1}$$

Where $v_A$ and $v_B$ are the output voltages of ports A and B, respectively, $v_A$=$d_1v_{in}$ and $v_B$=$d_2v_{in}$.

Further, the formula (1) can be rewritten

$$M_C = \frac{v_0}{v_{in}} = (d_1 - d_2) \tag{2}$$

Where $M_C$ is defined as voltage gains of the DB-AC, it reflects the input-output relationship of the converter and it is determined by the duty cycles of the two legs.

The interrelation between $M_C$ and ($d_1$, $d_2$) are presented in Fig. 4 and it is clear observed that the range of $M_C$ is from -1 to 1. That is to say, the proposed DB-AC has the capability of bipolar voltage gains. Similar to the TABLE II above, the DB-AC is divided into in-phase operation state and out-of-phase operation state based on the voltage polarity between input and output. It should be pointed out that the converter has three modulation modes (Modes I, II, II), regardless of the output voltage and the input voltage in the same phase or the inverse phase, but modulation modes I and III are the special cases of modulation mode II. To avoid repeating description, the modulation mode II is taken as an example to analyze in detail in the operation process A and B of the proposed converter. Additionally, it is stipulated that the load current $i_o$ flows from output ports A to output ports B in the positive direction, that is, $i_o$>0, and vice versa, the load current $i_o$ in a negative direction. Because the operation process of the converter is different when the input voltage is different at different half-waves, in order to fully analyze the operation process of the converter, the positive half-wave of the input voltage is analyzed in detail in process A (A. OPERATION PROCESS IN IN-PHASE), and the negative half-wave of the input voltage is analyzed in detail in process B (B. OPERATION PROCESS IN OUT-OF-PHASE).

TABLE I
COMPARISON BETWEEN THE PROPOSED DB-AC AND PREVIOUSLY PUBLISHED BIPOLAR VOLTAGE GAIN AC-AC CONVERTERS

| | DB-AC | Proposed in [26] (Fig. 1(b)) | Proposed in [13] (Fig. 1(c)) | Proposed in [28] (Fig. 1(d)) | Proposed in [24] |
|---|---|---|---|---|---|
| Voltage gain | $d_1$-$d_2$ | 2-1/$d$, $d_3$/($d_3$-1), ($d_1$-$d_3$)/(1-$d_3$) | $d_1$-$d_2$ | $d$, $d_1$/($d_1$-1), 2-1/$d_2$ | (1-$d$)/(1-2$d$),(1-2$d$)/(1-$d$) |
| Switches numbers | 8 | 8 | 8 | 8 | 2 |
| Passive devices | 4 inductors, 3 capacitors | 1 inductor, 1 capacitor | 1 inductor, 3 capacitors | 4 inductors, 5 capacitors | 3 inductors, 3 capacitors |
| Ground sharing | Yes | Yes | Yes | No | No |
| Dead time | No | Yes | Yes | No | No |
| Reliable commutation | No commutation problem | Need soft commutation strategies | No commutation problem | No commutation problem | An external snubber circuit is needed |
| Same inverting and non-inverting process | Yes | No | Yes | Possible | No |
| Adopt bidirectional switches | No | Yes | No | No | Yes |
| Controllable degrees of freedom | Two ($d_1$ and $d_2$) | One ($d$) or Two ($d_1$and $d_3$) | Two ($d_1$ and $d_2$) | One ($d$ or $d_1$or $d_2$) | One ($d$) |

TABLE II
PARTITIONING TABLE OF WORK MODE

| $v_0$ | Modulation modes | $d_1$ | $d_2$ |
|---|---|---|---|
| $v_0$ is in phase with $v_{in}$ | Mode I | $0<d_{1x}<1$ | 0 |
| | Mode II | $0<d_{1x}<1$ | $0<d_{2x}<d_{1x}$ |
| | Mode III | 1 | $0<d_{2x}<1$ |
| $v_0$ is out of phase with $v_{in}$ | Mode I | 0 | $0<d_{2x}<1$ |
| | Mode II | $0<d_{1x}<d_{2x}$ | $0<d_{2x}<1$ |
| | Mode III | $0<d_{1x}<1$ | 1 |

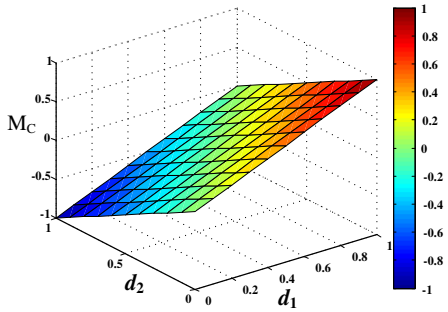


Fig. 4 The relationship between $M_C$ and ($d_1$, $d_2$).

### A. Operation Process in In-phase

In this operation process $M_C$>0, and the output voltage $v_o$ maintains the same phase as the input voltage $v_{in}$, and the two duty cycles of $d_1$ and $d_2$ range from 0 to 1 respectively, but $d_1$>$d_2$. At this modulation modes, the proposed converter has the maximum controllable degree of freedom. Further, in order to analyze in detail, the working process is discussed when the $i_o$>0, $i_o$<0, and the input voltage is positive half-wave. At this point, the switches $T_2$, $T_{2c}$, $T_{2p}$ and $T_{2cp}$ are always ON, $T_1$, $T_{1c}$, $T_{1p}$ and $T_{1cp}$ are modulated in a PWM manner. The gate signal and operation with current flowing of the proposed DB-AC is shown in Fig. 5 and Fig. 6, respectively. Fig. 6 (a), (b), and (c) are employed to illustrate the working process of the proposed converter when $i_o$>0, and Fig. 6 (d), (e), and (f) are used to describe the working process of the converter when $i_o$<0.

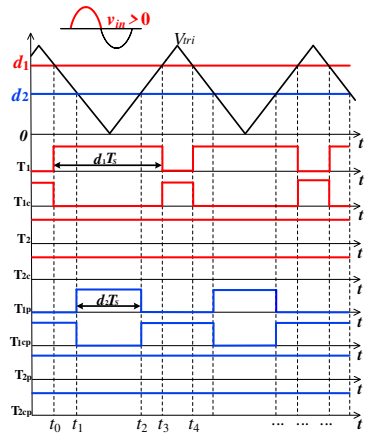
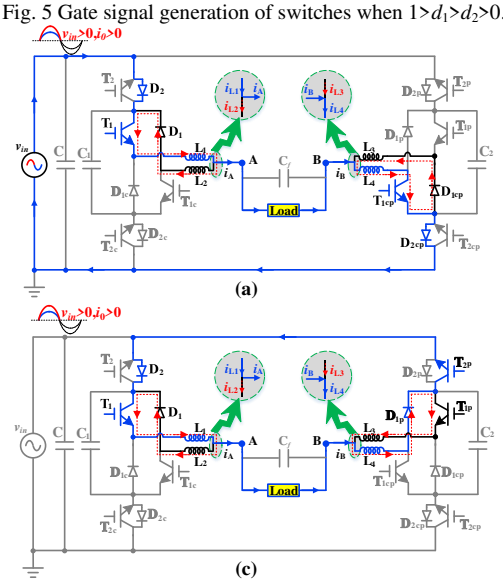


Fig. 5 Gate signal generation of switches when 1>$d_1$>$d_2$>0.



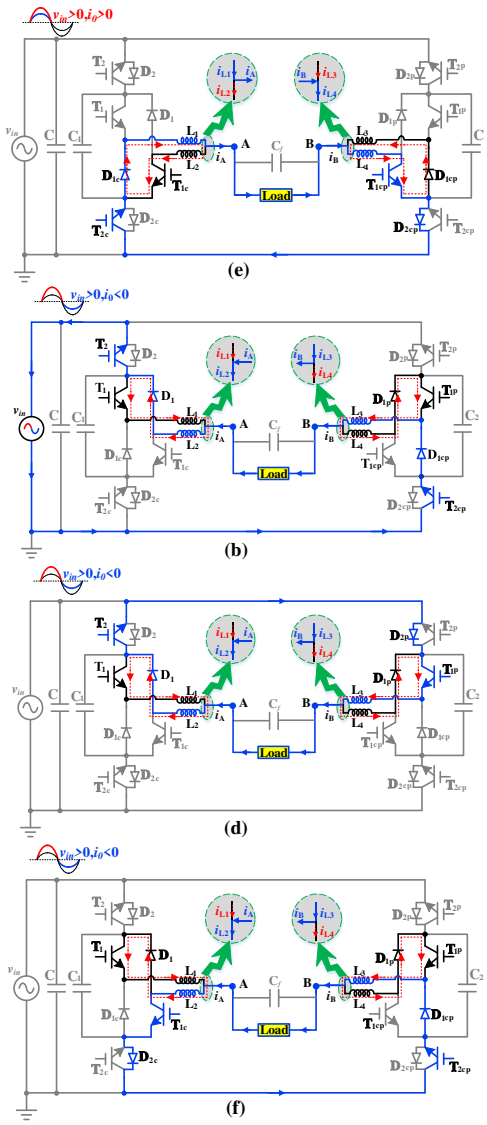



Fig. 6 The effective switching states of DB-AC under operation process A ($1>d_1>d_2>0$) and $v_{in}>0$.

**State I [$t_0$~$t_1$]**

As shown in Fig. 6(a), in this state, the switches $T_2$, $T_{2c}$, $T_{2p}$, $T_{2cp}$, $T_1$ and $T_{1cp}$ are all turned on and the $T_{1p}$, $T_{1c}$ are turned off. At this time, the converter is in active state, and the voltage and current relationships are as follows:

$$v_{Lsum} = v_{in} - v_o \tag{3}$$

$$L_{eq}\frac{\mathrm{d}i_{L1}}{dt} = 2L\frac{\mathrm{d}i_{L1}}{dt} = 2L\frac{di_{L4}}{dt} = (1-d_1+d_2)v_{in} \tag{4}$$

Where $v_{Lsum}$ is the sum of voltages across all inductors, and it contains three parts: $v_{L1}$, $v_{L4}$, $L$ represent the inductance values of the separation inductors $L_1$~$L_4$.

When the inductor current $i_o$<0, the switches operate in the same order as when the inductor current $i_o$>0, but the diodes $D_2$ and $D_{2cp}$ become reverse biased, and the diodes $D_1$, $D_{1cp}$ become forward biased. Therefore, a current path shown in Fig. 6 (b) is formed. Since the inductance values of the four separate inductors are the same, the voltage and current relationships in the circuit at this time are the same as formulas (3) and (4). Consequently, the above relationship formulas are not repeated here.

**State II [$t_1$~$t_2$]**

Fig. 6 (c) is adopted to describing state II of the converter, this moment, switches $T_1$, $T_2$, $T_{2c}$, $T_{1p}$, $T_{2p}$ and $T_{2cp}$ are ON, and other switches $T_{1c}$ and $T_{1cp}$ are OFF. Additionally, the body diodes $D_1$ and the fast recovery diodes $D_{1p}$ are forward biased. The current loop is shown in Fig. 6 (b), and the relationship of the voltage and current can be expressed as follows.

$$v_L = -v_o \tag{5}$$

$$L_{eq}\frac{\mathrm{d}i_{L1}}{dt} = 2L\frac{\mathrm{d}i_{L1}}{dt} = 2L\frac{di_{L4}}{dt} = (d_2-d_1)v_{in} \tag{6}$$

Similarly, if the inductor current $i_o$<0 at this state, the diodes $D_1$ and $D_{2p}$ become forward biased, and the diodes $D_2$, $D_{1p}$ become reverse biased. Thus, the current flow loop is shown in Fig. 6 (d), and the relationship between voltage and current is similar to formulas (5) and (6).

**State III [$t_2$~$t_3$]**

State III is similar to state I, therefore, Fig. 6 (a) can also be used to describe state III. The variation of output filter inductor current is the same as that of state I, so it is not repeated. Similarly, when the inductor current $i_o$<0, the working process of the converter is the same as that of Fig. 6 (b).

**State IV [$t_3$~$t_4$]**

The converter is in state IV, when the switches $T_{1c}$, $T_2$, $T_{2c}$, $T_{1cp}$, $T_{2p}$ and $T_{2cp}$ are ON, and at the same time the switches $T_1$ and $T_{1p}$ is OFF. State IV is described in Fig. 6 (e), the converter is in continuous flow state right now. The relationship between the voltage and current can be expressed as follows.

$$L_{eq}\frac{\mathrm{d}i_{L1}}{dt} = 2L\frac{\mathrm{d}i_{L1}}{dt} = 2L\frac{di_{L4}}{dt} = (d_1-1)v_{in} \tag{7}$$

Fig. 6 (f) can be employed to describe the working process of the proposed converter with inductor current $i_o$<0 in state II. At this point, the diodes $D_{1cp}$ and $D_{2c}$ become forward biased, and the diodes $D_{1c}$, $D_{2cp}$ become reverse biased, and the inductor current also decreases linearly. The relationship between voltage and current is also similar to formulas (7).

Combined with the analysis of the working process of the proposed converters and the PWM modulation strategies mentioned above, it can be seen that each legs of the converters has no state in which all switches are turned-on simultaneously, hence the circulating currents are also eliminated. Additionally, through the above analysis, we can see that the current flow direction on the four separated inductors is fixed regardless of the direction of the load current. Fig. 6 also shows that only two separated inductors ($L_1$ and $L_4$) or ($L_2$ and $L_3$) conduct the current ($i_A$ and $i_B$) at a time. At the same time, it can be seen that no matter in which state the converter works, the current always has a current loop, which effectively ensures the safe commutation of the proposed converter. The current relationship is as follows:

$$i_A = i_{L1} - i_{L2} = i_B = i_{L4} - i_{L3} \tag{8}$$

When the input voltage is in negative half-waves, the modulation principles and working process of the proposed converter are similar to the above analysis. Hence, in order to avoid repetition, this paper will not describe it again.

*B. Operation Process in Out-of-phase*

Similar to the above, when the output voltage $v_o$ is out of phase with the input voltage $v_{in}$, the operation and analysis process is the same as that of the in-phase above. And limited to

length, the detailed analysis is not carried out in this paper and only shown the relevant information in Fig. 7 and Fig. 8. In order to increase the diversity of analysis, the working process diagram of the proposed converter is given when the input voltage is negative half-wave.

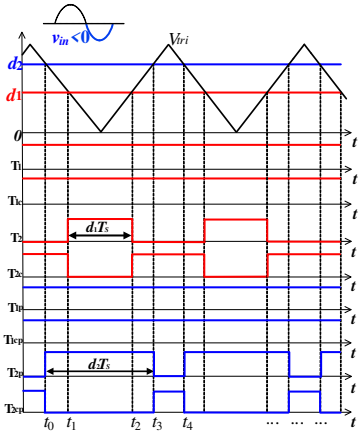
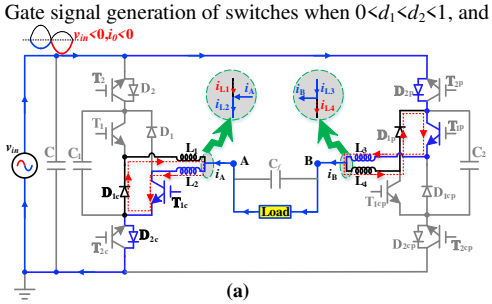
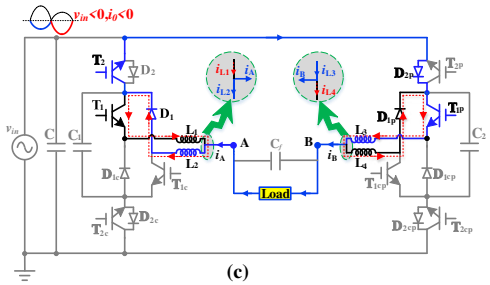



Fig. 7 Gate signal generation of switches when $0<d_1<d_2<1$, and $v_{in}<0$.




(a)

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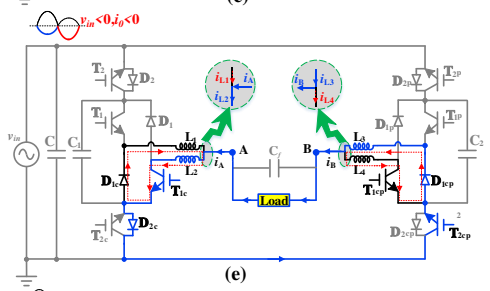
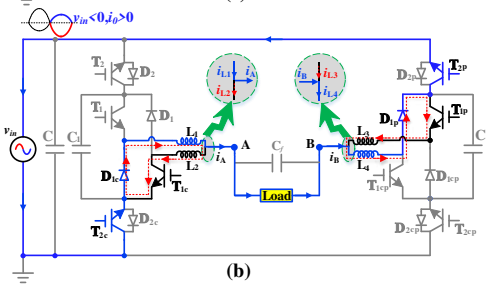
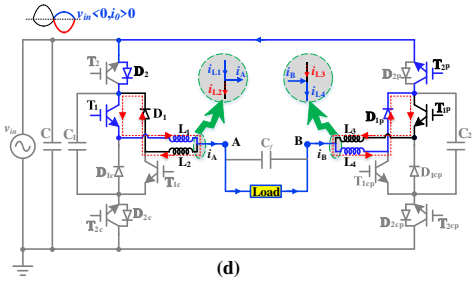


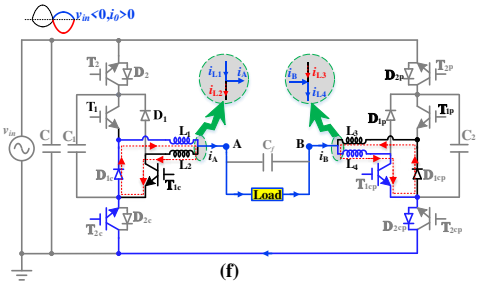

(e)




(b)




(d)



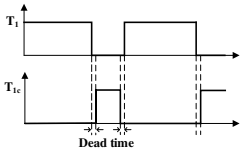

(f)

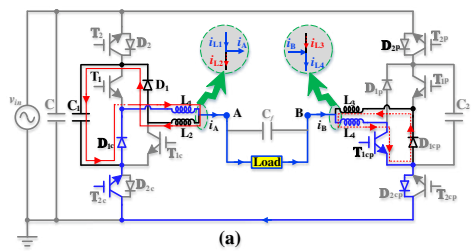
Fig. 8 The effective switching states of DB-AC under operation process B ($1>d_2>d_1>0$) and $v_{in}<0$.

### *C. Dead Time and Overlap Time*

Due to the delayed response of electronic circuits and semiconductor switching devices, the two switches with complementary signals may have the problem of dead-time and overlap-time in the operation of the converter. Taking the output voltage $v_o$ is in phase with $v_{in}$ and the converter adopts the modulation modes I as an example, the analysis will be carried out. In addition, this paper only takes the positive half-wave of input voltage as an example to carry on the analysis. At present, the switches $T_2$, $T_{2c}$, $T_{1cp}$, $T_{2p}$ and $T_{2cp}$ are always ON, and $T_{1p}$ is always OFF.

Ideally, the switches $T_1$ and $T_{1c}$ are modulated in a PWM manner, and the switches use complementary signals. However, due to the existence of dead time in the actual work of the converter, the switches $T_1$ and $T_{1c}$ are turned off in the dead-time, shown in Fig. 9. At present, the capacitor $C_1$ or $C_2$ bypass the separated inductors currents, shown in Fig. 9 (a) and (b). Similarly, there will also be overlap time in the actual work of the converter. The overlap time in which the switches $T_1$ and $T_{1c}$ are turned ON, shown in Fig. 10. The separated inductors limit the shoot-through current by providing a high impedance path at this time [35].




(a)

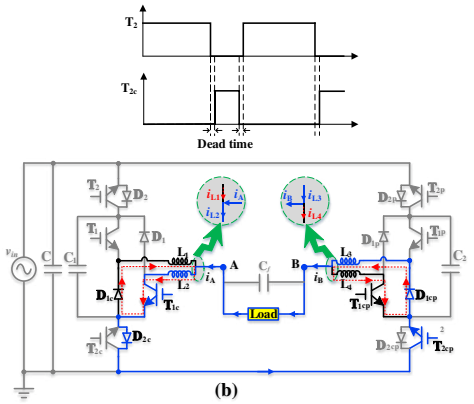



Fig. 9 Operation of the DB-AC during dead time. (a) $i_o$>0. (b) $i_o$<0.

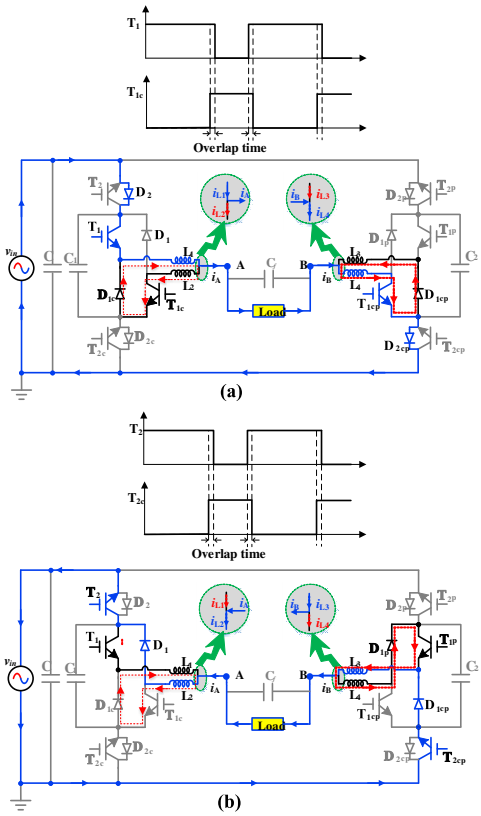



Fig. 10 Operation of the DB-AC during dead time. (a) $i_o$>0. (b) $i_o$<0.

Through the detailed analysis of the different working processes mentioned above, it can be seen that the converters mentioned in this paper can operate reliably under different working conditions and the proposed converter can guarantee the safe commutation without any other measures.

## IV. Design Consideration

Based on the above analysis, in this section, the guidelines of the parameter selection for the DB-AC are given. The known parameters: input voltage $v_{in}$=160-200V (50Hz) ac, range of voltage gain $M_C$ is [-1, 1], output voltage $v_o$=80-120V (50Hz) ac, the rated power of the converter is $P_o$=500W, allowable current and voltage ripples $k_i \leqslant 20\%$ of $i_L$ and $k_v \leqslant 20\%$ of $v_o$ (or $v_{in}$), and assuming that the minimum conversion efficiency of the proposed converter is 0.8.

### A. Selecting of Switches

The two important bases for selecting the switches are the maximum current through the switches and the maximum voltage across the switch when it is open. In this topology, the maximum voltage across each switch is equal to the input peak voltage, that is $v_{in.pk}$=282.84V. The maximum current through the switches is given by the following equation:

$$I_{S.\max} = \frac{v_0 i_0}{v_{in.\min}\eta} = \frac{P_0}{v_{in.\min}\eta} = \frac{500W}{80V} = 6.25A \qquad (9)$$

Therefore, the switches used in proposed converter is initially selected as an IKW75T60 (600V/75A) and IGW50T60 (600V/50A) IGBT. As is well known, the higher the switching frequency is, the less the filters will be at a cost of more switching losses. But, considering the selected switches type, the switching frequency $f_s$ is chosen as 18 kHz as a tradeoff. Additionally, diodes $D_1$, $D_{1c}$, $D_{1p}$ and $D_{1cp}$ choose fast recovery diodes, the type of which is RHRG6080.

### B. Selecting of Separated Inductors

According to the above analysis, when the two duty cycles $d_1$ and $d_2$ of the converter are between 0 and 1, the converter has four working states in a switching period, of which two are active modes and two are continuous modes. Additionally, according to the different relationship of the two duty cycles, the relationship between the duration of the continuous current in two continuous current modes of the converter is obtained as follows.

If $d_1+d_2>1$,

then $(1-d_1)T_S>d_2T_S$.

Similarly, if $d_1+d_2=1$, then $(1-d_1)T_S=d_2T_S$; If $d_1+d_2<1$, then $(1-d_1)T_S>d_2T_S$. Therefore, in order to ensure continuous-conduction mode (CCM) operation of the converter, the designed inductor must satisfy the continuity of the CCM under the different operation modes of the converter. Additionally, the maximum and minimum voltage gains of the converter can be determined according to the input and output voltages of the converter.

$$M_{C.\max} = \left(d_{1x} - d_{2x}\right)_{\max} = \frac{v_{0.\max}}{v_{in.\min}} = \frac{120}{160} = 0.75 \qquad (10)$$

$$M_{C.\min} = \left(d_{1x} - d_{2x}\right)_{\min} = \frac{v_{0.\min}}{v_{in.\max}} = \frac{80}{200} = 0.4 \qquad (11)$$

It can be seen from the above formula that different combinations can be realized through two duty cycles when the voltage gain $M_C$ is guaranteed, which effectively improves the controllable freedom of the converter. It should be pointed out that during the design of the converter in this paper, we assume that the duty cycles $d_{2.\min}$=0.1. Therefore, the maximum and minimum values of duty cycles $d_1$ can be determined, $d_{1.\max}$=0.85, $d_{1.\min}$=0.5. The following is a discussion of inductor design under different operation conditions.

1) When $d_1+d_2<1$

During one switching period $T_s$, there is

$$L_{eq}\frac{\Delta i_L}{(1-d_1)T_S} = v_0 \qquad (12)$$

In the formula above, $\Delta i_L=2k_iI_L$ and $I_L$ represent current ripple and average value of $i_L$, respectively. For the converter, we can get formulas (13) and (14).

$$v_{in} i_{in} \eta = v_0 i_0 \tag{13}$$

$$i_{in} = M_C I_L = (d_1 - d_2) I_L \tag{14}$$

Combining (2), (13) and (14), we can get the formula (15).

$$I_L = \frac{i_0}{\eta} \tag{15}$$

From (10), (12) and (15), equivalent inductor $L_{eq}$ must be satisfied such that

$$\begin{aligned} L_{eq} &\geq \frac{v_{0.\max}(1-d_{1.\max})\eta_{\min}}{2k_i f_S i_{0.\min}} \\ &= \frac{120\times(1-0.85)\times 0.8}{2\times 0.2\times 18\times 10^3\times(500/120)} = 0.48mH \end{aligned} \tag{16}$$

Therefore, the separated inductors used in paper is selected as $L_1$=$L_2$=$L_3$=$L_4$=$L_{eq}$/2=0.24$m$H.

2) When $d_1$+$d_2$>1

The design principle of the inductor is similar to the above, so it is not discussed here. We can get the following formula for calculating separated inductors $L$.

$$\begin{aligned} L_{eq} &\geq \frac{v_{0.\max} d_{2.\min} \eta_{\min}}{2k_i f_S i_{0.\min}} \\ &= \frac{120\times 0.1\times 0.8}{2\times 0.2\times 18\times 10^3\times(500/120)} = 0.32mH \end{aligned} \tag{17}$$

Therefore, the separated inductors used in paper is selected as $L_1$=$L_2$=$L_3$=$L_4$=$L_{eq}$/2=0.16$m$H.

In order to ensure the CCM of the converter under different conditions, the inductance value of the separated inductor is 0.3$m$H.

### C. Selecting of Output Filter Capacitor $C_f$

During one $T_s$, the following equation is gained such that

$$\Delta v_0 = \frac{i_0 \Delta t}{C_f} = \frac{i_0\left(\frac{d_1 - d_2}{2}\right)T_S}{C_f} \tag{18}$$

To limit the output voltage ripple, output filter capacitor $C_f$ must satisfy the following:

$$\begin{aligned} C_f &\geq \frac{i_{0.\max}(d_1-d_2)_{\max}}{k_u v_{0.\min} f_S} = \frac{i_{0.\max} M_{C.\max}}{k_u v_{0.\min} f_S} \\ &= \frac{(500/80)\times 0.75}{0.2\times 80\times 18\times 10^3} = 16.28\mu F \end{aligned} \tag{19}$$

The maximum voltage across $C_f$ is $\sqrt{2}v_{0.\max} = 170$, therefore, $C_f$ is chosen as 20$\mu$F/850V.

TABLE III
SPECIFICATION OF THE DB-AC EXPERIMENT

| Parameters | Values |
|---|---|
| Peak Input voltage $v_{in}$ | [160-200]/50Hz |
| Voltage gains $M_c$ | [-1 1] |
| Output power $P_o$ | 500W |
| Switching frequency $f_c$ | 18kHz |
| Separated inductors $L_1$~$L_4$ | 0.3$m$H |
| Capacitors $C$, $C_1$, $C_2$, $C_f$ | 20$\mu$F |
| IGBTs $T_1$, $T_{1c}$, $T_{1p}$,$T_{1cp}$ | IGW50T60 |
| IGBTs $T_2$, $T_{2c}$,$T_{2p}$,$T_{2cp}$ | IKW75T60 |
| Diodes | RHRG6080 |

## V. EXPERIMENTAL RESULTS OF THE DB-AC

### A. Experimental Results of DB-AC

In order to verify the rationality and feasibility of the proposed AC-AC converter, a 500-W laboratory prototype of the DB-AC is fabricated and tested successfully. The photograph of the experimental setup is shown in Fig. 11, and the design specifications of the converter are offered in Table IV. For fully proving the performance and advantage of the proposed AC-AC converter, several different experiments were conducted specifically under the working scenarios shown in TABLE IV.

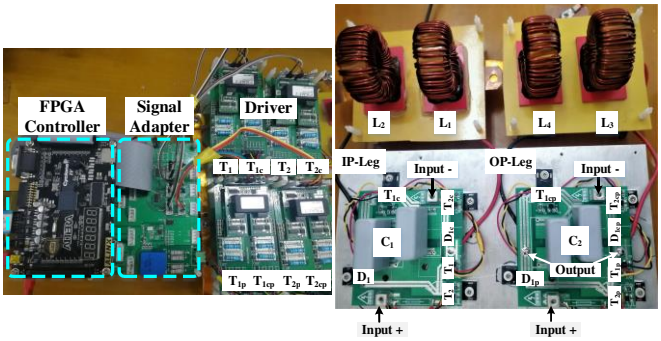



Fig. 11 Photograph of the experimental prototype.

TABLE IV
EXPERIMENTAL SCENARIOS OF THE DB-AC

| Scenario number | $d_1$ | $d_2$ | Load | Operation process |
|---|---|---|---|---|
| Scenario I | 0.85 | 0.25 | $R$=20Ω | In-phase |
| Scenario II | 0.4 | 1 | $R$=20Ω, $X_L$=12.1Ω | Out-of-phase |
| Scenario III | 0.6 | 0 | non-linear load | In-phase |

**Scenario I**

Fig. 12-15 show the results of Scenario I. Fig. 12 shows the four switches ($T_1$, $T_{1C}$, $T_2$, $T_{2C}$) signals of DB-AC. It can be seen from the diagram that there are only two switches operating at high frequency on one leg in each half-wave period, and the other two switches are in the low-frequency and normally open state. On the other hand, the two complementary signals do not have any delay during the switching process, that is to say, the proposed AC-AC converter does not need to set dead-time during its operation, which is completely consistent with theoretical analysis. Fig.13 (a) shows the waveforms of the input voltage $v_{in}$, output voltage $v_o$, and output current $i_o$. And Fig. 13 (b) shows the voltage waveforms of the capacitors $C_1$, $C_2$ and the voltage waveforms of the switches $T_2$, $T_{2P}$. It can be seen that the voltage at both ends of switches and capacitors are half-wave voltage, and the maximum value is the peak value of input voltage $v_{in}$. The high frequency voltages $v_A$, $v_B$, $v_{AB}$ and unfiltered current $i_H$ waveforms are shown in Fig. 14(a). Fig. 14(b) also shows the zoomed waveforms of $v_A$, $v_B$, $v_{AB}$ and $i_H$. As can be seen, unfiltered current $i_H$ has four change process within one cycle. Fig. 15 shows the voltage waveforms of switches $T_1$, $T_{1P}$ and current waveforms of separated inductors $L_1$, $L_3$. Similarly, Fig. 15 (b) shows the zoomed waveforms. The results waveforms prove that there is no excessive voltage and current surges in the converter during the Scenario I and the experimental results are in good agreement with the theoretical analysis results above.

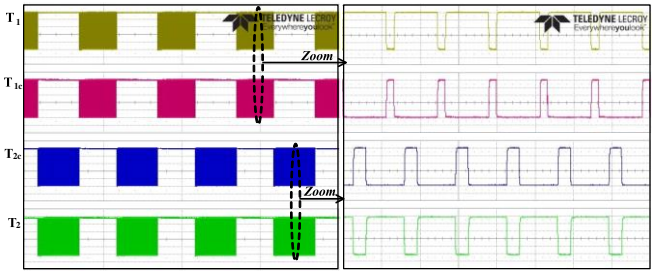



Fig. 12 Switching signals of $T_1$, $T_{1C}$, $T_2$, $T_{2C}$. (Time: 20*ms*/div and 40$\mu$*s*/div).

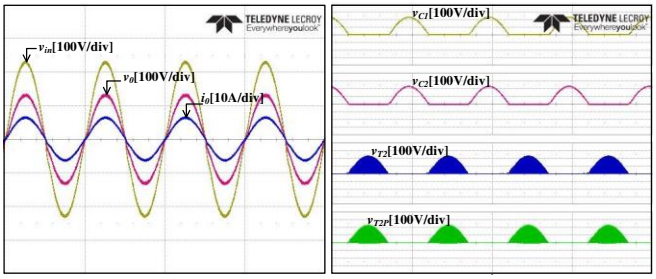



Fig. 13 Experimental waveforms of the DB-AC under Scenario I with a pure resistive load (a) Waveforms of input voltage $v_{in}$, output voltage $v_o$, and output current $i_o$ with 20*ms*/div. (b) Voltage waveforms of capacitors ($C_1$, $C_2$), and switches ($T_2$, $T_{2P}$) with 20*ms*/div.

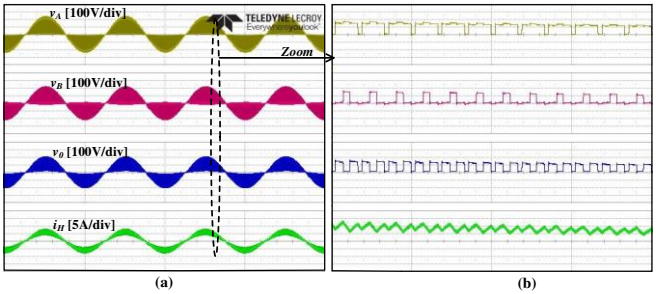



Fig. 14 High frequency voltages $v_A$, $v_B$, $v_{AB}$ and unfiltered current $i_H$ waveforms (a) Time at 20*ms*. (b) Time at 200$\mu$*s*.

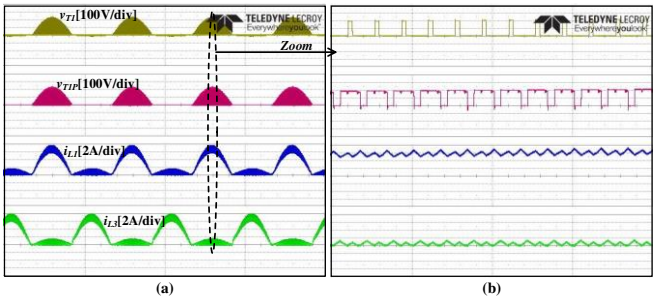



Fig. 15 Voltage waveforms of switches $T_1$, $T_{1P}$, current waveforms of limiting inductors $L_1$, $L_3$. (a) Time at 20*ms*/div (b) Time at 200$\mu$*s*/div.

**Scenario II**

Fig. 16-18 show the results of Scenario II. Unlike Scenario I, in this case, the output voltage $v_o$ is out of phase with the input voltage $v_{in}$. Besides, in order to distinguish the performance of the converter, the load type is selected for *RL* load and set the duty cycle $d_2$ to 1. The specific analysis are as follows.

Fig. 16 (a) shows the input voltage $v_{in}$, the output voltage $v_o$ and the output current $i_o$. As can be seen from the graph, the difference of phase angle between $v_{in}$ and $v_o$ is about 180°. Similar to Fig. 13 (b), the voltage waveforms of capacitors $C_1$, $C_2$ and switches $T_2$, $T_{2P}$ in this scenario is shown in Fig. 16 (b), and the $v_{T2p}$ remains at zero level with the duty ratio $d_2$ equals 1. It can be also seen in Fig. 17, the voltage $v_B$ is presented in the form of power frequency (50Hz). Besides, as compared to Scenario I, as shown in Fig. 18, the voltage of switch $T_{1p}$ equals 0, and the separated inductors current $i_{L1}$, $i_{L3}$ only have two processes. In summary, the converter works well under Scenario II.

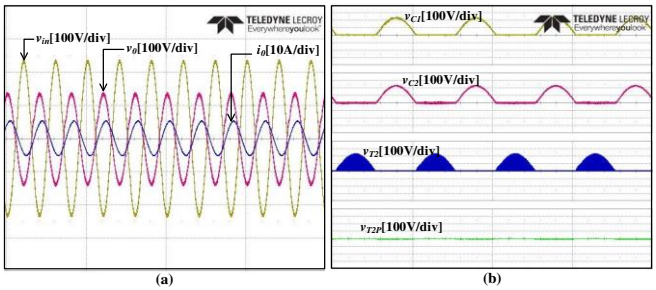



Fig. 16 Experimental waveforms of the DB-AC under Scenario II with *RL* load. (a) Waveforms of input voltage, output voltage, and output current with 50*ms*/div. (b) Voltage waveforms of capacitors ($C_1$, $C_2$), and switches ($T_2$, $T_{2P}$) with 20*ms*/div.

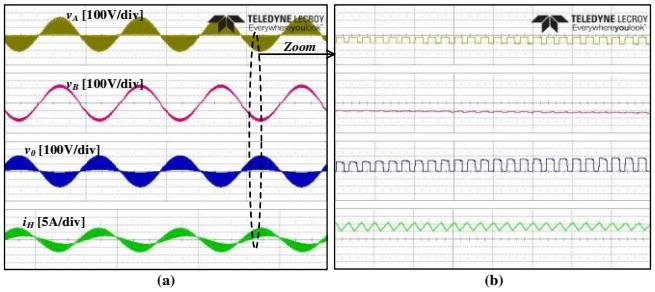



Fig. 17 High frequency voltages ($v_A$, $v_B$, $v_{AB}$) and filter inductor current waveforms (a) Time at 20*ms*. (b) Time at 200$\mu$*s*.

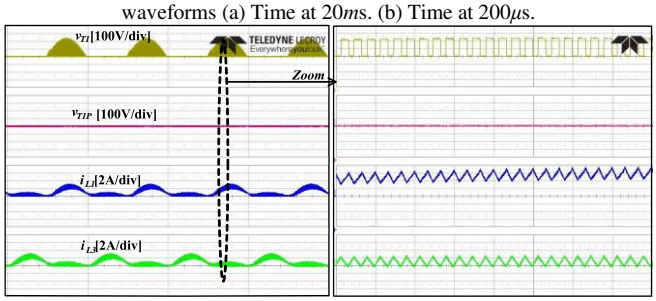



Fig. 18 Voltage waveforms of switches ($T_1$, $T_{1P}$), current waveforms of limiting inductors ($L_1$, $L_3$). (a) Time at 20*ms*/div (b) Time at 200$\mu$*s*/div.

**Scenario III**

Fig. 19 and Fig. 20 show the experimental waveforms of the DB-AC under Scenario III with non-liner load. In this scenario, a single-phase uncontrollable rectifier bridge with capacitor filter and a pure resistive load is chosen as the non-linear load, which results in a large distortion of the voltage and current on the input AC side, as shown in Fig. 19(a). In addition, because the duty ratio $d_2$ is equal to 0, the $v_{T2p}$ is half of the input voltage waveform shown in Fig. 19(b). And the converter high frequency output voltage ($v_{AB}$), the unfiltered current ($i_H$) and two separated inductors currents ($i_{L1}$, $i_{L3}$) are shown in Fig. 20.

Fig. 21 and 22 are the experimental results of DB-AC with 2.5μs dead-time and overlap time respectively. From the experimental waveforms, it can be seen that the DB-AC proposed in this paper does not have the problem of commutation and shoot-through, and can run stably and reliably in dead-time and overlap time.

Fig. 23(a) shows the efficiency curves under a fixed pure resistive load ($R$=20Ω) with different duty ratio $d_1$ and $d_2$,

however, the voltage gain ($M_C$) of the converter is all set as 0.7 under the three different scenarios. Fig. 23(b) shows the comparison between the measured value and the theoretical value with $d_1$=0.7, $d_2$=0. The theoretical value can be obtained by equation (20) and in order to simplify the calculation, we only analyze the power loss of the switches ($T_1$, $T_{1c}$, $T_{1p}$, $T_{1cp}$, $T_2$, $T_{2c}$, $T_{2p}$, $T_{2cp}$), body diodes ($D_2$, $D_{2c}$, $D_{2p}$, $D_{2cp}$), independent diodes ($D_1$, $D_{1c}$, $D_{1p}$, $D_{1cp}$) and inductors ($L_1$, $L_2$, $L_3$, $L_4$). The analysis process is obtained as follows:

$$\eta_{\mathrm{Th}}=\frac{P_{\mathrm{out}}}{P_{\mathrm{in}}}\times 100\%=\frac{P_{\mathrm{out}}}{P_{\mathrm{out}}+P_{\mathrm{loss}}}\times 100\% \tag{20}$$

Where $\eta_{\mathrm{Th}}$ is theoretical value of efficiency; $P_{\mathrm{in}}$, $P_{\mathrm{out}}$ and $P_{\mathrm{loss}}$ are the input power, output power and power loss of the converter within one power frequency cycle respectively.

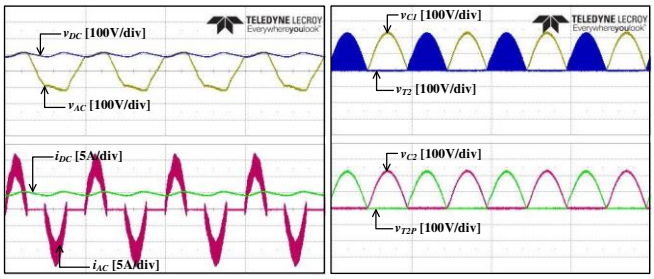



Fig. 19 Voltage waveforms of switches ($T_1$, $T_{1P}$), current waveforms of limiting inductors ($L_1$, $L_3$). (a) Time at 20$ms$/div (b) Time at 200$\mu s$/div.

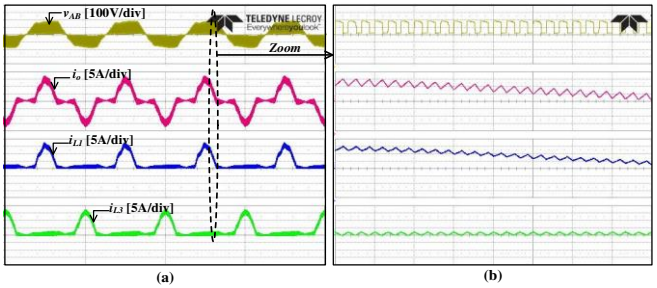



Fig. 20 Voltage waveforms of switches ($T_1$, $T_{1P}$), current waveforms of limiting inductors ($L_1$, $L_3$). (a) Time at 20$ms$/div (b) Time at 200$\mu s$/div.

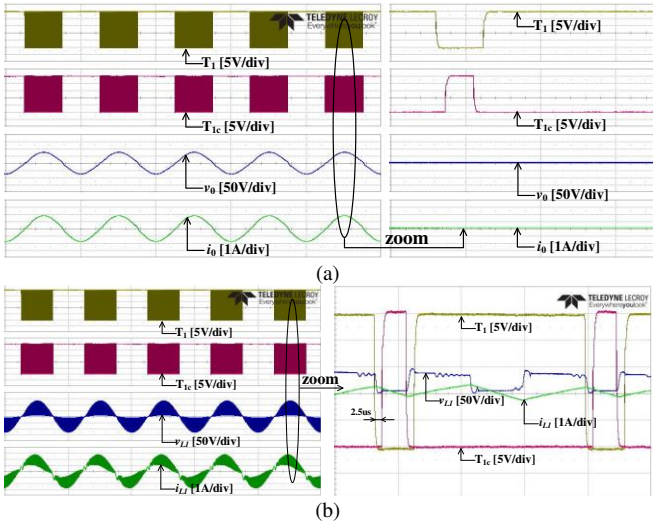



Fig. 21 The experimental results with 2.5 μs dead times: (a) the switch signals of $T_1$ and $T_{1c}$, the output voltage $v_0$ and the output current $i_0$; (b) the switch signals of $T_1$ and $T_{1c}$, the voltage of inductor $L_1$$v_{L1}$and the current of inductor $L_1$ $i_{L1}$

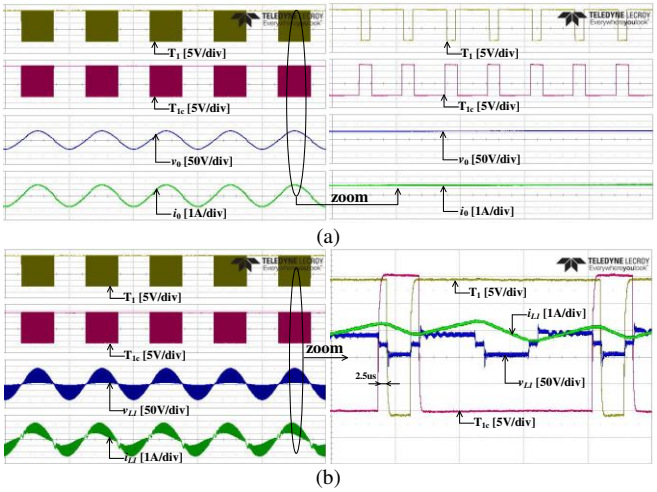



Fig. 22 The experimental results with 2.5 μs dead times: (a) the switch signals of $T_1$ and $T_{1c}$, the output voltage $v_0$ and the output current $i_0$; (b) the switch signals of $T_1$ and $T_{1c}$, the voltage of inductor $L_1$$v_{L1}$and the current of inductor $L_1$ $i_{L1}$

Then, the power loss can be calculated by (21):

$$\begin{aligned}P_{\mathrm{loss}} \approx\ & P_{\mathrm{IGBT\text{-}S}}+P_{\mathrm{IGBT\text{-}CON}}+P_{\mathrm{D\text{-}on}}\\ &+P_{\mathrm{D\text{-}off}}+P_{\mathrm{D,turn\text{-}on}}+P_{\mathrm{D,turn\text{-}off}}+P_{\mathrm{inductor}}\end{aligned} \tag{21}$$

Where $P_{\mathrm{IGBT\text{-}S}}$ and $P_{\mathrm{IGBT\text{-}CON}}$ are the IGBT turn-on, turn-off and conduction loss respectively; $P_{\mathrm{D\text{-}on}}$, $P_{\mathrm{D\text{-}off}}$, $P_{\mathrm{D,turn\text{-}on}}$, $P_{\mathrm{D,turn\text{-}off}}$ and $P_{\mathrm{inductor}}$ are diode on state loss, diode off state loss, diode turn-on loss, diode turn-off loss and inductor loss, respectively.

$$P_{IGBT-S}=0.02\frac{f_s}{2}(E_{\mathrm{on}}+E_{\mathrm{off}})\frac{I_{in}}{I_C}\frac{U_{in}}{U_{CC}}N \tag{22}$$

$$\begin{aligned}P_{\mathrm{IGBT\text{-}CON}}=0.01\Bigg[&\left(\frac{1}{4}d\cos\varphi V_{\mathrm{CE(sat)}}I_{in}+\frac{2d\cos\varphi}{3\pi}r_{\mathrm{CE}}I_{\mathrm{in}}^2\right)\\&+\left(\frac{1}{4}\cos\varphi V_{\mathrm{CE(sat)}}I_{in}+\frac{2\cos\varphi}{3\pi}r_{\mathrm{CE}}I_{\mathrm{in}}^2\right)\Bigg]N\end{aligned} \tag{23}$$

Where $E_{\mathrm{on}}$ is the turn-on loss; $E_{\mathrm{off}}$ is the turn-off loss; $f_s$ is the switching frequency; $V_{\mathrm{CE(sat)}}$ is saturation voltage drop; $I_{\mathrm{in}}$ is the current (A) when the IGBT is in the on state; $d$ is duty cycle; $N$ is the number of IGBT.

The power loss of the body diodes ($D_2$, $D_{2c}$, $D_{2p}$, $D_{2cp}$) are included. And the power loss of the independent diodes ($D_1$, $D_{1c}$, $D_{1p}$, $D_{1cp}$) are calculated as follows:

$$P_{D-on}\approx 0.01dV_FI_Fn \tag{24}$$

$$P_{D-off}\approx 0.01\left[(1-d)V_RI_R+V_RI_R\right]n \tag{25}$$

$$P_{D,turn-on}\approx 0.01\times 0.5V_{fp}I_{fp}t_{fp}f_sn \tag{26}$$

$$P_{D,turn-off}\approx 0.01\times 0.5V_{rp}I_{rp}t_bf_sn \tag{27}$$

Where $t_{\mathrm{fp}}$ and $t_{\mathrm{b}}$ are the turn-on and turn-off time of the independent diode respectively; $n$ is the number of the independent diode; $V$ and $I$ are the corresponding voltage and current.

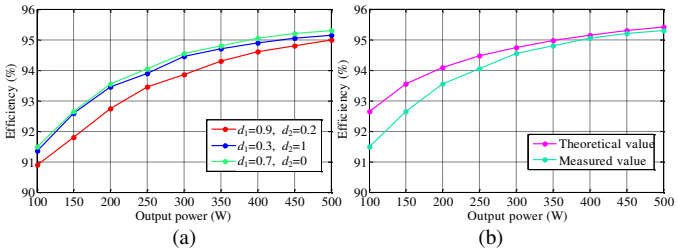



Fig. 23 Efficiency performance of DB-AC. (a) three scenarios. (b) comparison between the measured value and the theoretical value with $d_1$=0.7, $d_2$=0.

As can be seen from the figure, when the output power reaches 500W, the efficiency of the converter is over 95%. And the DB-AC will obtain higher efficiency in some cases with one duty cycle equals to 1 or 0. Because in the above two working conditions, the switching loss of the switches is smaller than other scenarios.

### B. *Application of Converter as DFVC*

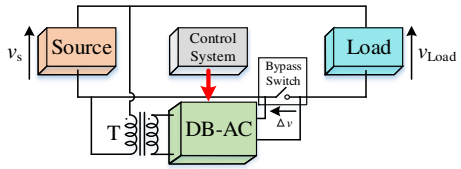



Fig. 24 The proposed DFVC.

From the above analysis, it can be seen that the DB-AC has the performance of output bipolar voltage. Therefore, as shown in Fig. 24, the DB-AC can be fully used as DFVC to address voltage swell and sag problems appeared in the power grid. And as the swell or sag of the power grid voltage appear, the bypass switch is turned off, the DB-AC operates in DFVC mode and provides compensation voltage for the system. Conversely, when the grid voltage is nominal voltage, the bypass switch is connected and the DFVC is in the bypass mode. As can be seen from Fig. 24, the relationship between the supply voltage $v_s$, load voltage $v_{Load}$ and the compensation voltage $\Delta v$ provided by DFVC is as follows.

$$v_R = v_S - v_{AC} \tag{28}$$

In order to verify the application of the proposed DB-AC as DFVC, two experiments were successfully implemented in the conditions of grid voltage swell and sag respectively, and the waveforms of experimental results are shown in Fig. 25 and Fig. 26. Due to the limitation of laboratory conditions, the standard voltage is set to 110Vrms. And that is to say, the load voltage $v_{Load}$ should be maintained at 110Vrms by DFVC.

Voltage sag: Fig. 25 shows the experimental waveforms of the DFVC under voltage sag condition, $v_S$=60Vrms<$v_{std}$=110 Vrms, and the grid voltage experiences approximately 45.45% voltage sag. At this point, the DFVC should be provided a 50V compensation voltage to maintain the load voltage $v_{Load}$ at 110Vrms, and the proposed DB-AC works in non-inverting operation with the $v_{AC}$ and $v_S$ are in-phase.

Voltage swell: Fig. 26 shows the experimental waveforms of the DFVC under voltage swell condition, $v_S$=160Vrms>$v_{std}$ =110Vrms, and the grid voltage experiences approximately 45.45% voltage swell. In order to adjust the load voltage $v_{Load}$ to the nominal voltage 110V, the DFVC should be provided a inverted 50V compensation voltage. As can be seen from the Fig .26, the supply voltage $v_s$ and compensation voltage $\Delta v$ are out-of-phase.

In order to prove more fully that the proposed converter can solve both voltage sag and swell problems. The waveforms of two dynamic experimental results are shown in Figs. 27 and 28. The experimental results show that the proposed converter can solve the voltage fluctuation problem well when it is used as DFVC. In addition, in order to prove the ability of the DB-AC to output bipolar voltage, the experimental results of DB-AC with transition from inverting to non-inverting operation shown in Fig. 29 is given.

In summary, when voltage swell or sag occur in the grid, the DFVC based on the proposed DB-AC works well, and it can provide a bipolar voltage.

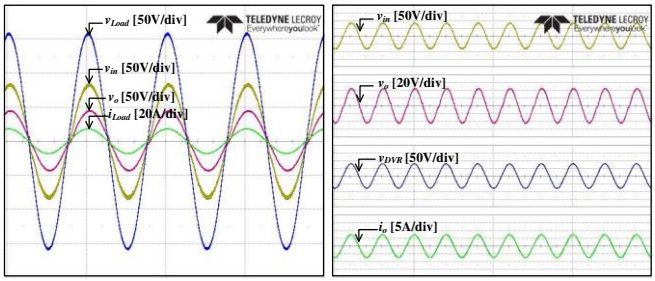



Fig. 25 Experimental waveforms of the DB-AC used as DFVC ($v_S$ is grid voltage, $U_R$ represents load voltage, $v_{AC}$ is the output voltage of the DB-AC).

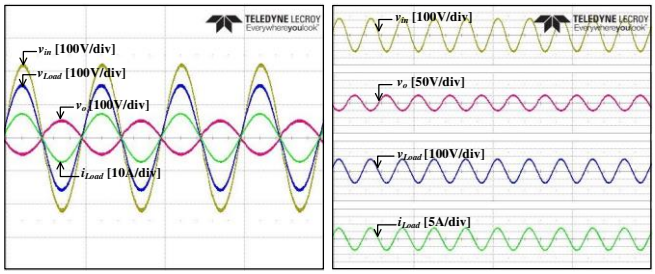



Fig. 26 Experimental waveforms of the DB-AC used as DFVC ($v_S$ is grid voltage, $v_R$ represents load voltage, $v_{AC}$ is the output voltage of the DB-AC).

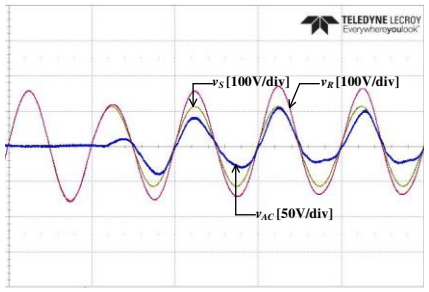



Fig. 27 Dynamic results for voltage sag mitigation ($v_S$ is grid voltage, $v_R$ represents load voltage, $v_{AC}$ is the output voltage of the DB-AC).

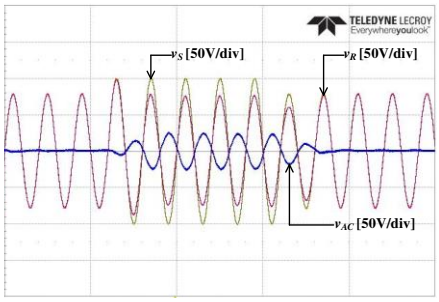



Fig. 28 Dynamic results for voltage swell mitigation ($v_S$ is grid voltage, $v_R$ represents load voltage, $v_{AC}$ is the output voltage of the DB-AC).

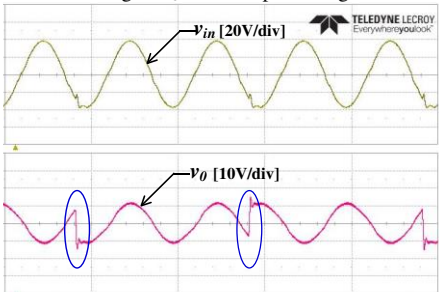



Fig. 29 The experimental results of DB-AC with transition from inverting to non-inverting operation.

## VI. Conclusion

In this paper, a novel bipolar-type ac-ac converter topology based on dual-buck PWM ac choppers is proposed. It can obtain bipolar output voltage gain, that is, an in-phase or out-of-phase output voltage with the input voltage can be obtained. Therefore, it has capability to compensate both voltage sag and swell when used in a DFVC. Especially, an advantage is that the proposed ac-ac converter has the same buck/boost operation process for non-inverting and inverting modes, which ensures the continuously average current supply to the low-voltage output side without a high-value capacitor to support power. Additionally, due to the common sharing ground of the input and output, the feature that output can reverse or maintain phase angle with input is supported well. By adopting two-level non-differential dual-buck ac chopper legs with two separation inductors, the proposed converter overcomes the commutation problem and improves the utilization of the duty cycles due to there is no dead-time. Partial free-wheeling diodes can be chosen independently with fast reverse recovery features to minimize switching loss. Finally, a detailed analysis of the proposed converter and DFVC has been presented and validated by experiment.

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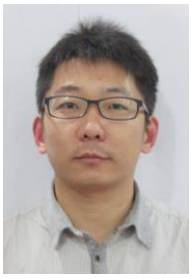

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