Gate Bias Incorporation into Cardiff Behavioural Modelling Formulation

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***Abstract*—This paper presents a novel approach to incorporate gate bias voltage variations into the Cardiff behavioural model formulation. In particular, it is observed that the model coefficients can be expressed effectively as a linear function of bias voltage. As a result, the intensity of the load-pull measurement can decrease up to 80 % as the interpolation of the data with respect to the gate bias voltage can be exploited. The experiment was done on a 4 W GaN technology on-wafer device and the result is verified on 0.2 W GaAs technology device.**

***Keywords*—Load-pull, Behavioural model, Power amplifiers**

I. Introduction

To meet the requirements of modern communication standards with high peak to average power ratio (PAPR) and increasing bandwidth, more complex power amplifier (PA) structures are required (e.g. Doherty, envelope tracking and out phasing). Due to trade-offs between different design parameters (e.g. efficiency and linearity) the design of complex PA structures necessitates multidimensional characterisation data [1], [2]. A designer might need to vary several variables at the same time to be able to analyse the nonlinear behaviour of the active device and find the best compromise to meet all the design specifications. Therefore, to collect all the data for the design process, intensive and time-consuming measurements are inevitable.

One of the key motives behind the development of the nonlinear behavioural model has always been a reduction in the measurement and simulation time [3]. In fact, an accurate and reliable nonlinear behavioural model is an enabler for interpolation of the data; hence, it reduces the required intensity of the measurement data. Keysights's X-parameters [4] and Cardiff University's Cardiff behavioural model [3] are two behavioural models widely accepted by the industry. In terms of mathematical formulation, each of these models has a different approach to model the nonlinear behaviour of the transistor device. X-parameters is based on the superposition principle [5] whereas the Cardiff model is based on mixing theory without assuming harmonic superposition [6].

In the current formulation of both X-parameters and Cardiff model, the drain voltage (V_{ds}) and gate voltage (V_{gs}) are treated as independent variables [6],[7] ; hence, load-pull measurement at each V_{ds} and V_{gs} point is required to generate a bias-dependent model. The work presented in this paper includes a study aimed at incorporating V_{gs} into the Cardiff model formulation, which enables interpolation of the data with respect to V_{gs}; thus, can reduce measurement time.

Section II describes the measurement system used for this experiment. In section III, the incorporation of V_{gs} in the Cardiff model is discussed along with a brief overview of the Cardiff model's formulation. Finally, model verification is covered in section IV.

II. Measurement Strategy

For this experiment, an open-loop active load-pull measurement is used. Fig. 1 shows the schematic block diagram of the measurement system.

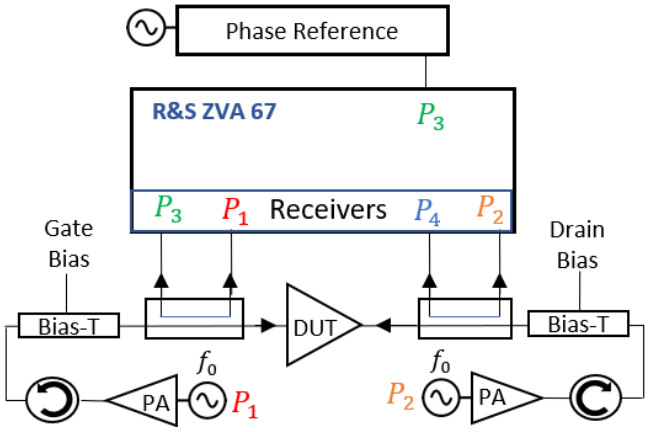


Fig. 1. Block diagram of the open-loop active load-pull measurement setup used for this experiment.

The measurements were conducted on a probe station with a fundamental frequency of 3.5 GHz and in a class AB bias environment. The measurements were conducted statically using continuous wave (CW) excitation. Load-pull is conducted only at the fundamental, with harmonic frequencies terminated at the system impedance (50 Ω). The drain voltage was fixed at 50 V while the gate voltage was swept from -2 to -3 V with 0.1 V step. The input drive (P_{av}) was swept from 17 to 26 dBm. Unless specified otherwise, the experiment is based on the measurement results of a 4 W GaN-on-SiC device.

III. Incorporating the Gate Bias Voltage Into the Cardiff Model's Formulation

A. *A theoretical overview of the Cardiff behavioural model*

The Cardiff model is a polynomial based mathematic formulation in the A, B waves domain. The model is capable of

mathematically relating the response of the transistor ($B_{p,h}$) to the stimulus signal ($A_{p,h}$) through a set of coefficients ($L_{p,h,r,n}$). Equation (1) shows the mathematical formulation of the Cardiff model for fundamental load-pull measurements [6]. The 'p' and 'h' subscripts denote the respective port and harmonics, and 'm' and 'n' denote the coefficient related power wave's magnitude and phase exponent respectively

$$B_{p,h} = Q_{1,1}^{h} \sum_{r=0}^{r=\frac{w-h}{2}} \cdot \sum_{n=-(\frac{w-h}{2}-r)}^{n=h+(\frac{w-h}{2}-r)} L_{p,h,m,n}(A_{1,1})|A_{2,1}|^{m}\left(\frac{Q_{2,1}}{Q_{1,1}}\right)^{n} \quad (1)$$

The parameter 'w' represents the model order which determines the complexity and number of the model coefficients. Depending on the application, the model order can be varied to meet the model accuracy requirement. Work in [8] investigates the complexity requirement of the model, and it suggests a model order of 5 or 7 is good to model fundamental load-pull data. For this experiment, a model order of 5 with 10 coefficients was selected.

In general, the task of the model generation is to extract several model coefficients ($L_{p,h,m,n}$) for each port and harmonics, which are indexed to different independent variables. These variables can be frequency, the magnitude of the input incident wave |A11|, drain and gate bias level. These coefficients are imported into a computer-aided design (CAD) software for simulation and data analysis purposes.

Therefore, to include the bias voltage sweep in the current Cardiff model's formulation, load-pull measurement at each bias point is required.

B. *Including gate bias voltage sweep in the Cardiff model*

Fig. 2 shows (a) the real, and (b) imaginary part of the model coefficients ($L_{m,n}$) for $B_{2,1}$wave with respect to the changes in the gate bias. As in this paper only the coefficients for $B_{2,1}$ were considered, to avoid the complexity of the coefficient's subscripts only the corresponding 'm' and 'n' subscripts will be used. For example, the coefficient $'L_{2,1,m,n}'$ will be shown as $'L_{m,n}'$.

As it is shown in Fig. 2, both real and imaginary parts of the model coefficients show a behaviour that can be approximated reasonably well with a linear function with respect to gate bias voltage. Therefore, a new set of model coefficients can be generated using a Least Mean Squares (LMS) algorithm [6], illustrated in eqs. (2) and (3).

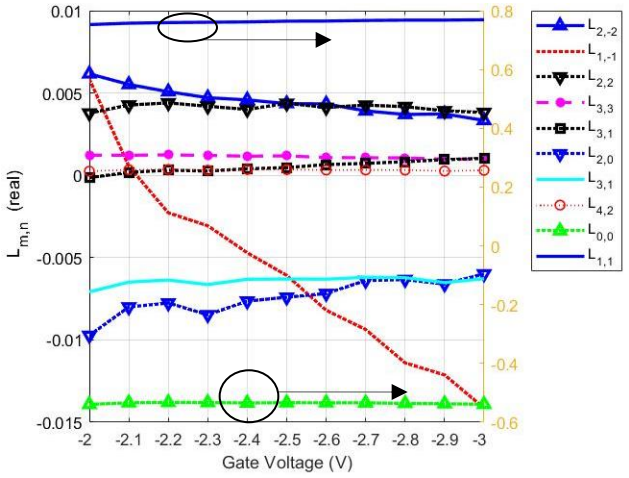
$$[V_{gs}] = \begin{bmatrix} {V_{gs,1}}^{0} & {V_{gs,1}}^{1} \\ {V_{gs,2}}^{0} & {V_{gs,2}}^{1} \\ {V_{gs,3}}^{0} & {V_{gs,3}}^{1} \\ \vdots & \vdots \\ {V_{gs,N}}^{0} & {V_{gs,N}}^{1} \end{bmatrix} \quad (2)$$

$$[K_{m,n}] = \left([V_{gs}]^{H}.[V_{gs}]\right)^{-1}[V_{gs}]^{H}[L_{m,n}] \quad (4)$$

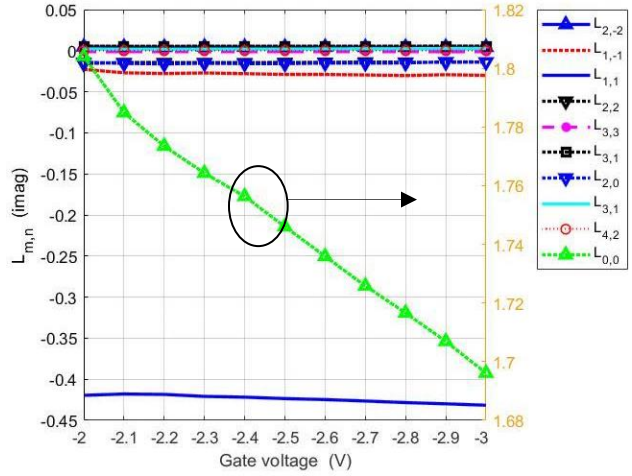
In equation (4), $[K_{m,n}]$ represents the new model coefficient set that incorporates V_{gs}. Therefore, the model's formulation can be updated as it is shown in (4).

$$B_{p,h} = Q_{1,1}^{h} \sum_{r=0}^{r=\frac{w-h}{2}} \cdot \sum_{n=-(\frac{w-h}{2}-r)}^{n=h+(\frac{w-h}{2}-r)} \left(\sum_{s=0}^{1} K_{p,h,m,n}(A_{1,1}).{V_{gs}}^{s}\right).|A_{2,1}|^{m}\left(\frac{Q_{2,1}}{Q_{1,1}}\right)^{n} \quad (4)$$

With reference to (4) the V_{gs} is no longer an independent variable; hence, it enables the interpolation of the data with respect to the gate bias voltage.



(a)



(b)

Fig. 2. (a) real, (b) imaginary part of the model coefficients ($L_{m,n}$) vs gate voltage (V_{gs}). Drive level (P_{av}) was selected at 17 dBm.

IV. MODEL VERIFICATION

Fig.3 shows the comparison between the measured and modelled data for load reflection coefficients ($\Gamma_L = \frac{A_{2,1}}{B_{2,1}}$) at -2.8 V gate bias and 17 dBm drive level. The modelled data is generated from the new model's coefficients ($K_{m,n}$).

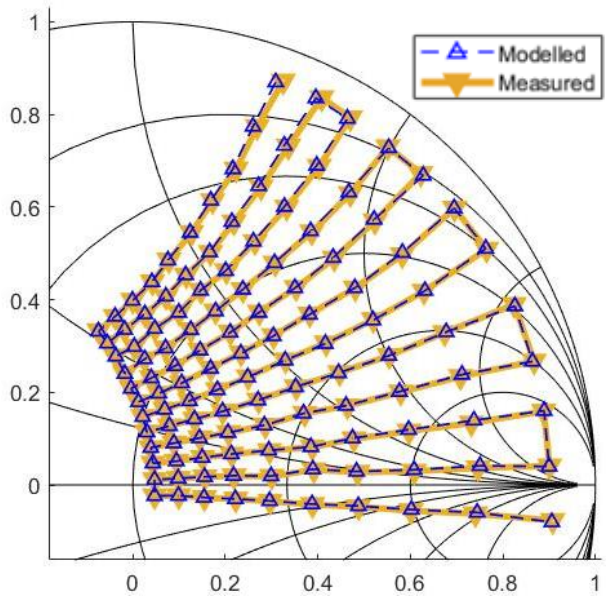


Fig. 3. Comparison of measured and modelled load reflection coefficients (Γ_L) at $V_{gs} = -2.8\,V$ and P_{av}= 17 dBm. The modelled data is generated from the new model's coefficients ($K_{m,n}$), which incorporate the gate bias voltage.

With reference to Fig. 3, there is a very good match between the modelled and measured data at a particular gate bias and input drive level point.

To investigate the accuracy of the model and validate it over all the measurement data, the normalised mean squared error (NMSE) is used. The definition of NMSE is illustrated in (5) [9].

$$NMSE = \frac{\sum_i |{B_{21}}^{meas} - {B_{21}}^{model}|^2}{\sum_i |{B_{21}}^{meas}|^2} \quad (5)$$

Fig.4 shows the calculated NMSE (dB) value at different V_{gs} and input drive (P_{av}) levels. Each data point on the graph represents the deviation of the model from the measured $B_{2,1}$ wave at a specific gate bias and input drive level.

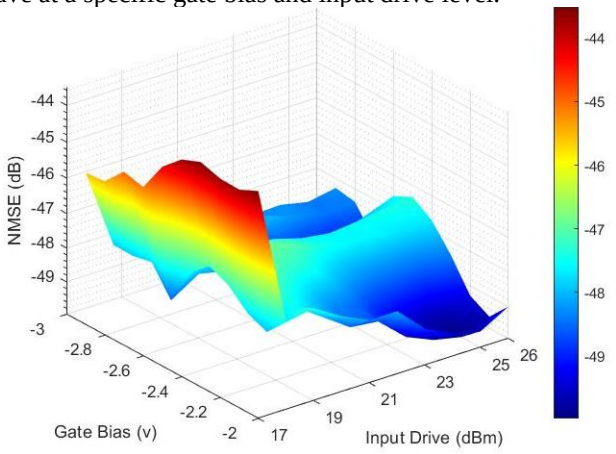
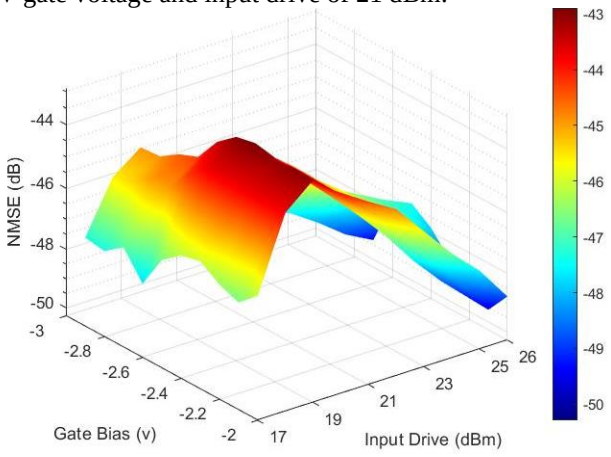


Fig.4. The calculated NMSE (dB) value for different gate bias and input drive levels.

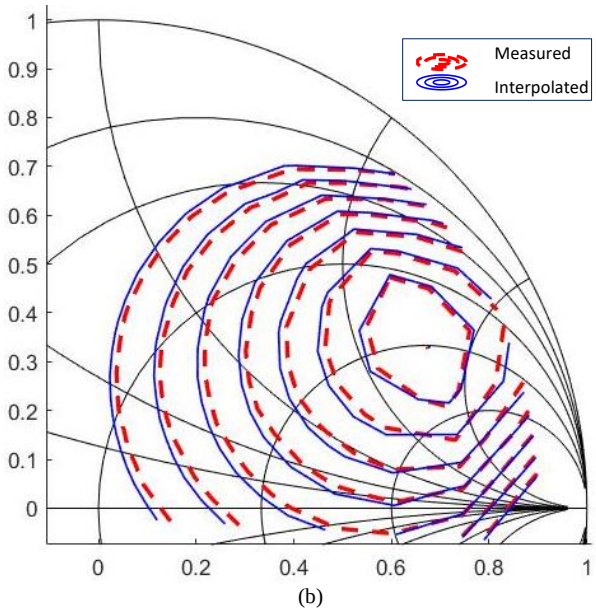
As it is shown in Fig.4, the calculated NMSE value is less than -45 dB (i.e. less than 0.5%) at all data points. This validates that the model is able to predict the measurement data over different gate bias and input drive levels.

A. *Interpolation ability*

To examine the interpolation of the load-pull data with respect to the gate voltage, measurement data at only two gate bias point at -2.0 V and -3.0 V (endpoints) were used to generate the model. Fig.5 shows (a) the deviation of the interpolated and measured $B_{2,1}$ wave at different V_{gs} and input drive (P_{av}) levels in terms of NMSE (dB) value, and (b) compares the measured and interpolated efficiency contours at -2.5 V gate voltage and input drive of 21 dBm.



(a)



(b)

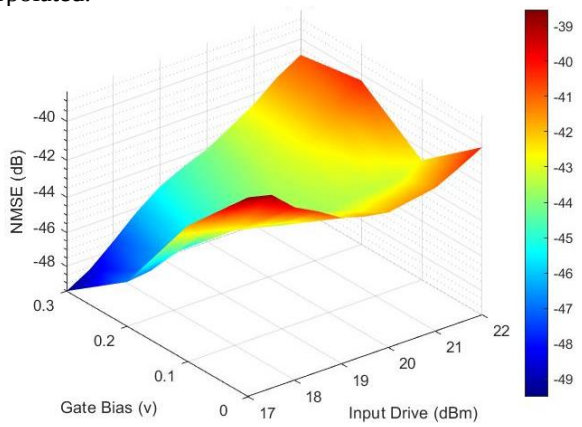
Fig. 5. Comparison of measured and interpolated data. (a) Calculated NMSE (dB) $B_{2,1}$, and (b) measured and interpolated efficiency contours with the step of 0.75 dB and maximum efficiency of 47%. The corresponding gate bias level and input drive level are -2.5 V and 21 dBm respectively. The NMSE value for plotted efficiency contours is -37.5 dB (less than 1.3 % deviation).

With reference to Fig.5, the new set of Cardiff model's coefficients are capable to interpolate the load-pull data with very high accuracy (NMSE value of less the -44 dB at all data points). In this analysis, 11 points of bias have been reduced to 2 and the model accurately predicts the data. This demonstrates an 80% reduction of necessary measurements for this bias range.

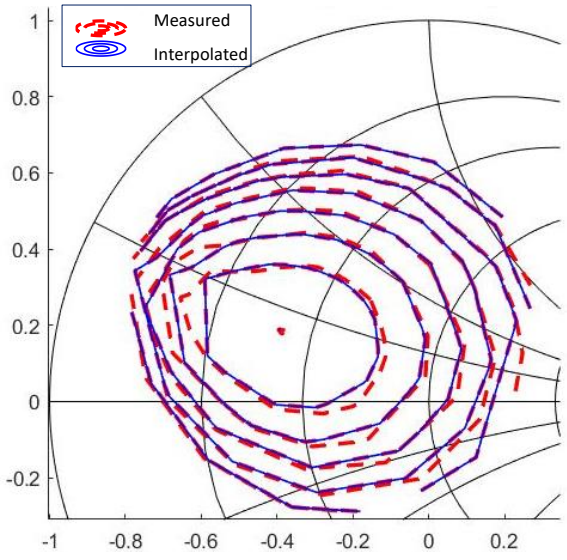
B. *Validation and generalisation of the new model coefficients on a GaAs transistor device*

For further validation and generalisation of the discussed phenomena, the same approach was applied on a 0.1 µm gate length E-mode technology from Win Semiconductor (PIH1-10) GaAs transistor device. The measurement of the GaAs device was done at 28 GHz with gate bias being swept from 0 V to +0.3 V with steps of 0.1 V in class C and B bias environment (pinch-off voltage was 0.3 V). The drain bias was fixed at 4 V.

Fig. 6 shows (a) the calculated NMSE (dB) values over different V_{gs} and input drive sweep comparing measured and interpolated data for $B_{2,1}$ wave (b) output power contours at gate voltage of +0.2 V and drive level of 19 dBm. For model generation, only data at 0 V and +0.3 V gate bias levels (endpoints) were used and data at middle points were interpolated.



(a)



(b)

Fig.6. Comparison of measured and interpolated data of the GaAs device. (a) Calculated NMSE (dB) $B_{2,1}$, and (b) measured and interpolated power contours (at $V_{gs} = +0.2$ and drive level of 19 dBm) with step of 0.5 dB and maximum output power of 22 dBm. The NMSE value for plotted power contours is -45 dB (less than 0.5 % deviation).

With reference to Fig. 6, there is a very good match between the measured and interpolated data, where the NMSE value is less than -40 dB (1%) at all data points. In general, model accuracy of -40 dB will produce power contours with ±0.1 dB accuracy.

V. Conclusion

The work presented in this paper validates that the gate voltage can be included in the Cardiff model's coefficients, which results in up to 80% reduction in the intensity of the load-pull measurement with respect to gate bias. The model's coefficients have a relatively linear relationship with respect to changes to the gate bias; hence, by only using the load-pull measurement data at the endpoints, model's coefficients can be generated with the ability to predict the load-pull data at all the middle points.

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