Continuous Operation of LVDC Source/Load Under DC faults in MMC-DC Distribution Systems

Bin Li, Hui Lv, Weijie Wen*, Haijin Liu, Ziwei Zhang, Gen Li and Botong Li

***Abstract*—With penetration and usage of renewable sources and loads based on power electronics increasing, the modular multi-level converter based direct current (MMC-DC) distribution system is getting broad attention. In MMC-DC system, DC/DC converters are employed to link the low voltage DC (LVDC) source/load and the medium-voltage DC (MVDC) distribution system. DC fault ride through capability at MVDC side is one of the technical difficulties, and has been the focus of previous studies. However, whether LVDC source/load could operate continuously under MVDC faults is still an open question. In this paper, key facilities, protection procedures and operating characteristics of LVDC source/load in two typical MMC-DC frameworks based on half bridge submodules (HB-MMC-DC) and full bridge submodules (FB-MMC-DC) are studied respectively. Analyses show LVDC source/load could operate continuously in HB-MMC-DC system with the help of DCCBs, but with voltage variation exceeding acceptable range, they fail to operate continuously in FB-MMC-DC systems. Therefore, a controllable storage unit is deployed at the LVDC side of the DC/DC converters to suppress voltage variation. The working principle and parameter design of the proposed solution are presented. Case studies are carried out in PSCAD/EMTDC for verification. Finally, comprehensive comparisons between the two MMC-DC systems are conducted.**

***Index Terms*—modular multi-level converter, fault current elimination, load voltage source and load, continuous operating.**

I. Introduction

Comparing with alternating current (AC) distribution systems, modular multilevel converter (MMC) based direct current (MMC-DC) distribution systems have remarkable features of enabling high penetration of renewable sources (photovoltaic unit and wind turbine) and energy storage elements, reducing power conversion stages and decreasing power losses [1]-[6]. Therefore, it has attracted considerably more attention [7],[8].

Typical MMC-DC distribution systems are illustrated in Fig. 1. The AC/DC and DC/DC converters are the interfaces with AC systems and DC sources/loads. Converters connect through medium-voltage DC (MVDC) distribution lines. As the low voltage DC (LVDC) loads and distributed renewable sources may not be directly connected into MVDC systems due to their low interface voltages [9],[10], DC/DC converters are deployed. One showcase of the MMC-DC distribution network is the Tangjia Bay project commissioned in China in 2018, wherein MMCs and DC/DC converters are employed [11].

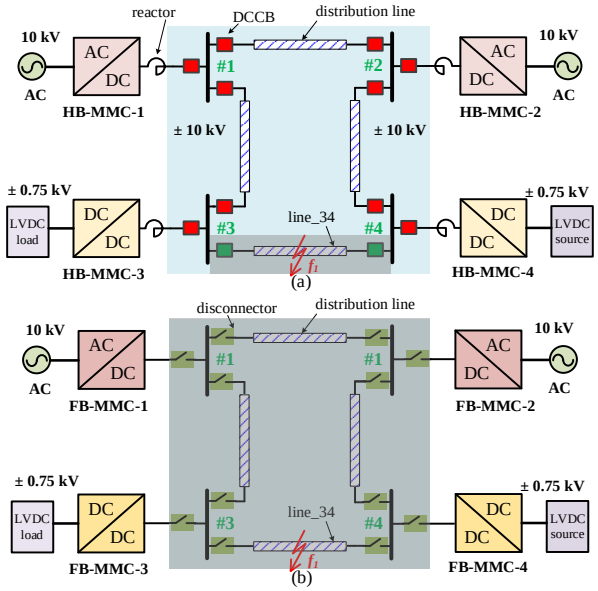

Fig. 1. Typical MMC-DC distribution system schemes. (a) HB-MMC-DC distribution system with DCCBs; (b) FB-MMC-DC distribution system with dis-connectors.

Due to the rapid increasing rate and the lack of current zero-crossing points, a fast and reliable DC fault current interruption is of great difficulty [12]-[14]. Therefore, the DC network protection is one of the bottlenecks limiting the wide applications of DC technologies and thus receives significant attention in the literature. According to fault current interruption measures proposed by scholars from all over the world, there are two typical system frameworks: half bridge submodules (HBSM) based MMC-DC (HB-MMC-DC) system with direct current circuit breakers (DCCBs) [14]-[18] and full bridge submodules (FBSM) based MMC-DC (FB-MMC-DC) system with dis-connectors[19]-[21], as respectively shown in Figs. 1(a) and (b).

In the system shown in Fig. 1(a), all HB-MMCs may feed fault currents to the fault point once a DC fault (f_1) occurs [22],

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and relative DCCBs are triggered to eliminate the fault current through faulty line and isolate the fault point. As a result, blackout only occurs to the faulty line.

In the system shown in Fig.1(b), all converters are based on submodules (SM) capable of outputting bi-directional voltage, represented typically by FBSMs. When short-circuit fault (f_1) occurs, by adjusting control strategy of FB-MMCs to start fault current elimination mode, fault current fed by converter itself could be eliminated. With all converters in power system starting fault current elimination mode to force fault current through faulty line to zero, faulty line could be isolated easily by dis-connectors without arc quenching ability. As a result, blackout occurs to whole system at MVDC side until relative dis-connectors are open and converters recover to normal state.

In fact, during the fault elimination period of the above-mentioned MMC-DC system, many studies focus on the power quality and stable operation at MVDC side as well. In [23], the impact on bus voltage quality of distribution network is studied under different faults occurred at DC and AC side. In [24], the possible application of the series and shunt DC electric springs for fault-ride-through support are explored. Moreover, super-capacitors damping effect on the voltage dips caused by the short circuit faults is analyzed in [25]. [26] discussed how the fault current limiters improve power quality by reducing a voltage dips effect.

In general, previous studies focused on fault current interruption of DCCBs in Fig. 1(a), fault current elimination of a single converter in Fig. 2(b) and power quality improvement at MVDC side during the fault elimination period. Despite such valuable contributions to the DC network, the operating characteristics and continuous operation of LVDC source/load under MVDC faults are still under-researched.

To bridge the above research gaps, in this paper, the continuous operation capability of LVDC source/load in HB-MMC-DC systems with DCCBs (Framework 1) and FB-MMC-DC systems with dis-connectors (Framework 2) is discussed. The mechanism of voltage variation at the LVDC side of the DC/DC converter is revealed. To tackle the problem of non-continuous operation of LVDC source/load in Framework 2, a controllable storage unit deployed at the LVDC side of DC/DC converters is proposed. Operating principle and parameter design of the proposed solution are presented. The analysis and the proposed approach are verified in the two MMC-DC systems through simulations conducted in PSCAD/EMTDC. A good system performance of the continuous operation of LVDC source/load under MVDC faults can be ensured in the two systems.

II. Operating Characteristics of LVDC Source/Load in HB-MMC DC Systems with DCCBs

A. Operating characteristics of key facilities

For the HB-MMC-DC system shown in Fig.1(a), the key facilities of the HBSM based AC/DC and DC/DC converters, DCCBs, and current limiting reactors are illustrated in Fig. 2. Their operating characteristics are presented in this section for studying the behavior of the LVDC source/load under MVDC faults.

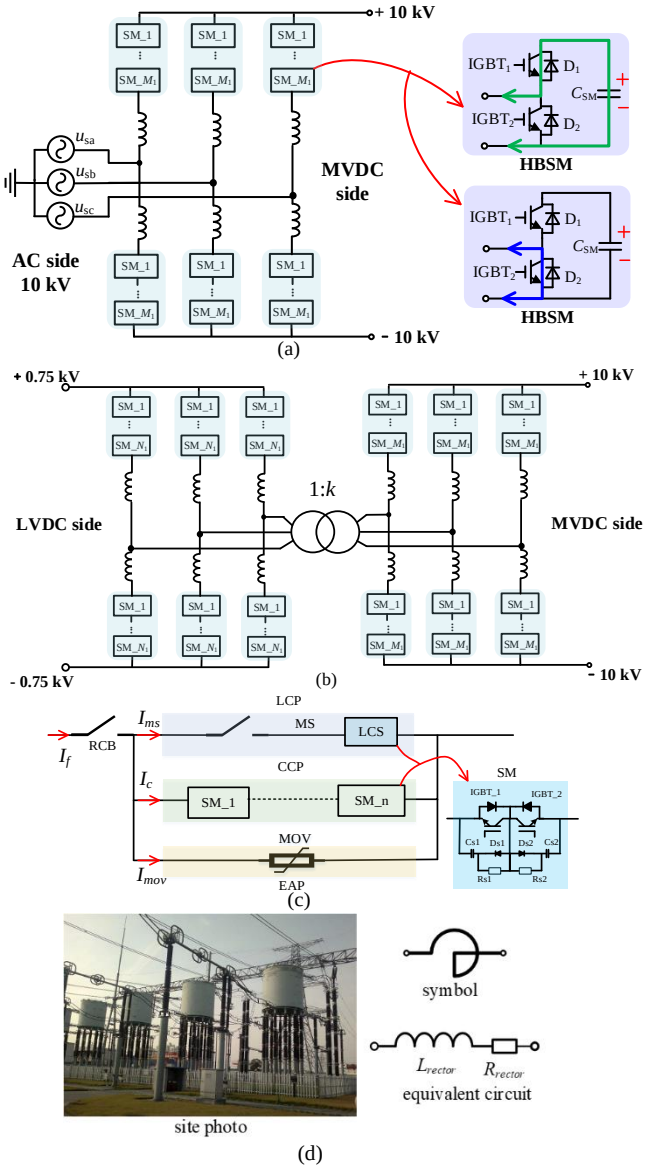

Fig. 2. Key equipment in the HB-MMC-DC framework. (a) AC/DC converter based on HBSM; (b) DC/DC converter based on HBSM; (c) Hybrid DCCB; (d) Current limiting reactor.

(1) AC/DC and DC/DC converters based on HBSMs

In Fig. 2(a), the AC/DC converter consists of six arms wherein each arm is made of M_1 series-connected HBSMs. The DC/DC converter shown in Fig. 2(b) can be regarded as two AC/DC converters connected by a transformer with a ratio of (1: k). The number of HBSM in each arm is M_1 for the MVDC side and N_1 for the LVDC side. Generally, N_1 is much smaller than M_1 due to the lower DC voltage in the LVDC side.

During normal states, from the view of the MVDC side, both AC-DC converter and DC-DC converter could be regarded as a controllable voltage source supported by equivalent capacitor (C_{dc}=6C_{SM}/M_1). The capacitor will discharge if a DC fault occurs at MVDC side, which may contribute to the rapid increase of the fault current. Due to the freewheeling effect of diodes (D_2) in HBSMs, fault currents from the AC system will feed to fault point continuously if the converter is blocked by

its own overcurrent protection [22].

In this case, DCCBs are essential to interrupt fault current and isolate the faulty line. Moreover, to avoid the block of converters triggered by its own overcurrent protection and ensure the fault current to be within the interruption capability of DCCB, current limiting reactors are essential to suppress the rate-of-rise of the fault current.

(2) Hybrid DCCBs

Different from AC system, basic reason for the lack of zero-crossing points of fault current in DC system is that equivalent power source in MVDC system is not alternating, and regular mechanical switches cannot output arc voltage comparable with system voltage. The main function of DCCB is to insert transient interruption voltage (TIV) into power system. With TIV larger than the output voltage of equivalent power source, fault current is forced to zero and is interrupted finally. Up to now, many topologies have been proposed for DCCBs[14]-[18]. In this paper, taking typical hybrid DCCB illustrated in Fig.2(c) as an example, its structure and working principle are introduced as follows:

A typical hybrid DCCB consists of the residual current circuit breaker (RCB), load current path (LCP), current commutation path (CCP) and energy absorption path (EAP). LCP is made of a mechanical switch (MS) and a load current switch (LCS). LCS and CCP are made of modularly designed SMs with anti-series connected insulated gate bipolar transistors (IGBTs). For a voltage level of 10 kV, one SM is enough for LCS [28]. EAP is made of the metal oxide varistor (MOV). RCB and MS are actually ultra-fast mechanical switches, just like AC circuit breaker.

DC current flows through the RCB and LCP under normal conditions, which results in low power losses (several kilowatts). When DCCBs are triggered due to a DC fault, along with multiple current commutations (LCP→CCP→EAP), the fault current will be finally forced into the EAP in which a TIV will be created and inserted into the DC circuit. Thanks to the TIV established by the DCCB, the residual fault current will be fully dissipated [29]. When analyzing operating characteristics of LVDC source/load under DC faults, the DCCB can be regarded as a controllable "black-box" with variable impedance. The TIV generated by this "black-box" will buy some time for the protection system and will be analyzed in the following sections.

(3) Current limiting reactor

Current limiting reactors are installed at the DC outlets of converters to suppress the discharging of C_{dc} and limit the rate-of-rise of fault current [27]. As shown in Fig. 2(d), the reactor can be modelled as an inductor ($L_{reactor}$) in series with a resistor (R_{eactor}). In existing studies, $R_{reactor}$ is neglected. However, according to the pilot project of a 10 kV DC distribution power system in Suzhou, China, $L_{reactor}$ is 10 mH, and $R_{reactor}$ is inevitable (≈ 94.5mΩ) [30]. The negative effects are: $R_{reactor}$ generates long-term operating losses during normal state; $L_{reactor}$ slows down the response speed of DC power system when regulating power flow.

B. Procedures of DC fault protection

DC fault protection procedures of Framework 1 is illustrated in Fig. 3. In case of an MVDC fault, the relay protection will firstly react based on its local measurement. The time for this fault detection is $\triangle t_1 \approx 1$ ms [31]. Then, the local relay will communicate with the remote relay units to select the faulty line, such as the current differential protection in which $\triangle t_2 \approx 2$ ms is needed [32].

The triggered DCCBs may take $\triangle t_3 \approx 2$ ms to establish the TIV [33]. $\triangle t_3$ is mainly decided by the operating speed of MS in DCCBs. Once the TIV is established, the fault current, also named as residual current, might be AC with a small amplitude or DC with an amplitude smaller than the chopping current of RCB. $\triangle t_4$ indicates the time for the residual current to have zero-crossing points [29], which is the time of dissipating the residual energy. $\triangle t_4$ is decided by multiple factors, like the fault location, fault type, fault impedance and the TIV established by the DCCB.

The faulty line will be isolated once the residual current interrupted by the RCB. Then, $\triangle t_5$ is needed for the post-fault restoration.

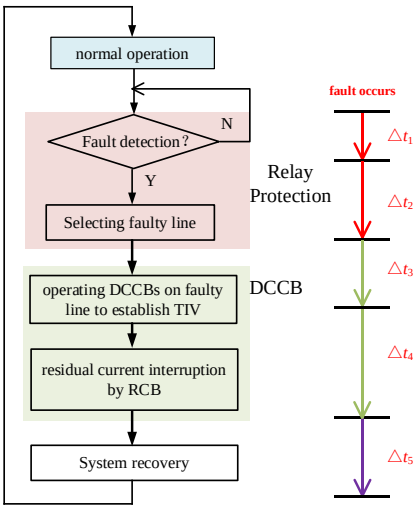

Fig. 3. Procedures of DC fault protection in HB-MMC-DC distribution systems with DCCBs.

C. Operating characteristics of LVDC source/load under DC faults

Equivalent circuit and power flow of the DC/DC converter based on HBSM during different states are illustrated in Fig. 4. The LVDC (AC/DC-1) and MVDC (AC/DC-2) converters are linked by a transformer. Voltage quality is one of the criteria for the assessment of power quality, and the voltage quality at the LVDC side (U_{dc1}) determines the operating capability of the LVDC source/load under normal and abnormal circumstances. Therefore, the following section will discuss whether the LVDC source/load can operate continuously by analyzing the voltage variation ratio under MVDC faults.

AC/DC-1 can be considered as an "energy tank" composed of an equivalent capacitor with a capacitance of $C_{dc1}=6C_{SM}/N_1$. Taking the power flow from LVDC side to MVDC side as an example, during normal states, as shown in Fig. 4(a), P_{in_1} and P_{out_1} are equal, and U_{dc1} is stable. According to the abovementioned DC protection procedures, the TIV has not been established in the initial stages ($\triangle t_1+\triangle t_2+\triangle t_3 \approx 5$ ms) of the DC fault and the control of the converter remains the same. During this period, the equivalent capacitor of AC/DC-2

(C_{dc2}=6C_{SM}/M_1) is discharging. The arm voltages (u_{ap_2}, u_{bp_2}, u_{cp_2}, u_{an_2}, u_{bn_2}, u_{cn_2}) are still regulated as balanced but with a voltage drop due to the discharge of the capacitor. As a result, the voltage u_2 at the AC side of AC/DC-2 and P_{out_1} decrease as well, but within tolerable margins. However, the dynamic balance between P_{in_1} and P_{out_1} is disturbed. Considering the imbalance power stored in all capacitors in AC/DC-1, the variation of U_{dc1} can be expressed in (1), (2) and (3).

$$6 \cdot N_1 \cdot C_{SM} \cdot dU_{SM} \cdot (U_{SM} + \frac{1}{2} dU_{SM}) = \int (P_{in\_1} - P_{out\_1}) \cdot dt \quad (1)$$

$$C_{dc1} \cdot dU_{dc1} \cdot (U_{dc1} + \frac{1}{2} dU_{dc1}) = \int (P_{in\_1} - P_{out\_1}) \cdot dt \quad (2)$$

$$\varepsilon = \frac{dU_{dc1}}{U_{dc1}} \quad (3)$$

The discharging of C_{dc2} will stop when the TIV is established (~5 ms after the fault). Along with the recovery of u_2 and P_{out_1}, P_{in_1} and P_{out_1} will reach balance again, and U_{dc1} will recover as well.

In fact, during the initial stage when AC/DC-2 is not blocked, u_2 and P_{out_1} only drop a little. The imbalance between P_{in_1} and P_{out_1} during this period ($dt \approx 5$ ms) is not large enough to make the voltage variation ratio ε (= dU_{dc1}/U_{dc1}) exceed the acceptable range (± 10 %). Therefore, the LVDC voltage quality can meet the system requirement under MVDC faults, the source/load is able to operate continuously.

Taking a distributed renewable source with maximum output power of 1.5 MW at the LVDC side of the DC/DC converter as an example. Parameters of AC/DC-1 are: N_1= 8, C_{SM} = 20000 μF, P_{in_1} = 1.5 MW, U_{dc1} = 1.5 kV. These parameters are designed according to the method in [34] and are used in the case studies in Section IV.

Case 1: Considering the most severe working condition of a solid DC fault at the outlet of AC/DC-2. The discharging speed of C_{dc2} is limited by the current limiting reactor and the u_2 and P_{out_1} drop less than 20%. In this case, the TIV can be established by DCCBs within 5 ms, and therefore, converters are not blocked. By solving (1), (2) and (3), dU_{dc1} is 0.065kV and ε is 4.35% (<10%). Thus, the voltage quality at the LVDC side is sufficient for source/load to operate continuously under MVDC faults.

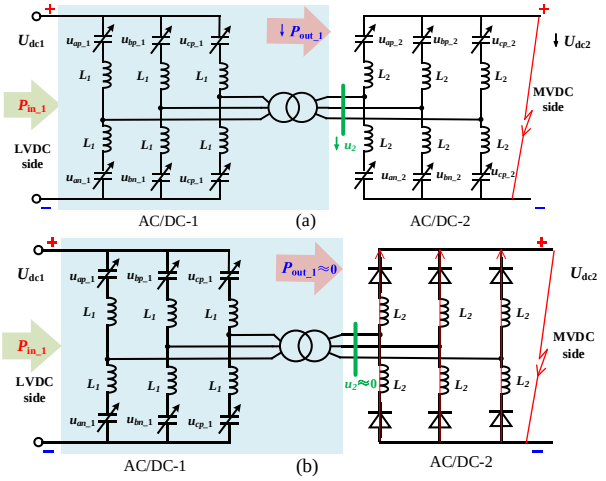

Fig.4. Equivalent circuits and power flow of DC/DC converter based on HBSM during different stages. (a) Before blocking; (b) After blocking.

Case 2: If relay protection or DCCBs fail to operate, the TIV will not be established. Then, AC/DC-2 may be blocked by its own overcurrent protection. The equivalent circuit of the blocked DC/DC converter is shown in Fig. 4(b). Fault currents will flow through the freewheeling diodes in each arm. In this case, u_2 and P_{out_1} will drop largely to near zero. The duration (dt) of the blocking can be hundreds of milliseconds. The long-time imbalance between P_{in_1} and P_{out_1} will lead to a severe voltage variation (much greater than 10%). Since the voltage quality cannot meet the system requirement, the LVDC source/load is unable to operate continuously in this case.

Therefore, in Framework 1, the LVDC source/load can operate continuously under an MVDC fault only if DCCBs can work properly and AC/DC-2 is not blocked. Detailed simulations of Cases 1 and 2 will be presented in Section IV.

III. Operating Characteristics of LVDC Source/Load in FB-MMC DC Systems with Dis-connectors

A. Operating characteristics of key facilities

Referring to Fig. 1(b), the AC/DC and DC/DC converters based on FBSM, and dis-connectors are key facilities which are described as follows.

(1) AC/DC and DC/DC converters based on FBSMs

The schematic diagrams and multiple operating modes of the FBSM are illustrated in Fig. 5. p1 and p2 are the two ports of each FBSM. The voltage difference from p1 to p2 is the output voltage (u_{SM}) of each FBSM, as shown in Fig. 5(a).

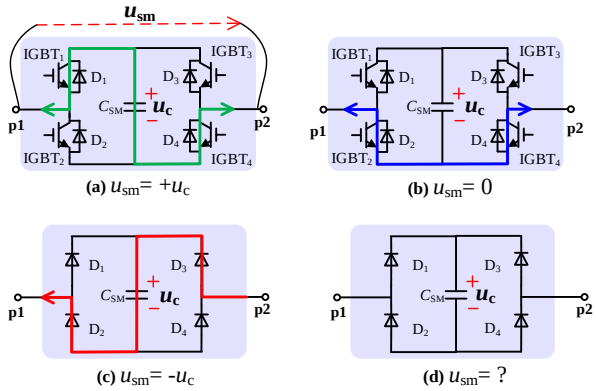

Fig. 5. Operating modes of the FBSM.

During normal states, the output voltage u_{SM} can be +u_c or zero, as shown in Figs. 5(a) and (b). This is similar to the HBSM in Fig. 2(a).

All IGBTs in the FBSM can be turned off when the fault current elimination mode is activated due to a DC fault. u_{SM} will be - u_c if the current flows through D_3 and D_2, as shown in Fig. 5(c). In this case, the capacitor will be charged and the amplitude of u_{SM} will increase. The fault current fed by this converter will be eliminated when the current flowing through the FBSM decreases to zero, as shown in Fig. 5(d). In this case, u_{SM} is uncertain.

If the voltage amplitude of the external circuit is larger than u_c, the amplitude of u_{SM} will equal to u_c, and direction is consistent with the external circuit. If the voltage amplitude of external circuit is smaller than u_c, no current can flow through the diodes, then u_{SM} will be decided by the external voltage, which means that the circuit from p1 to p2 can be regarded as

an open-circuit.

(2) Dis-connectors

According to arc extinguishing ability, switch gears in AC systems can be divided to: circuit breakers, load switches and dis-connectors. A mechanical switch is composed of two parts: arc extinguishing chamber and operating mechanism. Details can be found in [35]. Arc extinguishing ability of a mechanical switch is determined by the specific structure of the arc extinguishing chamber. For mechanical switches with a voltage level of 10 kV, the vacuum interrupter is widely used as the arc extinguishing chamber. Differing from SF6 arc extinguishing chamber, the structure of the vacuum interrupter is quite uniform, which means that dis-connectors, RCB and MS based on vacuum interrupter at the voltage level of 10 kV are nearly the same. Similar to AC vacuum circuit breakers, these switches can interrupt current at the natural zero-crossing point.

B. Procedures of DC fault protection

Procedures of DC fault protection in Framework 2 are illustrated in Fig. 6. In case of an MVDC fault, the relay protection will firstly react based on its local measurement. $\triangle T_1 \approx 1$ ms is needed for fault detection [31].

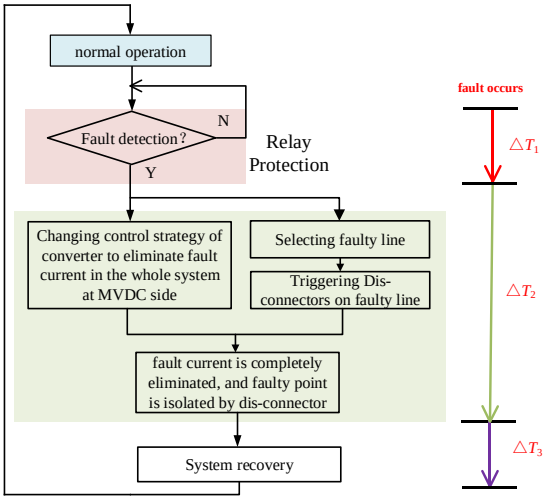

Fig. 6. Procedures of DC fault protection in FB-MMC-DC distribution systems with dis-connectors.

Then, all converters will start the fault current elimination mode by adjusting its control strategy. The fault currents in the MVDC circuit will start decreasing. Along with the decrease of fault currents, the local relay will communicate with the remote relay units to select the faulty line, such as the current differential protection. Then, triggering signals will be sent to the dis-connectors in the faulty line. When fault currents fed by all converters are eliminated, the faulty line can be finally isolated by the dis-connectors. As shown in Fig. 6, $\triangle T_2$ is the time for completing the fault current elimination by all FB-MMCs at MVDC side. $\triangle T_2$ is variable and can be affected by fault type, fault location and fault impedance. According to studies in the literature, the maximum of $\triangle T_2$ is usually within 20 ms [36].

All FB-MMCs will start to recover by adjusting its control strategy once the faulty line is isolated by dis-connectors. $\triangle T_3$ is the time for the post-fault restoration.

It should be noted, without reactors at the MVDC side, the response speed of Framework 2 is faster than Framework 1, which means that $\triangle T_3$ is shorter than $\triangle t_5$.

C. Operating characteristic of LVDC source/load under faults

Similar to the analysis in Section II-C, voltage quality at the LVDC side (U_{dc1}) affects the continuous operation capability of the DC source/load. At the initial stage of DC faults ($\triangle T_1 \approx 1$ ms), the control strategy of AC/DC-2 has not changed. Its equivalent circuit is the same as Fig. 4(a). Although C_{dc2} of AC/DC-2 discharges, voltage on each bridge arm (u_{ap_2}, u_{bp_2}, u_{cp_2}, u_{an_2}, u_{bn_2}, u_{cn_2}) is still balanced. u_2 at the AC side of AC/DC-2 and P_{out_1} decrease, but within tolerable margins.

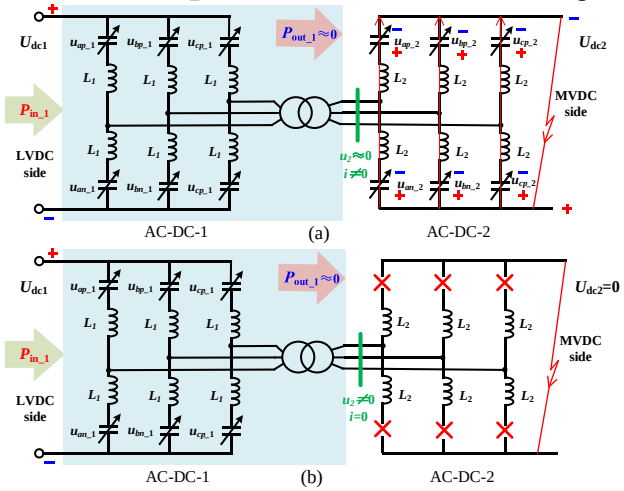

Fig. 7. Equivalent circuits and power flow of DC/DC converter based on FBSM after blocking. (a) During fault current elimination period; (b) After fault current is eliminated.

After starting the fault current elimination mode, at the initial stage, the current flowing through each arm is not zero. The equivalent circuit and power flow of the DC/DC converter are illustrated in Fig. 7(a). In this case, all FBSMs operate in the mode shown in Fig. 5(c), and the fault current will charge the capacitor of FBSMs. As shown in Fig. 7(a), arm voltages of AC-DC-2 (u_{ap_2}, u_{bp_2}, u_{cp_2}, u_{an_2}, u_{bn_2}, u_{cn_2}) are equal. Therefore, u_2 and P_{out_1} are nearly zero as the fault current in each arm is eliminated and P_{in_1} and P_{out_1} are unbalanced in this period.

After the current fed by this converter is eliminated, it needs to wait until the faulty line is isolated by dis-connectors. All FBSMs work in the mode shown in Fig. 5(d) when the current becomes zero. As the valve-side line-to-line voltage is lower than the DC side capacitor voltage, there will be no current in the converter. Therefore, the equivalent circuit and power flow of the DC/DC converter can be illustrated in Fig. 7(b). Each arm can be regarded as an open-circuit, P_{out_1} is still zero and the imbalance between P_{in_1} and P_{out_1} exists constantly. During this period, all surplus energy of AC/DC-1 is stored in the equivalent capacitor (C_{dc1}=6C_{SM}/N_1), which leads to the voltage variation of U_{dc1} (dU_{dc1}).

According to the protection procedures in Fig. 6, this fault current elimination stage can last for $\triangle T_2 \approx 20$ ms. In this case, voltage variation caused by the imbalance between P_{in_1} and P_{out_1} may have exceeded the acceptable range dramatically, which leads to the interruption of the LVDC source/load.

Case 3: Taking the same distributed renewable source in Section II-C as an example: P_{in_1} is 1.5 MW, P_{out_1} is zero, and the fault current elimination time is 20 ms. By solving (1), (2) and (3), dU_{dc1} is 1kV and ε is 66.7%, which is far beyond the acceptable range (±10%). In this case, the worsened voltage quality will hinder the continuous operation of the LVDC source/load. Detailed simulations of Case 3 will be presented in Section IV.

D. Controllable storage unit for continuous operation

To tackle the problem of the interruption of LVDC source/load in Framework 2 due to MVDC faults, a controllable storage unit is proposed in this paper. The proposed device is deployed at the LVDC side of the DC/DC converter as shown in Fig. 8.

(a) Operating principle

As shown in Fig.8, the controllable storage unit consists of a capacitor ($C_{storage}$) and an IGBT switch ($S_{storage}$). During normal states, $S_{storage}$ is off, the voltage on $C_{storage}$ is equal to the maximum of the rated voltage (U_{dc1}). When the converter starts the fault current elimination mode, $S_{storage}$ will be turned on. Then, $C_{storage}$ will be parallel with C_{dc1} (the equivalent capacitors of AC/DC-1). $C_{storage}$ helps to hold the LVDC voltage within an acceptable range.

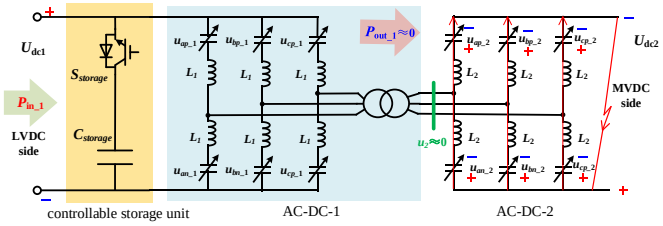

Fig.8. Equivalent circuit and power flow of DC/DC converter with the controllable storage unit after starting fault current elimination mode.

(b) Parameter design

According to the analysis in the above subsection C, the voltage variation is caused by the surplus energy $[\int(P_{in\_1}-P_{out\_1})\cdot dt]$ during the fault current elimination period. By turning on $S_{storage}$, the equivalent capacitance changes from C_{dc1} to $(C_{dc1}+C_{storage})$, which helps to reduce the variation of U_{dc1}. In this case, (1), (2) and (3) change into (4). By setting ε to be the acceptable limit (±10%), and considering the maximum energy of $\int(P_{in\_1}-P_{out\_1})\cdot dt$, the required $C_{storage}$ can be obtained. The withstand voltage of $C_{storage}$ and $S_{storage}$ is equal to the rated LVDC voltage with a safety margin, such as 1.5.

$$C_{storage}=\frac{2\cdot\int(P_{in\_1}-P_{out\_1})\cdot dt}{U_{dc1}^{\ 2}\cdot\varepsilon\cdot(2+\varepsilon)}-C_{dc1} \tag{4}$$

Case 4: Taking the same distributed renewable source in Section II-C as an example: P_{in_1} is 1.5 MW, P_{out_1} is zero, and the fault current elimination time is 20 ms. $C_{storage}$ is 112 mF. In this case, the controllable storage unit improves the voltage quality to meet system requirement, therefore, the LVDC source/load can operate continuously under MVDC faults.

IV. Case Studies

To verify the theoretical analysis of the Cases 1~4 in Sections II and III, simulation models based on the Frameworks shown in Figs.1 (a) and (b) are established in PSCAD/EMTDC. Detailed parameters of simulation models are listed in Table I. One of the most severe conditions has been considered: a solid pole-to-pole short circuit fault at the line_34 in Fig. 1 is set at t = 3 s. Simulation results of those four cases analyzed in Sections II and III are illustrated in Fig. 9 and Fig.10.

TABLE I
PARAMETERS OF SIMULATION MODELS

Parameters	Items	Values
Capacity of MMC-1 (MW)	P_{rate1}	3
Capacity of MMC-2 (MW)	P_{rate2}	3
Capacity of MMC-3 (MW)	P_{rate3}	1.5
Capacity of MMC-4 (MW)	P_{rate4}	1.5
LVDC voltage	U_{dc1}	± 0.75
MVDC voltage	U_{dc2}	± 10
LVDC side SM number in each arm	N_1	8
MVDC side SM number in each arm	M_1	20
LVDC side SM capacitor (μF)	C_{SM}	20000
Current limiting reactor (mH)	L_m	10
Rated interruption current of DCCB (kA)	I_{br}	6
$C_{storage}$ of MMC-3 (mF)	$C_{storage1}$	112
$C_{storage}$ of MMC-4 (mF)	$C_{storage2}$	112

Fig. 9 shows the simulation results of the simulation model in which the LVDC side of DC/DC converters is connected to the distributed renewable source, and Fig.10 shows the simulation results of the simulation model in which the LVDC side of DC/DC converters is connected to DC load. In addition, Case 1 and Case2 are based on Framework 1 and Case 3 and Case 4 are based on Framework 2.

In Case 1, relay protection and DCCB can operate properly, and the TIV is established by DCCBs at t = 3.005 s. In Case 2, failure occurs to relay protection or DCCB, and converters are blocked by its own overcurrent protection at t = 3.006s. In Case 3, converters start the fault current elimination mode at t = 3.001 s. The system starts to recover at t = 3.02 s once the faulty line is completely isolated. In this case, there is no controllable storage unit at the LVDC side of MMC-3 and MMC-4. In Case 4, the only difference from Case 3 is that controllable storage unit is deployed at LVDC side of MMC-3 and MMC-4.

For Case 1, simulation results are illustrated by the pink curve in Fig. 9 and Fig.10. Since current limiting reactors have effectively suppressed the discharging of converters and DCCBs have rapidly established the TIV, as shown in Fig. 9 (a) and (b), Fig.10 (a) and (b), the decreases of U_{dc2} and P_{out1} are limited. So, the imbalance between P_{out1} and P_{in1} is quite small, as shown in Fig. 9 (a) and (c), Fig.10 (a) and (c). It can be known from Fig. 9 (d) and Fig. 10 (d) that the value of voltage variation ratio is only about 4% and the LVDC source/load can operate continuously under MVDC faults.

For Case 2, simulation results are illustrated by the red curve in Fig. 9 and Fig.10. When relay protection or DCCB refuse to respond to DC faults, converters are blocked by its own overcurrent protection for safety concern. In this case, as shown in Fig. 9 (a) and (b), Fig.10 (a) and (b), U_{dc2} and P_{out1} immediately drop almost to zero once the converter is blocked. The long-time imbalance between P_{out1} and P_{in1} leads to the severe variation of U_{dc1} and the interruption of the LVDC source/load, as shown in Fig. 9 and Fig.10.

For Cases 3 and 4, simulation results are illustrated respectively by the blue curve and green curve in Fig. 9 and Fig.10. As shown in Fig. 9 (a) and (b), Fig.10 (a) and (b), U_{dc2}

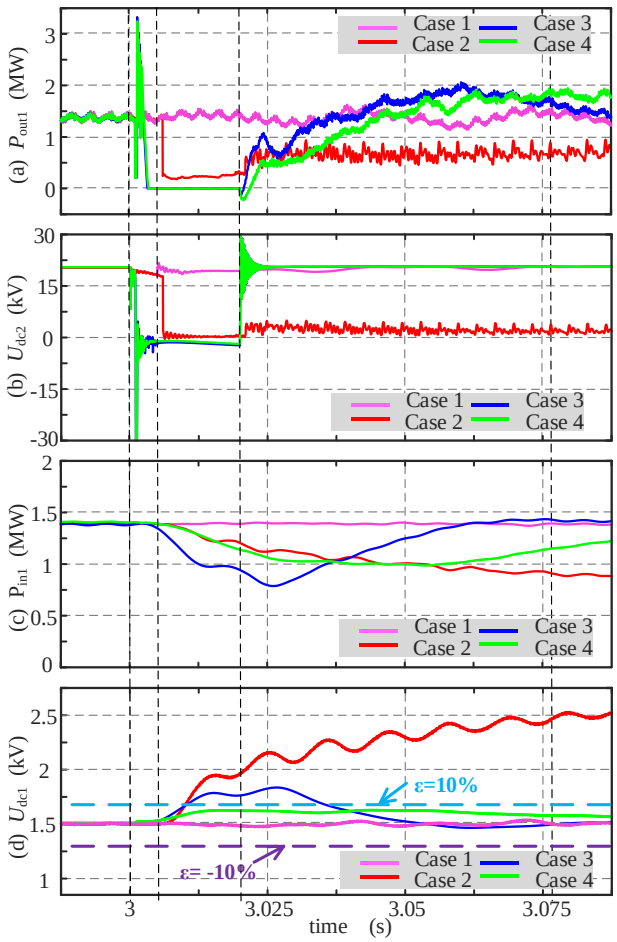

Fig. 9. System responses of the four cases with LVDC source. (a) P_{out1}; (b) U_{dc2}; (c) P_{in1}; (d) U_{dc1}.

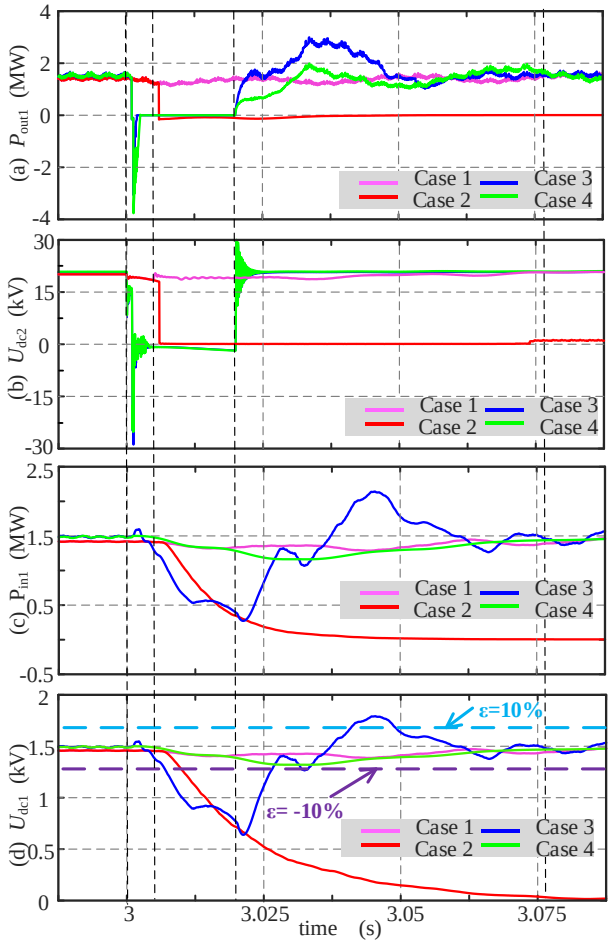

Fig. 10. System responses of the four cases with LVDC load. (a) P_{out1}; (b) U_{dc2}; (c) P_{in1}; (d) U_{dc1}

and P_{out1} drop to zero immediately when converters start the fault current elimination mode. U_{dc2} and P_{out1} start to recover to a normal state when converters recover at t = 3.02 s after the faulty line is isolated. However, in Case 3, without the controllable storage unit, during the interval of the 20 ms, the power imbalance causes a large voltage variation of U_{dc1} and the decrease of P_{in1}. The voltage variation ratio is much greater than 10%, thus, the interruption of the LVDC source/load occurs under the MVDC fault. In Case 4, during the interval of 20 ms, the deployed controllable storage unit helps to maintain U_{dc1} and P_{in1}. As shown in Fig. 9 (c) and (d), Fig.10 (c) and (d), the voltage variation ratio is smaller than 10%. In this case, the LVDC source/load can operate continuously without being interrupted by the MVDC fault.

V. Comparisons

The LVDC source/load in both Cases 1 and 4 can work continuously without being interrupted by MVDC faults. In this section, Framework 1 and Framework 2 with the proposed controllable storage unit are compared in terms of capital cost, continuous operation capability of LVDC source/load and system response speed. It is worth meaning that the operating losses of the HB-MMC and FB-MMC are not included as it has been widely discussed in the literature [36].

The difference of construction cost between the two MMC-DC systems in Fig.1(a) and Fig.1(b) is mainly reflected by facilities based on power electronic devices and traditional electrical apparatus.

(1) Power electronic devices

Facilities and electronic devices in these two typical MMC-DC systems are listed in Table II and Table III respectively. For fair comparison, same commercial IGBTs and diodes are used in these facilities.

Referring to Figs.1 and 2, in Framework 1, the number of IGBTs/diodes used in MMC-1 and MMC--2 is $2\times6\times2\times M_1 = 24M_1$; number of IGBTs/diodes used in MMC-3 and MMC-4 is $2\times6\times2\times(M_1+N_1) = 24(M_1+N_1)$. Due to the configuration of the FBSM, the power electronics devices in FBSM based converters are twice in number when comparing to HBSM based converters. Considering good voltage waveform and electrical tolerance of single power electronic devices, the commercial IGBT module (FZ600R12KE3, rating voltage of 1.2kV, rating current of 0.6kA, price of 1056 yuan) produced by Infineon is used. Herein, M_1 is 20 and N_1 is 8.

The same IGBT module is used in hybrid DCCB and the controllable storage unit. Referring to Fig. 2(c), since the TIV in the hybrid DCCB, which is decided by the clamped voltage of the MOV, is usually 1.6 p.u. of the rated DC voltage, at least 14 series-connected SMs are needed to satisfy the voltage tolerance requirement. Considering the 6 kA rated interruption current of the DCCB, at least 5 parallel-connected SMs are needed to satisfy the current tolerance requirement. One SM is used in the LCS of LCP. Then, the total number of

IGBTs/diodes in the hybrid DCCB is 2×(14×5+1)=142. The number of IGBTs/diodes used in the 24 DCCBs are 24×2×(14×5+1)=3408.

As mentioned in Section III-D, the rated voltage of $S_{storage}$ of the controllable storage unit is 1.5 kV. Therefore, two IGBT modules are series connected to satisfy the voltage and current tolerance requirements. Then, the total number of IGBTs/ diodes in the two controllable storage units is 4.

TABLE II
KEY FACILITIES IN THE TWO SYSTEMS

Items	Framework 1	Framework 2
AC/DC converter	2	2
DC/DC converter	2	2
Hybrid DCCB	24	0
Controllable storage unit	0	2

TABLE III
IGBTS AND DIODES USED IN THE TWO SYSTEMS

Items	Framework 1		Framework 2	
	IGBTs	diodes	IGBTs	diodes
2 AC/DC	480	480	960	960
2 DC/DC	672	672	1344	1344
24 Hybrid DCCBs	3408	3408	0	0
2 Controllable storage units	0	0	4	4
Total Number	**4560**	**4560**	**2308**	**2308**
Cost	**4.81 million RMB**		**2.44 million RMB**	

(2) traditional electrical apparatus

8 reactors of 10 mH are used in Framework 1. According to [37], the cost of air reactors is estimated to be 1560 RMB/mH. Therefore, 124800 RMB is needed for 8 reactors.

2 capacitors of 112 mF and rated voltage of 1.5 kV are needed in the controllable units. According to [38], the cost of capacitors is estimated to be 1RMB/J. Therefore, 252000 RMB is needed for two capacitors.

(3) Continuous operation capability of LVDC source/load under MVDC faults

According to the analysis in Section II and the simulation results of Case 1 in Section IV, if converters are not blocked and DCCBs can establish the TIV within 5ms in Framework 1, the voltage variation at the LVDC side will be limited within an acceptable range. According to the analysis in Section III and the simulation results of Case 4 in Section IV, the LVDC source/load in Framework 2 will not be interrupted thanks to the employment of the proposed controllable storage unit. It should be noted that the capacity of controllable storage unit should be designed according to the rating capacity of converter.

In general, since the voltage quality can meet the system requirement, the LVDC source/load could operate continuously in both Framework 1 and Framework 2 without being affected by DC faults at MVDC side.

(4) system response speed

Because air reactor could slow down system response speed, after faulty line is isolated, Framework 2 could be recovered to normal state faster than Framework 1.

The comparisons of the two systems are summarized in Table IV.

TABLE IV
COMPARISON BETWEEN THE TWO SYSTEMS

Items	Framework 1	Framework 2
Capital cost	large	Small
Continuous operation capability of LVDC source/load	High	High
System response speed	Slow	Fast

It can be seen from Tables III and IV that the capital cost of Framework 1 is higher than Framework 2 due to the former's large application of DCCBs.

VI. CONCLUSION

With the rapid development of renewable sources and loads with DC interfaces, MMC-DC systems are excellent alternatives for traditional AC systems in future distribution power grids. In this paper, the continuous operation capability of LVDC sources/loads under MVDC faults in two typical MMC-DC frameworks is studied. The research shows that due to the application of DCCBs in HB-MMC-DC systems, power imbalance of DC-DC converter is quite little, and the LVDC source/load can operate continuously without being interrupted by MVDC faults. However, with FB-MMCs dealing with MVDC faults, long-time power imbalance occurs to DC-DC converter, and the surplus energy could lead to significant voltage variation at LVDC side and further result in non-continuous operating of LVDC source/load in FB-MMC-DC systems. To tackle this problem, a controllable storage unit is proposed to ensure the continuous operation of the LVDC source/load. The structure, installing position and parameter design of this controllable storage unit are presented. For completeness, comprehensive comparisons between the two typical MMC-DC systems are conducted.

The main contribution of this paper is revealing the mechanism of power imbalance and voltage variation at LVDC side and proposing a controllable storage unit to solve the non-continuous operating problem in FB-MMC-DC systems so as to save the high capital cost of DCCBs.

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