A Low-Loss Integrated Circuit Breaker for HVDC Applications

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***Abstract*—Hybrid dc circuit breakers (HCBs) are recognized as suitable devices for protecting high-voltage direct-current (HVDC) systems, along with other dc circuit breakers (DCCB). However, compared to mechanical circuit breakers, HCBs exhibit higher conduction losses. Such losses are inevitable under no-fault conditions as current may flow through some of the semiconductor switches. An integrated circuit breaker (ICB) minimizing these losses is presented in this paper, and this is achieved by replacing semiconductor switches by mechanical components in the current path. For completeness, the topology design, operating sequence and a mathematical analysis for component sizing of the device are provided. In addition, an estimation of the conduction losses is quantified. It is estimated that the power losses of an ICB are 2 to 30% of an HCB only. The ICB has been implemented in PSCAD/EMTDC to demonstrate its effectiveness for isolating dc faults, with simulations conducted on a three-terminal HVDC grid.**

***Index Terms*—HVDC, protection, dc circuit breaker.**

I. Introduction

HIGH-VOLTAGE direct-current (HVDC) networks have been widely deployed for bulk power transmission over high-voltage alternating-current systems due to their lower power losses and greater controllability. More recently, there has been a growing interest of connecting converter terminals to build multi-terminal HVDC grids. This has been reflected not only by a substantial amount of academic research [1], [2], but also by recent practical projects, such as the ±200kV$_{dc}$ Zhoushan five-terminal HVDC grid and the ±500kV$_{dc}$ Zhangbei four-terminal HVDC system [3], [4]. These two multi-terminal systems are intended for the grid integration of renewables while, at the same time, ensuring reliability of power supply.

Despite the advantages offered by HVDC grids, their deployment is hindered by an inevitable challenge: dc grid protection. Although ac circuit breakers (ACCBs) could be used for isolating dc faults, their speed of operation is slow and the whole system must be temporarily de-energised if they are employed [5], [6]. Alternatively, converters with fault blocking capability may be immediately blocked (or controlled to reverse their dc voltage) to suppress a dc fault; however, protection schemes based on such converters are not selective: all converters have to be blocked to isolate the fault [7], [8].

The widely accepted option for selective protection is the use of dc circuit breakers (DCCBs). Three main technologies have been proposed: passive and active resonant DCCBs, full solid-state DCCBs (SSCB) and hybrid DCCBs (HCBs). When a fault occurs, passive resonant DCCB, via (passive) inductors and capacitors, generate an oscillating current superimposed with the fault current, creating zero-crossings. As these devices are mechanical-based, they have a low cost and exhibit negligible conduction losses [9]. However, their slow operating speed makes them less attractive than other options. Active resonant DCCBs are instead more suitable for protecting HVDC systems. Compared to their passive counterparts, active resonant DCCBs have pre-charged capacitors to actively inject counter currents upon faults. This way, a zero-crossing is rapidly created by imposing a high frequency counter current (>1000 Hz). A fast mechanical switch can then open within 5-10 ms [10], [11]. This type of DCCBs, together with HCBs, have been considered for the Zhangbei HVDC system [12]. SSCBs can immediately block a fault; however, their conduction losses are unacceptably high due to the deployment of a large number of semiconductor switches in the current path [13], [14].

Considerable research has been dedicated to the HCB [15]. Its main shortcoming is the high investment cost arising from the hundreds of semiconductor switches used in its bidirectional main breaker (BMB). Although its power losses are more than 10 times lower than those in a SSCB [16], they are still high compared to the losses of mechanical DCCBs—which have an extremely low on-resistance and no forward voltage drop. Hence, a significantly higher amount of energy is dissipated within the lifetime of an HCB compared to that of a mechanical-based device. Moreover, adequate cooling systems are required for the load current switches (LCSs) within the load current branch of the HCB—further increasing its cost and volume [16].

Research has been carried out to reduce the number of semiconductor switches in HCBs to decrease investment costs. An interesting concept is the integrated circuit breaker (ICB) (or multi-port DCCB) [17]-[26]. In addition to a current interruption branch, an ICB contains bypass and supplementary branches with ultra-fast disconnectors (UFDs) and LCSs. The main disadvantage of the device is the amount of power losses contributed by the LCSs. This issue has been overlooked in the literature, with solutions limited to those from manufacturers [27], [28]. Connecting multiple IGBT units in parallel could reduce losses, but these would not be minimized, and the additional IGBTs would increase the cost of the LCSs [27].

Reference [28] presents an HCB without LCSs. Although its losses are extremely low, this device requires the sequential operation of multiple fast mechanical switches for fault current interruption, hence introducing extra delays. Mechanical-based

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active resonant DCCBs also avoid using LCSs [29]-[33]. These devices have resonant circuits formed by reactors and pre-charged capacitors to enable zero-crossing currents. However, the capacitors may only be charged to the voltage level of the dc system, while the charging process is not fully controllable. To further reduce losses, switches based on highly efficient wide-bandgap materials (*e.g.* silicon carbide) may replace silicon-based switches in DCCBs.

In line with the discussion in the previous paragraphs, a low-loss ICB is presented in this paper. As in previous topologies found in the literature, a single current interruption branch is used. In addition, the device here presented offers the following benefits: 1) by removing the LCSs from load current branches where current flows under no-fault conditions, conduction losses are reduced to 2 to 30% of those of an HCB with a similar current rating; 2) current commutation is achieved by inserting pre-charged capacitors with very small voltages (i.e. their voltage rating is very low); 3) the charging of these capacitors is very fast (~15 ms) and their voltage is fully controllable.

II. Hybrid and Integrated Circuit Breakers

A. Conventional Hybrid DC Circuit Breaker

(**Note:** In this paper, the definitions of time in the CIGRE Technical Brochure 683 are used, as shown in Fig. 1 [34].)

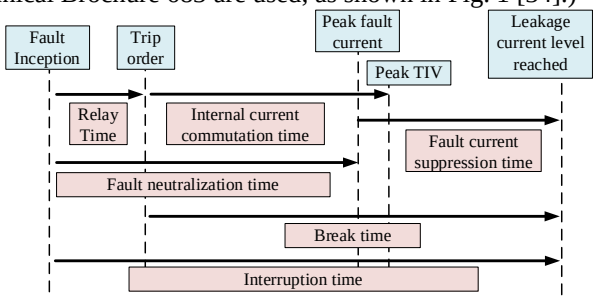


Fig. 1. Time definition throughout a fault blocking event [34].

Fig. 2 shows a schematic for an HCB. The device has a load current branch and a BMB. The load current branch is formed by a mechanical UFD and an LCS based on a few semi-conductor switches [15]. Under no-fault conditions, current flows through the load current branch only. Power losses are incurred due to the forward voltage drop and on-resistance of the LCS. If a fault occurs, the LCS blocks to commutate current to the BMB, which features hundreds of semiconductor switches. The anti-series connected IGBTs in the LCS may block current in either direction. S_1 can be opened to block a current flowing from point A to B, whereas S_2 can be opened if current flows from B to A. Only one IGBT is opened at a time and, hence, the voltage is not shared between S_1 and S_2.

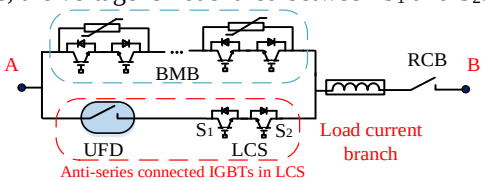


Fig. 2. Schematic of a conventional HCB.

The UFD opens after current commutation, taking around 2 to 3 ms. After the UFD is fully opened, the BMB immediately blocks to block the fault current and the fault energy is absorbed by the associated surge arrester. The residual current breaker (RCB) is opened at last to prevent the arrester from overloading.

The speed of internal current commutation is within 3 ms, mainly due to the delay of UFD action. The operation of the semiconductor switches is within tens of microseconds. Such a speed is sufficient for system protection.

B. Conventional Integrated Circuit Breaker

Fig. 3 shows the general topology of an ICB. The device features a single current interruption branch (*e.g.* unidirectional main breaker), which contains most semiconductor switches. The load current branches are similar as those in an HCB and current flows through them under no-fault conditions. Supplementary branches operate in coordination with the load current branches to ensure that, upon a fault, the fault current is commutated to the current interruption branch. These branches can contain an LCS and a UFD each (as a load current branch does) [17]-[22], or be based on thyristors or diodes [23]-[26].

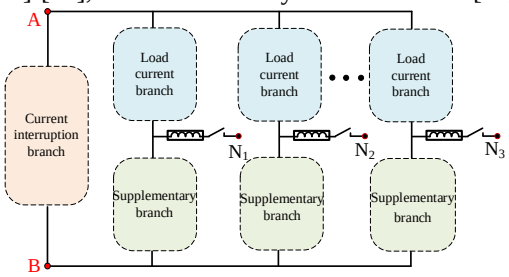


Fig. 3. General topology of an ICB.

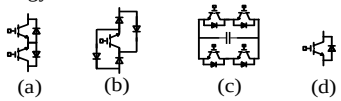


Fig. 4. Configurations of semiconductor switches for the main breaker and LCSs of an ICB: (a) anti-series IGBT unit; (b) bridged one-IGBT-four-diode unit; (c) full-bridge unit; (d) single IGBT unit.

Different configurations of semiconductor switches can be deployed for both the LCSs and the current interruption branch and, thus, their selection should be done with care. These are shown in Fig. 4. Anti-series IGBT units are used to block current in both directions but feature two IGBTs per unit [20]. To reduce the number of IGBTs by half, bridged one-IGBT-four-diode units may be adopted [21]. Full-bridge units exhibit the highest number of IGBTs, but facilitate voltage sharing among units during and after fault blocking. A single IGBT unit has the smallest number of components; however, it can only block current in one direction; in addition, current commutation takes longer if pre-fault currents flow through its diode [22].

III. Low-Loss Integrated Circuit Breaker

A. Low-Loss ICB Concept

Fig. 5 shows the structure of the low-loss ICB. As in Fig. 3, the presented ICB consists of a current interruption branch, load current branches and supplementary branches. However, the configuration of both the bypass and supplementary branches is different to other topologies found in the literature.

As shown in Fig. 5, only mechanical-based UFDs (UFD_{A1}, … UFD_{An}) are deployed in the load current branches, while the LCSs associated with their cooling systems have been removed. Hence, currents do not flow through any semiconductor switch under no-fault conditions. Power losses are thus minimized as forward voltage drops and on-resistances are avoided.

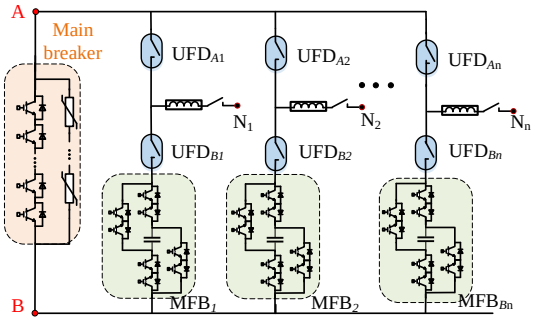


Fig. 5. Structure of the low-loss ICB.

The supplementary branches contain modified full-bridge (MFB) units and UFDs (UFD$_{B1}$, … UFD$_{Bn}$). Under no-fault conditions, the MFBs are fully blocked to ensure zero current at the supplementary branches and to prevent the capacitors from charging or discharging. However, under fault conditions, the MFBs are used to inject reversed voltages at the load current branches to create zero-crossing currents. To achieve this, the MFBs' capacitors are pre-charged to the same voltage level.

(**Note:** A precise control of the capacitor voltage is desirable. If there are many MFBs, the capacitors can be charged one by one to facilitate the charging process. By increasing the capacitance and switching frequency of the IGBTs within the MFBs, an improved voltage regulation may be achieved.)

A UFD cannot be opened with arc when there is a continuous current flowing through it. Therefore, the UFDs at the load current branches can fully open only when the current flowing through them is very close to zero and such current is commutated to another branch. The supplementary branches in the ICB enable this commutation and, hence, the UFDs can keep being opened to reach an adequate separation distance.

Once the UFD current is commutated, the main breaker can block immediately afterwards to isolate the fault. Following fault isolation, the capacitors' voltage can be regulated to the pre-fault voltage level. (Further details on the operating sequence of the ICB are provided in Section III-B.)

At the current interruption branch, unidirectional IGBT units are used as they contain a reduced number of semiconductor switches compared to other options in Fig. 4. This is sufficient, as for a fault occurring at an arbitrary node (N$_1$, … N$_n$, see Fig. 5), the current will flow from point A to B only due to the current commutation achieved by the supplementary branches.

B. Operating sequence

For simplicity, the operating sequence of the low-loss ICB is described for a configuration with three nodes, as shown in Fig. 6. However, the same sequence is applicable for devices with additional nodes. Prior to a dc fault, current flows only through the load current branches, as shown in Fig. 6(a), minimizing power losses. Both the main breaker and the MFBs are blocked to prevent leakage current from flowing through them. When a fault occurs at a node of the ICB (*e.g.* N$_3$), fault currents will be fed from the healthy nodes (N$_1$ and N$_2$) to the faulty node through the load current branches. This is shown in Fig. 6(b).

When the fault is detected, a tripping signal will be sent to UFD$_{A1}$, UFD$_{A2}$ and UFD$_{B3}$ for them to open. However, currents still flow through UFD$_{A1}$ and UFD$_{A2}$ as their contacts cannot be separated electrically. To be able to open these UFDs with arc, the currents flowing through them should be commutated to the supplementary branches, but this can only happen until they are virtually zero. As shown in Fig. 6(c), this is achieved by the simultaneous closing of the main breaker and MFBs at the healthy nodes (MFB$_1$ and MFB$_2$). The MFBs can then insert immediately a reversed voltage to create a zero-crossing current at the load current branches. This voltage should be defined according to the current direction at the load current branch and the polarity of the capacitor voltage. For instance, if the voltage polarity and current direction ($i_1^{(1)}$) are as shown in Fig. 7(a), IGBTs S$_1$ and S$_3$ of the MFB should be closed so that the inserted voltage is reversed. The polarity of the voltage across UFD$_{A1}$ (U_{ufdA1}) can hence be changed and the zero-crossing of $i_1^{(1)}$ is created. Conversely, if the direction of $i_1^{(1)}$ is as shown in Fig. 7(b), IGBTs S$_2$ and S$_4$ should be closed instead. The speed for voltage injection depends on the operation of the IGBT units (*i.e.*, several tens of microseconds).

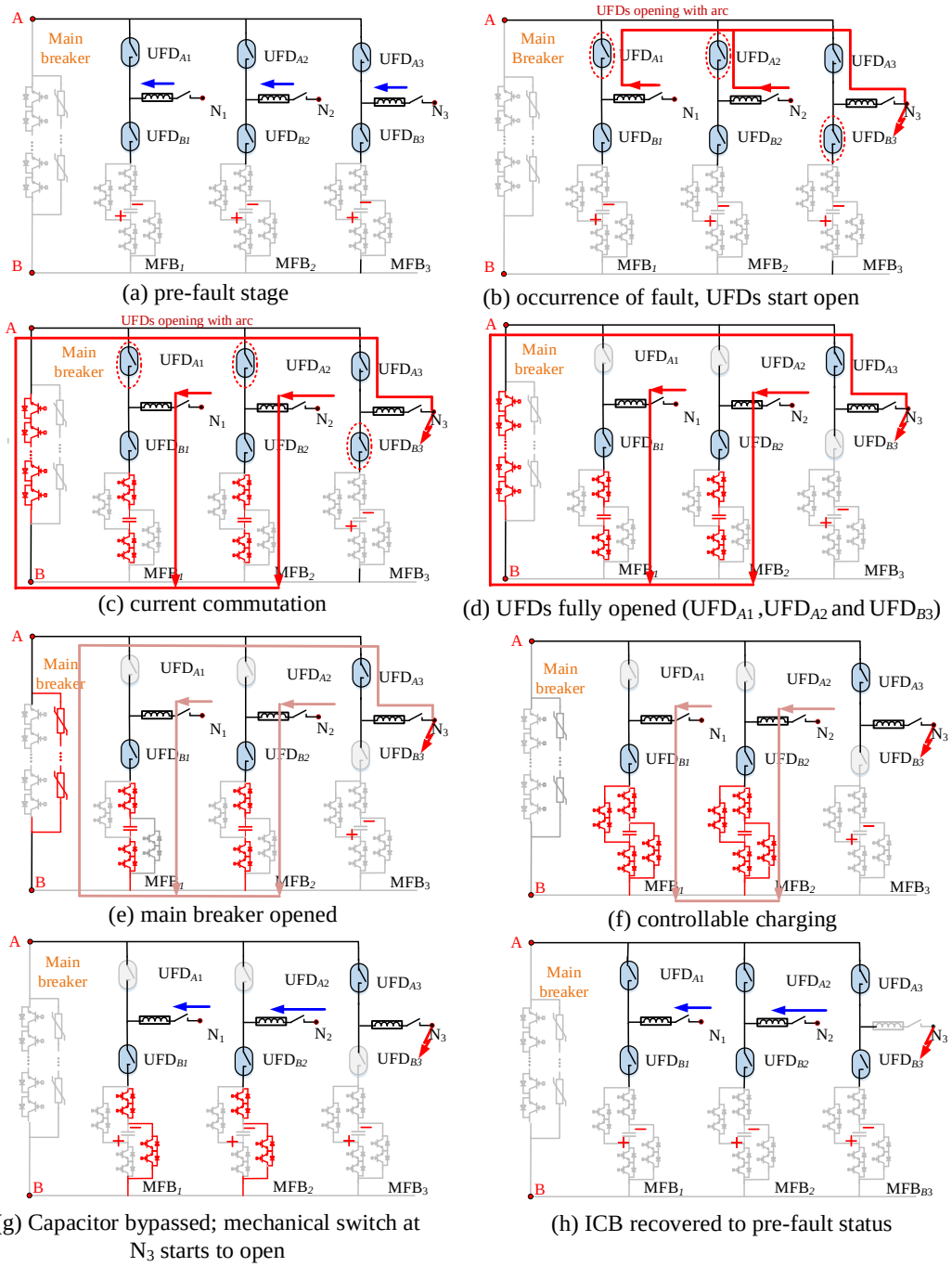
Once the current at the load current branches is brought to virtually zero (<0.01 kA), UFD$_{A1}$, UFD$_{A2}$ and UFD$_{B3}$ are opened with arc within 3 ms (similar as the operating speed of HCBs) [15]. (Ultra-fast vacuum switches could have been used instead of UFDs due to their low conduction losses, incurring a delay in milliseconds only as they open [36].) As the contacts of the UFDs separate extremely fast, a large arc resistance (*e.g.* 100 Ω) is created. However, this value is much larger than the resistance of the main breaker and the MFBs. Thus, current will keep flowing through the main breaker, and the contacts of the UFDs are able to further move to reach an adequate separation distance. (A similar commutation approach employing UFDs with capacitors was experimentally tested in [35]. A low voltage (< 2kV) is adopted, but suitable discussion is provided to justify scalability for high voltage applications; *e.g.* 320 kV.)

As the UFDs are fully opened by now, the high voltage transient is withstood, as shown in Fig. 6(d). In addition, the main breaker can immediately block, and the fault energy will be absorbed by the surge arresters, as shown in Fig. 6(e). The fault current will drop to zero once the energy is fully absorbed.

It is worth noting that UFDs could be different from each other in practice and opening them simultaneously could be challenging. If the main breaker is blocked before a UFD should have opened, its corresponding MFB may be damaged by over-voltage. For instance, if UFD$_{A1}$, UFD$_{A2}$ and the main breaker open and UFD$_{B3}$ does not, the MFBs will be exposed to the arrester voltage. To prevent this, the main breaker must be blocked only after all corresponding UFDs are opened.

Immediately after the main breaker has blocked, current will keep flowing through the healthy circuits. Simultaneously, the MFBs at these circuits (MFB$_1$ and MFB$_2$) can operate to charge their capacitors to the pre-fault level, as shown in Fig. 6(f). A proportional-integral (PI) controller is adopted to regulate the capacitor voltage (U_{meas}) to a desired reference value (U_{c_ref}), as shown Fig. 8. The sources for charging the capacitors are the converters connected to N$_1$ and N$_2$. These can be either local or remote converters connected through a transmission line.

The charging process takes up to tens of milliseconds. However, as the fault current has already been blocked, such a time duration is acceptable. To ensure fast charging and to avoid overshoots, the gains of the PI controller should be accurately tuned. A suitable analysis of the system's open loop



(a) pre-fault stage

(b) occurrence of fault, UFDs start open

(c) current commutation

(d) UFDs fully opened (UFD$_{A1}$,UFD$_{A2}$ and UFD$_{B3}$)

(e) main breaker opened

(f) controllable charging

(g) Capacitor bypassed; mechanical switch at N$_3$ starts to open

(h) ICB recovered to pre-fault status

Fig. 6. Operating sequence of the low-loss ICB.

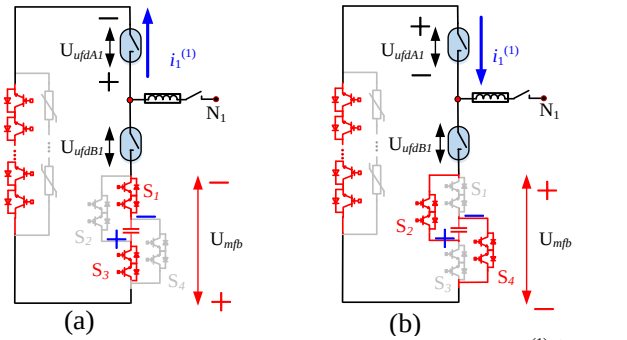


Fig. 7. Detailed MFB action to create current zero-crossing: (a) $i_1^{(1)}$ flowing from N$_1$ to other nodes; (b) $i_1^{(1)}$ flowing from other nodes to N$_1$.

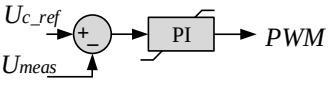


Fig. 8. Controller to charge the capacitor of the MFBs.

response will facilitate this process. In addition, a derivative action may be also incorporated to further reduce overshoot. To increase the speed of charging, a large proportional gain may be employed as long as stability is not affected. Also, the switching frequency of IGBTs can be increased.

Once their voltage is regulated to the pre-fault level, the capacitors of the MFBs can be bypassed to prevent them from further charging or discharging, as shown in Fig. 6(g), while current between healthy nodes flows through the closed IGBTs

of the MFBs (highlighted in red). This will last until the residual mechanical switch opens at the faulty node N_3 (see Fig. 6(h)), which takes 50 to 60 ms as in an RCB of an HCB. The opening of the residual mechanical switch allows the recovery of all other components to their pre-fault status. All the UFDs at load current branches can be reclosed and, hence, the current can flow through them while incurring extremely low losses. The MFBs and the main breaker are re-opened to prevent leakage currents. Alternatively, instead of opening the residual mechanical switch at N_3, UFD_{A3} can also be opened even faster to separate the faulty point and allow the other components to recover to their pre-fault status. This will make the residual mechanical switch redundant. Removing this switch may further reduce the cost of the ICB.

The operating sequence just described enables the ICB to isolate faults at an arbitrary node. Moreover, it can be recovered to further protect the system from additional faults. The time for internal current commutation (from Fig. 6(a) to 6(e)) is less than 3 ms, which is similar as in conventional HCBs; *i.e.*, no extra delay is incurred. In addition, the current flowing through the healthy nodes is not fully blocked. Current still flows through N_1 and N_2 as these nodes are connected to a power source either directly or through a transmission line. However, during the transient regime following the fault, the currents will exhibit fluctuations, which can last for over a hundred milliseconds until steady-state is reached. The charging of the capacitor is a controllable process taking a very short period. Thus, no cooling system is required for the MFBs—current will flow only through the mechanical UFDs at the load current branches prior and following the fault isolation process.

The ICB can also clear multiple faults if the energy rating of surge arrester and the current rating of the main breaker are sufficient. The same operating sequence can be followed to clear a second fault if the RCB at the first faulty node opens after the first fault or if multiple faults happen simultaneously. An exception is for a second fault occurring before the MFBs' capacitors are fully recharged. Here, current commutation will fail due to the capacitors' reduced voltage level. However, as the recharging duration is very short (*e.g.* < 20 ms), multiple faults at such a short interval would be unlikely.

Reclosure of the ICB is achievable. Its main breaker can be reclosed after the capacitors of the MFBs are recharged to pre-fault levels (see Fig. 6(g)). This is to inject a current to the faulty node (N_3) to determine whether the fault is non-permanent (following a fault discrimination method). UFD_{A3} and the RCB should stay closed in this period. If a non-permanent fault is identified and cleared, the main breaker will re-open. Otherwise, UFD_{A1} and UFD_{A2} can be reclosed to connect N_1 and N_2 to N_3. The IGBTs in the MFBs will be opened also.

IV. ICB Analysis and Component Sizing

A. Component Sizing

The components within the ICB presented in Section III should withstand significant magnitudes of current and voltage during a fault. The worst-case scenario is for a solid fault taking place directly at one of the nodes of the ICB (*e.g.* at N_3).

Prior to any breaking operation, the fault current is fed through healthy nodes, as shown in Fig. 6(b). The equivalent circuit of the ICB during this period is given in Fig. 9. L_1, L_2 and L_3 are the current limiting reactors at each node, while R_1, R_2 and R_3 are the (extremely small) resistances of the UFDs at the load current branches. To obtain the maximum fault current, the voltages at the healthy nodes (u_1 and u_2) are maintained at the rated dc system voltage (U_{dc}) before fault isolation:

$$u_1(t) = u_2(t) = U_{dc} \tag{1}$$

Resistive effects are ignored as the inductances are much larger than the resistances. Node currents are described by

$$\begin{cases} U_{dc} - u_A(t) = L_1 \frac{di_1(t)}{dt} \\ U_{dc} - u_A(t) = L_2 \frac{di_2(t)}{dt} \\ 0 - u_A(t) = L_3 \frac{di_3(t)}{dt} \\ \frac{di_1(t)}{dt} + \frac{di_2(t)}{dt} + \frac{di_3(t)}{dt} = 0 \end{cases} \tag{2}$$

where $i_1(t)$, $i_2(t)$ and $i_3(t)$ are the node currents. The sign convention for these currents is given in Fig. 9. As the fault occurs at N_3, $i_3(t)$ is also the fault current. The voltage at the faulty node is zero. The voltage across the inductor is then given as $(0 - u_A(t))$ in the 3rd equation in (2). It is worth mentioning that the 4th expression is valid as the sum of the currents entering Point A is equal to zero, which is a constant. There is no other alternative conduction path. Hence, the sum of the derivatives of these currents must be also zero.

Solving for the node currents in (2) at time t_1 yields

$$\begin{cases} I_3^-(t_1) = I_3(t_o) - (t_1 - t_o) \times \frac{U_{dc}}{L_3 + 1/(1/L_1 + 1/L_2)} \\ I_2^-(t_1) = I_2(t_o) + (t_1 - t_o) \times \frac{1}{L_2\left(\frac{1}{L_1} + \frac{1}{L_2}\right)} \times \frac{U_{dc}}{L_3 + 1/(1/L_1 + 1/L_2)} \\ I_1^-(t_1) = I_1(t_o) + (t_1 - t_o) \times \frac{1}{L_1\left(\frac{1}{L_1} + \frac{1}{L_2}\right)} \times \frac{U_{dc}}{L_3 + 1/(1/L_1 + 1/L_2)} \end{cases} \tag{3}$$

where $I_1(t_o)$, $I_2(t_o)$ and $I_3(t_o)$ are the pre-fault currents at the nodes. Superscript "–" denotes a pre-action steady-state operating condition and "+" denotes a post-action steady-state condition. Times t_0 and t_1 are, respectively, the time at which the fault occurs and the start of ICB action.

At t_1, the main breaker and the MFBs at healthy nodes are closed so that a reversed voltage is inserted. The equivalent circuit of the ICB for this condition is shown in Fig. 10, where R_{MB} is the on-resistance, U_{MBfwd} is the forward voltage drop of the main breaker, and C_1 and C_2 are the inserted pre-charged capacitors of MFB_1 and MFB_2, respectively. Since there is a reduced number of IGBTs within the MFBs, their on-resistance and forward voltage drops are ignored. Assuming that $I_1^-(t_1)$ and $I_2^-(t_1)$ are positive (*i.e.* current flows from the nodes to the faulty point), the voltages at the capacitor ends ($u_{lcr1}(t)$ and $u_{lcr2}(t)$) and at point A ($u_A(t)$) will have the following relationship:

$$\begin{cases} u_{lcr1}^-(t_1) - u_A^-(t_1) > 0 \\ u_{lcr2}^-(t_1) - u_A^-(t_1) > 0 \end{cases} \tag{4}$$

To create a zero-crossing at the load current branches (*i.e.* currents through R_1 and R_2), the following condition should be satisfied following ICB action:

$$\begin{cases} u_{lcr1}^+(t_1) - u_A^+(t_1) \le 0 \\ u_{lcr2}^+(t_1) - u_A^+(t_1) \le 0 \end{cases} \tag{5}$$

which, using the circuit from Fig. 10, can be rewritten as:

$$\begin{cases} u_{c1}^+(t_1) \ge I_3^+(t_1) \times R_{MB} - U_{MBfwd} \\ u_{c2}^+(t_1) \ge I_3^+(t_1) \times R_{MB} - U_{MBfwd} \end{cases} \tag{6}$$

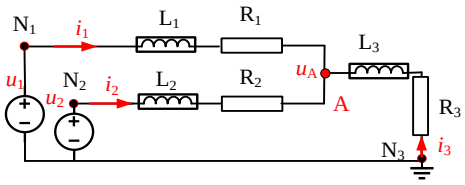


Fig. 9. Equivalent circuit of an ICB before breaking operation.

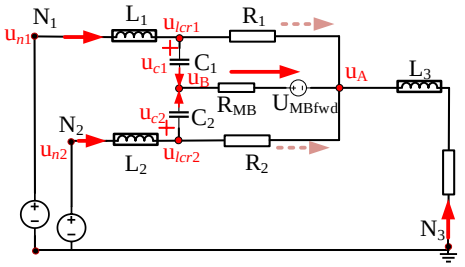


Fig. 10. Equivalent circuits of an ICB when it starts inserting voltage.

where $u_{c1}^{+}(t_1)$ and $u_{c2}^{+}(t_1)$ are the voltages across the pre-charged capacitors at t_1. $I_3^{+}(t_1)$ is the current flowing through the main breaker and it is equal to $I_3^{-}(t_1)$. It should be noted that R_1 and R_2 have been ignored in (6). The main breaker has much more IGBTs than LCSs do and, hence, its resistance R_{MB} is larger than the LCSs' resistances ($R_{MB} \gg R_1$; $R_{MB} \gg R_2$).

The values of R_{MB} and U_{MBfwd} will depend on the number of IGBTs in the main breaker. For a DCCB rated at several-hundred kilovolts, a main breaker could have hundreds of IGBTs and, hence, the voltage drop across it at a time t_1 would be around several hundred volts [21]. Thus, a voltage less than 1 kV is adequate for $u_{c1}^{+}(t_1)$ and $u_{lcr2}^{+}(t_1)$ and, as a result, also suitable as the voltage rating of the capacitor. It should be noted that this voltage would be a fraction of the dc system rating.

If the stray inductance between the main breaker and the MFBs is considered, the capacitors need to be further charged to a higher level to counter the voltage drop across them during the current commutation. Such a voltage could be in range of several hundred volts, depending on the value of the inductance and the rate of change of current. The general expressions of $u_{c1}^{+}(t_1)$ and $u_{c2}^{+}(t_1)$ then become

$$\begin{cases} u_{c1}^{+}(t_1) \geq I_3^{+}(t_1) \times R_{MB} - U_{MBfwd} + U_{stray} \\ u_{c2}^{+}(t_1) \geq I_3^{+}(t_1) \times R_{MB} - U_{MBfwd} + U_{stray} \end{cases} \tag{7}$$

$$U_{stray} = L_{stray} \times \frac{di_3(t)}{dt} \tag{8}$$

where L_{stray} and U_{stray} are the stray inductance and voltage.

If the injected voltage of a load current branch is smaller than the voltage drop across the main breaker, its current cannot be fully commutated to the main breaker and, hence, the current will be blocked. DCCBs at the remote ends of transmission lines connected to a failed branch will have to be opened to stop fault propagation. However, commutation failure in a load current branch will not affect other branches which successfully commutate their currents to the main breaker. As a result, their currents can be blocked by the main breaker.

Once the currents at the load current branches (flowing at R_1 and R_2) reach virtually zero, the UFDs will start to open exhibiting arcs and will reach their full dielectric insulation capability following a time delay of 2 to 3 ms. The equivalent circuit of the ICB within the delay is shown in Fig. 11.

It can be seen that the fault current $i_3(t)$ will keep increasing through the MFBs and the main breaker. The detailed equation for this condition is derived as:

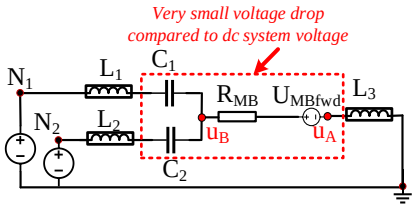


Fig. 11. Equivalent circuits of an ICB during UFD opening.

$$\begin{cases} L_1 \frac{di_1(t)}{dt} + u_{c1}(t) = U_{dc} - u_B(t) \\ L_2 \frac{di_2(t)}{dt} + u_{c2}(t) = U_{dc} - u_B(t) \\ L_3 \frac{di_3(t)}{dt} + i_3(t) \times R_{MB} = u_B(t) + U_{MBfwd} \\ \frac{di_1(t)}{dt} + \frac{di_2(t)}{dt} + \frac{di_3(t)}{dt} = 0 \end{cases} \tag{9}$$

Voltage $u_B(t)$ at point B is then obtained as

$$u_B(t) = \frac{\left(\frac{1}{L_1}+\frac{1}{L_2}\right)U_{dc} + \frac{1}{L_3}[U_{MBfwd} + i_3(t)R_{MB}] - \left(\frac{u_{c1}(t)}{L_1}+\frac{u_{c2}(t)}{L_2}\right)}{\left(\frac{1}{L_1}+\frac{1}{L_2}+\frac{1}{L_3}\right)} \tag{10}$$

Since the total voltage drop across the main breaker is much smaller than the dc system voltage (*i.e.*, $-U_{MBfwd} - i_3(t)R_{MB} \ll U_{dc}$) while inductors L_1, L_2 and L_3 at the nodes have a similar inductance, term $\frac{1}{L_3}[-U_{MBfwd} - i_3(t)R_{MB}]$ in (10) can be neglected. In addition, as $u_{c1}(t)$ and $u_{c2}(t)$ are a fraction of the dc system rating (*e.g.* less than 1 kV), $\frac{u_{c1}(t)}{L_1} + \frac{u_{c2}(t)}{L_2}$ is also negligible. Thus, (10) can be simplified to

$$u_B(t) = \frac{\left(\frac{1}{L_1}+\frac{1}{L_2}\right)U_{dc}}{\left(\frac{1}{L_1}+\frac{1}{L_2}+\frac{1}{L_3}\right)} \tag{11}$$

Let t_2 be the time when the main breaker blocks to interrupt fault current. The maximum fault current is given as:

$$I_3^{-}(t_2) = I_3^{+}(t_1) - (t_2 - t_1)\frac{U_{dc}}{L_3 + 1/\left(1/L_1 + 1/L_2\right)} \tag{12}$$

which implies that the current rating of the main breaker should be at least $I_3^{-}(t_2)$. Currents $i_1(t)$ and $i_2(t)$ at t_2 are given as

$$\begin{cases} I_1^{-}(t_2) = I_1^{+}(t_1) + (t_2 - t_1)\frac{1}{L_1\left(\frac{1}{L_1}+\frac{1}{L_2}\right)} \times \frac{U_{dc}}{L_3 + 1/\left(1/L_1 + 1/L_2\right)} \\ I_2^{-}(t_2) = I_2^{+}(t_1) + (t_2 - t_1)\frac{1}{L_2\left(\frac{1}{L_1}+\frac{1}{L_2}\right)} \times \frac{U_{dc}}{L_3 + 1/\left(1/L_1 + 1/L_2\right)} \end{cases} \tag{13}$$

As these currents flow through the MFBs, the current rating of MFB_1 and MFB_2 should be no less than $I_1^{-}(t_2)$ and $I_2^{-}(t_2)$.

Although (12) and (13) have been derived using a three-node ICB, they can be easily extended for a device with *n* nodes. For an *n*-node ICB with a fault occurring at node *j*, the total susceptance of the healthy nodes is expressed as

$$\frac{1}{L_{hlthy}} = \sum_{\substack{\beta=0 \\ \beta \neq j}}^{n-1} \frac{1}{(L_j)} \tag{14}$$

The maximum fault current flowing through the faulty node *j* is then derived as:

$$I_j^{-}(t_2) = I_j(t_o) - (t_2 - t_0)\frac{U_{rated}}{L_j + L_{hlthy}} \tag{15}$$

where $I_j(t_o)$ is the initial current at node *j*. It should be noticed that this expression only shows the fault current flowing through the faulty node at t_2, but the currents through healthy nodes (*i.e.* in (13)) are different.

The maximum fault current flowing through an MFB at a healthy node is:

$$I_\beta^{-}(t_2) = I_j^{-}(t_2) \times \frac{L_{total}}{L_\beta} \tag{16}$$

where $1/L_{\text{total}}$ is the total susceptance of all nodes, including the one at the faulty node *j*:

$$\frac{1}{L_{total}} = \sum_{\beta=0}^{n} \frac{1}{(L_j)} \quad (17)$$

Hence, for an *n*-node ICB, the current rating of the main breaker and the MFBs should be no less than $I_j^-(t_2)$ and $I_\beta^-(t_2)$.

The voltage rating of the main breaker and for all UFDs is typically selected as 1.5 times of the dc system rating (*i.e.* $1.5U_{dc}$) [15]. The surge arrester across the main breaker should be also rated at $1.5U_{dc}$ to prevent the main breaker and UFDs from exhibiting overvoltages.

The energy rating of the surge arrester is calculated as:

$$E_{MB} = 1.5U_{dc} \times I_j^-(t_2) \times (\tfrac{t_3 - t_2}{2}) \quad (18)$$

where t_3 is the time when fault energy has been fully absorbed.

If clearance of multiple faults is required, the surge arrester's rating needs to be further increased. The maximum current needs to be recalculated considering the total number of nodes, node inductances, speed to block fault current and the number of faults required to be isolated simultaneously. Once the maximum current is estimated, the minimum energy rating required by the surge arrester can be obtained.

It should be highlighted that nodes are connected to dc sources for this analysis, and a fault is applied directly to one of them. This is to ensure a maximum current can be calculated as the impedance between the faulted node and any voltage sources is minimized. Hence, the designed ICB can be connected to any converters or transmission lines. However, if the dc lines are taken into account for the calculation, these should be considered as an extra inductance to be added to the reactor at each node [18]. In other words, they will be considered as reactors but exhibiting a larger inductance.

B. Discussion on Conduction Losses

The conduction losses of the presented ICB are similar to those of mechanical-based DCCBs. The power losses at a load current branch (P_{loss_β}) of an ICB are simply calculated with

$$P_{\text{loss}\_\beta} = {i_\beta}^2 \times R_\beta \quad (19)$$

where i_β and R_β are the current and the resistance of the UFD.

Conversely, the power losses of a load current branch of an HCB (P_{loss_HCB}) are composed by the power losses of the UFD and the LCS (with the latter being dominant), given by:

$$P_{\text{loss}\_HCB} = {i_\beta}^2 \times R_\beta + {i_\beta}^2 \times R_{LCS} + i_\beta \times U_{LCSfwd} \quad (20)$$

where R_{LCS} and U_{LCSfwd} represent the equivalent on-resistance and forward voltage drop of the LCS (since an LCS could have multiple IGBTs).

A comparison between P_{loss_β} and P_{loss_HCB} is made by conducting a sensitivity analysis where system performance is assessed by varying R_β from 200 $\mu\Omega$ to 2000 $\mu\Omega$. The values of R_{LCS} and U_{LCSfwd} are selected as 4 mΩ and 2.1 V, respectively [21]. R_β is set initially to 500 $\mu\Omega$, which considers both the conductor and contacts. The contact resistance may be from tens of $\mu\Omega$ to 1500 $\mu\Omega$, but it varies with the type of contact material and the number of UFD being switched [37]. However, information on the conductor resistance is not widely available in the literature, which justifies the analysis.

Current i_β is increased from 0 to 3 kA. As shown in Fig. 12(a), $P_{\text{loss}\_HCB} = 46.8$ kW—mainly contributed by the LCS (${i_\beta}^2 \times R_{LCS} = 36$ kW; $i_\beta \times U_{\text{LCSfwd}} = 6.3$ kW). Conversely, $P_{\text{loss}\_\beta} = 4.5$ kW, which represents a reduction by almost 10 times compared to the HCB. Although such a difference would be smaller when the load current is low, P_{loss_β} is significantly lower than P_{loss_HCB} (*e.g.* around 6 kW less when i_β = 1 kA).

Fig. 12(b) shows the ratio of power losses of both devices (P_{loss_β} /P_{loss_HCB}) against the ratio of on-resistance of LCS and UFD (R_β/R_{LCS}). This ratio is changed from 0.05 to 0.5 by keeping R_{LCS} as 4 mΩ but varying R_β from 200 to 2000 $\mu\Omega$. It is observed that P_{loss_β} is only 2% to 30% of P_{loss_HCB} (as R_β/R_{LCS} increases). A lower ratio of R_β/R_{LCS} and a smaller magnitude of i_β would lead to a smaller P_{loss_β} /P_{loss_HCB} and vice versa. However, as previously mentioned, R_β is typically less than 1 mΩ ($R_\beta/R_{LCS} < 0.25$). Thus, P_{loss_β} remains lower than 17% of P_{loss_HCB} even for a high current (*e.g.* 3 kA).

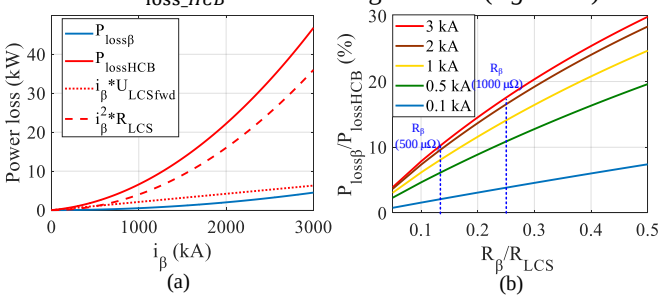


Fig. 12. Comparison of losses: (a) power loss against current i_β; (b) power loss ratio (P_{loss_β} /P_{loss_HCB}) with different on-resistance ratio and i_β (R_β/R_{LCS}).

Considering that DCCBs should operate for a long period of time, a significant energy saving can be achieved if ICBs are adopted. Moreover, reduction of power losses has implications on the design of cooling systems. For instance, the cooling system for the LCSs within HCBs would not be required in the low-loss ICB presented in this paper.

C. Comparison Between Different DCCB Topologies

Active resonant DCCBs, such as the SCiBreak circuit breaker presented in [38], [39], also exhibit low power losses. A current zero-crossing is also created at the load current branch by the injection of a reversed voltage by a capacitor. Differences and similarities between the ICB presented in this paper and the SCiBreak device are discussed next.

The SCiBreak circuit breaker is a mechanical-based device and, hence, can be located at the load current branch without causing significant power losses. The current interrupter starts to block the fault current, incurring a delay of ~3 ms. For this device, the rating of the capacitor used to inject the reversed voltage is only a small percentage of the system voltage—preventing the need for a fully rated capacitor. A voltage source converter is needed for controlling the voltage injection. As opposed to the ICB, the SCiBreak device does not require UFDs and has been designed to protect one node per DCCB.

With regards to the ICB, the main breaker is based on semiconductors and is located at a separate current interruption branch as opposed to a load current branch. The main breaker blocks the fault following a minor delay caused by the opening of UFDs. A minimum delay time is ~1.8 ms [40]. Arguably, the ICB's current blocking is slightly faster than for active resonant breakers, although such a difference may be insignificant. Each capacitor of the ICB is rated at a fraction of the system voltage (*e.g.* <1 %) and it is connected within an MFB.

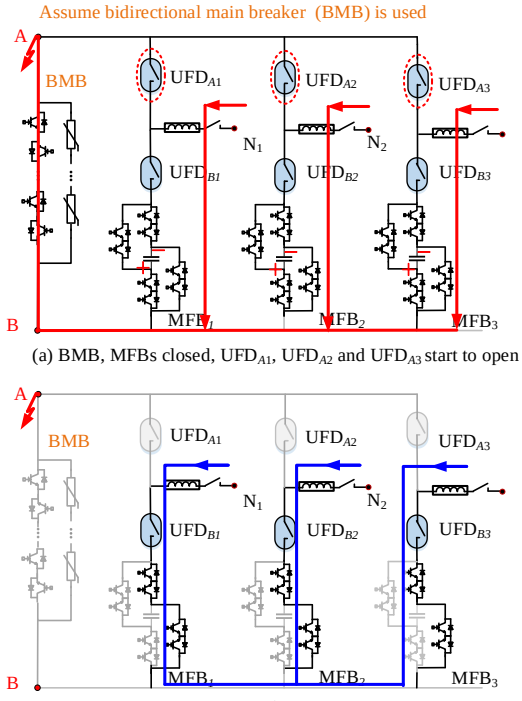
The use of a capacitor with a low voltage rating is a common advantage of the ICB and the SCiBreak device. In the ICB though, the voltage charging process of the capacitor is fully controllable. Both devices employ a similar current commutation method, but this was first demonstrated at high power for the SCiBreak circuit breaker in [39]. However, a major advantage of the ICB is its capability to protect multiple nodes with a single device.

Other DCCB topologies using fewer semiconductor devices to block fault currents than typical HCBs have been designed [20], [21], [41], [42]. They achieve this by using a single IGBT string to block fault current, while extra switchgear (*e.g.* UFDs) is used to configure the direction of the current. For instance, the use of IGBTs is reduced by half in the device presented in [41]. A single node is protected by this DCCB.

A major advantage of the low-loss ICB introduced in this paper compared to other alternatives found in the literature is its capability to protect multiple nodes with a single device. It should be emphasized that the ICB topologies presented in [20], [21], [42] also achieve this. The ICB in [21] features a significantly lower number of semiconductors by including additional UFDs or diodes. The ICB in [20] has a reduced number of both semiconductor switches and surge arresters. Reference [42] considers the functionality of dc current flow control embedded within the device. However, the devices in [20], [21], [42] consider LCSs at their load current branches, which increases power losses—such a shortcoming is avoided by the low-loss ICB introduced this paper.

D. Isolation of DC Bus Faults and Backup Protection

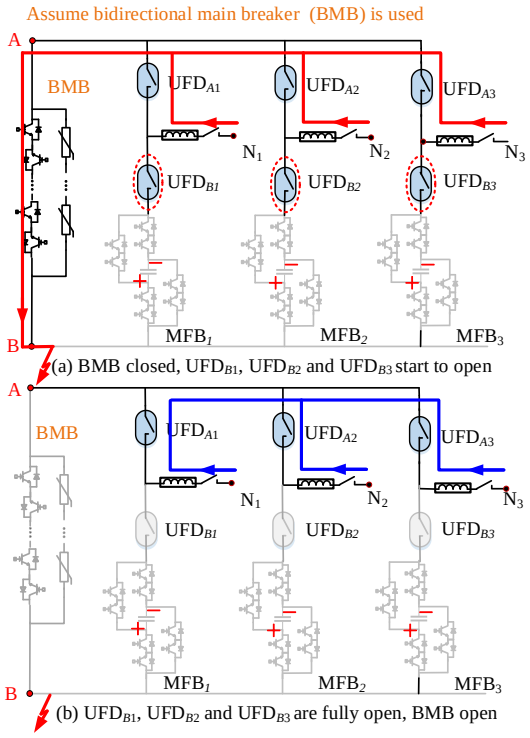
Isolation of dc bus faults and backup protection are desirable capabilities of any DCCB. For instance, both features are achievable with a multiport DCCB using bidirectional thyristor units in its main breaker, as shown in [43]. The presented ICB in this paper may also offer these capabilities if its unidirectional main breaker is replaced by a BMB.



(a) BMB, MFBs closed, UFD$_{A1}$, UFD$_{A2}$ and UFD$_{A3}$ start to open

(b) UFD$_{A1}$, UFD$_{A2}$ and UFD$_{A3}$ fully open, BMB open

Fig. 13. Operation of an ICB to isolate the fault at Bus A.



(a) BMB closed, UFD$_{B1}$, UFD$_{B2}$ and UFD$_{B3}$ start to open

(b) UFD$_{B1}$, UFD$_{B2}$ and UFD$_{B3}$ are fully open, BMB open

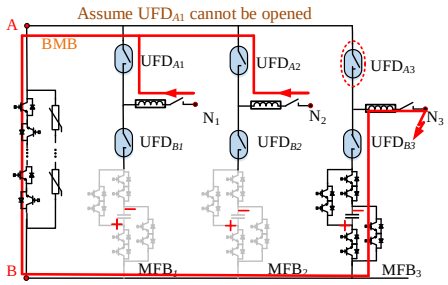
Fig. 14. Operation of an ICB to isolate a fault at Bus B.

The procedure to isolate a fault at Bus A is shown in Fig. 13. Once the fault is detected, the BMB and all MFBs need to close immediately for current commutation. UFD$_{A1}$, UFD$_{A2}$ and UFD$_{A3}$ then open, as shown in Fig. 13(a). The BMB can subsequently open to block the fault, as shown in Fig. 13(b). Current will continue to flow between all nodes through the MFBs once the fault has been successfully blocked.

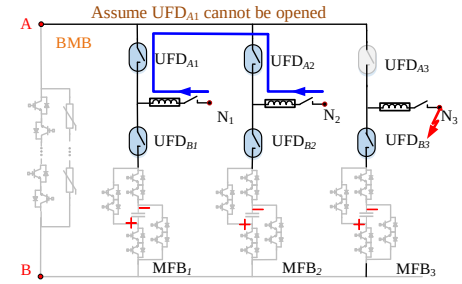
The ICB can also isolate faults at Bus B, as shown in Fig. 14. After the fault, the BMB closes immediately and UFD$_{B1}$, UFD$_{B2}$ and UFD$_{B3}$ start to open. The MFBs do not need to act while the fault current flows through its surge arresters (omitted in the drawing) prior to the closure of the BMB. Once the UFDs are fully opened, the BMB may open to block the fault, as shown in Fig. 14(b). Once the fault is blocked, current can be exchanged between all nodes.

The device presented in this paper arguably offers an extra advantage compared to the DCCB in [43] following a fault. In the presented ICB, the post-fault currents cause small power losses similar to those of the LCSs of HCBs as they flow through MFBs containing only a few IGBTs. Instead, post-fault currents flowing through the DCCB in [43] do so through a string of series-connected thyristors. Given that the string is rated at system voltage level, as a result, larger power losses are produced, which could be comparable to those of a SSCB.

Backup protection may be also achieved by incorporating a BMB to the ICB. To this end, consider the failure of UFD$_{A1}$ (see Fig. 15) so that it cannot open. Once the fault at N$_3$ is detected, MFB$_3$ and the main breaker need to close immediately and, hence, all the currents can be commutated to the main breaker (see Fig. 15(a)). UFD$_{A3}$ will then start to open. It can be seen that the current will now flow from Bus A to Bus B for backup protection. Since a BMB is used, the main breaker is capable of blocking current in both directions. Once UFD$_{A3}$ fully opens, the BMB and MFB$_3$ can then open to block the fault, as shown in Fig. 15(b). Currents at the healthy nodes will keep flowing.



(a) close the main breaker and MFB$_3$



(b) UFD$_{A3}$ fully open, main breaker and MFB$_3$ open

Fig. 15. Backup protection for isolating a fault at N$_3$.

TABLE I
COMPARISON OF ADVANTAGES

	Presented ICB	DCCB in [43]
Bus fault isolation	Yes, if BMB is used	Yes, BMB has been used
Backup protection	Yes, if BMB is used	Yes, BMB has been used
Mechanical switches	6	3
Strings of thyristors	0	2×4
Strings of IGBTs	1 (2 for BMB)	0
Voltage rating of capacitors	<1 % of system voltage	High voltage
Pre-charge circuit	No	Required

A comparison between the ICB and the DCCB in [43] is given in Table I. Notice that the design in Section III considers a unidirectional main breaker with a single string of IGBTs. Once this is replaced by a BMB to enable bus fault isolation and backup protection, two strings of IGBTs are considered instead.

Although the DCCB contains fewer mechanical switches than the ICB, and a thyristor has a lower unit price compared to an IGBT, the total number of required thyristors in [43] is much higher than the number of IGBTs in the ICB—even following inclusion of the BMB. This facilitates device maintenance for the ICB as mechanical switches are easier to maintain compared to semiconductor devices. In addition, the voltage rating of the capacitors within the ICB's MFBs is <1% of the system voltage (0.5-5 kV), which is significantly lower when compared to the DCCB, rated at 110 kV. Moreover, the ICB does not require a pre-charge circuit, as capacitor charging is achieved by the current flowing through the MFBs following fault isolation. The DCCB requires a pre-charge circuit with a voltage source to charge the capacitor.

V. SIMULATION STUDIES

Simulation studies are performed to verify the effectiveness of the low-loss ICB to provide protection for an HVDC grid. The meshed three-terminal HVDC system shown in Fig. 16 has been simulated in PSCAD/EMTDC. This is a monopolar system, with an ICB located at each terminal. For bipolar HVDC systems, two ICBs should be deployed instead per terminal (one for the positive pole and one for the negative pole). A time step of 5 μs has been adopted.

The dc system is rated at 400 kV and meshed by overhead lines modeled as lumped π sections. All converter terminals are voltage source converters (VSCs) operating under voltage droop control [44]. System parameters are given in Table II.

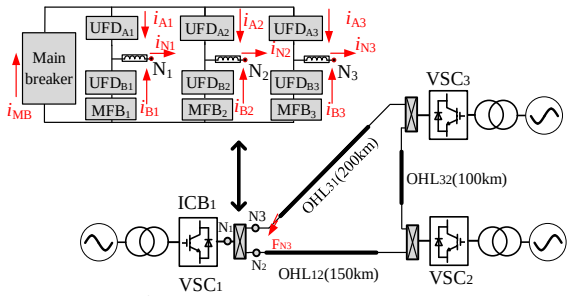


Fig. 16. Protection of a meshed three-terminal HVDC system using the presented low-loss ICB.

TABLE II
SYSTEM PARAMETERS

Component	Parameter/control setting
DC line (per 50 km)	R = 0.57 Ω; C = 0.615 μF; L = 0.04678 H
VSC$_0$	Droop gain: –0.05 kV/kA; current reference:
VSC$_1$	2 kA; voltage reference: 400 kV Droop gain: –0.05 kV/kA; current reference: 1 kA; voltage reference: 400 kV
VSC$_2$	Droop gain: –0.05 kV/kA; current reference: –2 kA; voltage reference: 400 kV

The voltage rating of the ICBs is set to 600 kV and a current rating of 3 kA is chosen. IGBT module 5SNA 3000K452300 [45], with voltage and current ratings of 4.5 kV and 3 kA, respectively, is used for the main breaker and the MFBs. Should a higher current rating be desired (*e.g.* 6 kA), additional IGBTs should be connected in parallel or IGBTs with higher current rating should be selected instead.

For the main breaker, >134 IGBTs should be connected in series to withstand a voltage of 600 kV. Considering each IGBT has a forward voltage drop of 0.7 V and a resistance of 0.7 mΩ, the total voltage drop for the main breaker is calculated as ~380 V. To inject the reversed voltage, the capacitors of the MFBs are charged to 0.5 kV.

The voltage-current curve of the surge arrester significantly affects the voltage across the ICB during protection. This curve is provided in Fig.17. The base voltage is 400 kV (as the system voltage). The voltage-current rating is selected as 1.5 to ensure the peak voltage across the ICB is around 600 kV.

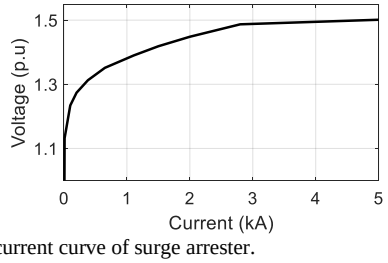


Fig. 17. Voltage-current curve of surge arrester.

The UFDs are modeled as follows. When they are closed, their resistance is set to 500 μΩ. As they open, this value increases to 100 Ω when the currents flowing through the UFDs reach 0.01 kA or lower. The total time to open a UFD is set to 2.5 ms. Current commutation can be maintained while a UFD opens. This is due to the large arc resistance exhibited by UFDs, and most currents will flow through the low-resistance branches

(*i.e.* MFBs and main breaker). Once the UFDs fully open after 2.5 ms, their resistance is increased to 10^8 Ω.

The inductors of the ICBs are selected to have an inductance of 0.2 H, as this limits the maximum rate of change of current to 1.33 kA/ms. It is worth mentioning that the selection of this inductance is identical as for typical HCBs, as the inductors for both type of devices are connected in the same way. Although a larger inductance would reduce the maximum rate of change of current, this could affect system stability. Therefore, small inductance values are preferred as long as the DCCB has a sufficient current rating to withstand a maximum fault current.

A. Isolation of a Solid DC Fault

A solid dc fault test is undertaken, with simulation results shown in Figs. 18-20. Results are focused on ICB_1 (dc terminal of VSC_1) to clearly show the protection performance of the ICB.

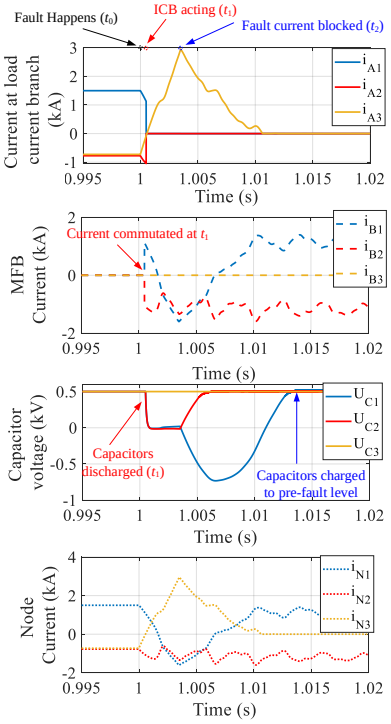


Fig. 18. System current and voltages.

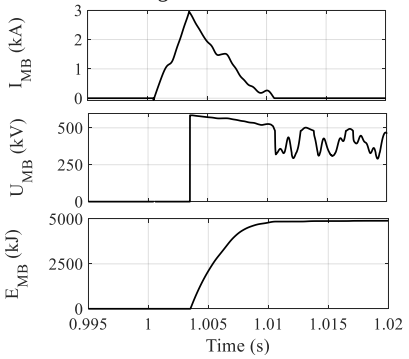


Fig. 19. Current, voltage and dissipated fault energy of the main breaker.

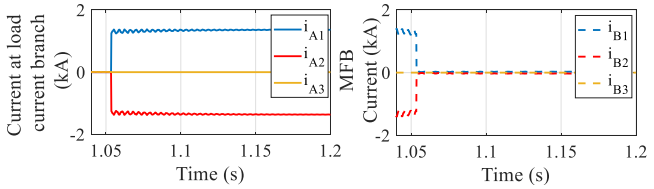


Fig. 20. Currents at healthy nodes are re-commutated to load current branches.

The fault is applied at node N_3 at 1 s (t_0) into the simulation. It can be observed that prior to the fault, current flows through the UFDs at the load current branches only (UFD_{A1}, UFD_{A2} and UFD_{A3}). The values of such currents are i_{A1} = 1.5 kA (for UFD_{A1}), i_{A2} = 0.77 kA (UFD_{A2}) and i_{A3} = 0.73 kA (UFD_{A3}). No current flows through the MFBs at the supplementary branches (*i.e.* $i_{B1} = i_{B2} = i_{B3} = 0$) as the MFBs and main breaker are open.

The fault is detected within 0.5 ms (at t_1) and the ICB acts to isolate the fault. The MFBs at the healthy branches (MFB_1 and MFB_2) and the main breaker are closed simultaneously. Consequently, the pre-charged capacitors of MFB_1 and MFB_2 are inserted, providing reversed voltages to immediately draw i_{A1} and i_{A2} to virtually zero. It is worth mentioning that as the initial directions of i_{A1} and i_{A2} are opposite, different pairs of IGBTs within the MFBs are closed for the voltage insertion (*e.g.* S_1 and S_3, or S_2 and S_4 in Fig. 7). The currents of the healthy nodes are then commutated to the supplementary branches, and i_{B1} and i_{B2} become different from zero. This way, UFD_{A1} and UFD_{A2} can be opened along with UFD_{B3}. The total operating speed of the UFDs is 3 ms. During this period, i_{A3} keeps rising and flowing through the load current branches connected to the faulty node. MFB_3 remains open and, hence, i_{B3} remains equal to zero. In addition, the capacitors of MFB_1 and MFB_2 are discharged and their voltages drop virtually to zero. The capacitors are then temporarily bypassed prior to the recharging progress to prevent their voltages from becoming negative. This will help to speed up the recharging process to a pre-fault value in a later stage.

The main breaker immediately blocks the fault current after the corresponding UFDs fully open. Fig. 19 shows that the fault current at the main breaker I_{MB} drops to zero and ~5000 kJ of energy is absorbed by the surge arrester. The maximum voltage across the main breaker is 600 kV (1.5 times of the voltage rating of the dc system), determined by the surge arrester. In Fig. 18, it is also observed that the current in node N_3 (i_{A3}) drops to zero; thus, the fault has been successfully isolated.

MFB_1 and MFB_2 recharge their capacitors to 0.5 kV after the main breaker has blocked, taking ~15 ms in total (see Fig. 18). The MFBs then act to bypass their respective capacitor to prevent it from further charging and discharging. The currents flowing at the healthy nodes (i_{A1} and i_{A2}) remain unblocked via the supplementary branches. To prevent the dissipation of a significant amount of power at MFB_1 and MFB_2, the currents flowing through them (i_{B1} and i_{B2}) must be re-commutated to the load current branches after the residual mechanical circuit breaker at Node 3 opens (as discussed in Section II-B, see Fig. 6(h)). This requires the re-closure of UFD_{A1} and UFD_{A2}.

The total time to open the residual mechanical circuit breaker and for the re-closure of the UFDs has been set to 50 ms in this study. Fig. 20 shows that once UFD_{A1} and UFD_{A2} re-close at around 1.053 s, i_{B1} and i_{B2} are immediately commutated to the load current branches, given that i_{A1} and i_{A2} change to ±1.36 kA, while i_{B1} and i_{B2} become zero. This ensures that current only flows through mechanical components; hence, power losses are minimized while the system is well protected.

It should be noted that in the 50 ms when currents flow through the MFBs after the fault has been blocked, the currents have a magnitude of only ±1.36 kA, which is within the continuous current operating limit (3 kA) of the selected IGBTs. To withstand larger post-fault currents, IGBTs with higher

current ratings should be adopted or additional IGBTs may be connected in parallel. Given that power is dissipated in the MFBs during this period, IGBTs with a low resistance and forward volage drop are desirable.

B. Test of ICB with a Voltage Safety Margin of 60%

A safety margin of around 60% of the DCCB's rated voltage is usually considered in practice. To this end, a test considering a voltage rating of 960 kV is conducted, requiring 214 IGBTs. The peak voltage drop across the main breaker is calculated as 0.6 kV. To clearly distinguish the results from those in the first test, the capacitors of the MFBs are charged to a much higher value (5 kV as opposed to 0.5 kV).

A similar fault as in Section V-A is simulated, with results shown in Figs. 21 to 23. Prior to the fault, current flows through the UFDs at the load current branches only (UFD_{A1}, UFD_{A2} and UFD_{A3}, see Fig. 21). The fault is detected at t_1 (1.0005 s) and the ICB commutates currents to the MFBs and the main breaker. The capacitors of MFB_1 and MFB_2 are discharged, driving i_{A1} and i_{A2} to virtually zero, as also seen in Fig. 21. UFD_{A1}, UFD_{A2} and UFD_{B3} then open in 3 ms. The main breaker has not yet been blocked and, hence, i_{A3} keeps rising.

Once all the corresponding UFDs open, the main breaker immediately blocks. Consequently, the fault drops to zero and ~5000 kJ of energy is absorbed by the surge arrester (see Fig. 22). The maximum voltage across the main breaker is 600 kV. This value is irrespective to the voltage rating of the ICB and is determined by the surge arrester. MFB_1 and MFB_2 recharge their capacitors to 5 kV after the main breaker opens, taking around 20 ms (also shown in Fig. 21).

Fig. 23 shows that the currents flowing through the MFBs are re-commutated to the load current branches after the mechanical circuit breaker at Node 3 opens (at ~1.053 ms). This implies that i_{B1} and i_{B2} become zero, and i_{A1} and i_{A2} become non-zero. This way, the power losses of the ICB after fault isolation are minimized as there is no current flowing through the MFBs.

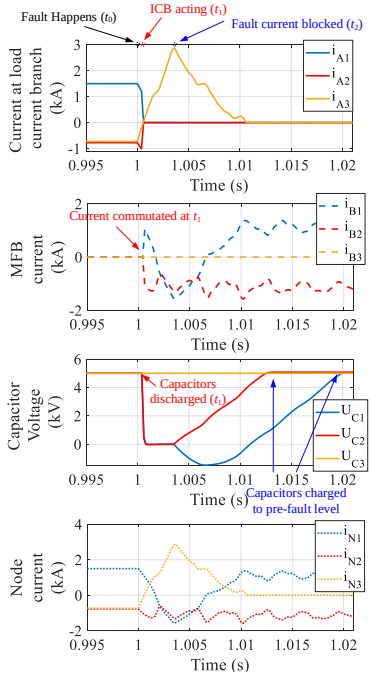


Fig. 21. System current and voltages (capacitors' voltage: 5 kV).

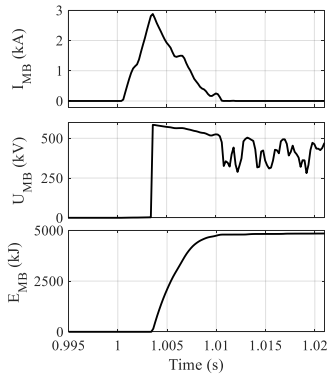


Fig. 22. Current, voltage and fault energy (capacitors' voltage: 5 kV).

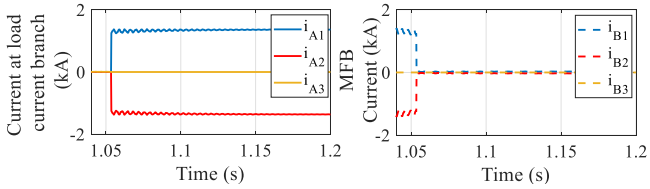


Fig. 23. Currents at healthy nodes (capacitors' voltage: 5 kV).

The simulation studies and analyses conducted in this and in the previous sections demonstrate the feasibility of the low-loss ICB concept for the protection of an HVDC system. However, significant effort is still required to deploy such a device in a practical project. To achieve this, a functional prototype is desirable so as to experimentally demonstrate the reliability and functionality of the presented ICB device. However, this falls out of the scope of this paper.

VI. Conclusion

An ICB with extremely low conduction losses has been presented in this paper. A distinctive feature of the device is the use of mechanical components in the load current branches. This way, conduction losses are reduced by 70 to 98% compared to other ICBs and HCBs, which employ LCSs at the load current branches. Instead, innovative MFBs are deployed at the supplementary branches to commutate current without introducing extra time delays. Therefore, the time to block fault current is comparable to other DCCB solutions, while the currents in healthy circuits remain unblocked throughout the duration of a fault event. The device may be further optimized by avoiding the inclusion of residual mechanical switches.

The voltage rating of the MFBs in the presented device is very small, and the charging process of their capacitors is fast and fully controllable. This is a unique feature compared to most active resonant DCCBs, whose capacitors will be charged to the voltage level of the system—hence taking a longer time.

To illustrate the successful operation of the ICB, simulations have been conducted in PSCAD/EMTDC, with results showing the capability of the device to isolate faults within a few milliseconds. For completeness, a detailed mathematical analysis has been presented to estimate the ratings of an ICB. It has been shown that the power losses of the device are significantly lower than those of an HCB. This further demonstrates the potential of the low-loss ICB towards practical deployment for the protection of HVDC systems.

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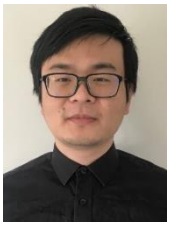

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