A Generalized Switched-Capacitor Step-up Multi-level Inverter Employing Single DC Source

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***Abstract*—In this paper, a new generalized step-up multilevel DC-AC converter is proposed, which is suitable for applications with low-voltage input sources such as photovoltaic power generation and electric vehicles. This inverter can achieve a high voltage gain by controlling the series-parallel conversion of DC power supply and capacitors. Only one DC voltage source and a few power devices are employed. The maximum output voltage and the number of output levels can be further increased through the switched-capacitor unit's extension and the submodule cascaded extension. Moreover, the capacitor voltages are self-balanced without complicated voltage control circuits. The complementary operating mechanism between each pair of switches simplifies the modulation algorithm. The inductive-load ability is fully taken into account in the proposed inverter. Additionally, a remarkable characteristic of the inverter is that the charging and discharging states among different capacitors are synchronous, which reduces the voltage ripple of the front-end capacitors. The circuit structure, the working principle, the modulation strategy, the capacitors and losses analysis are presented in detail. Afterwards, the advantages of the proposed inverter are analyzed by comparing with other recently proposed inverters. Finally, the steady-state and dynamic performance of the proposed inverter is verified and validated by simulation and experiment.**

***Index terms*— Multilevel inverter, switched capacitor, single DC source, voltage self-balancing, modulation strategy.**

I. Introduction

Nowadays, multilevel inverters (MLIs) have become a widespread power electronic equipment in energy conversion systems, such as renewable energy generation, electric vehicles (EVs) and motor drives [1]-[6]. Compared with the two-level inverter, MLIs can reduce the total harmonic distortion (THD) of the output voltage by increasing the number of output voltage levels. Additionally, they are widely considered for their merits in low device stress voltage, low electromagnetic interference and small output filter size [7], [8].

Conventional MLIs can be classified as: neutral point clamped (NPC) inverter [9], [10], flying capacitor (FC) inverter [11], [12] and cascaded H-bridge (CHB) inverter [13], [14]. However, NPC and FC have complicated topologies and face the challenge of bus capacitors voltage balancing [9], [11]. CHB inverters need multiple isolated DC power supplies when the output voltage levels increases [15]. In addition, numerous novel MLIs have been proposed to integrate more power sources and loads. The improvement of these MLIs focuses on increasing the output voltage levels, reducing the components, and simplifying the modulation strategy. Asymmetric multilevel inverters proposed in [14] and [16] use unbalanced DC voltage sources to reduce the number of power devices. However, multiple isolated DC sources are required to supply each conversion cell. Hybrid topologies, composed of different types of MLIs, such as NPC, FC and T-type, have been analyzed in [17]. These topologies can reduce the components, and therefore, reduce the capital cost. However, their modulation strategies are complicated.

In general, most of the DC voltage sources such as photovoltaic (PV) panels and batteries of EVs are in low-voltage [18]. However, traditional voltage-source inverters operate in the buck converter mode without the capability of voltage boosting [19]. Therefore, to achieve a desired AC output voltage in case of low-voltage DC supplies, one of the commonly used structures is to add a DC-DC boost converter to the front-end of the inverter. However, this two-stage structure leads to the increase of total losses and the decrease of efficiency [20].

Recently, to overcome the above-mentioned limitations that the inverter does not have independent boosting capabilities, MLIs integrating switched-capacitor (SC) have become an effective solution [21]-[24]. Switched-capacitor multilevel inverters (SCMLIs) are capable of producing a multilevel output voltage, which is several times of the DC input voltage thanks to the parallel charging and series discharging among the capacitors and DC power supplies. What's more, the capacitor voltage self-balancing can be achieved without complex voltage control circuits as the capacitors are always charged to a fixed voltage at specific phases of a period. Thus, the modulation strategy is simple. The MLI proposed in [22] combines the SC structure with the boost converter to achieve a considerable boosting capability. However, the inverter can only generate a five-level voltage which has a large harmonic

This work was supported in part by the National Natural Science Foundation of China under Grant 51507155, and in part by the Youth key Teacher Project of Henan Higher Educational Institutions under Grant 2019GGJS011. *(Corresponding author: Gen Li.)*

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content. In [23] and [24], the voltages of the two capacitors are charged to half of the DC source voltage to obtain a nine-level voltage. However, the maximum output voltage is only twice the input voltage, and the SC structures are fixed and difficult to extend.

To further increase the output voltage levels and the boost gain, many extended SCMLIs have been proposed. A seven-level inverter based on the front-end SC structure and back-end H-bridge is proposed in [25]. This inverter can increase the output level and boost gain through its cascade extension. However, each submodule still requires an independent DC voltage source. The SCMLIs based on extendable SC are proposed in [26]-[29]. Only one DC source and several capacitors are used in these topologies. The output voltage levels and boost gain can be flexibly configured by extending the number of the SC units. Moreover, the capacitor voltage self-balancing is achieved. However, the topologies proposed in [26]-[28] still have inherent shortcomings that numerous power switches are needed. The topology proposed in [29] can reduce switches with the sacrifice of limiting the capability of integrating inductive loads.

Considering the above-mentioned challenges, this paper presents a generalized step-up SCMLI suitable for applications with low-voltage input DC sources such as PVs and EVs. This topology increases the output voltage levels and boost gain by expanding the SC unit. It can be used as an independent inverter due to its ability to integrate inductive loads. Moreover, the voltage of capacitors is self-balanced without complicated voltage balancing control. In addition, the working states between each pair of switches are complementary, and therefore, simplify the modulation strategy.

In Section II, the topology of the proposed inverter is presented first. Then, the operating principle and modulation strategy of a nine-level inverter with three SC units are analyzed in detail. The capacitor voltage self-balancing, the capacitance determining, and power losses analysis are conducted in Section III. Section IV gives a comparative study of the proposed inverter and analyzes its cascaded extension. The effectiveness and feasibility of the proposed inverter are verified by simulation and experiment in Section V.

II. Proposed Generalized SCMLI

A. Circuit Description

The proposed generalized SCMLI is shown in Fig. 1. The topology consists of a single DC voltage source V_{dc}, an extendable switched capacitor circuit and two half-bridge circuits. All switches are IGBT or MOSFET with anti-parallel diodes. The switches S_{i1}, S_{i2} and diode D_i are used to control the series-parallel conversion of capacitors C_i (i =2, 3, ..., n). The capacitor C_1 is controlled by S_{12} and D_1. The switch S_0 will only be turned on when the inverter outputs 0 and $\pm V_{dc}$ to control the charging of capacitors. The switch pairs S_1 and S_2, S_3 and S_4 form two half-bridge circuits for completing the positive and negative polarity conversion of the output voltage. The output voltage levels of the proposed inverter are determined by the number of the SC units. By controlling the series-parallel conversion of the power supply and capacitors,

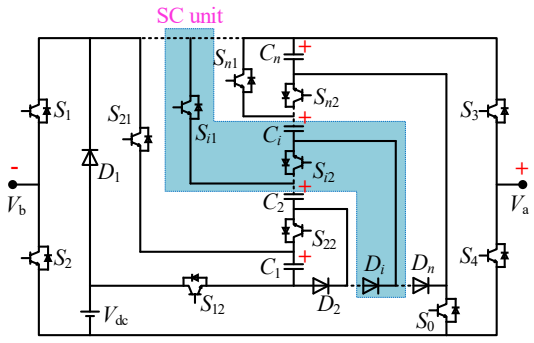


Fig. 1. Generalized topology of the proposed SCMLI.

the inverter with n SC units can output a total of $2n$+3 voltage levels, i.e., 0, $\pm V_{dc}$, $\pm 2V_{dc}$, …, $\pm(n+1)V_{dc}$. Moreover, the amplitude of the output voltage is (n+1) times of the DC input voltage. In this case, the number of required switches (N_{SW}), the diode (N_D), and the total standing voltage (TSV, which is the sum of the voltage stress on all switches) can be expressed as follows:

$$N_{SW} = 2n + 4, \tag{1}$$

$$N_D = n, \tag{2}$$

$$\mathrm{TSV} = 7n + 3. \tag{3}$$

B. Operating Principle

In this study, the proposed nine-level inverter (n=3) is taken as an example to analyze its operating principle. Figs. 2(a)~(i) shows the nine operating modes when the inverter outputs different levels. In order to simplify the analysis, the influences of parasitic parameters for devices and the circuit are ignored. The capacitance is assumed to be large enough that the voltage fluctuations are negligible. The analysis is based on the condition that the inverter has entered into a steady state.

Mode 1 (V_{ab}=+4V_{dc}): As shown in Fig. 2(a), the switches S_2, S_3, S_{12}, S_{22} and S_{32} are turned ON, whereas the other switches are turned OFF. The diodes D_1, D_2 and D_3 are reverse biased. The capacitors C_1, C_2 and C_3 are discharged in series with the power source.

Mode 2 (V_{ab}=+3V_{dc}): As shown in Fig. 2(b), the switches S_2, S_3, S_{12}, S_{22} and S_{31} are turned ON, the other switches are turned off. The diodes D_1 and D_2 are reverse biased, and the D_3 is forward biased. The capacitor C_3 is connected in parallel with C_2, and then C_2 and C_3 are discharged simultaneously in series with the power source V_{dc} and capacitor C_1.

Mode 3 (V_{ab}=+2V_{dc}): As shown in Fig. 2(c), the switches S_2, S_3, S_{12}, S_{21} and S_{31} are turned ON, the other switches are turned OFF. The diode D_1 is reverse biased, D_2 and D_3 are forward biased. The capacitors C_1, C_2, and C_3 are connected in parallel, and then they are discharged simultaneously in series with the power source V_{dc}.

Mode 4 (V_{ab}=+V_{dc}): As shown in Fig. 2(d), the switches S_0, S_2, S_3, S_{21} and S_{31} are turned ON, the other switches are turned OFF. The diodes D_1, D_2 and D_3 are forward biased. In this case, the capacitors C_1, C_2, and C_3 are connected in paral-

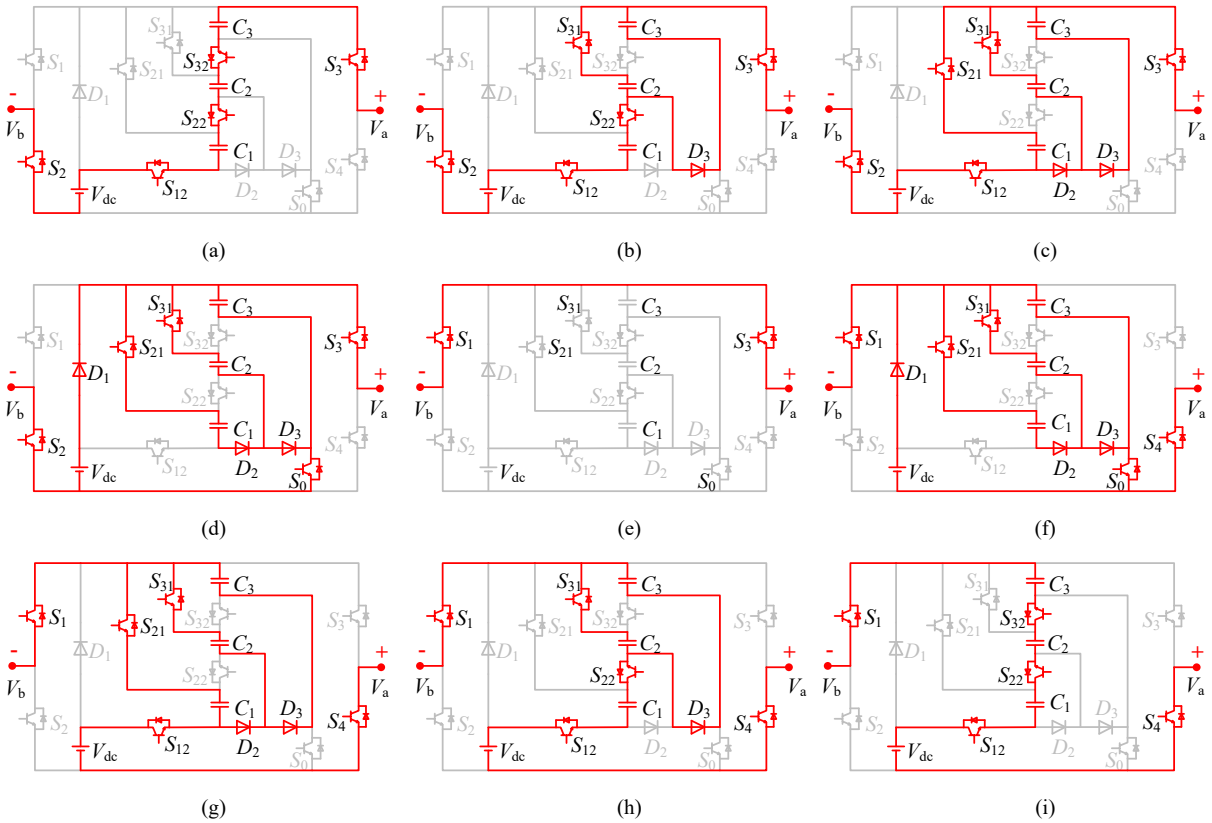


Fig. 2. Nine operating modes of the proposed nine-level inverter (n=3). (a) Mode 1, $V_{ab}=4V_{dc}$. (b) Mode 2, $V_{ab}=3V_{dc}$. (c) Mode 3, $V_{ab}=2V_{dc}$. (d) Mode 4, $V_{ab}=V_{dc}$. (e) Mode 5, $V_{ab}=0$. (f) Mode 6, $V_{ab}=-V_{dc}$. (g) Mode 7, $V_{ab}=-2V_{dc}$. (h) Mode 8, $V_{ab}=-3V_{dc}$. (i) Mode 9, $V_{ab}=-4V_{dc}$.

TABLE I
OPERATING STATES OF SWITCHES, DIODES AND CAPACITORS

Modes	Output voltage	ON-state switches and diodes	Capacitor states		
			C_1	C_2	C_3
1	$4V_{dc}$	S_2, S_3, S_{12}, S_{22}, S_{32}	D	D	D
2	$3V_{dc}$	S_2, S_3, S_{12}, S_{22}, S_{31}, D_3	D	D	D
3	$2V_{dc}$	S_2, S_3, S_{12}, S_{21}, S_{31}, D_2, D_3	D	D	D
4	V_{dc}	S_2, S_3, S_0, S_{21}, S_{31}, D_1, D_2, D_3	C	C	C
5	0	S_1, S_3, S_0, S_{21}, S_{31}, D_1, D_2, D_3	--	--	--
6	$-V_{dc}$	S_1, S_4, S_0, S_{21}, S_{31}, D_1, D_2, D_3	C	C	C
7	$-2V_{dc}$	S_1, S_4, S_{12}, S_{21}, S_{31}, D_2, D_3	D	D	D
8	$-3V_{dc}$	S_1, S_4, S_{12}, S_{22}, S_{31}, D_3	D	D	D
9	$-4V_{dc}$	S_1, S_4, S_{12}, S_{22}, S_{32}	D	D	D

The entry "C", "--", and "D" indicate that the capacitors are in charging, rest and discharging states, respectively.

lel with the power source. They are charged from the input voltage, and ($V_{C1}=V_{C2}=V_{C3}=V_{dc}$).

Mode 5 ($V_{ab}=0$): As shown in Fig. 2(e), the switches S_1, S_3, S_0, S_{21} and S_{31} are turned ON, the other switches are turned OFF. The diodes D_1, D_2 and D_3 are all turned on.

Similarly, when the inverter works in mode 6 ($V_{ab}=-V_{dc}$), mode 7 ($V_{ab}=-2V_{dc}$), mode 8 ($V_{ab}=-3V_{dc}$) and mode 9 ($V_{ab}=-4V_{dc}$) at the negative half-period, the operating states of the switches, diodes and capacitors in the SC circuit are the same as the mode 4 ($V_{ab}=V_{dc}$), mode 3 ($V_{ab}=2V_{dc}$), mode 2 ($V_{ab}=3V_{dc}$), and mode 1 ($V_{ab}=4V_{dc}$) at the positive half-period. However, to reverse the output voltage, the switching states of the switches in the two half-bridge circuits are changed from turning on S_2 and S_3 (S_1 and S_4 are turned off) to turning on S_1 and S_4 (S_2 and S_3 are turned off). The operating modes of the inverter in the negative half period are shown in Figs. 2(f)~(i). Table I shows the operating states of switches, diodes and capacitors when the proposed inverter operates in different modes. It can be seen from the table that the switches S_1 and S_2, S_3 and S_4, S_0 and S_{12}, S_{21} and S_{22}, S_{31} and S_{32} all work in pair switching modes, and the charging and discharging states of capacitors C_1, C_2 and C_3 are synchronous.

It should be noted that the red solid lines in Fig. 2 only represent the current paths of the inverter in the corresponding operating modes, and they do not represent whether the switches are turned on or off. The reason why the operating states of other switches are set as shown in Table II is to minimize the switching times of switches during the mode switching (mode 4/mode 5 and mode 5/mode 6) of the inverter and therefore, to reduce the switching losses.

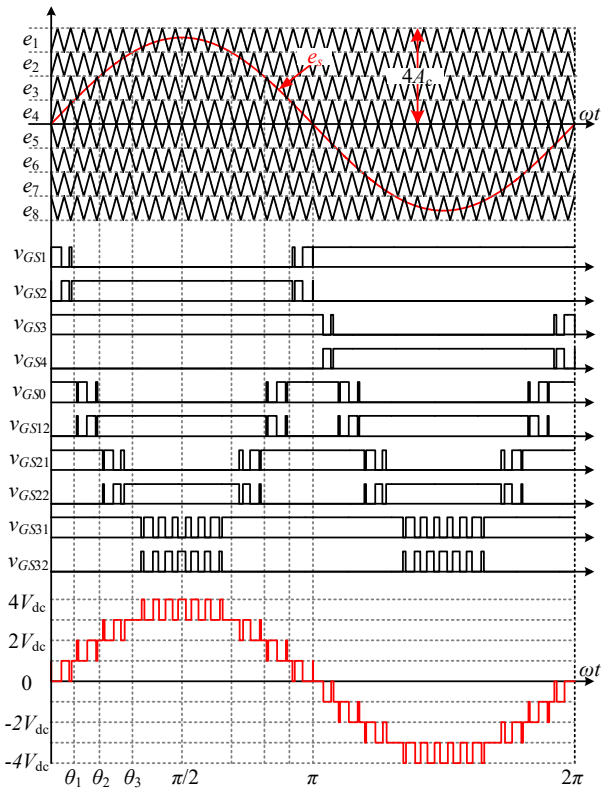


Fig. 3. PD-PWM control method for the proposed nine-level inverter (n=3).

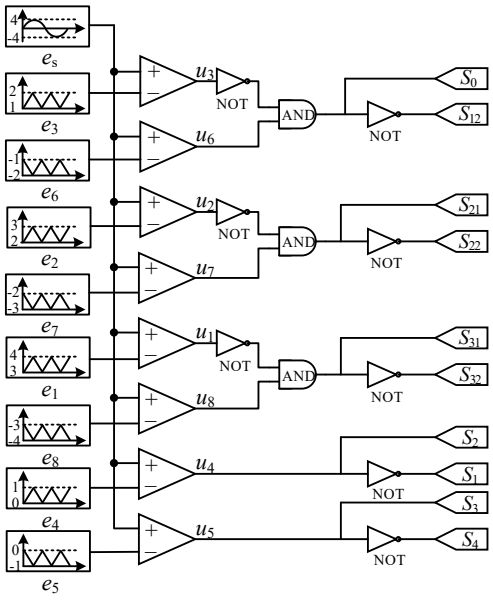


Fig. 4. Logic scheme for the proposed nine-level inverter (n=3).

C. Modulation Strategy

There are many modulation techniques, such as the space vector modulation (SVM) [7], [30], the selective harmonic elimination (SHE) [23], [31], and the phase disposition pulse width modulation (PD-PWM) [27], [28], which can be used to control multilevel inverters. In this study, considering its simple operation and a low THD, the phase disposition pulse width modulation (PD-PWM) is employed to analyze the modulation strategy of the proposed inverter.

Fig. 3 shows the PD-PWM control method of the proposed inverter. The eight triangular carrier waveforms e_1~e_8 with the same amplitude A_c and the same frequency f_c are sequentially stacked and compared with a sinusoidal reference waveform e_s=A_s·sin(2πf_{ref}) whose amplitude and frequency are A_s and f_{ref}. Then, the obtained 8-channel original pulse waveforms u_1~u_8 are combined with relevant logic to obtain gate pulse signals v_{GS1}~v_{GS32} to drive the switches. The specific logic scheme of the proposed inverter is shown in Fig. 4.

It is noted that some switch pairs working complementarily between two adjacent switches are used in the proposed inverter, i.e., the switch pairs S_1 and S_2, S_3 and S_4, S_0 and S_{12}, S_{21} and S_{22}, S_{31} and S_{32}. Therefore, in practical applications, a dead time must be set for the switch pairs to avoid damaging the power supply and capacitors when the operating modes of the inverter are switched.

In the PD-PWM method, the modulation index is determined by the amplitude of the carrier and reference waveforms. The modulation index M for the proposed inverter (n=3) can be expressed as

$$M = \frac{A_s}{4A_c}. \tag{4}$$

The range of M is 0<M≤1. The inverter outputs three levels when 0<M≤0.25, five levels when 0.25<M≤0.5, seven levels when 0.5<M≤0.75 and nine levels when 0.75<M≤1.

III. Capacitors and Losses Analysis

A. Capacitors Voltage Self-Balancing

Maintaining the voltage balance of the capacitors is important to ensure the reliable operation of the inverter. There are several approaches to maintain the balance of capacitor voltages: adopting separate DC sources; using auxiliary voltage balancing circuits; and selecting redundant switching states. For the proposed inverter, the capacitor voltages can achieve self-balancing inherently in each half period through the mechanism of parallel charging and series discharging between the switched-capacitors and power source.

As shown in Fig. 2 and Table I, the capacitors C_1, C_2 and C_3 are connected in parallel with the DC voltage source during the levels of 0 and ±V_{dc}. Considering that the parasitic resistance in each charging loop is very small, and therefore, the capacitors can be assumed to be instantaneously charged to the source voltage V_{dc}. It should be noted that the instantaneous charging of capacitors may cause some electromagnetic interference problems because of spike currents. Switches may even be burned if the spike current is too large. However, the spike current can be suppressed by adopting quasi-resonant inductors.

Conversely, when the inverter outputs other voltage levels, all the three pre-charged capacitors will discharge in series

with the DC voltage source. In this process, the voltage of the capacitors will continue to drop from their rated value (V_{dc}) until the next charging cycle. In other words, whenever the inverter outputs the level of $\pm V_{dc}$, the capacitor will be charged to the input voltage and therefore, there is no continuous voltage deviation. Hence, in the proposed inverter, capacitor voltage can achieve self-balancing in each half period without involving complex voltage control circuits as the capacitors are always charged to a fixed voltage at specific phases of a period.

B. Capacitance Determination

The continuous charging and discharging for capacitors may lead to voltage ripple. The quality of the output voltage waveform will be affected if the voltage ripple is too large. Therefore, it is important to determine a suitable capacitance to optimize the circuit volume and cost without affecting its performance.

Taking the proposed inverter (n=3) as an example. Fig. 2 and Table I show that the charging and discharging states of all capacitors in the inverter are synchronized. Therefore, when the inverter outputs $2V_{dc}$, $3V_{dc}$ and $4V_{dc}$ in the positive half-period, the capacitors C_1, C_2 and C_3 will have the same longest continuous discharging interval [θ_1, π-θ_1]. Moreover, the same continuous discharging interval also occurs in the negative half-period. In Fig. 3, the key modulation interval phase angles θ_1, θ_2 and θ_3 can be expressed as

$$\theta_1 = \arcsin\left(\frac{1}{4M}\right), \tag{5}$$

$$\theta_2 = \arcsin\left(\frac{1}{2M}\right), \tag{6}$$

$$\theta_3 = \arcsin\left(\frac{3}{4M}\right). \tag{7}$$

Therefore, the maximum continuous discharging amount ΔQ_{Ci} of the capacitor C_i (i = 1, 2, 3) can be calculated as

$$\Delta Q_{Ci} = \frac{1}{2\pi f_o}\int_{\theta_1}^{\pi-\theta_1} i_{Ci}\, d\omega t, \tag{8}$$

where f_o is the frequency of output voltage and i_{Ci} is the discharging current of capacitor C_i. It can be seen from Fig. 3 that the output voltage V_{ab} varies between V_{dc} and $2V_{dc}$ in the intervals [θ_1, θ_2] and [π-θ_2, π-θ_1], V_{ab} varies between $2V_{dc}$ and $3V_{dc}$ in the intervals [θ_2, θ_3] and [π-θ_3, π-θ_2]. V_{ab} varies between $3V_{dc}$ and $4V_{dc}$ in the interval [θ_3 π-θ_3]. The duty ratio of the output level in each modulation interval can be calculated as

$$D_{D1} = 4M\sin\omega t \qquad \omega t \in [0, \theta_1], \tag{9}$$

$$D_{D2} = 4M\sin\omega t - 1 \qquad \omega t \in [\theta_1, \theta_2], \tag{10}$$

$$D_{D3} = 4M\sin\omega t - 2 \qquad \omega t \in [\theta_2, \theta_3], \tag{11}$$

$$D_{D4} = 4M\sin\omega t - 3 \qquad \omega t \in [\theta_3, \pi - \theta_3]. \tag{12}$$

Due to the quadrant symmetry of the output voltage of the inverter, the duty ratio D_{D2} in the interval [θ_1, θ_2] is the same as the interval [π-θ_2, π-θ_1]. The load current and voltage will be step-pulse waveforms if the inverter load is pure resistive with a value of R_o. According to the operating mode 3 of the inverter in Fig. 2(d), the discharging currents of capacitors C_1, C_2 and C_3 are $2V_{dc}/(3R_o)$ when the output level is $2V_{dc}$. When the output level is $3V_{dc}$, the discharging current of capacitor C_1 is $3V_{dc}/R_o$ and the discharging currents of C_2 and C_3 are $3V_{dc}/(2R_o)$. When the output level is $4V_{dc}$, the discharging currents of capacitors C_1, C_2 and C_3 are $4V_{dc}/R_o$. Therefore, the maximum continuous discharging amount ΔQ_{Ci} of the capacitor C_i can be further calculated as

$$\begin{aligned}\Delta Q_{C1} = \frac{2}{2\pi f_o}\Bigg[&\int_{\theta_1}^{\theta_2} D_{D2}\frac{2V_{dc}}{3R_o}d\omega t + \int_{\theta_2}^{\theta_3}(1-D_{D3})\frac{2V_{dc}}{3R_o}d\omega t \\ &+\int_{\theta_2}^{\theta_3} D_{D3}\frac{3V_{dc}}{R_o}d\omega t\Bigg] + \frac{1}{2\pi f_o}\Bigg[\int_{\theta_3}^{\pi-\theta_3}(1-D_{D4})\frac{3V_{dc}}{R_o}d\omega t \\ &+\int_{\theta_3}^{\pi-\theta_3} D_{D4}\frac{4V_{dc}}{R_o}d\omega t\Bigg]\end{aligned}, \tag{13}$$

$$\begin{aligned}\Delta Q_{C2} = \Delta Q_{C3} = \frac{2}{2\pi f_o}\Bigg[&\int_{\theta_1}^{\theta_2} D_{D2}\frac{2V_{dc}}{3R_o}d\omega t + \int_{\theta_2}^{\theta_3}(1-D_{D3})\frac{2V_{dc}}{3R_o}d\omega t \\ &+\int_{\theta_2}^{\theta_3} D_{D3}\frac{3V_{dc}}{2R_o}d\omega t\Bigg] + \frac{1}{2\pi f_o}\Bigg[\int_{\theta_3}^{\pi-\theta_3}(1-D_{D4})\frac{3V_{dc}}{2R_o}d\omega t \\ &+\int_{\theta_3}^{\pi-\theta_3} D_{D4}\frac{4V_{dc}}{R_o}d\omega t\Bigg]\end{aligned}. \tag{14}$$

If the allowable voltage ripple of each capacitor cannot exceed 10% of its rated voltage, the capacitance of the capacitor in the inverter should satisfy

$$C_i \geq \frac{\Delta Q_{Ci}}{0.1V_{dc}}. \tag{15}$$

Based on the above analysis, the three capacitors are discharged simultaneously because the charging and discharging states of different capacitors in the proposed inverter are synchronous. For instance, with an output level of $2V_{dc}$ of the proposed inverter, capacitors C_2 and C_3 share 2/3 of the discharging amount for capacitor C_1. Therefore, compared with the solution in [29] which uses a single capacitor C_1 to provide all the discharging amount to achieve the same output $2V_{dc}$. The proposed inverter alleviates the large discharging amount of front-end capacitors and therefore, reduces their voltage ripples. In fact, the discharging amount of different capacitors in the proposed inverter are almost the same. Therefore, capacitors with the same capacitance should be selected for practical applications.

From the above analysis, it can be seen that the continuous discharging period of capacitors is at the scale of a modulation cycle in the proposed inverter. Therefore, to limit the voltage ripple of capacitors and maintain the self-balancing voltage, a larger capacitance is needed compared with the inverter proposed in [32]-[33], which can achieve the voltage balance in a switching period. However, it should be emphasized that the number of output voltage levels and high boost gain are the advantages of the proposed inverter in this paper. Moreover, according to (15), the capacitors with a large capacitance help reduce the voltage ripples, but it may affect the power density,

dimension and cost of the inverter. Therefore, in practical applications, the selection of the capacitors should be a trade-off between technical performance and power density, dimension and cost, which requires an optimal design. However, it should be highlighted that the parameter optimization design, although highly desirable to verify its performance, falls out of the scope of this work.

C. Power Losses Analysis

1) Switching Losses: The switching losses of the inverter can be calculated according to the charging and discharging processes of the parasitic capacitor in the switching devices. Based on the theory in [34], it is assumed that the capacitance of the parasitic capacitor is linear. When the switches are turned off, the voltage of the parasitic capacitor C_S is gradually charged from 0 to V_T, where V_T is the approximated maximum block voltage (MBV) of power switches. The MBV of each power switch in the proposed inverter is shown in Table II. When the switches are turned on, the parasitic capacitor is short-circuited with the on-resistance of the switching device, and all the electric energy stored inside C_S is consumed by the internal resistor in the form of heat. The energy losses of the power switches during each switching cycle can be expressed as

$$E_{SW} = C_S V_T^2 . \tag{16}$$

TABLE II
THE MBV OF EACH SWITCH IN THE PROPOSED INVERTER

Switches	S_{12}, S_{21}, S_{22}, S_{31}, S_{32}	S_0	S_1, S_2, S_3, S_4
MBV	V_{dc}	$3V_{dc}$	$4V_{dc}$

Therefore, the switching losses of the power switches can be calculated as

$$P_{SW} = C_S V_T^2 f_S . \tag{17}$$

where f_S is the equivalent switching frequency. According to Fig. 3, in the intervals [0, θ_1] and [π-θ_1, π], the switch S_1 is repeatedly turned ON or OFF. In other intervals, the switch S_1 remains ON or OFF. Therefore, the average number of switching transitions $\overline{N_{S1}}$ in one period of the reference waveform is calculated as

$$\overline{N_{S1}} = \frac{2\theta_1}{2\pi}\cdot\frac{f_c}{f_{ref}} = \frac{\arcsin\left(\frac{1}{4M}\right)}{\pi}\cdot\frac{f_c}{f_{ref}} . \tag{18}$$

From (18), the average number of switching transients is determined by the frequency modulation index f_c/f_{ref}. Due to the symmetry of the drive waveform of switches, the average number of switching transients of the switches S_2, S_3 and S_4 are the same as S_1. Therefore, the equivalent switching frequency f_{Sk} of the switches S_k (k = 1, 2, 3, 4) is

$$f_{Sk} = \overline{N_{S1}}\cdot f_{ref} = \frac{\arcsin\left(\frac{1}{4M}\right)}{\pi}\cdot f_c . \tag{19}$$

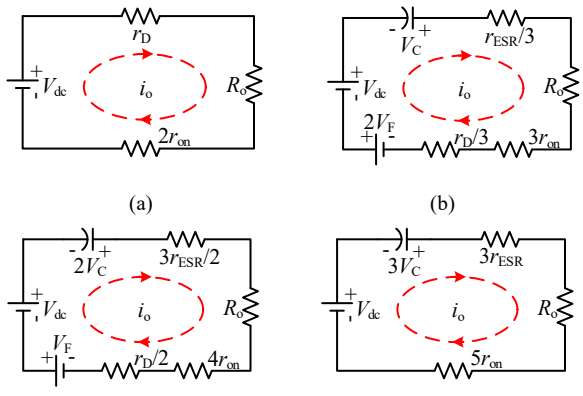


Fig. 5. Equivalent discharging current path for each operating state. (a) V_{ab}=±V_{dc}. (b) V_{ab}=±2V_{dc}. (c) V_{ab}=±3V_{dc}. (d) V_{ab}=±4V_{dc}.

TABLE III
EQUIVALENT PARASITIC PARAMETERS IN EACH OPERATING STATE

j	$V_{ab,j}$	$V_{Deq,j}$	$r_{eq,j}$
1	±V_{dc}	V_F	$2r_{on}$+r_D
2	±2V_{dc}	2V_F	$3r_{on}$+r_D/3+r_{ESR}/3
3	±3V_{dc}	V_F	$4r_{on}$+r_D/2+3r_{ESR}/2
4	±4V_{dc}	0	5r_D+3r_{ESR}

According to equation (19), the switching losses of the switches P_{Sk} are given as

$$P_{Sk} = 16 C_s V_{dc}^2 f_c \cdot \frac{\arcsin\left(\frac{1}{4M}\right)}{\pi} . \tag{20}$$

The same argument can be applied to other switches, and their switching losses can be calculated as

$$P_{S0} = 9P_{S12} = 9 C_s V_{dc}^2 f_c \cdot \frac{2\arcsin\left(\frac{1}{2M}\right) - 2\arcsin\left(\frac{1}{4M}\right)}{\pi} . \tag{21}$$

$$P_{S21} = P_{S22} = C_s V_{dc}^2 f_c \cdot \frac{2\arcsin\left(\frac{3}{4M}\right) - 2\arcsin\left(\frac{1}{2M}\right)}{\pi} . \tag{22}$$

$$P_{S31} = P_{S32} = C_s V_{dc}^2 f_c \cdot \frac{\pi - 2\arcsin\left(\frac{3}{4M}\right)}{\pi} . \tag{23}$$

As a result, based on equations (20)-(23), the total switching losses of the proposed inverter are as follows:

$$P_{SW} = 4P_{Sk} + 10P_{S12} + 2P_{S_{21}} + 2P_{S_{31}} . \tag{24}$$

2) Conduction Losses: The conduction losses of the inverter are caused by the parasitic parameters of switching devices and capacitors. Fig. 5 shows the equivalent discharging current path in each operating state of the proposed inverter

(n=3). The parasitic parameters of the equivalent circuit path are listed in Table III, wherein V_{ab}, V_{Deq}, r_{eq} and R_o are the output voltage, the equivalent voltage drop of the diode, the equivalent parasitic resistance of the power devices and the load resistance, respectively. In order to simplify the analysis, some assumptions are made: all switches have the same on-state internal resistance r_{on}, and all diodes including the parallel diodes of switches have the same forward voltage drop V_F and internal resistance r_D and all capacitors have the same equivalent series resistance r_{ESR}.

From the above analysis, the total conduction losses of the inverter can be calculated as

$$P_{Cond}=\frac{2}{\pi}\sum_{j=1}^{4}\left\{\begin{bmatrix}(V_{ab,j}-V_{Deq,j})/(r_{eq,j}+R_o)\end{bmatrix}^2\times r_{eq,j}\times \begin{bmatrix}D_{Dj}\cdot(\theta_j-\theta_{j-1})+(1-D_{Dj+1})(\theta_{j+1}-\theta_j)\end{bmatrix}\right\}. \quad (25)$$

where D_{Dj} (j=1, 2, 3, 4) is the duty ratio of each modulation interval in equations (9)-(12), and D_{D5}=1.

3) Ripple Losses: The ripple losses of SCMLIs are caused by the fluctuations of capacitor voltages. From (8), the voltage ripples of the capacitors ΔV_{Ci} can be obtained by

$$\Delta V_{Ci}=\frac{1}{2\pi f_o C_i}\int_{\theta_2}^{\pi-\theta_2} i_{Ci}\,d\omega t\,. \quad (26)$$

Therefore, the ripple losses P_{Rip} of the proposed inverter can be calculated as

$$P_{Rip}=2\sum_{i=1}^{3} C_i\Delta V_{C_i}^2 f_o\,. \quad (27)$$

Finally, based on equations (24), (25) and (27), the total losses P_{Loss} and efficiency η of the proposed inverter can be calculated as

$$P_{Loss}=P_{SW}+P_{Cond}+P_{Rip}\,, \quad (28)$$

$$\eta=\frac{P_{out}}{P_{in}}=\frac{P_{out}}{P_{out}+P_{Loss}}\,, \quad (29)$$

where P_{in} and P_{out} are the input and output power of the proposed inverter, respectively.

IV. Topology Comparisons and Cascaded Extension

A. Comparative Study

In this section, in order to illustrate the pros and cons of the proposed inverter, a comprehensive comparison with other well-known SCMLIs in [25]-[29] has been made with the consideration of ($2m$+1) output voltage levels or m steps. As shown in Table IV, the comparison mainly focuses on the numbers of DC sources, capacitors, switches and diodes. In addition, the boost gain, the H-bridge's stress, and the inductive load ability are compared in detail as well. The comparison results of the number of power devices, including switch tubes and diodes, are further depicted in Fig. 6.

The switched capacitor structure proposed in [25] is inextensible and the number of output levels can only be increased by its cascaded extension. Although this extended structure with multiple input sources can reduce the number of capacitors, its boost gain is a constant 3 that cannot be further enhanced through extension. Compared with the topology in [25], the proposed generalized topology and the topologies in [26]-[29] with modular SC structure have more flexibility. The output voltage levels and the boost gain can be linearly increased with the modular extension of SC units.

TABLE IV
Comparison with Other Topologies

Parameters	[25]	[26]	[27]	[28]	[29]	Proposed
Num. of DC sources	$m/3$	1	1	1	1	1
Num. of capacitors	$2m/3$	m-1	m-1	m-1	m-1	m-1
Num. of switches	$8m/3$	$3m$+1	$5m$-1	$3m$+1	m+4	$2m$+2
Num. of diodes	$2m/3$	0	0	0	$2m$-2	m-1
Boost Gain	3	m	m	m	m	m
H-bridge's stress	$3V_{dc}$	mV_{dc}	V_{dc}	mV_{dc}	mV_{dc}	mV_{dc}
Inductive-load ability	YES	YES	YES	YES	NO	YES

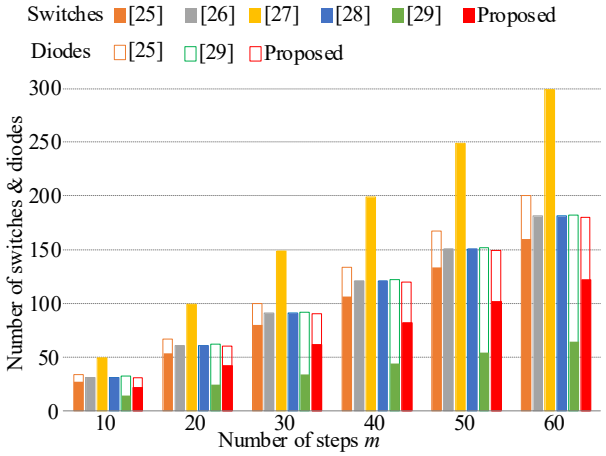


Fig. 6. Comparison for number of power devices in terms of number of steps.

According to Table IV and Fig. 6, another advantage of the proposed topology is that the number of its power devices, especially switches, is reduced compared to topologies in [26]-[28]. The reduction of switches helps reduce the use of drive circuits, which will be beneficial to reduce the system volume, cost and modulation complexity. The topology in [29] uses the minimum power switches compared with other topologies. However, the capacity of integrating inductive loads is severely limited because the topology employs a large number of diodes, which blocks the channel for feedback current from the ac output side to the dc input side.

Compared with the topology in [27], the proposed topology and the topologies in [26], [28] and [29] have a common disadvantage that the four switches in the H-bridge have to withstand the voltage stress accumulated by the SC boost circuit. However, the topology in [27] uses a large number of switches to reduce the voltage stress on switches.

Based on the above comparison, the proposed inverter has considerable advantages in many performances, such as the flexibility of the extension structure, the number of power devices, the boosting capacity and the capability of integrating

inductive loads. In addition, the proposed inverter is suitable for medium and low voltage applications because an H-bridge is used in this topology to convert the output voltage polarity. This inverter can be used for high voltage applications through its cascaded extension.

B. Cascaded Extension

The proposed inverter can be used in high voltage applications through its cascaded extension. Fig. 7 demonstrates the extended structure cascaded by k seven-level submodules (n=2).

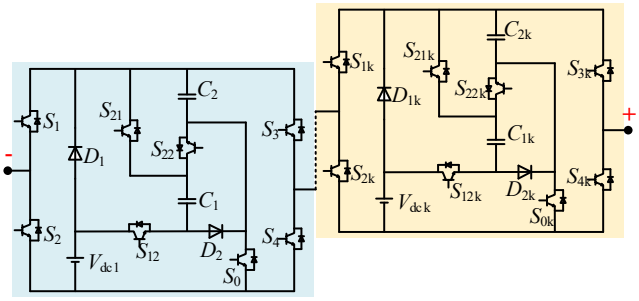


Fig. 7. Cascaded extension of the proposed inverter.

This extended structure is more suitable for applications with multiple isolated DC power sources, such as photovoltaic power generation. Similar to other cascaded inverters, the proposed cascaded extension also has two forms: symmetric and asymmetric. Considering high voltage applications, this study only analyses the symmetrical form, i.e., V_{dc1}=V_{dc2}= … =V_{dck}=V_{dc}. In this configuration, the capacitors C_{1i} and C_{2i} (i=1, 2, …, k) in each submodule have synchronized charging and discharging states. Meanwhile, the charging voltage of all capacitors is equal to the DC input voltage V_{dc}. Therefore, for k submodules, the number of required capacitors (N_C), switches (N_{SW}), diodes (N_D), and generated voltage levels (N_{Level}) can be obtained as:

$$N_C = 2k\,, \tag{30}$$

$$N_{SW} = 8k\,, \tag{31}$$

$$N_D = 2k\,, \tag{32}$$

$$N_{Level} = 6k+1\,. \tag{33}$$

Due to the boosting capacity of the SC unit, the switches S_{1i}~S_{4i} have to withstand the maximum block voltage of $3V_{dc}$. However, this maximum voltage is constant and will not increase with the cascaded extension, which occupies an advantage compared to the topologies in [35] and [36] where two switches need to bear cumulative voltage stress.

V. Simulation and Experimental Results

A. Simulation Results

To verify the effectiveness of the proposed SCMLI and evaluate its performance, a simulation model of a nine-level inverter (n=3) is constructed in MATLAB/Simulink software platform. The specific simulation parameters are shown in Table V. Fig. 8 shows the steady state and the dynamic simulation results when the load changes.

The steady-state simulation results of the proposed inverter are shown in Figs. 8(a)~(c). Fig. 8(a) is the output voltage and load current waveforms of the inverter with pure resistive load (R=50 Ω). Both the voltage and current exhibit sinusoidal

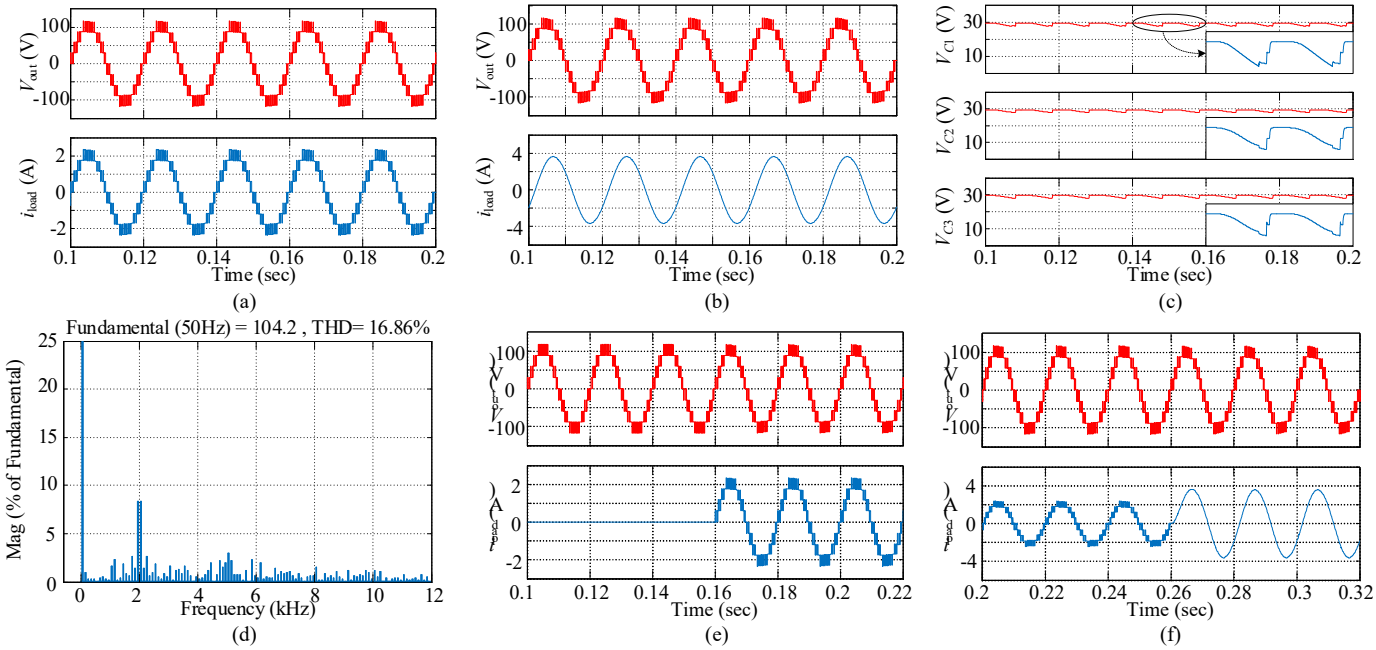


Fig. 8. Simulation results of steady state and dynamic. (a) Output voltage and load current with the pure resistive load. (b) Output voltage and load current with the resistive-inductive load (cosφ=0.85). (c) Capacitor voltage. (d) THD of the output voltage. (e) Output voltage and load current when load changes from no load to R=50 Ω. (f) Output voltage and load current when load changes from R=50 Ω to R=25 Ω & L=50 mH.

TABLE V
SIMULATION PARAMETERS

Parameters	Values
Input Voltage (V_{dc})	30 V
Capacitors (C_1, C_2, C_3)	2200 μF
Carrier Frequency (f_c)	2 kHz
Modulation Index (M)	0.9
Output Frequency (f_o)	50 Hz
Resistive Load (R)	50 Ω
Resistive-Inductive Load (R-L)	25 Ω & 50 mH

staircase waveforms with nine levels. The amplitude of the output voltage is 120 V which is four times of the DC input voltage. Fig. 8(b) shows the output voltage and load current waveforms of the inverter with resistive-inductive load (R=25 Ω, L=50 mH, cosφ=0.85). The load current waveform is much smoother owing to the filtering effect of the inductive load. The phase difference between the output voltage and load current demonstrates the inverter's ability to integrate inductive loads. In this inverter, bidirectional switching devices have been used to achieve a bidirectional current. The negative current can be absorbed by the buffer DC capacitors within the DC voltage source. For instance, by the DC capacitor of the DC-DC converter of the PV panel. The voltage waveforms of capacitors C_1, C_2 and C_3 are shown in Fig. 8(c). It can be seen that the charging voltage of the three capacitors is 30 V. The voltage fluctuations exhibit periodically, which proves the voltage self-balancing ability of the selected capacitors. The fast Fourier transform (FFT) of the output voltage is given in Fig. 8(d) which shows that THD is 16.86% and the harmonics are mainly distributed at the fundamental frequency of the carrier frequency.

Furthermore, the dynamic simulation results for load changes are given in Figs. 8(e) and (f). It can be seen that the output voltage is almost unaffected during the load transient. Moreover, the load current is changed instantaneously when the load changes from no load to a purely resistive load R=50 Ω and then to a resistive-inductive load of R=25 Ω & L=50 mH. Then, the inverter becomes stable gradually. It should be mentioned that the tests are conducted under an open loop control which aims to validate the effectiveness of the proposed inverter by emulating the changing of system operating conditions.

B. Experimental Results

To further validate the effectiveness and feasibility of the proposed inverter in terms of steady-state and dynamic performance, an experimental prototype of a nine-level inverter (n=3) has been constructed as shown in Fig. 9. The specifications of experimental components are listed in Table VI. In order to correspond to simulation results, the experimental parameters are consistent with the simulation parameters.

Fig. 10 shows the steady-state experimental results of the inverter (n=3). The output voltage and load current waveforms under a purely resistive load condition (R=50 Ω) are shown in

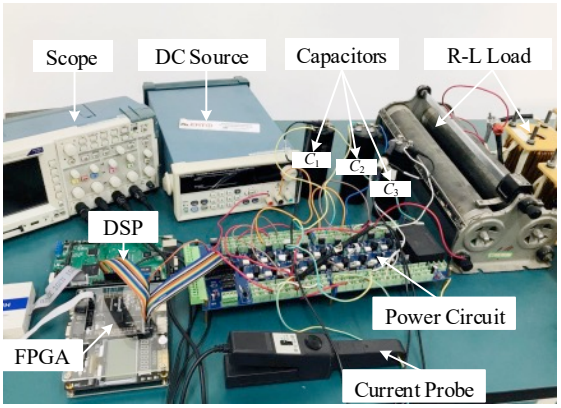


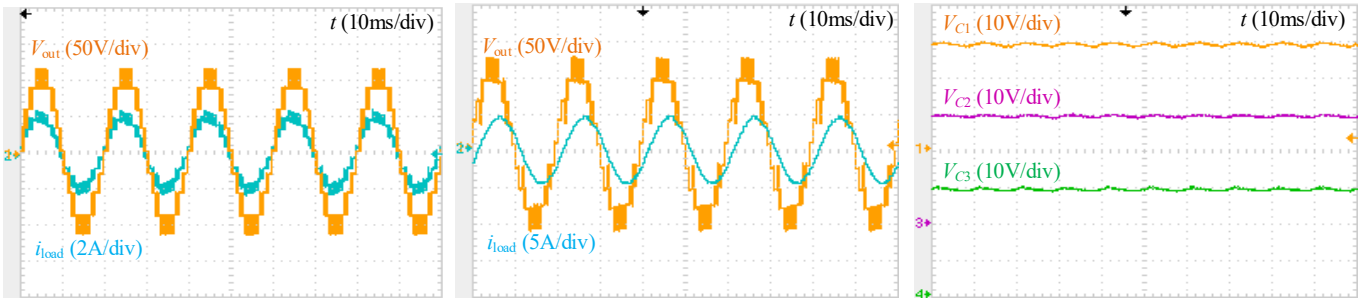
Fig. 9. Experimental prototype of the proposed inverter (n=3).

TABLE VI
SPECIFICATIONS OF EXPERIMENTAL COMPONENTS

Components	Specifications
Main control chips	TMS320F28335+EP4CE15
MOSFET	SPP20N60C3
Diode	MBR20200CTG
Optocoupler	HCPL-4504
Driver	UCC27516

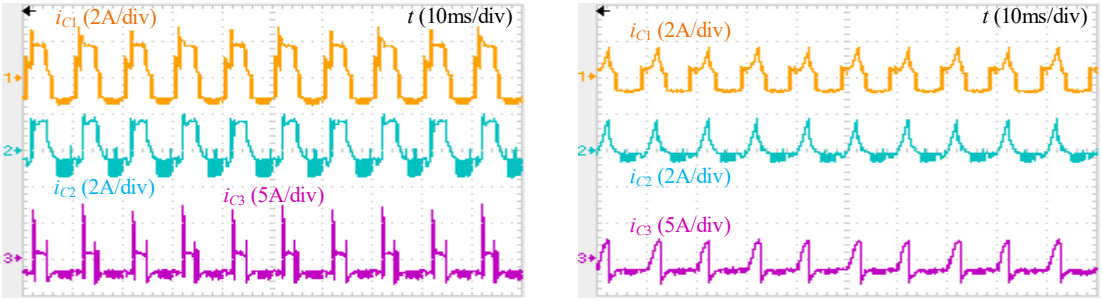
Fig. 10(a). The waveforms show that the amplitude of the output voltage is 118.2 V. This value is slightly lower than the theoretical value of 120 V, which is mainly caused by the voltage drop of power switches and diodes. The load current also exhibits nine levels with an amplitude of 2.34 A. Under this output power condition, the conversion efficiency of the proposed inverter is 93.9%, which is higher than 90.6% of the topology in [26] under the same experimental condition. Fig. 10 (b) shows that the output voltage and the load current waveforms under a resistive-inductive load condition (R-L=25 Ω & 50 mH). The amplitude of the output voltage is 117.6 V, and the load current exhibits a sinusoid with an amplitude of 4.12 A. The efficiency of the proposed inverter is 93.5%, which is still higher than the 90.1% of the topology in [26]. Fig. 10(c) shows that the voltage waveforms of three capacitors. Their voltage varies from 27.6 V to 29.4 V, and the difference can be neglected. The simulation and experimental results show good agreement, which verifies the effectiveness of the proposed inverter topology and its modulation strategy.

Meanwhile, the current waveforms of capacitors are also shown in Fig. 11(a). It can be seen that the spike current will be generated when capacitors are charged. Among the three capacitors, the peak current of C_3 is the largest and the peak value reaches 7.5 A, which is caused by the minimum internal resistance of the devices in the charging path. The spike current can be suppressed by adding a quasi-resonant inductor in the charging path of capacitors. Considering the quasi-resonant condition and the damping effect of parasitic impedances, an inductor of 0.5 mH is connected in series with the switch S_0. The current waveforms of the capacitors with the quasi-resonant inductor are shown in Fig. 11(b). It can be seen



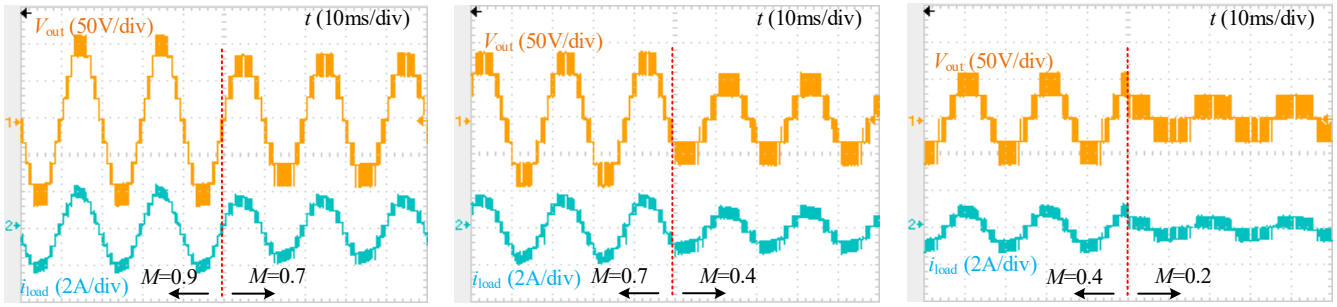
(a) (b) (c)

Fig. 10. Steady-state experimental results of the inverter. (a) V_{out} and i_{load} with resistive load. (b) V_{out} and i_{load} with resistive-inductive load (cosφ=0.85). (c) Voltage waveforms of the capacitors.



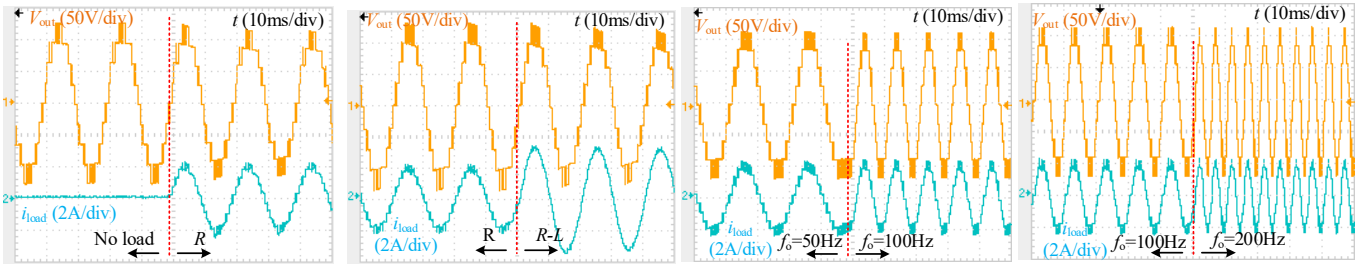
(a) (b)

Fig. 11. Experimental results of the capacitors' currents. (a) without quasi-resonant inductor. (b) with quasi-resonant inductor.



(a) (b) (c)

Fig. 12. Dynamic experimental results. (a) change of M from 0.9 to 0.7, (b) change of M from 0.7 to 0.4 and (c) change of M from 0.4 to 0.2.

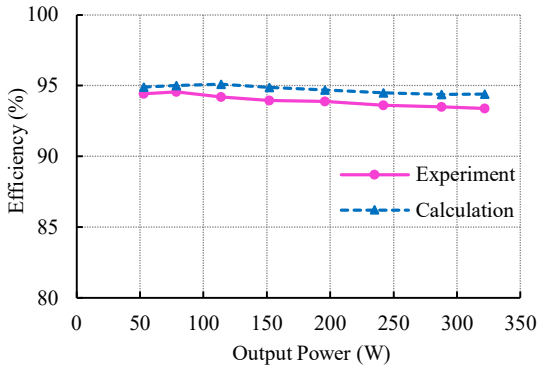


(a) (b) (c) (d)

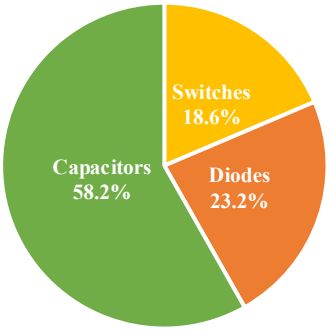
Fig. 13. Dynamic experimental results. (a) change of load from no load to R=50 Ω, (b) change of load from R=50 Ω to R=25 Ω & L=50 mH, (c) change of output frequency f_o from 50 Hz to 100 Hz, and (d) change of f_o from 100 Hz to 200 Hz.

that the peak current of capacitors is effectively suppressed, which is beneficial to reduce the EMI issue and prolong the capacitor lifetime.

Additionally, several experiments have been performed to test the inverter's dynamic performance under different dynamic conditions which include the changes of modulation index, load condition and output frequency. Fig. 12 shows the experimental waveforms when the modulation index M changes. It can be seen that in the process that the M is gradually reduced from a high modulation index (M=0.9) to a low modulation index (M=0.2), output voltage level changes from nine-level to three-level gradually and the load current also decreases accordingly. Moreover, the waveforms quickly recover to the steady state after these changes. These results fulfill the theoretical analysis and design requirements. Figs. 13(a)~(b) shows the output voltage and load current wave-



(a)



(b)

Fig. 14. Efficiency and power losses analysis. (a) Efficiency curve of the proposed inverter (n=3). (b) Power losses distribution.

forms when the load changes from no load to a purely resistive load R=50 Ω and then to a resistive-inductive load R=25 Ω & L=50 mH. It can be seen that the dynamics observed from the experiment are almost the same as the simulations. Figs. 13(c)~(d) shows the experimental waveforms when the inverter's output frequency f_o changes from 50 Hz to 100 Hz and then to 200 Hz. The output voltage and load current waveforms quickly recover to a steady state after f_o changes, which proves that the inverter can operate in a wide range of output frequency. The above experiment results show that the output voltage and the load current of the proposed inverter can react and enter the steady state quickly in different dynamic scenarios.

The efficiency curves under experiment and calculation of the proposed inverter (n=3) against the output power are shown in Fig. 14(a). It can be observed that the maximum experiment efficiency of the proposed inverter has a value of 94.6% within the measured output power range. For comparison, the calculated maximum efficiency using the same experimental parameters (V_{dc}=30 V, f_o=50 Hz, r_{on}=0.19 Ω, V_F=0.8 V, r_{ESR}=60 mΩ and R_{load}=50 Ω) is 95.1%. The efficiency has a slight decrease as the output power increases, which is caused by the increased capacitor voltage ripple. The losses distribution is measured and depicted in Fig. 14(b). It can be seen that the capacitor losses, consisting of voltage ripple losses and conduction losses, account for a large proportion of the total power losses. Therefore, capacitors with a large capacitance are beneficial to improve efficiency, which must be optimally designed with the consideration of system volume and capital cost.

VI. Conclusion

A generalized single-input SCMLI has been presented in this paper with the ability of voltage boosting and integrating inductive-loads. This inverter can achieve more output levels and a high boost gain by extending the SC units. Therefore, it is suitable for applications with low-voltage input sources such as PVs and EVs. The operating principle of the proposed nine-level inverter (n=3) indicates that the capacitors are equipped with the inherent voltage self-balancing capability. Moreover, the characteristics of the switch pairs simplify the inverter modulation algorithm. As the charging and discharging states among different capacitors in the proposed topology are synchronous, the voltage ripples of the front-end capacitors are reduced. The proposed method of determining the capacitance provides a theory for selecting optimal capacitors. Compared with other recently proposed SCMLIs, the proposed inverter reduces the power devices considering the capability of integrating inductive loads. Simulation and experimental results prove that the proposed SCMLI has excellent steady-state and dynamic performance. It should be mentioned that the proposed inverter has a limitation which is that the four switches in the H-bridge must withstand the voltage stress accumulated by the SC boost circuit. Therefore, the proposed inverter is suitable for medium and low voltage applications with the possibility of high voltage applications through its cascaded extension.

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