Analysis and Mitigation of DC Voltage Imbalance for Medium-Voltage Cascaded Three-level Neutral-Point-Clamped Converters

Jinlei Chen, Wenlong Ming, *Member, IEEE*, Carlos E. Ugalde-Loo, *Senior Member, IEEE*, Sheng Wang, *Member, IEEE*, and Nick Jenkins, *Fellow, IEEE*

***Abstract*- The cascaded three-level neutral-point-clamped (3L-NPC) converter and the modular multi-level converter (MMC) are attractive solutions for medium-voltage direct-current (MVDC) applications. Due to their low cost compared to MMCs, cascaded 3L-NPC converters have been adopted in ANGLE-DC—a 30 MVA MVDC link demonstration project in North Wales, UK. DC voltage imbalance across submodules (SMs) is a common challenge for both types of MVDC converters. Such imbalance is topology dependent and remains under-researched for cascaded 3L-NPC converters. In this paper, small-signal model-based analysis has been done to reveal that the dc voltage imbalance in cascaded 3L-NPC converters is caused by an unstable system pole. Two voltage balancing methods are presented. The first method is based on PI controllers to precisely regulate SMs' voltages without influencing output power. However, it relies on communication between a central controller and local controllers within SMs. The second method uses inverse-droop based control to take over the dc voltage regulation upon loss of communication. Both balancing methods are experimentally validated using a 30 kVA testbed based on the ANGLE-DC project. It has been demonstrated that the dc voltages of SMs can be effectively balanced with both methods during changes of load conditions and dc bus voltages.**

***Index Terms*- medium-voltage direct-current, cascaded three-level neutral-point-clamped converters, voltage imbalance.**

I. Introduction

Distributed generators and energy storage devices are being more frequently incorporated into distribution networks, but their effective integration requires flexible and precise control of power flows. Medium-voltage direct-current (MVDC) technology is a recent development offering good controllability of power flows, enhanced power transfer capability and, hence, a better control of network voltages. However, this is at the expense of the additional capital cost of using MVDC converters, an added complexity in system operation and the possible introduction of harmonics [1], [2].

To date, a few practical MVDC links have been built [3]-[6]. At Eagle Pass (Texas, USA), a ± 16 kV voltage source converter (VSC) based dc link was built in 2003 to interconnect two distribution networks [3]. At Tangjiawan (Zhuhai, China), a three-terminal ± 10 kV MVDC project was trialed in 2018 [4]. At Exebridge (South West England, UK), through the Network Equilibrium project, a "Flexible Power Link" consisting of two back-to-back VSCs was constructed in 2014 to connect two 33 kV distribution networks [5]. In North Wales, UK, the ANGLE-DC project was launched in 2017 to adapt a medium-voltage ac (MVAC) circuit for MVDC operation. By converting an existing twin ac circuit at 33 kV to ± 27 kV dc, the power transfer capacity between the island of Anglesey and Bangor (mainland) can be increased by more than 23%, enabling more distributed generation to be connected on the island [6].

Although the adoption of an MVDC link offers advantages, the challenges that come with its introduction are worthy of attention [7]. As more distributed generation and loads are connected through power electronic devices, the system inertia will decrease and frequency instability may appear [7]. Harmonic and reliability issues also arise from using power converters [7], [8]. In medium-voltage (MV) applications, since a single two/three level converter cannot withstand the voltage level, multilevel topologies are required. Among them, those using cascaded modular converters are preferred due to their exceptional waveform quality, compact and modular design [9].

For cascaded modular converters, a significant challenge is that the total dc voltage should be divided equally for each submodule (SM) [10]. Two main cascaded modular converter topologies are available for MV levels: the modular multilevel converter (MMC) [11] and the cascaded three-level neutral-point-clamped (3L-NPC) converter [12]. The ANGLE-DC project uses cascaded 3L-NPC converters, where the dc connection of each SM is in series to establish the dc link voltage. This topology uses mature technologies employed for MV motor drives and has a relatively low cost and a small footprint [12]. The low cost is the main reason for using the cascaded 3L-NPC converters in ANGLE-DC although MMCs have other advantages. Detailed comparison of both types of converters is discussed in [9], where the total cost of the ownership (TCO), return on investment, reliability, and efficiency are considered. The TCO of a set of cascaded 3L-NPC converters is \$867,535 which is much lower compared with \$1,045,470 for the MMC. Reliability and efficiency requirements can be also met with a 3L-NPC converter, although the performance in these two areas is inferior to an MMC [6], [9]. The potential low cost using the cascaded 3L-

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J. Chen, W. Ming, C. E. Ugalde-Loo, S. Wang and N. Jenkins are with the School of Engineering, Cardiff University, Cardiff, CF24 3AA (e-mail: ChenJ111, MingW, Ugalde-LooC, WangS9, JenkinsN6@cardiff.ac.uk)

NPC can be considered as an attractive factor for its adoption in more practical projects.

Although there are publications addressing the control of a single 3L-NPC converter (e.g. [13]-[17]), the dc voltage imbalance within SMs of such converter has yet to be investigated and methods for balancing the dc voltages in a cascaded 3L-NPC converter have not been found in public resources.

Issues resulting from dc voltage imbalance in MMCs and mitigation solutions have been reported in the literature [18]-[20]. However, as the causes of the imbalance are topology dependent, transferring the mitigation methods from MMCs to cascaded 3L-NPC converters directly should be done with care. For instance, voltage imbalance in an MMC is caused by the uneven charging and discharging duration of the SM capacitors [11]. On the other hand, the SMs of a cascaded 3L-NPC converter topology always turn on or off at the same time. Hence, typical MMC solutions [18], [19] including the sorting and the nearest level methods, may not be suitable.

The cause of dc voltage imbalance across SMs within a cascaded 3L-NPC converter was analyzed in detail. It is revealed that the dc voltage imbalance may occur due to the inversely proportional relationship between the incremental dc voltage and duty cycle within a SM when under power control. This cause is further confirmed by analyzing the system model, where each SM is represented as an equivalent impedance as viewed from the dc input terminal. Under dc voltage imbalance, there is an unstable system pole located at the right-half of the s-plane. Two balancing control methods are presented to shift the location of system poles and hence, to mitigate the dc voltage imbalance: a PI-based control method that requires communication with a central controller and a communication-less inverse-droop based control method. It is shown that the communication-dependent PI-based method achieves a precise balancing control of dc voltages and decoupling from the power controller. Upon loss of communication, the PI-based method is replaced by the inverse-droop based method to prevent an interruption in system operation. In the presented methods, only an additional PI/inverse-droop controller is required in each SM, and no other hardware is required except for a dc voltage sensor. Thus, the extra cost to the entire system will be limited.

The presented dc voltage balancing control methods are verified through simulations conducted with MATLAB/ Simulink based on the system parameters of the ANGLE-DC project. The effectiveness of the control methods is also experimentally validated using a laboratory-scale MVDC testbed, which is down scaled from the ANGLE-DC project.

II. MVDC System Modeling and Voltage Imbalance Analysis

A. ANGLE-DC MVDC Link

ANGLE-DC, the first trial of an MVDC link in the Great Britain (GB) electrical power system, is a demonstration project that enhances the power transfer capacity and thermal capability between the island of Anglesey and Bangor in North Wales by converting an ac transmission corridor into dc operation (see Fig. 1). This conversion allows an increased volume of renewable generation to flow mainland from Anglesey without exceeding thermal limits of existing assets. Through dc operation, a previously normally open circuit is kept permanently closed, enabling regulation of power and voltage [6].

B. Cascaded 3L-NPC Topology

The MVDC link in ANGLE-DC is based on two controllable VSC stations, as shown in Fig. 2. For each converter station at the end of the dc circuit of the MVDC link, twelve dc series-connected 3L-NPC SMs are installed to build up the dc voltage to ±27 kV. Sets of six SMs are connected with six-winding isolation transformers (see Tr.*ij* in Fig. 2). The isolation transformer is with a vector group connection of Yd11, where the high-voltage (primary) winding is star-connected and the low-voltage (secondary) winding is delta-connected with a 30-degree lead. A grounding resistor is connected in shunt at the midpoint of the cascaded SMs to achieve a bipolar operation. Relevant parameters of the ANGLE-DC converter stations are shown in Table I [8].

Fig. 1. MVDC circuit from Anglesey to Bangor in North Wales [6].

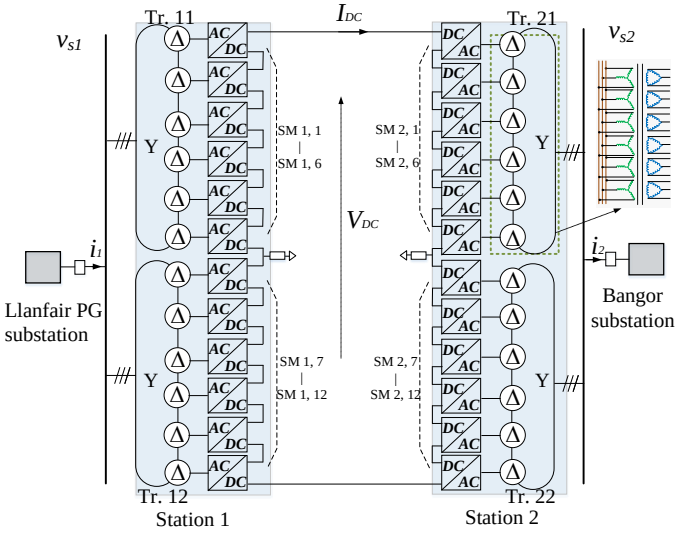


Fig. 2. Cascaded converter topology used in ANGLE-DC link.

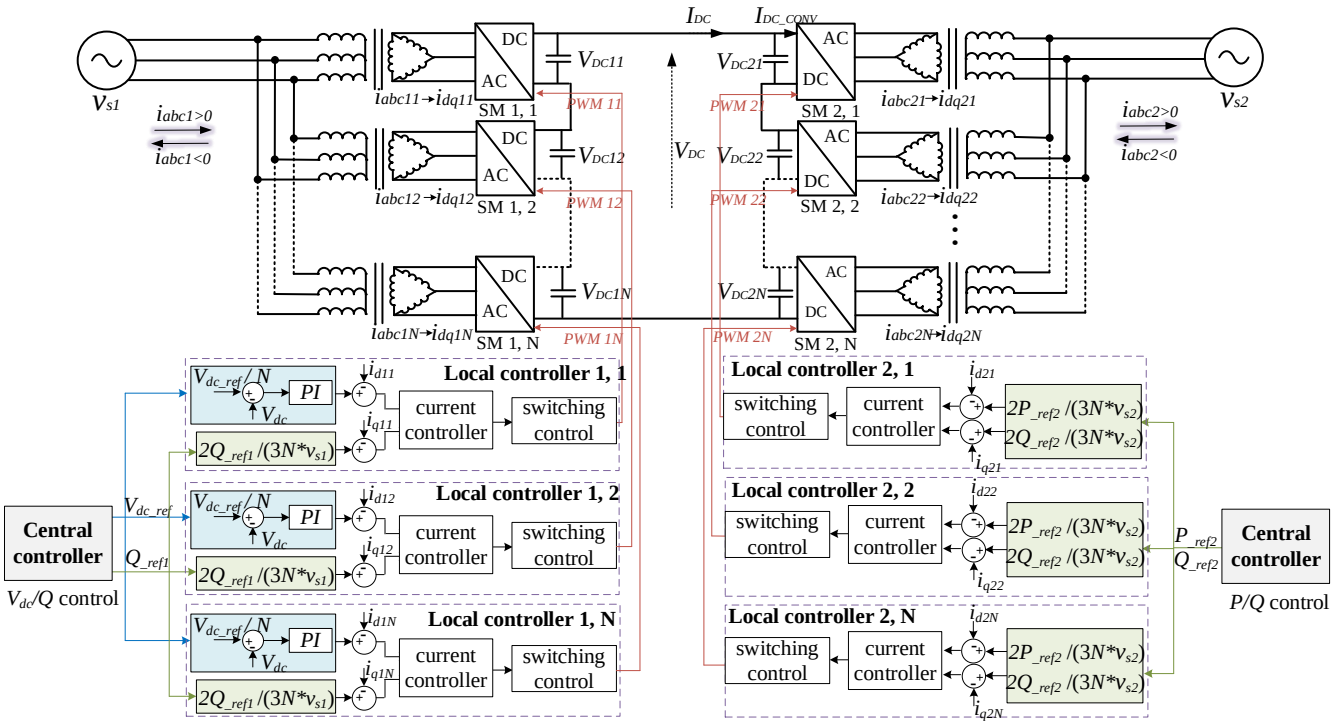


Fig. 4. Control schematic of the back-to-back MVDC system with *N* cascaded SMs.

TABLE I
PARAMETERS OF THE ANGLE-DC CONVERTERS [8]

Power rating S	33 MVA	DC link voltage V_{DC}	±27 kV
RMS value of $v_{s1,\ s2}$	33 kV	Transformer rating	2×17 MVA Y-33 kV/Δ-2.1 kV
Transformer impedance	0.2 p.u.	DC capacitance (per VSC)	2300 μF

C. Cause for DC Voltage Imbalance in Cascaded 3L-NPC Converters and MMCs

A cascaded 3L-NPC converter topology consisting of two SMs is used as an example to analyze the dc voltage imbalance.

If ac power is equally shared by both SMs, then $i_{s1} = i_{s2}$. For each SM, the ac output power is equal to the dc input power. Thus, at steady-state, $V_{dc1} = V_{dc2}$, and no current flows through the dc capacitors of the SMs, as shown in Fig. 3(a).

However, in practice a slight voltage difference between SM1 and SM2 may appear under transients due to the asynchronous update of control variables, sampling and mismatched component parameters. For example, if $C_{dc1u,l}$ is smaller than $C_{dc2u,l}$ due to the manufacturing tolerance or component degradation, v_{dc1} will be slightly higher than v_{dc2} during a perturbation in the dc link voltage, as shown in Fig. 3 (b).

This voltage difference between SMs may lead to a further dc voltage imbalance. As the ac power of each SM is regulated by a current controller, equal power sharing can still be achieved under dc voltage perturbations due to the high bandwidth of the current controller. If power flows from the dc side to the ac side, the duty cycle of SM1 (D_1) with a higher voltage (V_{dc1}) will be reduced by the current controller, whereas the duty cycle of SM2 (D_2) with a lower voltage (V_{dc2}) will increase. The inverse relationship between duty cycle and dc voltage will inevitably cause V_{dc1} to continue increasing and conversely, V_{dc2} to continue reducing.

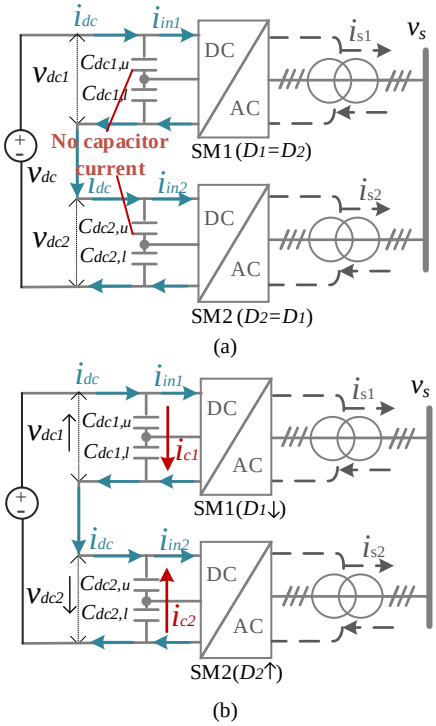


Fig. 3. Cascaded 3L-NPC converter circuit.

However, the voltage imbalance will not occur if the power flows from the ac side to the dc side. Although the duty cycle is still inversely proportional to the dc voltage, the higher the dc voltage of a SM is, the smaller the duty cycle is and, the less time required for charging time by the ac current. Thus, the dc voltage will be automatically decreased.

For MMCs, the uneven charging and discharging processes are caused by the SMs being turned on and off during a fundamental period. This means that only a certain amount of SM capacitors is connected at any time while other capacitors are bypassed [21]. As the instantaneous arm currents flowing through the SMs will be different at different phase angles of a sinusoidal cycle, the charging to the SM capacitors is also different, which leads to the voltage imbalance of the MMC.

D. Small-Signal Modeling

A further investigation of dc voltage imbalance is conducted based on small-signal modeling. The modeling of a single SM is firstly presented in this section. The relationship among all cascaded SMs is then obtained in Section II-E for in-depth analysis of dc voltage imbalance.

1) V_{dc}/Q and P/Q control method

For the back-to-back VSC system in Fig. 2, one converter station is operated using inverter control (*P/Q* control), whereas the other station using rectifier control (V_{dc} control). The inverter station is responsible for regulating the power flow through the dc link, while the rectifier station regulates the total dc link voltage.

For the system with *N* cascaded SMs, the control schematic adopted in this paper is shown in Fig. 4, where each SM is independently controlled by its local controller. A high-level central controller is employed to manage the local controllers. Thus, communication between a high-level central controller and the local controllers in the SMs is required.

The dc voltage imbalance previously highlighted is exhibited at the inverter station. Although the dc link voltage is regulated to achieve a constant value, it cannot be guaranteed that the voltage is equally shared by all SMs.

2) Small-signal model for a single SM

The input-to-SM-output transfer matrix for the i^{th} SM at the inverter station is obtained from a state-space representation following linearization of the nonlinear system model [22]. The current controller and the converter plant in a *dq* reference frame are included in the state-space model. It is assumed that the grid voltage v_s is constant and the phase-locked loop (PLL) is ideal; thus, the PLL dynamics are not taken into account.

In this paper, the neutral-point voltage is controlled by a common-mode modulation signal m_0 [16]. This signal is generated by the voltage difference between the upper and lower capacitors through a PI controller, and then superimposed on the three-phase modulation wave generated by the current controller. The average neutral-point current can be regulated to zero using this method, so the dc offset of the neutral-point voltage can be eliminated. As m_0 only influences the common-mode voltage, the dynamics of the neutral-point voltage are decoupled from those of the terminal voltages [17]. Thus, the dc voltage controller can be designed independently from the neutral-point voltage controller. As only the dc voltage imbalance resulting in the cascaded topology is the main scope of this paper, the dynamics of the neutral-point voltage are not considered in the system model.

The state-space representation for the i^{th} SM is given by

$$\frac{d}{dt}\begin{bmatrix}\Delta x_{id\_I}\\ \Delta x_{iq\_I}\\ \Delta i_{di}\\ \Delta i_{qi}\\ \Delta v_{dci}\end{bmatrix} = \mathbf{A}\underbrace{\begin{bmatrix}\Delta x_{id\_I}\\ \Delta x_{iq\_I}\\ \Delta i_{di}\\ \Delta i_{qi}\\ \Delta v_{dci}\end{bmatrix}}_{\mathbf{x}} + \mathbf{B}\underbrace{\begin{bmatrix}\Delta P_i^*\\ \Delta Q_i^*\\ \Delta i_{dc}\end{bmatrix}}_{\mathbf{u}} \tag{1}$$

$$\mathbf{y} = \mathbf{C}\mathbf{x} \tag{2}$$

where

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & -k_{iid} & 0 & 0\\ 0 & 0 & 0 & -k_{iiq} & 0\\ \frac{1}{L_s} & 0 & -\frac{R}{L_s}-\frac{k_{pid}}{L_s} & 0 & \frac{V_s+RI_d-\omega LI_q}{L_sV_{dc}}\\ 0 & \frac{1}{L_s} & 0 & -\frac{R}{L_s}-\frac{k_{piq}}{L_s} & \frac{RI_q+\omega LI_d}{L_sV_{dc}}\\ \frac{-3I_d}{2C_{dc}V_{dc}} & \frac{-3I_q}{2C_{dc}V_{dc}} & -\frac{3V_s+3(R-k_{pid})I_d}{2C_{dc}V_{dc}} & -\frac{3(R-k_{piq})I_q}{2C_{dc}V_{dc}} & 0 \end{bmatrix},$$

$$\mathbf{B} = \begin{bmatrix} \frac{2k_{iid}}{3V_s} & 0 & 0\\ 0 & \frac{2k_{iiq}}{3V_s} & 0\\ \frac{2k_{pid}}{3L_sV_s} & 0 & 0\\ 0 & \frac{2k_{piq}}{3L_sV_s} & 0\\ -\frac{k_{pid}I_d}{C_{dc}V_{dc}V_s} & -\frac{k_{piq}I_q}{C_{dc}V_{dc}V_s} & \frac{1}{C_{dc}} \end{bmatrix}, \mathbf{C} = [0 \quad 0 \quad 0 \quad 0 \quad 1].$$

In the state-space representation, $\mathbf{u} = [\Delta P_i^* \quad \Delta Q_i^* \quad \Delta i_{dc}]^T$ is the input vector, Δv_{dci} is a scalar output, and $\mathbf{x} = [\Delta x_{id\_I} \ \Delta x_{iq\_I} \ \Delta i_{di} \ \Delta i_{qi} \ \Delta v_{dci}]^T$ is the state vector. In the adopted notation, uppercase variables represent RMS values (or average values) and 'Δ' stands for perturbed variables. P_i^* is the reference of active power, Q_i^* is the reference of reactive power, i_{dc} is the dc link current, i_{di} is the *d*-axis current, i_{qi} is the *q*-axis current, and v_{dci} is the dc voltage. L_s, R and C_{dc} are the transformer leakage inductance, ac circuit resistance and dc capacitance of each SM, ω is the grid frequency, $k_{pid,q}$ and $k_{iid,q}$ are the proportional and integral gains of the PI controller, and Δx_{id_I} and Δx_{iq_I} are the outputs of the integral action of the PI controller. The equations used for extracting the small-signal model are given in the Appendix.

Based on (1) and (2), the transfer matrix representation in the Laplace domain is given as

$$\mathbf{Y}(s) = [\mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B}]\mathbf{U}(s) = \mathbf{C}\frac{\text{adj}(s\mathbf{I}-\mathbf{A})}{\det(s\mathbf{I}-\mathbf{A})}\mathbf{B}\mathbf{U}(s) = \mathbf{G}(s)\mathbf{U}(s) \tag{3}$$

where s is the Laplace variable, 'adj' stands for the adjoint matrix of $(s\mathbf{I}-\mathbf{A})$, 'det' for its determinant, $\mathbf{G}(s) = \mathbf{C}\frac{\text{adj}(s\mathbf{I}-\mathbf{A})}{\det(s\mathbf{I}-\mathbf{A})}\mathbf{B}$ is the transfer matrix, and $\det(s\mathbf{I}-\mathbf{A})$ is the characteristic polynomial. From (1)-(3), Δv_{dci} can be expressed as

$$\Delta v_{dci} = G_P(s)\Delta P_i^* + G_Q(s)\Delta Q_i^* + G_{idc}(s)\Delta i_{dc} \tag{4}$$

where

$$G_p(s) = \mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\begin{bmatrix}\frac{2k_{iid}}{3V_s} & 0 & \frac{2k_{pid}}{3L_sV_s} & 0 & -\frac{k_{pid}I_d}{C_{dc}V_{dc}V_s}\end{bmatrix}^T,$$

$G_Q(s) = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\left[0 \quad \frac{2k_{iiq}}{3V_S} \quad 0 \quad \frac{2k_{piq}}{3L_SV_S} \quad -\frac{k_{piq}I_q}{C_{dc}V_{dc}V_S}\right]^T$, and $G_{idc}(s) = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\left[0 \quad 0 \quad 0 \quad 0 \quad \frac{1}{C_{dc}}\right]^T$.

E. Analysis of DC Voltage Imbalance

As a single SM is modeled, the relationship between different SMs is obtained by analyzing the equivalent dc circuit consisting of cascaded SMs. Assuming the parameters for each SM are identical, the voltage equations for an N SM-cascaded converter are represented as:

$$\begin{cases} \Delta v_{dc1} = G_P(s)\Delta P_1^* + G_Q(s)\Delta Q_1^* + G_{idc}(s)\Delta i_{dc} \\ \Delta v_{dc2} = G_P(s)\Delta P_2^* + G_Q(s)\Delta Q_2^* + G_{idc}(s)\Delta i_{dc} \\ \vdots \\ \Delta v_{dcN} = G_P(s)\Delta P_N^* + G_Q(s)\Delta Q_N^* + G_{idc}(s)\Delta i_{dc} \\ \sum_{i=1}^{N}\Delta v_{dci} = \Delta v_{dc\_link} \end{cases} \quad (5)$$

As seen from Fig. 4, for an equal current sharing in each SM, $\Delta P_1^* = \Delta P_2^* = \cdots = \Delta P_N^* = \frac{\Delta P^*}{N}$ and $\Delta Q_1^* = \Delta Q_2^* = \cdots = \Delta Q_N^* = \frac{\Delta Q^*}{N}$. An equivalent dc circuit for such conditions is shown in Fig. 5.

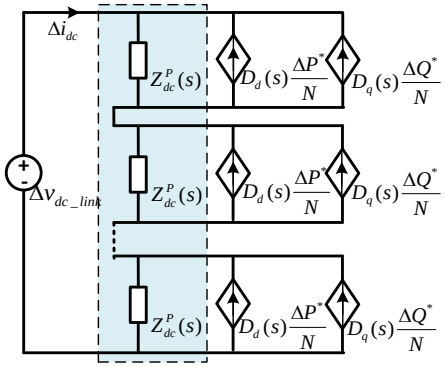


Fig. 5. Equivalent dc circuit for equal current sharing in each SM.

In Fig. 5, $Z_{dc}^P(s) = G_{idc}(s)$, $D_d(s) = G_P(s)/G_{idc}(s)$, $D_q(s) = G_Q(s)/G_{idc}(s)$. A relationship between the neighbouring SMs is obtained from the equivalent dc circuit as follows:

$$\frac{\Delta v_{dc,i}}{Z_{dc}^P(s)} = \frac{\Delta v_{dc,i+1}}{Z_{dc}^P(s)} = \Delta i_{dc} - \frac{D_d(s)\Delta P^* + D_q(s)\Delta Q^*}{N} \quad (6)$$

Based on (3) and (6),

$$\det(s\mathbf{I} - \mathbf{A})\left(\Delta v_{dc,i} - \Delta v_{dc,i+1}\right) = (a_5s^5 + a_4s^4 + a_3s^3 + a_2s^2 + a_1s + a_0)\left(\Delta v_{dc,i} - \Delta v_{dc,i+1}\right) = 0 \quad (7)$$

where a_0, a_1, a_2, a_3, a_4 and a_5 are given in the Appendix. From (7), ensuring an equal voltage sharing between SMs and the speed to achieve this are dictated by the eigenvalues of system matrix $\mathbf{A}$ (i.e., the poles of the $Z_{dc}^P(s)$). The root locus of $Z_{dc}^P(s)$ with varying operating points is shown in Fig. 6. System parameters in Table I are used to plot the root locus. As the system has five poles, only the dominant poles are displayed for clarity. Fig. 6(a) shows the trajectory of the dominant poles when P changes from –1 p.u. to 1 p.u. with Q equal to zero. As it can be seen, a right-half-plane pole is introduced when the active power is changed from a negative value (rectifier mode) to a positive value (inverter mode), which is the cause of the dc voltage imbalance. Fig. 6(b) shows instead the trajectories

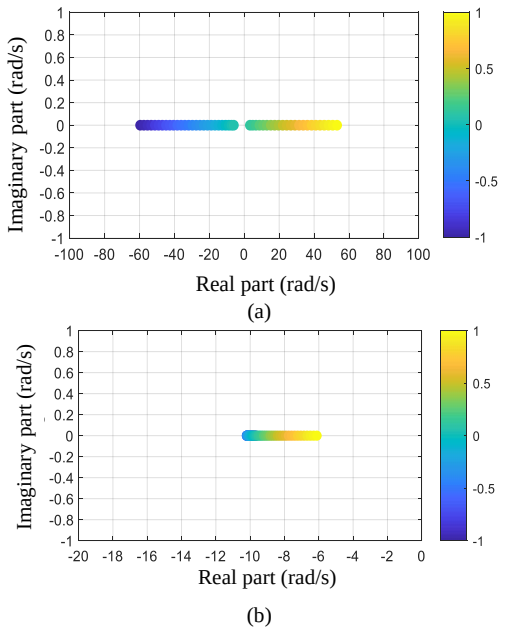


Fig. 6. Root locus of dominant poles (obtained by solving equation (7)) for different power operating conditions. (a) P changes and $Q = 0$. (b) Q changes and $P = 0$.

when Q changes from –1 p.u. to 1 p.u. and P is set to zero. It is observed that the dc voltage balance is not affected by Q as the pole is always located at the left-half of the s-plane, although the response time for voltage balancing would slow down as the pole moves closer to the imaginary axis.

III. Voltage Balancing Control Strategies

Two control methods to achieve a balanced dc voltage are presented in this section. Firstly, a PI-based method relying on communications is presented. Then, a droop-based control method, suitable upon loss of communication, is discussed.

A. Description of the voltage balancing control methods

1) PI-based method with communication.

A block diagram for this control method is shown in Fig. 7.

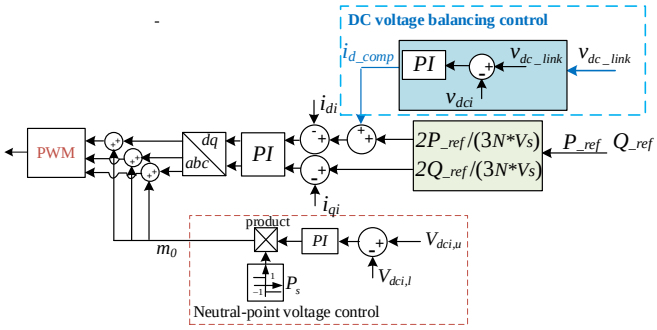


Fig. 7. PI-based voltage balancing controller with communication.

The PI-based dc voltage balancing controller is added to each P/Q controller at the inverter station. A high-level central controller measures the dc link voltage and sends the instantaneous value to the low-level controller at each SM. The low-level controller uses the average dc voltage and compares it with the dc voltage of each SM. A PI controller is used to

generate a compensating current reference to adjust the dc voltage. Through this feedback structure, the dc voltage of each SM can converge to the average value. As reactive power has a negligible effect on the voltage imbalance, the PI-based structure is added to the *d*-axis control loop only (i.e., superimposed with the active power controller). In addition, a PI-based neutral-point voltage control method is used to balance the neutral-point voltage of each SM. The output of its PI controller acts as the zero-sequence variable which is added on the three-phase sinusoidal modulation waveforms.

Due to the integral action of the PI controller, the steady-state error of dc voltage difference is driven to zero. In addition, as the central controller sends the instantaneous dc link voltage value to each SM, the sum of the compensation currents supplied by the PI controllers is zero (i.e. $\sum_{i=1}^{N} i_{d\_compi} = G_{PI}(s)\sum_{i=1}^{N}\left(\frac{v_{dc\_link}}{N} - v_{dci}\right) = 0$ and $G_{PI}(s)$ is the transfer function of the dc voltage balancing PI controller). Therefore, the voltage balancing control method does not affect the output power, which means it is decoupled from the power control.

To verify the decoupling between the dc voltage balancing control and the neutral-point voltage balancing control, a set of comparative simulations was conducted. Fig. 8(a) shows the neutral-voltage when a single 3L-NPC SM is used (without cascading other SMs), while Fig. 8(b) shows the neutral-point voltage of one SM in the case of four cascaded SMs. The neutral-point voltage in both cases shows similar values with regards to the dc offsets and the 3rd order voltage ripples.

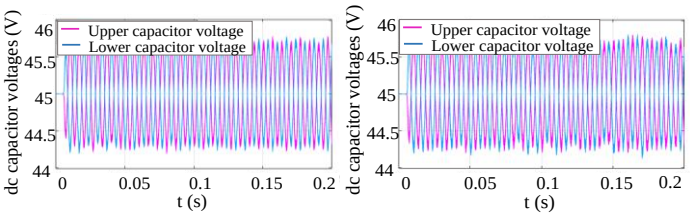


Fig. 8. Neutral-point voltage waveforms: (a) waveforms without dc voltage balancing control; (b) waveforms with dc voltage balancing control.

2) Droop-based method without communication

Communication may be lost during operation. Under such conditions, the high-level central controller would not be able to send dc link voltage information to the SMs—thus making the system vulnerable to instability. To prevent this, a self-balancing control method without the need for communication is presented. The method is inspired by the droop control strategies employed in dc/dc converters [23], [24] and adapted to control the cascaded 3L-NPC converter.

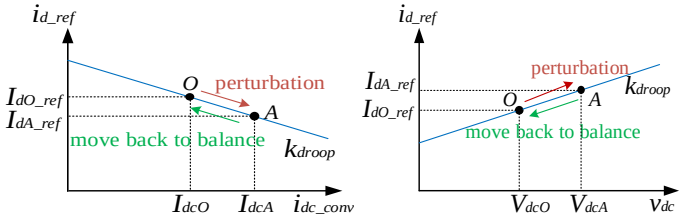


Fig. 9. Droop curves for voltage balancing control. (a) $i_{dc\_conv} - i_d^*$ curve. (b) $v_{dc} - i_d^*$ curve.

Two potential control implementations are discussed. In the first one, shown in Fig. 9(a), the current reference i_d^* is adjusted by i_{dc_conv}, which is the dc current entering the converter after passing through the dc capacitor (see Fig. 4). Current i_{dc_conv} could move from the equilibrium point I_{dcO} to I_{dcA} following a perturbation, which discharges the dc capacitor. According to the droop curve, i_d^* will decrease to prevent the dc capacitor from discharging so that the operating condition moves back to the equilibrium point. The advantage of using this method is that it does not require dc voltage sensors. However, the reconstruction of i_{dc_conv} through ac currents may introduce noise interference, which is not desirable.

The second method, called the inverse-droop controller, is shown in Fig. 9(b). When v_{dc} changes from the equilibrium point V_{dcO} to V_{dcA} following a perturbation, i_d^* increases according to the curve shown. Thus, the discharge of the dc capacitor will be accelerated to move the dc voltage down to the equilibrium point.

Since the noise introduced by the reconstruction of current in the first method may deteriorate the control performance, the inverse-droop controller is adopted instead. Its schematic is shown in Fig. 10. It should be noted that due to the fixed reference point V_{dcO}, the sum of i_{d_compi} is not guaranteed to be zero (i.e., $\sum_{i=1}^{N} i_{d\_compi} = K_{droop}\sum_{i=1}^{N}(v_{dci} - V_{dcO}) \neq 0$). This means the dc voltage balancing control is coupled to the power control loop. Due to this, it is recommended that the inverse-droop controller is adopted as a replacement of the PI-based controller only upon communication failure.

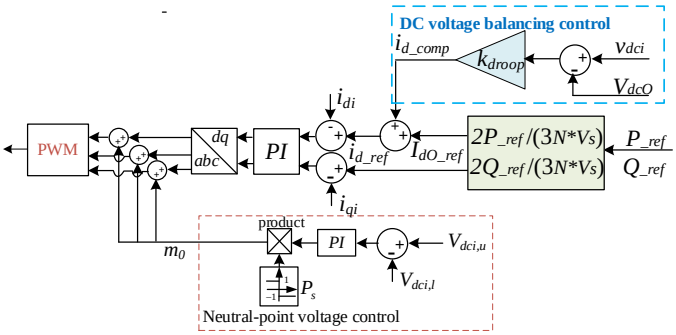


Fig. 10. Inverse-droop based voltage balancing controller.

B. Controller parameter design and stability analysis

Controller parameters should be properly selected for the presented voltage balancing controllers. The selection can be performed through small-signal analysis and pole placement. The system poles should be placed in the left-half plane to guarantee system stability.

In normal operating conditions, all the SMs are operated under PI-based control with communication. When some SMs are lost due to communication issues, these SMs could switch to the alternative droop-based control. Thus, three different control configurations are analyzed in this paper: 1) all SMs operate using a PI-based control with communication with the high-level central controller; 2) all SMs switch to the inverse-droop based control when communication with the high-level central controller is lost; 3) only the communication-less SMs switch to inverse-droop based control, with the remaining SMs

working with communication with the high-level central controller (denoted as hybrid structure).

1) All SMs work with communication

With the use of dc voltage balancing control, the voltage equation (4) is rewritten as

$$\Delta v_{dci} = G_P(s)\frac{\Delta P^*}{N} + G_P'(s)G_{PI}(s)\left(\frac{\Delta v_{dc_{link}}}{N} - \Delta v_{dci}\right) + G_{idc}(s)\Delta i_{dc} \quad (8)$$

where the current source generated from reactive power has been omitted due to its negligible influence. In (8), $G_P'(s) = \frac{3V_s}{2}G_P(s)$ and $G_{PI}(s) = -\frac{k_{pudc}s + k_{iudc}}{s}$. The gain of $G_{PI}(s)$ is negative due to the defined positive current direction shown in Fig. 4. Based on [25], $k_{iudc} = 200k_{pudc}$ is adopted. Letting $Z_{dc}^C(s) = \frac{G_{idc}(s)}{G_P(s)G_{PI}(s)}$, the equivalent dc circuit of the cascaded topology is shown in Fig. 11.

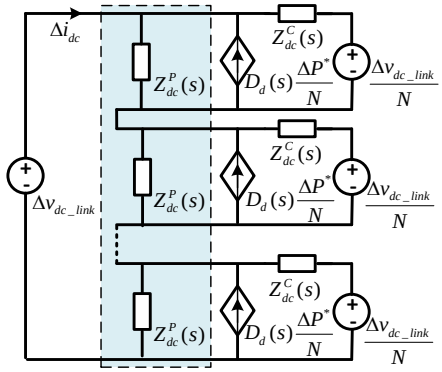


Fig. 11. Equivalent dc circuit with PI controller.

From Fig. 11, as each SM works with communication and all SMs have the same parameters, the equivalent dc circuit of each SM is identical. The input dc impedance $Z_{dc}^U(s)$ of each SM is obtained by setting the output of the voltage and current sources to zero, resulting in

$$Z_{dc}^U(s) = Z_{dc}^C(s)//Z_{dc}^P(s) = \frac{G_{idc}(s)}{1+G_P'(s)G_{PI}(s)} \quad (9)$$

where symbol '//' stands for a parallel connection. The relationship between the neighboring SMs in Fig. 10 is given by

$$\underbrace{\left(\det(s\mathbf{I}-\mathbf{A})\,s - \mathbf{C}\mathrm{adj}(s\mathbf{I}-\mathbf{A})\begin{bmatrix}\frac{2k_{iid}}{3V_s}\\0\\\frac{2k_{pid}}{3LV_s}\\0\\-\frac{3k_{pid}I_d}{2C_{dc}V_{dc}}\end{bmatrix}\left(k_{pudc}s + k_{iudc}\right)\right)}_{G_{u,1}(s)} \times \left(\Delta v_{dc,i} - \Delta v_{dc,i+1}\right) = \left(a_6's^6 + a_5's^5 + a_4's^4 + a_3's^3 + a_2's^2 + a_1's + a_0'\right)\left(\Delta v_{dc,i} - \Delta v_{dc,i+1}\right) = 0 \quad (10)$$

where a_0', a_1', a_2', a_3', a_4', a_5', a_6' are given in the Appendix. $G_{u,1}(s)$ is the denominator term of $Z_{dc}^U(s)$ following suitable algebraic expansion. Thus, the eigenvalues of $G_{u,1}(s)$ are the poles of $Z_{dc}^U(s)$. The root locus of the dominant poles of $Z_{dc}^U(s)$ is shown in Fig. 12 for both positive and negative power flows. The eigenvalue trajectories are plotted for rated power (i.e., P =1 p.u.) as proportional gain k_{pudc} increases from 0 to 50 p.u., with a base value $Z_{dc\_base} = \frac{V_{DC\_base}^2}{S_{base}}$ ($S_{base} = S$, $V_{DC\_base} = V_{DC}$).

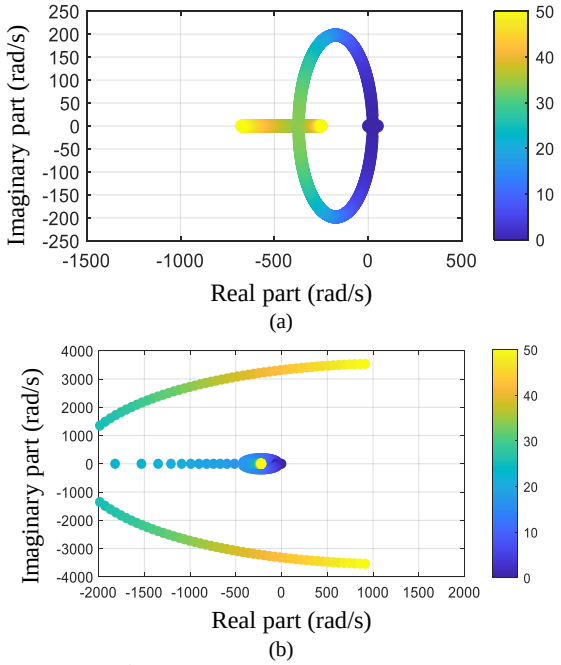


Fig. 12. Root locus of dominant poles (obtained by solving equation (10)) with increasing k_{pudc} under PI controller. (a) Positive power flow. (b) Negative power flow.

For an inverter mode, shown in Fig. 12(a), the poles move to the left-half of the s-plane as k_{pudc} increases, thus demonstrating the effectiveness of the voltage balancing method. However, the value of k_{pudc} should not be too large; otherwise, the poles may become unstable when power flow is reversed, as shown in Fig. 12(b).

To ensure an acceptable damping ratio of complex conjugate dominant poles (≥ 0.5), these poles should lie inside a specific region of the complex plane within a radial line drawn from the origin and its reflection across the real axis. The radial line is at an angle of 60° with reference to the negative real axis [26]. This condition is achieved if the proportional gain of the PI controller is selected as $k_{pudc} = 25$.

2) All SMs work without communication

The voltage equation for SMs without communication is given by

$$\Delta v_{dci} = G_P(s)\frac{\Delta P^*}{N} + G_P'(s)k_{droop}\Delta v_{dci} + G_{idc}(s)\Delta i_{dc} \quad (11)$$

where $Z_{dc}^{C1}(s) = \frac{G_{idc}(s)}{k_{droop}G_P'(s)}$. Fig. 13 shows the equivalent circuit for this condition, from where the dc equivalent impedance with inverse-droop controller is obtained as

$$Z_{dc}^{U1}(s) = Z_{dc}^{C1}(s)//Z_{dc}^P(s) = \frac{G_{idc}(s)}{1+k_{droop}G_P'(s)} \quad (12)$$

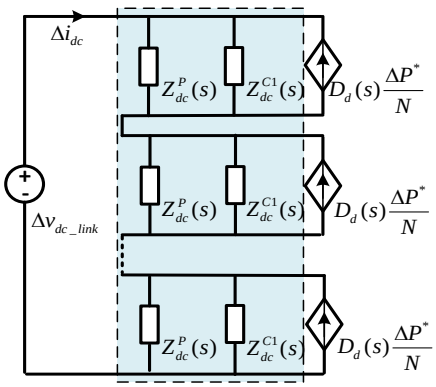


Fig. 13. Equivalent dc circuit with inverse-droop controller.

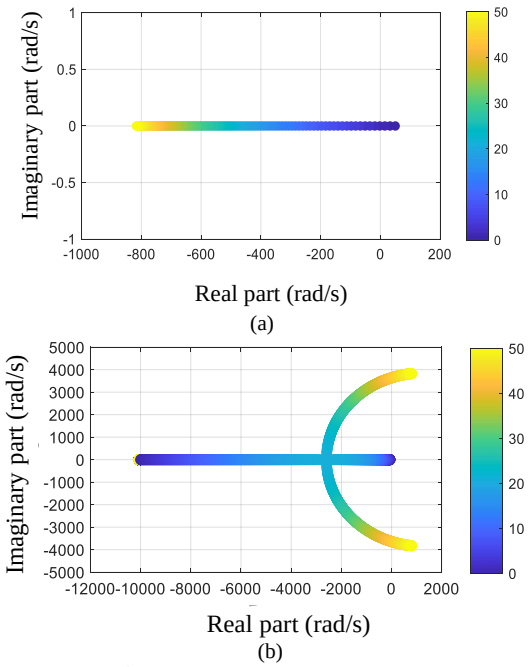


Fig. 14. Root locus of dominant poles (obtained by solving equation (13)) with increasing k_{droop} under inverse-droop controller. (a) Positive power flow. (b) Negative power flow.

The voltage equation of neighbouring SMs is given by

$$\underbrace{\left(\det(s\mathbf{I}-\mathbf{A})-\mathbf{C}\mathrm{adj}(s\mathbf{I}-\mathbf{A})\begin{bmatrix}\frac{2k_{iid}}{3V_s}\\0\\\frac{2k_{pid}}{3LV_s}\\0\\-\frac{3k_{pid}I_d}{2C_{dc}V_{dc}}\end{bmatrix}k_{droop}\right)\times}_{G_{u,2}(s)}$$

$$\left(\Delta v_{dc,i}-\Delta v_{dc,i+1}\right)=\left(a_5''s^5+a_4''s^4+a_3''s^3+a_2''s^2+a_1''s+a_0''\right)\left(\Delta v_{dc,i}-\Delta v_{dc,i+1}\right)=0 \quad (13)$$

where a_0'', a_1'', a_2'', a_3'', a_4'', a_5'' are given in the Appendix. $G_{u,2}(s)$ is the denominator term of $Z_{dc}^{U1}(s)$. The root locus of the dominant poles as the droop coefficient k_{droop} is increased from 0 to 50 p.u., for P = 1 p.u., is plotted for both positive and negative power flows. As shown in Fig. 14, increasing the value of k_{droop} will guarantee the system is stable for an inverter operation. However, its value should not be too large to preserve stability for rectifier operation. Although a larger k_{droop} ensures a better voltage balance characteristic, it may affect the accuracy of the output power [27]. Thus, an appropriate value should be carefully selected considering both the performance of voltage balancing and the impact on the power control. The value of the droop coefficient k_{droop} is set as 10 to maximize the voltage balancing performance and to restrict the influence on the power control.

3) Some SMs have communication

If the number of SMs with communication is m and the number of SMs without communication is l (with $l = N - m$), then

$$m\Delta v_{dc,i}+l\Delta v_{dc,j}=\Delta v_{dc\_link} \quad (14)$$

where Δv_{dci} and Δv_{dcj} denote the dc voltage of the i^{th} SM with communication and the dc voltage of the j^{th} SM without communication, respectively. Combining equations (10), (13) and (14), a relationship between $\Delta v_{dc,i}$ and $\Delta v_{dc,j}$ is obtained as

$$\mathbf{C}\mathrm{adj}(s\mathbf{I}-\mathbf{A})\begin{bmatrix}0&0&0&0&\frac{1}{C_{dc}}\end{bmatrix}^{\boldsymbol{T}}\left((N-m)G_{u,1}(s)+mG_{u,2}(s)s\right)\left(\Delta v_{dc,i}-\Delta v_{dc,j}\right)=0 \quad (15)$$

where $G_{u,1}(s)$ and $G_{u,2}(s)$ are the same as in (10) and (13). Fig. 15 shows the root locus of the dominant poles p_i (i =1, 2) as m varies from 1 to 11, with the active power being kept at 1 p.u. The controller parameters are selected according to the analyses in Sections III-B-1 and III-B-2, where $k_{pudc} = 25$ and $k_{droop} = 10$. As it can be seen, one of the poles moves close to the imaginary axis as m is increased, which means that the difference of dc voltage between SMs converges to zero at a decreased rate. The worst case happens when m = 11.

To have a comprehensive understanding of the hybrid control structure, the Bode diagram of a transfer function $G_d(s)=\frac{\Delta v_{dci}(s)-\Delta v_{dcj}(s)}{\Delta v_{dc_{link}}(s)}$ is used to analyze the disturbance rejection ability of the cascaded converters [28]. $G_d(s)$ reflects the impact of the dc link voltage perturbation on the voltage difference between SMs. The smaller the amplitude of $G_d(s)$ is, the better the disturbance rejection.

Both cases for m=1 and m=11 are studied, and the Bode diagram is shown in Fig. 16. The voltage balancing performance for both cases is influenced by the perturbation of

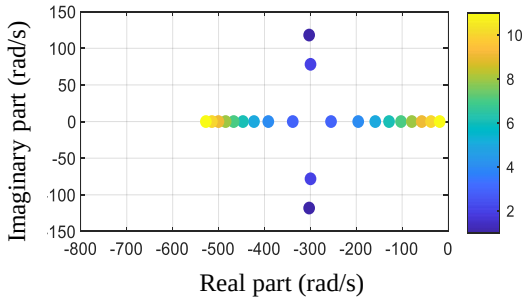


Fig. 15. Root locus of dominant poles (obtained by solving equation (15)) with increasing values of m, with $k_{pudc} = 25$ and $k_{droop} = 10$.

the dc link voltage. However, the magnitude in the Bode diagram for the case when m=1 (i.e., 1 PI controller and 11 inverse-droop controllers) is lower than that for the case when m=11 (i.e., 11 PI controllers and 1 inverse-droop controller) at frequencies below 400 rad/s, which implies that a larger dc voltage error may appear resulting from the perturbation as m increases. This illustrates that the disturbance rejection ability is decreased as more PI-based controllers are used in the hybrid structure.

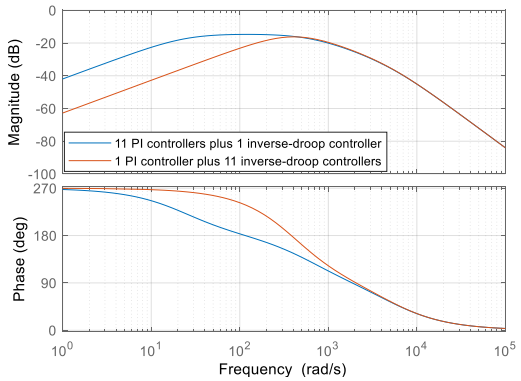


Fig. 16. Bode diagram of $G_d(s) = \frac{\Delta v_{dci}(s) - \Delta v_{dcj}(s)}{\Delta v_{dc_{link}}(s)}$.

On the contrary, if all the SMs work under the same control strategy (either PI-based control or inverse-droop based control), they will exhibit a similar dynamic performance regardless of the number of cascaded SMs. Thus, it is recommended that all the SMs should automatically switch to communication-less control as described in Section III-A-2 if communication with any SM is lost.

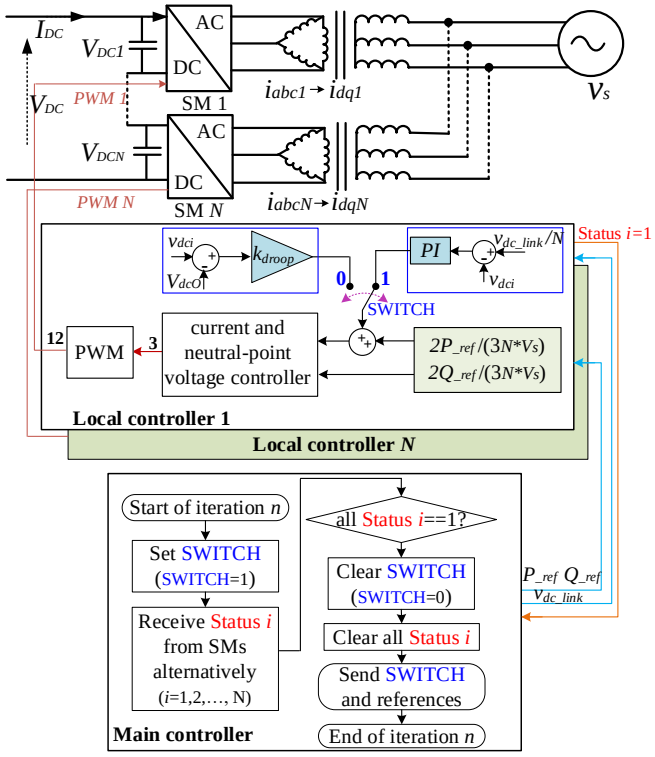


Fig. 17. Overall control structure combing both control loops.

Both dc voltage balancing control methods combing their mode switching are integrated into Fig. 17. The control modes are selected by the SWITCH command. The PI-based voltage balancing control is used when SWITCH = 1 and switches to the droop-based control with SWITCH = 0. To achieve this, the Status i is returned from the SM's controller to the main controller. If all Status i equal 1, the communication is assumed as normal, and SWITCH is set as 1 by the main controller. Otherwise, there are communication failures of SMs. SWITCH will be set as zero to switch the SMs to the droop-based control mode. The SMs which lost communication will automatically switch their control mode.

C. Simulation results

The control methods presented in Section III were verified by conducting simulations in MATLAB/Simulink, with results shown in Fig. 18 and Fig. 19. Operation for twelve cascaded SMs is simulated, and the simulation parameters are provided in Table I. The performance of the voltage balancing control methods is assessed for step changes in the dc link voltage, with results presented in Fig. 18(a) when communication is available (PI-based control) and in Fig. 18(b) when communication is lost (inverse-droop based control). The controller parameters are the same as those in Sections III-B-1 and III-B-2.

From the results, it can be seen that both control methods successfully achieve dc voltage balancing upon step changes in the dc link voltage (see how the traces for all SMs exhibit a similar behavior). This is consistent with the eigenvalue analysis presented in Sections III-B-1 and III-B-2.

For completeness, system performance is also verified for a hybrid control structure considering some SMs with communication and the rest without it, as described in Section

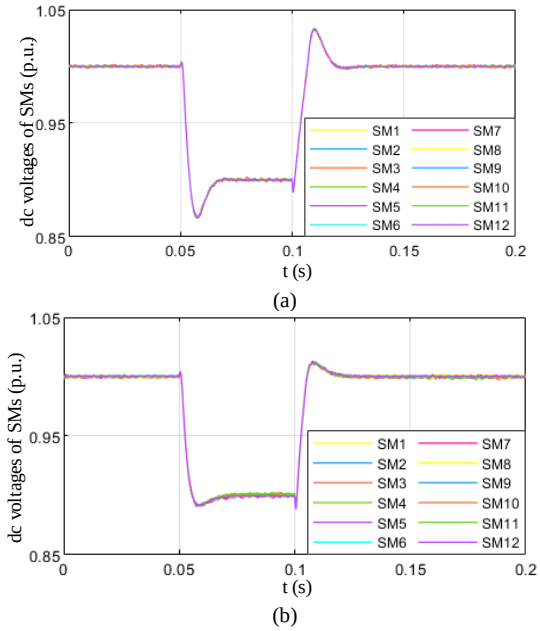


Fig. 18. DC voltages of SMs 1 to 12. (a) with PI-based control. (b) with inverse-droop based control.

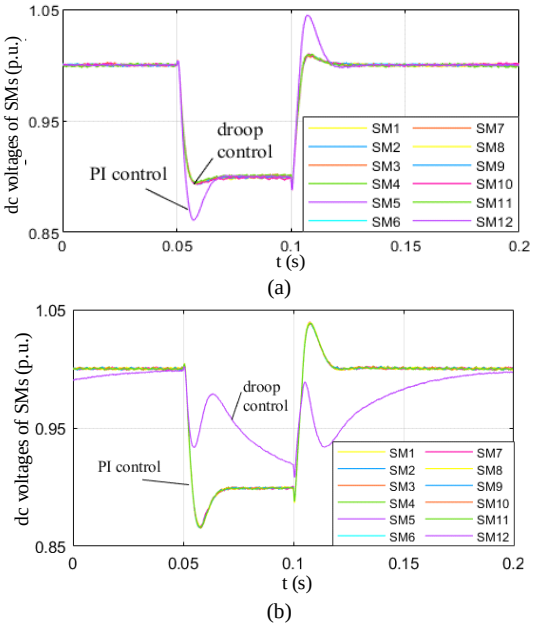


Fig. 19. DC voltages of SMs 1 to 12 for a hybrid control structure. (a) 1 PI controller plus 11 inverse-droop controllers. (b) 1 inverse-droop controller plus 11 PI controllers.

III-B-3. Results for a step change in the dc link voltage are shown in Fig. 17. For simplicity, only the extreme cases are provided: the results shown in Fig. 19(a) correspond to the case when m = 1 (i.e., a single SM has communication and 11 SMs feature the communication-less inverse-droop controllers), whereas results in Fig. 19(b) show the case for m = 11 (i.e., 11 SMs have communication and 1 SM features the communication-less inverse-droop controller). As it can be observed from these results, an increase in the number of SMs with PI-based control in the hybrid structure will aggravate the dc voltage imbalance under dynamic conditions.

IV. Hardware Configuration of the MVDC Testbed

A. Laboratory scale testbed of cascaded 3L-NPC converters

The laboratory-scale MVDC testbed is shown in Fig. 20. The testbed has the same per unit values as the converters used in the ANGLE-DC project. The labels of stations 1 and 2 are consistent with those in Fig. 2, and the two cables connecting the two cabinets represent the dc link.

The detailed internal SMs and components of the MVDC testbed, including the twelve 3L-NPC cascaded SMs, the high-level central controller and isolation transformers, are shown in Fig. 21. The high-level central controller is used to coordinate and monitor the operation of the SMs. Current and voltage sensors for signal measurements and other hardware devices such as ac breakers and relays are also included.

The parameters of the MVDC experimental testbed and those from the ANGLE-DC project are shown in Table II. The same per unit values have been adopted for a suitable comparison. Since the leakage inductance of the transformer for the testbed is significantly smaller than that of the real system, an additional L-type grid-connected inductor is used, with

$$L_{p.u.} = \frac{L_S {N_{Tr.}}^2/12}{L_{base}} = \frac{\omega_{base} L_S {N_{Tr.}}^2/12}{Z_{ac\_base}} = 0.22\ \text{p. u.} \quad (16)$$

$$C_{p.u.} = \frac{C_{dc}/12}{C_{base}} = \frac{C_{dc}/12}{\frac{1}{\omega_{base} Z_{dc\_base}}} = 5.5\ \text{p. u.} \quad (17)$$

where $Z_{ac\_base} = \frac{V_{AC\_base}^2}{S_{base}}$ ($S_{base} = S$, $V_{AC\_base} = V$), $\omega_{base} = \omega$, and N_{Tr} is the turns ratio of the isolation transformer.

TABLE II
Parameter Comparison of the ANGLE-DC and the MVDC Testbed in Per Unit Values [15][29]

Parameters	ANGLE-DC station	Per unit	MVDC testbed
Power rating S	33 MVA	1 p.u.	30 kVA
AC voltage V (rms of $v_{1,2}$)	33 kV	1 p.u.	415 V
DC link voltage V_{DC}	±27 kV	1 p.u.	±540 V
Transformer rating	2×17 MVA Y-33 kV/Δ-2.1 kV	1 p.u.	2×15 kVA Y-415 V/Δ-41.5 V
Transformer impedance	0.2 p.u.	0.2 p.u.	—
Filter inductance (per VSC)	—	0.22 p.u.	0.5 mH
DC capacitance (per VSC)	2300 μF	5.32 p.u./ 5.5 p.u.	5400 μF
Switching frequency	750 Hz	—	10 kHz

Fig. 20. Lab-scaled MVDC platform.

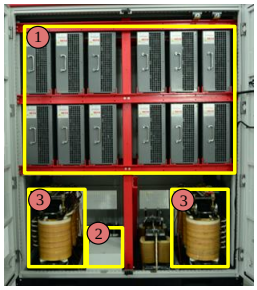


Fig. 21. Internal structure of the MVDC experimental testbed: 1) 3L-NPC SMs; 2) high-level central controller; 3) isolation transformers.

The control parameters used in the experimental testbed are shown in Table III. To verify the performance of the testbed and the ANGLE-DC system under same per unit values, a set of comparative tests for one SM has been done. The experimental results are compared with those obtained by simulation, where

the parameters of the real ANGLE-DC system are used. For simplicity, the performance of the dc link voltage is shown for a step reference change only, with results provided in Fig. 22. As it can be seen, the VSC of the MVDC testbed has a similar dynamic performance (in terms of overshoot and rise time) as the one in the ANGLE-DC system. Although the experimental performance exhibits slightly slower dynamics, this is attributed to unmodelled control delays.

TABLE III
PER UNIT VALUES OF CONTROL PARAMETERS

Proportional parameter of *d*-axis current controller (k_{pid})	4.29	Proportional parameter of neutral-point voltage controller (k_{NP})	1
Integral parameter of *d*-axis current controller (k_{iid})	10	Proportional parameter of dc voltage balancing controller (k_{pudc})	6
Proportional parameter of *d*-axis current controller (k_{piq})	4.29	Integral parameter of dc voltage balancing controller (k_{iudc})	120
Integral parameter of *d*-axis current controller (k_{iiq})	10	Proportional parameter of dc voltage balancing controller (k_{doop})	2

B. Communication

The overall communication diagram for the MVDC testbed is shown in Fig. 23. The high-level central controller supervises the behavior of the SMs and communicates with a PC in real time to monitor the status of the system operation. Code Composer Studio (CCS) codes are translated automatically from the MATLAB/Simulink

model and then downloaded to the controllers for an easy implementation. Processors TMS320F28335 are used for the central and SM controllers, which are a preferred type of microchips for industrial applications [30]. Other functions of the central controller include command dispatch, sending suitable references to the SMs and PWM carrier synchronization. The communication between the central controller and each SM controller is based on the Modbus protocol. The SM controllers operate according to the received information from the central controller.

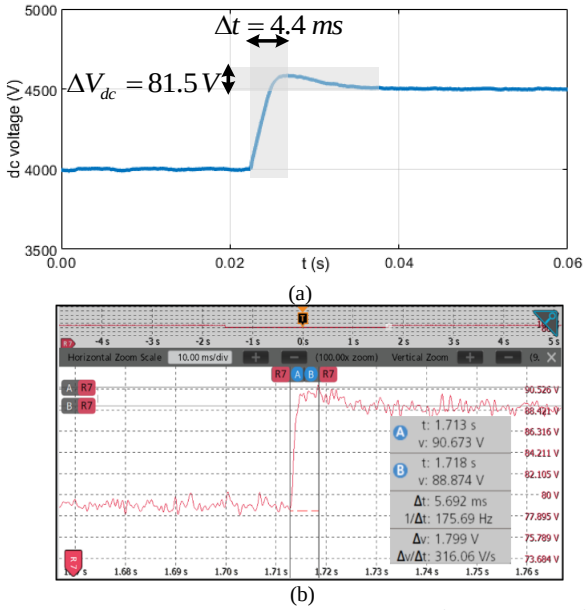


Fig. 22. Step-change dc voltage tests. (a) Simulation of one converter from the ANGLE-DC project. (b) Experimental result for one converter in the testbed.

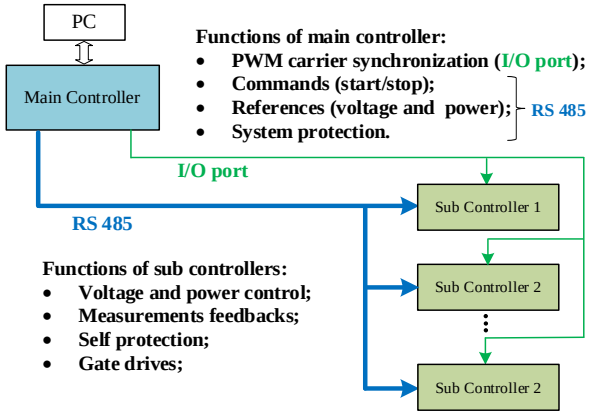


Fig. 23. Communication diagram of the MVDC testbed.

V. EXPERIMENTAL VALIDATION

The three control scheme configurations described in Section III-B are experimentally validated, including PI-based control (with communications), inverse-droop based control (communication-less) and the hybrid control combining the former two methods. Two power amplifiers (PA-3*3000-AB/260/2G) are connected with the MVDC testbed to emulate the ac grids. Eight SMs are cascaded together, constituting a 720 V dc link voltage. Four SMs are connected to the upper transformer (Tr.*i*1) and the other four to the lower transformer (Tr.*i*2), with a grounding resistor at the midpoint of SMs. This follows the structure shown in Fig. 2, where twelve SMs as opposed to 8 are considered. The testbed is operated at around 4.2 kW due to the limited power capacity of the power amplifier, which has a maximum output power of 9 kW.

For the experiments, the performance of the voltage balancing methods is assessed for reference changes in the set points of active power and dc voltage. Fig. 24 shows representative experimental results for the PI-based control scheme. The top purple trace shows the dc link voltage, the red trace (second layer from the top) shows the dc link current, and the green, orange, pink and dark blue traces (third layer) show the dc voltages of four SMs. The bottom blue trace shows the current of phase *a*. At the start of the experiment, the dc link voltage is increased by the rectifier station to the rated value (i.e., 720 V). After the rated dc link voltage is reached, the inverter station begins to regulate power according to the active power references (at around 4.2 kW) sent by the high-level central controller. At this point, the PI-based voltage balancing controller is enabled. Fig. 24(a) shows results for a reference change in power, whereas Fig. 24(b) shows results for a reference change in dc voltage. The references are modified using ramp functions with slopes of 750 W/s and 10 V/s, respectively, to achieve a smooth dynamic behavior, as opposed to step changes. For simplicity, dc voltage traces for 4 SMs

(SM1, SM2, SM5 and SM6) are shown only. It can be observed that all SMs exhibit a balanced dc voltage performance for both types of reference change.

Fig. 25 shows the system performance when communication is lost. Under such conditions, the dc voltage balancing control is disabled altogether. The dc voltages of the SMs diverge afterwards, although the total dc link voltage is kept constant. To avoid overvoltage at some SMs, the system protection is triggered, during which the PWM driving signals are blocked and the ac coil relays in the three-phase ac circuits are opened.

A final experiment is conducted for the case of invalid communication. In this case, communication-less inverse-droop based control will be activated in place of the PI-based control requiring communication. Fig. 26 shows the experimental results when all SMs operate with the inverse-droop controllers. Similar experimental conditions as for the PI-based control method are used, with the results presented in Fig. 26 showing the system performance upon ramp reference changes in active power and dc link voltage as previously discussed. As it can be seen, the inverse-droop based method ensures system stability when communication is not available.

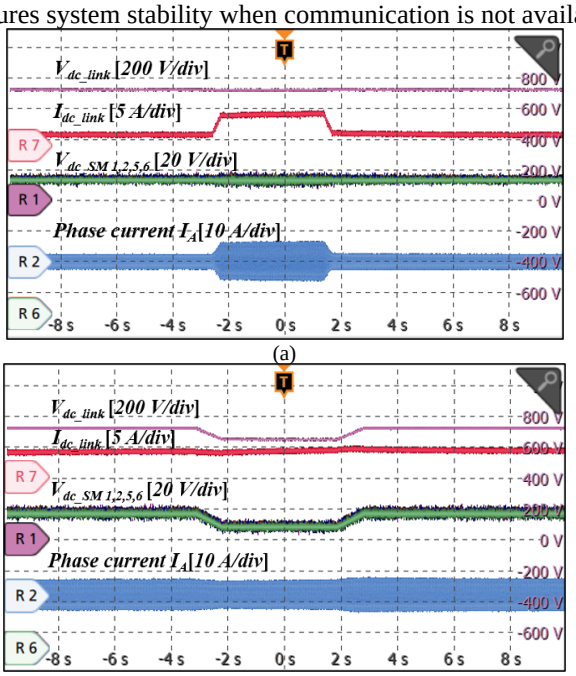


Fig. 24. Operation with PI-based dc voltage balancing controllers. Results for: (a) active power reference change; (b) dc link voltage reference change.

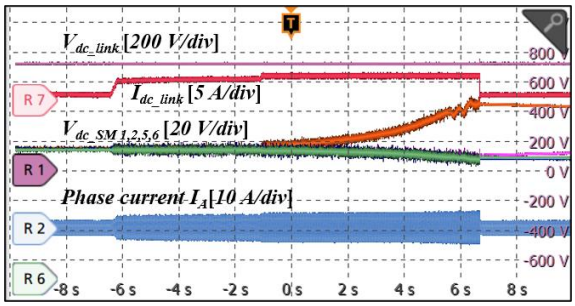


Fig. 25. Operation when communication is lost.

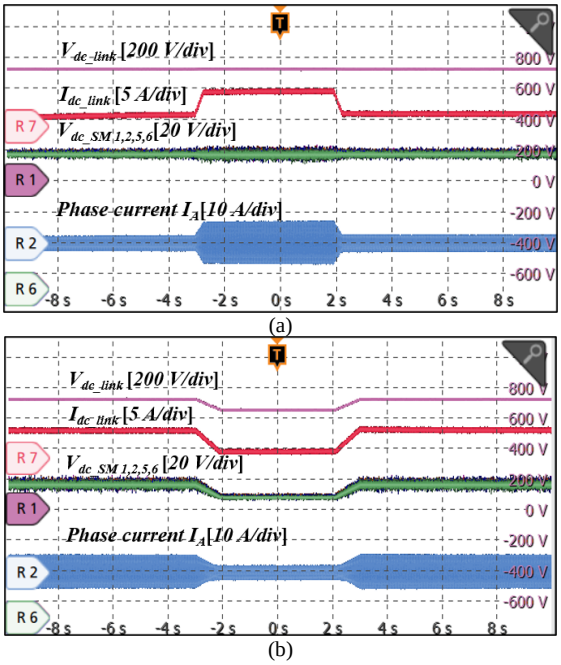
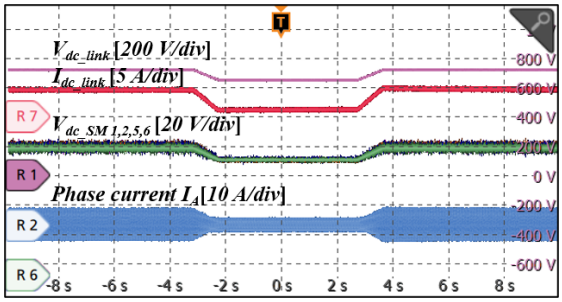


Fig. 26. Operation with droop-based dc voltage balancing controllers. Results for: (a) active power reference change; (b) dc link voltage reference.

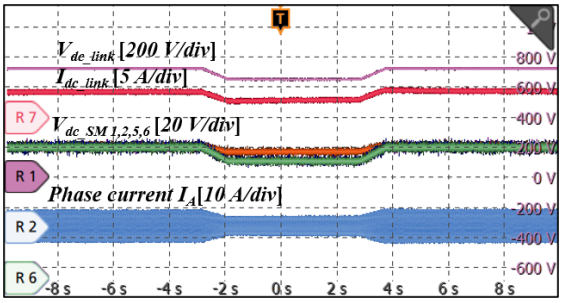
However, as the given voltage reference employed is the historic value just before communication is lost, the inverse-droop controller will influence the output power accuracy during the reference change of dc link voltage, regulated by the rectifier station, as shown in Fig. 26(b). This demonstrates the coupling between the voltage balancing controller and the power controller, as discussed in Section III. Given that the main focus of this paper is to address dc voltage imbalance, compensation for power accuracy falls out of the scope of the work. The interested reader is referred to [31], where a suitable control method to mitigate this disadvantage can be found.

The experimental performance of a hybrid control structure combining both dc voltage balancing methods is shown in Fig. 27. Two extreme cases are studied: one PI-based controller and seven inverse-droop based controllers (with results shown in Fig. 27(a)) and seven PI-based controllers and one inverse-droop based controller (with results shown Fig. 27(b)). It can be seen that the dc voltage balancing performance worsens as the number of PI-based controllers in a hybrid structure increases. Since the hybrid control method influences the dc voltage balancing performance, it is recommended that all SMs change from PI-based to the inverse-droop based control once communication fails at any SM. For completeness, Fig. 28 shows the transition between the control modes.

Tests are also conducted to explore the influence of the dc voltage balance control on the neutral-point voltage control. The neutral-point voltages (upper and lower dc capacitors' voltages) of the SM1, 2, 5 and 6 are shown in Fig. 29. It can be seen that the neutral-point voltage of any SM is still balanced under the presented dc voltage balancing control. To further validate the decoupling between the dc voltage balancing control and neutral-point voltage balancing control, an experimental test has been conducted with results shown in Fig.



(a)



(b)

Fig. 27. Operation with hybrid dc voltage balancing control methods. (a) one PI-based controller and seven inverse-droop based controllers. (b) seven PI-based controllers and one inverse-droop based controller.

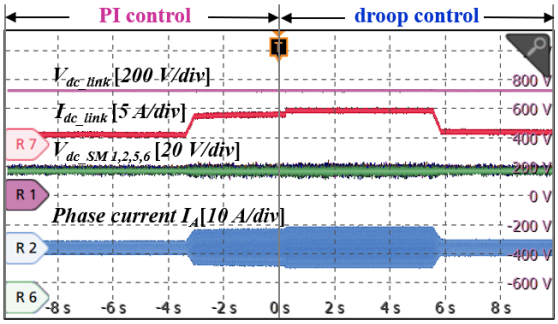


Fig. 28. Waveforms under mode transition.

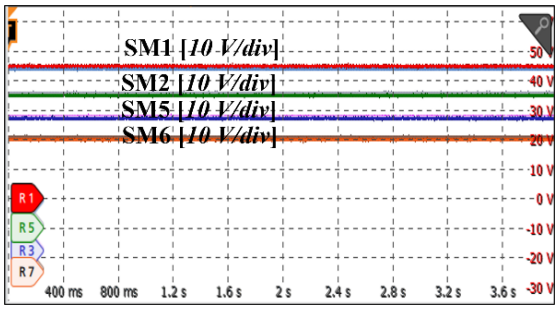


Fig. 29. Upper and lower dc voltage waveforms of SM1,2,5,6 under dc voltage balancing control.

30 (the performance of 4 SMs is shown only). At the beginning of the test, the SMs are equipped with both neutral-point voltage balancing control and dc voltage balancing control. At time 0.8 s, the dc voltage balancing control is disabled. As it can be seen, a divergent dc voltage imbalance occurs afterwards. However, neutral-point voltage balance is still maintained although the dc voltage is unbalanced.

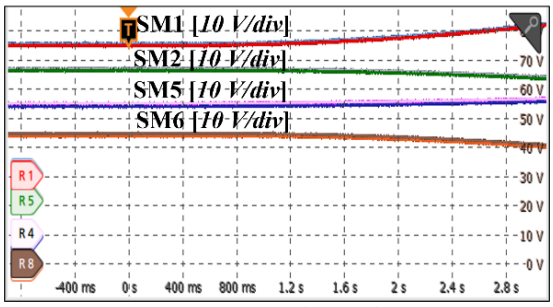


Fig. 30. Upper and lower dc voltage waveforms of SM1,2,5,6 under dc voltage balance and imbalance.

It should be emphasized that the controller parameters in the experimental tests in Section V (see Table III) are smaller than the ones used in the simulations presented in Section III. The reason is that the voltage imbalance is not too severe due to the restricted power condition used in the experiments. Thus, the controller parameters have been selected smaller than the set of parameters used for rated power.

VI. Discussion

A. Design Guidance of DC Voltage Balancing Control for Cascaded 3L-NPC Converters

Some design guidance of dc voltage balancing control for cascaded 3L-NPC converters is provided below.

Firstly, in terms of the selection of control structure, the use of PI-based control for all SMs is recommended when communication works properly. This is due to its precise voltage balancing control and decoupling from the output power. However, upon communication failure, it is recommended that all SMs are switched to inverse-droop based control concurrently to maintain system operation. The hybrid structure is not recommended as SMs using a different type of controller will exhibit different impedance characteristics. Thus, the responses to external inputs such as dc link voltage variations will differ, which influences voltage balancing.

Secondly, to switch from the PI-based control scheme to an inverse-droop scheme, the Modbus protocol between the central and SM controllers is used. Under normal conditions, each SM will return an acceptance flag after receiving voltage information from the central controller. If the central controller does not receive a flag from one SM within a certain time interval, it is considered that the SM has a communication failure. Subsequently, the remaining modules will be notified to switch to inverse-droop control. The SM with communication failure will automatically switch to inverse-droop control if the dc voltage information is not updated.

Thirdly, for cascaded converters with an arbitrary number of SMs, the equivalent impedance can be utilized for stability analysis as well as for tuning the voltage balancing controller. The impedance model of single SM can be firstly derived, and then the system poles can be obtained by aggregating the model of each SM. The dominant system poles can be modified by adjusting controller parameters to provide a desired performance.

B. Control Comparison between MMCs and Cascaded 3L-NPC Converters

To implement the voltage balancing controllers into cascaded 3L-NPC converters, a digital voltage PI controller is added to each SM's controller to modify the PWM duty cycle. However, this is not suitable for MMCs as they have several SMs. Using PI controllers (used with PWM) would require a large amount of PWM ports which cannot be provided by a single microchip. Instead of using a PI-based control scheme, the sorting-based voltage balancing control with nearest-level modulation is always used in the MMC.

In the presented control scheme, a PI/droop-based controller is sufficient to achieve the dc voltage balance. No additional control structure or sensors (except for a dc voltage sensor) are required. In addition, the dc voltage control loop will not influence the dc drift of the neutral-point voltage. Thus, the dc voltage balancing control can be independently designed. It can be concluded that the presented balancing method will not add significant control complexity to the control scheme.

VII. Conclusions

Integration of distributed generators and energy storage devices into distribution networks can be facilitated through the adoption of MVDC technology, in which the cascaded 3L-NPC converter is a promising enabling option. The cascaded 3L-NPC converters have a lower cost compared with MMCs. Due to their economic benefits, they have the potential to be adopted in practical projects such as ANGLE-DC.

DC voltage imbalance across SMs may be exhibited for such converters. This paper reveals the cause of imbalance and presents two control methods to balance the voltages among SMs. Through detailed modeling of the 3L-NPC converter, it is found that dc voltage imbalance is exhibited due to a right half-plane pole in the system. A conventional PI-based method is effective to counteract it. This relies on communications through a central controller, and real-time dc link voltage data is sent to each SM. As the sum of control variables from all PI controllers within SMs is zero, the dc voltage balancing control is decoupled from the power control. Due to this advantage, the PI-based method is adopted as the default controller for voltage balancing. However, there is always the risk to lose communication and, thereby, to exhibit stability issues.

Upon loss of communication, it is shown that an inverse-droop based method may take over the voltage balancing control, offering a good performance. Here, dc voltages are automatically balanced according to the droop characteristics of SMs. This alternative method ensures the continuous operation of the system at the expense of accuracy of output power. Although hybrid configurations featuring PI and inverse-droop based controllers in the same converter station can be adopted, all SMs should be switched to the droop control mode concurrently upon loss of communication at any SM to ensure good transient performance of the system.

The dc voltage balancing control schemes presented in this paper have been verified with simulation results in MATLAB/ Simulink. The effectiveness of the presented control schemes has also been demonstrated using an MVDC experimental testbed with similar per unit values as those of the ANGLE-DC project. The good agreement between experimental and simulation results presented in the paper thus demonstrates the practical relevance of the work.

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Appendix

The voltage equations of the ac side at dq frames are:

$$v_d = \frac{v_{dc}\delta_d}{2} = Ri_d + L\frac{di_d}{dt} - \omega Li_q + v_s$$

$$v_q = \frac{v_{dc}\delta_q}{2} = Ri_q + L\frac{di_q}{dt} + \omega Li_d$$

where δ_d and δ_q are the duty cycles calculated by the current PI controllers:

$$\delta_d = \frac{2}{V_{dc}}\left[k_{pid}(i_d^* - i_d) + k_{iid}\int_0^t (i_d^* - i_d)dt - \omega Li_q + v_s\right]$$

$$\delta_q = \frac{2}{V_{dc}}\left[k_{piq}(i_q^* - i_q) + k_{iiq}\int_0^t (i_q^* - i_q)dt + \omega Li_d\right]$$

where $i_d^* = \frac{2P^*}{3V_s}$ and $i_q^* = \frac{2Q^*}{3V_s}$ are the current references.

The dc side equations are:

$$v_{dc}i_{dc\_conv} = \frac{3}{2}(v_d i_d + v_q i_q)$$

$$C_{dc}\frac{dv_{dc}}{dt} = i_{dc} - i_{dc\_conv}$$

For the state-space representation in (5), let $k_1 = -k_{iid}$, $k_2 = -k_{iiq}$, $k_3 = \frac{1}{L_s}$, $k_4 = -\frac{R}{L_s} - \frac{k_{pid}}{L_s}$, $k_5 = \frac{V_s + RI_d - \omega LI_q}{L_s V_{dc}}$, $k_6 = \frac{1}{L_s}$, $k_7 = -\frac{R}{L_s} - \frac{k_{piq}}{L_s}$, $k_8 = \frac{RI_q + \omega LI_d}{L_s V_{dc}}$, $k_9 = \frac{-3I_d}{2C_{dc}V_{dc}}$, $k_{10} = \frac{-3I_q}{2C_{dc}V_{dc}}$, $k_{11} = -\frac{3V_s + 3(R - k_{pid})I_d}{2C_{dc}V_{dc}}$, $k_{12} = -\frac{3(R - k_{piq})I_q}{2C_{dc}V_{dc}}$, $k_{13} = k_{iid}$, $k_{14} = \frac{k_{pid}}{L_s}$, $k_{15} = \frac{3k_{pid}I_d}{2C_{dc}V_{dc}}$.

The coefficients in equation (7) are:

$a_5 = 1$, $a_4 = -(k_4 + k_7)$, $a_3 = k_4k_7 - k_3k_1 - k_6k_2 - k_5k_{11} - k_8k_{12}$, $a_2 = k_6k_2k_4 + k_7k_3k_1 + k_5k_7k_{11} + k_4k_{12}k_8 - k_5k_9k_1 - k_8k_{10}k_2$, $a_1 = k_6k_2k_3k_1 + k_5k_7k_9k_1 + k_8k_2k_4k_{10} - k_6k_5k_2k_{11} - k_8k_{12}k_3k_1$, $a_0 = k_6k_2k_9k_{11}k_5 + k_3k_1k_2k_{10}k_8$.

The coefficients in equation (10) are:

$a_6' = a_5$, $a_5' = a_4 + k_{pudc}\lambda_4$, $a_4' = a_3 + k_{pudc}\lambda_3 + k_{iudc}\lambda_4$, $a_3' = a_2 + k_{pudc}\lambda_2 + k_{iudc}\lambda_3$, $a_2' = a_1 + k_{pudc}\lambda_1 + k_{iudc}\lambda_2$, $a_1' = a_0 + k_{pudc}\lambda_0 + k_{iudc}\lambda_1$, $a_0' = k_{iudc}\lambda_0$, where $\lambda_4 = k_{15}$, $\lambda_3 = k_9k_{13} + k_{11}k_{14} - k_{15}(k_4 + k_7)$, $\lambda_2 = k_{15}(k_4k_7 - k_1k_3 - k_6k_2) + k_{13}(k_{11}k_3 - k_9k_7 - k_9k_4) + k_{14}(k_1k_9 - k_{11}k_7)$, $\lambda_1 = k_{15}(k_6k_2k_4 + k_7k_3k_1) + k_{13}(k_4k_7k_9 - k_3k_{11}k_7 - k_6k_2k_9) - k_{14}k_1k_7k_9$, $\lambda_0 = k_{15}k_6k_2k_3k_1 + k_{13}(k_6k_2k_4k_9 + k_6k_2k_3k_{11}) + k_{14}k_6k_2k_9k_1$.

The coefficients in equation (13) are:

$a_5'' = a_5$, $a_4'' = a_4 + k_{droop}\lambda_4$, $a_3'' = a_3 + k_{droop}\lambda_3$, $a_2'' = a_2 + k_{droop}\lambda_2$, $a_1'' = a_1 + k_{droop}\lambda_1$, $a_0'' = a_0 + k_{droop}\lambda_0$.

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Jinlei Chen received the B.Eng. and M.Eng. Degrees in Automation from Shandong University, Jinan, China, in 2015 and 2018, respectively. He is currently working toward the Ph.D. degree in electrical engineering with Cardiff University, Cardiff, U.K.

His research interests include modeling and control of medium-voltage dc (MVDC) power converters.

Wenlong Ming (M'16) received the B.Eng. and M.Eng. Degrees in Automation from Shandong University, Jinan, China, in 2007 and 2010, respectively. He received the Ph.D. degree in Automatic Control and Systems Engineering from the University of Sheffield, Sheffield, U.K., in 2015. He is the winner of the prestigious IET Control & Automation Doctoral Dissertation Prize in 2017. He has been a Senior Lecturer of Power Electronics at Cardiff University, U.K., since August 2020 and a Senior Research Fellow funded by Compound Semiconductor Applications (CSA) Catapult, U.K., for 5 years since April 2020.

He was with the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, USA in 2012 as an academic visiting scholar. He has (co-)authored more than 60 papers published in leading journals or refereed IEEE conferences. His research interests focus on packaging, characterisation, modelling and applications of wide-bandgap compound semiconductor power devices.

Carlos E. Ugalde-Loo (SM'19, M'02) was born in Mexico City. He received the B.Sc. degree in electronics and communications engineering from Instituto Tecnológico y de Estudios Superiores de Monterrey, Mexico City, México, in 2002, the M.Sc. degree in electrical engineering from Instituto Politécnico Nacional, Mexico City, México, in 2005, and the Ph.D. degree in electronics and electrical engineering from the University of Glasgow, Scotland, U.K., in 2009.

In 2010 he joined the School of Engineering in Cardiff University, Wales, U.K. He is currently Reader in Electrical Power Systems and Deputy Group Leader of the Centre for Integrated Renewable Energy Generation and Supply. His academic expertise includes power system stability and control, grid integration and control of renewables, dc transmission, modelling and control of integrated energy systems and multivariable control.

Sheng Wang (M'17) received the B.Eng. degree from both Cardiff University, U.K. and North China Electric Power University, China in 2011. He received the Ph.D. degree from Cardiff University, U.K., in 2016. Between 2013- 2014, 2016-2018 and 2018-2020, he was a Research Assistant, a Research Associate and a KTP Associate with Cardiff University, U.K. Since 2020, he has been a Lecturer with the School of Engineering, Cardiff University. His research interests include control and protection of HVDC and MVDC, power electronic devices and compound semiconductor.

Nick Jenkins (M'81–SM'97–F'05) received the B.Sc. degree from Southampton University, Southampton, U.K., in 1974, the M.Sc. degree from Reading University, Reading, U.K., in 1975, and the Ph.D. degree from Imperial College London, London, U.K., in 1986.

He is currently a Professor at Cardiff University, Cardiff, U.K. Before moving to academia, his career included 14 years of industrial experience, of which five years were in developing countries. While at university, he has developed teaching and research activities in both electrical power engineering and renewable energy.

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