OPERATION AND PROTECTION OF VSC-HVDC GRIDS

THESIS SUBMITTED FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

2022

Wei Liu

SCHOOL OF ENGINEERING
CARDIFF UNIVERSITY

To my family

Declaration

This thesis is the result of my own independent work, except where otherwise stated, and the views expressed are my own. Other sources are acknowledged by explicit references. The thesis has not been edited by a third party beyond what is permitted by Cardiff University's Use of Third-Party Editors by Research Degree Students Procedure.

Signed…………………………(candidate) Date …………………..……

STATEMENT 1

This thesis is being submitted in partial fulfilment of the requirements for the degree of ……… (insert PhD, MD, MPhil, etc., as appropriate).

Signed…………………………(candidate) Date …………………..……

STATEMENT 2

This work has not been submitted in substance for any other degree or award at this or any other university or place of learning, nor is it being submitted concurrently for any other degree or award (outside of any formal collaboration agreement between the University and a partner organisation).

Signed…………………………(candidate) Date …………………..……

STATEMENT 3

I hereby give consent for my thesis, if accepted, to be available in the University's Open Access repository (or, where approved, to be available in the University's library and for inter-library loan), and for the title and summary to be made available to outside organisations, subject to the expiry of a University-approved bar on access if applicable.

Signed…………………………(candidate) Date …………………..……

Abstract

Voltage source converter based high-voltage direct-current (VSC-HVDC) systems have shown their advantages over line commutated converter (LCC) based systems in renewable energy integrations, weak ac grid connections and passive network energisations. Worldwide applications of VSC-HVDC have created great potentials to build multi-terminal DC (MTDC) grids to further improve the efficiency and flexibility of power networks.

However, technical challenges still exist in operating MTDC grids safely and reliably. Current flow controls and fault protections within MTDC grids have not been fully addressed and remain critical aspects that need to be further studied. This thesis focuses on conducting investigations on operations and protections of VSC based dc grids.

Current flow controls in meshed MTDC grids are needed to avoid the overload of transmission lines. Analysis of different types of current flow controllers (CFCs) is conducted in this thesis. It is revealed that the half-bridge CFCs (HB-CFCs) are of low cost and high flexibility. A level-shift modulation method, as well as a dual-loop control, is proposed to reduce the switching losses of the HB-CFC and improve its controllability. To guide its controller design, small-signal models of HB-CFCs are derived. The function of the HB-CFC and the effectiveness of the proposed modulation method are verified through simulations.

Protection of dc faults is deemed to be of high cost since dc circuit breakers (DCCBs) are expensive. To cope with this issue, a new device, integrating of DCCBs and HB-CFCs, is proposed. The presented new device can significantly reduce the number of semiconductor devices while containing the functions of the two devices. Detailed analysis of the proposed device is conducted, and simulations are carried out in PSCAD/EMTDC to verify the analysis.

Besides dc faults and grid-side ac faults, valve-side ac faults will induce severe consequences to half-bridge (HB) and full-bridge (FB) modular multilevel converters (MMCs), especially in bipolar HVDC systems. However, fault behaviour and protection methods have not been fully studied for such faults. To bridge this gap, the analysis of valve-side single-phase fault for MMC based HVDC systems are investigated in this thesis. Protection methods against such faults are proposed. For completeness, the effectiveness of the proposed methods is verified by simulations conducted in PSCAD/EMTDC.

The study of this research is expected to contribute to the operation and protection of VSC-HVDC grids.

Acknowledgements

First of all, my most profound and greatest gratitude goes to my supervisors, Prof. Jun Liang and Dr. Carlos E. Ugalde-Loo. It is a great honour for me to be a PhD student of Prof. Jun Liang for the past three and half years. Without his valuable instructions and support, the research work could not reach the same level. It is also a privilege for me to be under the supervision of Dr. Carlos E. Ugalde-Loo. His tremendous support and wise advice have made my PhD study a remarkable and happy journey, which will be treasured for my whole life.

I would like to thank the technical and financial support from the InnoDC project. It is a valuable and memorable experience within the family of InnoDC. Special thanks go to my project manager, Mrs Manon Davies, for her professional support, making my research work go smoothly as planned. I would like to thank all the colleagues in the InnoDC project, especially the Cardiff team, Dr. Peng Yang, Dr. Gayan Abeynayake, and Dr. Davide Pinzan.

I would like to thank the colleagues and friends at Cardiff University, Dr. Gen Li, Dr. Chuanyue Li, Dr. Sheng Wang, Dr. Yue Zhou, Dr. Xiandong Xu and Dr. Wenlong Ming, for their ponderable advice and suggestions during my research.

I would like to thank my supervisors during my secondments in EFACEC, Portugal and CEPRI, China: Mr. Hugo Martins, Mr. Rui Dias Jorge from EFACEC, Prof. Helder Leite from Uporto, and Dr. Yongning Chi and Dr. Yan Li from CEPRI.

My deepest thanks go to my family, especially to my parents and my parents-in-law, for their unconditional love and support.

Last but not least, I would like to thank my beloved wife and son. Xiaoyu, thank you for your understanding and endless love. My life has been lit up since I met you. Thank you, Mingze, for the great joy and happiness you have brought to your Mum and me.

Wei Liu

II

Contents

Abbreviations

ACCB   Alternative current circuit breaker

ANPC   Active neutral point clamped

CFC   Current flow controller

DAB   Dual active bridge

DCCB   Direct current circuit breaker

FB   Full bridge

GaN   Gallium Nitride

HB   Half bridge

HB-CFC   Half-bridge current flow controller

HCB   Hybrid circuit breaker

HVAC   High voltage alternate current

HVDC   High voltage direct current

IGBT   Insulated gate bipolar transistor

LCC   Line commutation converter

LCS   Load commutation switch

LVDC   Low voltage direct current

MB   Main breaker

MMC   Modular multilevel converter

MOSFET   Metal-oxide-semiconductor field effect transistor

MOV   Metal oxide varistor

MTDC   Multi-terminal HVDC

MVDC   Medium voltage direct current

NPC   Neutral point clamped

OHL	Overhead line
PCC	Point of common coupling
PI	Proportional integral
PLL	Phase lock loop
p.u.	Per unit
PWM	Pulse width modulation
RHP	Right-half plane
RES	Renewable energy source
Si	Silicon
SiC	Silicon carbide
SM	Submodule
SFG	Single phase ground
STATCOM	Static synchronous compensator
SSCB	Solid-state circuit breaker
UFD	Ultra-fast disconnector
UPFC	Unified power flow controller
VSC	Voltage source converter
ZOH	Zero-order hold

List of Figures

X

List of Tables

Chapter 1   Introduction

1.1.   Background

With the increasing concerns on climate and environmental changes, policies on net-zero greenhouse gas emissions have been proposed by major countries all over the world.

In June 2019, the UK became the first major country to legislate a net-zero target for carbon emissions by 2050 [1]. The UK government is shaping its policies and regulations to encourage sustainable development to achieve a net-zero for the whole society. In line with the Paris Agreement, the EU aims to be climate-neutral by 2050 - an economy with net-zero greenhouse gas emissions. The EU Commission proposed the first European Climate Law in March 2020 to enshrine the 2050 climate-neutrality target into law [2]. In Asia, on 22nd September 2020, China has announced the "30·and 60" target to peak its carbon dioxide (CO_2) emissions before 2030 and reach carbon neutrality by 2060 [3].

1.1.1.   Renewable energy generation

Renewable energy generations, such as wind power and solar photovoltaic, play a significant role in achieving carbon neutrality [4]. In 2018, the EU had an installed capacity of producing 160 GW onshore and 19 GW offshore wind energy. This accounted for around 14% of the EU's electricity demand [5]. Within the year 2020, the EU installed 14.6 GW new wind capacity and will increase to 105 GW over the next five years [6]. To meet the requirements for a climate-neutral sector in 2050, the capacity will increase from the level of 180 GW to 351 GW in 2030 and around 700-1200 GW by 2050 in the EU. Among them, it has been estimated that around 240 to 450 GW will be from offshore wind, which may supply 30% of the future electricity demand [5]. The UK has the largest installed offshore wind capacity globally, with 9.8 GW installed, which will rise to 19.5 GW by the mid-2020s [7]. In recent years, the capacities of one single wind turbine and the whole wind farm have kept increasing. The rating of the wind turbine manufactured by GE reached 12-13 MW in 2021 [8], and a 16 MW prototype of wind turbine was developed and tested by Mingyang Smart

Chapter 1 Introduction

Energy group in August 2021 [9]. Fig. 1-1 shows the evolution of offshore wind turbines between 1991 and 2021. The capacity may keep increasing to 17 MW by 2035, as shown in Fig. 1-2 [10].
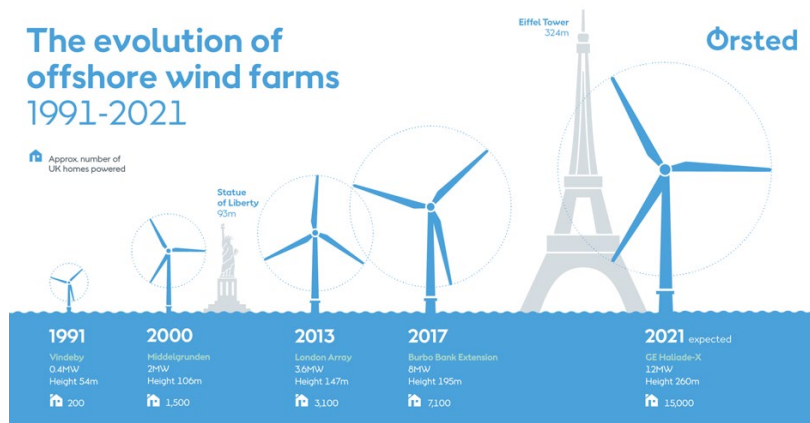
Fig. 1-1. The evolution of offshore wind turbines [13].
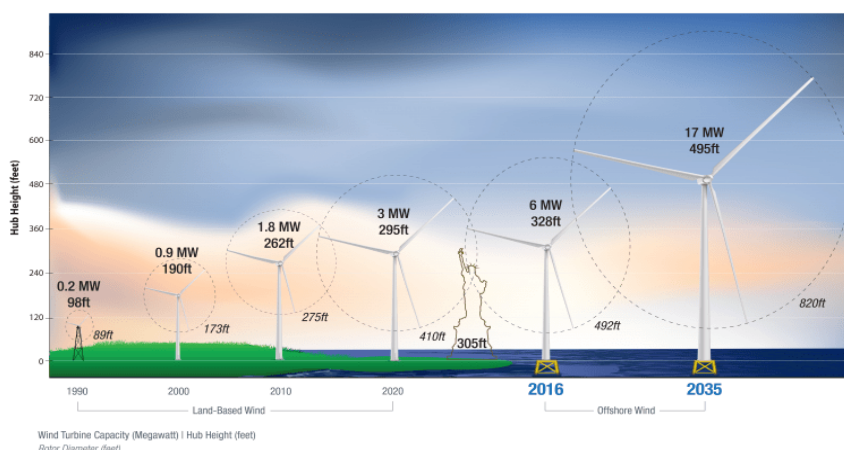
Fig. 1-2. Size of onshore and offshore wind turbines [10].

The largest wind farm was London Array, with a capacity of 630 MW till 2018. Hornsea One project took over the status with a rating of 1.2 GW, which was the first time that the offshore wind farm had ever been built over one gigawatt [11]. Its sister project, Hornsea Two, will take the crown with a capacity of 1.4 GW once operational in 2022 [12]. The newly scheduled project, Dogger Bank wind farm, is estimated to generate 3.6 GW of power when completed in 2026 [8]. By 2030, one-third of the UK's electricity will come from offshore wind [13].

In the meantime, solar power is also developing fast and providing substantial power to the grid. It is estimated by BloombergNEF that solar power has the potential to meet 20% of the EU's electricity demand by 2040 [14].

1.1.2.   VSC HVDC technology

Renewable energy sources (RES) are normally located far away from load centres. Bulk power transmission with low power losses and high reliability is greatly needed. High-voltage direct-current (HVDC), as a power electronics-based technology, enables the transport of electricity over long distances and the integration of high shares of RES into the power system with high efficiency. Line commutation converters (LCCs) dominated this application due to their low cost and power losses at the early stage, which has been widely used for over 70 years [15]. With the fast development of the technologies in power electronics and increasing demands of renewable energy integrations, voltage source converters (VSCs) are exhibiting more advantages over LCCs as the commutation of LCCs is dependent on the stiffness of connected ac grids and the footprints of LLCs are much larger.

In 1997, the first experimental two-level VSC HVDC system (3 MW, ±10 kV) was tested in Hellisjon, Sweden. After that, in 1999, ABB commissioned the first commercial VSC HVDC project (called HVDC Light® by Hitachi Energy) on the island of Gotland in Sweden with a rating of 50 MW, ±80 kV [16]. With the evolution of VSC topologies from two-level, three-level to multilevel (e.g., modular multilevel converter (MMC)), power losses of a VSC HVDC system have been significantly reduced, which has pushed the increasing applications of VSCs in the high voltage area [17]. Thanks to these improvements, VSC-based systems have been widely deployed in practical projects in recent years, especially for offshore wind farms [18]. BorWin1 project was the first offshore wind farm connected onshore grids with the HVDC link (built by ABB). The project was commissioned in 2011 with a power rating of 400MW and a voltage level of ±150 kV [19].

Compared to LCC-based systems, VSC-based technologies can provide extra functionalities: a) full four-quadrant operations with independent active and reactive power control; b) flexible ac voltage control to support weak ac grids; c) capability to black start and feed passive systems; d) flexibility of forming multi-terminal DC grids [20]. Therefore, with such characteristics, VSC-based HVDC is more suitable for large-scale renewable energy integrations.

1.1.3.   VSC HVDC projects

VSC based HVDC projects have been built widely in recent years around the world thanks to the development of MMC based technologies. At the initial stage, most VSC HVDC systems are built as point-to-point or back-to-back configurations. Due to their good power quality performance, flexible control capability and small footprints, VSCs are preferred to be used in many areas, such as interconnectors between different power grids, integrations of offshore wind power, connections of different ac networks and transmissions of bulk power over long distances.

In this subsection, VSC HVDC systems in three typical countries, the UK, Germany and China, are introduced in detail to show their different functionalities. In the UK, at the current stage, VSC HVDC links are mainly used as interconnectors with other countries for power exchange. While in the North Sea of Germany, VSC HVDC links are mostly used to connect with offshore wind farms to integrate wind power into grids. In China, VSC HVDC systems are deployed as connectors between different ac grids to strengthen the ac networks or as links for bulk power transmission to send the power from the western area to its load centres. Typical projects in these three countries are listed below.

a) UK

The UK deployed HVDC links with its neighbouring countries to achieve power balance and enable excess power to be traded between countries. In the early years, four LCC based HVDC links were built up with France, Netherlands, Belgium, and Ireland to exchange power. The first interconnector, the IFA project, was put into operation in 1986, having the capability of transmitting 2000 MW between the UK and France.

With the successful application of VSCs, especially MMCs, most of the current constructed projects are deploying VSC HVDC technologies. Table 1-1 lists the existing and constructing VSC based interconnectors in the UK till now. It can be seen that the power capacities of such links have reached 1400 MW, and the dc-link voltage has reached ±525 kV [27].

Table 1-1. UK's VSC interconnectors with other countries.

Projects	Country Interconnected	Year Commission	Voltage rating	Power rating
East-West Interconnector [21]	Ireland	2013	± 200 kV	500 MW
NeMo [22][23]	Belgium	2019	± 400 kV	1000 MW
IFA2 [24]	France	2020	± 320 kV	1000 MW
North Sea Link[25]	Norway	2021	± 515 kV	1400 MW
Eleclink [26]	France	2022	± 320 kV	1000 MW
Viking Link [27]	Denmark	2023	± 525 kV	1400 MW
FAB Link [28]	France	2025	± 320 kV	1400 MW

b) Germany

Offshore wind energy from the European powerhouse, the North Sea, will play a crucial role in climate neutrality by 2050. Germany has set ambitious goals, achieving 20 GW offshore wind power by 2030 [29]. The commissioned and the under-constructing offshore wind projects in Germany are summarised in Table 1-2. To further increase the pace, 2 GW programs have been set up. It is estimated that, under the 2 GW program, between 2028 and 2030, TenneT will realise at least six 525 kV 2 GW HVDC links at the German North Sea [30].

Table 1-2. VSC HVDC links for offshore wind farms in Germany.

Projects	Year Commission	Transmission distance	Voltage rating	Power rating
BorWin1	2011	200 km	± 150 kV	400 MW
BorWin2	2015	200 km	± 300 kV	800 MW
DolWin1	2015	165 km	± 320 kV	800 MW
HelWin1	2015	130 km	± 250 kV	576 MW
HelWin2	2015	130 km	± 320 kV	690 MW
SylWin1	2015	205 km	± 320 kV	864 MW
DolWin2	2016	135 km	± 320 kV	900 MW
DolWin3	2018	160 km	± 320 kV	900 MW
BorWin3	2019	200 km	± 320 kV	900 MW
DolWin5	2024	130 km	± 320 kV	900 MW
DolWin6	2023	90 km	± 320 kV	900 MW
BorWin5	2025	230 km	± 320 kV	900 MW

c) China

The VSC HVDC technologies have been developing rapidly in China following the first VSC HVDC link commissioned in 2011 at Nanhui, Shanghai. Around ten VSC HVDC projects have been built or are under construction so far in China. Table 1-3 summarises the list of projects. The largest capacity of VSC HVDC stations has reached 5 GW with ±800 kV dc voltages in the Wudongde project, which was constructed by the China Southern Power Grid (CSG). The length of the transmission lines (overhead lines) is around 1450 km. It is the first time that full-bridge FB-SMs (70%) and HB-SMs (30%) are used in one MMC station to handle dc faults [38]. In North China, when commissioned in 2020, the four-terminal Zhangbei project became the first meshed VSC-based MTDC grids globally and operated with 16 DCCBs to protect dc faults [47]. Details on the multi-terminal HVDC projects will be illustrated in Section 1.1.4.

Table 1-3. VSC HVDC projects in China.

Projects	Year Commission	Transmission distance	Voltage rating	Power rating
Nanhui [31]	2011	8.4 km	± 30 kV	18 MW
Dalian [32]	2013	43 km	± 320 kV	1000 MW
Nan'ao [33]	2013	32 km	± 160 kV	200 MW
Zhoushan [34]	2014	134 km	± 200 kV	400 MW
Luxi [34]	2016	B2B	± 350 kV	1000 MW
Yu'e [36]	2019	B2B	± 420 kV	1250×4MW
Xiamen [37]	2015	10.7 km	± 320 kV	1000 MW
Wudongde [38]	2021	1489 km	± 800 kV	8000 MW
Zhangbei [47]	2021	495 km	± 500 kV	3000 MW
Rudong [39][40]	2022	100 km	± 400 kV	1100 MW

1.1.4.　Multi-terminal DC grids

The VSC HVDC systems commissioned in the EU and the UK are all point-to-point links so far. There is a potential to connect the existing HVDC links to form multi-terminal DC (MTDC) grids to promote systems' flexibility and efficiency further [41].

The UK is planning to build a three-terminal VSC MTDC grid in Scotland, the first VSC based MTDC grid in Europe, which aims to connect the Shetland Islands to the Scottish mainland, as shown in Fig. 1-3, to improve the security of power supply for Shetland. The project was awarded to Hitachi Energy by Scottish and Southern Electricity Networks Transmission (SSEN) in 2020 [42].

The Shetland interconnector will be connected with the existing 320 kV Caithness-Moray Link [43] to form an MTDC grid. The commissioning year of this project plans to be 2024. When completed, SSEN can efficiently benefit from both wind and hydropower to increase the reliability and capacity of the power network in the Scotland areas [44].
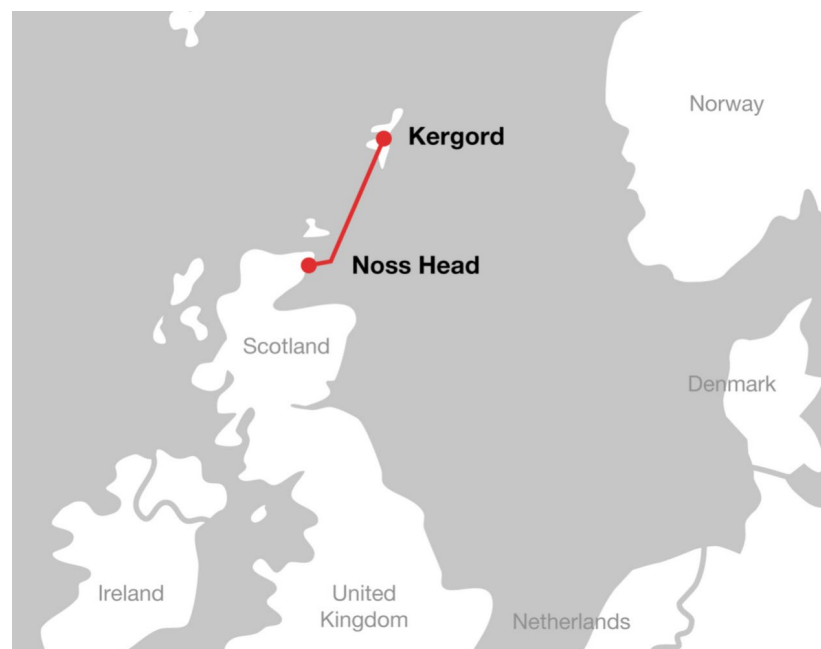
Fig. 1-3. The Shetland link in Scotland [44].

Demonstration projects of MTDC grids have been built in China by its State Grid and Southern Power Grid.

The Nan'ao three-terminal project is the first MTDC grid in the world that employs VSC-based HVDC technology. The dc voltage of the project is ± 160 kV, and the power ratings of the three terminals are 200 MW, 100 MW and 50 MW [45].

A five-terminal VSC HVDC system was built in Zhoushan, China and put into operation in 2014. The dc voltage is ± 200 kV. The capacity of the Zhoushan Station

is 400 MW, which is the largest station in this project. The capacities of other stations are 300 MW, 100 MW and 100 MW, respectively [46].

In Zhangbei, China, a four-terminal meshed HVDC grid, as shown in Fig. 1-4, began its construction in February 2018 and was commissioned in June 2020, which aims to provide up to 3 GW clean wind power to Beijing [47], [48]. The dc voltage of the system is ±500 kV with bipolar configurations. Its corridors of overhead transmission lines cover 227 km in Zhangbei, 126 km in Beijing, 219 km in Fengning, and 66 km in Kangbao areas [49]. The power capacities of Beijing and Zhangbei stations are 3 GW, and the other two stations are 1.5 GW. Pumped hydro storage has been used in one terminal (Fengning Station) to mitigate the intermittent fluctuations induced by wind speed and loads [50]. This project makes breakthroughs in the power capacity, voltage level and configuration of MTDC grids. There are 16 DCCBs deployed in the system to handle dc faults within the grid, which is the first time that DCCBs are commercially used in an MTDC grid [51]-[53]. This project provides a strong reference for future developments of MTDC grids.
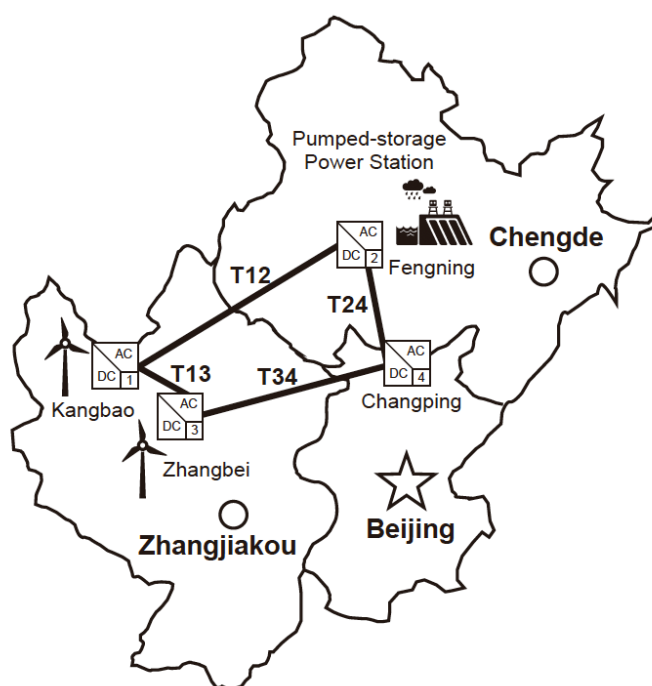
Fig. 1-4. Zhangbei four-terminal MTDC grid [53].

1.1.5.   Technical challenges of VSC HVDC

The deployment of VSC HVDC systems brings advantages when integrating renewable energy into power grids. However, there are still challenges and obstacles on the way to building future HVDC grids [54].

One of the issues within VSC based HVDC systems is the protection of dc faults [55]. No neutral zero-crossings exist in the dc current upon a dc-side fault, making the interruption of fault current more complex than that in an ac system [56]. Therefore, conventional ac circuit breakers are not applicable to a dc grid. On the other hand, since the transients within a dc grid are much faster than those in an ac grid, faster switches are needed to isolate dc faults [57]. DC circuit breakers (DCCBs) with high operating speeds are in great demand. Hybrid DCCBs (HCBs) have been proposed by manufacturers to satisfy these demands [58]-[59]. However, the capital cost of an HCB is still relatively high. The development of a low cost and high reliable DCCB remains an essential topic that needs to be studied.

Meshed MTDC grids are promising solutions in the future to promote system-level flexibility and redundancy of power grids [41], [60]. However, power flows within MTDC grids need to be actively controlled to achieve these goals. Unfortunately, the converters installed at the terminal cannot achieve this task [61]. Therefore, devices with current flow control capability are required for MTDC grids [62]. Otherwise, imbalanced current flows may induce the overloading of transmission lines [63]. Several concepts on power (current) flow control of MTDC grids have been discussed in [64]-[65]. However, detailed control methods on such devices, such as modulations, have not been well presented. The topologies and control methods for these current flow control devices need to be investigated further.

Grid-side ac faults in an HVDC system have been widely analysed with related fault-ride through methods being proposed [66]-[67]. The behaviour of VSCs under grid-side ac fault has been regulated by grid codes [68]-[71]. However, valve-side ac ground fault, which occurs internally between the valve and its interface transformer, remains an area that has not been studied sufficiently. Although the occurrence of this type of fault is low, it may bring severe consequences to a VSC, especially for bipolar systems. Without proper protection methods in place, the fast transients following a

valve-side fault may damage power electronics converters. Protection methods against valve-side ac faults need to be proposed, and, therefore, this topic needs further studies.

In a summary, VSC based HVDC technologies are promising solutions for integrations of renewable energy. The development of MTDC grids can further promote the grid's efficiency and flexibility. However, there are still challenges before MTDC schemes are widely used. For instance, actions on reducing capital costs and power losses, protecting ac and dc faults, controlling dc power flows, and promoting systems' stability and reliability need to be taken. New materials, devices and control schemes still need to be studied to contribute to the development of MTDC grids.

1.2. Research objectives

This thesis focuses on analysing the operations and protections of VSC HVDC grids. The objectives of this thesis include:

a) To investigate current flow control devices (CFCs) for meshed MTDC grids.

b) To develop modulation and control methods for the investigated half-bridge current flow controllers (HB-CFCs).

c) To investigate a low-cost dc protection device integrated with current flow control capability

d) To develop protection methods against valve-side ac faults for HB-MMCs and FB-MMCs in bipolar systems.

1.3. Contributions of this thesis

The main contributions of this thesis are listed below:

a) The operating modes of the HB-CFC have been investigated based on its function when regulating current flows. A level-shift modulation method has been proposed for the HB-CFC, which ensures that only one bridge is modulated by PWM signals for each specific mode. This can reduce the switching power losses and avoid interactions between different bridges, thus, simplifying the control of the HB-CFC. For completeness, small-signal models of the HB-CFC are derived, which provides a reference for designing controllers for the HB-CFC. Both time-domain and frequency-domain simulations have been conducted to verify the analysis.

b) A new device with the capability of dc fault protections and dc current regulations are proposed. HCBs and the investigated HB-CFC are integrated into one single device. Such a combination significantly reduces the number of semiconductor switches. Thus, the capital costs are reduced. The function and effectiveness of the proposed device are verified by simulations in PSCAD/EMTDC.

c) The consequences of valve-side ground faults for HB-and FB-MMCs in bipolar systems are analysed. It is revealed that the absence of zero-crossings of the ac current and SM overvoltage appears when such a fault occurs in an HB-MMC based bipolar system. For an FB-MMC system, such faults may lead to severe SM overvoltage (around 2 p.u.), which may damage the converter. Protection methods for both HB-and FB-MMCs are proposed, with the effectiveness verified by simulation results in PSCAD/EMTDC.

1.4.   Outline of this thesis

The research is conducted through both theoretical analysis and simulation verifications, which focuses on the operations and protections of VSC HVDC grids. The current flow control and dc protections are discussed in Chapters 3 and 4. Besides dc current flow controls and dc protections, valve-side ac faults of MMCs have been investigated in this thesis. Analysis of valve-side ac faults on HB-MMCs is presented in Chapter 5, and on FB-MMCs is presented in Chapter 6.

The outline of the thesis is as below:

Chapter 2: Overview of VSC HVDC technologies

In this chapter, the state-of-the-art VSC based HVDC technologies are reviewed. The topologies of VSCs, their modulation and control methods are summarised first. The configuration of HVDC grids is described in detail. The challenges of operating HVDC links or MTDC grids are analysed. The demands of regulating dc current flow within a meshed MTDC network are elaborated. Furthermore, protections of ac and dc faults for VSC HVDC systems are discussed. Different strategies and protection devices are introduced and compared. Valve-side ac faults may damage power

electronic converters if proper protection methods are not in place. The demands of investigating protection strategies for such faults are highlighted.

Chapter 3: DC current flow controller

This chapter first presents the demands of dc current flow control in meshed MTDC networks, and the background of current flow controllers (CFCs) are introduced. The HB-CFC are studied in detail. Based on its different functions when regulating current flows, four operation modes are classified. Equations are derived under different operating modes. Meanwhile, a level-shift modulation method has been proposed to simplify the control of the HB-CFC. To better operate and control the HB-CFC in an MTDC network, a small-signal analysis has been conducted. The small-signal models obtained have been verified by frequency-domain analysis. Time-domain simulation results are given to verify the proposed scheme.

Chapter 4: DC protection device with current flow control capability

A new device, the CB/CFC, which combines the function of the DCCB with the HB-CFC, is proposed in this chapter to reduce the number of power electronic devices. The proposed device can operate as an HB-CFC to balance current flows and as a DCCB to isolate dc faults. The modulation and control methods proposed in Chapter 3 are extended and deployed by the CB/CFC when regulating current flows. Time-domain simulations are conducted to verify the function of the proposed device in an MTDC grid. The case studies in Chapter 4 further verify the effectiveness of the level-shift modulation and control methods proposed in Chapter 3.

To add further value, the functionality and its consumed semiconductor devices are calculated. The proposed device has been compared with two existing schemes in the open literature. It is revealed that the proposed CB/CFC can further reduce capital costs.

Chapter 5: Protection of valve-side faults for HB-MMCs in bipolar systems

Besides dc protection discussed in Chapter 4, protections of valve-side faults are investigated in this study. In this chapter, the characteristic of valve-side single-phase ground ac faults in an HB-MMC HVDC system is analysed. The critical challenges under such a fault for an HB-MMC, the issues of the absence of zero-crossings, are

illustrated. To protect the HB-MMC following a valve-side fault, strategies are proposed in this section. Simulation results are given to verify the effectiveness of the proposed strategies.

Chapter 6: Protection of valve-side faults for FB-MMCs in bipolar systems

In this chapter, the characteristic of valve-side single-phase ac faults in an FB-MMC HVDC system is analysed. The overcurrent and overvoltage problems caused by such faults are studied. Thyristor-based strategy is proposed to protect FB-MMCs following a valve-side fault. Schemes of installing thyristor at the dc and ac sides are proposed. The characteristics of these two methods are summarised with simulations conducted in PSCAD/EMTDC. To add further values, the presented methods have also been verified in a multi-terminal system. In addition, the post-fault restoration process under a transient fault condition is illustrated.

Chapter 7: Conclusion

This chapter concludes and summarises the thesis. Potential future work is presented.

1.5.   List of publications

The doctoral thesis has resulted in the following publications:

[1] **W. Liu**, C Li, CE Ugalde-Loo, S Wang, G Li, J Liang "Operation and Control of an HVDC Circuit Breaker with Current Flow Control Capability," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 9, no. 4, pp. 4447-4458, Aug. 2021,

[2] **W. Liu**, G. Li, J. Liang, C. E. Ugalde-Loo, C. Li and X. Guillaud, "Protection of Single-Phase Fault at the Transformer Valve Side of FB-MMC-Based Bipolar HVDC Systems," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 10, pp. 8416-8427, Oct. 2020.

[3] G. Li, **W. Liu**, T. Joseph, J. Liang and Z. Song, "Double-Thyristor-Based Protection for Valve-Side Single-Phase-to-Ground Faults in HB-MMC-Based Bipolar HVDC Systems," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 7, pp. 5810-5815, July 2020.

[4] **W. Liu**, J. Liang, C. E. Ugalde-Loo, C. Li, G. Li and P. Yang, "Level-shift Modulation and Control of a Dual H-bridge Current Flow Controller in Meshed HVDC systems," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019, pp. 62-66.

[5] **W. Liu**, J. Liang, C. E. Ugalde-Loo, G. Li, C. Li and F. Colas, "Modeling and Frequency Analysis of a Dual H-bridge Current Flow Controller in Meshed HVDC systems," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, Genova, Italy, 2019, pp. P.1-P.9.

The author has authored and co-authored the following publications during the PhD study:

[1] **W. Liu**, J. Yu, G. Li, J. Liang, C.E. Ugalde-Loo, and A. Moon "Analysis and Protection of Converter-Side AC Faults in a Cascaded Converter-Based MVDC Link: ANGLE-DC Project," *IEEE Transactions on Smart grid (early access).*

[2] **W. Liu**, G. Li, C. E. Ugalde-Loo and J. Liang, "Start-up strategy for modular multilevel converters with modified nearest level modulation method," in *8th Renewable Power Generation Conference (RPG 2019),* Shanghai, China, 2019, pp. 1-6. (3rd prize 'Best Conference Paper')

[3] C. Li, **W. Liu**, J. Liang, X. Ding and L. Cipcigan, "Improved Grid Impedance Compensation for Phase-Locked Loop to Stabilize the Very-Weak-Grid Connection of VSIs," *IEEE Transactions on Power Delivery(early access).*

[4] S. Wang, W. Ming, **W. Liu**, C. Li, C. E. Ugalde Loo and J. Liang, "A Multi-Function Integrated Circuit Breaker for DC Grid Applications," *IEEE Transactions on Power Delivery*, vol. 36, no. 2, pp. 566-577, April 2021.

[5] G. Li, **W. Liu**, T. Joseph, J. Liang, T. An, J. Lu, M. Szechtman, B. Andersen, Q. Zhuang, "Control Strategies of Full-Voltage to Half-Voltage Operation for LCC and Hybrid LCC/MMC based UHVDC Systems," *Energies*, vol. 12, no. 4, 742, February 2019.

[6] G. Li, T. An, J. Liang, **W. Liu**, T. Joseph, J. Lu, M. Szechtman, B. R Andersen, Y. Lan., "Power reversal strategies for hybrid LCC/MMC HVDC systems," *CSEE Journal of Power and Energy Systems*, vol. 6, no. 1, pp. 203-212, March 2020.

[7] G. Li, T. An, J. Liang, **W. Liu**, T. Joseph, J. Lu, Y. Lan. "Studies of commutation failures in hybrid LCC/MMC HVDC systems," *Global Energy Interconnection,* vol. 3, no. 3, pp. 193-204, June 2020.

[8] P. Yang, W. Ming, J. Liang, J. Wu and **W. Liu**, "Reduction of DC-link Ripples for SiC-based Three-phase Four-wire Inverters with Unbalanced Loads," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE),* Baltimore, MD, USA, 2019, pp. 2819-2835.

Chapter 2 Overview of VSC HVDC Technologies

2.1. Introduction

The first commercialised VSC HVDC link constructed by ABB was put into operation in Gotland Island, Sweden, in 1999. Two-level converters were employed with a dc voltage of $\pm$ 80 kV and power capacity of 50 MW. Self-commutating devices (IGBTs) were used to build up the converters. Thanks to the development of power electronics, the level of voltage and the capacity of power for VSC HVDC systems have been significantly increased. By now, the highest dc voltage of the VSC station reaches $\pm$ 800 kV with a power rating of 5 GW, which is ten times the voltage level and one hundred times the power rating of the first VSC HVDC project, respectively [72]-[73]. Besides point-to-point links, meshed multi-terminal DC grids have been constructed. As introduced in Chapter 1, a four-terminal MTDC grid was commissioned in June 2020 with a dc voltage of $\pm$ 500 kV and a power rating of 3 GW in Beijing, China.

In this chapter, an overview of VSC based HVDC technologies will be given. Topologies of VSCs, configurations of VSC HVDC systems, and practical VSC HVDC projects, so far, are summarised. The state-of-the-art for dc circuit breakers and current flow controllers are presented. Protection methods on dc-and ac-faults are reviewed with challenges emphasised.

2.2. VSC HVDC systems

In this section, the topologies of VSCs and configurations of HVDC systems are reviewed.

2.2.1. Topology of VSCs

Power electronic-based converters are key devices for HVDC systems. At the early stage, thyristor-based LCC systems have dominated HVDC projects due to their low capital costs and high-power capacity. With the development of power electronic

devices and related converter topologies, VSCs have shown advantages over LCCs. The topologies of VSCs are summarised next.

a)   Two-level converter

The two-level converter is one of the most frequently used types of VSCs, especially in systems with a voltage level of several kilovolts or below, such as motor drives and PV systems [74]-[75]. The schematic of a three-phase two-level converter is shown in Fig. 2-1. The two-level converter contains a dc bus which is normally provided by a dc capacitor to maintain its dc voltage approximately constant. There are six arms that are built up by fully controllable switching devices. IGBTs with anti-parallel diodes or field-effect transistors (MOSFETs) are mostly used to build up two-level converters. However, in HVDC application areas, series-connected structures have to be used to withstand large voltage (typically tens or hundreds of kilovolts).
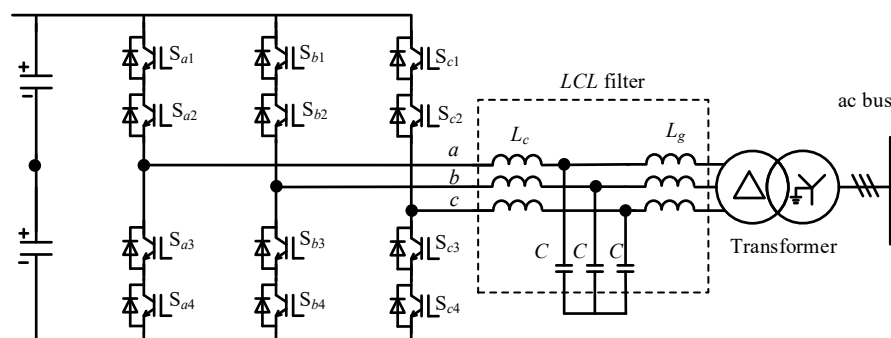
Fig. 2-1. Topology of the two-level converter.

The two-level converter is regulated by pulse-width modulation (PWM) signals. The modulation signals are compared with high-frequency carriers (e.g. triangular carriers) to generate PWM signals, as shown in Fig. 2-2.

When the modulation signal is higher than the triangular carrier, the switching devices in the upper arm are switched on. Conversely, the devices in the lower arm are switched on. In this way, the two-level converter converts the constant dc bus voltage into ac voltages.

However, the output ac voltages typically contain high-frequency harmonics. Therefore, ac filters (*L, LC or LCL* filters), as shown in Fig. 2-1, are needed to remove high-frequency harmonics. A higher switching frequency leads to a higher frequency spectrum of its harmonics. Thus, the sizes and costs of ac filters can be reduced, and

power quality can be improved. However, a higher switching frequency will significantly increase the switching power losses. It is a trade-off to select the switching frequency when designing a VSC. A typical switching frequency of two-level converters in HVDC applications is around 1 kHz or 2 kHz [76]-[77].
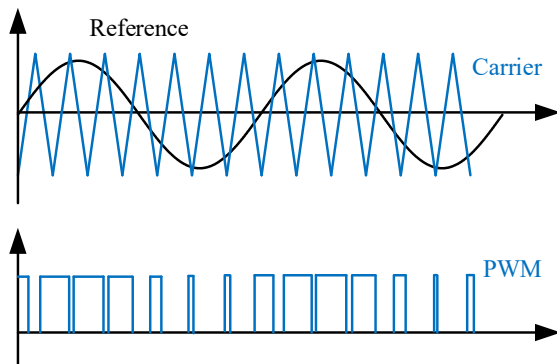
Fig. 2-2. Modulation waveforms of two-level converters.

b) Three-level NPC converter

The three-level neutral-point-clamped (NPC) converter was introduced in early 80s [78]-[79]. Since that, the topology has been widely used in applications with a power rating of several megawatts, such as medium motor drives [80]-[81]. The schematic of a three-level NPC converter is given in Fig. 2-3. Additional diodes are used to clamp the voltages applied to the IGBTs. Compared to conventional two-level converters, the three-level NPC converter provides higher power quality (e.g. fewer harmonics) [78].
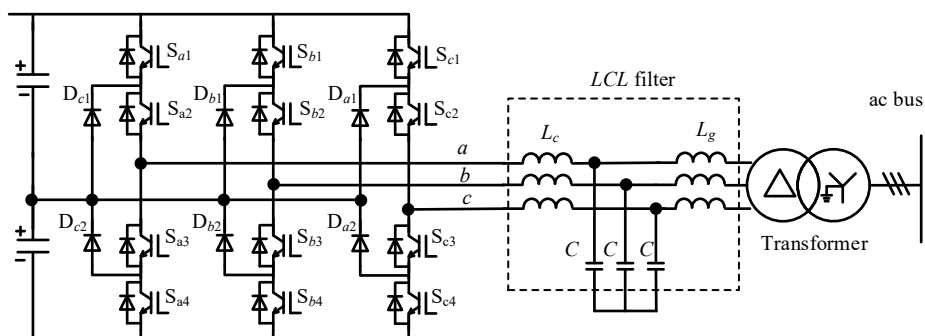
Fig. 2-3. Topology of three-level neutral-point-clamped (NPC) converter.

Therefore, it is an alternative solution for HVDC systems. AC filters are still needed to remove the harmonics caused by the PWM switching. Similar to two-level

converters, switching devices in the three-level NPC need to be series-connected to withstand system-level voltage for HV applications. Several HVDC projects, in the early stage, use such topology instead of two-level converters, such as Eagle Pass in the USA [82].

One of the issues that three-level NPC converters face is that the power losses between different switching devices are not balanced [83]-[85]. This may lead to an over-temperature of semiconductors under some critical conditions. Therefore, overrating design is required. However, the capital costs will, at the same time, be increased. To tackle this issue, the three-level active NPC (ANPC) converter is proposed [86]-[87]. The topology is shown in Fig. 2-4. The replacement of diodes into controllable devices (e.g. IGBTs) ensures that the power losses are better distributed among different devices.
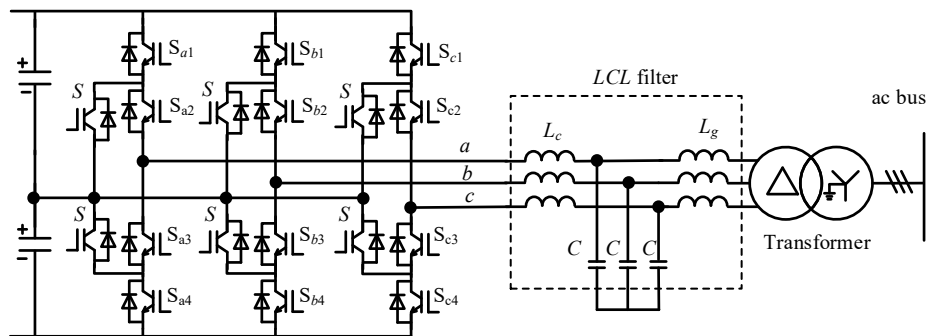
Fig. 2-4. Topology of three-level active neutral-point-clamped (ANPC) converter.

The three-level ANPC converter has been used in several VSC HVDC links. The Murrraylink, located in South Australia and Sunraysia region, was commissioned in 2002 with ANPC converters. The dc voltage of the HVDC link is ± 150 kV, and its power rating is 220 MW[88]. The same topology was used in the CrossSound link in the USA with a power rating of 330 MW and a dc voltage of ± 150 kV. This project was manufactured by ABB and commissioned in 2002 [89].

c) Modular multilevel converter

The modular multilevel converter (MMC) was first proposed by R. Marquardt and A. Lesnicar in 2003 [90]. The first commercial MMC based HVDC system is the ± 200 kV Trans Bay Cable (TBC) project with a power rating of 400 MW, which is located in San Francisco and was completed in 2010 [91]-[92]. Following that, the

MMC has become the most popular and commonly used type of VSCs for HVDC applications. The MMC significantly reduces power losses of VSC HVDC systems and improve their power quality [93]-[94]. By exclusion of large ac filters, the footprint of an MMC based HVDC system is much smaller. Furthermore, due to the modularised concept, the design and implementation of an MMC are technically more accessible than that of a conventional two-level or three-level converter.

Fig. 2-5 shows the topology of an MMC with HB SMs. It consists of three legs for a three-phase application. Each leg contains one upper arm and one lower arm. The arm is built by N submodules (SMs) with a series-connected inductor. The dc voltage is divided by N SMs instead of series-connected switching devices as that of a two-level converter. Therefore, with such a configuration, the voltage balancing issues caused by directly series connected IGBTs are relieved, and the gate signals do not have to be as sophisticated as those of two- or three-level converters [95].
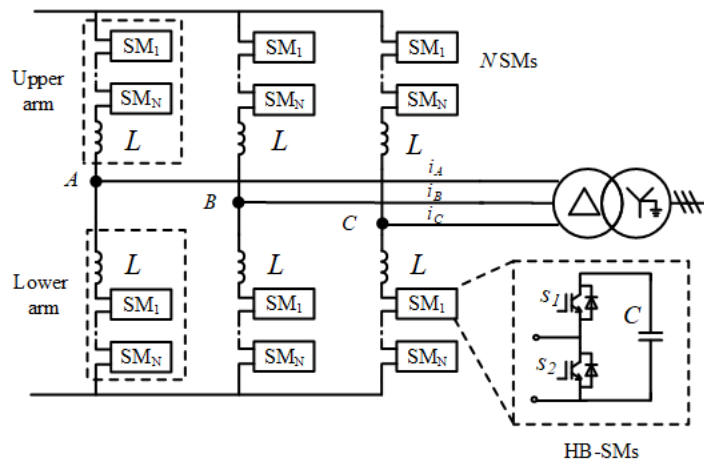
Fig. 2-5. Topology of modular multi-level converters (MMCs).

Since being proposed in 2003, HB topologies have dominated the applications of MMCs due to their low capital costs and power losses [96]. However, HB based MMCs cannot interrupt dc fault currents. The free-wheeling diodes still carry fault currents even when the HB-MMC is blocked, which endangers the safe operation of HVDC systems [97].

To solve this issue, different configurations of SMs have been investigated. Full bridge SMs (FB-SMs) and clamped double SMs (CDSMs) are proposed [96], and their schematics are shown in Fig. 2-6 [98]. When adopting such a topology, MMCs have

the capability to isolate dc faults. Once the gate signals are removed, the dc capacitors of SMs are inserted into the fault paths. In such a way, the fault current will be blocked and reduced to zero in a short time. However, when FB-MMCs are used, the capital costs are significantly increased [99]. Hybrid schemes, such as adopting both FB- and HB-SMs in one MMC, are proposed to reduce the number of semiconductor devices but still with the capability of dc fault isolation [100]. These topologies with capabilities of dc fault handlings are preferred by systems where transient faults occasionally occur, such as transmission line-based systems. FB-MMCs have been discussed in [101]-[104]. A hybrid scheme with both FB- and HB-SMs in one MMC has been used in the Wudongde project [73].

(a) FB-SMs   (b) CDSMs
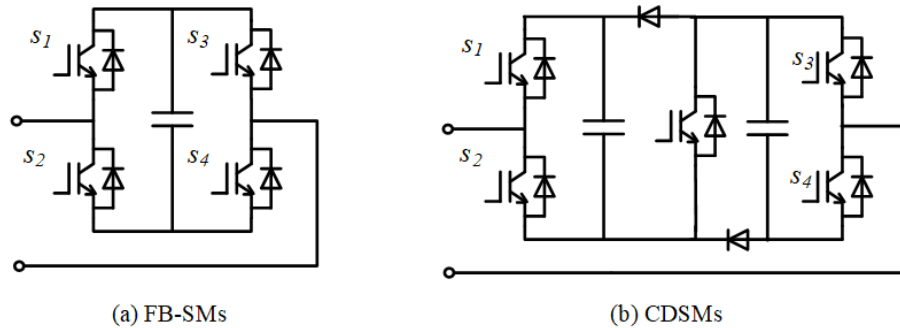
Fig. 2-6. Full bridge and clamped double SMs.

2.2.2.   Configuration of VSC stations

Three basic configurations, i.e. symmetrical monopole, asymmetrical monopole, and bi-pole, are typically adopted by HVDC systems. The configurations of VSC stations and their characteristics will be introduced in this subsection.

a) Symmetrical monopolar system

Fig. 2-7 shows the configuration of a symmetrical monopolar system. For such systems, two fully insulated conductors are adopted. The magnitudes of dc voltage are equal, and their polarities are opposite. Such a system can be grounded through a high impedance at the dc-side at the middle point of shunt capacitors/resistors or ac side through transformers [105]. It should be noted that, with a high impedance grounding, once a pole-to-ground dc fault occurs, the voltage of the healthy pole will increase to around 2 times its rated value [106]-[107]. This should be considered when designing the insulation schemes. Symmetrical monopolar configurations have been widely

employed in VSC HVDC systems at the early stage since the transmission lines only withstand half of the rated dc voltage during normal conditions [108].
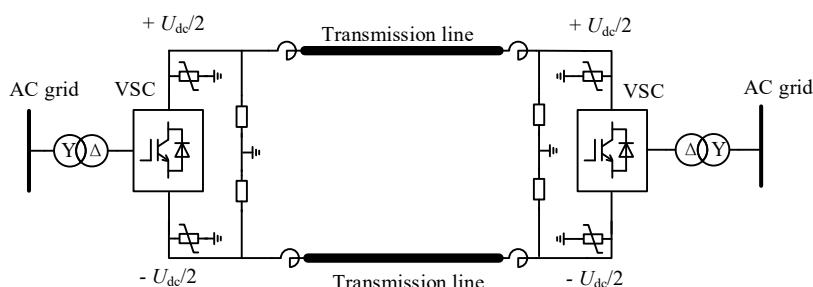
Fig. 2-7. Configuration of symmetrical monopolar system.

b) Asymmetrical monopolar system

Fig. 2-8 shows the configuration of an asymmetrical monopolar system. The system is grounded at its dc-side. Different to a symmetrical system, only one high voltage insulated transmission line is needed in such a system. Natural conductors or metallic returns can be used for the other path with the ground potential. This can reduce the costs and risks of insulation failure for the grounded pole [41]. Omitting the ground conductors may be possible when ground currents are permitted. But it may have influences on the environment [109]. It should be noted that the transformer windings of the secondary side will have to withstand dc offset voltage in such systems, which is half of the dc voltage[110]. This factor should be considered when designing transformers for such systems. So far, only a few projects use such configurations [114].
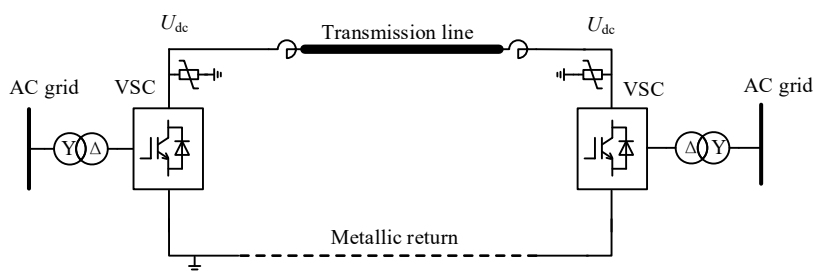
Fig. 2-8. Configuration of asymmetrical monopolar system.

c) Bipolar system

Fig. 2-9 shows the configuration of a bipolar system. A bipolar system can be seen as a combination of two asymmetrical systems. The groundings with the connected

metallic return are shared by the two asymmetrical systems [110]. Each pole has its ac transformers, and under normal conditions, the two poles are operated under balanced modes, which ensures the current at the grounded line is zero. This is needed when the system is directly grounded with the earth or sea. Similar to asymmetrical systems, the transformer of the system needs to withstand a dc component, which is half of the dc voltage [111].
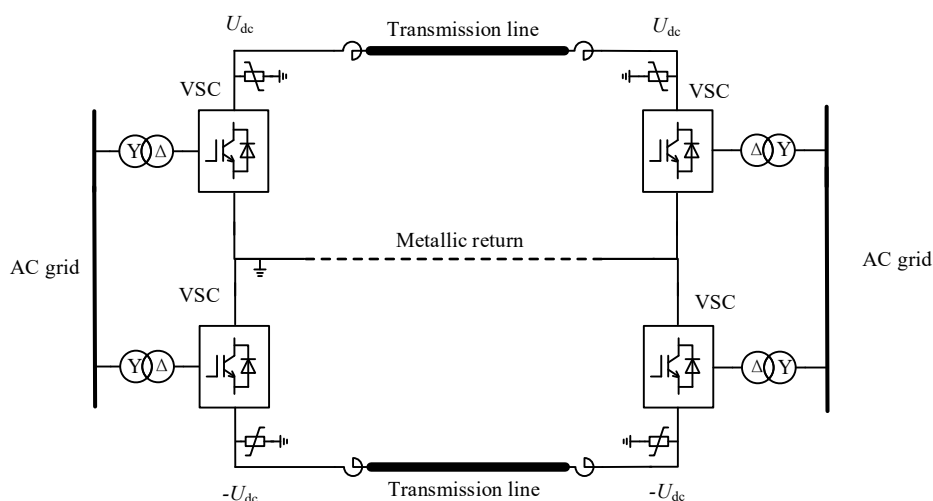
Fig. 2-9. Configuration of bipolar systems.

The two converters in a bipolar system can operate independently. Therefore, 50% of the power capacity is left when one pole experiences a fault or is under maintenance. This improves the reliability of the system [112]. With increasing demands of power capacity, bipolar systems are more and more commonly deployed by VSC HVDC systems [25], [115].

2.2.3.   DC grids

The successful development of point-to-point HVDC links has proven the advantages of HVDC technologies. LCC HVDC systems have been well recognised as solutions for bulk power transmissions over a long distance, interconnectors of submarine cables and connection of asynchronous ac grids [109]. At the early stage, LCC HVDC has dominated practical projects. However, LCC based HVDC systems are not suitable to form an MTDC grid to enhance systems' reliability and efficiency further since the directions of the current of LCCs cannot be reversed [110]. Moreover, the VSC based HVDC technology has broadened the application range of HVDC to

new areas such as connections with weak ac grids, offshore wind farms, and further forming an MTDC grid [41].

Typical types of MTDC grids includes radial and meshed configurations [109]. A string connection of the radial MTDC grid is shown in Fig. 2-10. The radial connection can be extended from point-to-point links. Flexibility is improved by such a configuration in case disturbance occurs for some of the stations [113]. DC circuit breakers are recommended to be installed in case of dc faults and to avoid the outage of the entire network. The three-terminal Nan'ao project and five-terminal Zhoushan project are configured as a radial network [33], [45], [46]. A star connection of MTDC grids, as shown in Fig. 2-11, could be an alternative solution [118]. Switching stations are used to provide connections for different dc lines.
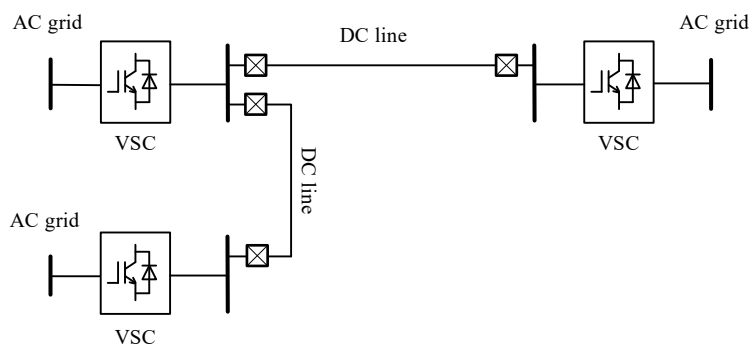
Fig. 2-10. Single line diagram of a string connection of an MTDC grid.
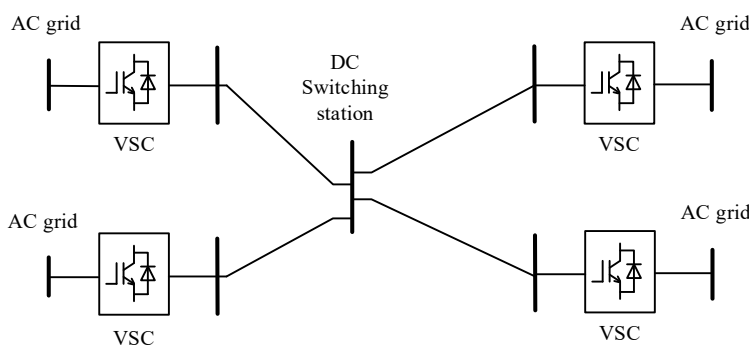
Fig. 2-11. Single line diagram of a star connection of an MTDC grid.

To further enhance the reliability and efficiency, meshed MTDC grids are proposed and developed. A typical diagram is illustrated in Fig. 2-12. The Zhangbei project is configured as a four-terminal meshed MTDC grid to provide redundancy and compensate for the fluctuation of renewable generation [47]. Within such a network,

as paralleled current paths exist, dc circuit breaker and current flow controller are normally required to supervise the operation of the grid.
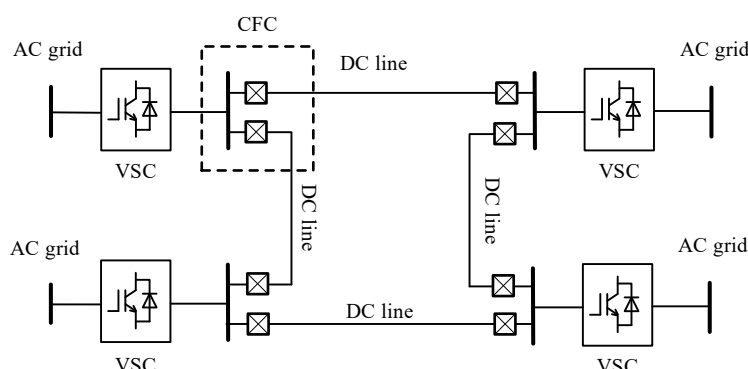
Fig. 2-12. Single line diagram of a meshed MTDC grid.

2.3. Components for implementing MTDC grids

MTDC grids are promising solutions to increase the level of renewable energy integrations. Reliability and flexibility can be improved through establishing dc grids either by connecting existing HVDC links or building new infrastructures [116]. However, there are still obstacles on the way to achieving MTDC grids. The isolation of dc faults, the control of dc power flows, and the connections between different dc voltage levels remain technical challenges [117]. In this section, components used in an MTDC grid to tackle these challenges will be reviewed.

2.3.1. DC circuit breaker

The interruption of dc current is much more difficult than ac due to the absence of neutral zero-crossings. Conventional ac circuit breakers with a mechanical switch cannot be used in a dc system directly [98], [110]. Circuit breakers for HVDC systems should be developed. Different topologies of DCCBs have been proposed. By analysing their mechanism, the types of DCCBs can be categorised into three types, i.e. mechanical circuit breakers, solid-state circuit breakers and hybrid circuit breakers [119]-[121].

a) Mechanical circuit breaker (MCB)

Fig. 2-13 illustrates the typical schematic of a mechanical breaker. Different from a conventional circuit breaker, a resonant branch is added to create zero-crossings for

the current interruption [41]. The load current flows through the mechanical branch under normal conditions with low power losses. When a fault is detected, the resonant branch will generate a resonant current, which helps to create a zero-crossing for the mechanical branch. Thus, the mechanical switch can be open when zero-crossing appears. At the early stage, passive resonant circuits are used. But the time of the appearance of a zero-crossing may still take several ac cycles, and the load conditions influence the behaviour of the passive MCBs [122].
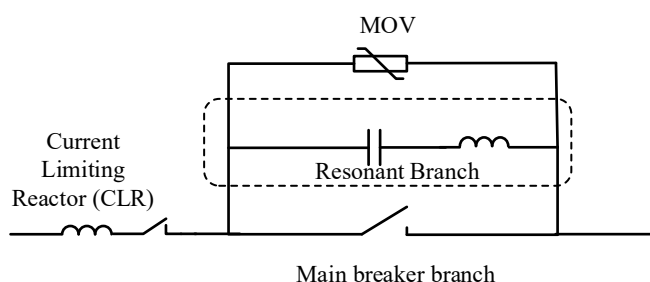
Fig. 2-13. Diagram of a passive mechanical DCCB.

This causes a delay in the interruption of dc faults in an HVDC grid. The active resonant scheme with pre-charged circuits is proposed to reduce the interruption time. A general diagram of active MCB is shown in Fig. 2-14. The capacitors in the resonant path are pre-charged, which will speed up the process of creating zero-crossings. By this method, the time of interruption of a dc fault is reduced [123]. On the other hand, to improve the response of the mechanical switch, electromagnetic forced technology has been proposed [124]. Such schemes have been discussed in MVDC systems [125]-[127].
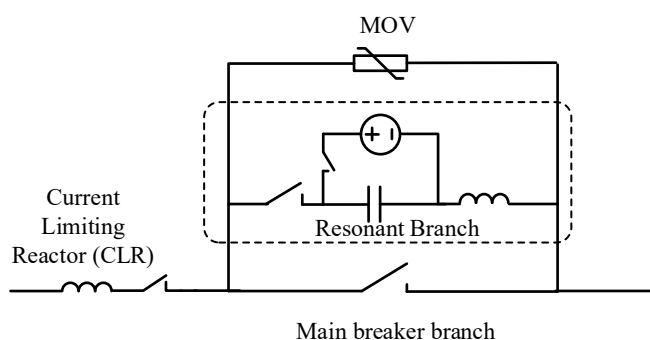
Fig. 2-14. Diagram of an active mechanical DCCB.

With the continuous technical development of MCBs, the operation time has been reduced to around 10 ms. The resonant MCB, deployed in the Nan'ao project and was

put into operation in 2017, has the capability of interrupting a fault current of 9 kA within 3.5 ms [128]. This is the first time that a mechanical HVDC breaker has been used in a multi-terminal dc system [129].

b) Solid-state breaker (SSCB)

Fig. 2-15 illustrates the typical schematic of a solid-state dc breaker (SSCB). To overcome the shortage of a mechanical switch (only can be switched off with a zero-crossing) for dc applications, semiconductor devices are used for SSCBs. As the response time of semiconductor devices are much faster than that of a mechanical device and there is no requirement to wait for a zero-crossing [130], such a configuration is more preferred by a system where high-speed fault isolation is needed [131].
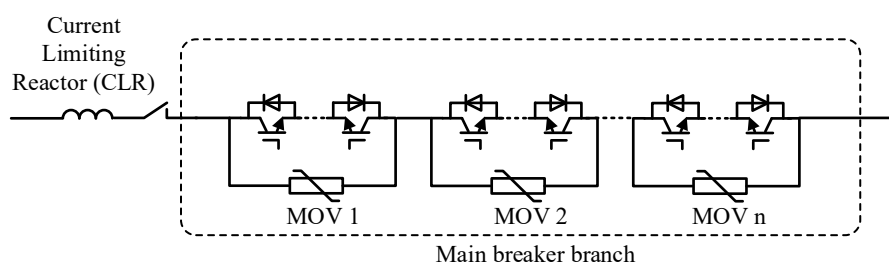
Fig. 2-15. Diagram of a solid-state circuit breaker (SSCB).

As it can be seen, within an SSCB, the semiconductor devices in the main breaker (MB) branch will fully withstand high dc voltages (up to 1.5 to 2 p.u.), a large number of series-connected devices are needed. This brings critical challenges to capital costs and power losses when deploying an SSCB in HVDC systems [41]. The power losses are much higher than that of an MCB since the voltage drop of the series-connected semiconductor devices is larger than mechanical conductors [130]. Due to this reason, by far, no SSCBs have been used in HVDC systems.

c) Hybrid circuit breaker (HCB)

To mitigate the shortcomings of the low operating speed of an MCB and the high power losses of an SSCB, hybrid concepts have been proposed. The schematic of a hybrid circuit breaker is shown in Fig. 2-16. Compared with the topology of the SSCB in Fig. 2-15, it can be seen that a new low-loss branch, consisting of a mechanical switch and several semiconductors, is added [132]. During normal conditions, the load

current flows through the low-loss branch. As the number of semiconductor devices in the low-loss branch is much smaller than MBs, power losses are significantly reduced compared to an SSCB.
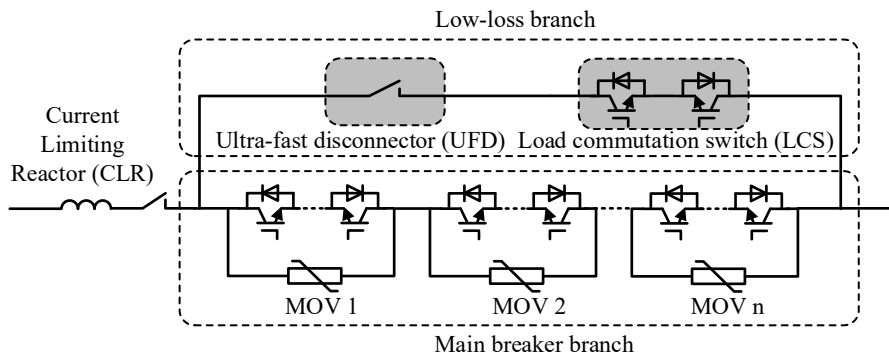
Fig. 2-16. Diagram of a hybrid circuit breaker.

The first prototype of the HCB is proposed by ABB with the capabilities of interrupting 8.5 kA dc current in a 320 kV system [132]-[133]. Following that, an FB-SM based HCB is proposed. Its schematic is given in Fig. 2-17. With such a topology, the direct series-connected scheme is avoided. The capacitors in the FB-SMs can help to balance the transient voltages during the fault interruption process [134]. This topology has been used in the Zhoushan project in Zhejiang, China [135].
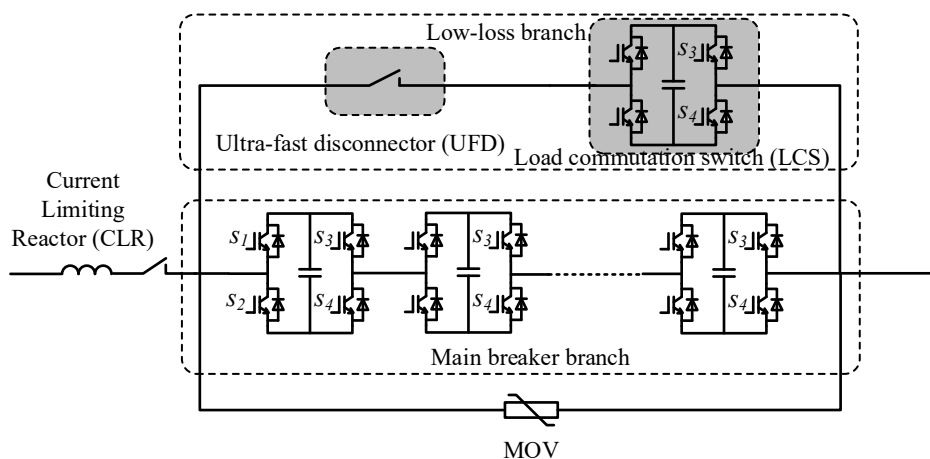
Fig. 2-17. Schematic of an FB-SM based HCB.

As the cost of a diode is lower than that of an IGBT, a diode-based HCB is proposed. The schematic is illustrated in Fig. 2-18. A diode rectifier is used in this topology. By such a configuration, using unidirectional devices to interrupt bidirectional current is possible. Therefore, 50% of switching devices (IGBTs) in the main breaker branch

can be saved, and it leads to a reduction of capital costs [137]. Such a topology has been used in the Zhangbei project with a dc voltage rating of 500 kV. The capability of the current interruption is 25 kA with a time of around 3 ms [136]-[137].
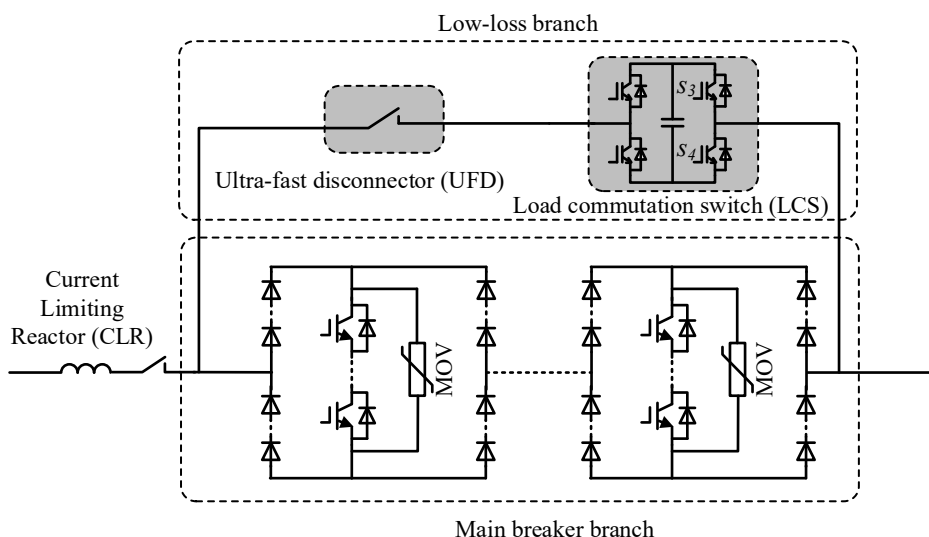
Fig. 2-18. Schematic of the diode-based HCB.

HCBs exhibit promising solutions for HVDC applications as they have low power losses, which is similar to an MCB during normal conditions. And they can operate within several milliseconds, which satisfy the requirements of protection for HVDC systems. However, the costs of HCBs are still concerns as including them within an MTDC grid may significantly increase the capital costs of the whole system. Cost-effective protection schemes still remain areas that need further study. This will be discussed and investigated in Chapter 4 of the thesis.

2.3.2.   Current flow controller

Within a transmission network, power flows or current flows are dependent on the interaction of power generations and consumptions as well as available transmission paths [138]. Without a good supervising of power flows in meshed networks, some transmission lines may be lightly loaded while the other overloaded since the power is not directly controlled by generators or converters. Therefore, to solve this issue, power flow controllers for ac systems or current flow controllers (CFCs) for dc systems are needed [139].

For ac systems, devices and control strategies have been deployed to manage power flows. Inductors and/or capacitors can be used to regulate power flows as they can absorb or inject reactive power and change the impedance of transmission lines, thus, changing power flows [140]. From control perspectives, the tap setting of transformers, the control signals of active and reactive power for generations can be changed to influence power flows [141]. UPFCs have been investigated to effectively regulate power flows for ac networks. A 500 kV UPFC has been put into operation in 2017 [142]-[143].

Different to an ac system, the inductance of transmission lines will have no influence on the steady-state dc power flows in MTDC networks. The devices and control strategies applied to an ac system are not applicable to dc systems. Current flow controllers (CFCs), specially designed for dc systems, are needed.

a) Series resistance

At steady states, only the resistance of transmission lines influences current flows within dc networks. One of the ways to regulate current flows in transmission lines is inserting resistors into related transmission lines [144]. The schematic is shown in Fig. 2-19. To change the values of inserted resistance, normally, power electronic switches can be used in parallel with the resistors. By switching on and off the power electronic switches, the equivalent resistance inserted can be changed accordingly. The structure of this method is simple. However, this method will bring additional power losses and large cooling systems are needed to dissipate the heat [145]. Due to these reasons, the method has not been widely used in HVDC systems.
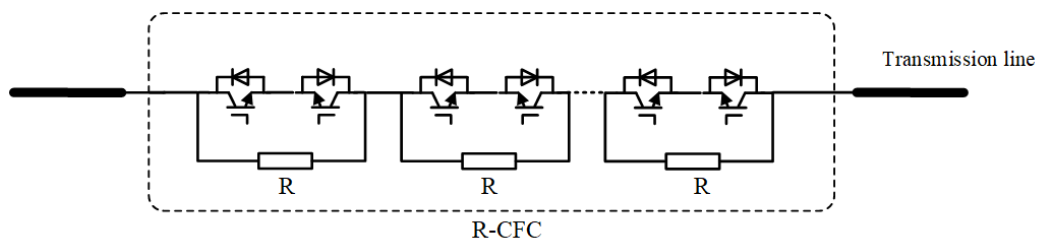
Fig. 2-19. Resistor-based CFC (R-CFC).

b) Series voltage source converter

To mitigate the disadvantage of the resistor-based method, i.e. consuming a large amount of energy and generating considerable heat, active based methods are

proposed. Voltage source-based devices are inserted into transmission lines to regulate current flows [146]. A schematic of the voltage source-based method is shown in Fig. 2-20. The device exchanges power with its connected grid. In such a way, power losses can be significantly reduced. However, such topology brings another aspect that needs to be considered. The insulation level of such a device is high. The footprint of ac transformer is quite large, which will enlarge the size and capital cost of the device [147]. This will limit the number of these devices used in HVDC systems.
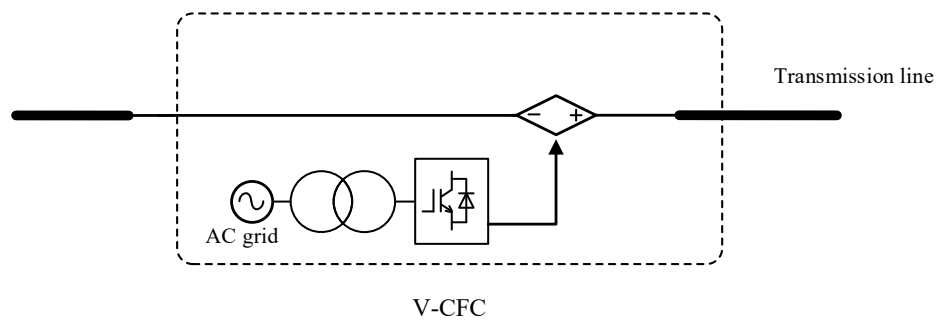
Fig. 2-20. Series voltage source-based CFC (V-CFC).

c) Interline CFC

Concepts of interline CFCs are proposed to tackle the previous issues [148]-[150]. Instead of exchanging power with nearby ac grids, the interline CFC balances current flows between different dc lines [151]. The device is directly inserted into nearby dc transmission lines, as shown in Fig. 2-21. No insulation transformers are needed. Therefore, its footprint is much smaller.
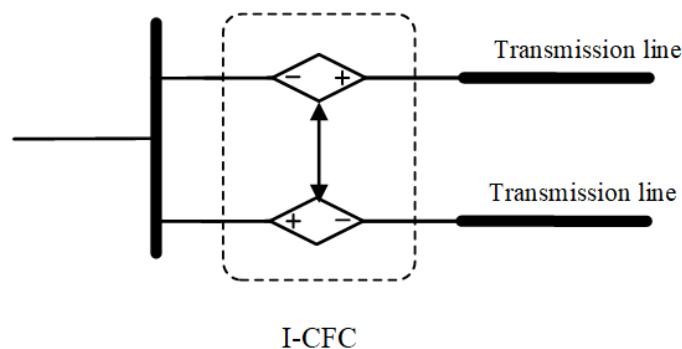
Fig. 2-21. General diagram of interline CFC (I-CFC).

The dual H-bridge CFC has been discussed in [152]-[153]. Its topology is shown in Fig. 2-22 as it can be seen that the two H-bridges are connected with a common dc bus. PWM signals can be applied to the H-bridges to regulate current flows between

its connected two transmission lines. Since the device is in series with transmission lines, the isolation transformer is eliminated.

This topology is a promising solution with low capital costs and small footprints. The modulation and control of such a topology have been investigated [150], [152]. However, they cannot ensure a smooth transfer between different operating modes. The direction of the current in the transmission lines has to be detected to generate control signals[152]. This will complicate the control scheme and detailed analysis has not been given. The operation and control of such devices will be further investigated with the level-shift modulation method proposed in this thesis.
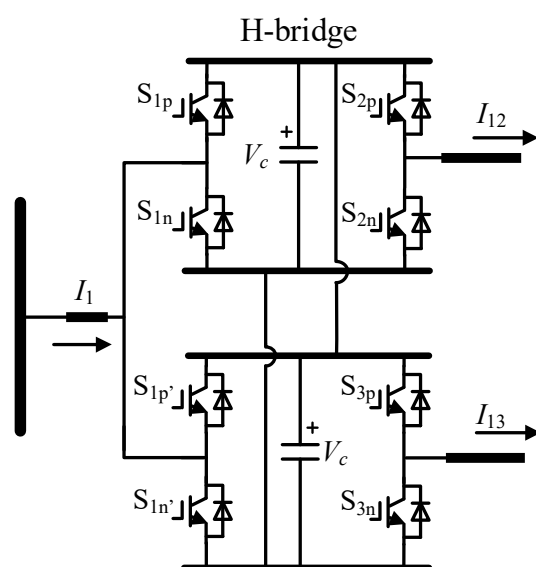
Fig. 2-22. Diagram of dual H-bridge CFC.

2.3.3.　　DC transformer

With the rapid development of dc technologies, HVDC systems with different voltage levels have been built recently. DC lines with different voltage ratings need to be connected in the future, forming a dc grid to increase the system's flexibility and reliability. Similar to the requirements of ac transformers in ac systems, dc transformers are needed to ensure the connection of dc lines with different voltages.

However, conventional ac transformers cannot be used in a dc system since pure dc systems cannot generate alternating flux for conventional transformers [154]. To solve this issue, power electronics-based DC/DC converters are investigated to serve as dc transformers [155]. The schematic of a typical dc transformer is shown in Fig.

2-23. As it can be seen, two DC/AC converters are connected through ac transformers. The DC/AC converter will provide ac components to feed the ac transformer. The ac transformer provides the conversion ratio between the connected two dc lines [156]. For a dc transformer, high/medium frequency ac transformers can be used to reduce the sizes and weights and, thus, reduce their costs [157].
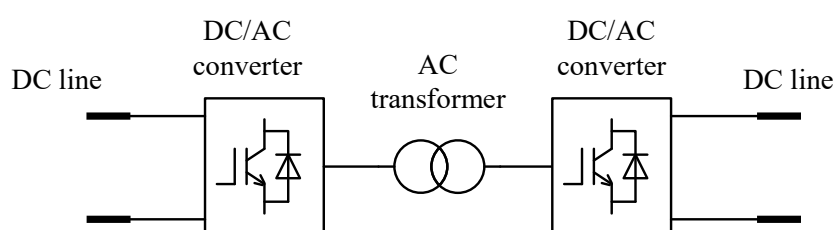
Fig. 2-23. Typical schematic of dc transformers.

Based on different applications, topologies of DC/AC converters can be designed specifically. DABs and MMCs are the most common investigated topologies [158]-[159]. The topology of a DAB converter is shown in Fig. 2-24. The DABs are more suitable for MVDC and LVDC systems with soft switching technologies, which can provide a high-efficiency power conversion. But it may not be suitable for HVDC systems. MMC based dc transformers, as shown in Fig. 2-25, are promising candidates for HVDC systems as the voltage stress can be reduced [156]. The study of this thesis will not cover research on dc transformers, but this will be included in future work.
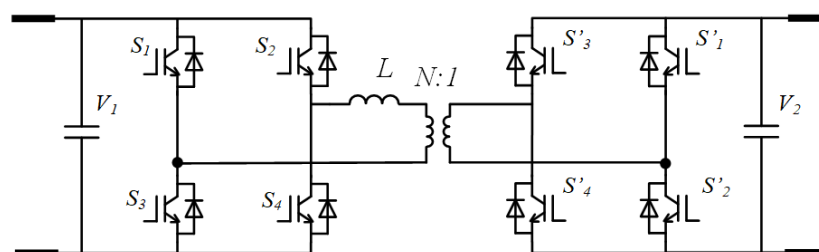
Fig. 2-24. Topology of the dual active bridge (DAB) converter.

33
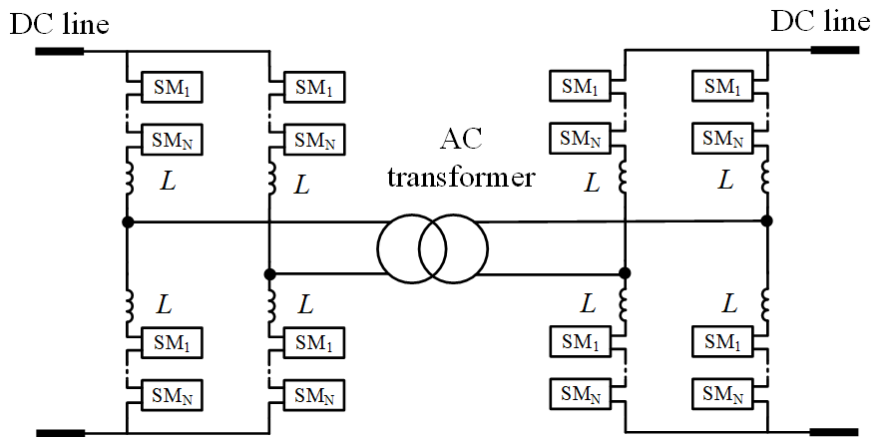
Fig. 2-25. Typical schematic of MMC based dc transformer.

2.4. DC fault protection

DC fault protection remains a critical area for VSC HVDC systems. Fast, economical, and discriminative dc fault protection methods are in great demand for building an MTDC grid [41]. Although a number of HVDC links and MTDC grids have been commissioned or are under constructed, effective dc protection methods with economical protection devices still need further study. So far, there are three solutions to address dc faults for VSC HVDC systems, which will be reviewed next.

2.4.1. Protection with ac circuit breakers

As analysed in section 2.2.1, two-level VSCs or HB-MMCs cannot interrupt dc fault currents due to the free-wheeling diode effects. Therefore, additional devices are needed to handle dc faults [110].

ACCBs are the most economical solutions and have been deployed in point-to-point VSC HVDC links at the early stage before DCCBs are commercially available. When a dc fault occurs, VSCs will be blocked to protect IGBTs from overheating. However, the fault current will continue to flow through the free-wheeling diodes, as shown in Fig. 2-26. The grid-side ACCB has to be tripped to interrupt the fault current.

However, it takes time (several fundamental cycles) for ACCBs to be fully opened. Before that, the free-wheeling diodes take the fault current. This will add stress to the MMCs and may endanger their safe operation. Thyristors are mostly installed in the SMs of MMCs, i.e. parallel with the diodes of the lower devices in the SMs, to reduce the thermal stress of diodes [160].

With this scheme, the fault isolation process usually takes several hundred milliseconds. It may influence the connected systems, especially in an MTDC grid, where the long outage will interrupt power transmissions. Therefore, protection methods with ACCBs are mostly deployed by point-to-point HVDC links.
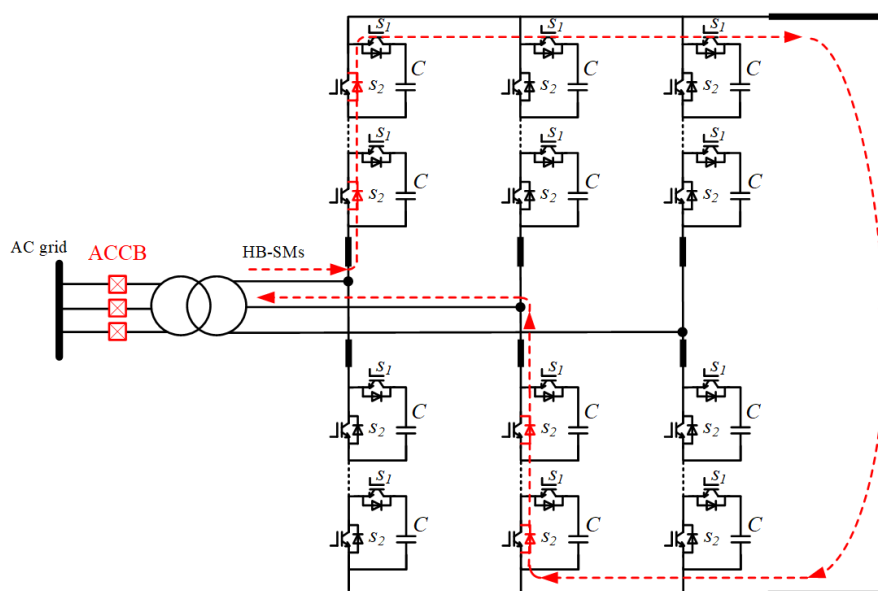
Fig. 2-26. Fault current path when dc faults occur in HB based MMC systems.

2.4.2. Protection with dc circuit breakers

The response time of DCCBs is much faster compared to ACCBs. The dc breaker is installed in series with dc transmission lines. When a dc fault occurs, the DCCB is switched off to interrupt the fault current. Thus, the free-wheeling effects are eliminated[134]-[136]. This is shown in Fig. 2-27.

Hybrid dc circuit breakers have been investigated a lot since being proposed. The operating time of a hybrid circuit breaker is normally 3-10 ms [132]-[133]. In an MTDC network, faulted parts need to be isolated in a short time, while other healthy parts need to remain in operation to reduce the fault impact on the entire system. It exhibits great advantages of using a DCCB compared to an ACCB regarding the time response. DC breakers have been used in several demonstrated projects to evaluate performance in recent years [134]-[137]. At the current stage, the capital cost of a DCCB remains a concern, which is still an obstacle before wide deployment.
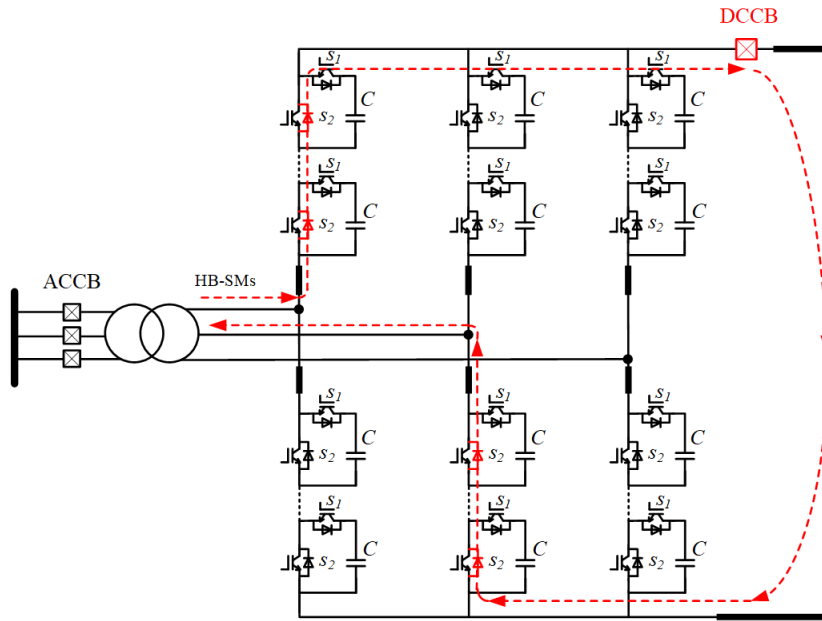
Fig. 2-27. DC circuit breaker interrupts fault current in an HB-MMC system.

2.4.3.   Protection with fault handling converters

As presented in section 2.2.1, modified topologies of MMCs can interrupt dc fault current. Therefore, deploying converters with capabilities of dc fault isolation serves as an alternative solution.

Taking the FB-MMC and CDSM as examples, when a dc fault occurs, the FB-MMC and CDSM can be blocked to interrupt the fault current path. Different from an HB-MMC, the capacitors of SMs are inserted into the current path. This is shown in Fig. 2-28. Therefore, the dc current will decay to zero [98]-[99]. Following that, disconnectors can be used to isolate the faulted part, and other parts can restore to normal operations. It should be noted that the FB-MMCs have the capability to control their dc side voltage to zero or even reverse its dc side voltage [161]. This characteristic may be used to help to extinguish the transient arcs by generating a negative voltage to the system [39]. Therefore, it is preferred by transmission line based HVDC systems.

However, compared to HB-MMCs, the capital costs and power losses are higher. It is a trade-off when selecting a scheme of FB-MMCs or HB-MMCs together with DCCBs. So far, the hybrid topologies (combination of HB-and FB-SMs as shown in Fig. 2-29) have been used to reduce the costs and power losses.

(a) FB-SMs (b) CDSMs
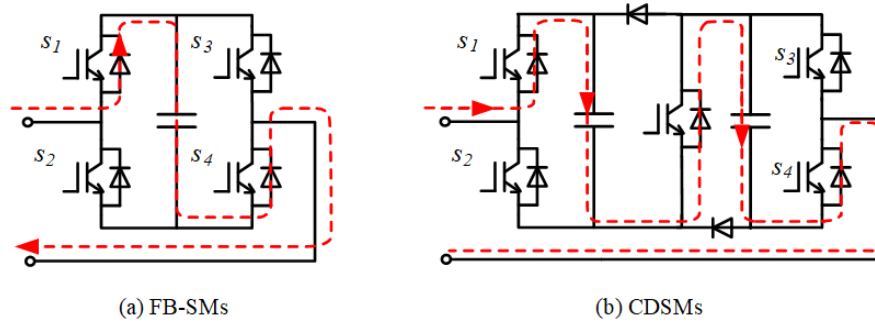
Fig. 2-28. DC fault current paths when FB-SMs and CDSMs are blocked.
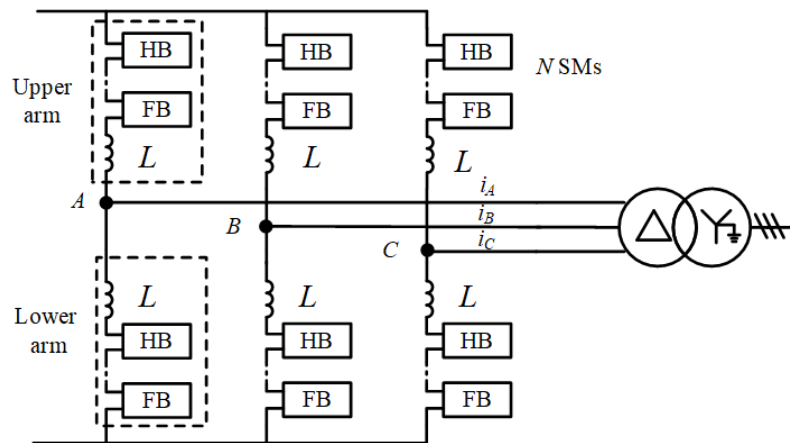
Fig. 2-29. Combination of HB-and FB-SMs in one station.

2.5. AC fault protection

2.5.1. Grid-side ac fault

AC fault ride-through and protection remain important aspects in VSC HVDC systems. Different to LCCs, self-commutated device based VSCs have the capability to fully control the ac side voltages. Therefore, VSCs can ride through grid-side ac faults and, moreover, contribute to the restoration of their connected ac systems [110].

Occurrences of grid-side ac faults, as shown in Fig. 2-30, normally leads to unbalanced grid side ac voltages at the point of common coupling (PCC). This will influence the operations of phase lock loops (PLLs) and current controllers of VSCs, which may cause distortion to the output current [110]. The unbalanced currents and voltages result in uncontrolled oscillations of the active and reactive power delivered to the network. At the same time, the unbalanced power may generate oscillations on the dc voltage of the VSCs.
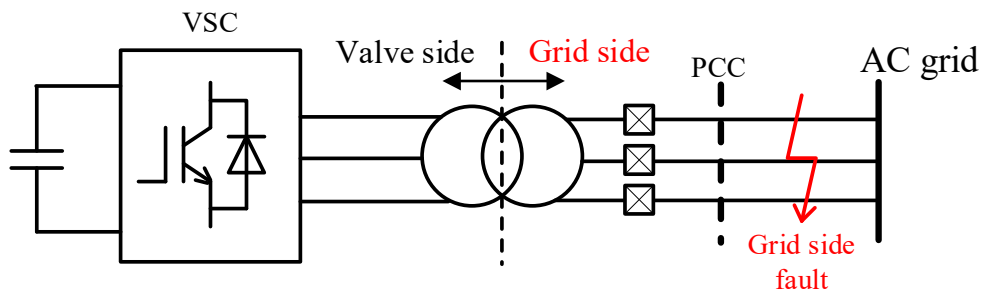
Fig. 2-30. Grid-side ac faults in a VSC HVDC system.

To mitigate the influence, the decoupled double synchronous reference frame PLL (DDSRF-PLL) and the double second-order generalised integrator PLL (DSOGI-PLL) have been proposed to better synchronous unbalanced grids [162]-[163]. Based on the above modified PLLs, positive and negative sequence current controllers can be set up to manage related components, and their control reference will be selected based on grid codes accordingly. For MMCs, the voltage balancing algorithms of their SMs also need to be considered. This has been discussed in [164]-[165].

2.5.2.   Valve-side ac fault

Grid-side ac faults have been investigated, and the behaviour of MMCs following the fault has been requested by grid codes.

However, valve-side ac faults, which occurs in the area between the converter and its connected ac transformer, as shown in Fig. 2-31, have not been fully studied. Although the possibility of occurrence of such faults is quite low, a valve-side ac fault may lead to severe consequences for HVDC systems.
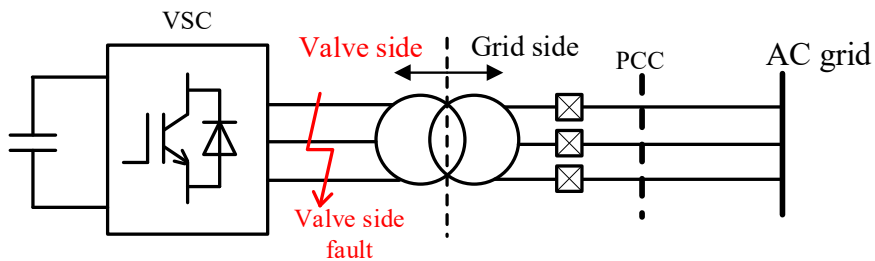
Fig. 2-31. Valve side ac faults in a VSC HVDC system.

Power electronic converters are installed in the station halls, while their transformers are typically installed outside the station hall. Wall bushings are used to maintain the insulations, where conductors need to protrude the hall wall. The

insulation failure or flashover of wall bushings and transformer windings leads to a valve-side ac fault. Both LCC and VSC systems have experienced such faults in practical projects [166]-[168].

Among different types of valve-side ac faults, single-phase ground faults are the most common ones. And due to the zero-sequence path involved by ground faults, large fault current and/or transient overvoltage will exhibit. When it occurs in different systems, the consequences are different. Analysis and protection methods need to be further studied on such faults.

When such a fault occurs in an LCC based HVDC system, commutation failure will be induced [169]-[170]. For a symmetrical VSC based HVDC system, the fault can result in a dc bus voltage oscillation as shown in Fig. 2-32, and the pole-to-ground voltage can reach a magnitude around 2 p.u. The insulation level of dc lines in such a system should be carefully designed. Arrestors need to be installed to avoid severe overvoltage.
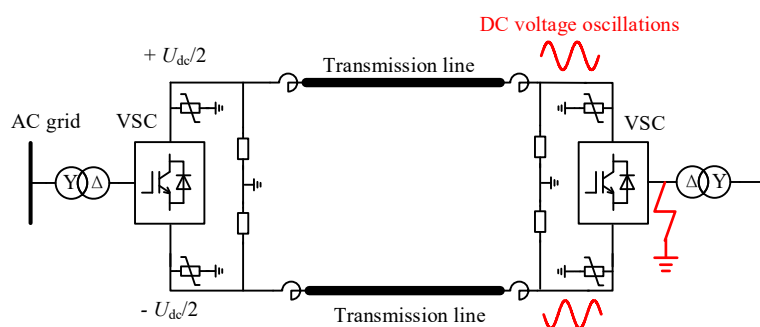
Fig. 2-32. Valve side ac faults in a symmetrical VSC HVDC system.

Different to symmetrical systems, low impedance groundings are adopted in an asymmetrical or bipolar system. Valve-side ac ground faults will generate large zero-sequence currents in such a system. For the faulted phase, its voltage remains to zero. However, the voltages of the non-faulted phases exhibit negative cycles following the valve-side ground fault. These negative cycles will induce fault current through the free-wheeling diodes in the lower arms of two-level VSCs, three-level VSCs or HB-MMCs [171]. An HB-MMC based system are given in Fig. 2-33 as an example to show fault behaviours of valve-side ground ac faults. The fault current flows from the free-wheeling diodes in the lower arms even after the gate signals of IGBTs are removed. Therefore, ACCBs have to be used to interrupt such fault currents. However,

due to the uni-directional conduction of the diodes (as shown in Fig. 2-33), the generated large fault current contains dc offsets. The grid-side currents are lack of zero-crossings due to these dc offsets. The grid-side ACCBs cannot be switched off in time due to the absence of zero crossings [172]. Protection methods against such faults needs to be developed. The analysis on such faults for HB-MMC based systems will be given in Chapter 5 with protection methods proposed.
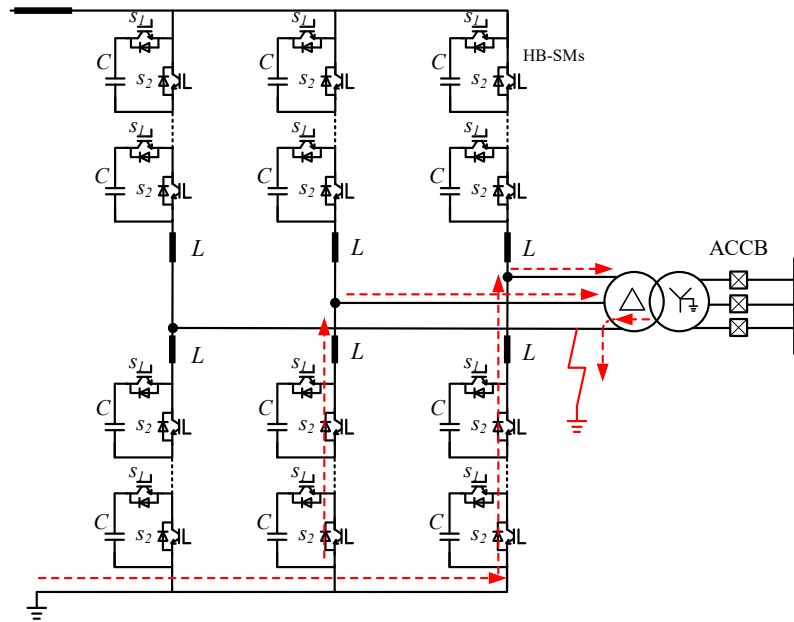
Fig. 2-33. Fault current paths for an HB-MMC system following a valve-side ac ground fault.

The free-wheeling diode effects will not appear in FB-MMC systems. When the gate signals are removed, the FB SMs will interrupt the fault current paths in the lower arms. However, the overvoltage issues will appear. The dc-link charges SMs in the upper arms. Severe overvoltage (around 2 p.u.) will exhibit in their SMs in the upper arms without proper protection in place. Arrestors are normally used to clamp and reduce the level of overvoltage. However, around 1.5 p.u. overvoltage still exists [173]. Further studies still need to be conducted.

The study on protection methods for VSC HVDC systems under valve-side ac faults remains an important area. However, such fault analysis has not been fully conducted, and related protection methods have not been fully investigated for MMC based bipolar systems. To bridge this gap, the analysis of valve-side ac faults in bipolar MMC HVDC systems is conducted, and protection methods are investigated in this thesis. The results will be presented in Chapter 5 and Chapter 6

2.6. Summary

In this chapter, the state-of-the-art VSC based HVDC technologies have been reviewed. VSC HVDC systems exhibit advantages over LCC HVDC systems or HVAC systems for renewable energy integrations. Such technologies have been widely used all over the world since the implementation of the first VSC HVDC link in 1999. With more and more HVDC links being commissioned, MTDC grids are promising solutions for further improving the efficiency and reliability of power grids.

However, there are still challenges on the way to building further MTDC grids so as to satisfy the demands of renewable power generation. The control of dc power flows, isolation of dc faults, and protection of different types of ac faults remain key aspects that need to be studied. Both control methods and hardware devices are needed to ensure safe operations of MTDC grids.

To clearly illustrate the background and scope of the study in this thesis, the technologies on DCCBs, CFCs, dc transformers have been reviewed, and fault protection methods were summarised with research questions emphasised. The proposed schemes and methods to tackle these issues will be presented in the next chapters.

Chapter 3   DC Current Flow Controller

3.1.   Introduction

Voltage source converter (VSC) based HVDC technologies exhibit advantages over traditional line commutated converter (LCC) based technologies when employed for large-scale renewable energy integration. Plenty of VSC based point-to-point links have been built so far. The construction of multi-terminal dc (MTDC) grids has been widely discussed in the literature as a means to enhance the flexibility and stability of transmission systems and, thus, further promote the system's economic efficiency. However, there are still important obstacles preventing the wide-scale deployment of meshed MTDC grids. One of them is the effective regulation of current flows in a dc system, as this is dominated by the resistance of the transmission lines. Therefore, currents cannot be directly controlled by the converters installed in the nodes, which may result in overloadings of transmission lines. Theoretically, in an n-terminal system, it is possible to regulate current flow up to n cables [109]. However, when the number of cables is larger than n, the dc current flow cannot be fully controlled. Furthermore, in order to reduce the control complexity of the converters at the terminals, CFCs can be added to each meshed network. By such a configuration, the control of the converters can be focused on their output power and/or dc voltage. Therefore, current flow controllers are in great demand to regulate current flows in meshed MTDC grids with multi dc cables.

Resistors can be inserted into the dc cables to regulate the current flow. Although this method is simple, such methods will generate extra power losses. To solve this issue, power electronics-based CFCs has been investigated for MTDC grids [174]-[176]. Among them, the interline dc/dc converters are promising solutions as the interline schemes do not need large isolation transformers and, thus, are of low cost and small footprint [176]-[177]. Several topologies with control methods have been investigated in the literature [178]-[180]. Interline CFCs with unidirectional devices are presented in [181]. The advantages of these schemes are their simple structures with a reduced number of power electronic devices[182]. However, the deployments of unidirectional devices may bring complexity to the control schemes, and

overvoltage may occur during transient conditions. Dual-H bridge schemes, employing devices with free-wheel paths, can mitigate the above issue [177], [179]. Their operating characteristics have been presented with modulation investigated in [180], [183], [184]. In [183], the current direction of transmission lines needed to be precisely detected to generate PWM modulation signals, which may add difficulties of its control during transient and the flexibility of the dual-H bridge CFC has not been fully used. In [184], dual PWM signals are deployed to control both the current and voltage of the dual-H bridge CFC. However, this induces extra switching losses since two PWM signals are used during the operations of the dual-H bridge CFC. Small-signal models of the dual H-bridge CFCs have been derived [178]. However, the difference of the small-signal models under different operating models has not been studied. Therefore, further study needs to be conducted on the interline CFCs.

This chapter presents the small-signal models and control of half-bridge current flow controllers (HB-CFCs) in meshed MTDC networks. The dual-H bridge CFC is simplified to an HB-CFCs. To clearly illustrate the operating principle of the HB-CFCs, four operation modes are classified for the HB-CFCs based on different functions when regulating current flows. The current sharing and reversal modes will be analysed in detail. To simplify the control of the HB-CFC and fully utilize its flexibility, a level-shift modulation method is proposed. Meanwhile, to better operate and control the HB-CFC within MTDC networks, a small-signal analysis has been conducted, and the small-signal models of the HB-CFC are derived. Simulations are conducted in PSCAD/EMTDC and PSIM to verify the analysis.

3.2. Current flow controllers in MTDC grids

In a meshed MTDC grid, dc current flows are mostly dominated by the resistance of the transmission lines. Therefore, the currents of dc lines cannot be fully controlled by the converters installed in the nodes. As shown in Fig. 3-1, paralleled paths exist in meshed MTDC grids (e.g. L_{13}), which may lead to the existence of circulating currents (e.g. i_{cir}) within the meshed network. Therefore, CFCs are needed to balance current flow, thus, to avoid over-loading of transmission lines.

(a) Four-terminal system

(b) Three-terminal system
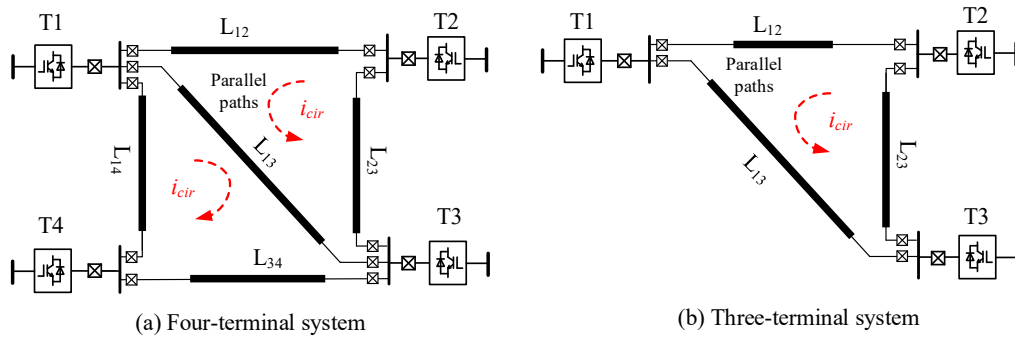
Fig. 3-1. Meshed MTDC grids with parallel paths.

To reduce the control complexity of the converters at the terminals of and fully control the dc current flows in meshed dc grid., normally, CFCs can be added to each meshed network. As shown in Fig. 3-2, to fully regulate the current flows among the transmission lines, two CFCs are normally required for the four-terminal system, and one CFC is required for the three-terminal system. The CFCs are installed at the nodes of the MTDC network and regulate currents among its connected transmission lines.

(a) Two CFCs installed

(b) One CFC installed
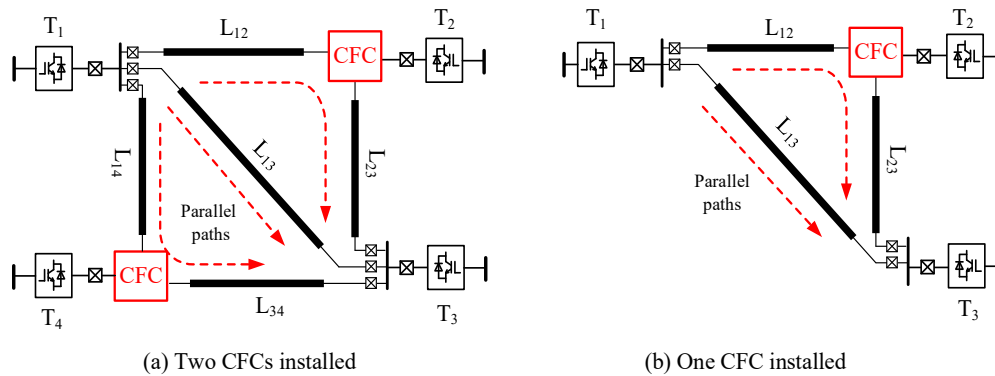
Fig. 3-2. Meshed MTDC grids with CFCs installed.

3.3. Half bridge-based CFC

As an interline configuration, dual H-bridge CFCs have been investigated in [152]. The dual H-bridge CFC consists of two H-bridges with two paralleled capacitors (i.e. common dc bus), as shown in Fig. 3-3. In this application, the dual H-bridge CFC controller is installed in one of the nodes (N_1) of the MTDC grid. Fig. 3-3(b) presents the schematic of the dual H-bridge CFC. One bridge from the H-bridge is connected with Node 1, while the other bridges are connected to the transmission lines to regulate their currents.

(a) System configuration

(b) Schematic Dual H-bridge CFC
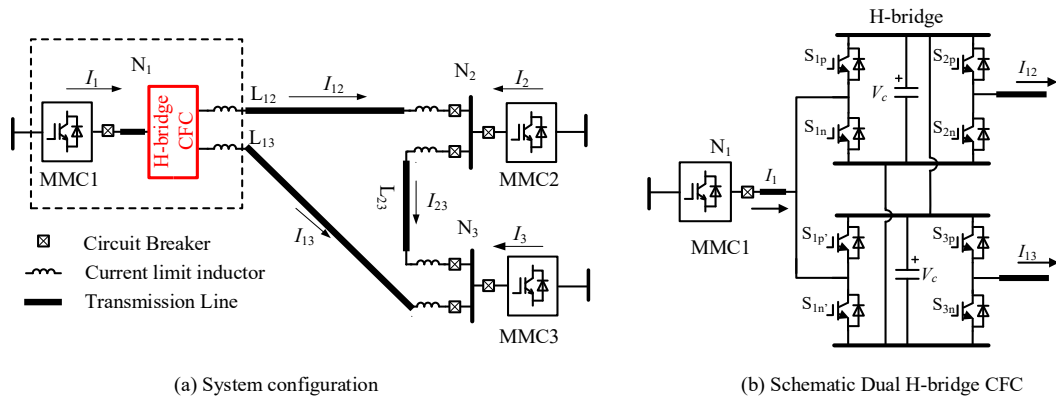
Fig. 3-3. MTDC grid with dual H-bridge CFC.

It can be seen from Fig. 3-3(b) that the switching pairs of the two H-bridges connected with N_1 are parallel with each other. Therefore, the topology of the dual H-bridge CFC can be simplified by merging its paralleled devices (see devices coloured as red in Fig. 3-4 (a)). This results in a simplified topology with three half-bridges, i.e., the half-bridge CFC (HB-CFC as shown in Fig. 3-4 (b)). By such a simplification, two IGBT devices and a capacitor can be saved.

(a) Dual H-bridge
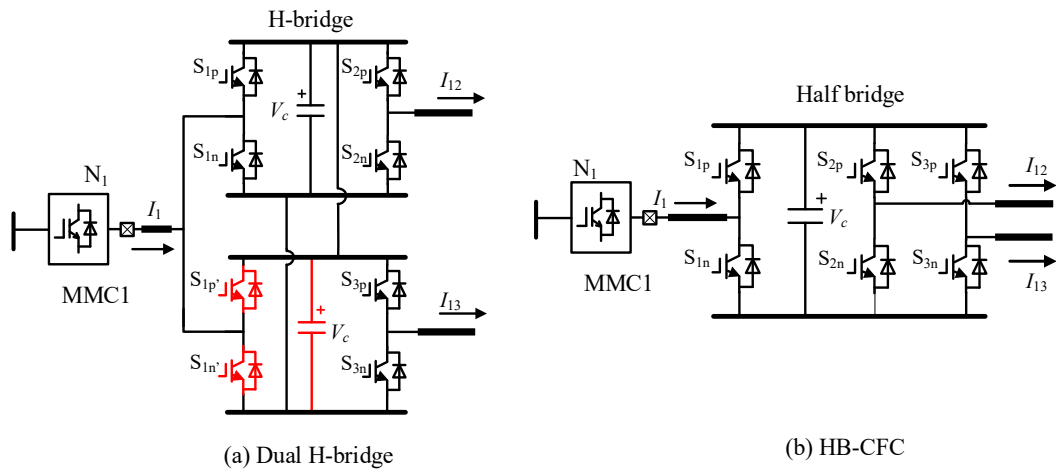
(b) HB-CFC

Fig. 3-4. Topology of HB-CFC.

3.4. Operation modes of the HB-CFC

Based on the relationship between the node current I_1 and the transmission line currents I_{12} and I_{13}, the HB-CFC has four operating modes. This subsection focuses on analysing different control modes of the HB-CFC. The control schematic of the HB-CFC together will be elaborated in Section 3.5.

3.4.1. Bypass mode

The HB-CFC operates in this mode when all switches $S_{ip,n}$ are kept in on-states. An equivalent circuit of the HB-CFC under the bypass mode is given in Fig. 3-5. It can be seen that the capacitor is bypassed under such mode. Since the voltage of the capacitor V_c is zero, no influence will be imposed on the dc network. Instead, the current flows within the network are determined by the resistance of transmission lines.

(a) All switches on-state   (b) Equivalent circuit
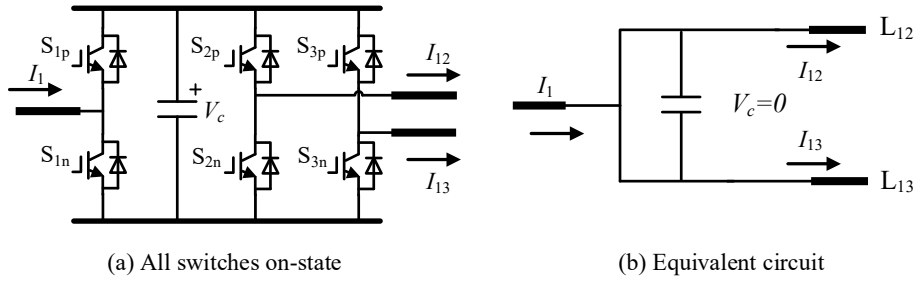
Fig. 3-5. HB-CFC operated under bypass mode.

As presented in (3-1), the node current I_1 equals the sum of the currents in its connected transmission lines.

$$I_1 = I_{12} + I_{13} \tag{3-1}$$

The HB-CFC is selected to operate in this mode when no demand for current regulation is needed. The bypass mode can reduce switching losses of power electronics devices.

3.4.2. Current nulling mode

The HB-CFC operates in this mode when the capacitor is fully inserted into one of the transmission lines. For example, as shown in Fig. 3-6(a), when S_{1p}, S_{2p} and S_{3n} are in an on-state, the capacitor is fully inserted into transmission line L_{13}. An equivalent circuit is given in Fig. 3-6(b).

Under such operation mode, the dc current will flow through L_{12} only, and the current of L_{13} is reduced to zero:

$$I_{12} = I_1, \; I_{13} = 0 \tag{3-2}$$

This will help to null the current of related transmission lines (whenever maintenance is needed) and, at the same time, keep other parts of the MTDC grid active.

(a) S_{1p}, S_{2p} and S_{3n} are in on-states

(b) Equivalent circuit
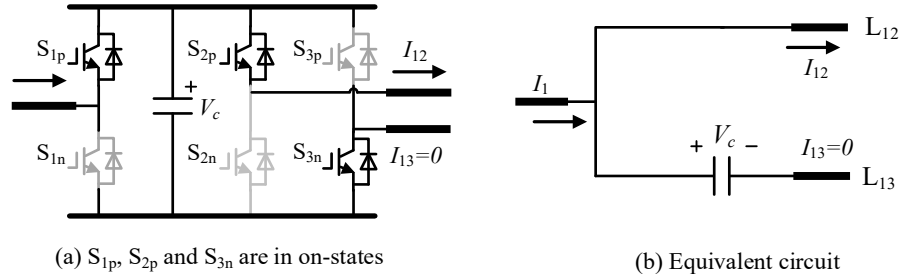
Fig. 3-6. HB-CFC operated under the current nulling mode.

3.4.3. Current sharing mode

The CB-CFC operates in this mode when the bridge (the bridge built up by S_{1p} and S_{1n} in Fig. 3-7) connected with the node (i.e. MMC1) is regulated by a PWM signal. As shown in Fig. 3-7(a), when S_{1p} is switched on, the capacitor is inserted into L_{13} with a positive voltage V_c, and it is charged by I_{13}. When S_{1n} is switched on, the capacitor is inserted into L_{12} with a negative voltage V_c, and it is discharged by I_{12} [see Fig. 3-7(b),]. By the modulation of the PWM signals, two equivalent controllable dc sources are inserted into the two transmission lines, as shown in Fig. 3-8.

(a) S_{1p} is *on*

(b) S_{1n} is *on*
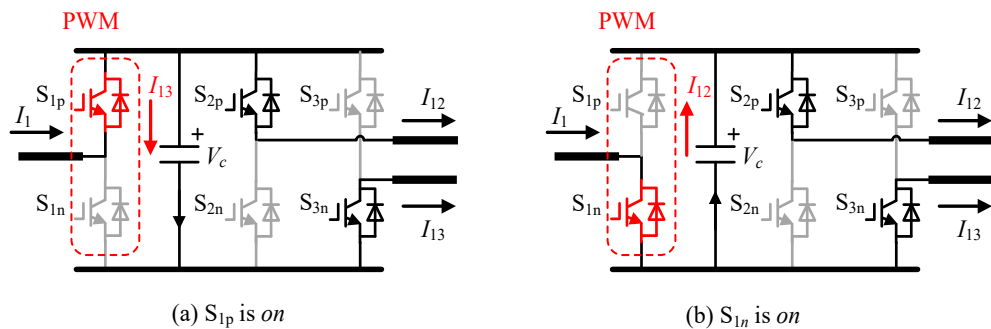
Fig. 3-7. HB-CFC operated under current sharing mode.
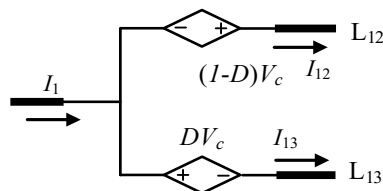
Fig. 3-8. Equivalent circuit of the HB-CFC under the current sharing mode.

When operated in a steady condition, the average current flowing through the capacitor within a period of the PWM should be zero, maintaining the energy balance of the capacitor (i.e., the average of charging and discharging current is equal):

$$I_{13}DT = I_{12}(1-D)T \tag{3-3}$$

where T is the period and D is the duty ratio of the PWM. Deriving (3-1) and (3-3)the line currents are;

$$I_{12} = I_1D, \quad I_{13} = I_1(1-D) \tag{3-4}$$

From (3-4), it can be seen that line currents I_{12} and I_{13} are regulated by the duty ratio D. As the value of D is between 0 and 1, I_{12} and I_{13} both have a magnitude lower than the magnitude of I_1. The current sharing mode can be used to distribute the node current between connected transmission lines, which can help to optimize the current flows with an MTDC grid.

3.4.4. Current reversal mode

The CB/CFC operates in this mode when one of the bridges connected with the transmission lines is regulated by a PWM signal. As shown in Fig. 3-9, the bridge connected with L_{12} is taken as an example to explain its operation process. When S_{2n} is switched on, the capacitor is inserted to the node with a positive voltage V_c and charged by node current I_1 (the current from MMC1 in Fig. 3-4(b)). When S_{2p} is switched on, the capacitor is inserted into L_{13} and discharged with current I_{13} (reversed direction).

(a) S_{2n} is *on*   (b) S_{2p} is *on*
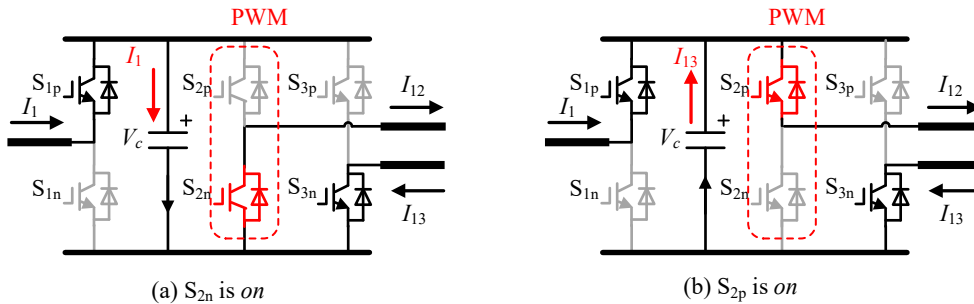
Fig. 3-9. HB-CFC operates under current reversal mode.
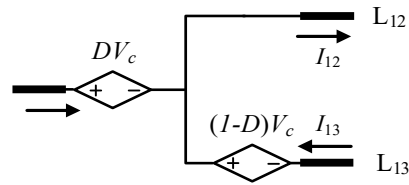
Fig. 3-10. Equivalent circuit of the HB-CFC under the current reversal mode.

An equivalent circuit is shown in Fig. 3-10. When operating in a steady condition, the average current flowing through the capacitor within a period of the PWM should be zero, maintaining the energy balance of the capacitor (i.e., the average of charging and discharging current is equal):

$$I_1(1-D)T = -I_{13}DT \tag{3-5}$$

Deriving (3-1) and (3-5), the line currents are:

$$I_{12} = I_1 / D, \; I_{13} = -I_1(1-D)/D \tag{3-6}$$

From (3-6), it can be seen that line currents I_{12} and I_{13} are regulated by the duty ratio D. Since the value of D is between 0 and 1, I_{12} has a greater magnitude than that of I_1. It should be noted that, under this mode, current I_{13} is reversed. Similarly, I_{12} will be reversed when a PWM signal is applied to the bridge connected with L_{13}. The current reversal mode can be used to reverse the current flow in one of the transmission lines, which, in turn, could prevent the overloading of other transmission lines within a meshed MTDC grid.

3.5. Small-signal modelling and frequency domain analysis

As analysed in Section 3.4, the HB-CFC is modulated by PWM signals to regulate the current flows. Due to its discrete switching processes, the HB-CFC exhibits a non-linear and time-varying characteristic. To better understand its dynamic behaviour and, thus, design a proper controller, the switching processes should be linearised to obtain a small-signal model of the HB-CFC. The small-signal modelling will be presented next.

3.5.1. Small-signal modelling

In this subsection, an averaging technique of the PWM switching process is used to linearise the HB-CFC and obtain its small-signal models in the frequency domain [187]. The state-space modelling method can also get the same result. Since the switching bridges are not the same under different operating modes thus, the small-signal model will be derived separately for the current sharing and reversal modes.

To investigate the small-signal model of the HB-CFC in an MTDC grid, an equivalent system-level diagram is illustrated in Fig. 3-11. Since the dynamics of current flow regulation are in the timescale of seconds, the transmission lines are modelled as equivalent inductors and resistors in series (capacitances of the transmission lines are eliminated since they dominate the characteristics in a higher frequency range). To focus more on the characteristics of HB-CFC, switching models are used for the HB-CFC, while the MMCs are represented by their average models.
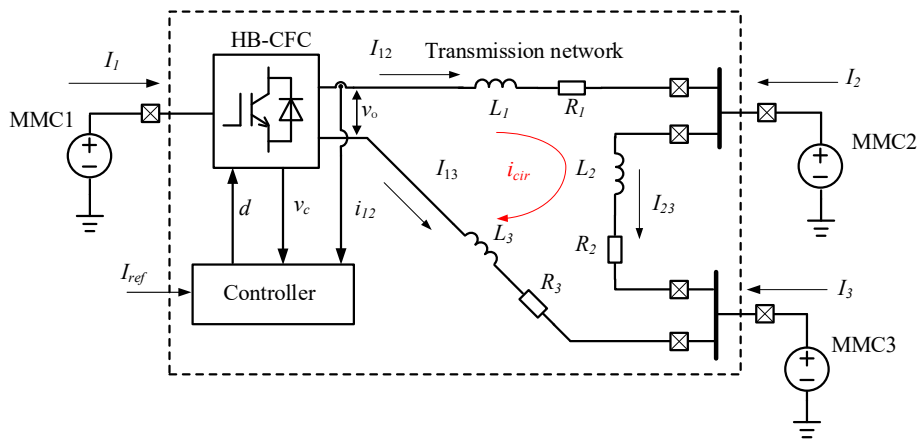
Fig. 3-11. Equivalent diagram of the HB-CFC in an MTDC grid.

a) Current sharing mode

Under this operating mode, the PWM signal is applied to the bridge which connected with the node. Since the structure of the circuit will be changed by the PWM signal, the differential equation for the capacitor voltage, when the output of the PWM signal is '1' and '0', are given (3-7) and (3-8), respectively:

$$C\frac{dv_c(t)}{dt} = i_1(t) - i_{12}(t) : \text{interval } d \tag{3-7}$$

$$C\frac{dv_c(t)}{dt} = -i_{12}(t) : \text{interval } 1\text{-}d \tag{3-8}$$

where C is the value of the capacitor in the HB-CFC, $v_c(t)$ the capacitor voltage in the HB-CFC, $i_1(t)$ the node current, $i_{12}(t)$ the current of L$_{12}$, and d the duty ratio of the PWM (d is the duty ratio for the leg connected with the converter at the terminal).

By calculating the average value of the capacitor voltage v_c in one PWM duty cycle (i.e. apply an average operator to (3-7) and (3-8)), an average switching model is obtained:

$$C\frac{d\langle v_c(t)\rangle_T}{dt} = (i_1(t) - i_{12}(t))d - i_{12}(t)(1-d) = i_1(t)d - i_{12}(t) \tag{3-9}$$

where $\langle \ \rangle_T$ is the average operator for one PWM duty cycle.

However, such a model is still nonlinear owing to the presence of the product of the two time-dependent quantities $i_1(t)$ and $d(t)$. To obtain the small-signal approximation, perturbations are added to (3-9).

$$v_c(t) = V_c + \hat{v}_c(t), i_1 = I_1 + \hat{i}_1(t), i_{12} = I_{12} + \hat{i}_{12}(t), d = D + \hat{d}(t) \tag{3-10}$$

where V_c, I_1, I_{12} and D are the dc component and $\hat{v}_c(t)$ $\hat{i}_1(t)$ $\hat{i}_{12}(t)$ $\hat{d}(t)$ are the ac perturbations.

Neglecting its second-order nonlinear and dc terms, a linearized model is obtained,

$$C\frac{d\hat{v}_c(t)}{dt} = D\hat{i}_1(t) + \hat{d}(t)I_1 - \hat{i}_{12}(t) \tag{3-11}$$

As shown in Fig. 3-8, under the current sharing mode, voltage $v_c(t)$ is directly applied to the network of the transmission lines (i.e. $v_o = v_c$ in Fig. 3-11). Therefore, when analysing the transmission networks, the following differential equation is obtained as (3-12) and linearized as (3-13),

$$L\frac{di_{12}(t)}{dt} + Ri_{12}(t) = v_c(t) \tag{3-12}$$

$$L\frac{d\hat{i}_{12}(t)}{dt}+R\hat{i}_{12}(t)=\hat{v}_c(t) \tag{3-13}$$

where L is the total inductance of the network (i.e. $L = L_1+L_2+L_3$), and R is the total resistance of the network (i.e. $R = R_1+R_2+R_3$) [see Fig. 3-11].

By applying Laplace transform to (3-11) and (3-13), we can get its duty ratio to output (i.e. the line current) transfer function as below,

$$G_{id}(s)=\frac{\hat{i}_{12}(s)}{\hat{d}(s)}=\frac{I_1}{LCs^2+RCs+1} \tag{3-14}$$

b) Current reversal mode

Under this operating mode, the PWM signal is applied to the bridge connected with the transmission lines. Similar to the current sharing mode, since the structure of the circuit will be changed by the PWM signal, the differential equation for the capacitor voltage when the output of the PWM signal is '1' and '0', are given (3-15) and (3-16), respectively:

$$C\frac{dv_c(t)}{dt}=i_1(t)-i_{12}(t):\ \text{interval } d \tag{3-15}$$

$$C\frac{dv_c(t)}{dt}=i_1(t):\ \text{interval } 1\text{-}d \tag{3-16}$$

By calculating the average value of the capacitor voltage in one PWM duty cycle (i.e. apply an average operator to (3-15) and (3-16), an average switching model is obtained:

$$C\frac{d\langle v_c\rangle_T}{dt}=(i_1(t)-i_{12}(t))d+i_1(t)(1-d)=i_1(t)-i_{12}(t)d \tag{3-17}$$

Similarly, to obtain the small-signal approximation under current reversal mode, perturbations: $v_c(t)=V_c+\hat{v}_c(t), i_1=I_1+\hat{i}_1(t), i_{12}=I_{12}+\hat{i}_{12}(t), d=D+\hat{d}(t)$ are added to (3-17). Neglecting its second-order nonlinear and dc terms, a linearized model is obtained,

$$C\frac{d\hat{v}_c(t)}{dt} = \hat{i}_1(t) - \hat{i}_{12}(t)D - \hat{d}(t)I_{12} \tag{3-18}$$

Different from the current sharing mode, the voltage applied to the network of the transmission lines $v_o(t)$ (v_o is the voltage generated by the CFC and seen by the transmission lines as shown in Fig. 3-11) is also different when the switching state changes within a PWM duty cycle under the current reversal mode (i.e. $v_{o(t)} = v_c$ when $d = 1$ while $v_o = 0$ when $d = 0$ as given in (3-19)). The following differential equation is obtained as (3-19) and linearized as (3-20),

$$L\frac{di_{12}(t)}{dt} + Ri_{12}(t) = v_o(t) \tag{3-19}$$

$$v_o(t) = V_c \hat{d}(t) + D\hat{v}_c(t) = L\frac{d\hat{i}_{12}(t)}{dt} + R\hat{i}_{12}(t) \tag{3-20}$$

By applying Laplace transform to (3-18) and (3-20), we can get its duty ratio to its output (i.e. line current) transfer function as below,

$$G_{id} = \frac{\hat{i}_{12}(s)}{\hat{d}(s)} = -\frac{DI_{12} - V_c Cs}{LCs^2 + RCs + D^2} \tag{3-21}$$

It can be seen from (3-14) and (3-21) that the transfer functions of the HB-CFC under the current sharing mode and reversal mode are different. A right half-plane (RHP) ZERO exists in the transfer function under the current reversal mode, as shown in (3-21). This indicates that the CFC behaves as a non-minimum phase system under this operating mode. The RHP ZERO brings an extra phase lag (90 degrees) in the frequency response of the system and worsens the dynamic response during the transient. Therefore, attention should be paid when designing the controller due to its implication on system stability.

3.5.2.   Frequency-domain analysis

To verify the validity and accuracy of the small-signal model derived in the previous sub-section, a method of frequency-domain analysis is carried out. The HB-CFC, together with an MTDC grid, as shown in Fig. 3-11, is built in PSIM in this study to do the ac sweep analysis. A perturbation $\hat{d}$ (small-signal ac component) is

injected into the PWM duty ratio D (steady-state dc component), and the variation in its output (i.e. the current $\hat{i}_{12}$) is fed back to the ac sweep block as shown in Fig. 3-12. By comparing the magnitude and phase difference between $\hat{a}$ and $\hat{i}_{12}$ in the frequency domain, the frequency responses of the HB-CFC are obtained, i.e.

$$G_{id}(s) = \frac{\hat{i}_{12}(s)}{\hat{d}(s)}$$

where $G_{id}(s)$ is the transfer function between from duty ratio to the output current.
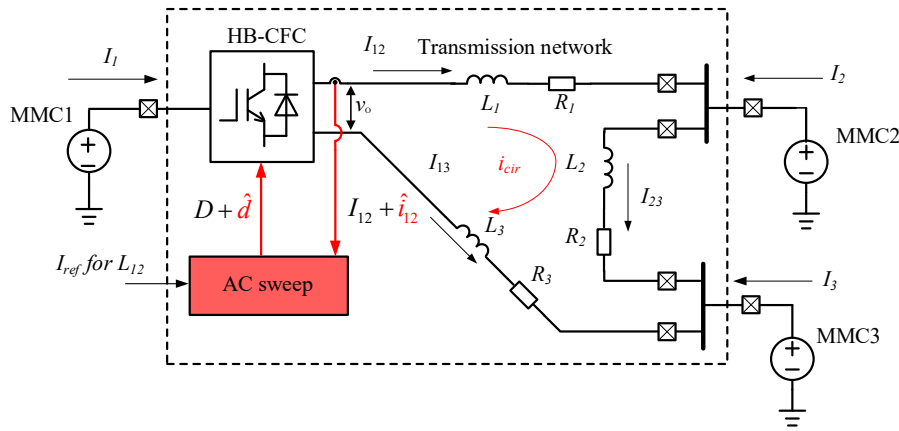
Fig. 3-12. Frequency-domain analysis (ac sweep) of the HB-CFC.

3.5.3. Cascaded controller design

As analysed in Section 3.5.1, under the current reversal mode, the transfer function of the HB-CFC from duty ratio to the output current contains an RHP ZERO. This difference may add difficulty when designing a unified controller for both the current sharing and reversal modes.

To relieve the difficulty in designing a unified controller and reduce the influence of the RHP ZERO, a dual-loop control is investigated. The controller consists of an inner voltage control loop, which supervises its capacitor voltage and an outer control loop. As shown in Fig. 3-13, the current of one transmission line (e.g. i_{12}) is fed back to the outer control loop, and it generates a voltage reference for the inner control loop. Control block diagrams are given in Fig. 3-14. As analysed in Section 3.5.1, when only the single-loop control is used, the transfer function $G_{id}(s)$ contains a RHP ZERO for the current reversal mode.

When the dual-loop control is adopted, as shown in Fig. 3-14(b), the transfer functions for both the inner control loop and outer loop are considered. The transfer function, based on the dual-loop control as shown in Fig. 3-13, will be derived below.
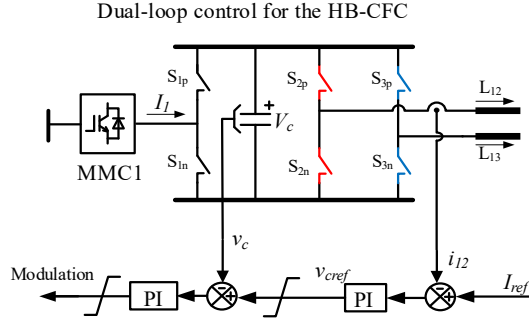
Fig. 3-13. Dual-loop control.

(a) Single loop control

(b) Dual-loop control
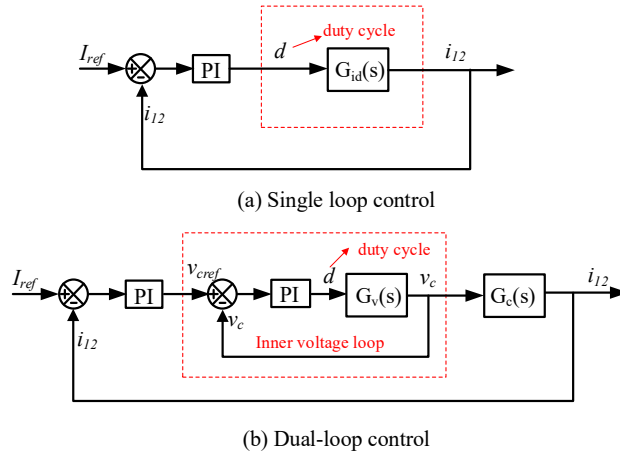
Fig. 3-14. Control block diagram.

Under the current sharing mode, the transfer function $G_v^s(s)$ from the duty ratio $\hat{d}$ to the capacitor voltage $\hat{v}_c$, and the transfer function $G_c^s(s)$ from $\hat{v}_c$ to output current $\hat{i}_{12}$, are derived as:

$$G_v^s(s) = \frac{v_c(s)}{d(s)} = \frac{I_1(Ls+R)}{LCs^2 + RCs + 1} \tag{3-22}$$

$$G_c^s(s) = \frac{i_{12}(s)}{v_c(s)} = \frac{1}{Ls+R} \tag{3-23}$$

Under the current reversal mode, the transfer function $G_v^r(s)$ from the duty ratio $\hat{d}$ to the capacitor voltage $\hat{v}_c$ and the transfer function $G_c^r(s)$ from $\hat{v}_c$ to output current $\hat{i}_{12}$ is derived as:

$$G_v^r(s) = \frac{v_c(s)}{d(s)} = \frac{(Ls+R)I_{12} + (1-D)V_c}{LCs^2 + RCs + (1-D)^2} \tag{3-24}$$

$$G_c^r(s) = \frac{i_{12}(s)}{v_c(s)} \approx \frac{D}{Ls+R} \tag{3-25}$$

By comparing (3-22), (3-23) with (3-24), (3-25), it can be seen that the transfer functions of the HB-CFC have similar structures when inner current loops are included (i.e. the transfer functions for the inner control loops $G_v^s(s)$ and $G_v^r(s)$ are both second-order systems without RHP ZERO and the transfer functions for the outer control loop $G_c^s(s)$ and $G_c^r(s)$ are both first-order system). The influence of the RHP ZERO is neglected by the dual-loop control. In the meantime, the dual-loop control can also supervise its capacitor voltage, which can avoid overvoltage cases during transient conditions. Thus, it is more reliable compared to the single-loop control.

It should be noted that although the phase delay caused by the RHP ZERO is eliminated by the dual-loop control scheme, the delays caused by samplings (e.g ZOH induced by digital samplings and controls) and PMW modulations still exists in both the single and dual loop control schemes. The control block diagrams considering the delays caused by samplings and PWM modulations are given in Fig. 3-15.

A ZOH is normally used to approximatively model the process of the PWM modulation [188]. Its transfer function is,

$$G_{ZOH}(s) = \frac{1-e^{-sT_s}}{s} \approx T_s e^{-0.5sT_s} \tag{3-26}$$

where T_s is the modulation period.

The PWM modulation process induces around 0.5 Ts time delay to the control system, which needs to be considered when designing controllers. Furthermore, when digital sampling is used (for HVDC applications, digital controllers are mostly

deployed), the digital samplings and control process normally causes another T_s time delay (i.e. e^{-sT_s}) [188]. Such delays (total around 1.5 T_s) may cause instability issues to the control systems. Therefore, extra phase margins need to be further considered when designing related controllers to compensate for the phase delays caused by the digital samplings and PWM modulations.

(a) Single loop control

(b) Dual-loop control
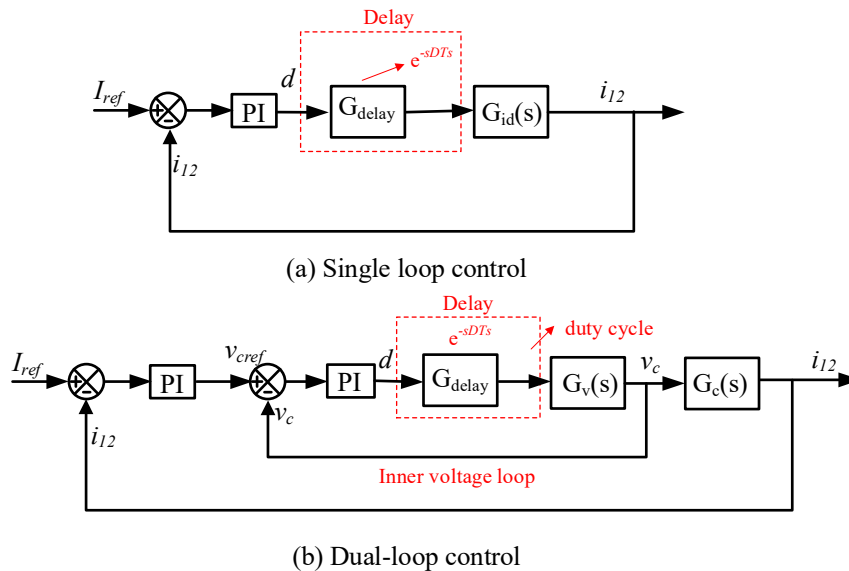
Fig. 3-15. Control block diagrams when delays are considered.

3.6. Level shift modulation

As analysed in Section 3.4, the current sharing and reversal modes are achieved by deploying specific PMW modulation signals on different bridges of the HB-CFC. Based on this observation, such characteristics can be used to design its modulation and control methods. To simplify its control process, a level shift modulation has been investigated and will be discussed in detail in this section.

In this section, the topologies with reverse blocking (RB) devices (without free-wheeling diodes) are introduced first, as it is simple to explain the principle of the HB-CFC and negative dc voltage can be obtained using such devices directly. However, since the RB devices are normally of high costs and power losses, topologies using devices with free-wheeling diodes are more recommended for real applications. Both of the topologies with level-shift modulation methods will be introduced next.

3.6.1. Switches without free-wheeling diodes

Switches without free-wheeling diodes (paths) are used in the HB-CFC first to elaborate on the principle of the level shift modulation. Such power electronics device application (without free-wheeling diodes) includes IGCTs or reverse blocking IGBTs (RB-IGBTs), etc. It should note that such RB devices, e.g. IGBTs with series diodes or RB-IGBTs, will induce more cost and power losses. Therefore, the topologies with RB devices, elaborated in this subsection, is mainly used for explaining the principle of this device.

As shown in Fig. 3-16(a), three level-shifted carriers are used to generate PWM signals, which are, respectively, used to control one specific converter leg of the HB-CFC. The level-shifted modulation can ensure that only one bridge is regulated by PWM signals at a time. Through the dual-loop control, as shown in Fig. 3-16(b), the HB-CFC will either operate in the current sharing mode or current reversal mode. It should be noted that when the modulation signal is fixed to a value of 0 or 1. The HB-CFC will operate in the current nulling mode. The node current will be fully (100%) distributed to one of the transmission lines while the other line is zero.
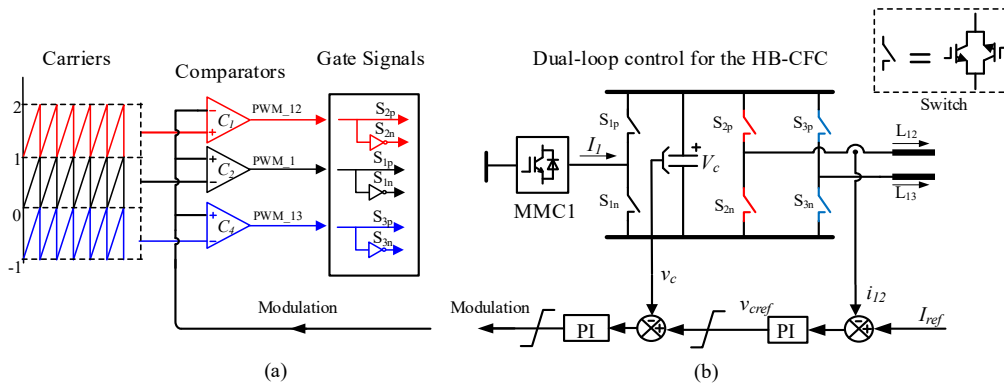
Fig. 3-16. Modulation strategy using switches without free-wheeling diodes.

The above configuration of the HB-CFC clearly shows the principle of the level shift modulation method. Since, the switches in this topology do not contain free-wheeling diodes, as a result, the capacitor voltage V_c can be regulated to a negative value to maintain the capability of the current flow control. This simplifies the control process of the HB-CFC. However, as a power electronic converter, the HB-CFC, when configured in such a manner, may add difficulties for the current commutation for

practical applications. Switching devices with free-wheeling diodes are more recommended to be used for real applications. This will be analysed next.

3.6.2. Switches with free-wheeling diodes

To tackle the issues (difficulties for the current commutation) discussed in the previous sub-section, switches with free-wheeling diodes are deployed for the HB-CFC, as shown in Fig. 3-17(b). Such a configuration is more practical in real applications. However, due to the anti-parallel free-wheeling diodes within the switches (e.g. IGBTs), the voltage of the capacitor V_c cannot be regulated to a negative value. A negative value is indeed needed when the current of L_{12} should be reduced. To overcome this shortcoming, a modified level shift modulation method is investigated. When a negative voltage is needed (i.e. when v_{cref} is negative in Fig. 3-17(b)), the on/off logic of the switches is reversed. This can be achieved by adding a sign detection module in the controller (software-based, and no extra hardware is needed). Furthermore, to achieve this, a new carrier is added in Fig. 3-17(a). This is different from Fig. 3-16(a).

When the on/off logic of the switches is reversed, the positions of L_{12} and L_{13} are exchanged with each other. This produces an equivalent negative voltage to L_{12}. Thus, reduction of I_{12} is achievable. An equivalent circuit is given in Fig. 3-18 to show the exchanging of the positions of L_{12} and L_{13}. This transition process can be implemented by modifying the PWM signals based on the sign of v_{cref}, as illustrated in Fig. 3-17 (a).
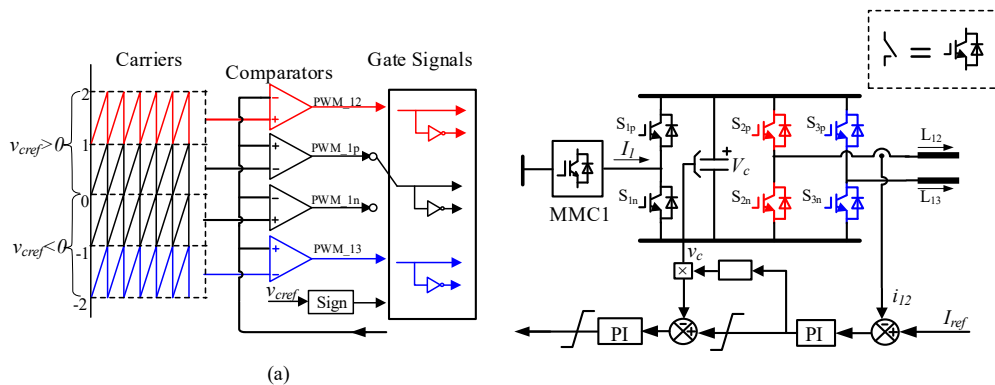
Fig. 3-17. Modulation strategy using switches with free-wheeling diodes.

(a) $v_{cref} > 0$ (b) $v_{cref} < 0$
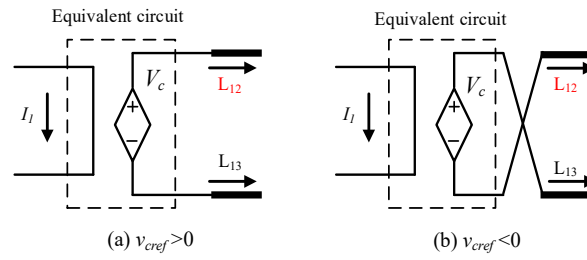
Fig. 3-18. Equivalent circuit of the HB-CFC.

Through the analysis in this subsection, it can be seen that the negative voltage can still be maintained by exchanging the position of transmission lines. Therefore, the topology using devices with free-wheeling diodes are recommended to be used in practical applications.

3.7. Simulation results

3.7.1. Time-domain simulation results

A three-terminal MTDC grid model with an HB-CFC installed at Node 1, as shown in Fig. 3-11, has been built in PSCAD to verify the analysis in this section. The VSCs are built with their average models to simplify the system. To focus more on the characteristics of the HB-CFC, it is modelled with a detailed switching model. The transmission lines are modelled as inductors and resistors. The parameters of the system are given in Table 3-1.

Table 3-1. System parameters of the MTDC grid with the HB-CFC.

Parameter	Value
Rated dc voltage	500 kV
Rated power of VSC1, VSC2, VSC3	500, 150, 700 kVA
Inductor/ Resistor of Line 12	180 mH / 2 Ω
Inductor/ Resistor of Line 13	150 mH / 1 Ω
Inductor/ Resistor of Line 23	100 mH / 0.2 Ω
Capacitor of the CFC	20 mF
Rated voltage of CFC	8 kV
Switching frequency	1 kHz
Sampling frequency	20 kHz

Notes: The total resistance of the three lines are 3.2 Ω (see Table 3-1) and the maximum current is 1.5 kA. The maximum dc voltage is 3.2 Ω ×1.5 kA = 4.8 kV. Therefore, the rated voltage of the CFC is selected as 8 kV in this study with margins.

The dual-loop control with the level shift modulation is adopted. The control diagram is given in Fig. 3-19. The duty ratio *d* is generated by the control loop and compared with the level-sifted carriers. Three gate signals (PWM12, PWM1 and PWM13 as shown in Fig. 3-19) will be generated. Since the carriers have been level-shifted, only one of the three gate signals will be a PWM signal (i.e. the duty ratio d will only be compared with one carrier) and the other two will be either constant 1 or 0.
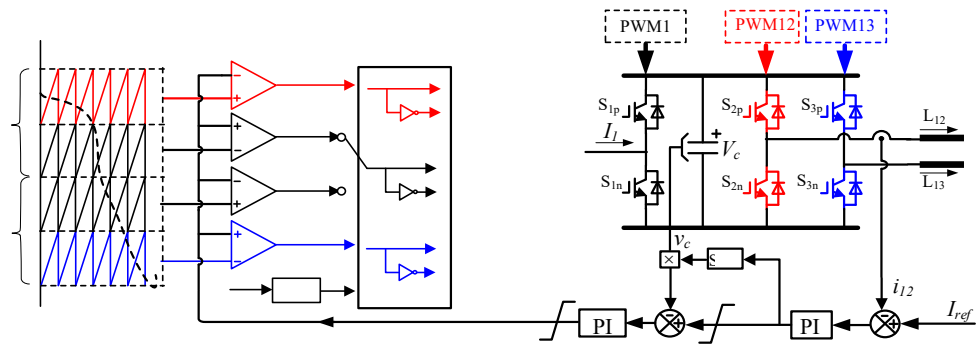
Fig. 3-19. Control diagram with level shift modulations.

The simulation results are given in Fig. 3-20. The HB-CFC begins to operate at *t* = 2 s. The red dashed line is the reference of I_{12}. From the simulation results, it can be observed that I_{12} can follow its reference well. Between 2-6 s and 9-12 s, the HB-CFC operates under the current sharing mode. The current of L_{12} and L_{13} are both smaller than the node current I_1 (I_1 is 1 kA as shown in the black dashed line). While between 6-9 s and 12-15 s, the HB-CFC operates under the current reversal mode. Either the magnitude of I_{12} or I_{13} can be larger than the node current, and the other one will be reversed. This has verified the analysis in Section 3.4. Fig. 3-20(b) shows the PWM signals during the transition of the HB-CFC's operations between different modes. It can be seen that only one bridge is modulated by PWM signals at a time, and there are no interactions between bridges. This verifies the effectiveness of the proposed dual-loop control and level shift modulation method in the previous sections.
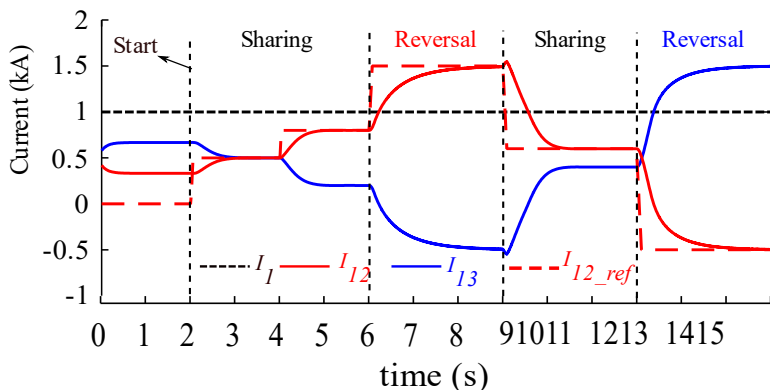
(a) Current of transmission lines
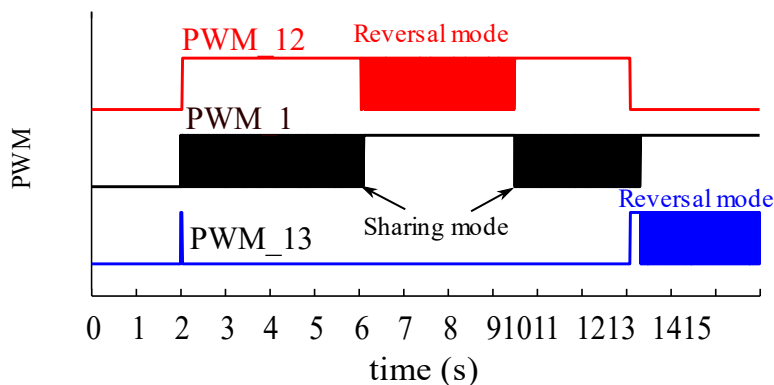
(b) PWM signals

Fig. 3-20. Simulation results of the current flow control in the MTDC grid.

3.7.2. Frequency-domain simulation results

As described in Section 3.5.2, frequency analysis has been carried out in PSIM software to verify the derived small-signal models of the HB-CFC. By comparing the injected variations $\hat{d}$ with its output $\hat{i}_{12}$, the frequency responses of the HB-CFC are obtained. Note that, in this study, the magnitude of the ac component $\hat{d}$ is selected to be 0.05 of its dc component D. As the switching frequency of the HB-CFC is 1 kHz, the frequency range of the ac sweep is set from 0.1 Hz to 500 Hz.

The simulation results are illustrated in Fig. 3-21. The blue carves are plotted according to (3-14) and (3-21) while the red curves are plotted based on the data through the ac sweep conducted in PSIM. It is observed that under the current reversal mode, an extra 90-degree phase delay (270 degrees in total) is included compared to the current sharing mode. This verifies the analysis in Section 3.5.1.
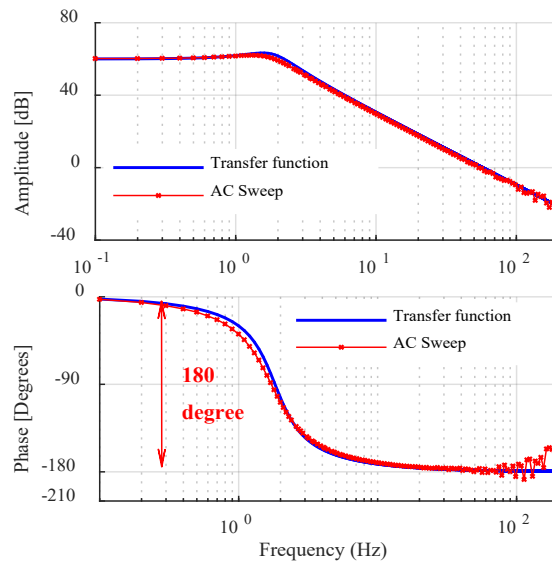
(a) Current sharing mode
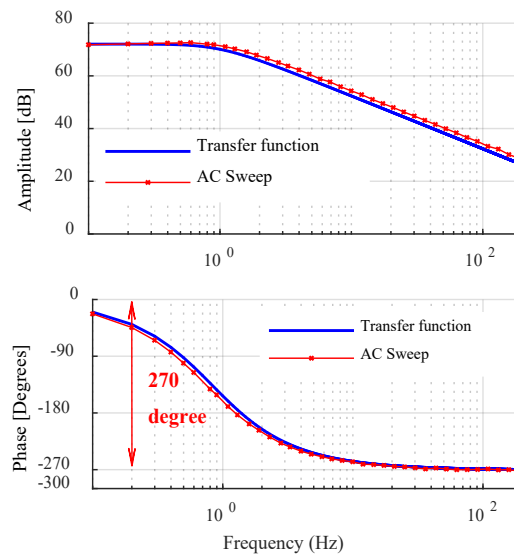
(b) Current reversal mode

Fig. 3-21. Frequency responses of the HB-CFC.

3.8.   Summary

In the chapter, the demands for installing CFCs in an MTDC grid are presented first. The topology of HB-CFC is investigated. Four operating modes have been clarified for the HB-CFC. Based on the clarified operating modes, a level shift modulation method has been proposed. By the proposed modulation method, only one bridge of the HB-CFC is regulated by PWM signals at a time. A significant benefit

obtained from it is the possibility of current regulation irrespective of the direction of the current at interfacing transmission lines. This simplifies the overall control strategy of the device and reduces its switching losses.

To provide guidance to the controller design of the HB-CFC. Small-signal modelling has been conducted. It was found that different from the current sharing mode, the transfer function of the current reversal mode contains an RHP ZERO, which will include an extra 90-degree phase delay in the frequency response of the system. This has been verified by the simulation results. The RHP ZERO may cause instability of the system when the controllers are not well designed. A dual-loop control together with the level shift modulation has been investigated to eliminate the influence of RHP ZERO. The analysis of the HB-CFC and the effectiveness of proposed control methods have been verified by time-domain and frequency-domain simulations.

Chapter 4   DC Protection Device with Current Flow Control Capability

4.1.   Introduction

Meshed HVDC grids are promising solutions for bulk power transmissions due to their enhanced flexibility and reliability. With the development of point-to-point HVDC links and the increase of renewable energy generations, there is a potential to connect existing HVDC links to form MTDC grids in the future. However, the installation of dc circuit breakers (DCCBs) and current flow controllers (CFCs) will be required to isolate dc faults and fully control the dc current flows within MTDC grids.

The propagation of dc faults is fast since the impedance of a dc network is low. To isolate a dc fault in a short time and maintain the safety of MTDC grids, power electronics-based DCCBs and CFCs are needed. However, such devices will significantly increase the capital costs of the system, especially in a multi-line system.

To reduce the costs of these devices, integrated schemes are proposed [189]. As MB branches of an HCB, as shown in Fig. 2-16, consist of a large number of semiconductor devices, their costs are relatively high. Therefore, the use of HCBs sharing MBs branches has been proposed for multi-line connections [189]-[191]. To further reduce the costs, diode and thyristor-based schemes have been examined as their costs are lower compared to those of IGBT based schemes [192], [193]. However, only few references have assessed the integration of current flow control into HCBs, which would further reduce capital costs. In [194], the low-loss branches of HCBs are integrated to operate as a CFC. Both current regulation and dc fault isolation are implemented, and the semiconductor switch count is reduced by eliminating the need for a separate CFC. However, the number of the MB branches, which contribute to most of the costs, are not reduced. To further reduce the number of semiconductors, [195] proposed a scheme to share the MBs. In this way, a large number of components can be avoided. Although [194] and [195] represent noteworthy attempts to integrate CFC and HCB capabilities, their costs are still relatively high, and the control and

modulation methods for CFC operation have not yet been analysed in detail. Further studies are still needed.

In this chapter, a new integrated device, i.e. the CB/CFC, is investigated. The device combines the function of a DCCB and HB-CFC into one topology. The modulation and control methods investigated in Chapter 3 are extended to this device, which can simplify its control process. The topology of the proposed device is introduced first in Section 4.2. The operating principles of the device operated as a CFC and DCCB are illustrated in Section 4.3 and Section 4.4, respectively. The comparisons of the CB/CFC with other existing schemes are given in Section 4.5. It can be revealed that the proposed device can further reduce the number of power electronics devices. The function of the CB/CFC is verified by simulations conducted in PSCAD/EMTDC. The results are given in Section 4.6. Section 4.7 summarises this chapter.

4.2. Configuration of the CB/CFC

4.2.1. Topology of the CB/CFC

The CB/CFC integrates a multi-line HCB and an HB-CFC into one device to reduce the number of power electronic devices while maintaining the same functions, i.e. isolating dc faults and regulating dc current flows. The configuration of the CB/CFC is illustrated in Fig. 4-1, which consists of three main parts, i.e. the main breaker branch, the capacitor branch and the low-loss branches.
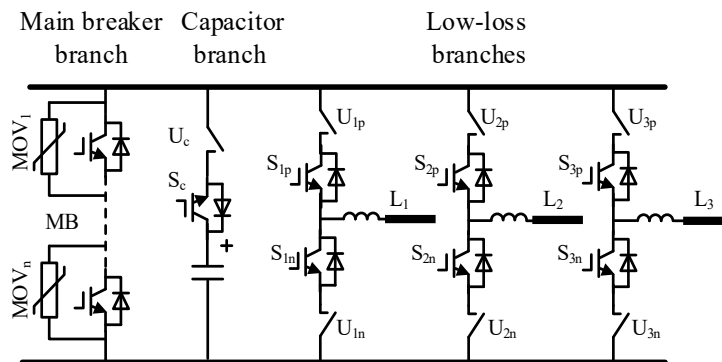
Fig. 4-1. Configuration of the CB/CFC.

The main breaker branch is used to interrupt dc fault currents when the device operates as a DCCB. Since this branch will have to withstand the high dc voltage

(around 1.5 times of dc-link voltage), hundreds of IGBTs are required for HVDC applications. Therefore, it takes up most of the capital costs. The capacitor branch contains a capacitor, which provides a constant dc bus when it operates as an HB-CFC. The loss branches carry dc current during normal operations. Since the number of power electronic devices is small (several IGBTs) compared to the main breaker branch, their power losses are much lower. Therefore, the load currents flow through the low-loss branches under normal conditions (without faults).

It can be seen in Fig. 4-1 that mechanical switches ($U_{ip,n}$) have been embedded into the low-loss branches. These switches are used to physically isolate faulted lines following a dc fault. Since the required time for dc fault isolation is around several milli-seconds, the operation time of the mechanical switches in this topology should be on the scale of milliseconds. It should be noted that the stray inductance in HV systems may be higher than MV and LV systems due to the high inclusion distance of HV devices (the value of insulation distance of such devices is high). Therefore, the high-frequency switching devices (IGBTs) may experience a hard-commutation process. Therefore, symmetrical mechanical layouts (to reduce the stray inductances) for the topology and a softer switching action (to reduce the di/dt) are recommended for the CB/CFC so as to reduce the voltage stresses and switching losses. Furthermore, RCD snubber circuits or arrestors can be used to clamp the voltage across the switches.

4.2.2.   System-level configuration

The CB/CFC is normally recommended to install at the dc terminals. Fig. 4-2 shows a schematic of the CB/CFC installed in the node of an MTDC grid. As shown in Fig. 4-2(a), at the terminal, two HCBs and one CFC is needed when separate devices are used. However, when the proposed CB/CFC scheme is adopted, two HCBs and one CFC are integrated into one device, as shown in Fig. 4-2(b).

(a) Separate CFC and HCBs   (b) CB/CFC
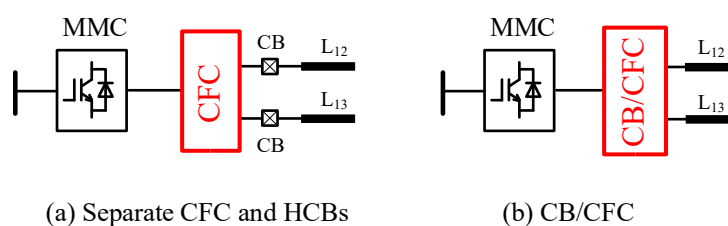
Fig. 4-2. CB/CFC installed in the node of an MTDC grid.

The system configuration of the CB/CFC in a three-terminal MTDC grid is shown in Fig. 4-3. A bipolar system is used (only the positive pole is shown in Fig. 4-3(a)). MMCs are used at each terminal to form the MTDC grid. As illustrated in Fig. 4-3(b), MMC1, $L_{12,}$ and L_{13} are connected to the middle points of low-loss branches of the CB/CFC. The operating principles of the CB/CFC will be presented next.

(a) MTDC grid with the CB/CFC

(b) Schematic of the CB/CFC
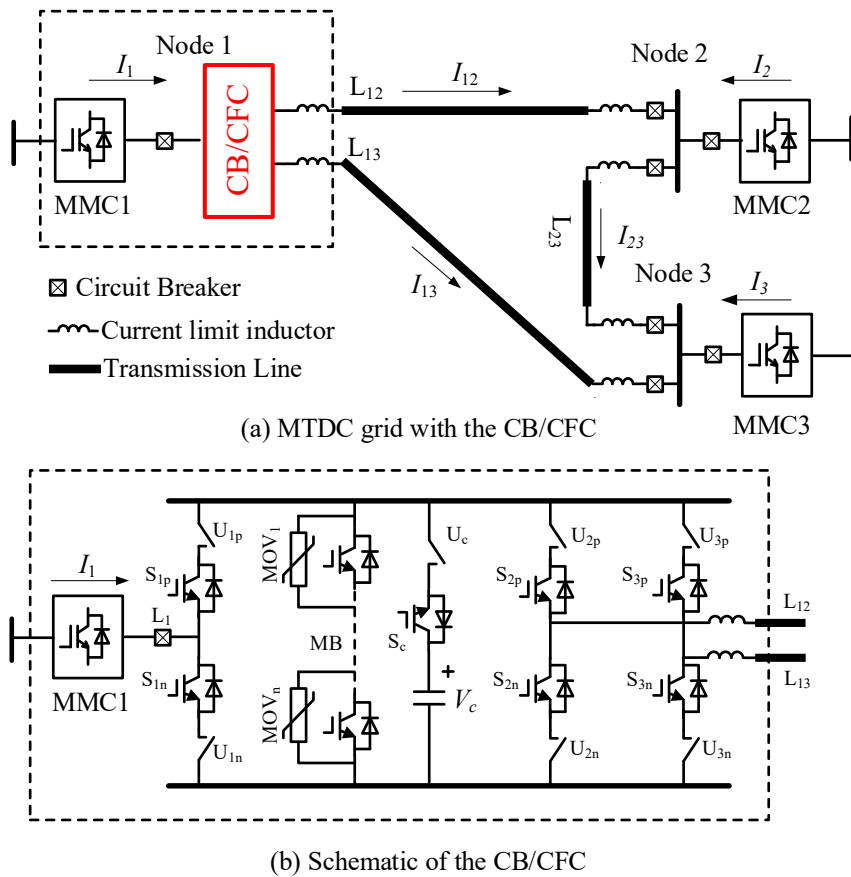
Fig. 4-3. System configuration with the CB/CFC in one node.

4.3. Operating as an HB-CFC

During normal conditions, the CB/CFC operates as an HB-CFC, regulating the currents between L_{12} and $L_{13.}$ Under such a case, the mechanical switches ($U_{ip,n}$) and U_c within the CB/CFC are all switched on, and the IGBTs in the MB are kept off-state. By such a configuration, the CB/CFC will operate as an HB-CFC, as shown in Fig. 4-4. The modulation and control methods of the CB/CFC, when operated as an HB-CFC, have been presented in Chapter 3.6.
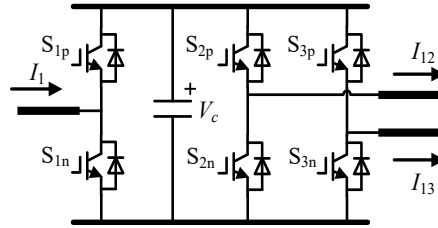
Fig. 4-4. Simplified topology of the CB-CFC when operated as a CFC.

4.4. Operating as an HCB

The CB/CFC operates as an HCB under dc fault conditions. The operation sequence of the CB/CFC when isolating a dc fault (a fault occurring at the transmission line of L_{13} is selected as an example) will be given below. A flow chart of the operation sequence is given in Fig. 4-5, and the detailed operation process is given in Fig. 4-6. To better show the operation process, typical waveforms of current and voltage for the fault isolation process is given in Fig. 4-7.
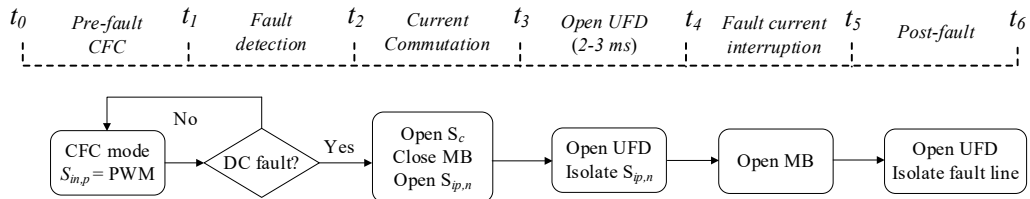
Fig. 4-5. Operation sequence of the CB/CFC.
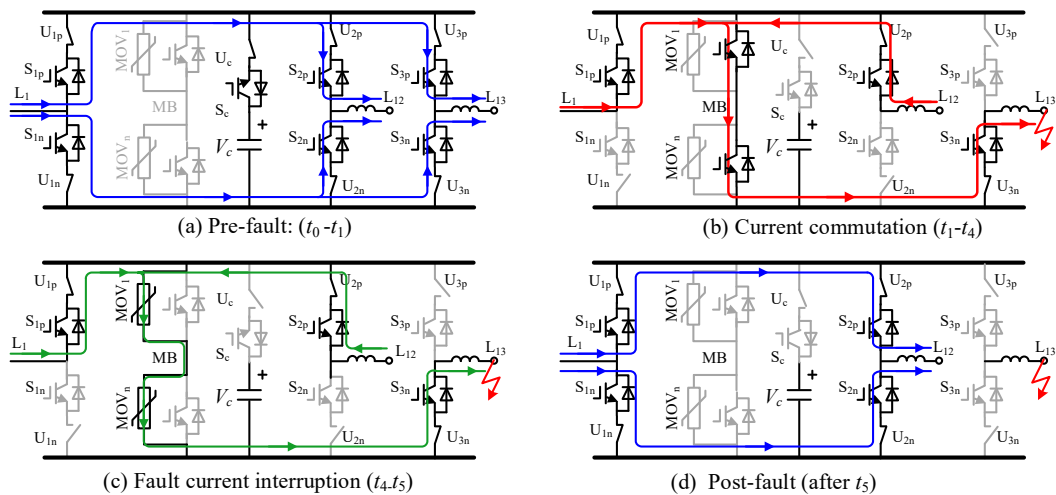
Fig. 4-6. Fault isolation process.

a) Pre-fault (t_0-t_1)

Before a dc fault occurs, the CB/CFC operates an HB-CFC. Under this condition, all the mechanical switches are in on-states, and the MB are in an off-state. The bridges

are regulated by their PWM signals to do the current flow control. The node current I_1 can flow through both the positive and negative buses of the CB-CFC, as shown in Fig. 4-6(a).

b) Current commutation (t_1-t_4)

A dc fault occurs at $t = t_1$. The current in the faulted line L_{13} increase quickly, and when the current i_{13} reaches its protection threshold (overcurrent protection is assumed to be used here to analyse the operation of the CB-CFC),

$$i_{13}(t_2) = I_{13} + \frac{V_{dc}}{L_e + L_{CLR}} \times (t_2 - t_1) \tag{4-1}$$

where I_{13} is the initial current before the fault, V_{dc} is the rated dc voltage of the MTDC grid, L_e and L_{CLR} are the equivalent inductances of the MMC and the current limiting reactor installed at the terminal.

When the fault is detected, S_c is first switched off to prevent discharging of the capacitor in the CB/CFC. After that, the MB will be switched on to prepare the current commutation process. $S_{ip,n}$ will be used to re-direct the currents within the CB/CFC. For the fault occurring at L_{13} in this study, S_{3p} is switched off to direct the current of the faulted line to flow through the negative bus only. S_{1n} and S_{2n} are switched off to direct the current in the healthy lines to flow through the positive bus only. This process can be seen in Fig. 4-6(b). After a period of time (normally in hundreds of micro-seconds), the fault current will be fully transferred into the MB, and its magnitude is approximated as:

$$i_{13}(t_3) = I_{13} + \frac{V_{dc}}{L_e + L_{CLR}} \times (t_3 - t_1) \tag{4-2}$$

When the commutation process is completed, the mechanical switches U_{1n}, U_{2n}, U_{3p} and U_c are ready to be switched off (since their current is zero) so as to isolate the IGBTs from the faulted line. This process takes several milliseconds typically, and the mechanical switches are fully opened at $t = t_4$, and the maximum current is expressed,

$$i_{13}(t_4) = I_{13} + \frac{V_{dc}}{L_e + L_{CLR}} \times (t_4 - t_1) \tag{4-3}$$

c) Fault current interruption (t_4-t_5)

When the mechanical switches are fully open at $t = t_4$, the MB is switched off to interrupt the fault current. As shown in Fig. 4-6(c), the fault current will be transferred into the MOVs and the energy stored in the inductors and transmission lines will be absorbed by the MOVs from t_4-t_5.

$$E_{MOV} = V_{MOV} \times I_{peak} \times \frac{(t_5 - t_4)}{2} \tag{4-4}$$

where V_{MOV} is the residual voltage of the MOVs and I_{peak} is the maximum cut-off current of the CB/CFC. The peak current, the residual voltage of the MOVs are the main parameters when designing the CB/CFC, which will determine the level of the energy absorption. Their values should be carefully examined. Normally, the residual voltage of the MOVs is 1.5 to 2 p.u. of the rated dc voltage. Therefore, the fault current will be reduced to zero within several milliseconds.

d) Fault isolation and post fault (after t_6)

When the fault current is reduced to zero at $t = t_5$, the faulted line can be permanently isolated by open U$_{3n}$, as shown in Fig. 4-6(d). After this, the healthy part of the system can be restored to its normal condition, and the CB/CFC can protect other connected dc lines. Typical waveforms of a fault interruption process are given in Fig. 4-7.
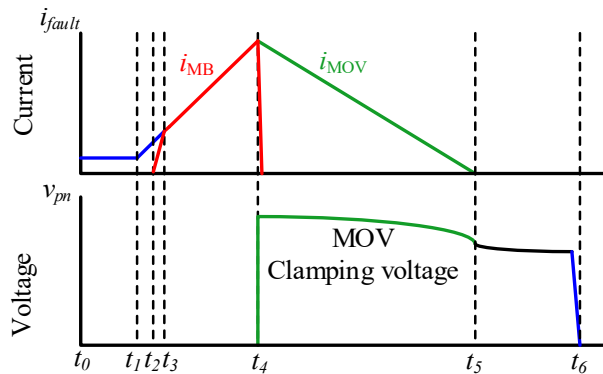
Fig. 4-7. Current and voltage waveforms of a typical fault interruption process.

4.5. Comparison and analysis

4.5.1. Components and costs evaluation

The advantages of the integrated CB/CFC are the reduction of the numbers of power electronic devices while maintaining the same functions when operated as an HCB and a CFC. A comparison is conducted with the other two schemes available in the open literature to show this improvement. The schematic of each scheme is shown in Fig. 4-8.

(a) Scheme I

(b) Scheme II

(c) Scheme CB/CFC
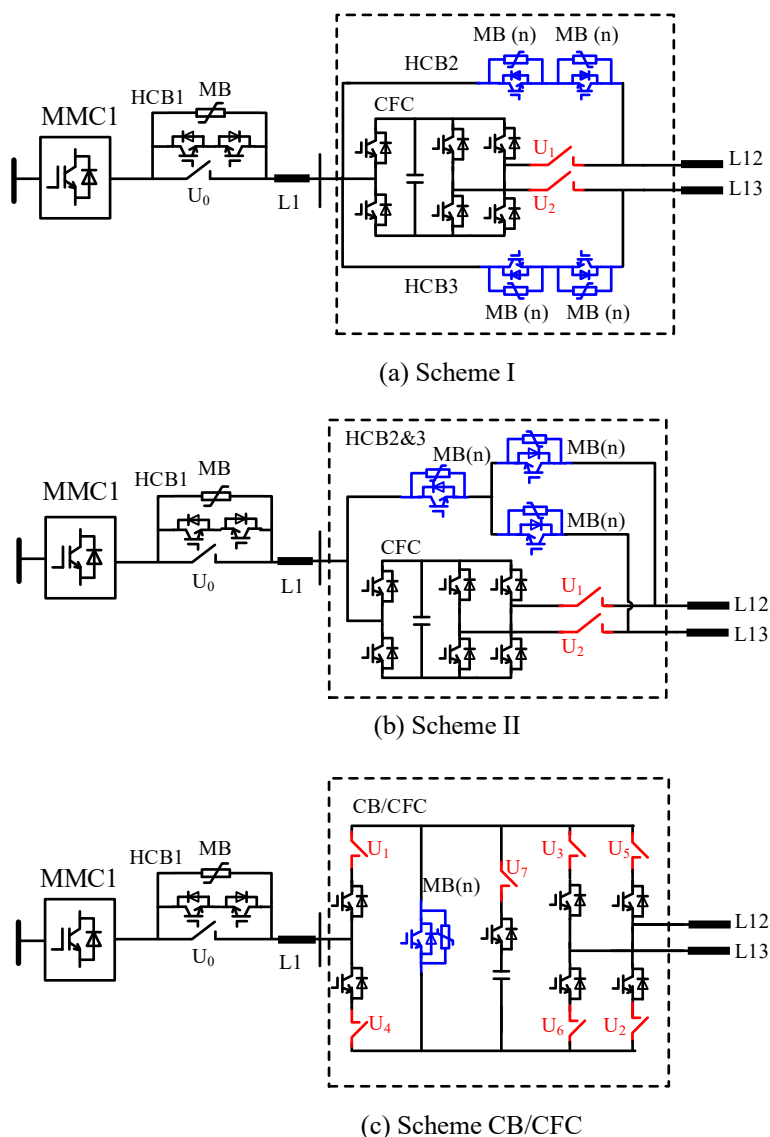
Fig. 4-8. Schematic of integrated schemes of CFC with HCB.

Fig. 4-8(a) shows the topology of the Scheme I presented in [194]. In this scheme, the LCSs of the two HCBs are integrated to operate as an HB-CFC. By such

integration, the number of power electronic devices is reduced as there is no need to employ a new CFC separately. However, four MB units are needed, and the number of devices in the MBs are the same.

Fig. 4-8(b) shows the topology of Scheme II [195]. Other than the combination of the LCSs, one MB unit is shared by two HCBs. Therefore, only three MB units are employed by this scheme, which can further save 25 % of power electronic devices (i.e. IGBTs in this application).

The proposed CB/CFC scheme is shown in Fig. 4-8(c). Compared to the other two schemes, the MB unit is shared by the three bridges, and since the low loss branches of the CB/CFC have the capability to redirect currents. Only uni-directional MB is needed. Therefore, the CB/CFC can further save around 50% of the power electronic devices.

An example is given below to show the advantages of the CB/CFC in terms of the number of power electronic devices used. The rated dc voltage is 500 kV, and the residual dc voltage for HCBs and the CB/CFC during the fault isolation process is around 900 kV. The maximum current interrupted by the CB/CFC is assumed to be 20 kA. Press-packed IGBTs rated at 4.5 kV/3 kA (5SNA 3000K452300) is used for the HCBs and CF/CFC [196]. The number of high voltage components is given in Table 4-1. From the table, it can be seen that the number of the MB units (MB contains hundreds of IGBTs for a 500 kV system) in the CB/CFC (Scheme III) is only 1/4 and 1/3 of Scheme I and Scheme II, respectively. This scheme will significantly reduce the number of IGBTs under this application. In the meantime, both the function of dc fault isolation and current flow control remains the same with the other two schemes.

Table 4-1. Number of high voltage components.

Scheme	No. of MB Units	No. of UFD Units	No. of IGBTs
I	4	2	$4n+6\times4$
II	3	2	$3n+6\times4$
III	1	7	$n+7\times4$

Notes: n is the number of IGBTs in the main branch. The value is normally in the range of hundreds for DCCBs for high voltage applications.

It should also be noted that the number of the mechanical switches (UFDs) in the CF/CFC is larger when compared to Schemes I and II. However, considering that the mechanical switches (UFDs) are more economical than power electronics-based MBs, the CB/CFC scheme exhibits a cost-effective and promising solution.

Table 4-2. Cost calculation of the MBs for 500 kV devices.

Scheme	No. of MB units	No. of IGBTs	Costs (Million)
I	4	800×4 = 3200	$ 28.8
II	3	800×3 = 2400	$ 21.6
III	1	800×1= 800	$ 7.2

Table 4-2 is given as an example to directly reflect the costs of MBs for the three schemes in a 500 kV system. It is assumed that 800 IGBTs are used to build up one MB unit (two IGBTs are used in parallel to withstand 20 kA fault current, and 400 IGBTs are in series to withstand 900 kV transient voltage per unit). Assuming that the price of one IGBT with its drives, RCD circuits, etc., is $9,000. Then the total cost of the MBs in each scheme is shown in the third column of Table 4-2. As it can be observed that the costs of the CB/CFC scheme are the lowest among the three schemes.

4.5.2. Modified topology

The HCBs, as a hybrid configuration, achieve a high interruption speed and a low conduction loss. However, reliability remains an essential aspect as it contains a large amount of power electronics devices (IGBTs) and several mechanical switches (i.e. UFDs).

A large amount of IGBTs is in series in the MB units. Therefore, to improve their reliability, press-packed devices, which have the short-circuit failure mode, are deployed. The failure of one single device will not influence the system operation as long as redundant devices are used. This can improve the reliability of the HCBs. As analysed in the previous subsection, the number of IGBTs of the CB/CFC scheme is much lower than the other two schemes. When only the IGBT's failure rate is considered, the CB/CFC is more reliable.

As the number of the mechanical switches in CB/CFC (7 UFDs) is larger than that of the other two schemes (2 UFDs). When one of the UFDs in the CB/CFC refuse to operate, it will fail to isolate a dc fault. The other UFDs are not redundant as the series IGBTs can do. To further improve the reliability, a modified topology is proposed, as shown in Fig. 4-9(a). By adding anti-series IGBTs to the MB of the original CB/CFC, a symmetrical topology is obtained. This symmetrical CB/CFC make it possible that there are two options to isolate one line. For example, when a fault occurs at L_{12}, either (U_4, U_5, U_6) or (U_1, U_2, U_3) can be used to isolate the fault. The two options are redundant to each other.
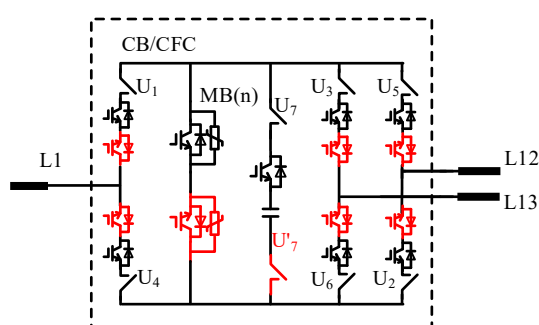
(a) IGBT based symmetrical topology
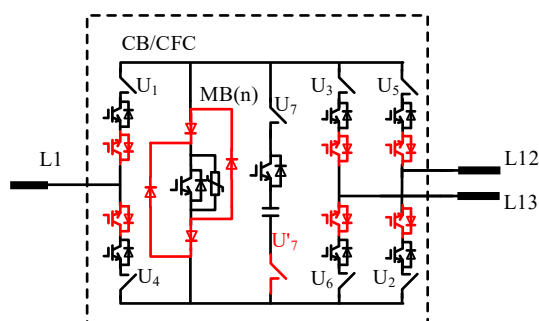
(b) Diode based symmetrical topology

Fig. 4-9. Modified topologies of the CB/CFC.

The modified topology doubles the number of IGBTs in the CB/CFC, although it improves the reliability. To reduce capital costs, a diode-based scheme is proposed. The topology is shown in Fig. 4-9(b). The diode-bridge are added to the MB unit to make it have the capability of interrupting bi-directional current. As the price of an IGBT is much higher (e.g. around 10 times) than that of a rectifier-diode, the diode-based scheme can further lower the cost. Similar concepts to reduce capital costs have been adopted in [137].

Since only one MB unit is adopted for the CB/CFC scheme, the number of IGBTs in the modified topology is still lower than Scheme I and II. This shows the advantage of the CB/CFC compared to the other two schemes.

4.6.   Simulation results

Simulations in PSCAD/EMTDC have been conducted to verify the operation and performance of the investigated CB/CFC. The MTDC grid shown in Fig. 4-3 is built, and the CB/CFC is installed in Node 1. The parameters of the system are given in Table 4-3. The transmission lines are modelled as π sections in this study. The maximum of its current capability is 1.5 kA. When the transmitted current is over 1.5 kA, the CB/CFC will be enabled to avoid overloading.

Table 4-3. Parameters of the MTDC system.

Parameter	Value
Rated dc voltage	500 kV
Rated power MMC1, 2, 3	1000 MW,1000 MW, 1500 MW
Transformer rated capacity	1200 MVA,1200 MVA,1800 MVA
Transformer ratio	500 kV/260 kV
Transformer leakage inductance	0.15 p.u.
Arm inductance	60 mH
SM Capacitor	18 mF
Number of SMs in each arm	250
DC current limiting inductor	300 mH /100 mH
Pi-section (per 40 km)	0.38 Ω, 84.4 mH, 0.46 μF
Capability of transmission line	1.5 kA
Length of Line 12, Line 13, Line 23	200 km, 200 km, 200 km

In this study, MMC1 regulates the system's dc voltage V_{dc}. The other two MMCs regulate their active power P_2 and P_3, respectively. All three MMCs supervise their reactive power.

The parameters of the CB/CFC are given in Table 4-4. The maximum current interruption capability is 20 kA. A 10 mF capacitor is used in the CB/CFC as a dc bus, and its rated value is 5 kV. The switching frequency of the CB/CFC when operating as a CFC is 500 Hz. The residual voltage of the MOVs in this CB/CFC is 900 kV. Simulation results of the current flow control and dc fault isolation will be presented next.

Table 4-4. Parameters of the CB/CFC.

Parameter	Value
Maximum current interruption capability	20 kA
Maximum LCS current	20 kA
Rated CFC voltage	5 kV
Rated voltage of MBs/clamping voltage of MBs	500 kV/900 kV
Opening time of UFDs	2 ms
Switching frequency	500 Hz
Sampling frequency	20 kHz
Capacitor in the CB/CFC	10 mF

4.6.1. Current flow control

Three operating points (see Points A, B and C in Table 4-5) of the MTDC grid are selected to assess the performance of the CB/CFC for current flow control. When regulating the current flows, the operation of the CB/CFC is the same as an HB-CFC (as analysed in Section 4.3). Therefore, both the current sharing mode and current reversal mode will be verified.

Table 4-5. Operating points of the system.

Operating point	Parameters	MMC1	MMC2	MMC3
Point A	Active power	500 MW	500 MW	−1000 MW
	Node current	1 kA	1 kA	−2 kA
Point B	Active power	1000 MW	500 MW	−1500 MW
	Node current	2 kA	1 kA	−3 kA
Point C	Active power	500 MW	1000 MW	−1500 MW
	Node current	1 kA	2 kA	−3 kA

a) Current sharing mode

The simulation results are given in Fig. 4-10. As it can be seen from Fig. 4-10(a), the system operates at Point A initially. MMC1 and MMC2 provide 1000 MW active power to MMC3. The currents in transmission lines are all within their safe operating area (see Fig. 4-10(c)). From $t = 3$ s, the operating point moves to Point B. The active power provided by MMC1 increases from 500 MW to 1000 MW (i.e. the reference

for MMC1 increases from 500MW to 1000MW). This leads to an increase of the currents in transmission lines, and the current in L_{13} is beyond its rated capacity (i.e. 1.5 kA), reaching around 1.7 kA.
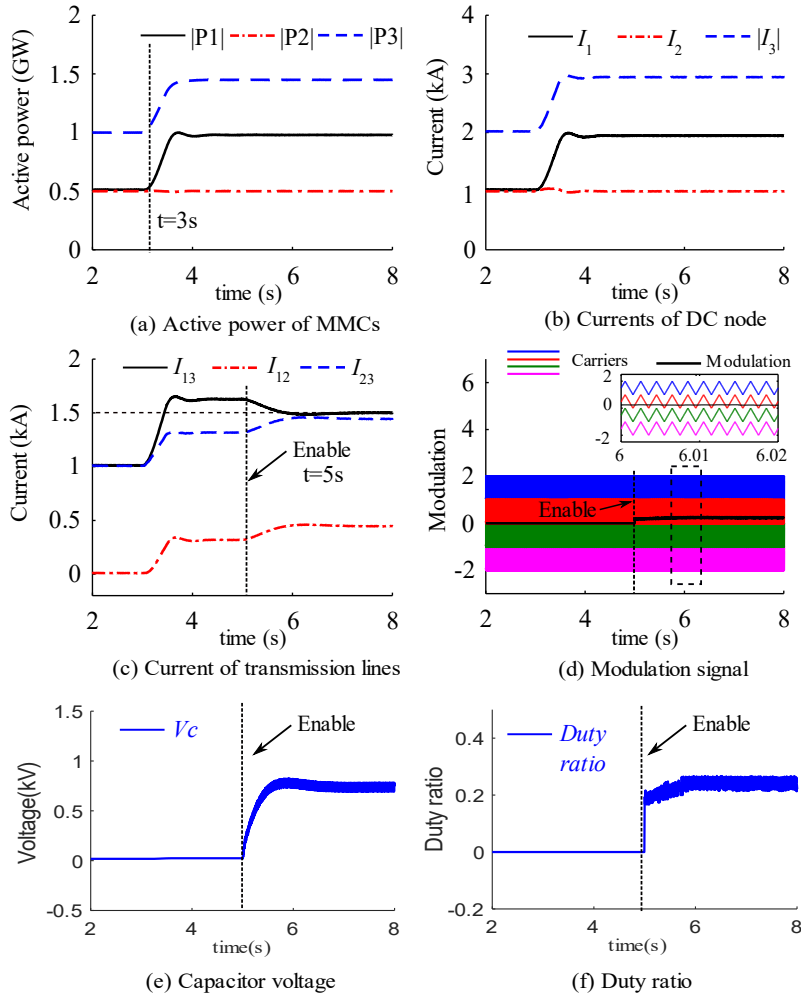
Fig. 4-10. CB/CFC operated in the current sharing mode.

To balance the current flow in the MTDC grid, the CB/CFC begins to work at $t = 5$ s. It can be seen from Fig. 4-10 (c) that the current in L_{13} is brought back to 1.5 kA by the operation of the CB/CFC at around $t = 6$ s. The additional current is transferred to the L_{12} and L_{23} to avoid overloading of the L_{13}. As the rated dc bus voltage of the CB/CFC is around 5 kV, its operation will not influence the node current provided by the MMCs. This can be seen from Fig. 4-10 (b)

As the currents in L_{12} and L_{13} ($I_{12} = 1.5$ kA, $I_{13} = 0.5$ kA) are smaller than the node current I_1 (2 kA see the black curve in Fig. 4-10(b)), the CB/CFC operates under the current sharing mode. This can be observed by the modulation signal shown in Fig.

4-10(d), which verify the analysis in Section 3.6. The voltage of the capacitor in the CB/CFC is given in Fig. 4-10(e). It can be seen that the voltage of the capacitor is around 1 kV when the CFC is enabled. This voltage is in series with transmission lines to help to regulate the dc current flow. The duty ratio of the PWM signal is given in Fig. 4-10(f).

b) Current reversal mode

To assess the CB/CFC's performance under its current reversal mode, the operations of the MTDC grid is transferred from Point A to Point C. Namely, the active power of MMC2 are increased from 500 MW to 1000 MW. The output current of MMC2 reaches 2 kA. This brings the current of L_{23} from 1 kA to a value of around 1.7 kA (see Fig. 4-11(c)), which exceeds the capacitor of L_{23}.
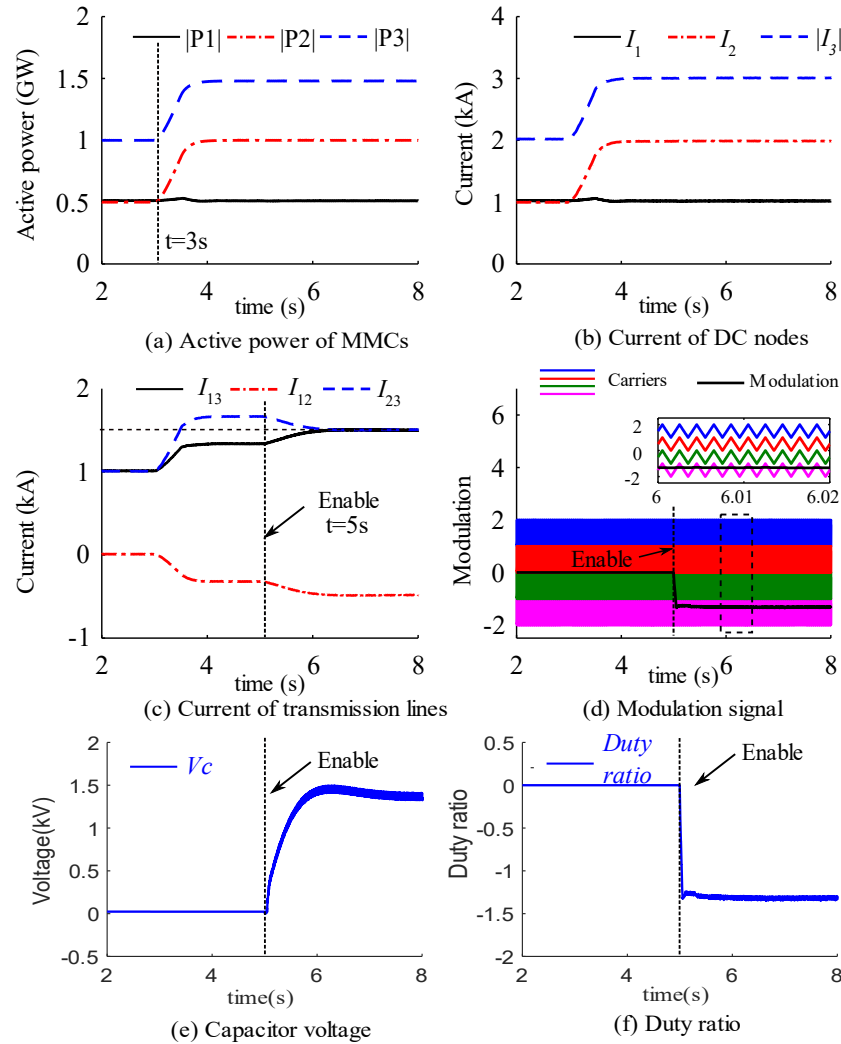
Fig. 4-11. CB/CFC operated in the current reversal mode.

To balance the current flows, the CB/CFC is enabled at $t = 5$s, and the current of L_{23} is reduced to around 1.5 kA at $t = 6$s. The extra current is re-directed into L_{12} and L_{13} to maintain the safe operation of the whole grid.

As it can be seen from Fig. 4-11(c), the current in L_{13} under this case (reaches 1.5 kA) is higher than the node current I_1 (1 kA), and the direction of $I_{12\text{ is}}$ reversed. The CB/CFC operates in the current reversal mode. This can also be observed in Fig. 4-11(d). The modulation signal locates in the area of the current reversal mode, which verifies the analysis in Section 3.6. The voltage of the capacitor in the CB/CFC is given in Fig. 4-11 (e). It can be seen that the voltage of the capacitor is around 1.5 kV when the CFC is enabled. This voltage is in series with transmission lines to help to regulate the dc current flow. The duty ratio of the PWM signal is given in Fig. 4-11(f).

4.6.2. DC fault isolation

To fully assess the operation of the CB/CFC for fault isolation, the faults (solid fault) occurring both at dc transmission lines and dc terminals are conducted. Fig. 4-12 shows the location of the dc fault in this study.

<div align="center">

(a) Fault at dc lines   (b) Fault at dc terminal

</div>
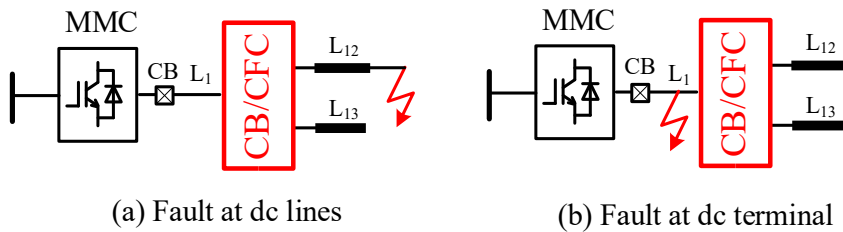
Fig. 4-12. Location of the dc faults.

a) A fault occurring at L_{12}

The fault occurring at L_{12} is taken as an example to show the behaviour of the CB/CFC when operating as an HCB. The simulation results are given in Fig. 4-13. The fault occurs at $t = 3$ s, which leads to a rapid increase of dc current in $L_{12,}$ as shown in Fig. 4-13(a). When the fault is detected, the CB/CFC starts its protection action process, as described in Fig. 4-5.
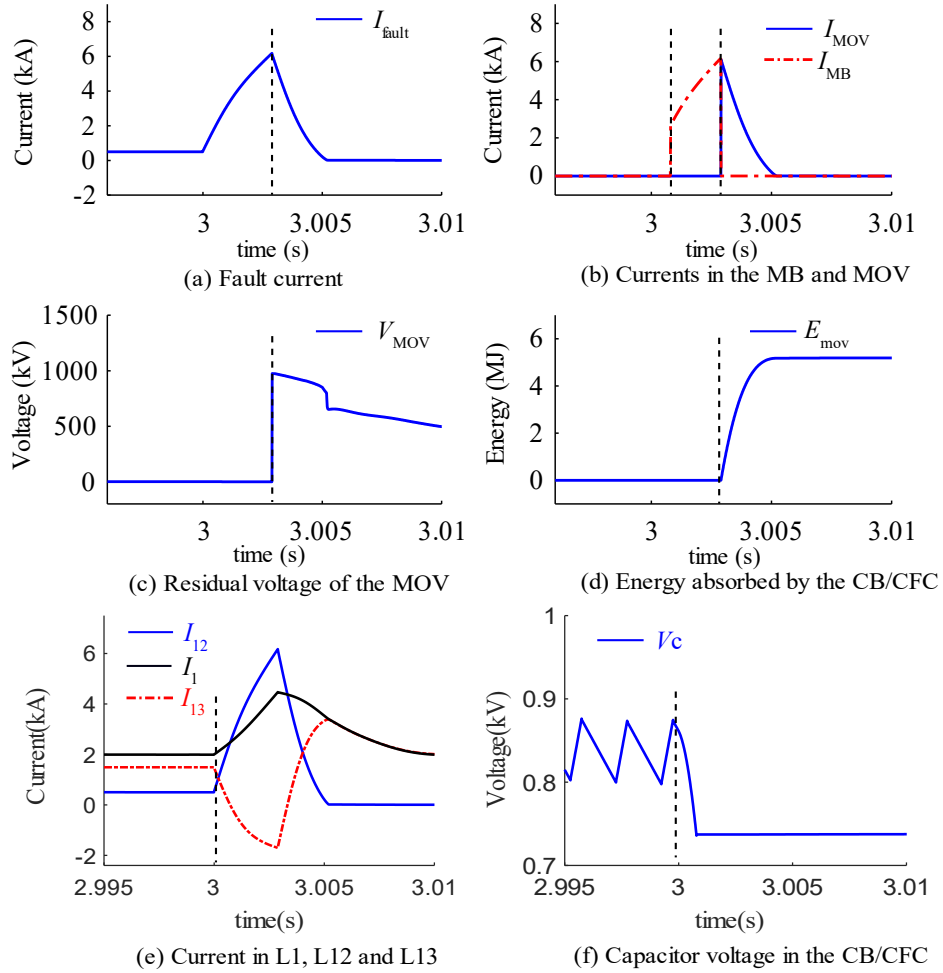
Fig. 4-13. Protection of the dc fault occurring at L_{12}.

It can be seen from Fig. 4-13(b) that the fault current is transferred into the MB at around $t = 3.0008$s, and the UFDs begins to operate after that. After around 2 ms, the UFDs are fully opened, which create a condition for the MB to be switched off. The MB is switched off to interrupt fault current at around $t = 3.0029$s. It can be observed in Fig. 4-13(c) that the residual voltage of the MOV is around 900 kV at the initial stage of the fault interruption. The fault current decays to zero at around $t = 3.0052$s, and the energy absorbed by the MOV is around 5.75 MJ, as shown in Fig. 4-13(b) and (d), respectively. The current in the transmission lines (connected with the CB/CFC) are given in Fig. 4-13(e). It can be seen that the current in the faulted line I_{12} is reduced to zero while the other lines continue to carry the current. The voltage of the capacitor in the CFC is given in Fig. 4-13(f). No overvoltage occurs during the transients. This simulation result verifies the function of the CB/CFC when it isolates dc faults which occur at the dc lines.

b) A fault occurring at the dc terminal

The simulation results of a fault occurring at the terminal are given in Fig. 4-14. The fault occurs at $t = 3$s. The current in the faulted line increases rapidly (see Fig. 4-14 (a)).

(a) Fault current

(b) Current in the MB and MOV

(c) Residual voltage of the MOV

(d) Energy absorbed by the CB/CFC

(e) Current in L12 and L13

(f) Capacitor voltage in the CB/CFC
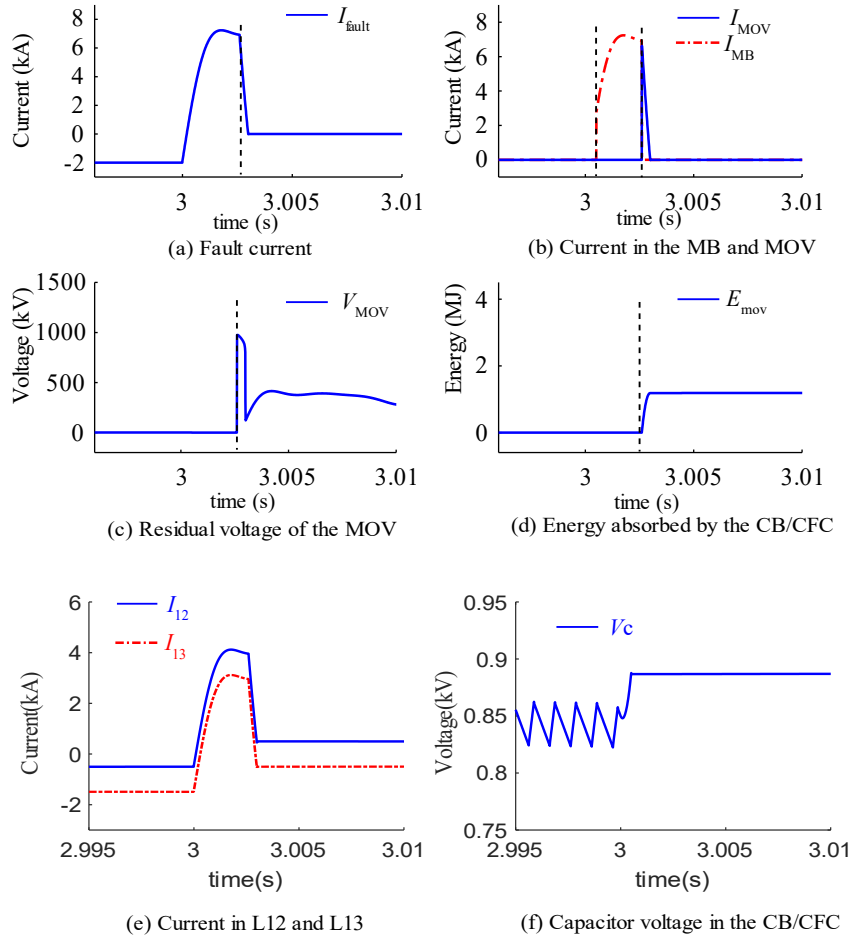
Fig. 4-14. Protection of the dc fault occurring at dc terminal.

After the fault is detected, the CB/CFC first transfer the fault current into the MB branch. This process completes at $t = 3.0005$s, as shown in Fig. 4-14 (b). Then the UFDs starts their actions and are fully opened after 2 ms. Following that, the MB begins to interrupt the fault current. The fault current decays to zero at around $t = 3.003$ s. The residual voltage and the energy absorbed by the MOV are given in Fig. 4-14(c) and (d), respectively. This result verifies the function of the CB/CFC when it isolates a fault occurring at the dc terminal. The current in the transmission lines (connected with the CB/CFC) are given in Fig. 4-14((e). It can be seen that the current in the healthy lines L12 and L13 continue to carry the current. This will be further explained

in the next subsection The voltage of the capacitor in the CB/CFC is given in Fig. 4-14 (f). No overvoltage occurs during the transients.

c) Comparison of dc fault isolation with other schemes

It should be noted that the isolation process of a fault occurring at the terminal with the CB/CFC and the other two or separate HCBs is different. As shown in Fig. 4-15(a), when a fault at the terminal is isolated with separate HCBs or the devices of Scheme I and II, L_{12} and L_{13} are also disconnected from each other as they both need to be disconnected with L_1. This will influence the current flow between L_{12} and L_{13}.

(a) Separate HCBs and Schemes I, II   (b) CB/CFC
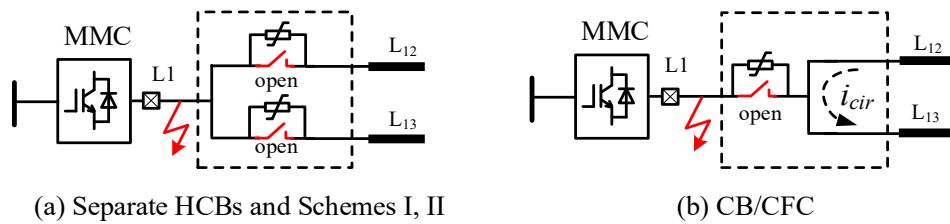
Fig. 4-15. Fault isolation process at the dc terminal.

However, when the CB/CFC is adopted, L_{12} and L_{13} remain the connection between each other as only L_1 is disconnected from the network. This will reduce the influence of the fault on the whole dc system's operation.

Simulations are conducted, and detailed waveforms of the currents in transmission lines are given in Fig. 4-16. As it can be observed that the fault current is reduced to zero by at t = 3.003s, the fault isolation process of which has been analysed in the previous subsection. After that, L_{12} and L_{13} are disconnected from each other, and the current cannot flow through L_{12} and L_{13} anymore, as shown in Fig. 4-16(a).

(a) Separate HCBs or Schemes I and II   (b) CB/CFC
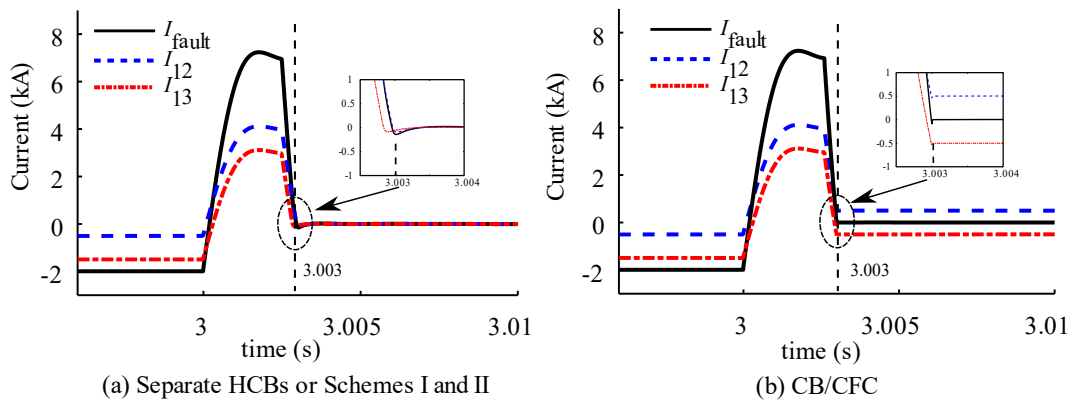
Fig. 4-16. Waveforms of the currents in L_{12} and L_{13}.

However, for the CB/CFC scheme, the connection of L_{12} and L_{13} still exists after the fault isolation process, and 0.5 kA dc current still flows through L_{12} and L_{13}. Therefore, the CB/CFC scheme will induce less influence on the healthy part of the MTDC grid.

4.7. Summary

In this chapter, a new device, the CB/CFC, which integrates the function of the HCB and the HB-CFC, is proposed. The CF/CFC can operate as a CFC during normal conditions to regulate current flows within a meshed MTDC grid. While under the dc fault conditions, it can operate as an HCB to isolate dc faults.

Compared to separate schemes, by the combination, the number of semiconductor devices can be significantly reduced with the same function achieved. Comparisons have been conducted with the other two schemes. It is revealed that the CB/CFC can further reduce the number of semiconductor devices.

To verify the analysis and the function of the CB/CFC, simulations have been conducted in PSCAD/EMTDC. Both the functions of dc fault isolation and current flow control have been assessed. Given the reduction in the number of IGBTs for a CB/CFC, the presented device represents a good option to achieve current flow regulation and dc fault protection—using a single integrated power electronics device.

Chapter 5   Protection of Valve-side Faults for HB-MMCs in Bipolar Systems

5.1.   Introduction

With the development of power electronic devices, converter topologies and their high-power applications, MMC based HVDC systems have been deployed in practical projects. HB based MMCs are preferred solutions as their capital costs are relatively lower compared to FB-MMCs or other hybrid topologies. Therefore, much attention has been paid to this topology.

At the initial stage, most MMC based HVDC systems are configured as symmetrical types [108], which contributes to reducing the insulation level. With the increasing demands of bulk power transmissions, bipolar HVDC systems are common options. Such configurations provide more power capability and increase redundancy as two asymmetrical poles can operate independently[111]-[112].

However, bipolar MMC based HVDC system shows specific characteristics and exhibits special technical issues. For instance, due to the asymmetrical groundings, the valve-side windings of the interface transformer have to withstand dc offset voltage, which increases their insulation levels. Thus, the interface transformer needs to be particularly designed [114].

Upon an insulation failure or a flashover occurring at the valve-side, bipolar systems experience severe consequences[197]-[198]. Both non-zero crossing and overvoltage issues appear under such faults for HB-MMCs [199]. The absence of zero-crossings may lead to the misoperation of grid-side ACCBs, which significantly endangers the safety of the systems [200]. In [198], an auxiliary grounding ACCB is installed at the grid-side of the converter to create zero-crossings in the total currents in the grid-side. However, the grid-side fault induced may aggravate the fault impact to nearby ac grids. In [200], an *R-L* based grounding method is proposed to create zero-crossings for grid-side current. However, the *R-L* grounding method may cause a large current flowing from the lower arms for a long time, which may lead to overheating of the diode. Extra dc breakers are needed to interrupt the current [201].

Full-bridge or hybrid SMs are proposed to create zero-crossing for grid-side current. However, these schemes will bring severe overvoltage issues in SMs [202]. The above discussion shows that the absence of zero-crossing issues caused by valve-side single-phase ground faults in HB-MMC based bipolar systems have not been fully addressed.

In this chapter, the characteristics of valve-side faults in HB-MMC based bipolar systems will be analysed in Section 5.2, with the fault detection method discussed in Section 5.3. The proposed protection methods will be presented in Section 5.4. To verify the effectiveness of the investigated methods, simulations in PSCAD/EMTDC are conducted with the results given in Section 5.5. Section 5.6 summarises this chapter.

5.2. Fault characteristic analysis

5.2.1. Control of HB-MMCs in bipolar systems

The analysis will be conducted with bipolar HVDC systems. A bipolar HVDC system is shown in Fig. 5-1. As it can be seen that solid grounding is used at the middle point of the dc side (between the two MMCs) for a bipolar configuration.
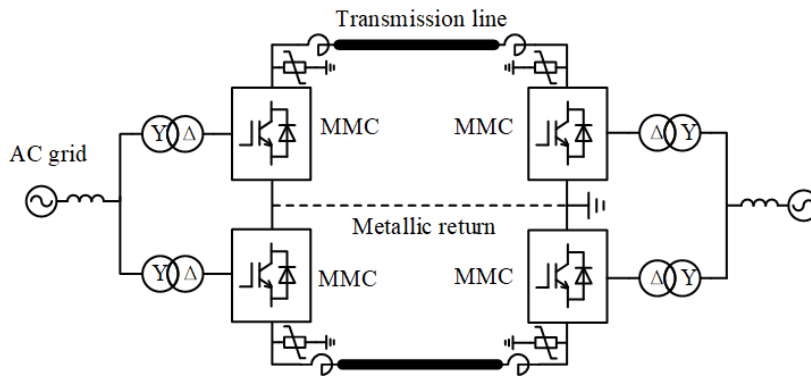
Fig. 5-1. MMC based bipolar system.

A detailed schematic of an HB-MMC with its interface transformer is given in Fig. 5-2. The valve-side windings of the transformer are configured as delta/wye types, which helps to remove the zero-sequence components caused by grid-side faults. The neutral ground point is set at the grid-side.

A single-phase equivalent circuit of an HB-MMC under normal operating conditions is shown in Fig. 5-3(a), with relevant waveforms (phase *a* as an example) illustrated in Fig. 5-3(b).
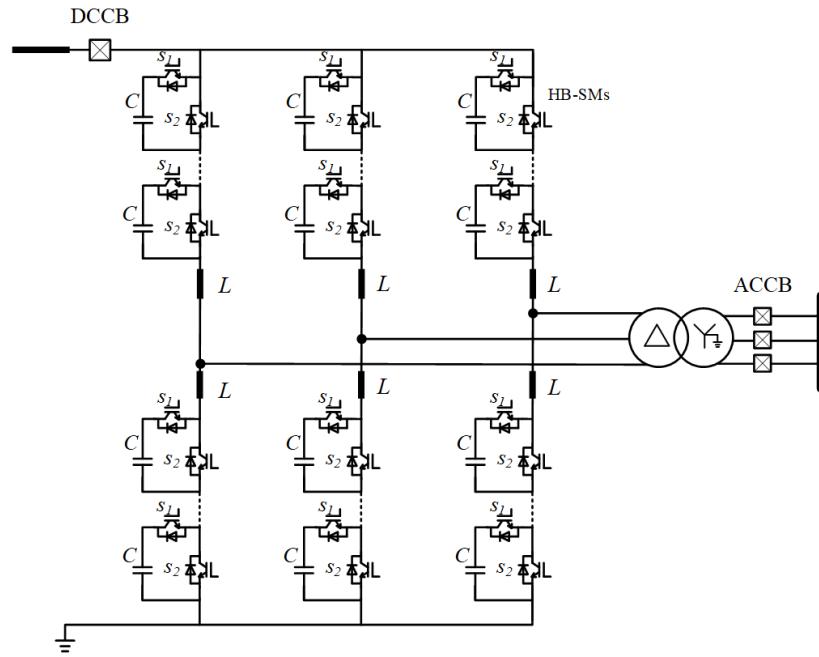
Fig. 5-2. Schematic diagram of an HB-MMC with its interface transformer.
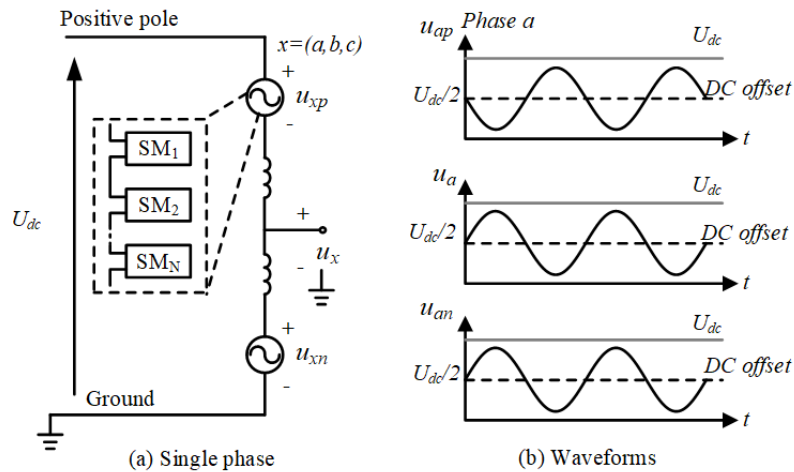
Fig. 5-3. Single-phase equivalent circuit diagram of the HB-MMC.

In an HB-MMC, the voltages of the upper arms and lower arms are modulated by SMs. Therefore, they are represented as controlled voltage sources (u_{xp} and u_{xn} in Fig. 5-3(a)). As discussed in Section 2.2.1, HB based SMs cannot generate symmetrical negative voltages as FB based SMs can do. The voltages generated by the upper and lower arms of an HB-MMC contain both ac and dc components,

$$u_{xp} = V_{dc}^{offset} - u_m \tag{5-1}$$

$$u_{xn} = V_{dc}^{offset} + u_m \tag{5-2}$$

$$u_m = \frac{U_{dc}}{2} m \sin(\omega t + \phi_x) \qquad (5\text{-}3)$$

where V_{dc}^{offset} is the dc offset voltage, u_m is the modulated ac components in the SMs of the upper and lower arms, m is the modulation index.

At the steady-state condition, the sum of upper arm voltage and lower arm voltages equals the dc-link voltage (the sum of the voltages of arm inductors in the upper arms and lower arms is zero for the fundamental components), i.e.

$$u_{xp} + u_{xn} = 2V_{dc}^{offset} = U_{dc} \qquad (5\text{-}4)$$

$$V_{dc}^{offset} = 0.5U_{dc} \qquad (5\text{-}5)$$

Therefore, the ac side output voltage is,

$$u_x = \frac{u_{xn} - u_{xn}}{2} + \frac{U_{dc}}{2} = \frac{U_{dc}}{2} m \sin(\omega t + \phi_x) + \frac{U_{dc}}{2} \qquad (5\text{-}6)$$

where u_x is the desired ac voltage (phase voltage), φ_x the phase angle, x represents phase *a, b* or *c*.

It can be observed from (5-5) that the dc offset voltage equals 0.5 $U_{dc.}$ As the lower arm is solidly grounded directly in a bipolar system, as shown in Fig. 5-3(a), the ac output voltage of the MMC (referred to the ground potential) equals the voltage of lower arms (the voltage of the arm inductor is not considered here), i.e.

$$u_x = u_{xn} = \frac{U_{dc}}{2} m \sin(\omega t + \varphi_x) + 0.5U_{dc} \qquad (5\text{-}7)$$

It can be seen from (5-7) that the valve-side windings of the interface transformer have to withstand this dc offset voltage in a bipolar system.

5.2.2.   Absence of zero-crossings

A valve-side ac fault leads to a new ground point in a bipolar system, which creates a zero-sequence current path. This is shown in Fig. 5-4. This path will induce a large

inrush current for the HB-MMC, and the faulted converter has to be blocked to avoid overcurrent and overheating of its IGBTs.
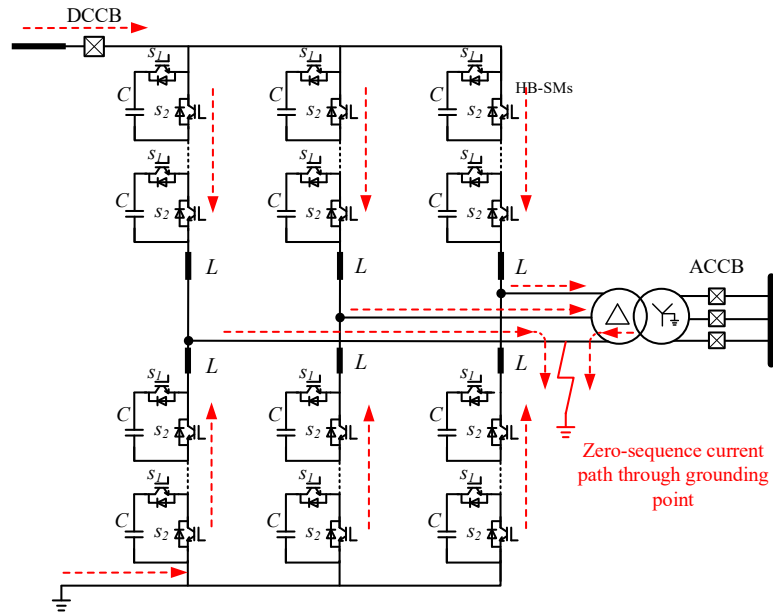
Fig. 5-4. Zero-sequence current path caused by the valve-side ac ground fault.

However, only blocking the HB-MMC is not enough to protect the converter and cannot interrupt the fault current in the lower arms of the HB-MMC since the free-wheeling diodes within the SMs still conduct the fault current and suffer from overcurrent. An equivalent circuit of the blocked HB-MMC following the fault is given in Fig. 5-5. The fault is assumed to occur at phase *c* here. The analysis will be given below.
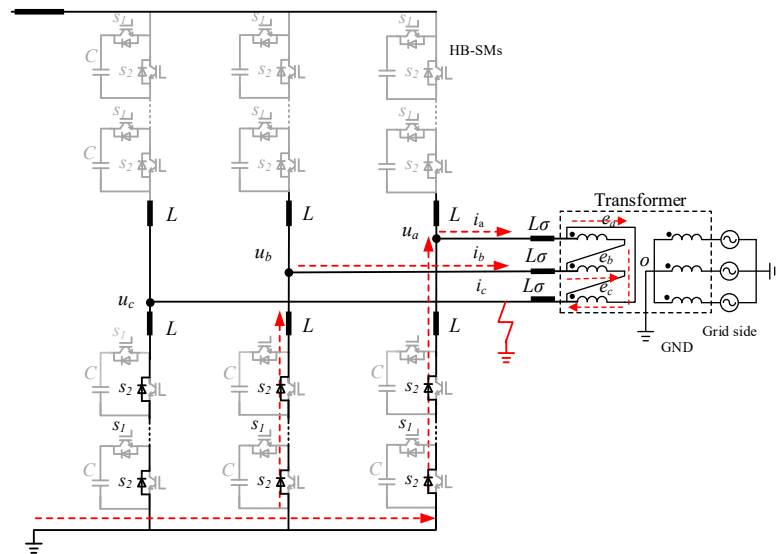
Fig. 5-5. Equivalent circuit of blocked HB-MMCs after valve-side ground faults.

As shown in Fig. 5-5, following the valve-side single-phase ground fault, the voltage of the faulted phase (phase c in Fig. 5-5) reduces to a low level (near to zero referred to as the ground potential). In contrast, the voltage of non-fault phases still exists since they are fed by the transformer. The ac components of voltage in the non-fault phases increase from the phase voltage to the line-to-line voltage. Furthermore, the dc offset voltage (0.5 U_{dc}) will disappear due to the faulted point created by the fault. The waveforms when a fault occurs at phase *c* is shown in Fig. 5-6 (Fig. 5-6(a) shows the pre-fault voltage and Fig. 5-6(b) shows the post-fault voltage).
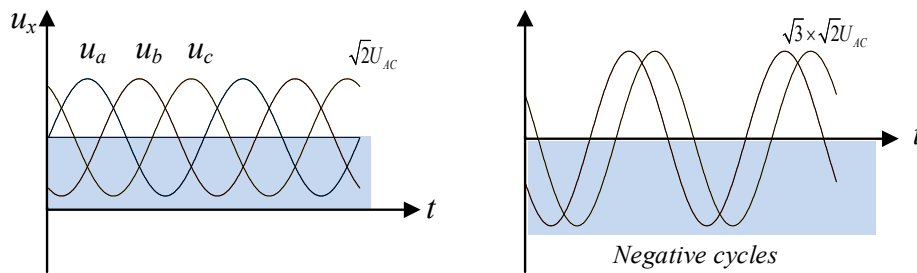
Fig. 5-6. Waveforms of valve-side pre-fault and post-fault ac voltages.

As it can be seen that negative cycles appear in the non-faulted phases (DC offsets disappear). Those negative cycles will keep generating current in the diodes of the lower arms even when the HB-MMC is blocked. An equivalent circuit is given in Fig. 5-7 to show the current in windings of the transformer following the fault.
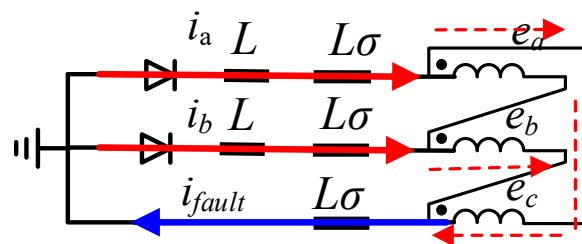
Fig. 5-7. Fault current in the windings of the transformer.

Since the currents in the diodes are uni-directional (see the arrows in Fig. 5-7), the fault currents contain large dc components. As a result, the current flowing through the windings of the transformer contains dc offset. This has been analysed in [200] in detail. As the current is provided by the ac grid through the transformer, the dc offset current in the windings of the transformer will lead to the absence of zero crossings in

the currents of the grid-side ACCB as shown in Fig. 5-8 (simulation results are given in Fig. 5-15(a)), which prevent its normal operations (cannot interrupt the fault current). Simulation results to verify this analysis (absence of zero-crossing) is given in Section 5.5 in detail.
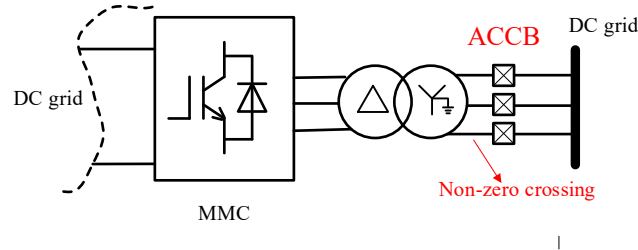
Fig. 5-8. The configuration of ACCB at the grid side.

Overheating of diodes may occur under such conditions without proper protection methods in place. The protection method to tackle this issue will be given in Sections 5.4.1 and 5.4.2.

5.2.3.　　Overvoltage of SMs

As analysed in the previous subsection, negative cycles in the valve-side ac voltages (in the non-faulted phases) are induced due to the ground fault. For instance, a fault that occurs at phase *c* is shown in Fig. 5-9.
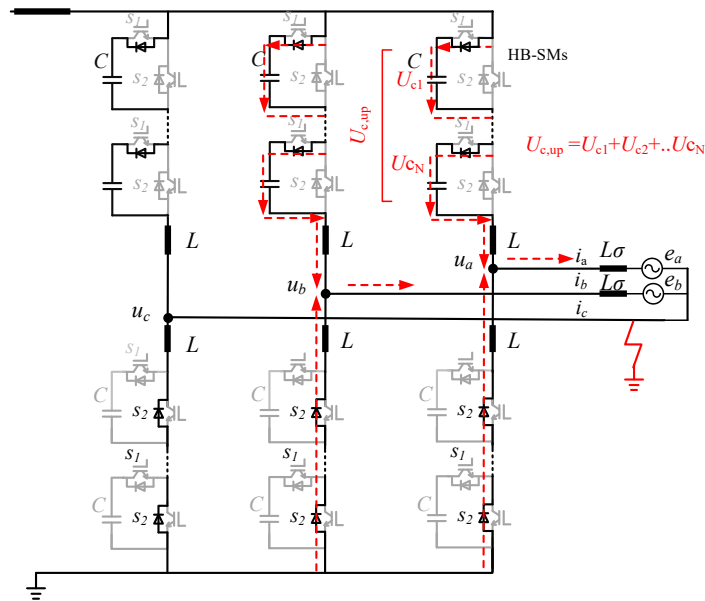
Fig. 5-9. A single-phase ground fault occurs in phase *c*.

Following the fault, the voltage in phase c is reduced to nearly zero (i.e. $u_c \approx 0$). However, the ac grid still feeds ac voltage to the valve-side through the interface transformer. An equivalent circuit is given in Fig. 5-9. The voltages fed by the transformer are represented by e_a and e_b in the non-faulted phases. The leakage inductance of the transformer and the inductance of the ac grid (seen by the valve-side) is represented by $L\sigma$. DC offsets are removed by the ground point in phase c. Therefore, the voltage in the non-faulted phase will withstand different potential compared to the pre-fault conditions.

Phase a is used as an example to calculate u_a after the fault. An equivalent circuit is given in Fig. 5-10.
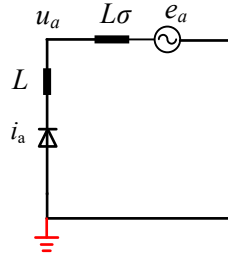
Fig. 5-10. Equivalent circuit of lower arms in phase a following a fault occurring in phase c.

The voltage u_a is determined by e_a, L and $L\sigma$. According to the Kirchhoff voltage law, u_a is derived as,

$$u_a = e_a \frac{L}{L_\sigma + L} \tag{5-8}$$

where e_a is the voltage fed by the ac grid, L_σ is the equivalent inductance of the interface transformer and grid, and L is the inductance of the arm inductor. It can be seen from (5-8) that, following the fault, the phase-to-ground voltage of the non-fault phases depend on the relationship of the leakage inductance of the transformer and the arm inductance. Since e_a is the ac voltage provided by the ac grid through the transformer, this leads to the voltage in the middle points of legs u_x ($x=a, b$) containing negative values (non-faulted phases). These negative values (do not exist in the pre-fault conditions) lead to overcharging of capacitors in the upper arms of the HB-MMC.

Normally, for an MMC under steady-state conditions, the sum of the capacitor voltage in either one upper arm or lower arm equals the dc voltage U_{dc}. However,

92

following the fault, the voltage of capacitors in the upper arms will be overcharged when the voltage in the middle of legs u_x *(x = a and b)* is negative [see the red dash line in the upper arms of HB-MMC in Fig. 5-9]. The voltage in the capacitors of upper arms is calculated,

$$U_{c,up} = U_{dc} - u_a = U_{dc} - e_a \frac{L}{L_\sigma + L}$$
(5-9)

where $U_{c,up}$ is the sum of the capacitor voltages in the upper arms.

It should be seen from (5-9) that the level of overvoltage is determined by the arm inductance L and the leakage inductance of the transformer together with transmission line L_σ. Normally, the arm inductance L is in the same range as L_σ [109]. Therefore, the level of overvoltage will not be higher than 0.5 p.u. In this study, the overvoltage level is around 0.3 p.u. This can be seen in the simulation results in Section 5.5.1. When the SMs are designed, voltage margins needed to be considered to withstand this overvoltage.

5.3. Fault detection

A valve-side ac fault creates a zero-sequence current path, which is different from grid-side ac faults or dc faults. The current path has been shown in Fig. 5-4. Therefore, the presence of zero-sequence current is used to detect such faults. When the detected zero-sequence current is higher than a threshold, a valve-side ground fault occurs.

$$\left| i_0 \right| = \frac{\left| i_a + i_b + i_c \right|}{3} > I_T$$
(5-10)

where i_0 is the zero-sequence current at the valve-side, and I_T is the threshold for fault detection.

5.4. Protection methods

5.4.1.   Double thyristor installed in SMs

To protect the diodes in MMCs from overheating under dc fault conditions, thyristors are deployed in mostly HB based SMs, as shown in Fig. 5-11 (a). The thyristors are triggered following the detection of dc faults to share and reduce the

current flowing through the diodes. Since the current capacity of a thyristor is much higher and the resistance is lower than that of a fast recovery diode, overheating of the diodes in the lower device of an HB-SM can be eliminated by the paralleled thyristor.
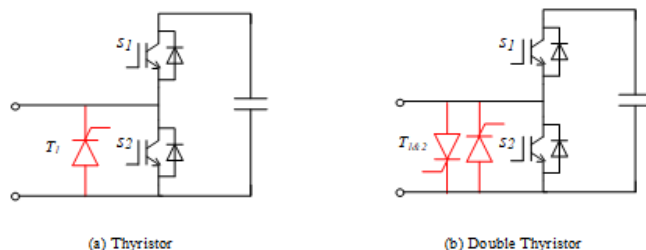
Fig. 5-11. Double thyristor-based SMs.

However, since thyristors are uni-directional devices, the issues of non-zero crossings still exist when T_1 is triggered under a valve-side single-phase fault. To concur with this issue, the double thyristor protection scheme is proposed. As shown in Fig. 5-11 (b), two thyristors T_1 and T_2, are installed in parallel with the lower IGBT in an HB SMs.

The system installed with double thyristors is given in Fig. 5-12. Such configurations of thyristor have been proposed to protect dc fault [203]. However, the function of protecting HB-MMCs from valve-side ac faults has not been analysed and verified.
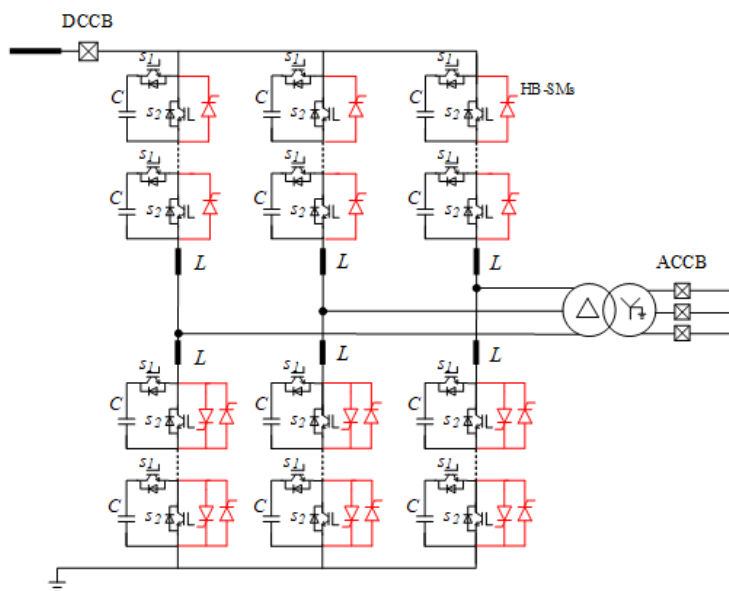
Fig. 5-12. Schematic of the HB MMC with double thyristor-based protection.

When a valve side ac fault is detected, the two thyristors in the lower arms, as shown in Fig. 5-12, are triggered. In this way, symmetrical current paths are created for ac components. The ac current will see zero crossings within a short time (a few fundamental periods), and related ACCB can be switched off to interrupt the fault current. The effectiveness of the double thyristor-based protection will be verified in Section 5.5.

As the press-pack diodes have more overcurrent capability, in some projects with press-pack devices, thyristors used to protect dc faults (e.g. T_1 in Fig. 5-11 (a)) can be removed. With such topologies, only T_2 is needed as shown in Fig. 5-13.
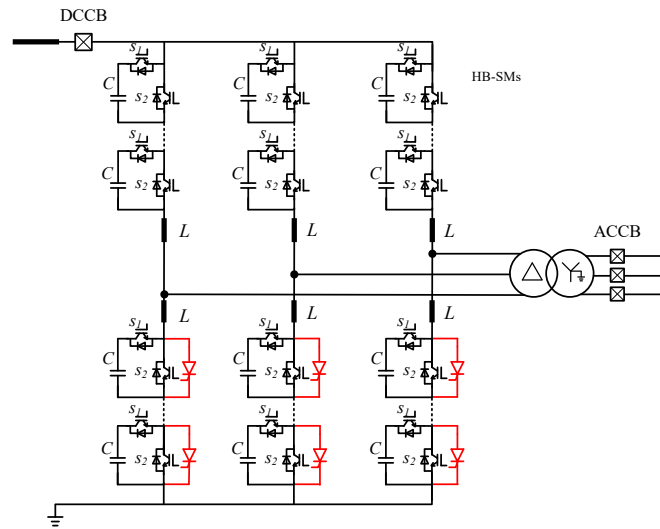
Fig. 5-13. Schematic of the HB MMC (Press-pack diode used) with single thyristor to protect valve-side faults.

5.4.2. Double thyristor installed at the ac-side

The protection method discussed in Section 5.4.1 solves the issues of non-zero crossings following valve-side ground faults. However, the overvoltage issue caused by the negative cycles still exist. To better tackle this problem, the thyristors can be re-located to the ac-side. This scheme is shown in Fig. 5-14. The double thyristors installed in SMs are put at the ac-side between ac lines. Such a method has been proposed to protect HB-MMCs from dc faults [204]. However, the function of protecting HB-MMCs from valve-side ac faults has not been analysed and verified, which will be analysed in this subsection.

When a valve-side fault is detected, the thyristors are triggered, which fully short circuits the system to create a symmetrical fault, thus, creating zero crossings for ACCBs.
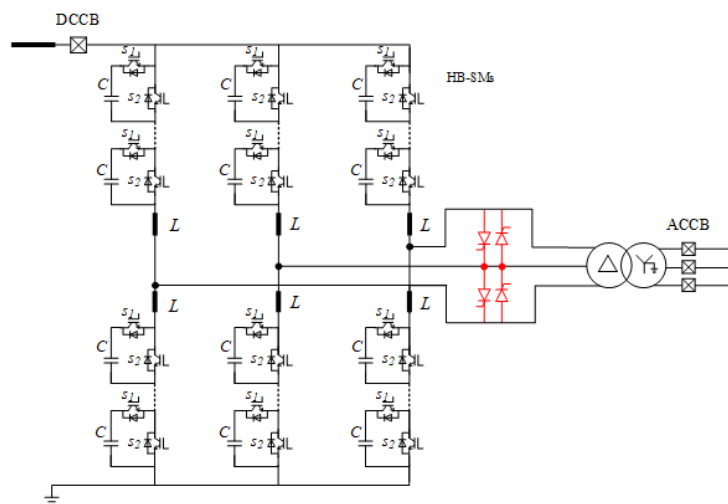
Fig. 5-14. Thyristors installed in the ac-side to protect valve-side faults.

This configuration brings three benefits. 1) The number of thyristors can be reduced. It can be seen that since the thyristors are used to short circuit ac lines, only two strings are needed between the three phases. While, if installed in SMs, the number of thyristors in the lower arms is equal to that of these strings. Furthermore, the thyristors in the SMs of the upper arms can be saved since the installed thyristors in the ac-side can help to divide the dc fault current when triggered after a dc fault. 2) Negative cycles seen by the upper arms are removed. Since the arm inductors are not included by the short circuit point created by the thyristors, u_x ($x = a,b,c$) will be nearly zero other than sinusoidal waveforms. Therefore, overvoltage can be eliminated. 3) Compact design of SMs may be achieved. Since the thyristors are moved from SMs to the ac-side, a compact design can be obtained physically. The effectiveness of the thyristor-based protection, which installs thyristors at the ac-side, will be verified in Section 5.5.

5.5. Simulations

To verify the analysis and proposed protection method, a point-to-point link, as shown in Fig. 5-1, is built in PSCAD/EMTDC. Since the positive and negative poles in a bipolar system can operate independently, simulations are conducted in the positive pole. The parameters of the system are given in Table 5-1.

Table 5-1. Parameters of the HB-MMC in each terminal.

Parameter	Value
Rated active power	2×1 GW
Rated dc voltage	± 500 kV
RMS ac voltage (line-to-line)	260 kV
Transformer capacity	2×1125 MVA
Transformer leakage inductance	0.15 p.u.
Transformer ratio	500 kV/260 kV
Arm inductance	105 mH
SM Capacitor	8 mF
Number of SMs in each arm	240
DC smoothing inductor	100 mH

5.5.1. Block the converter only

Simulations are conducted in this subsection when the HB-MMC is blocked directly to verify the analysis in Section 5.2.2.

Fig. 5-15 shows the waveforms following a valve side single-phase ground fault (occurs at t = 1s and in phase *c*) when the HB-MMC is blocked directly without other protection methods in place. As it can be seen from Fig. 5-15(b) that negative cycles appear for the valve-side voltages in the healthy phases. This leads to overvoltage of SMs (around 1.3 p.u.) in the upper arms of the healthy phases, as illustrated in Fig. 5-15(d). The analysis in Section 5.2.3 is verified. As analysed in section 5.2.2, the grid side current will lack zero crossings after the fault. This is verified by Fig. 5-15(a). The lack of zero-crossings prevents the switching off of the ACCBs. The fault current will not be interrupted timely, which will endanger the system's safety.

5.5.2. Double thyristors installed in SMs

The waveforms following a valve side single-phase ground fault, when the double thyristors installed in the SMs of lower arms are triggered, is shown in Fig. 5-16. It can be seen from Fig. 5-16 (b) and (d) that negative cycles still exist, and SMs in the upper arms experience around 1.3 p.u. overvoltage, which is similar to the case of blocking the HB-MMC only. However, since the double thyristors mitigate the single direction conductive phenomena of the diode after the HB-MMC is blocked, the grid side ac currents contain zero-crossings, as shown in Fig. 5-16 (a). Therefore, in such

cases, ACCBs can be switched off to isolate the fault. This verifies the analysis in Section 5.4.1.
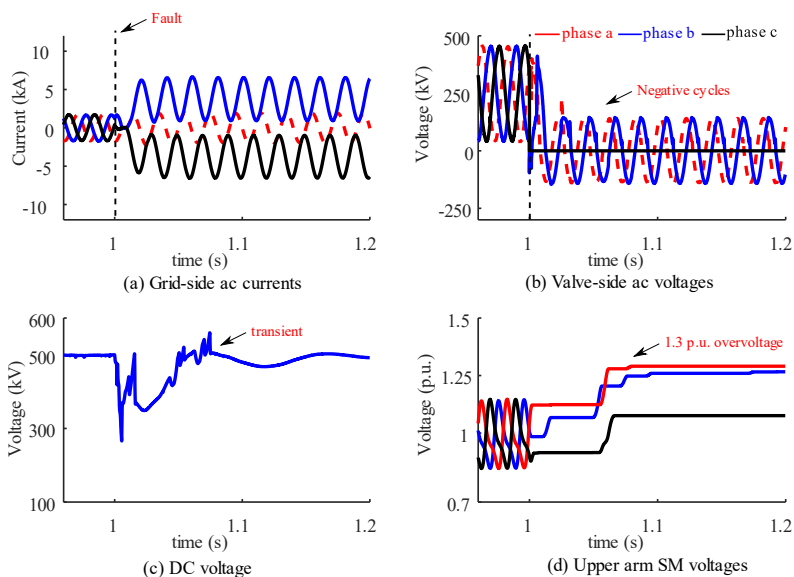
Fig. 5-15. Block the HB-MMC only following the fault.
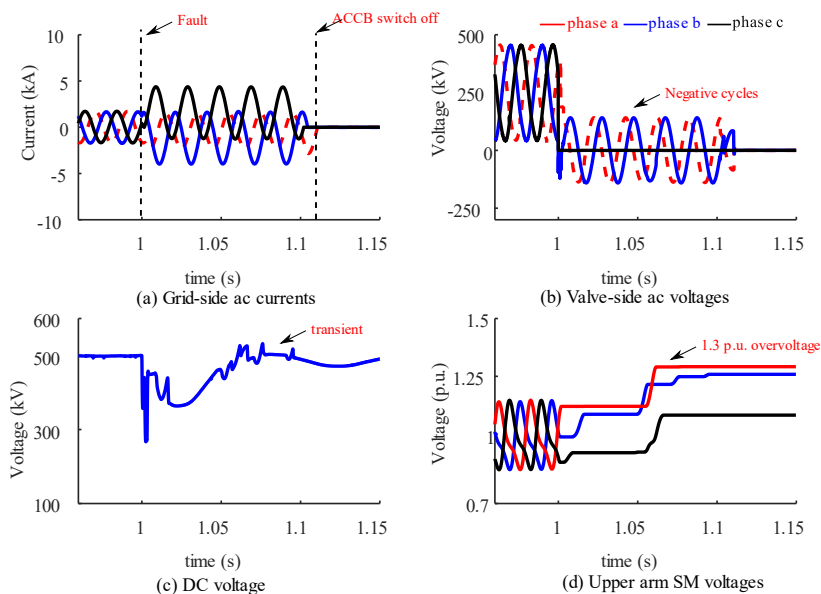
Fig. 5-16. Trigger the double thyristors installed in the SMS following the fault.

5.5.3. Double thyristors installed at the ac-side

The simulations with the double thyristor protection methods are conducted. Fig. 5-17 shows the waveforms following a valve side single-phase ground fault when the double thyristors installed at the ac-side are triggered. As the triggered thyristors cause a three-phase short circuit fault at the valve-side, there are no negative cycles for the

valve-side voltages [see Fig. 5-17 (b)]. Therefore, the SMs in the upper arms will not experience overvoltage, as shown in Fig. 5-17 (d). The thyristors create a symmetrical three-phase fault with zero-crossings exhibiting at the grid side. ACCBs can be switched off to isolate the fault. This is shown in Fig. 5-17 (a). Different to the scheme of thyristors installed in SMs, the advantage of the thyristors installed at the ac-side is that no overvoltage exists, and the number of thyristors can be reduced. The re-position of thyristors from SMs to the ac-side can provide a solution for compact designs of SMs. The analysis in Section 5.4.2 has been verified.
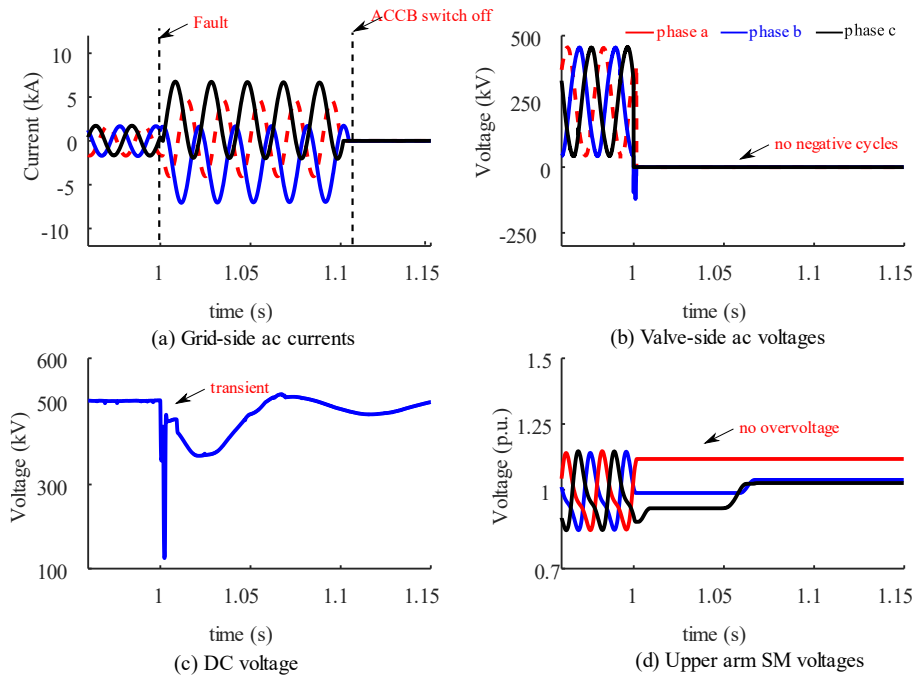
Fig. 5-17. Trigger the ac-side thyristors following the fault.

5.6. Summary

In this chapter, the characteristic of valve-side single-phase ground fault in HB-MMC based bipolar system has been analysed. The issues caused by such faults, no zero crossings and SM overvoltage, have been investigated.

To concur with these issues, two thyristor-based protection methods have been proposed. Adding double thyristors in the SMs of lower arms is proposed first. By triggering the double thyristors following the fault, zero crossings will be created and, thus, switching off the ACCBs can be used to isolate the fault timely. It has been revealed that the SMs in the healthy arms still face the issues of overvoltage (around 1.3 p.u.). To prevent the overvoltage problem, the other protection method has been

proposed: the thyristors are re-positioned to the ac-side. By such a configuration, the issues of SM overvoltage are solved. This method may provide other advantages: reducing the number of thyristors and contributing to a compact SM design. The two protection methods have been verified by simulation conducted in PSCAD/EMTDC. These two protection methods contribute to providing valuable references for designing protection systems against valve-side ac faults for HB-MMCs.

Chapter 6   Protection of Valve-side Faults for FB-MMCs in Bipolar Systems

6.1.   Introduction

FB-MMCs have been deployed in VSC HVDC systems in recent years due to their capability of dc voltage regulations. With such capability, an FB-MMC is able to ride through dc faults without the inclusion of DCCBs and, instead, can contribute to the fault recovery process. Therefore, FB-MMCs are promising alternatives for building dc grids.

The solutions of ac and dc fault ride-through in FB-MMC based HDC systems have been investigated widely, with methods being presented. The characteristics of dc faults handling are the attractions of adopting FB-MMCs with higher capital costs and power losses compared to HB-MMCs.

Since FB-SMs' output can be V_c, 0 and -V_c, this has given another freedom of the control of FB-MMCs. The dc voltage can be regulated with an extra controller and overmodulation is achievable [99]. This might be beneficial when the dc voltage has to be reduced for some conditions (e.g. under different weather conditions) [109]. The dc voltage of FB-MMCs can be regulated to zero or even reversed to ride through dc faults. The bipolar output of FB-SMs permits the converter to control both ac and dc current even under the conditions of a stiff dc short circuit.

Although with the capability of dc fault handling, FB-MMCs still cannot ride through the valve-side ac ground faults. Different to grid-side ac faults, valve-side ac faults create large zero-sequence fault currents as traditional *dq*-frame based control methods cannot handle zero-sequence components [205]. This may damage the converter without proper protection schemes in place. The FB-MMC has to be blocked to avoid overcurrent. However, blocking the FB-MMC directly will lead to a severe overvoltage (around 2 p.u.) in its SMs. Hybrid SMs are proposed to avoid overvoltage issues [103]. However, this scheme will lead to non-zero-crossing issues, as analysed in Chapter 5. An active control method is proposed in [206], which controls the dc voltage to zero following a valve-side single-phase ground fault. However, this

method may experience overcurrent in the converter arms, especially in an MTDC grid, where current from multi-lines will be injected into the faulted FB-MMC. As FB-MMCs are being assessed to use in real applications, to maintain safe operations of FB-MMCs against valve-side ac faults, protection methods are in great demand to be developed.

In this chapter, the behaviour of such a fault in FB-MMC based bipolar HVDC systems will be analysed with its consequences investigated. It has been found that the FB-MMC itself cannot ride through such a fault, and damage may be caused without additional protection devices included. Thyristors are deployed to protect the FB-MMCs. Based on that, two strategies-installing thyristors in the ac-or dc-sides, are proposed to protect FB-MMCs under such faults. The characteristics of these two methods are summarized. Simulation results are given in Section 6.5 to verify the effectiveness of the proposed methods. Section 6.6 concludes this chapter.

6.2. Fault characteristic analysis

6.2.1. Control of FB-MMCs in bipolar systems

As FB-SMs are adopted in the arms of FB-MMCs, the voltage in the upper and lower arms u_{xp} and u_{xn} ($x= a,b,c$) can be regulated to be positive and negative. Therefore, the dc offset voltage can also be regulated. This is different from that of HB-MMCs. An equivalent circuit of FB-MMCs is shown in Fig. 6-1.
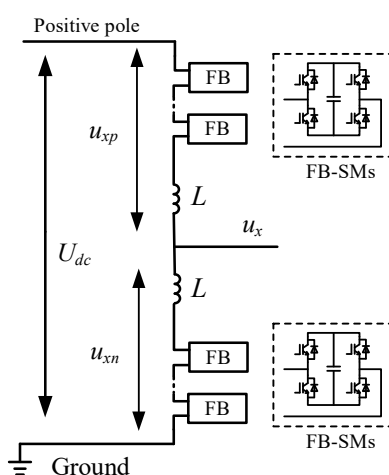
Fig. 6-1. Equivalent circuit of FB-MMCs (single phase is used as an example).

For FB-MMC, the regulated voltage in the upper and lower arms are,

$$u_{xp} = V_{dc}^{offset} \times k - u_m \tag{6-1}$$

$$u_{xn} = V_{dc}^{offset} \times k + u_m \tag{6-2}$$

$$u_m = \frac{U_{dc}}{2} m \sin(\omega t + \phi_x) \tag{6-3}$$

where V_{dc}^{offset} is the dc offset voltage, u_m is the modulated voltage in the SMs of the upper and lower arms for the ac components, m is the modulation index, k is the index to regulate dc offset voltage.

At the steady-state condition, the sum of upper arm voltage and lower arm voltages equals the dc-link voltage (the sum of the voltages of arm inductors in the upper arms and lower arms is zero for the fundamental components), i.e.

$$U_{dc} = u_{xp} + u_{xn} = 2V_{dc}^{offset} \times k \tag{6-4}$$

Therefore, the ac side output voltage is,

$$u_x = \frac{u_{xn} - u_{xp}}{2} + \frac{U_{dc}}{2} = \frac{U_{dc}}{2} m \sin(\omega t + \phi_x) + V_{dc}^{offset} \times k \tag{6-5}$$

where u_x is the desired ac voltage (phase voltage), φ_x the phase angle, x represents phase a, b or c.

When the FB-MMC are operating the same as HB-MMCs, $k = 1$. Under this condition, the offset voltage equals 0.5 $U_{dc.}$ However, when a dc fault occurs, k can be set to zero. In this way, the dc side voltage can be regulated to zero. This mode can be used to limit the dc current during dc fault conditions. Furthermore, k can be set to a negative value to help to rapidly extinguish the arcs. When the magnitude of k is smaller than 1 (between 0 to 1), an FB-MMC operates under the overmodulated mode [109].

6.2.2. Overvoltage of SMs

Similarly, once a valve-side ac fault occurs, a large zero-sequence current flow through the ground point. The FB-MMC has to be blocked to avoid overcurrent and

overheating of its IGBTs under conventional *dq*-frame based control schemes. When the FB-MMC is blocked, the FB-SMs in the lower arms will interrupt the fault current with their series inserted capacitors. This is shown in Fig. 6-2. The sum of the voltage V_c in each arm of the FB-MMC equals to U_{dc} (steady conditions are considered). This will stop current flowing through the free-wheeling diodes in the lower arms, which is different from the case in the HB-MMC systems.
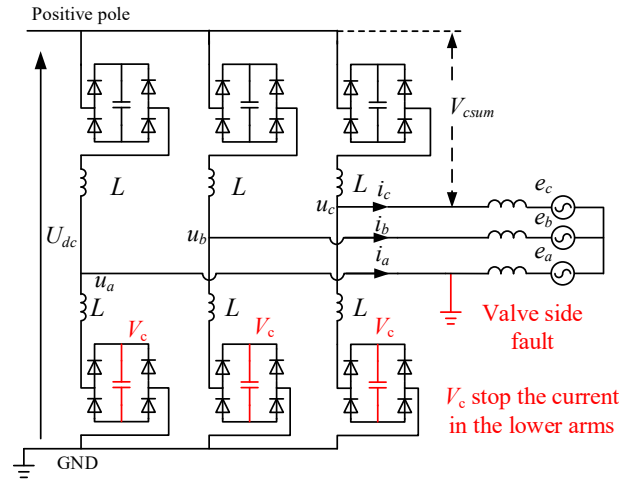
Fig. 6-2. Zero-sequence current path following an SFG fault at phase *a*.

Although the absence of zero-crossing issues, caused by the free-wheeling diodes, are eliminated, this will bring another challenge to FB-MMCs. After the valve-side ac fault, the voltage of the faulted phase becomes zero. The voltage magnitude of the other two healthy phases increase from (6-6) to the magnitude of line-to-line voltage (6-7) and, at the same time, the dc offset disappears,

$$u_{a,b,c} = \sqrt{2}V_{AC}\sin(\omega t + \varphi_{a,b,c} + \Delta\varphi_{a,b,c}) + 0.5U_{dc} \tag{6-6}$$

$$u_{b,c} = \sqrt{3} \times \sqrt{2}V_{AC}\sin(\omega t + \varphi_{b,c} + \Delta\varphi_{b,c}) \tag{6-7}$$

where V_{ac} is the RMS value of the output ac voltage under normal conditions.

Under this condition, the dc-link will charge the SMs in the upper arms during the negative cycles (the charging path is shown in Fig. 6-3), which will lead to the overvoltages of the SMs in the upper arms of the FB-MMCs. It should be noted that since the free-wheeling diodes in the HB-MMCs conduct current during the negative cycles, the magnitude of voltage $u_{b,c}$ is much lower. This is the difference between HB-MMCs and FB-MMCs following a valve-side ground fault.
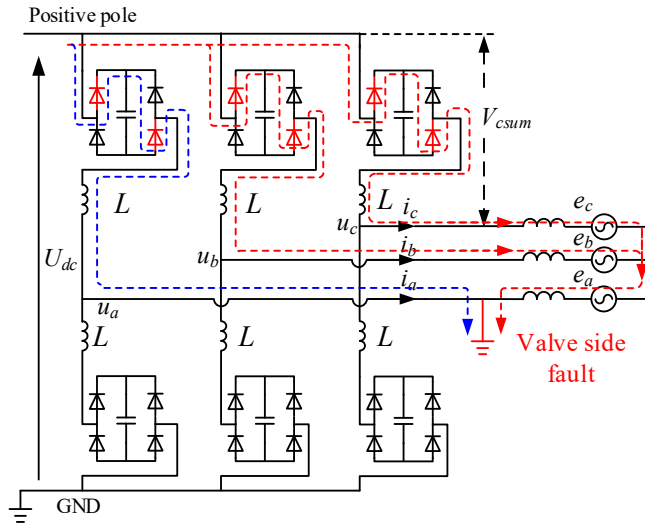
Fig. 6-3. Charging path of SMs in upper arms.

Under pre-fault conditions, the voltage of the upper arms is,

$$u_x^{up} = U_{dc} - u_x = 0.5U_{dc} - \sqrt{2}V_{AC}\sin(\omega t + \varphi_x + \Delta\varphi_x) \tag{6-8}$$

$$\left|u\right|_x^{up} = \left|U_{dc} - u_x\right| = 0.5U_{dc} + \sqrt{2}V_{AC} = (0.5 + 0.5m)U_{dc} \tag{6-9}$$

where m is the modulation index, which is normally smaller than 1.

Under normal conditions, the magnitude of the voltage, which the upper arms withstand, is lower than U_{dc} (i.e. the total dc voltage of the SMs in one upper arm is smaller than U_{dc}). However, following a valve-side ac fault, substitute (6-7) into (6-9), the voltage of the upper arms in the healthy phases results in,

$$u_{b,c}^{up} = U_{dc} - u_{b,c} = U_{dc} - \sqrt{3} \times \sqrt{2}V_{AC}\sin(\omega t + \varphi_{b,c} + \Delta\varphi_{b,c}) \tag{6-10}$$

Under such conditions, the magnitude of the voltage of the upper arms in the healthy phases equals to,

$$\left|u\right|_{b,c}^{up} = \left|U_{dc} - u_{b,c}\right| = U_{dc} + \sqrt{3} \times \sqrt{2}V_{AC} = (1 + 0.866m)U_{dc} \tag{6-11}$$

As it can be seen from (6-9) and (6-11) that after the fault, the magnitude of the upper arm voltage increase from a value of $(0.5+0.5m)U_{dc}$ to $(1+0.886m)U_{dc}$. When the worst case is considered (modulation index $m = 1$), the voltage reaches 1.886 p.u. of its rated value. Such a high voltage will charge the capacitors in the SMs of the

upper arms to around 2 p.u. when the transient energy is also considered. Charging paths are shown in Fig. 6-3 (with red dashed lines). Such an overvoltage may damage the FB-MMCs. Therefore, an effective protection strategy is required to protect FB-MMCs under valve-side ac fault. To protect the SMs from being overcharged, either the dc bus could be reduced, or the negative cycle of phase voltages be removed. Protection strategies from both its dc-side and ac-side will be presented next.

6.3.   Protection methods

6.3.1.   Protection from dc-side

As analysed in the previous section, only blocking the FB-MMC under a valve-side fault brings severe overvoltage in its upper arms. Since the FB-MMC can regulate its dc voltage to zero. One possible solution could be reducing the dc voltage actively following a valve-side ac ground fault. For the ac side current control, a zero-sequence current controller is added to supervise the ac side current. This has been proposed and presented in [206]. This method utilises the characteristic of the FB-MMC. However, this method still faces risks. Once the overcurrent is triggered during the protection process, the FB-MMCs will have to be blocked, which will lead to overvoltage of SMs again. This is mostly possible to occur in an MTDC grid where several dc lines will inject current to the faulted converter when its dc voltage is regulating to zero. Therefore, additional protection methods need to be studied.

To protect FB-MMCs, a thyristor-based branch is proposed and installed in the dc terminals to reduce the dc-link voltage following the fault. It can be seen from Fig. 6-4 that the thyristor branch is in parallel with the FB-MMC at its dc-side.
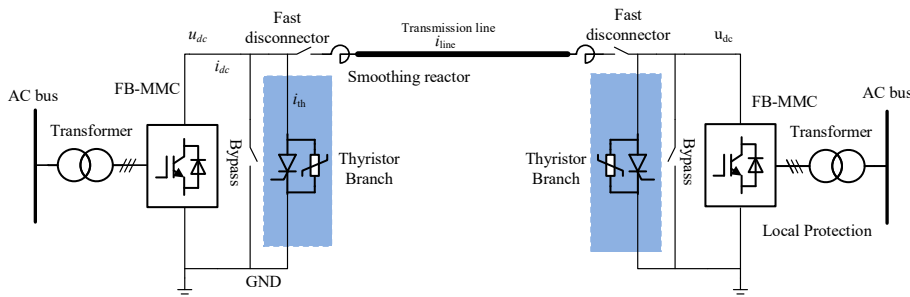
Fig. 6-4. Proposed dc-side thyristor-based protection method.

a) Faulted converter

Following a valve-side ac fault, the thyristor branch is triggered. The energy stored in the dc inductors and transmission lines is released immediately through the triggered thyristor branch instead of charging the SMs in the FB-MMC. In this way, the FB-MMC is blocked safely without SM overvoltage issues. After that, the grid-side ACCB can be used to disconnect the faulted terminal from the ac grid permanently.

b) Remote converter

The triggered thyristor branch creates a dc short circuit, which relieves the overvoltage issues of the faulted converter. However, the other FB-MMCs within the grid may experience overcurrent due to the short circuit.

Thanks to FB-MMCs' capability of dc voltage regulation, dc current controllers can be added to the control loop of FB-MMCs to avoid the dc-side overcurrent. A point-to-point link is given as an example to illustrate the dc control loop. This is shown in Fig. 6-5. As it can be seen, a cascaded configuration is adopted. The outer control loop (can be either dc voltage or active power control loop) generates a reference I_{dcref} for the dc current controller. The dc current is fed back and compared with its reference. This can ensure that the dc current is supervised by the FB-MMCs all the time. Even during dc fault conditions, its value can be maintained within the safe operating area. Thus, overcurrent is avoided.
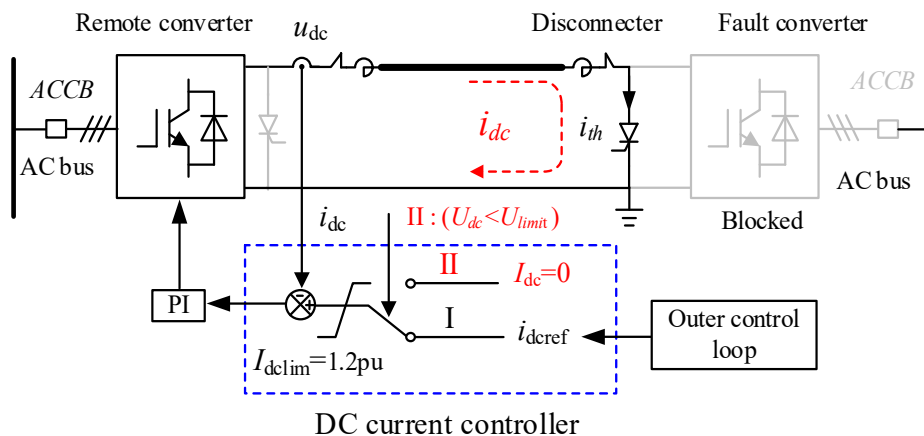
Fig. 6-5. DC current control loop.

For the remote FB-MMCs (healthy converters) in an MTDC grid, when the dc-link voltage is lower than a pre-set value (e.g. when U_{dc} is lower than 0.85 p.u.) or a dc fault is detected by its relays, the reference I_{dcref} is set to zero. This will contribute to reducing the current in the thyristor branch to zero. After the current flowing through the thyristor branch become zero, it will be automatically switched off. The disconnectors installed in the terminal can be used to isolate the faulted converter, and the other healthy parts of the grid can restart their operations. For a point-to-point link, the healthy terminal can only operate as a STATCOM due to the disconnection of the other terminal.

6.3.2. Protection from ac-side

As the presence of negative cycles of ac voltage following a valve-side ground fault is the main reason that causes the overvoltage issue. The dc-link will charge the capacitors in the upper arms during the negative cycles. Removing the negative cycles of ac voltages is an alternative solution.

To remove the negative cycles following the fault, thyristors are installed at the ac-side, as shown in Fig. 6-6. This method has been proposed to protect HB-MMCs from valve-side ac ground fault in Chapter 5. They will be triggered when a valve-side fault is detected to avoid the severe overcharging of SMs. The effectiveness of this method will be verified in Section 6.5.
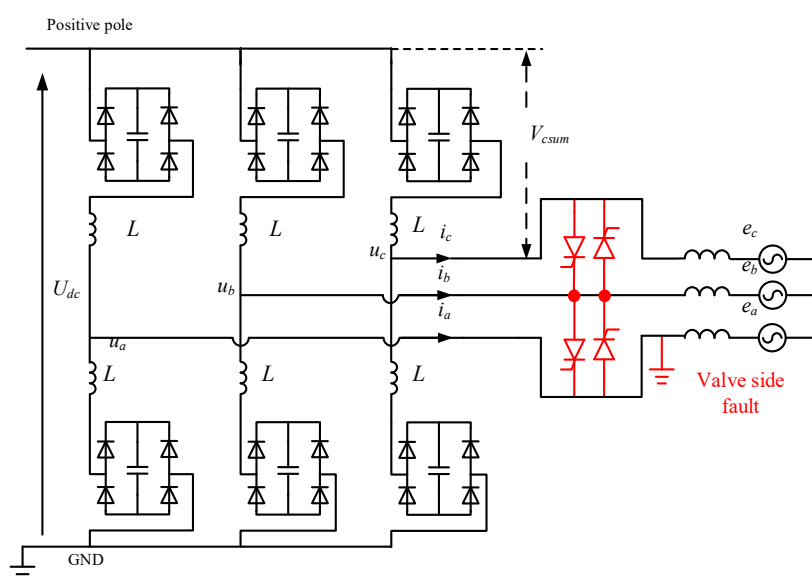
Fig. 6-6. Thyristor based protection when installed at the ac-side.

6.3.3.   Analysis of ac and dc side protections

In Sections 6.3.1 and 6.3.2, thyristors are installed at the dc- and ac-sides, respectively, to protect FB-MMCs from overvoltage. These two methods have their merits and demerits.

It can be seen that when the thyristors are installed at the ac-side, the protection procedure will not cause much influence on the dc system following the valve-side fault. The other healthy parts will maintain their operation. However, as the trigger thyristors cause a three-phase ac fault to the connected ac systems, this may inject fluctuation to the nearby ac grid.

When the thyristors are installed at the dc-side, the procedure will induce a dc- side short circuit, which may influence the operation of the dc system. But an FB-MMC based system can ride through the transient dc fault. By comparing the number of thyristors of these two schemes, it can be found that only one string of thyristors is used in Fig. 6-4 (*N* thyristors used). While in Fig. 6-6, four strings of thyristors (*4N* thyristors) are needed for the ac side protection scheme. The number of thyristors in the dc-side scheme is around only 25% of the ac-side protection scheme, which has been listed in Table 6-1. This is the advantage of such a scheme, and little influence is induced to the nearby ac grid. The characteristics of the two schemes are summarised in Table 6-1.

Table 6-1. Comparisons of the two schemes.

Schemes	Thyristors installed at ac-side	Thyristors installed at dc-side
Influence on dc systems	Small (Transient)	Large (DC short circuit)
Influence on ac systems	Large (AC short circuit)	Small (Transient)
Number of thyristors	4 *N*	*N*

It should be based on the practical circumstance when selecting these two schemes to protect FB-MMC against valve-side single-phase ac faults. The effectiveness of these two methods will be verified in Section 6.5.

6.4.   Transient fault considerations

As analysed in previous sections, FB-MMCs have the capability to control their dc voltage to zero actively. Therefore, when the dc-side thyristors are triggered as

presented in Section 6.3.1, the FB-MMCs can still be active. This may provide freedom to protect transient faults and make the recovery of the whole system faster.

The protection method presented in Section 6.3.1 blocks the faulted FB-MMC directly following the triggering of the thyristor branch. After that, its ac-side ACCB and dc-side disconnector are switched off to isolate the faulted converter to ensure the healthy parts of the MTDC grid are operational. This method is suitable to clear a permanent valve-side ac fault, such as the fault caused by the insulation failure of wall-bushing or windings of transformers. Under a non-permanent fault condition, such as the fault caused by recoverable flashover, the FB-MMC should be re-connected and restored to operate so as to reduce the impact on the whole MTDC grid and power transmission. However, the reclosure of an ACCB takes quite a long time (e.g. several hundred milliseconds). This leads to an undesirable interruption of power transmissions.

To mitigate these shortcomings, an active fault protection method is investigated in this subsection. After the thyristor is triggered, the faulted FB-MMC is kept in operation with extra controllers as shown in Fig. 6-7 and back to pre-fault condition when the fault is cleared. Upon a non-permanent fault, the recovery time of the system can be reduced with this method.
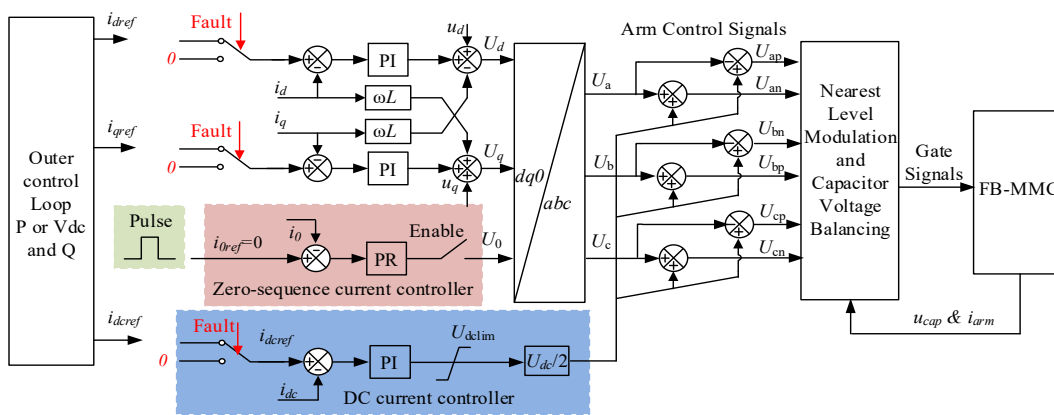
Fig. 6-7. Active based protection method with its corresponding controllers.

a) DC side control

To keep the faulted FB-MMC actively operated after the thyristor branch is triggered, a dc current controller is added to the FB-MMC's control loop (see the blue area in Fig. 6-7). The reference of the dc current is set to zero when a valve side fault

is detected. The FB-MMC will regulate its dc side current to zero, which avoids overcurrent and overheating of its IGBTs and, in the meantime, contributes to the reduction of the current in the thyristor branch.

b) AC side control

DC side current can be regulated by the FB-MMCs by adding dc current controller. However, once a valve-side ground fault occurs, the created zero-sequence path still brings overcurrent to the FB-MMC even after its dc-side voltage has been clamped to zero by the thyristor branch. Zero-sequence current cannot be suppressed by a conventional *dq*-frame based control scheme.

To solve the above issue, an additional zero-sequence current control loop acting simultaneously with the thyristor branch is added, as shown in Fig. 6-7. The zero-sequence controller is disabled during normal operations. Detection of a valve-side ground fault enable this controller, and its reference is set to zero to reduce the fault current. As the zero-sequence component exhibits the fundamental frequency, a proportional-resonant (PR) controller is adopted, which can suppress the ac current at a specific frequency more effectively compared to a P or PI controller.

c) System recovery

When both the ac and dc side current are reduced to zero, a non-permanent fault recovery after some time. To discriminate the type of the fault, a small pulse (e.g. 0.1-0.2 p.u of its dc current) is injected to the reference of the zero-sequence controller with a time delay (e.g. 30-50 ms) as shown in Fig. 6-7.

If no zero-sequence current is detected during the pulse injection period, this can be determined that the ac fault has been removed. Under this case, the zero-sequence current will be disabled again, and the FB-MMC will rebuild its ac-side voltage first. After the thyristor branch is turned off, the dc-side of the system can also start to recover.

However, if zero-sequence current still appears during the pulse injection period, the fault will be treated as permanent. The FB-MMC will be blocked and isolated by disconnectors for the grid. The healthy parts of the grid then start their recovery

process. The procedure of the active protection method is summarised in a flow chart as shown in Fig. 6-8.
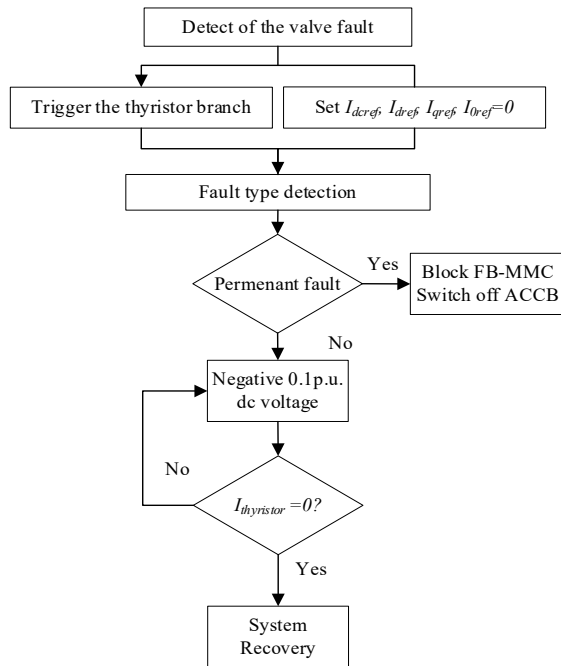
Fig. 6-8. Active protection procedure.

6.5.   Simulations

To verify the analysis and proposed protection strategies, both a point-to-point and a meshed MTDC bipolar systems have been built in PSCAD/EMTDC. The point-to-point system is shown in Fig. 6-9. Since the positive and negative poles in a bipolar system can be controlled independently, which can be seen as an asymmetrical system, simulation results on the positive pole are given as an example in this part.
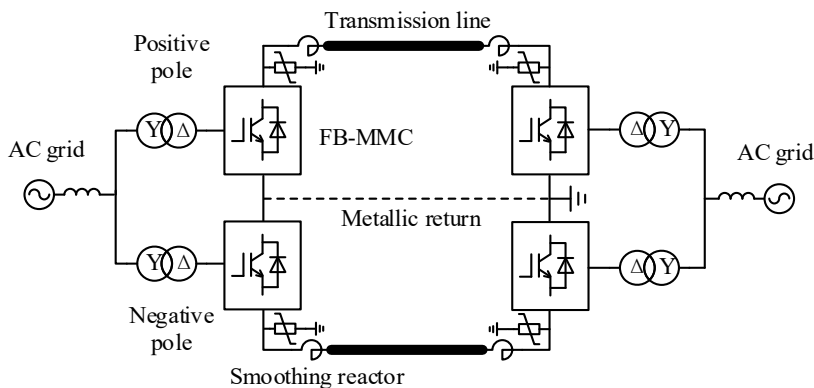
Fig. 6-9. FB-MMC based point-to-point link.

The three-terminal system is illustrated in Fig. 6-10. The parameters of the FB-MMC in each terminal are given in Table 6-2. In this chapter, a valve-side phase-to-ground fault is simulated at phase *a* for all the case studies, and the fault occurs at $t = 1$ s.
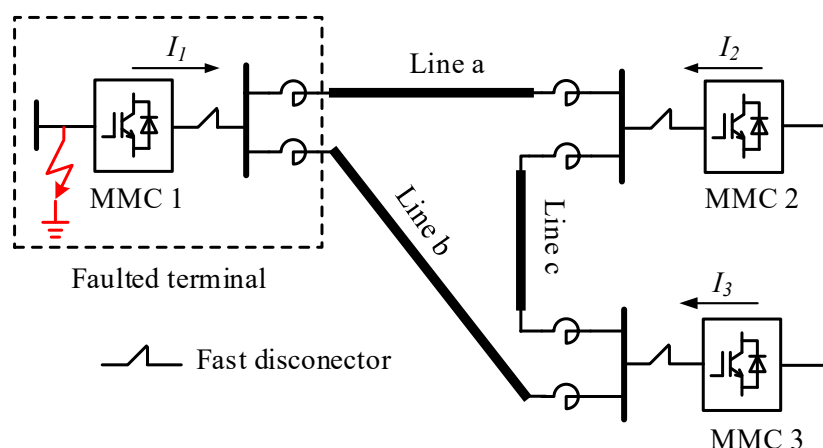
Fig. 6-10. FB-MMC based three-terminal grid (positive pole is shown).

Table 6-2. Parameters of the FB-MMC in each terminal.

Parameter	Value
Rated active power	2×1.5 GW
Rated dc voltage	± 500 kV
RMS ac voltage (line-to-line)	260 kV
Transformer capacity	2×1680 MVA
Transformer leakage inductance	0.15 p.u.
Transformer ratio	500 kV/260 kV
Arm inductance	60 mH
SM Capacitor	18 mF
Number of SMs in each arm	250
DC smoothing inductor	100 mH
Number of thyristors in each branch	350
Thyristor rating/peak surge current[207]	6500V/4250A/64kA
Thyristor I^2t capacity	20.48 MA^{2}s

Notes: The thyristor is selected with a voltage rating of 6500V with 64 kA surge current, which is normally used together with press-pack IGBTs in HB-MMCs to project dc faults. The capacity is enough to protect valve-side ac faults, which will be verified next.

6.5.1. Blocking the FB-MMC only

When the fault is detected, the FB-MMC is blocked after a time delay (e.g. 100 μs) without other protection measures in place. Simulation results are given in Fig. 6-11.
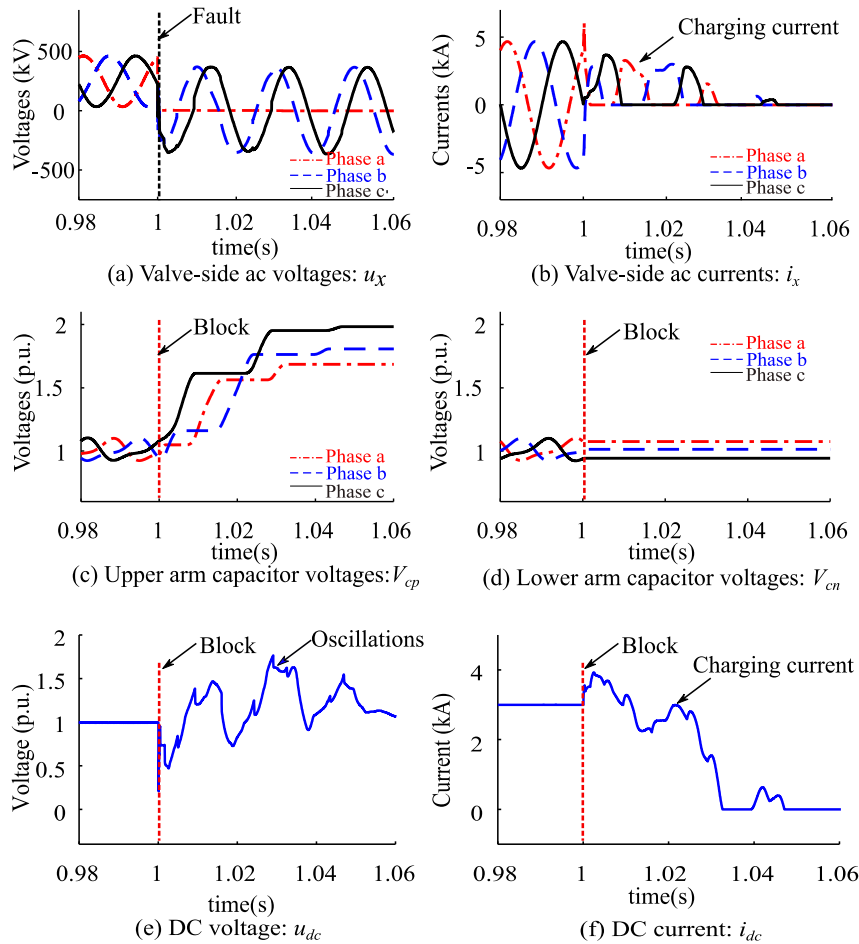
Fig. 6-11. Block the faulted FB-MMC only following the fault.

As it can be seen from Fig. 6-11 (a), following the fault, the phase voltage in the faulted phase becomes zero, and the magnitude of the phase voltage in the healthy phase increase to a line-to-line value without dc offsets. Negative cycles appear due to the exclusion of the dc offset voltage. This has verified the analysis in Section 6.2. Fig. 6-11(c) shows the capacitor voltage of SMs in the upper arms. It can be observed that the capacitors are overcharged, and the maximum voltage reaches around 2 p.u. From this result, it can be concluded that blocking the FB-MMC only under a valve-side ground fault leads to a severe overvoltage. Therefore, additional protection methods are needed.

6.5.2.   Protection from dc-side

a)   Case 1: point-to-point link

Fig. 6-12 shows the simulation results when the dc side protection method is used in the point-to-point link. When the fault is detected, the thyristor branch is triggered, and the FB-MMC is blocked simultaneously. From Fig. 6-12(a), it can be seen that negative cycles still exist in the voltage of the healthy phases. However, there is no overvoltage occurring in the upper arms of the FB-MMC (see Fig. 6-12(c)) as the dc side voltage has been reduced to zero by the thyristor branch (as shown in Fig. 6-12(d)).
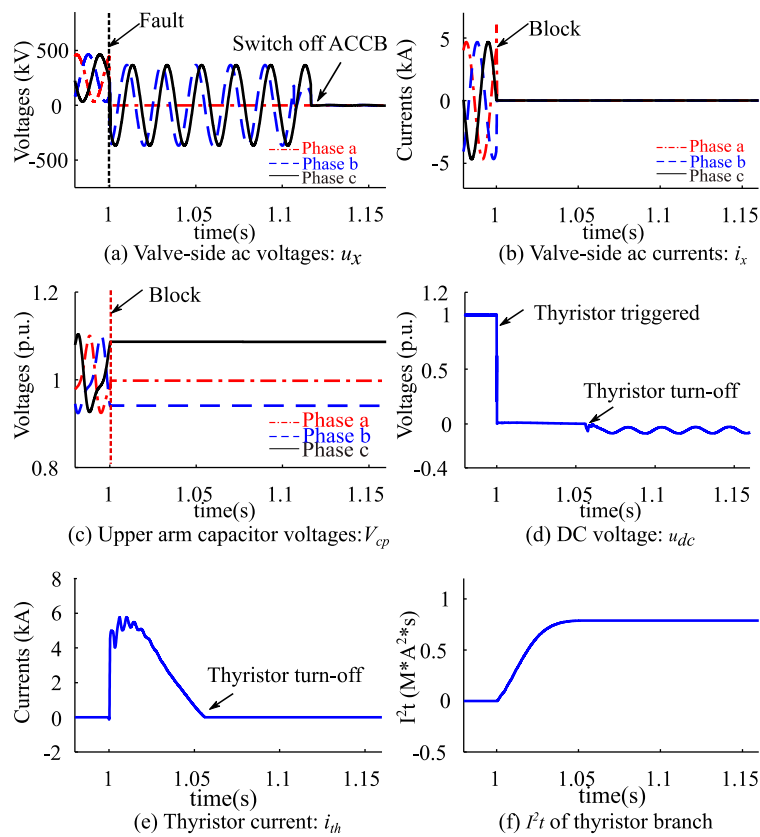
Fig. 6-12. DC side protection method.

The current in the thyristor branch and its I^2t, which represents the thermal capability, are given in Fig. 6-12(e) and (f), respectively. The value of the peak current is around 6 kA, and the I^2t is around 0.8 MA^{2}s. These values are within the SOA of the thyristors [207]. The current in the thyristor branch decays to zero as the FB-MMC in the other terminal regulates its dc current to zero. As it can be seen from Fig. 6-12(a), the ACCB is switched off after 100 ms to isolate the faulted part with the grid. No overvoltage occurs with this method. The FB-MMC is successfully protected.

b) Case 2: MTDC grid

To access the effectiveness of the proposed method and evaluate the influence of the triggering of the thyristor branch to other MMCs within an MTDC system. Simulations have been conducted based on the system, as shown in Fig. 6-10. Before the fault occurs, MMC2 regulates the dc voltage of the system. MMC1 and MMC3 regulate their active power.

A permanent fault occurs at MMC1. As shown in Fig. 6-13(a) and (b), no overcurrent occurs in MMC2 and MMC3 after the triggering of the thyristor branch since FB-MMCs have the capability to ride through dc faults. The dc voltage of the system and dc current of each converter is given in Fig. 6-13(c) and (d), respectively. The dc voltage is reduced to zero quickly by the thyristor branch. As it can be seen from Fig. 6-13(d), the peak value of the dc current for MMC2 is higher than the other two MMCs. This is because MMC2 supervises the system's dc voltage, and its current limit is set higher (5 kA in this study). However, these values remain in the safe operating area.
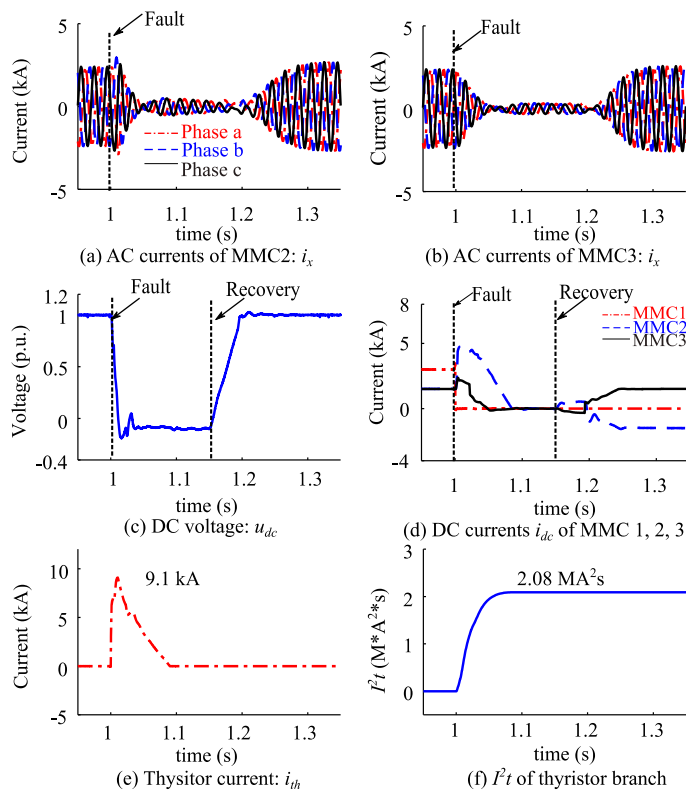
Fig. 6-13. The proposed method in an MTDC grid.

After the faulted FB-MMC is isolated, the healthy part of the grid recovers. As it can be seen in Fig. 6-13(c), the dc voltage begins to rebuild at $t = 1.15$s and is back to normal at $t = 1.2$ s. The active power of MMC2 and MMC3 restores to their pre-fault condition at $t = 1.25$ s. These results verify the effectiveness of the proposed methods in an MTDC grid.

It should be noted that different to a point-to-point link system, the current and I^2t of the thyristor branch is higher as more than one transmission line is injecting current into the thyristor branch in an MTDC grid. Their values are given in Fig. 6-13(e) and (f), which are still within the SOA of the selected thyristor branch.

c) Case 3: Two-and Three-phase faults

Although the possibility of two- and three-phase ground faults at the valve-side is much lower, for completeness, the protection method is evaluated under both two-and three-phase fault conditions.

The waveforms of the ac voltages under two-and three-phase faults are shown in Fig. 6-14. As it is observed, negative cycles occur at the healthy phase during a two-phase ground fault.

(a) Valve-side ac voltages: u_x (b) Valve-side ac voltages: u_x
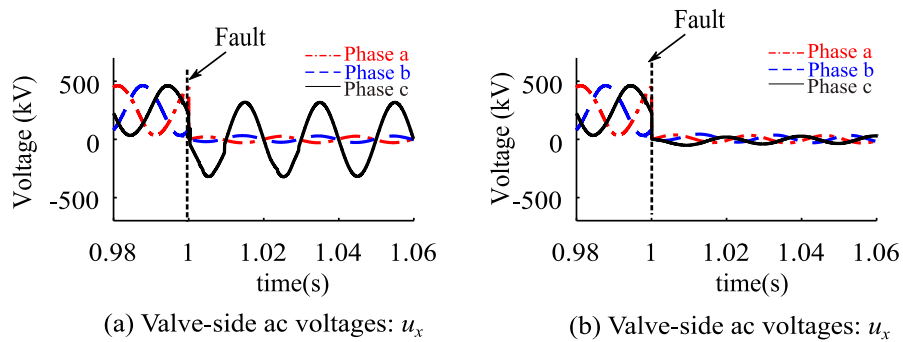
Fig. 6-14. AC side voltage under two- and three-phase fault.

The simulation results with and without the thyristor branch triggered are shown in Fig. 6-15. Similar to a single-phase fault condition, blocking the FB-MMC only leads to a 2 p.u. overvoltage in SMs of the upper arms. The overvoltage in the non-faulted phase is more severe than that of the grounded phases as the presence of negative cycles. However, when the thyristor branch is triggered, the overcurrent is prevented, as shown in Fig. 6-15(b).

(a) Upper arm capacitor voltages: V_{cp} (b) Upper arm capacitor voltages: V_{cp}
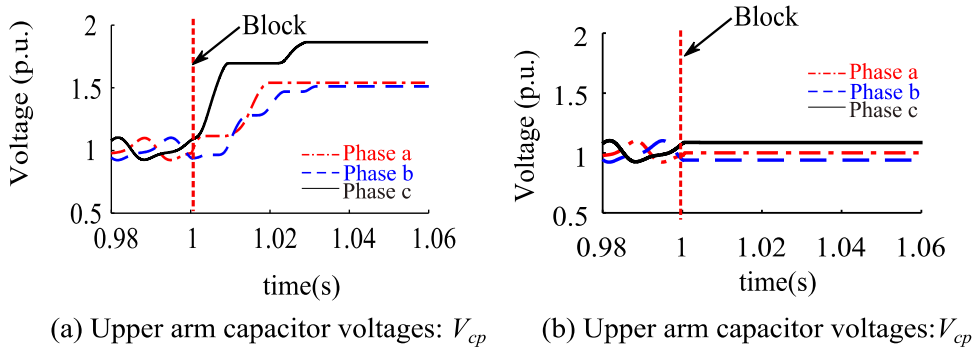
Fig. 6-15. Protection performance against two-phase ground fault.

Following a three-phase fault, the ac voltages in the three phases are all reduced to zero. No negative cycles are present. Therefore, compared to a single-phase or two-phase fault, the level of overvoltage is lower. The transient energy stored in the dc lines (including its smoothing inductors) leads to the overvoltage after the FB-MMC is blocked. It can be seen from Fig. 6-16(a) that, 1.5 p.u. overvoltage is induced by a three-phase fault. Instead, the overvoltage is avoided by the thyristor branch, as shown in Fig. 6-16(b). These results illustrate the effectiveness of the proposed thyristor branch to FB-MMCs against different types of valve-side ground faults.

(a) Upper arm capacitor voltages: V_{cp} (b) Upper arm capacitor voltages: V_{cp}
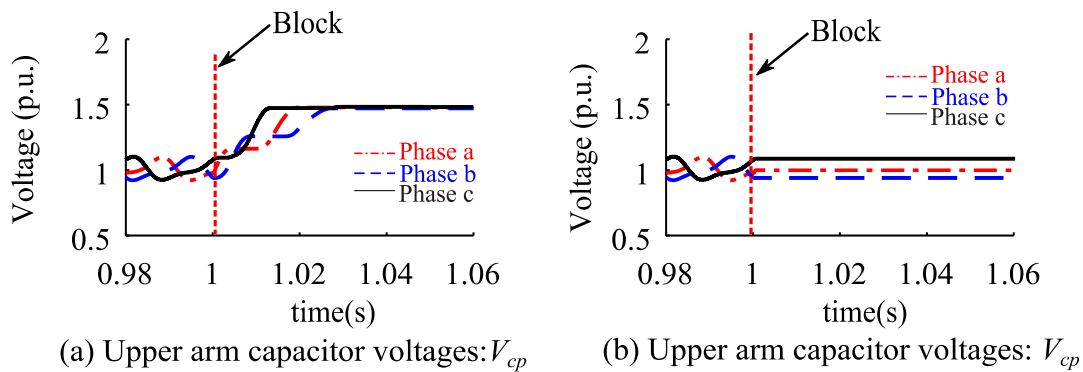
Fig. 6-16. Protection performance against three-phase ground fault.

6.5.3. Protection from ac-side

Fig. 6-17 shows the waveforms when the installed ac-side thyristors are triggered following the fault. Due to three-phase faults caused by the triggered thyristors, negative cycles of the voltages are removed, as shown in Fig. 6-17(b). Therefore, overvoltage of SMs is avoided [see Fig. 6-17(d)]. The grid-side ac currents are given in Fig. 6-17(a). Since the double thyristors provide a symmetrical path for the ac

current, zero crossings exist, which can ensure the operation of ACCBs, the fault can be isolated by the ACCBs. The analysis in Section 6.3.2 is verified.

(a) Grid-side ac currents

(b) Valve-side ac voltages

(c) DC voltage

(d) Upper arm SM voltages
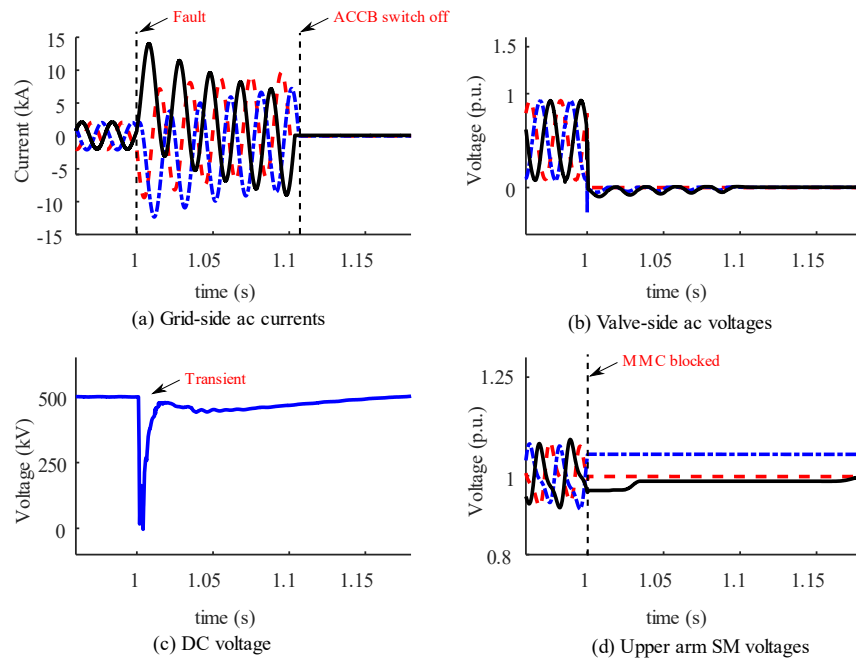
Fig. 6-17. Trigger ac-side thyristors following the fault.

6.5.4. Protection of transient fault

The simulation results with the active-based protection method are given in Fig. 6-18. The faulted FB-MMC is kept active other than being blocked after the thyristor branch is triggered.

The valve-side ac voltage is shown in Fig. 6-18(a), which is the same as Fig. 6-12(a). Thanks to the current control loops, the ac side current is regulated to zero after the fault, as shown in Fig. 6-18(b). No overcurrent appears in the arms of the FB-MMC. This can be seen in Fig. 6-18(g) and (h). As the dc voltage is clamped to zero (see Fig. 6-18(d)) by the triggered thyristor branch, no overvoltage occurs in SMs of the upper arms. Through these results, it can be seen that the active-based method can effectively protect the FB-MMC under a valve side single phase to ground fault condition.
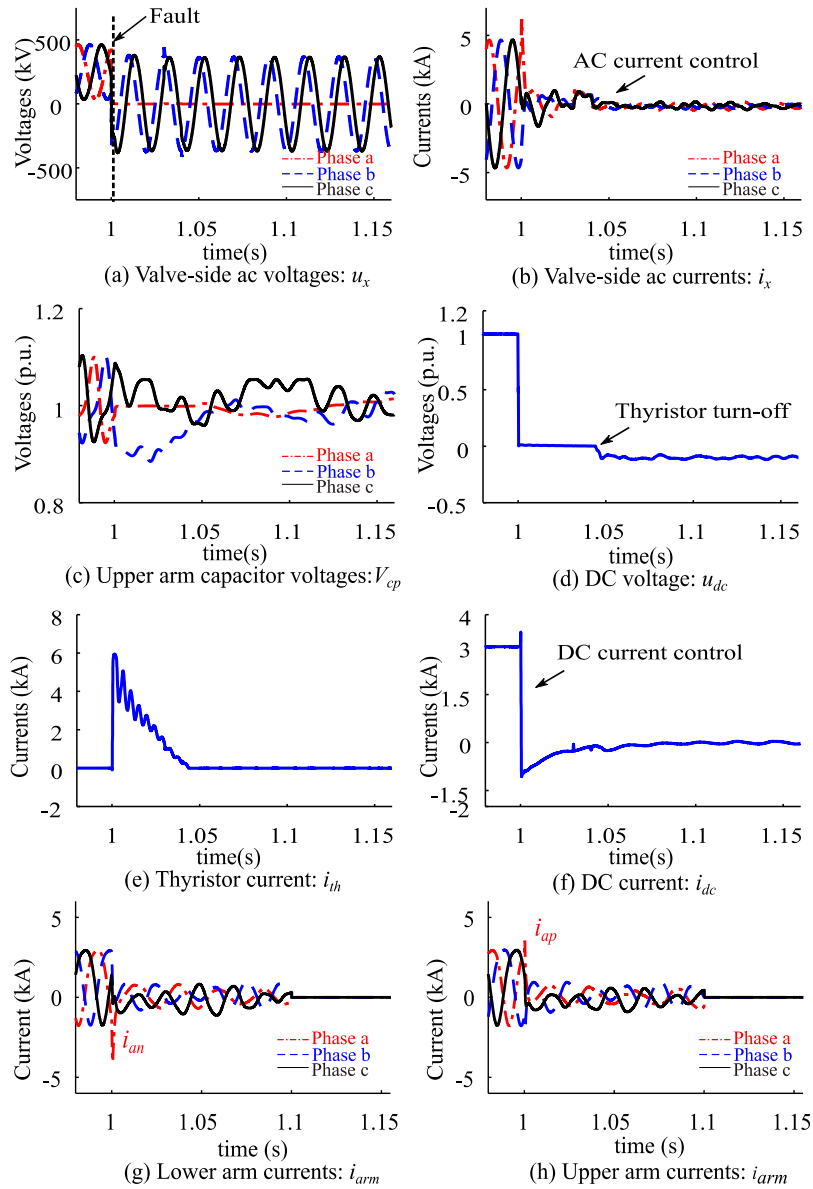
Fig. 6-18. Active based protection method.

a) Case 1: Permanent fault

As analysed in Section 6.4, the FB-MMC can help to discriminate the types of fault by injecting zero-sequence components into its control reference. Simulations are carried out by injecting a 10 ms pulse to its reference of the zero-sequence controller (30 ms delay after the fault detection).

Fig. 6-19 shows the results that a permanent fault is deemed as a zero-sequence current is still detected when the pulse is injected, as shown in Fig. 6-19(a). Under such a case, the FB-MMC will be blocked next, and its ACCB is then switched off to isolate the faulted FB-MMC.

(a) Zero-sequence current: i_0 (b) AC voltages: u_x
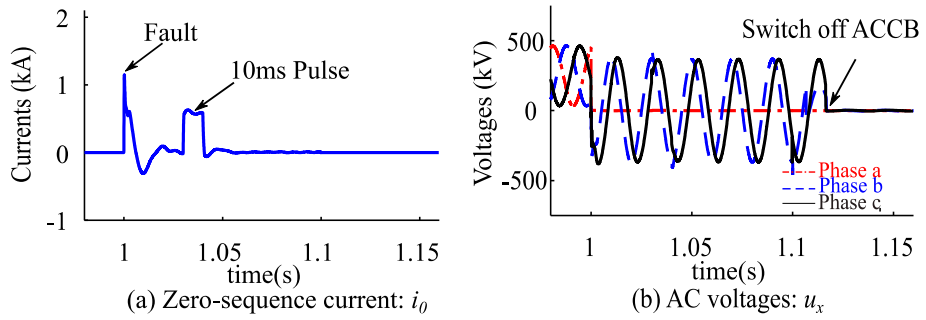
Fig. 6-19. Protection of a permanent fault.

b) Case 2: Non-permanent fault

When there is no zero-sequence current detected during the pulse injecting period, as shown in Fig. 6-20(a), this indicates that the fault is cleared. The FB-MMC then rebuilds its ac voltage by disabling its zero-sequence controller. The dc voltage can be restored within 50 ms, as shown in Fig. 6-20(b). Due to its fast recovery process, this method is suitable for the system, where non-permanent faults occur frequently.

(a) Zero-sequence current: i_0 (b) AC voltages u_x and DC voltages u_{dc}
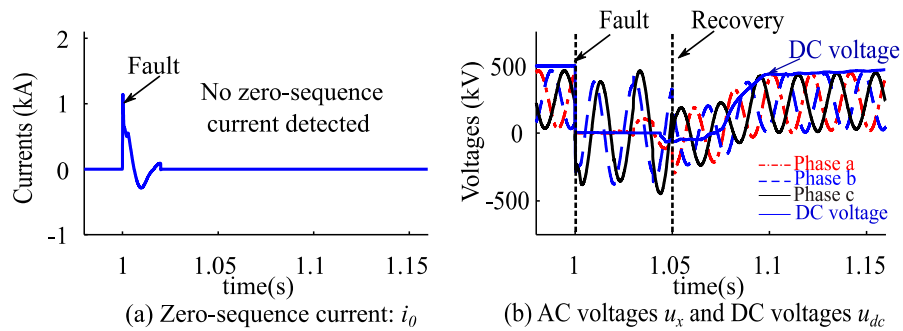
Fig. 6-20. Protection of a non-permanent fault.

6.6.   Summary

In this chapter, the behaviour of valve-side single-phase ground faults for FB-MMC based bipolar HVDC systems have been analysed. It is revealed that without proper protection methods in place, a valve-side single-phase ground fault brings severe overvoltage (around 2 p.u.) to the FB-SMs.

To solve this issue, thyristor-based methods have been proposed. The thyristors are proposed to install at the dc- or ac-sides of FB MMCs to prevent overvoltage. The characteristic of these two methods has been compared and summarised.

When installed at the dc-side, the thyristors are triggered to reduce the dc voltage following the fault. In this way, the overcharging of SMs in the upper arms is avoided.

For the dc side protection method, an active method is proposed. Additional flexibility is provided by the active protection method as it identifies whether the fault is permanent or not. This is achieved by injecting a small pulse to the zero-sequence current reference. In the case of a non-permanent fault, once it disappears, the FB-MMC can rebuild its output voltages quickly. Such a method is recommended to be adopted in systems that are vulnerable to non-permanent faults and sensitive to the interruption time of power transmission.

When installed at the ac-side, the thyristors are triggered to remove the negative cycles of the ac voltages. This can also effectively prevent the overcharging of SMs following the fault. This method does not create a dc fault during the fault handling process, which minimises the fault influence on its connected dc grid. Therefore, it is recommended to be used in systems that are sensitive to dc faults.

For completeness, the effectiveness of the proposed two methods has been verified by simulations conducted in PSCAD/EMTDC.

Chapter 7   Conclusions and future work

7.1.   Conclusion

VSC based HVDC systems have shown great potential and advantages over LCC HVDC systems for integrations of renewable power. Plenty of VSC HVDC projects have been built or are under constructing all around the world. Most of the existing HVDC systems are point-to-point links at the current stage. To further improve the flexibility and reliability, there are trends to connect the existing HVDC links to build MTDC grids. However, current flow controls and fault protection remain challenges on the ways to build MTDC grids. To mitigate these issues, the operation and protection of VSC HVDC grids were investigated in this thesis.

7.1.1.   Current flow controllers for MTDC grids

Within a meshed MTDC grid, parallel dc current paths may exist. The current flows within the network are not fully controlled. Under some operating conditions, one conductor may reach its thermal limit, whereas other paths may not be fully used. Current flow controllers need to be installed to operate a meshed MTDC grid with high efficiency and flexibility.

In Chapter 3, the necessity of including CFCs for a meshed MTDC grid was analysed. By comparing different schemes of CFCs, it has been revealed that HB-CFCs are promising topologies due to their simple structures and low costs. To better elaborate on the operation characteristics of the HB-CFC, four operating modes of the HB-CFC were classified in this study. Based on the clarified operating modes, a level shift modulation method has been proposed. By the proposed modulation method, only one bridge of the HB-CFC is regulated by PWM signals at a time. This contributes to reducing its switching losses compared to the dual PWM modulation methods of which two PWM signals are used. Another significant benefit obtained from it is the possibility of current regulation irrespective of the direction of the current at interfacing transmission lines. This simplifies the overall control strategy of the device.

To clearly give guidance to the controller design for HB-CFCs, small-signal modelling has been conducted. It has been found that the structures of transfer functions of the HB-CFC, under the current sharing and the current reversal modes, are different. An RHP ZERO exists in the small-signal models for the current reversal mode, which exhibit a non-minimum phase system behaviour. This leads to an extra 90-degree phase lag in the frequency response of the system. A dual-loop control together with the level-shift modulation has been proposed to mitigate the influence of the RHP ZERO. The analysis of the HB-CFCs and the proposed control methods have been verified by simulation results in PSCAD/EMTDC. This study contributes to providing reference on the operation of MTDC grids with balanced current flows among transmission lines.

7.1.2. DC protection device with current flow control capability

Installation of dc circuit breakers and current flow controllers will be required to quickly isolate faults and fully control current flows in a dc grid. However, the capital costs of a dc grid may increase significantly by including such devices.

In Chapter 4, a new device, the CB/CFC, integrating functions of both HCBs and HB-CFCs, is proposed. This integrated device can significantly reduce the number of semiconductors deployed while the same functions remain as separate schemes. Under normal conditions, this device operates as an HB-CFC to regulate current flows. When a dc fault is detected, it serves as an HCB to cope with dc faults.

Simulations have been conducted in Chapter 4 based on an MTDC grid to verify the function of the CB/CFC. The CB/CFC was installed in one of the terminals of the MTDC grid. When operated as an HB-CFC, the level-shift modulation method proposed in Chapter 3 was deployed. It has been revealed that the proposed CB/CFC is capable of both isolating dc faults and regulating current flow in a meshed MTDC grid.

To show the advantages of the CB/CFC regarding the semiconductor component, a comparison was made with two other alternatives available in the open literature. Given the reduction in the number of IGBTs for a CB/CFC, the presented device

represents a good option to achieve current flow regulation and dc fault protection by an integrated device in an MTDC grid.

7.1.3.   Protection of valve-side ac faults

The occurrence of valve-side ac faults in VSC HVDC systems brings severe consequences to VSCs. As the distance of the fault to VSCs is short and the isolation function of the interface transformer does not exist under such faults, the transients seen by converters are much more severe compared to those caused by grid-side ac faults. Without proper protection methods in place, the large inrush current and overvoltage caused by such faults may damage the power-electronic based converter and, thus, endanger the operation of HVDC systems.

In Chapter 5 and Chapter 6, the characteristics of valve-side ac faults have been analysed. It has been found that such faults will induce a large inrush fault current in a bipolar system due to the lower impedance grounding at the dc side. For HB-MMC based systems, the fault current contains large dc offsets, and zero-crossings may not appear for grid-side ac currents. This may lead to mis-operations of grid-side ACCB, and the fault cannot be isolated timely by ACCBs. This brings risks of overheating (damaging) for the diodes in the lower arms of HB-MMCs. For FB-MMC based bipolar systems, around 2 p.u. overvoltage may be caused in the SMs of upper arms once a single-phase-to-ground fault occurs.

To address the issues discussed above, protection methods were proposed in Chapter 5 and Chapter 6 for both HB and FB-MMCs, respectively. Thyristors were used as protective devices due to their lower costs and higher current capacity.

For HB-MMCs, the thyristors can be either installed in SMs or at the ac-side to mitigate the problem of the non-zero crossing. ACCBs can isolate such faults when zero-crossings appear after the thyristors are switched on. Installing thyristors at the ac-side provides a potential for compact SM design and reduction of the number of thyristors.

For FB-MMCs, the thyristors can be either installed at the ac-or dc-side to solve the overvoltage issue. When installed at the ac-side, the protection process (triggering the thyristors) induces little influence on the dc side operations of MTDC grids.

Therefore, this method is suitable for dc grids, of which hybrid HB and FB MMCs exist. When installed at the dc-side, the triggering of thyristors brings a transient short circuit at the dc-side. This scheme is more suitable for FB-MMC systems as they have the capability to ride through dc fault. The advantage of the dc-side protection method is that the number of thyristors is significantly reduced, and little influence is induced to the nearby ac grid following a valve-side single-phase fault. The characteristic of the two proposed protection methods has been summarised in Chapter 6. It needs to be considered according to the requirements of the real application when selecting schemes between these two methods.

The performance of the proposed methods against valve-side ac faults has been verified by simulations conducted in PSCAD/EMTDC. The analyses and proposed methods in Chapters 5 and 6 provide valuable references for designing protection systems against valve-side ac faults in MMC based HVDC systems.

7.2. Future work

The future work is listed below:

7.2.1. HB-CFCs

In Chapter 3, the proposed level-shift modulation method aims to control the HB-CFCs with three ports (i.e. three lines are connected with the HB-CFC). In the future, with the development of MTDC grids, the complexity of connections within an MTDC grid will increase. Multi-ports HB-CFC may be needed. Therefore, modulation and control methods for HB-CFCs with more than three ports are needed. Therefore, future work should consider investigating control and modelling methods for multi-port HB-CFCs. At the same time, system-level power dispatching and current flow control aspects should be investigated for MTDC grids in the future.

7.2.2. DC circuit breakers

The research in this thesis was mostly focusing on VSC HVDC systems built up with MMCs. With the development of power electronics and renewable generations in recent years, MVDC and LVDC systems are being discussed widely. As the impedances and structures of HVDC, MVDC and LVDC systems are different, the

requirement for dc fault isolations may also be different. Therefore, future work should consider investigating dc protections for MVDC and LVDC networks. Moreover, with the development of materials, new power electronic devices, such as SiC-and GaN-based devices, have been more and more used to replace Si devices. The design of DCCBs should also consider the new power electronics devices in future work.

7.2.3.   Valve-side ac faults

The valve-side faults in bipolar MMC based HVDC systems have been analysed in detail in Chapter 5 and Chapter 6. Protection methods were proposed for both HB and FB MMCs. At the current stage, the research in the thesis did not cover the MVDC and LVDC systems. As power electronics converters are more and more widely used in MVDC and LVDC networks, they are also facing risks upon valve-side ac faults. Since the topologies of converters in MVDC and LVDC systems are different from HVDC systems, the fault behaviour and consequences may also be different. Therefore, it is worth conducting analyses on valve-side ac faults for MVDC and LVDC systems s with related protection methods proposed. Low-cost mechanical switches may be investigated for protecting such faults.

References

[1] Achieving net-zero carbon emissions through a whole system approach: CST letter. [Online]. Available: https://www.gov.uk/government/publications/achieving-net-zero-carbon-emissions-through-a-whole-systems-approach.

[2] EU 2050 long-term strategy. [Online]. Available: https://ec.europa.eu/clima/policies/strategies/2050_en.

[3] Roadmap of 3060 carbon neutrality target. http://www.gov.cn/xinwen/2021-03/16/content_5593348.htm.

[4] Renewable energy directive. European Commission. [Online]. Available: https://ec.europa.eu/energy/topics/renewable-energy/renewable-energy-directive/overview_en.

[5] Guidance document on wind energy developments and EU nature legislation. [Online]. Available: https://ec.europa.eu/energy/topics/renewable-energy/onshore-and-offshore-wind_en#wind-power.

[6] Wind energy in Europe 2020 Statistics and the outlook for 2021-2025. [Online]. Available: https://windeurope.org/intelligence-platform/product/wind-energy-in-europe-in-2020-trends-and-statistics/.

[7] Offshore wind Sector Deal-one year on. [Online]. Available: https://www.gov.uk/government/publications/offshore-wind-sector-deal/offshore-wind-sector-deal-one-year-on

[8] This turbine will power the world's largest offshore wind farm. [Online]. Available: https://www.ge.com/news/reports/turbine-will-power-worlds-largest-offshore-wind-farm

[9] China's MingYang presents a 16 MW offshore wind giant. [Online]. Available: https://renewablesnow.com/news/chinas-mingyang-presents-16-mw-offshore-wind-giant-751821/

[10] Wind turbines: the bigger, the better. [Online]. Available: https://www.energy.gov/eere/articles/wind-turbines-bigger-better.

[11] The world's largest offshore wind farm-Hornsea Project one. [Online]. Available. https://hornseaprojectone.co.uk/about-the-project#project-timeline-2020

[12] Hornsea two-powering well over 1.3 million homes with green electricity. [Online]. Available: https://hornseaprojects.co.uk/hornsea-project-two.

[13] Offshore wind-limitless supply, limitless opportunity. [Online]. Available: https://orsted.co.uk/energy-solutions/offshore-

wind#:~:text=The%20UK%20is%20the%20world%20leader%20in%20offsho
re,a%20third%20of%20its%20electricity%20from%20offshore%20wind.

[14] Why the EU supports solar energy research and innovation. [Online]. Available:
https://ec.europa.eu/info/research-and-innovation/research-area/energy-
research-and-innovation/solar-energy_en

[15] M. Barnes, D. Van Hertem, S. P. Teeuwsen and M. Callavik, "HVDC Systems
in Smart Grids," *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2082-2098, Nov.
2017.

[16] ABB retraces its pioneering technology roots to upgrade the world's first HVDC
link. [Online]. Available: https://new.abb.com/news/detail/46097/abb-retraces-
its-pioneering-technology-roots-to-upgrade-worlds-first-hvdc-link.

[17] R. Marquardt, "Modular Multilevel Converters: State of the Art and Future
Progress," *IEEE Power Electronics Magazine*, vol. 5, no. 4, pp. 24-31, Dec.
2018.

[18] J. Lin, "Integrating the First HVDC-Based Offshore Wind Power into PJM
System—A Real Project Case Study," *IEEE Transactions on Industry
Applications*, vol. 52, no. 3, pp. 1970-1978, May-June 2016.

[19] BorWin1 project-First German DC connection to a wind farm at sea. [Online].
Available: https://www.tennet.eu/our-grid/offshore-projects-germany/borwin1/

[20] Improve grid performance with flexible HVDC technology. [Online]. Available:
https://www.siemens-energy.com/global/en/offerings/power-
transmission/portfolio/high-voltage-direct-current-transmission-
solutions/hvdc-plus.html

[21] East West Interconnector. [Online]. Available:
https://www.hitachienergy.com/case-studies/east-west-interconnector

[22] Interconnected to the heart of Europe's electricity market. [Online]. Available:
https://www.nemolink.co.uk/.

[23] Siemens energy. We connect Europe-Nemo link supplies electricity across
borders. [Online]. Available: https://www.siemens-
energy.com/global/en/news/magazine/2020/intereuropean-hvdc-link-
nemolink.html.

[24] IFA2: Connecting Britain to Cleaner Energy. [Online]. Available:
https://www.nationalgrid.com/ifa2-interconnector/connecting-britain-to-clean-
energy?utm_source=wickipedia&utm_medium=ExternalLinks&utm_campaig
n=IFA2.

[25] North Sea Link. [Online]. Available: https://www.northsealink.com/.

[26] The ElecLink Project. [Online]. Available:
https://www.eleclink.co.uk/index.php.

[27] Viking Link. [Online]. Available: https://viking-link.com/.

[28] France-Alderney-Britain project. [Online]. Available: https://www.fablink.net/.

[29] Programmer 2030. [Online]. Available: https://www.tennet.eu/our-grid/offshore-grid-netherlands/programme-2030/.

[30] The 2 GW program. [Online]. Available: https://www.tennet.eu/our-grid/offshore-outlook-2050/the-2gw-program/.

[31] Nanhui Wind Farm Integration. [Online]. Available: https://web.archive.org/web/20130702053357/http://www.epri.sgcc.com.cn/prgc/english/Company_Capability/201203/t20120307_1038855.html.

[32] Dalian City Infeed. [Online]. Available: https://web.archive.org/web/20130702045929/http://www.epri.sgcc.com.cn/prgc/english/Company_Capability/201203/t20120307_1038854.html.

[33] RXPE commissions the world's first VSV multi-terminal HVDC project. [Online]. Available: https://www.rxhk.co.uk/corporate/news/rxpe-commissions-worlds-first-vsc-multi-terminal-hvdc-project/.

[34] VSC-HVDC Project with the World's Highest Voltage and Transmission Capacity Completed and Put into Operation World's First five-terminal VSC-HVDC links. [Online] Available: https://nrec.com/en/web/upload/2019/05/13/15577090771736sc3av.pdf.

[35] http://eng.csg.cn/Press_release/News_2016/201609/t20160905_142899.html

[36] Yu'E Back to Back HVDC Converter Commissioned. [Online]. Available: https://www.rxhk.co.uk/corporate/news/yue-hvdc-commissioning-complete/.

[37] Xiamen Mainland – Xiamen Island HVDC Line, China. [Online]. Available: https://www.power-technology.com/marketdata/xiamen-mainland-xiamen-island-hvdc-line-china/

[38] A hybrid LCC/VSC HVDC System is being proved. [Online]. Available: https://www.cigre.org/article/GB/hybrid-lccvsc-hvdc-system-is-being-proved

[39] World's Largest Offshore Converter Station Successfully Installed. [Online]. Available: https://www.world-energy.org/article/19104.html

[40] Rudong Offshore Wind Power HVDC. [Online]. Available: https://www.rxhk.co.uk/corporate/news/rudong-offshore-wind-power-hvdc/.

[41] D. Van Hertem, O. Gomis-Bellmunt, and J. Liang, *HVDC Grids: For Offshore and Supergrid of the Future*, Wiley-IEEE Press, April 2016.

[42] Shetland project overview. [Online]. Available：https://www.ssen-transmission.co.uk/projects/shetland.

[43] Caithness-Moray link. [Online]. Available: https://www.ssen-transmission.co.uk/projects/caithness-moray/.

[44] Shetland HVDC project. [Online]. Available: https://www.hitachienergy.com/references/hvdc/shetland.

[45] H. Rao, "Architecture of Nan'ao multi-terminal VSC-HVDC system and its multi-functional control," *CSEE Journal of Power and Energy Systems*, vol. 1, no. 1, pp. 9-18, March 2015.

[46] G. Tang, Z. He, H. Pang, X. Huang and X. Zhang, "Basic topology and key devices of the five-terminal DC grid," *CSEE Journal of Power and Energy Systems*, vol. 1, no. 2, pp. 22-35, June 2015.

[47] Operation of the Zhangbei flexible DC grid. [Online]. Available: http://he.people.com.cn/n2/2020/0629/c192235-34119354.html.

[48] Commission of the Zhangbei MTDC grid. [Online]. Available: http://www.sasac.gov.cn/n4470048/n13461446/n15412215/n15441968/c15442620/content.html.

[49] Zhangbei VSC-HVDC Power Transmission project. [Online]. Available: https://www.nsenergybusiness.com/projects/zhangbei-vsc-hvdc-power-transmission-project/.

[50] The world's first DC grid with HVDC light technology. [Online]. Available: https://www.hitachiabb-powergrids.com/references/hvdc/zhangbei.

[51] Z. Lin, J. Qin, H. Ma, J. Liu, B. Yang and Y. Wang, "Design of 500kV Hybrid HVDC Circuit Breaker Control and Protection System," *2020 4th International Conference on HVDC (HVDC)*, 2020, pp. 134-139.

[52] H. Pang and X. Wei, "Research on Key Technology and Equipment for Zhangbei 500kV DC Grid," *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, 2018, pp. 2343-2351.

[53] NR's VSC-HVDC solution. [Online]. Available: https://www.nrec.com/en/web/upload/2019/05/13/155770883678038egom.pdf

[54] Y. Wang and R. Marquardt, "Future HVDC-grids employing modular multilevel converters and hybrid DC-breakers," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Sep. 2013, pp. 1–8.

[55] D. Jovcic, M. Taherbaneh, J. Taisne and S. Nguefeu, "Offshore DC Grids as an Interconnection of Radial Systems: Protection and Control Aspects," *IEEE Transactions on Smart Grid*, vol. 6, no. 2, pp. 903-910, March 2015.

[56] O. Cwikowski, A. Wood, A. Miller, M. Barnes and R. Shuttleworth, "Operating DC Circuit Breakers With MMC," *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 260-270, Feb. 2018.

[57] B. Geebelen, W. Leterme and D. V. Hertem, "Analysis of DC breaker requirements for different HVDC grid protection schemes," *11th IET International Conference on AC and DC Power Transmission*, 2015, pp. 1-7.

[58] J. H¨afner and B. Jacobson, "Proactive hybrid HVDC breakers—A key innovation for reliable HVDC grid," *in Proc. CIGRÉ Symp.*, Bologna, Italy, paper 264, Sep. 13–15, 2011.

[59] W. Zhou et al., "Development and test of a 200kV full-bridge based hybrid HVDC breaker," *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015, pp. 1-7.

[60] X. Li, L. Guo, C. Hong, Y. Zhang, Y. W. Li and C. Wang, "Hierarchical Control of Multiterminal DC Grids for Large-Scale Renewable Energy Integration,"

IEEE Transactions on Sustainable Energy, vol. 9, no. 3, pp. 1448-1457, July 2018.

[61] K. Rouzbehi, A. Miranian, A. Luna and P. Rodriguez, "Towards fully controllable multi-terminal DC grids using flexible DC transmission systems," in *IEEE Energy Conversion Congress and Exposition (ECCE),* 2014, pp. 1-5.

[62] Q. Mu, J. Liang, Y. Li and X. Zhou, "Power flow control devices in DC grids," in *Power and Energy Society General Meeting*, 2012, pp.1-7.

[63] E. Veilleux and B. Ooi, "Power flow analysis in multi-terminal HVDC grid," *in Power Systems Conf. and Expo. (PSCE)*, pp. 1-7, 2011.

[64] E. Veilleux and B. T. Ooi, "Multiterminal HVDC with Thyristor Power-Flow Controller," *IEEE Trans. Pow. Del*., vol. 27, no. 3, pp. 1205-1212, 2012.

[65] J. Sau-Bassols, E. Prieto-Araujo and O. Gomis-Bellmunt, "Modelling and control of an interline Current Flow Controller for meshed HVDC grids," *IEEE Trans. Power Del.*, vol. 32, issue 1, pp. 11-22, Feb. 2017.

[66] S. Cui, H. Lee, J. Jung, Y. Lee and S. Sul, "A Comprehensive AC-Side Single-Line-to-Ground Fault Ride Through Strategy of an MMC-Based HVDC System," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 6, no. 3, pp. 1021-1031, Sept. 2018.

[67] A. Moawwad, M. S. El Moursi and W. Xiao, "Advanced Fault Ride-Through Management Scheme for VSC-HVDC Connecting Offshore Wind Farms," *IEEE Transactions on Power Systems*, vol. 31, no. 6, pp. 4923-4934, Nov. 2016.

[68] National Grid, "*The Grid Code*", Issue 5 revision 36, 12 July 2019.

[69] R. Teixeira Pinto, S. F. Rodrigues, P. Bauer and J. Pierik, "Grid code compliance of VSC-HVDC in offshore multi-terminal DC networks," *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics* Society, Vienna, 2013, pp. 2057-2062.

[70] O. A. Giddani, G. P. Adam, O. Anaya-Lara, G. Burt and K. L. Lo, "Control strategies of VSC-HVDC transmission system for wind power integration to meet GB grid code requirements," *SPEEDAM 2010, Pisa*, 2010, pp. 385-390.

[71] M. Ndreko, A. Bucurenciu, M. Popov and M. A. M. M. van der Meijden, "On grid code compliance of offshore mtdc grids: modeling and analysis," *2015 IEEE Eindhoven PowerTech*, Eindhoven, 2015, pp. 1-6.

[72] Kunliulong DC Project has been placed into operation. [Online]. Available: http://eng.csg.cn/Press_release/News_2021/202101/t20210105_316697.html.

[73] Kunliulong UHV hybrid multi-terminal HVDC transmission project was successfully put into operation. [Online]. Available: https://www.nrec.com/en/index.php/about/newsInfo/83.html.

[74] Bin Wu; Mehdi Narimani, "Control of Induction Motor Drives," *High-Power Converters and AC Drives*, 2017, pp.321-352.

[75] Mahinda Vilathgamuwa; Dulika Nayanasiri; Shantha Gamini, *Power Electronics for Photovoltaic Power Systems*, Morgan & Claypool, 2015.

[76] Evolution of HVDC light. [Online]. Available: https://new.abb.com/news/detail/4224/evolution-of-hvdc-lightr

[77] B. R. Andersen, L. Xu and K. T. G. Wong, "Topologies for VSC transmission," *Seventh International Conference on AC-DC Power Transmission*, 2001, pp. 298-304.

[78] A. Nabae, I. Takahashi and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518-523, Sept. 1981.

[79] J. Rodriguez, S. Bernet, P. K. Steimer and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2219-2230, July 2010.

[80] R. Sommer, A. Mertens, C. Brunotte and G. Trauth, "Medium voltage drive system with NPC three-level inverter using IGBTs," IEE Seminar PWM Medium Voltage Drives (Ref. No. 2000/063), 2000, pp. 3/1-3/5.

[81] R. Sommer, A. Mertens, M. Griggs, H. -. Conraths, M. Bruckmann and T. Greif, "New medium voltage drive systems using three-level neutral point clamped inverter with high voltage IGBT," *Conference Record of the 1999 IEEE Industry Applications Conference. Thirty-Forth IAS Annual Meeting* (Cat. No.99CH36370), 1999, pp. 1513-1519 vol.3.

[82] A. Petersson and A. Edris, "Dynamic performance of the Eagle Pass back-to-back HVDC Light tie," *Seventh International Conference on AC-DC Power Transmission*, 2001, pp. 220-225.

[83] O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez and R. Teodorescu, "Power Capability Investigation Based on Electrothermal Models of Press-Pack IGBT Three-Level NPC and ANPC VSCs for Multimegawatt Wind Turbines," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3195-3206, July 2012.

[84] Y. Jiao, F. C. Lee and S. Lu, "Space Vector Modulation for Three-Level NPC Converter With Neutral Point Voltage Balance and Switching Loss Reduction," *IEEE Transactions on Power Electronics,* vol. 29, no. 10, pp. 5579-5591, Oct. 2014.

[85] T. Bruckner, S. Bernet and H. Guldner, "The active NPC converter and its loss-balancing control," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 855-868, June 2005.

[86] T. Bruckner and S. Bemet, "Loss balancing in three-level voltage source inverters applying active NPC switches," *2001 IEEE 32nd Annual Power Electronics Specialists Conference*, 2001, pp. 1135-1140 vol.2.

[87] N. Flourentzou, V. G. Agelidis and G. D. Demetriades, "VSC-Based HVDC Power Transmission Systems: An Overview," *IEEE Transactions on Power Electronics,* vol. 24, no. 3, pp. 592-602, March 2009.

[88] The world's longest underground power transmission system. [Online]. Available: https://www.hitachiabb-powergrids.com/references/hvdc/murraylink.

[89] Cross Sound Cable. [Online]. Available: http://www.crosssoundcable.com/.

[90] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," *IEEE Bologna Power Tech Conference Proceedings*, pp. 6 pp. Vol.3, 2003.

[91] Trans Bay Cable Project. [Online]. Available: https://www.transbaycable.com/

[92] S. P. Teeuwsen, "Modeling the Trans Bay Cable Project as Voltage-Sourced Converter with Modular Multilevel Converter design," *2011 IEEE Power and Energy Society General Meeting*, 2011, pp. 1-8.

[93] Q. Tu, Z. Xu and L. Xu, "Reduced Switching-Frequency Modulation and Circulating Current Suppression for Modular Multilevel Converters," *IEEE Transactions on Power Delivery*, vol. 26, no. 3, pp. 2009-2017, July 2011.

[94] Q. Tu and Z. Xu, "Power losses evaluation for modular multilevel converter with junction temperature feedback," in *2011 IEEE Power and Energy Society General Meeting*, 2011, pp. 1-7.

[95] A. Dekka, B. Wu, N. R. Zargari and R. L. Fuentes, "Dynamic Voltage Balancing Algorithm for Modular Multilevel Converter: A Unique Solution," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 952-963, Feb. 2016.

[96] R. Marquardt, "Modular multilevel converter: a universal concept for HVDC-networks and extended dc-bus-applications," in *Proc. Int. Power Electron. Conf.*, 2010, pp. 502–507.

[97] H. Iman-Eini and M. Liserre, "DC Fault Current Blocking With the Coordination of Half-Bridge MMC and the Hybrid DC Breaker," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 7, pp. 5503-5514, July 2020.

[98] D. Jovcic, W. Lin, S. Nguefeu and H. Saad, "Full bridge MMC converter controller for HVDC operation in normal and DC fault conditions," in *International Symposium on Power Electronics*, Novi Sad, 2017, pp. 1-6.

[99] W. Lin, D. Jovcic, S. Nguefeu and H. Saad, "Full-Bridge MMC Converter Optimal Design to HVDC Operational Requirements," *IEEE Transactions on Power Delivery*, vol. 31, no. 3, pp. 1342-1350, June 2016.

[100] R. Li, L. Xu, L. Yu and L. Yao, "A Hybrid Modular Multilevel Converter With Reduced Full-Bridge Submodules," *IEEE Transactions on Power Delivery*, vol. 35, no. 4, pp. 1876-1885, Aug. 2020.

[101] S. Wenig, M. Goertz, M. Suriyah and T. Leibfried, "Active DC fault management of a bipolar full-bridge MMC-HVDC scheme with metallic return," *2016 IEEE International Energy Conference (ENERGYCON)*, 2016, pp. 1-6.

[102] S. Wenig, M. Goertz, C. Hirsching, M. Suriyah and T. Leibfried, "On Full-Bridge Bipolar MMC-HVDC Control and Protection for Transient Fault and Interaction Studies," *IEEE Transactions on Power Delivery*, vol. 33, no. 6, pp. 2864-2873, Dec. 2018.

134

[103] A. Nami, J. Liang, F. Dijkhuizen and P. Lundberg, "Analysis of modular multilevel converters with DC short circuit fault blocking capability in bipolar HVDC transmission systems", *Proc. 17th Eur. Conf. Power Electron. Appl.,* pp. 1-10, Sep. 2015.

[104] P. Tuennerhoff, P. Ruffing and A. Schnettler, "Comprehensive fault type discrimination concept for bipolar full-bridge-based MMC HVDC systems with dedicated metallic return", *IEEE Trans. Power Del.,* vol. 33, no. 1, pp. 330-339, Feb. 2018.

[105] W. Su, X. Zhou, F. Cai, H. Chen, and F. Shi, "Application analysis of dc grounding resistance used in the Nanhui flexible HVDC," *Power Energy*, vol. 34, no. 6, Dec. 2013.

[106] K. Sano and H. Nakayama, "An Overvoltage-Less Protection Method for Pole-to-Ground Faults in Symmetrical Monopole HVDC Systems by Half-Bridge MMC," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 3383-3388.

[107] F. Palone, M. Marzinotto and L. Buono, "Temporary overvoltage mitigation in symmetrical monopole VSC-MMC HVDC links," in *2017 AEIT International Annual Conference*, 2017, pp. 1-6.

[108] M. Goertz, S. Wenig, S. Beckler, C. Hirsching, M. Suriyah and T. Leibfried, "Analysis of Cable Overvoltages in Symmetrical Monopolar and Rigid Bipolar HVDC Configuration," *IEEE Transactions on Power Delivery*, vol. 35, no. 4, pp. 2097-2107, Aug. 2020.

[109] D. Jovcic and K. Ahmed, High-Voltage Direct Current Transmission: Converter System and DC Grids. Hoboken, NJ, USA: Wiley, 2015.

[110] K. Sharifabadi, L Harnefors, H-P. Nee, S. Norrga and R. Teodorescu, "MMC-HVDC Transmission Technology and MTDC Networks," in *Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems*, IEEE, 2016, ch. 10, pp.336-372.

[111] Y. Xue and Z. Xu, "On the Bipolar MMC-HVDC Topology Suitable for Bulk Power Overhead Line Transmission: Configuration, Control, and DC Fault Analysis," *IEEE Transactions on Power Delivery*, vol. 29, no. 6, pp. 2420-2429, Dec. 2014.

[112] S. Wenig, M. Goertz, M. Suriyah and T. Leibfried, "Active DC fault management of a bipolar full-bridge MMC-HVDC scheme with metallic return," in *2016 IEEE International Energy Conference (ENERGYCON)*, 2016, pp. 1-6.

[113] D. Jovcic, M. Taherbaneh, J. Taisne and S. Nguefeu, "Developing regional, radial DC grids and their interconnection into large DC grids," *2014 IEEE PES General Meeting Conference & Exposition*, 2014, pp. 1-5.

[114] Y. Sato, "Novel IEGT based Modular Multilevel Converter for New Hokkaido-Honshu HVDC Power Transmission," *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD),* 2020, pp. 1-4.

[115] NordLink. Between Norway and Germany. [Online]. Available: https://www.hitachiabb-powergrids.com/references/hvdc/nordlink.

[116] N. R. Chaudhuri, R. Majumder and B. Chaudhuri, "System Frequency Support Through Multi-Terminal DC (MTDC) Grids," *IEEE Transactions on Power Systems*, vol. 28, no. 1, pp. 347-356, Feb. 2013.

[117] J. A. Ansari, C. Liu and S. A. Khan, "MMC Based MTDC Grids: A Detailed Review on Issues and Challenges for Operation, Control and Protection Schemes," *IEEE Access*, vol. 8, pp. 168154-168165, 2020.

[118] O. M. K. K. Nanayakkara, A. D. Rajapakse and R. Wachal, "Traveling-Wave-Based Line Fault Location in Star-Connected Multiterminal HVDC Systems," *IEEE Transactions on Power Delivery*, vol. 27, no. 4, pp. 2286-2294, Oct. 2012.

[119] F. Mohammadi et al., "HVDC Circuit Breakers: A Comprehensive Review," *IEEE Transactions on Power Electronics*, vol. 36, no. 12, pp. 13726-13739, Dec. 2021.

[120] F. Mohammadi et al., "HVDC Circuit Breakers: A Comprehensive Review," *IEEE Transactions on Power Electronics*, vol. 36, no. 12, pp. 13726-13739, Dec. 2021.

[121] K. Sano and M. Takasaki, "A Surgeless Solid-State DC Circuit Breaker for Voltage-Source-Converter-Based HVDC Systems," *IEEE Transactions on Industry Applications*, vol. 50, no. 4, pp. 2690-2699, July-Aug. 2014.

[122] M. M. Walter, " Switching arcs in passive resonance HVDC circuit breakers," Doctor of Science Thesis, 2013.

[123] W. Wen, et al., "Research on a current commutation drive circuit for hybrid dc circuit breaker and its optimisation design," *IET Generation, Transmission & Distribution*, vol. 10, no. 13, pp.

[124] W. Wen, et al., "Research on operating mechanism for ultra-fast 40.5-kV vacuum switches," *IEEE Trans. Power Del.*, vol. 30, no. 6, pp. 2553-2560, Dec. 2015.

[125] C. Peng, et al. "A fast mechanical switch for medium-voltage hybrid DC and AC circuit breakers," *IEEE Trans. Ind. Appl.,* vol. 52, no. 4, pp. 2911-2918, July-Aug. 2016.

[126] X. Song, C. Peng and A. Q. Huang, "A Medium-Voltage Hybrid DC Circuit Breaker, Part I: Solid-State Main Breaker Based on 15 kV SiC Emitter Turn-OFF Thyristor," *IEEE Journal of Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 278-288, March 2017.

[127] C. Peng, et al. "A Medium-Voltage Hybrid DC Circuit Breaker—Part II: Ultrafast Mechanical Switch," *IEEE Journal of Emerg. Sel. Topics Power Electron.,* vol. 5, no. 1, pp. 289-296, March 2017.

[128] Z. Zhang, et al. "Research on critical technical parameters of HVDC circuit breaker applied in Nan'ao multi-terminal VSC-HVDC project," *Power System Technology*, vol. 41, no. 8, pp. 2417-2422, Aug. 2017.

[129] World's first mechanical HVDC circuit breaker in operation. [Online]. Available:http://eng.csg.cn/Press_release/News_2017/201802/t20180209_164 843.html.

[130] R. Rodrigues, Y. Du, A. Antoniazzi and P. Cairoli, "A Review of Solid-State Circuit Breakers," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 364-377, Jan. 2021.

[131] L. Qi et al., "Solid-State Circuit Breaker Protection for DC Shipboard Power Systems: Breaker Design, Protection Scheme, Validation Testing," *IEEE Transactions on Industry Applications*, vol. 56, no. 2, pp. 952-960, March-April 2020.

[132] J. Hafner and B. Jacobson, "Proactive hybrid HVDC breakers – a key innovation for reliable HVDC grids", in *CIGRE Conf., Bologna*, Italy, Sept. 2011, pp. 1–8.

[133] C. Li, S. Wang and J. Liang, "Dual-circuit hybrid circuit breaker," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017, pp. P.1-P.10.

[134] W. Zhou, et al., "Development and test of a 200kV full-bridge based hybrid HVDC breaker," in *17th European Conference on Power Electronics and Applications* (EPE'15 ECCE-Europe), Geneva, 2015, pp. 1-7.

[135] G. Tang, Z. He, H. Pang, X. Huang and X. Zhang, "Basic topology and key devices of the five-terminal DC grid," *CSEE Journal of Power and Energy Systems,* vol. 1, no. 2, pp. 22-35, June 2015.

[136] NREC. VSC HVDC transmission. [Online]. Available: https://www.nrec.com/en/index.php/plan/planInfo/13.html.

[137] H. Pang and X. Wei, "Research on Key Technology and Equipment for Zhangbei 500kV DC Grid," *2018 International Power Electronics Conference* (IPEC-Niigata 2018 -ECCE Asia), 2018, pp. 2343-2351.

[138] J. Yang, Z. Yu, C. Ying, Z. Xu and G. You, "System-level Control Strategy of UPFC in Regional Power Grids," *2019 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, 2019, pp. 1-5.

[139] X. Zhong, M. Zhu, S. Wang and X. Cai, "Topology, Operation Principle and Control of three-line Composite DC Power Flow Controller," in *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*, 2020, pp. 1305-1309.

[140] L. Liming, Z. Pengcheng, K. Yong and C. Jian, "Unified Power Flow Controller: Comparison of Two Advanced Control Schemes and Performance Analysis for Power Flow Control," in *2006 CES/IEEE 5th International Power Electronics and Motion Control Conference*, 2006, pp. 1-5.

[141] W. J. Du, Z. Chen, H. F. Wang and P. Ju, "Robustness of Unified Power Flow Controller to the Variations of Control Operating Conditions," in *Proceedings of the 41st International Universities Power Engineering Conference*, 2006, pp. 507-510.

[142] L. Zhang, B. Zhou, P. Li, Y. Yuan, J. Xu and X. Kong, "Impact Evaluation for Distance Protection of Southern Suzhou 500kV UPFC," *2019 14th IEEE*

Conference on Industrial Electronics and Applications (ICIEA), 2019, pp. 293-298.

[143] Wang, Xu, Haiqian Wang, Jian Yang, Zheng Xu, Wentao Sun, Chen Wu and Chen Li. "Application of 500 kV UPFC in Suzhou southern power grid." *The Journal of Engineering*, pp: 2580-2584, 2019.

[144] E. Veilleux and B. Ooi, "Power flow analysis in multi-terminal HVDC grid," in *Proc. 2011 IEEE/PES Power Systems Conference and Exposition*, Phoenix, AZ, 2011, pp. 1-7.

[145] Q. Mu, J. Liang, Y. Li and X. Zhou, "Power flow control devices in DC grids," in *Proc. 2012 IEEE Power and Energy Society General Meeting*, San Diego, CA, 2012, pp. 1-7.

[146] K. Rouzbehi, S. S. Heidary Yazdi and N. Shariati Moghadam, "Power Flow Control in Multi-Terminal HVDC Grids Using a Serial-Parallel DC Power Flow Controller," *IEEE Access*, vol. 6, pp. 56934-56944, 2018.

[147] E. Veilleux and B. T. Ooi, "Multiterminal HVDC With Thyristor Power-Flow Controller," *IEEE Trans. Pow. Del.,* vol. 27, no. 3, pp. 1205-1212, 2012.

[148] J. Sau-Bassols, E. Prieto-Araujo and O. Gomis-Bellmunt, "Modelling and control of an interline Current Flow Controller for meshed HVDC grids," IEEE Trans. Power Del. vol. 32, issue 1, pp. 11-22, Feb. 2017.

[149] C. Barker and R. Whitehouse, "A current flow controller for use in HVDC grids," in *IET Int. Conf. on AC and DC Power Trans. (ACDC)*, pp. 1-5, 2012.

[150] N. Deng, P. Wang, X. Zhang, G. Tang, and J. Cao, "A DC current flow controller for meshed modular multilevel converter multi-terminal HVDC grids," *CSEE J. Power Energy Syst.*, vol. 1, no. 1, pp. 43–51, Mar. 2015.

[151] J. YI, M. ZHU, X. ZHONG, H. WANG and X. CAI, "An Improved Triple Interline DC Power Flow Controller for Bidirectional Power Control," in *2020 IEEE REGION 10 CONFERENCE (TENCON)*, 2020, pp. 1301-1306.

[152] S. Balasubramaniam, C. E. Ugalde-Loo, J. Liang, T. Joseph, R. King and A. Adamczyk, "Experimental Validation of Dual H-Bridge Current Flow Controllers for Meshed HVDC Grids," *IEEE Trans. Power Del.* vol. 33, no. 1, pp. 381-392, Sep. 2017.

[153] P. Wang, S. Feng, P. Liu, N. Jiang and X. -P. Zhang, "Nyquist stability analysis and capacitance selection for DC current flow controllers in meshed multi-terminal HVDC grids," *CSEE Journal of Power and Energy Systems*, vol. 7, no. 1, pp. 114-127, Jan. 2021.

[154] D. Jovcic and B. T. Ooi, "Developing DC Transmission Networks Using DC Transformers," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2535-2543, Oct. 2010.

[155] N. Denniston, A. M. Massoud, S. Ahmed and P. N. Enjeti, "Multiple-Module High-Gain High-Voltage DC-DC Transformers for Offshore Wind Energy Systems," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 5, pp. 1877-1886, May 2011.

[156] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday and B. W. Williams, "Quasi Two-Level Operation of Modular Multilevel Converter for

Use in a High-Power DC Transformer With DC Fault Isolation Capability," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 108-123, Jan. 2015.

[157] J. Zhang, Z. Wang and S. Shao, "A Three-Phase Modular Multilevel DC-DC Converter for Power Electronic Transformer Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 140-150, March 2017.

[158] S. Shao et al., "Modeling and Advanced Control of Dual Active Bridge DC-DC Converters: A Review," *IEEE Transactions on Power Electronics,* (early access).

[159] B. Zhao, Q. Song, W. Liu and Y. Sun, "Overview of Dual-Active-Bridge Isolated Bidirectional DC-DC Converter for High-Frequency-Link Power-Conversion System," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4091-4106, Aug. 2014.

[160] G. Li, W. Liu, T. Joseph, J. Liang and Z. Song, "Double-Thyristor-Based Protection for Valve-Side Single-Phase-to-Ground Faults in HB-MMC-Based Bipolar HVDC Systems," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 7, pp. 5810-5815, July 2020.

[161] D. Jovcic, W. Lin, S. Nguefeu and H. Saad, "Full bridge MMC converter controller for HVDC operation in normal and DC fault conditions," in *2017 International Symposium on Power Electronics*, 2017, pp. 1-6.

[162] Rodriguez, P., Pou, J., Bergas, J., Candela, J. I., Burgos, R.P. and Boroyevich, D., 'Decoupled Double Synchronous Reference Frame PLL for Power Converters Control'. *IEEE Transactions on Power Electronics*, 22, March 2007, 584-592.

[163] P. Rodriguez, A. Luna, M. Ciobotaru, R. Teodorescu and F. Blaabjerg, "Advanced Grid Synchronization System for Power Converters under Unbalanced and Distorted Operating Conditions," *IECON 2006 - 32nd Annual Conference on IEEE Industrial Electronics*, 2006, pp. 5173-5178.

[164] Y. Xiao and L. Peng, "A Novel Fault Ride-Through Strategy Based on Capacitor Energy Storage Inside MMC," *IEEE Transactions on Power Electronics,* vol. 35, no. 8, pp. 7960-7971, Aug. 2020.

[165] E. Shahriari, F. Gruson, P. Vermeersch, P. Delarue, F. Colas and X. Guillaud, "A Novel DC Fault Ride Through Control Methodology for Hybrid Modular Multilevel Converters in HVDC Systems*," IEEE Transactions on Power Delivery*, vol. 35, no. 6, pp. 2831-2840, Dec. 2020.

[166] J. Cheng and Z. Xu, "Analysis of AC faults in converter station and characteristics of its relay protection," Proceedings of the CSEE, vol. 31, no. 22, pp. 88-95, August 2011.

[167] N. Mei, Y. Li, D. Liu, X. Duan, C. Fu, H. Rao, "Study on the Operational Equation for Valve Short Circuit Protections in HVDC Projects," *Proceedings of the CSEE*, pp. 40–47, January 2009.

[168] Yang, J. Zheng, G. Tang, and Z. He, "Internal AC bus fault characteristics of VSC-HVDC system and protection coordination," Proceedings of the CSEE, vol. 30. no. 16, pp. 6-11, June 2010.

[169] J. Cheng and Z. Xu, "Analysis of AC faults in converter station and characteristics of its relay protection," *Proceedings of the CSEE*, vol. 31, no. 22, pp. 88-95, August 2011.

[170] N. Mei, Y. Li, D. Liu, X. Duan, C. Fu, H. Rao, "Study on the Operational Equation for Valve Short Circuit Protections in HVDC Projects," *Proceedings of the CSEE*, pp. 40–47, January 2009.

[171] J. Yang, J. Zheng, G. Tang, and Z. He, "Internal AC bus fault characteristics of VSC-HVDC system and protection coordination," *Proceedings of the CSEE*, vol. 30. no. 16, pp. 6-11, June 2010.

[172] Y. Zhou, Z. He, H. Pang, J. Yang, and Q. Li, "Protection of converter grounding fault on MMC based bipolar HVDC systems," *Proceedings of the CSEE*, vol. 35, no. 16, pp. 4062-4069, Aug. 2015.

[173] A. Nami, J. Liang, F. Dijkhuizen and P. Lundberg, "Analysis of modular multilevel converters with DC short circuit fault blocking capability in bipolar HVDC transmission systems," in *2015 17th European Conference on Power Electronics and Applications*, Geneva, 2015, pp. 1-10.

[174] C. Barker and R. Whitehouse, "A current flow controller for use in HVDC grids," in IET Int. Conf. on AC and DC Power Trans. (ACDC), pp. 1-5, 2012.

[175] K. Rouzbehi, S. S. Heidary Yazdi and N. Shariati Moghadam, "Power Flow Control in Multi-Terminal HVDC Grids Using a Serial-Parallel DC Power Flow Controller," *IEEE Access*, vol. 6, pp. 56934-56944, 2018.

[176] J. Sau-Bassols, E. Prieto-Araujo, O. Gomis-Bellmunt and F. Hassan, "Series Interline DC/DC Current Flow Controller for Meshed HVDC Grids," *IEEE Transactions on Power Delivery*, vol. 33, no. 2, pp. 881-891, April 2018.

[177] S. Balasubramaniam, C. E. Ugalde-Loo, J. Liang, T. Joseph and A. Adamczyk, "Pole Balancing and Thermal Management in Multiterminal HVDC Grids Using Single H-Bridge-Based Current Flow Controllers," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 6, pp. 4623-4634, June 2020.

[178] J. Sau-Bassols, R. Ferrer-San-José, E. Prieto-Araujo and O. Gomis-Bellmunt, "Multiport Interline Current Flow Controller for Meshed HVDC Grids," *IEEE Transactions on Industrial Electronics,* vol. 67, no. 7, pp. 5467-5478, July 2020.

[179] S. Balasubramaniam, C. E. Ugalde-Loo, J. Liang and T. Joseph, "Power Flow Management in MTdc Grids Using Series Current Flow Controllers," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 11, pp. 8485-8497, Nov. 2019.

[180] N. Deng, P. Wang, X. Zhang, G. Tang, and J. Cao, "A DC current flow controller for meshed modular multilevel converter multi-terminal HVDC grids," CSEE J. Power Energy Syst., vol. 1, no. 1, pp. 43-51, Mar. 2015.

[181] J. Sau-Bassols, R. Ferrer-San-José, E. Prieto-Araujo and O. Gomis-Bellmunt, "Unidirectional Series Interline DC/DC Current Flow Controller for Meshed HVDC grids," in *2019 21st European Conference on Power Electronics and Applications* (EPE '19 ECCE Europe), 2019, pp. P.1-P.8.

[182] J. Sau-Bassols, E. Prieto-Araujo, F. Hassan and O. Gomis-Bellmunt, "Selective Operation of Distributed Current Flow Controller Devices for Meshed HVDC

Grids," in *2020 IEEE Power & Energy Society General Meeting (PESGM)*, 2020, pp. 1-1.

[183] S. Balasubramaniam, J. Liang and C. E. Ugalde-Loo, "Control, dynamics and operation of a dual H-bridge current flow controller," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE), 2015, pp. 2386-2393.*

[184] F. Hassan, R. King, R. Whitehouse, and C. Barker, "Double modulation control (DMC) for dual H-bridge current flow controller (2B-CFC)," in *17th European Conf. on Power Electron. and Applications* (EPE'15 ECCE-Europe), Geneva, pp. 1-9, 2015.

[185] W. Liu, J. Liang, C. E. Ugalde-Loo, C. Li, G. Li and P. Yang, "Level-shift Modulation and Control of a Dual H-bridge Current Flow Controller in Meshed HVDC systems," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 62-66.

[186] W. Liu, J. Liang, C. E. Ugalde-Loo, G. Li, C. Li and F. Colas, "Modeling and Frequency Analysis of a Dual H-bridge Current Flow Controller in Meshed HVDC systems," *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, 2019, pp. P.1-P.9.

[187] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages", *Int. J. Electronics*, vol. 42, no. 6, pp. 521-550, June 1977.

[188] Simone Buso; Paolo Mattavelli, *Digital Control in Power Electronics*, 2nd Edition , Morgan & Claypool, 2015.

[189] E. Kontos, T. Schultz, L. Mackay, L. Ramirez-Elizondo, C. Franck, and P.Bauer, "Multi-line breaker for HVDC applications," *IEEE Trans. Power Del.*, vol. 8977, no. c, pp. 1–8, 2017.

[190] A. Mokhberdoran, D. V. Hertem, N, Silva, H. Leite, and A. Carvalho, "Multiport hybrid HVDC circuit breaker," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 309–320, Jan. 2018.

[191] W. Liu, F. Liu, Y. Zhuang, X. Zha, C. Chen, and T. Yu, "A Multiport Circuit Breaker-Based Multiterminal DC System Fault Protection," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 118-128, Mar. 2019.

[192] G. Tang, H. Pang, Z. He and X. Wei, "Research on Key Technology and Equipment for Zhangbei 500kV DC Grid," in *Proc. 2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, Niigata, 2018, pp. 2343-2351.

[193] G. Liu, F. Xu, Z. Xu, Z. Zhang, and G. Tang, "Assembly HVDC breaker for HVDC grids with modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 931–941, Feb. 2017.

[194] O. Cwikowski, J.Sau-Bassols, B. Chang, E. Prieto-Araujo, M, Barnes, O. Gomis-Bellmunt, R. Shuttleworth, "Integrated HVDC Circuit Breakers With Current Flow Control Capability," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 371-380, Feb. 2018.

[195] A. Mokhberdoran, O. Gomis-Bellmunt, N. Silva and A.Carvalho, "Current flow controlling hybrid dc circuit breaker" *IEEE Trans. Power Electron*., vol. 33, no. 2, pp. 1323–1334, Feb. 2017.

[196] 5SNA 3000K452300 data sheet. [Online]. ABB, 2017.

[197] J. P. Kjærgaard et al., "Bipolar operation of an HVDC VSC converter with an LCC converter," in *Proc. CIGRE Colloq. HVDC Power Electron. Syst.,* 2012, pp. 1–7.

[198] G. Andersson and M. Hyttinen, "Skagerrak the next generation," in *Proc. HVDC Power Electron. Tech., CIGRE*, 2015, pp. 1–9.

[199] G. Li, J. Liang, F. Ma, C. E. Ugalde-Loo, H. Liang, and H. Li, "Analysis of single-phase-to-ground faults at the valve-side of HB-MMCs in bipolar HVDC systems," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 2659–2665.

[200] G. Li, J. Liang, F. Ma, C. E. Ugalde-Loo, and H. Liang, "Analysis of single-phase-to-ground faults at the valve-side of HB-MMCs in HVDC systems," *IEEE Trans. Ind. Electron.,* vol. 66, no. 3, pp. 2444–2453, Mar. 2019.

[201] S. Xue, C. Gu, B. Liu and B. Fan, "Analysis and Protection Scheme of Station Internal AC Grounding Faults in a Bipolar MMC-HVDC System," in *IEEE Access*, vol. 8, pp. 26536-26548, 2020.

[202] T. Jonsson, P. Lundberg, S. Maiti, and Y. Jiang, "Converter technologies and functional requirements for reliable and economical HVDC grid design," in Proc. CIGRE Canada Conf., Sep. 9-10, 2013, pp. 1–9.

[203] X. Li, Q. Song, W. Liu, H. Rao, S. Xu and L. Li, "Protection of Nonpermanent Faults on DC Overhead Lines in MMC-Based HVDC Systems," *IEEE Trans. Power Del.*, vol. 28, no. 1, pp. 483-490, Jan. 2013.

[204] A. A. Elserougi, A. S. Abdel-Khalik, A. M. Massoud and S. Ahmed, "A New Protection Scheme for HVDC Converters Against DC-Side Faults With Current Suppression Capability," *IEEE Transactions on Power Delivery*, vol. 29, no. 4, pp. 1569-1577, Aug. 2014.

[205] L. Tang and B. T. Ooi, "Managing zero sequence in voltage source converter," in *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No.02CH37344)*, Pittsburgh, PA, USA, 2002, pp. 795-802 vol.2.

[206] W. Yang, Q. Song, H. Rao, S. Xu and Z. Zhu, "Converter side phase-to-ground fault protection of full-bridge modular multilevel converter-based bipolar HVDC," in *Proc. IECON of IEEE Industrial Electronics Society*, Beijing, 2017, pp. 185-189.

[207] Datasheet: Phase Control Thyristor, 5STP 42U6500. ABB, 2018