Accurate Characterisation and Modelling of SiC MOSFETs for Transient Simulation

Peng Yang

School of Engineering

Cardiff University

A thesis submitted to

Cardiff University

for the degree of

Doctor of Philosophy

January 2022

Abstract

Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) possess properties that are superior compared to their silicon counterparts, such as low conduction and switching losses, high thermal conductivity and operating temperatures, etc. SiC MOSFETs need to be evaluated either experimentally or through simulation to fully exploit or understand their benefits. Compared to experimentation, simulation is more time and cost-efficient so is preferred at the initial converter design stage. However, accurate and fast models of SiC MOSFETs need to be established for such simulation, which is challenging due to fast switching speed and frequency of SiC MOSFETs. This thesis focuses on improving the accuracy and speed of models of SiC MOSFETs and simplifying the modelling process at the same time.

Firstly, the characteristics of SiC MOSFETs required for the modelling were analysed. It was found that the I-V and C-V characteristics in their dynamic state have a significant impact on the accuracy of the models. However, the existing methods to measure and extract these characteristics are complex due to the multiple measurement equipment configurations are required. This thesis proposes a simplified dynamic-state characterisation method. This method analyses the relationship between characteristics and the switching waveforms of SiC MOSFETs, and extracts these characteristics directly from the switching waveforms measured by a double pulse tester to simplify the measurement process. These measured dynamic-state characteristics, combined with the conventional static-state characteristics, were used to built the SiC MOSFET model. The re-

lative root-mean-square (RMS) errors of the model can be reduced by at least a factor of 3, compared to the model that only considers the conventional static-state characteristics.

Based on the extracted characteristics, a measurement-based hybrid data-driven modelling method is proposed. Conventional equation-based models have drawbacks such as a complex modelling process, poor adaptability, low accuracy and slow simulation speed. The proposed modelling method utilised a hybrid data-driven model based on artificial neural networks to simplify the modelling process and improve the adaptability. The switching waveforms simulated by the proposed model are $1.5 \sim 3$ times closer to the experimental waveforms, compared to the commercial equation-based Angelov model. At the same time, the proposed model is 30% faster than the Angelov model in terms of simulation speed.

However, equipment required for the measurement-based modelling may not be available for some converter designers, therefore, a step-by-step datasheet-based modelling method is proposed, which is completely based on the datasheet without the use of any further data or equipment. Compared to the measurement-based modelling method, the datasheet-based modelling method results in 24% increase in RMS errors and cannot accurately match the gate driver resistor used in practical experiment. However, the datasheet-based modelling method features a simpler modelling process and 15% faster simulation speed so provides a more cost and time-efficient process for converter designers to quickly validate their converter design.

Acknowledgments

I would like to firstly express my sincere thanks to my supervisor, Prof. Jun Liang. His inspiration, advice and encouragement helped me throughout my research study. In addition, his patience and continuous guidance in improving my research ability is of great value to me and my future academic life.

I would like to express my heartfelt gratitude to my supervisor, Dr. Wenlong Ming, for his invaluable assitance, guidance and constructive criticism in conducting my research and developing this thesis. He is always available and patient to offer insightful guidance, ideas and suggestions to me.

I would like to thank my colleagues in CIREGS. Their friendship, help and encouragement made my PhD journey so enjoyable. Here, I would like to mention some of them and they are Dr. Gen Li, Dr. Sheng Wang, Dr. Chuanyue Li, Dr. Yue Zhou, Mr. Jinlei Chen, Miss Chen Li, Mr. Xun Jiang, Dr. Carlos E. Ugalde-Loo, Prof. Jianzhong Wu and Prof. Nick Jenkins.

I would like to acknowledge the financial support from the European Commission's Marie Curie InnoDC project, which provided me the best opportunity to explore and develop my career with valuable trainings. My thanks also go to other Early Stage Researchers and supervisors in InnoDC project for the interesting and useful discussions we shared during this project and also to the project manager Manon Davies for her patience dealing with our issues.

Finally, I would like to express my deepest thanks to my family for their endless encouragement, understanding, patience and support throughout my life.

Contents

List of Tables

List of Figures

Acronyms and Symbols

Acronyms

AI	Artificial Intelligence
ANN	Artificial Neural Network
CAGR	Compound Annual Growth Rate
DPT	Double Pulse Tester
DUT	Device Under Test
EMI	Electromagnetic Interference
EV	Electric Vehicle
GaN	Gallium Nitride
GHG	Greenhouse Gas
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
RMS	Root Mean Square
SiC	Silicon Carbide
Si	Silicon
VNA	Vector Network Analyser

WBG	Wide Bandgap

Symbols

C_{DS}	drain-source capacitance
C_{GD}	gate-drain capacitance
C_{GS}	gate-source capacitance
C_{iss}	input capacitance
C_{oss}	output capacitance
C_{rss}	reverse transfer capacitance
di/dt	current rate-of-change
dv/dt	voltage rate-of-change
E_{off}	the turn-off loss of SiC MOSFET
E_{on}	the turn-on loss of SiC MOSFET
I_G	gate current
I_L	load current
I_{DS}	drain-source current
K_p	transconductance coefficient of datasheet-based model
λ	coefficient of short-channel effect of the datasheet-based model
R_G	gate resistor
R_{CH}	channel resistance
R_{DRIFT}	the resistance of the drift region
R_{JFET}	the resistance of the JFET region

R_{on}	on resistance
R_{SUB}	the resistance of the substrate
T_j	junction temperature
t_{off}	the turn-off time of SiC MOSFET
t_{on}	the turn-on time of SiC MOSFET
V_{DC}	dc-bus voltage
V_{DG}	drain-gate voltage
V_{DS}	drain-source voltage
V_{GP}	gate plateau voltage
$V_{GS,th}$	threshold voltage
V_{GS}	drain-source voltage

Chapter 1

Introduction

1.1 Background

1.1.1 Climate Change and Role of Power Electronics

Global climate change is one of the biggest environmental challenges facing the world. Greenhouse gas (GHG) emission from human activities is a significant and dominant cause of climate change, resulting in temperature rise, melting glaciers, drought, wildfires, etc. [2].

Worldwide efforts have been made in fighting climate change. The Paris Agreement, a legally binding global climate change agreement adopted at Paris climate conference (COP21) in December 2015, has set out a global framework to avoid dangerous climate change by limiting global warming to well below 2 °C and pursuing efforts to limit it to 1.5 °C [3]. To achieve the goals of Paris Agreement, the European Union (EU) has announced the European Green Deal in December 2019, setting out an overarching objective for the EU to become climate neutral (i.e., net zero GHG emissions) by 2050, with an intermediate target of reducing net GHG emissions by at least 55% by 2030, compared to 1990 levels [4]. The UK government has also committed to cutting GHG emissions by 78% by 2035 compared to 1990 levels, and achieving net zero GHG emissions by 2050 [5].

To assist the government to deliver these goals, in energy and transport sectors,

a substantial increase in using renewable energy sources (e.g. wind energy, solar energy, etc.) and electric vehicles (EVs) is required. The UK government plans to increase its offshore wind capacity from 30 GW to 40 GW by 2030. Besides, sales of new petrol and diesel cars and vans will be banned by 2030 in UK to accelerate the transition from internal combustion engine vehicles to EVs [6].

Power electronics play a crucial role in the development of renewable energy sources and EVs. Most renewable energy sources rely on power electronics to regulate the voltage, frequency and power so that they can be connected to the power grid. In EVs, power electronics are indispensable to convert DC power from the battery into AC power to drive the motor or to convert AC power from the grid into DC power to charge the battery.

For their application in renewable energy sources and EVs, the development of power electronics has a continuous trend towards higher power density and higher efficiency. The development of power semiconductors is a crucial enabling factor to achieve these targets. Today's power semiconductors are still dominated by the mature and well-established silicon (Si) technology. In low voltage applications below 600 V, Si MOSFETs dominate the market, whereas Si insulated gate bipolar transistors (IGBTs) dominate the high voltage market from 600 V to 6.5 kV. However, after decades of development, Si power semiconductors are approaching their material theoretical limitations which become a barrier to the further improvement of power electronics. For high voltage applications, the maximum blocking voltage of the Si IGBT is lower than 6.5 kV, and the practical operating temperature is lower than 175 °C. Besides, in the bipolar structure of IGBTs, the switching speed is relatively slow due to the slow carrier velocity of holes, limiting the efficiency and switching frequency of power electronics [7].

1.1.2 Emergence of SiC MOSFETs

Since Si-based power semiconductors are facing a bottleneck, the emerging power semiconductors based on wide-bandgap (WBG) materials are drawing the atten-

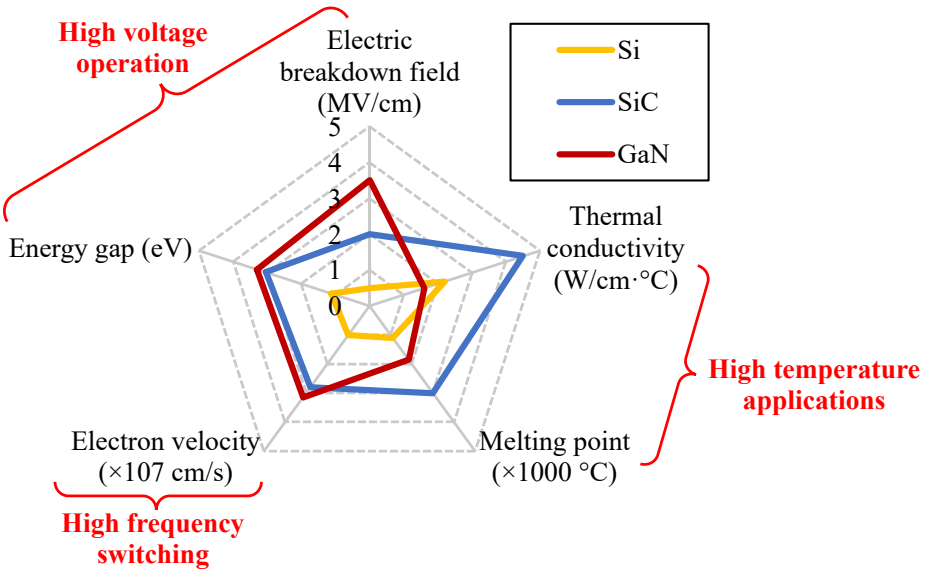


Figure 1.1: Comparison of Si, SiC and GaN relevant material properties [9].

tion due to their superior properties far beyond the limitations of their Si counterparts. These materials include silicon carbide (SiC), gallium nitride (GaN), gallium oxide (Ga_2O_3), diamond, etc. Among the possible candidates of WBG materials, silicon carbide (SiC) and gallium nitride (GaN) are the most popular ones due to the best trade-off between theoretical characteristics, commercial availability and technological maturity [8]. Ga_2O_3 and diamond have even wider bandgap than SiC and GaN, which are promising to achieve better performance. However, semiconductors based on Ga_2O_3 and diamond still have very low technical readiness level so they are not focused by this thesis. Fig. 1.1 highlights some key material properties of SiC and GaN compared to Si [9]. It is shown that the energy gap, electric breakdown field, thermal conductivity, melting point and electron velocity of WBG materials are significantly higher than those of Si. These advantages allow WBG semiconductors to operate at much higher voltage, temperature and switching frequency than Si semiconductors. Compared to GaN semiconductors, in today's market, SiC semiconductors presents more advantages in high-voltage high-power (600 V, kilowatts or above) applications [10].

Due to their superior properties, the market of SiC semiconductors is predicted to grow very quickly in the next few years. As shown in Fig. 1.2, a compound annual growth rate (CAGR) of 30%, from $225m in 2019 to $2.5bn in

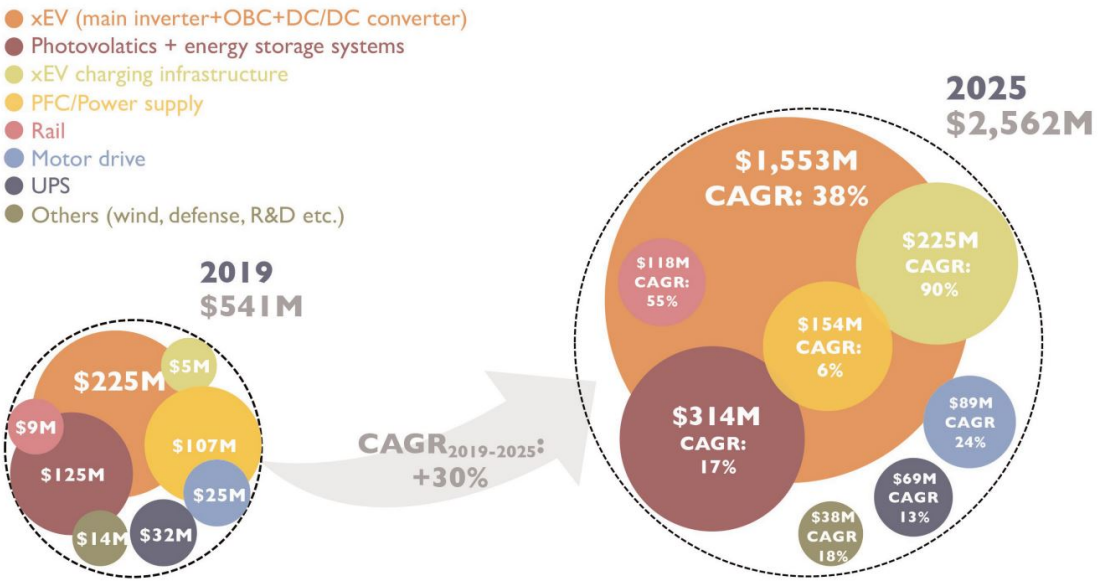


Figure 1.2: 2019-2025 market forecast of SiC power semiconductor split by application (CAGR: compound annual growth rate) [11].

2025, is estimated according to a report by Yole Development [11]. The adoption of SiC semiconductors covers a wide range of industrial applications including EVs, photovaltics, energy storage systems, power supply, motor driver, etc.

Among SiC semiconductors, SiC MOSFETs are the most developed active switches in the market. Since the breakdown field of SiC is 10 times higher than that of Si, SiC MOSFETs with ultra-high-voltage ratings (>10 kV) are practically achievable. Currently, SiC MOSFETs rated at 1.2 kV [12], 1.7 kV [13] and 3.3 kV [14] are commercially available, which can replace the Si insulated gate bipolar transistors (IGBTs) at the same voltage ratings. Wolfspeed has released the 10 kV SiC MOSFETs beyond the maximum voltage rating of 6.5 kV IGBTs and there are some laboratory research works on it [15]. The high breakdown voltage of SiC MOSFETs is attractive to reduce the complexity and increase the reliability of power electronics in high voltage applications.

Owing to the much wider energy bandgap of SiC materials, SiC MOSFETs can theoretically operate at temperatures beyond 500 °C [16]. Additionally, SiC has more than 3 times higher thermal conductivity than Si. This excellent thermal conductivity leads to a lower thermal resistance from junction to case, which allows SiC MOSFETs to dissipate more power losses with the same temperature

rise of junction temperature. The higher operating temperature, combined with the higher thermal conductivity can significantly reduce the cost and volume of cooling system for SiC-based power electronics.

SiC MOSFETs can switch more quickly than their Si counterparts. Firstly, since the breakdown field of SiC is 10 times higher than that of Si, a thinner drift layer with higher doping concentration can be utilised to manufacture the SiC MOSFET with a similar blocking voltage to their Si counterparts. Thus, a lower specific on-resistance and a smaller chip size is achieved in SiC MOSFETs. The reduced chip size enables smaller junction capacitance, resulting in a fast switching speed [17]. Secondly, due to the higher electron velocity of SiC, charge can be swept into and out of the junction capacitance very quickly, leading to a further increased switching speed of SiC MOSFETs.

1.1.3 Fast Switching Speed of SiC MOSFETs: Benefits and Challenges

The fast switching speed of SiC MOSFETs significantly affects overall performance of power electronics. On the one hand, it brings huge benefits to power electronics, including reduced power losses and increased switching frequency. These benefits lead to power electronics converters with high efficiency and high power density. On the other hand, the fast switching speed of SiC MOSFETs brings new challenges to power electronics, including electromagnetic interference (EMI) and reliability issues. Another challenge is that the high-efficiency high-power density design of power electronics requires accurate analysis of the fast switching behaviour of SiC MOSFETs to fully exploit their benefits in practical applications. These benefits and challenges are detailed as below:

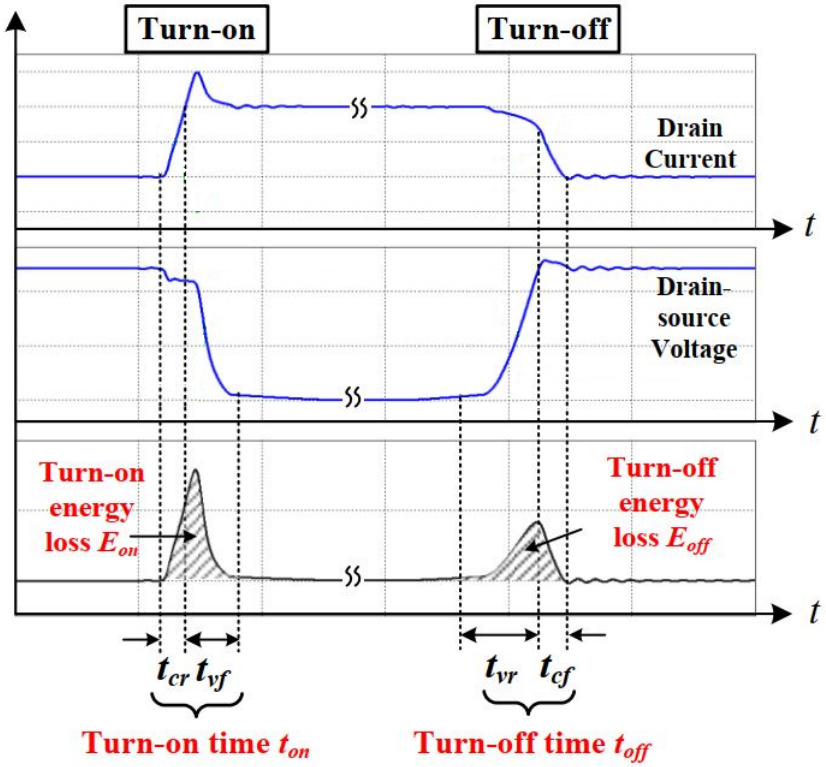
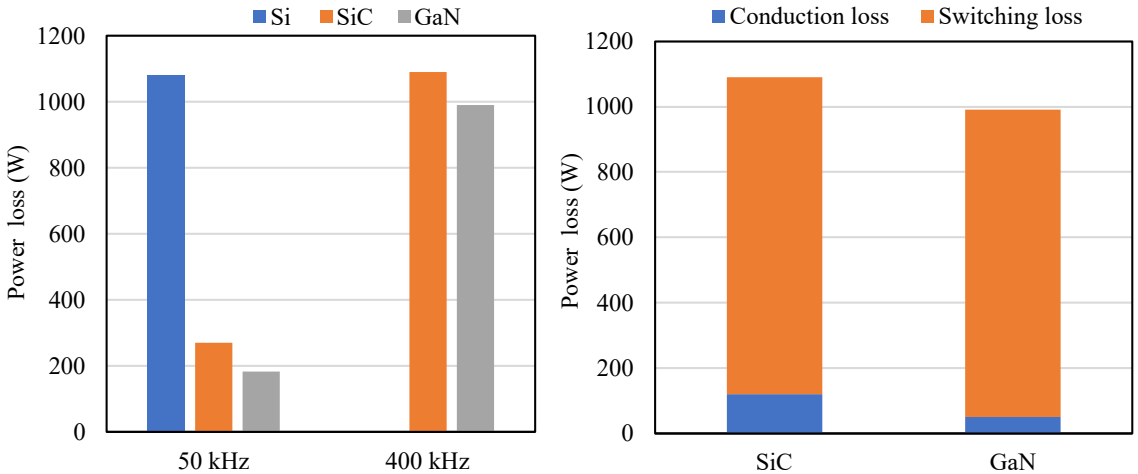


Figure 1.3: Switching waveforms of power semiconductors [17].



(a) Total loss.

(b) Conduction and switching losses at 400 kHz.

Figure 1.4: Comparison of power loss in different power semiconductors [18].

Benefits:

1) Loss and Efficiency

The power loss generated by power semiconductors consists of the conduction loss and the switching loss. The fast switching speed of the SiC MOSFET directly affects its switching loss. As shown in Fig. 1.3, each switching event (turn-on or turn-off) of power semiconductors takes a certain amount of switching time (i.e., t_{on} and t_{off} in Fig. 1.3). The overlapping of voltage and current of semiconductors during the switching event causes the switching loss (i.e., E_{on} and E_{off} in Fig. 1.3). Since SiC MOSFETs can switch much faster than Si IGBTs, the switching time of SiC MOSFETs is shorter than that of Si IGBTs, resulting in the reduced switching loss. Fig. 1.4 presents the total power loss of different power semiconductors for a 40 kW traction inverter [18]. It is shown in Fig. 1.4a that power loss of SiC MOSFETs is only 1/4 of the loss of Si IGBTs under the same switching frequency of 50 kHz. Fig. 1.4b shows that the switching loss is the main contributor to the total semiconductor loss for power electronics with a high switching frequency. Therefore, the greatly reduced switching loss due to the fast switching speed of SiC MOSFETs can significantly improve the efficiency of power electronics.

2) Power Density

Passive components (e.g., bulky dc bus capacitors, ac inductors and transformers, as well as harmonics and EMI filters) and cooling systems (e.g., heat sinks and cooling fans) are the dominating factors of the power density (size and weight) of power electronics [19].

The size and weight of passive components will be affected by the switching frequency of power semiconductors. For example, in a 5 kW boost converter, the size and weight of the filter inductor can be reduced by 70 % and 80%, respectively, if the switching frequency is increased from 20 kHz to 100 kHz, as shown in Fig. 1.5 [20]. The upper limit of the switching frequency is determined by the switching speed and switching loss. Firstly, it is obvious that the switching period

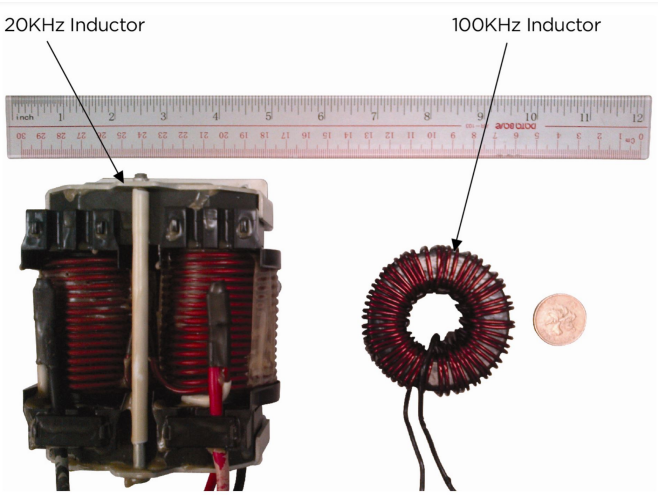


Figure 1.5: 5 kW filter inductors at switching frequencies of 20 kHz and 100 kHz [20].

(i.e., reciprocal of the switching frequency) must be longer than the switching time ($t_{on} + t_{off}$). Secondly, since the switching losses are proportional to the switching frequency, the switching frequency is limited by the maximum power losses that can be extracted by the cooling systems of power electronics. Therefore, the fast switching speed and low switching loss of SiC MOSFETs enables higher switching frequency of power electronics. As shown in Fig. 1.4a, in hard-switching converters, SiC MOSFETs can operate at 400 kHz with the same power loss as Si IGBTs operated at 50 kHz, resulting in significantly reduced size and weight of passive components.

The power loss of power semiconductors is one of the crucial parameters for designing the cooling systems of power electronics. Lower switching loss of SiC MOSFETs results in reduced weight and size of cooling systems. For example, in a 40 kW traction inverter presented in [18], the size of the heat sink can be reduced by 60% if Si IGBTs are replaced by SiC MOSFETs at the same switching frequency of 50 kHz.

Challenges:

1) EMI and Reliability

Although the fast switching speed of SiC MOSFETs can significantly improve the efficiency and power density of power electronics, it also causes challenges such as more serious electromagnetic interference (EMI) noise. EMI noise will affect the operation reliability of the power electronics converter and its neighbouring equipment. The dv/dt and di/dt generated during the switching transients are the main noise sources of EMI, especially at high-frequency range [21]. Faster switching speed of SiC MOSFETs inevitably causes higher dv/dt and di/dt, resulting in more critical EMI issues. Besides, the fast switching speed of the SiC MOSFET makes it more sensitive to circuit parasitics, causing ringing during the switching transient. Such ringing also plays an important role in increasing EMI noise. Furthermore, EMI noise, including common mode (CM) noise and differential mode (DM) noise, also increase with the switching frequency of power electronics. Since SiC MOSFETs usually operate at much higher switching frequency than Si IGBTs in practical applications, they will cause more EMI noise. As shown in Fig. 1.6, the measured EMI spectra of the inverter based on SiC MOSFETs are higher than those of the inverter based on Si IGBTs [22].

Considering their higher operating temperature and higher thermal conductivity, SiC has higher thermal reliability compared to Si [23]. However, some challenges exist in the reliability of SiC MOSFETs. Firstly, as an emerging technology, the reliability of SiC MOSFETs needs to be demonstrated for various applications [24]. Secondly, high temperature operation of SiC MOSFETs indicates more stringent requirement for the package material of SiC MOSFETs [7]. Thirdly, SiC MOSFETs have smaller die size than their Si counterparts under the same voltage and current ratings, resulting in higher current density and thermal stress of the SiC MOSFETs [25].

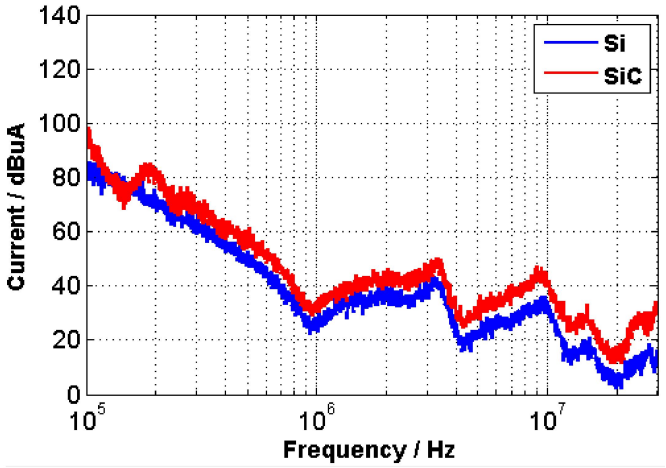


Figure 1.6: Measured EMI spectra of Si-based and SiC-based inverters [22]. The Si-based inverter operates at the switching frequency varying between 20-30 kHz. SiC-based inverter operates at the switching frequency between 80-120 kHz.

2) Design Optimisation of Power Electronics

Another challenge brought by the emergence of SiC MOSFETs is the design optimisation of power electronics to fully exploit the advantages of SiC MOSFETs and to mitigate the drawbacks. As described previously, some key performance indicators of power electronics, including efficiency, power density and reliability are all closely related to the fast switching behaviour of SiC MOSFETs. The cost is another key indicator although it is not mentioned above. However, these indicators might contradict each others in practical design as presented in Fig. 1.7. For example, by designing a smaller gate driver resistor for the SiC MOSFET, its switching speed becomes faster, resulting in reduced switching losses and increased efficiency. However, this also increases the dv/dt, di/dt and ringing of the switching transients, resulting in increased EMI noise and reduced reliability. By designing a higher switching frequency for the power electronics converter, the size and weight of passive components can be reduced, which can potentially increase the converter's power density. However, the increased switching frequency induces more switching loss, causing reduced efficiency of the converter. Besides, increased switching loss requires larger cooling systems, which reduces the converter's power density. Due to the counteracting effects between these indicators, trade-offs have to be made when a power electronics converter is designed.

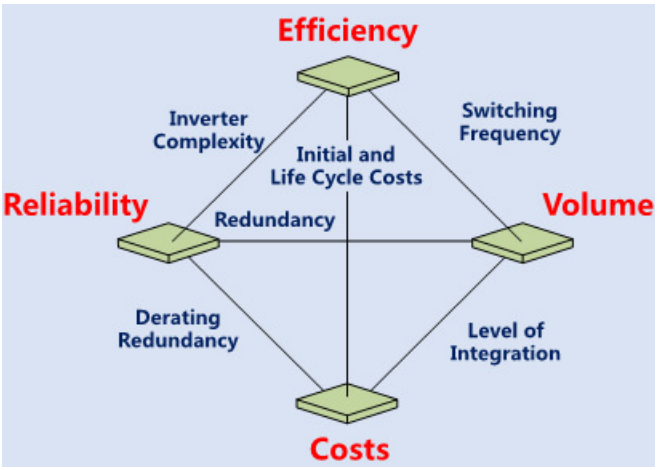


Figure 1.7: Counteracting effects of key performance indicators of power electronics [1].

Hardware prototyping is typically employed to design and optimise the performance indicators of the power electronics converter. However, due to the complex counteracting effects between these indicators, it requires multiple rounds of hardware prototyping to optimise the design parameters, which is expensive and time-consuming. Alternatively, virtual prototyping is a promising solution for the design optimisation of power electronics converters [26]. The virtual prototyping is based on mathematical models and multi-physics simulations to digitally design the converter parameters, which is less expensive and more time-efficient compared to hardware prototyping [27, 28]. Based on accurate mathematical multi-physics models of the converter and its components in virtual prototyping, multi-objective optimisation can be conducted to optimise the performance of the converter [29]. Since the fast switching transients of SiC MOSFETs affect many performance indicators (efficiency, power density, reliability, etc.), accurate transient simulation of SiC MOSFETs is essential for the virtual prototyping and multi-objective optimisation.

1.1.4 Transient Simulation of SiC MOSFETs

Transient simulation is to simulate the switching waveforms of SiC MOSFETs in practical converter applications. The performance of SiC MOSFETs related to

switching transients, such as power losses, di/dt, dv/dt, ringings and EMI can all be analysed from the simulated switching waveforms. The simulated results can be used as the input data for the multi-objective optimisation approach in virtual prototyping.

One of the biggest challenges for transient simulation of SiC MOSFETs is that the simulation need to be as accurate as possible so that the validity of the virtual prototyping can be guaranteed [30]. This challenge is much more critical for SiC MOSFETs than Si IGBTs because SiC MOSFETs feature much faster switching speed and much shorter switching transients. At the same time, the simulation needs to be fast enough for converters with complicated topologies.

The premise of accurate transient simulation is accurate characterisation and modelling of SiC MOSFETs. The characteristics of SiC MOSFETs need to be accurately measured at the first stage. Afterwards, an accurate model of SiC MOSFETs is built based on the measured characteristics. The model is then used for transient simulation and multi-objective optimisation of the power electronics converter. Finally, a converter prototype can be manufactured based on the optimisation results to validate the design. Such a design process is summarised as a design flow chart in Fig. 1.8. It can be seen that the characterisation (Step 1) and modelling (Step 2) of SiC MOSFETs play crucial roles in this flowchart.

1.2 Research Motivation

From the previous discussion of the background, it is aware that more effort is needed in the design optimisation of SiC-based power electronics before the superiorities of the SiC MOSFETs can be fully utilised, especially in the characterisation and modelling of SiC MOSFETs for accurate transient simulation.

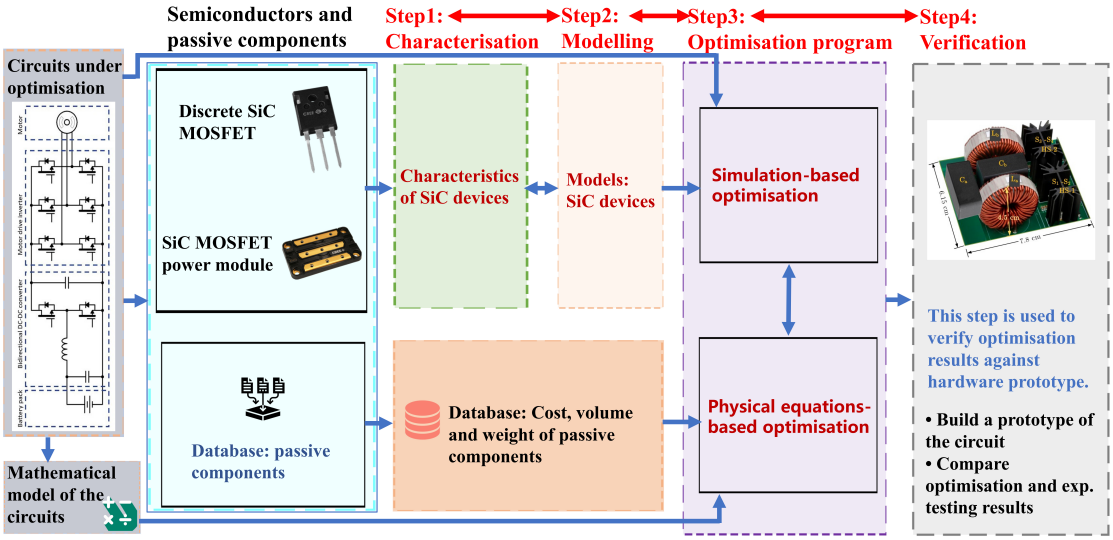


Figure 1.8: Virtual prototyping and multi-objective optimisation of power electronics based on characterisation and modelling of SiC MOSFETs.

1.2.1 Characterisation of SiC MOSFETs

Since the SiC MOSFET model is built based on its characteristics, the measurement method for accurate characterisation is required. The current-voltage (I-V) characteristics and capacitance-voltage (C-V) characteristics are the most important characteristics of SiC MOSFETs, which have great impacts on the switching behaviour of SiC MOSFETs. Therefore, there is a need to pay attention to the accurate measurement of these characteristics otherwise the models based on inaccurate characteristics will result in inaccurate simulation results and invalid design. In addition to the I-V and C-V characteristics in static state, it was found that the I-V and C-V characteristics in dynamic state (i.e., switching transient) have great impact on the accuracy of the model. However, the characterisation methods in previous studies [31–33] are very complex because multiple specialised measurement equipment such as the vector network analyser (VNA), the LCR meter, the gate charge evaluation circuit and the double pulse tester are required. Therefore, a research work on the simplified I-V and C-V characterisation methods in dynamic state is required to simplify the characterisation process and, at the same time, improve the accuracy of SiC MOSFET models.

1.2.2 Measurement-based Modelling of SiC MOSFETs

Once the characteristics of SiC MOSFETs are accurately measured, a measurement-based model can be built. And behavioural models can then be used. Firstly, the equivalent circuit model of SiC MOSFETs is constructed based on their physical structures. Secondly, the nonlinear components in the equivalent circuit are modelled based on mathematical equations to match the measured characteristics. Due to the high nonliearity of these characteristics, behavioural models (the detailed discussion is in Section 2.3.2) have following issues: 1) Complicated mathematical equations are required, which make it difficult to design suitable equations and to extract equation parameters; 2) The equations cannot accurately match the complex characteristics of the SiC MOSFET; 3) The designed mathematical equations lack adaptability to model different SiC MOSFETs with different characteristics accurately; 4) The complicated models have slow simulation speed. To address these issues, a research work is needed to investigate the modelling method of SiC MOSFETs which is accurate, fast, easy to use and adaptable to different devices.

1.2.3 Datasheet-based Modelling of SiC MOSFETs

Although measurement-based modelling method can deliver an accurate model for transient simulation based on measured characteristics, in some cases, the equipment required for the measurement-based modelling may not be achievable due to limited resources and high cost. The datasheet-based modelling method can be an alternative solution which is purely based on the characteristics of SiC MOSFETs obtained from the datasheet without the use of any further data or equipment. Many manufacturers provide transient simulation models along with the datasheets for their discrete devices. These models can be directly used by designers. However, the models for SiC MOSFETs power modules are currently not provided by manufacutures. There is a need to build models for these power modules based on the datasheets provided by manufacturers. Therefore, a study on the datasheet-based modelling method is required. Furthermore, a comprehens-

ive comparison between the measurement-based and datasheet-based modelling methods is required to provide a guidance for converter designers to choose the suitable method for their own applications.

1.3 Objectives and Contributions of This Thesis

The objectives and contributions of this thesis are outlined as follows:

- **Objective 1:** Investigate the method to measure the I-V and C-V characteristics of SiC MOSFETs in dynamic state to simplify the measurement process and improve the model accuracy of SiC MOSFETs in transient simulation.

  Contribution 1: A double-pulse-tester-based characterisation method was proposed to measure the I-V and C-V characteristics in dynamic state to improve the model accuracy in transient simulation. Conventionally, the DPT mainly focuses on measuring the switching waveforms of SiC MOSFETs. The contribution of the proposed method is to utilise the switching waveforms measured by the DPT to extract the dynamic-state I-V and C-V characteristics. The proposed method analysed the relationship of these characteristics with the switching waveforms of SiC MOSFETs, where these characteristics can be directly extracted from the switching waveforms. Since only a double pulse tester (DPT) is needed to be designed for the measurement of the switching waveforms, the proposed measurement method is much simpler than existing methods and can therefore be widely adopted by converter designers with low cost. The proposed method also reduced the self-heating of the SiC MOSFET when measuring the I-V characteristics in the high-voltage high-current ranges so that the errors induced by the increased junction temperature were reduced. These measured dynamic-state characteristics, combined with the conventional static-state characteristics, were used to built the SiC MOSFET model. The relative root-mean-square

(RMS) errors of the model can be reduced by at least 3 times, compared to the model that only considers the conventional static-state characteristics.

- **Objective 2:** Investigate the measurement-based method to accurately model the measured characteristics of SiC MOSFETs for fast transient simulation. In addition to accuracy and simulation speed, the modelling process needs to be simple and the modelling method needs to have good adaptability to model different types of SiC MOSFETs.

  Contribution 2: A measurement-based hybrid data-driven behavioural modelling methodology based on artificial neural networks (ANNs) has been proposed. For the first time, an ANN-based hybrid data-driven modelling method is proposed and verified for accurate transient simulation of SiC MOSFETs. The model was built based on the measured I-V and C-V characteristics. This proposed modelling method can overcome the challenges of the conventional behavioural modelling methods, such as model accuracy, simulation speed, adaptability, complex equation design, difficulties of parameter extraction, etc. The required training dataset and a proper hybrid model were identified for SiC MOSFETs. The switching waveforms simulated by the proposed model are $1.5 \sim 3$ times closer to the experimental waveforms, compared to a commercial Angelov model. At the same time, the proposed model is 30% faster than Angelov model in simulation speed.

- **Objective 3:** Investigate the datasheet-based modelling method to model the characteristics of SiC MOSFETs obtained from the datasheet. Besides, the comparison between the datasheet-based method and the measurement-based method need to be focused on to identify the usage of both methods.

  Contribution 3: A step-by-step modelling approach for SiC MOSFETs based on datasheet was proposed. A detailed and easy-to-follow parameter extraction process of each component in the model was clearly illustrated. The method is completely based on characteristics obtained from the data-

sheet without the need of any further data or equipment. Besides, a comprehensive comparison between the datasheet-based model and the measurement-based model was studied to provide a guidance for users to choose the suitable method for their own applications. Compared to the measurement-based modelling method, the datasheet-based modelling method presents 24% more relative RMS errors and cannot accurately match the gate driver resistor used in practical experiment. However, the datasheet-based modelling method features simpler modelling process and 15% faster simulation speed so provides a more cost and time-efficient process for converter designers to quickly validate their converter design.

1.4 Thesis Outline

The rest of this thesis is organised as follows:

Chapter 2 provides a literature review of operation principles of SiC MOSFET, state-of-the-art and challenges for the characterisation and modelling of SiC MOSFETs: including existing methods and challenges of: 1) static and dynamic characterisation of SiC MOSFETs; 2) the measurement-based behavioural modelling of SiC MOSFETs; 3) datasheet-based modelling of SiC MOSFETs.

Chapter 3 focuses on the accurate characterisation of SiC MOSFETs, including I-V and C-V characteristics. Firstly, the conventional I-V and C-V characterisation methods in static state and their limitations are illustrated. Secondly, after analysing the relation between the characteristics of the SiC MOSFET and its switching process, a double-pulse-tester-based characterisation method is proposed to measure the additional I-V and C-V characteristics in dynamic state as the complements of the conventionally-measured static-state characteristics. The measured dynamic-state characteristics can be used to improve the accuracy of the measurement-based model in Chapter 4.

Chapter 4 introduces a measurement-based modelling methodology for SiC

MOSFETs, i.e., a hybrid data-driven behavioural modelling methodology based on artificial neural networks. The model is trained with the I-V and C-V characteristics measured in Chapter 3. This proposed modelling method can overcome the challenges of the conventional behavioural modelling methods, such as model accuracy, simulation speed, adaptability, complex equation design, difficulties of parameter extraction, etc. The required training dataset and a proper hybrid model are identified for SiC MOSFETs. The effectiveness of the proposed modelling method is verified by comparing to a commercial measurement-based modelling method. The characterisation methods proposed in Chapter 3 are also verified based on the proposed hybrid data-driven model.

Chapter 5 illustrates a datasheet-based modelling methodology of SiC MOSFETs. Compared to the measurement-based methods in Chapter 4, the proposed datasheet-based modelling method only requires characteristics obtained from the datasheet of the SiC MOSFETs. Thus, the datasheet-based method can avoid complicated, time-consuming and expensive characterisation procedures. The detailed datasheet-based modelling approach is introduced step-by-step in this chapter, and its performance is compared to the measurement-based method in Chapter 4, in terms of required data, model accuracy, complexity and gate driver parameters.

Chapter 6 presents the conclusions and future work.

1.5 List of Publications

Published Academic Journal Papers

1. **P. Yang**, W. Ming, J. Liang, I. Ludtke, S. Berry and K. Floros, "Hybrid Data-driven Modelling Methodology for Fast and Accurate Transient Simulation of SiC MOSFETs," ***IEEE Transactions on Power Electronics***, vol. 37, no. 1, pp. 440-451, Jan. 2022, doi: 10.1109/TPEL.2021.3101713.

2. **P. Yang**, W. Ming, J. Liang, C. Ugalde, R. Navaratne, O. Ellabban, and

I. Ludtke, "SiC-Based Improved Neutral Legs with Reduced Capacitors for Three-phase Four-wire EV Chargers," ***IEEE Transactions on Transportation Electrification***, Early Access, 2022, doi: 10.1109/TTE.2021.3138333.

3. X. Jiang, Y. Zhou, W. Ming, **P. Yang**, and J. Wu, "An Overview of Soft Open Points in Electricity Distribution Networks", ***IEEE Transactions on Smart Grid***, Early Access, 2022.

Journal Papers Under Review or Preparation

1. **P. Yang**, W. Ming, J. Liang, R. Navaratne, I. Ludtke, and K. Floros, "Measurement Methodology for Self-Heating Reduction in High-Voltage High-Current Characterization of SiC MOSFETs," ***IEEE Electron Device Letters*** (first round review finished).

2. **P. Yang**, W. Ming, J. Liang, R. Navaratne, I. Ludtke, and K. Floros, "Double-Pulse-Tester-Based Measurement Method for Accurate Modeling of SiC MOSFETs," (under preparation for submission to ***IEEE Transactions on Power Electronics***).

3. M. Abdelrahman, **P. Yang**, W. Ming, J. Wu, and N. Jenkins, "Modified Unified Power Flow Controller for Medium Voltage Distribution Networks," ***IET Generation, Transmission and Distribution***, (under first round review).

4. C. Li, **P. Yang**, J. Wu, Y. Liu, I. Ludtke, and W Ming, "S-parameter-based Measurement Methodology for Accurate Extraction of Parasitic Inductance of SiC Power Modules", (under preparation for submission to ***IEEE Transactions on Power Electronics***).

Peer-reviewed Conference Papers

1. **P. Yang**, W. Ming and J. Liang, "A Step-by-step Modelling Approach for SiC Half-bridge Modules Considering Temperature Characteristics," ***2020 IEEE Energy Conversion Congress and Exposition (ECCE)***, 2020, pp. 2827-2834, doi: 10.1109/ECCE44975.2020.9235594.

2. **P. Yang**, W. Ming, J. Liang and J. Wu, "A SiC-based Neutral Leg for the Three-phase Four-wire Inverter," ***IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society***, 2019, pp. 1555-1560, doi: 10.1109/ IECON.2019.8927531.

3. **P. Yang**, W. Ming, J. Liang and J. Wu, "A Four-leg Buck Inverter for Three-phase Four-wire Systems with the Function of Reducing DC-bus Ripples," ***IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society***, 2019, pp. 1508-1513, doi: 10.1109/IECON.2019.8927264.

4. **P. Yang**, W. Ming, J. Liang and J. Wu, "Reduction of DC-link Ripples for Three-phase Four-wire Inverters with Unbalanced Loads," ***2019 IEEE Energy Conversion Congress and Exposition (ECCE)***, 2019, pp. 2819-2835, doi: 10. 1109/ECCE.2019.8912810.

5. W. Liu, J. Liang, C. E. Ugalde-Loo, C. Li, G. Li and **P. Yang**, "Level-shift Modulation and Control of a Dual H-bridge Current Flow Controller in Meshed HVDC systems," ***2019 IEEE Energy Conversion Congress and Exposition (ECCE)***, 2019, pp. 62-66, doi: 10.1109/ECCE.2019.8912857.

6. W. Ming, Q. Zhong, **P. Yang** and J. Liang, "Dual-Buck Arbitrary Voltage Divider with One Output Having Reduced Ripples," ***IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society***, 2018, pp. 3621-3626, doi: 10.1109/IECON.2018.8591447.

Chapter 2

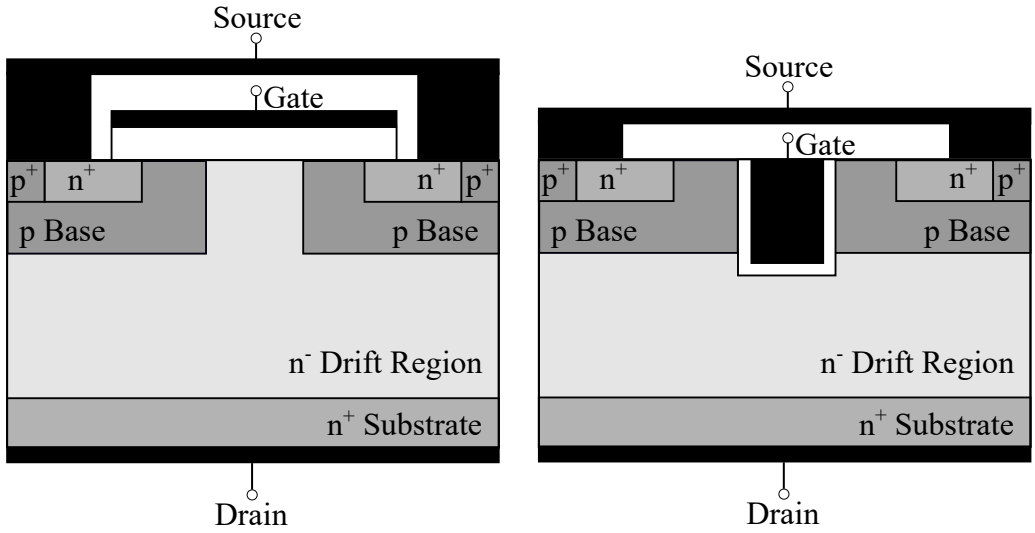
Literature Review

2.1 Operation Principle of SiC MOSFETs

2.1.1 Structure of SiC MOSFETs

Vertical structures are typically used for SiC MOSFETs to achieve a high blocking voltage. Fig. 2.1 shows two vertical structures of SiC MOSFETs, one is the planar structure (Fig. 2.1a), the other is the trench structure (Fig. 2.1b). These two structures are currently the most popular structures adopted by manufacturers. For example, Wolfspeed uses planar structure for its SiC MOSFETs in C2M^{TM} and C3M^{TM} series [34]; Infineon uses the trench structure for its SiC MOSFETs in CoolSiC^{TM} series [35]; Rohm uses both the planar structure in its SCT2 series products and the trench structure in its SCT3 series products [36].

It can be seen that the major difference between these two structures is their gate structures. The planar SiC MOSFET features a simple gate structure which can be easily manufactured, but it has high on-resistance causing high conduction loss. The trench SiC MOSFET is more attractive in lowering the on-resistance, but its complicated structure is relatively difficult to be manufactured [37]. It is worth noting that both planar SiC MOSFETs and trench SiC MOSFETs have undergone considerable development and optimisation, and several features have been added to the basic structures of Fig. 2.1 to improve their performance and



(a) Planar structure. (b) Trench structure.

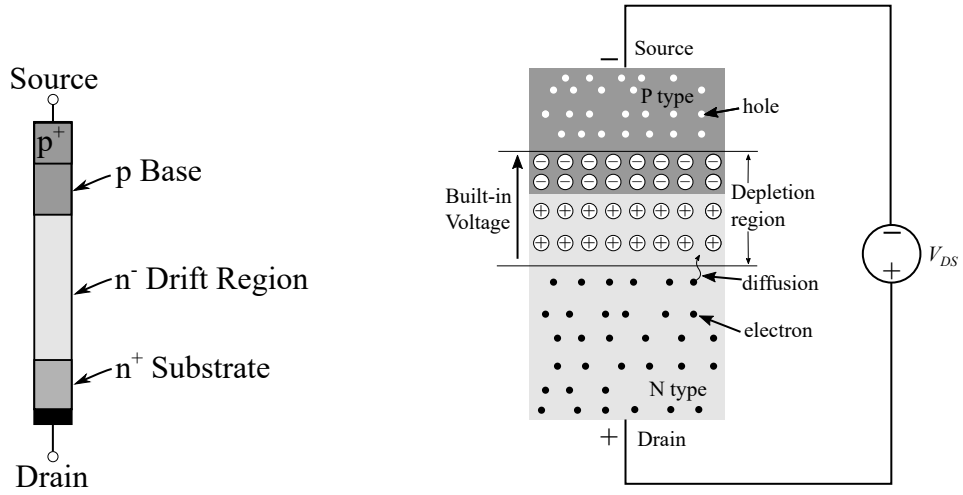
Figure 2.1: Two typical structures of SiC MOSFETs.

reliability. Since both the planar and trench SiC MOSFETs have similar operating principles, the planar type will be taken as an example to illustrate the operating principles of SiC MOSFETs.

2.1.2 Forward Blocking Mode of SiC MOSFETs

The operation mode of the SiC MOSFET is controlled by the gate-source voltage V_{GS}. When V_{GS} is lower than the threshold voltage, a forward conduction channel is not formed on the surface of the p-base region and thus the SiC MOSFET works in the forward blocking mode. In this mode, the operation principle of the SiC MOSFET can be simplified as a PN junction (i.e., a diode) as shown in Fig. 2.2a [38]. Therefore, the blocking mode of a diode can be used to understand the blocking mode of the SiC MOSFET.

As shown in Fig. 2.2b, when a positive drain-source voltage V_{DS} is applied to the SiC MOSFET in the forward blocking mode, the holes in the p type material (which is connected to the negative side of the voltage source) are pulled away from the PN junction. Similarly, the electrons in the n type material (which is connected to the positive side of the voltage source) are pulled away from the PN junction. Therefore, the thickness of the depletion region at the PN junction increases due to



(a) Simplified structure in forward blocking mode.

(b) Blocking mode of a PN junction.

Figure 2.2: Illustration of the forward blocking mode of SiC MOSFETs.

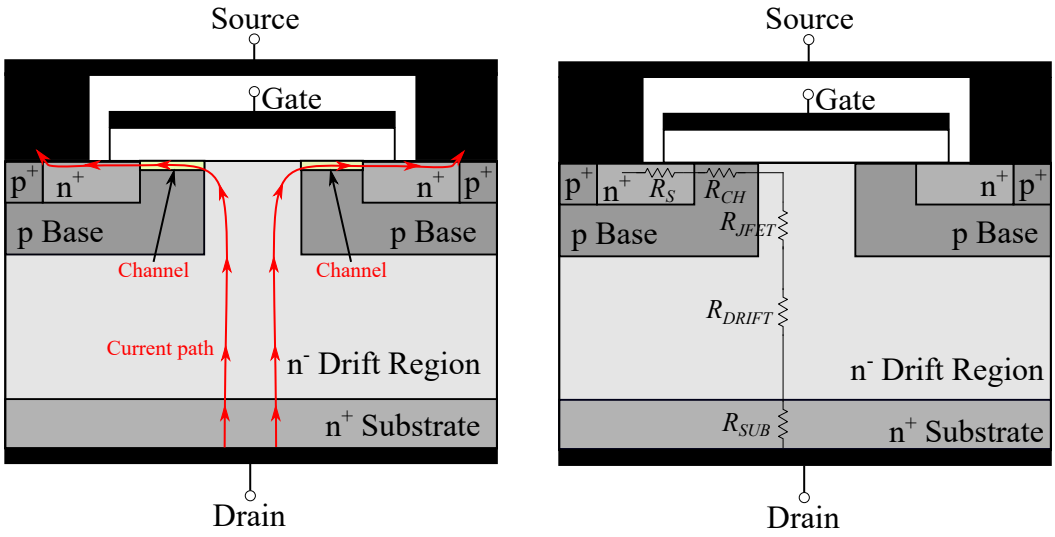
the positive V_{DS}, causing an increased built-in voltage. An equilibrium condition is reached and no current can flow when the built-in voltage in the depletion region equals to V_{DS} [39].

2.1.3 Forward Conduction Mode of SiC MOSFETs

When the gate-source voltage V_{GS} is larger than the threshold voltage, an inversion layer channel on the surface of the p-base region is formed as shown in Fig 2.3a and the SiC MOSFET works in the forward conduction mode [40]. The current can flow from drain to source through the inversion layer channel [41]. The current path is illustrated in Fig. 2.3a. The total on resistance in the current flow path is the sum of the resistance in each specific region as shown in Fig. 2.3b:

$$R_{on} = R_S + R_{CH} + R_{JEFT} + R_{DRIFT} + R_{SUB} \tag{2.1}$$

where R_S is the source resistance; R_{CH} is the channel resistance; R_{JEFT} is the resistance of the JFET region; R_{DRIFT} is the resistance of the drift region; R_{SUB} is the resistance of the substrate. The values of these resistances can be physically determined by the dimension and doping concentration of each region, as well as the bias gate-source and drain-source voltages (V_{GS} and V_{DS}). Detailed physical



(a) Current flow path. (b) On resistance.

Figure 2.3: Forward conduction mode of SiC MOSFETs.

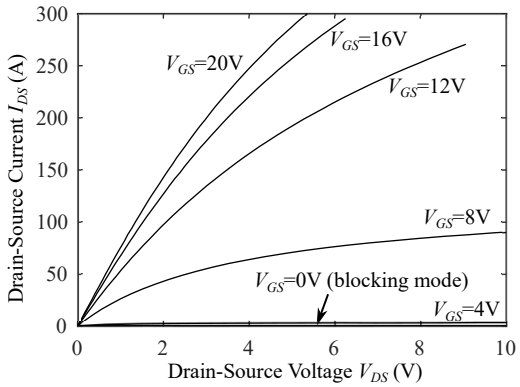


Figure 2.4: I-V characteristics of SiC MOSFET power module CAS120M12BM2.

equations of the on resistance have been derived in [42].

Due to the dependency of the on resistance on the bias voltages V_{GS} and V_{DS}, the current-voltage relation (i.e., I-V characteristics) is used to illustrate the on resistance and blocking mode under various bias conditions. Fig. 2.4 shows the nonlinear I-V characteristics of a SiC MOSFET power module CAS120M12BM2 [43].

2.1.4 Capacitances of SiC MOSFETs

Due to the unipolar conduction mechanism of SiC MOSFETs [44], only electrons are involved in the forward conduction mode as the majority carriers for N-channel SiC MOSFETs. The absence of minority carriers (i.e., holes for N-channel SiC

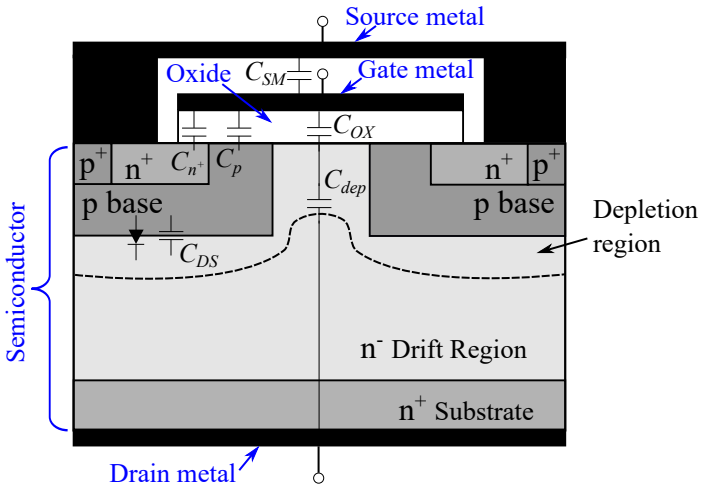


Figure 2.5: Capacitances within SiC MOSFETs.

MOSFETs) in the forward conduction mode allows immediate interruption of the current flow after the gate bias voltage is reduced below the threshold voltage [45]. Although this implies a very fast switching speed for SiC MOSFETs, in practice the switching speed is limited by the parasitic capacitances of SiC MOSFETs [46].

The capacitances within the SiC MOSFETs are presented in Fig. 2.5. According to their locations, they can be summarised as three capacitances: gate-source capacitance C_{GS}, gate-drain capacitance C_{GD} and drain-source capacitance C_{DS}.

As shown in Fig. 2.5, the gate-source capacitance is primarily determined by the overlap of the gate metal electrode with the N^+ source region and the p base region of the semiconductor, interfaced by the gate oxide. This forms the metal-oxide-semiconductor (MOS) capacitances C_{n^+} and C_p [47]. Besides, in the structure of SiC MOSFETs, the source metal electrode overlaps the gate metal electrode, producing the parallel metal plate capacitance C_{SM}. The values of C_{n^+}, C_p and C_{SM} can be determined by the geometry of the SiC MOSFET structure such as the width of the overlapping region and the thickness of the gate oxide. Detailed physical equations have been derived in [48]. The total gate-source capacitance C_{GS} can be obtained by adding up these three individual capacitances:

$$C_{GS} = C_{n^+} + C_p + C_{SM} \tag{2.2}$$

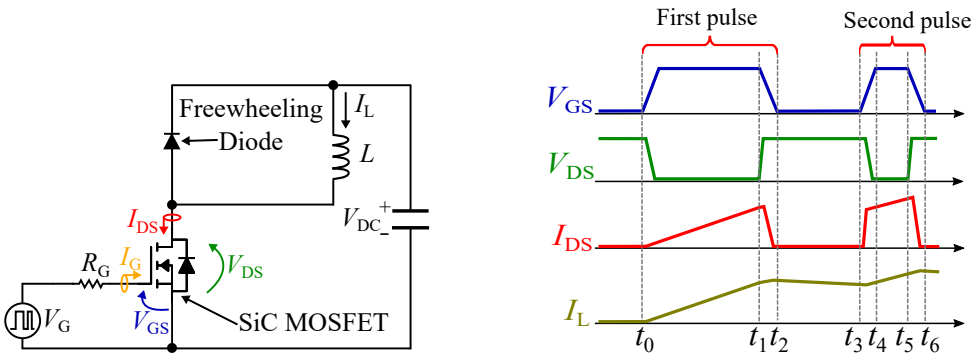
The gate-drain capacitance C_{GD} is also a MOS capacitance formed by the overlap of the gate metal electrode with the n^- drift region of the semiconductor. As shown in Fig. 2.5, C_{GD} can be treated as two individual capacitance (C_{OX} and C_{dep}) in series. C_{OX} is the specific capacitance of the gate oxide capacitance. C_{dep} is the specific capacitance of the semiconductor depletion region under the gate oxide. The value of C_{dep} is determined by the width of the depletion region. When the bias voltage V_{DG} increases, the width of the depletion region under the gate oxide increases, resulting in the reduction of C_{dep}. Detailed illustration and equations of C_{OX} and C_{dep} have been provided in [49]. Eventually, the gate-drain capacitance C_{GD} can be obtained as:

$$C_{GD} = \frac{C_{OX}C_{dep}}{C_{OX} + C_{dep}} \tag{2.3}$$

The drain-source capacitance C_{DS} is formed at the PN junction between the p base region and the n^- drift region, as shown in Fig. 2.5. According to Fig. 2.2b, a depletion region is formed in the PN junction when a positive V_{DS} is applied. C_{DS} is also determined by the width of the depletion region. When V_{DS} increases, the width of the depletion region increases and the value of C_{DS} reduces [50].

2.1.5 Switching Process of SiC MOSFETs

The switching process of SiC MOSFETs is significantly influenced by the I-V characteristics and capacitances of SiC MOSFETs. A double pulse tester (DPT) as shown in Fig. 2.6 is usually used to evaluate the switching performance of the SiC MOSFET [51]. A detailed operation principle of DPT is given in Section 2.2.1. The switching process of the SiC MOSFET and its relationship with the I-V characteristics and capacitances are illustrated based on the DPT and provided as below. To highlight the impact of I-V characteristics and capacitances on the switching process and to simplify the analysis, the parasitic inductances in the circuit are ignored. However, the parasitic inductances also significantly affect the switching process and need to be characterised accurately [52].



(a) Schematic of DPT.

(b) Operation principle of DPT.

Figure 2.6: Double pulse tester to evaluate the switching process of the SiC MOSFET.

Turn-on Process:

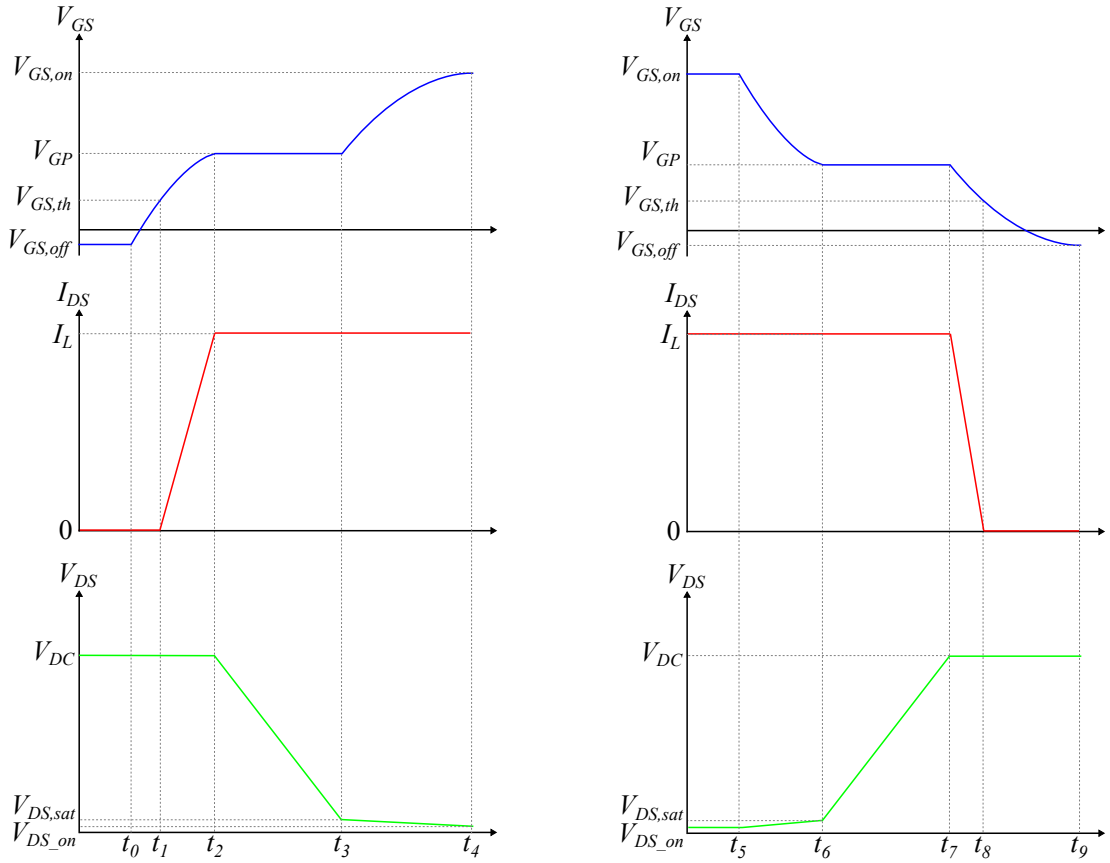
The turn on process of the SiC MOSFET is presented in Fig. 2.7a. It can be divided into four stages.

Stage 1: turn-on delay ($t_0 \sim t_1$)

At t_0, the gate driver voltage V_G in Fig. 2.6 jumps from $V_{G,off}$ to $V_{G,on}$. The gate capacitances C_{GS} and C_{GD} are charged by the gate driver voltage. The SiC MOSFET keeps the off-state since V_{GS} is lower than the threshold voltage $V_{GS,th}$ at this stage. The current I_{DS} remains zero and the load current I_L flows through the freewheeling diode. V_{DS} is clamped to V_{DC} by the freewheeling diode. The charging waveform of V_{GS} and the turn-on delay time are determined by the time constant of the RC circuit formed by the gate resistor R_G and gate capacitances. This stage ends when V_{GS} is charged to $V_{GS,th}$.

Stage 2: current rising ($t_1 \sim t_2$)

At t_1, V_{GS} reaches $V_{GS,th}$. The SiC MOSFET starts to conduct current and I_{DS} begins to rise. I_L starts to commutate from the freewheeling diode to the SiC MOSFET. V_{DS} is still clamped by the freewheeling diode. The charging waveform of V_{GS} is still determined by the time constant of the RC circuit formed by the gate resistor R_G and gate capacitances. The waveform of I_{DS} is determined by V_{GS} according to the I-V characteristics as shown in Fig. 2.4. The current rising time is determined by the time constant of the RC circuit. This stage ends when



(a) Turn-on process.

(b) Turn-off process.

Figure 2.7: Switching process of the SiC MOSFET.

I_{DS} equals to I_L.

Stage 3: voltage falling ($t_2 \sim t_3$)

At t_2, I_L finishes its commutation from the freewheeling diode to the SiC MOSFET, and the freewheeling diode begins to block voltage. V_{GS} reaches the gate plateau voltage V_{GP}. The value of V_{GP} is determined by the I-V characteristics with $I_{DS} = I_L$ and $V_{DS} = V_{DC}$. At this stage, V_{DS} starts to fall by the discharging of C_{GD} and C_{DS}. The voltage falling time (i.e., the discharging time) and the V_{DS} waveform are determined by values of C_{GD} and C_{DS}. This stage ends when V_{DS} falls to the saturation voltage V_{DS_sat}.

Stage 4: remaining period ($t_3 \sim t_4$)

After t_3, V_{GS} continues to be charged from V_{GP} to $V_{G,on}$ and V_{DS} continues to fall to the on-state voltage V_{DS_on}. The charging waveform of V_{GS} is determined by the RC circuit formed by the gate resistor R_G and gate capacitances. V_{DS_on}

is determined by the I-V characteristics. This stage ends when V_{GS} is charged to $V_{G,on}$.

Turn-off Process:

The turn off process of the SiC MOSFET is presented in Fig. 2.7b. It can be divided into four stages.

Stage 1: turn-off delay ($t_5 \sim t_6$)

At t_5, the gate driver voltage V_G in Fig. 2.6 jumps from $V_{G,on}$ to $V_{G,off}$. The gate capacitances C_{GS} and C_{GD} are discharged by the gate driver voltage. The SiC MOSFET keeps the on-state since V_{GS} is higher than the threshold voltage $V_{GS,th}$ at this stage. The current I_{DS} remains I_L and V_{DS} equals to V_{DS_on}. The V_{GS} waveform and the turn-off delay time are determined by the time constant of the RC circuit formed by the gate resistor R_G and gate capacitances. This stage ends when V_{GS} is discharged to the gate plateau voltage V_{GP}.

Stage 2: voltage rising ($t_6 \sim t_7$)

At t_6, V_{GS} reaches V_{GP} and I_{DS} remains I_L. V_{DS} starts to rise by the charging of C_{GD} and C_{DS}. The voltage rising time (i.e., the charging time) and the V_{DS} waveform are determined by values of C_{GD} and C_{DS}. This stage ends when V_{DS} rises to the V_{DC}.

Stage 3: current falling ($t_7 \sim t_8$)

At this stage, V_{DS} remains V_{DC} and V_{GS} is discharged from V_{GP} to $V_{GS,th}$. I_{DS} falls from I_L to zero as V_{GS} decreases. The discharging waveform of V_{GS} and the current falling time are determined by the time constant of the RC circuit formed by the gate resistor R_G and gate capacitances. The I_{DS} waveform is determined by V_{GS} according to the I-V characteristics. This stage ends when I_{DS} falls to zero.

Stage 4: remaining period ($t_8 \sim t_9$)

After t_8, V_{GS} continues to be discharged from $V_{GS,th}$ to $V_{G,off}$. The discharging waveform of V_{GS} is determined by the RC circuit formed by the gate resistor R_G

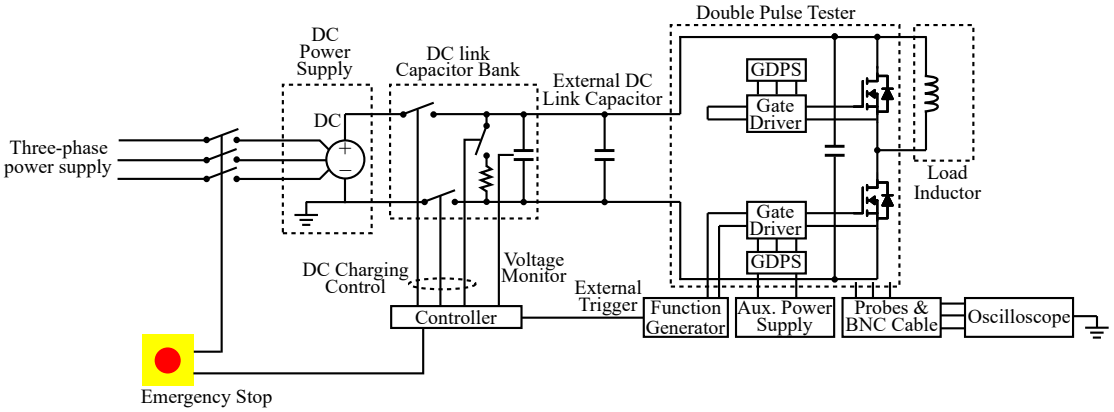


Figure 2.8: DPT setup.

and gate capacitances. This stage ends when V_{GS} is discharged to $V_{G,off}$.

Detailed analytical equations of the switching process have been provided in [53]. From the above analysis of turn-on and turn-off processes, it can be seen that the switching process of SiC MOSFETs is highly affected by the I-V characteristics and capacitances of the SiC MOSFET. Therefore, the I-V characteristics and capacitance characteristics need to be measured and modelled for transient simulation.

2.2 Characterisation of SiC MOSFETs

2.2.1 Dynamic Characterisation

Dynamic characterisation aims at measuring the switching waveforms of the SiC MOSFET to assess the dynamic performance of SiC MOSFETs including switching loss, switching transient parameters (e.g., switching time, dv/dt, di/dt), dynamic spikes (e.g., current/voltage overshoot), and parasitic ringing [54]. Besides, dynamic characterisation is a useful method to verify the simulation model of the SiC MOSFET by comparing the simulated switching waveforms to the measured switching waveforms [55].

The DPT is widely used to characterise the switching waveforms of the SiC MOSFET [56]. A DPT is the building block of most power electronics converters such as dc/dc buck converters, dc/dc boost converters, single phase inverters and

three-phase inverters, etc. Therefore, the DPT is one of the simplest circuits that can represent the operational environment of a real power electronics converter. A practical setup of DPT is presented in Fig. 2.8. In the setup of DPT, the PCB board needs to be carefully designed to reduce the parasitic inductance in both the gate driver loop and the power loop. Otherwise, oscillations or instability might be induced by large parasitic inductance [57]. The DPT circuit is shown in Fig. 2.6 and its operation principle is illustrated in Fig. 2.6b. During [t_0, t_1], the SiC MOSFET is turned on by the first pulse of the gate signal and the load current I_L is charged by DC bus voltage V_{DC} through the SiC MOSFET. This time interval is set to enable I_L to reach a target value. At t_1, the SiC MOSFET is turned off by the gate signal and the turn-off waveforms under the target load current and DC bus voltage can be measured during [t_1, t_2]. During [t_2, t_3], the SiC MOSFET keeps off-state and I_L flows through the freewheeling diode. This time interval needs to be short enough (typically 1-2 μs) to avoid significant reduction of I_L due to conduction loss. At t_3, the SiC MOSFET is turned on again by the second pulse of the gate signal. The turn-on waveforms under the target load current and DC bus voltage can be measured during [t_3, t_4]. During [t_4, t_5], the SiC MOSFET keeps on-state. This time interval need to be short enough (typically 1-2 μs) to avoid overcurrent and excessive conduction loss. During [t_5, t_6], the SiC MOSFET is turned off. A detailed design method of the DPT has been provided in [58].

Due to the fast switching speed of SiC MOSFETs, the challenges and instructions of the dynamic characterisation are highlighted according to literature review, including high-speed measurement and data processing:

High-speed Measurement

The measurement of the high-speed switching transients requires current and voltage probes with sufficient bandwidth to capture the fast rise and fall edges of the switching waveforms accurately [17].

For voltage measurement, in addition to high-bandwidth, galvanic isolation is

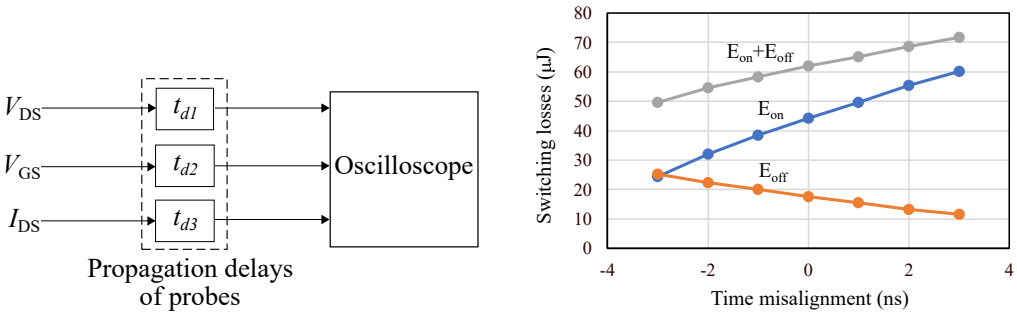
required if the dynamic characteristics of the high-side switch in a half-bridge leg configuration are measured [58]. There are two types of voltage probes usually used for voltage measurement in the literature: differential probes and passive probes [59]. Differential probes can provide useful galvanic isolation but have limited bandwidth [60]. Passive probes have high bandwidth but cannot provide galvanic isolation [61]. Tektronix recently announced the IsoVu Isolated Probe with both high bandwidth (up to 1 GHz) and galvanic isolation [62], which make it suitable for the voltage measurement of SiC MOSFETs.

For current measurement, high bandwidth and high accuracy are required. There are mainly three types of current probes in the literature: coaxial shunts, current transformer and Rogowski coil [63–65]. Coaxial shunt features high bandwidth and high accuracy, but has no galvanic isolation and requires pre-designed PCB layout for installing the coaxial shunts. Current transformer can provide high bandwidth and galvanic isolation, but it is not suitable for large current because its large physical size for large current measurement cannot fit in the circuit. The Rogowski coil can provide galvanic isolation but has limited bandwidth and accuracy. For dynamic characterisation using a DPT, the coaxial shunts are widely used for large current measurement with high bandwidth and high accuracy [66].

Data Processing

After switching waveforms are captured by an oscilloscope, post-processing of the measured data are required. Matlab is usually used to process the raw data and calculate the switching loss and switching time [67]. The Matlab code for automatic data processing has been developed in [54]. There are two critical issues in data processing: time alignment of waveforms and calculation of switching loss:

In practical measurement of switching waveforms, the probes used to measure the waveforms of V_{DS}, V_{GS} and I_{DS} have different propagation delays as shown in Fig. 2.9a. This causes the time misalignment of the measured waveforms. The time misalignment of V_{DS} and I_{DS} can cause significant errors in the calcu-



(a) Propagation delays of probes.

(b) Errors of switching loss due to time misalignment.

Figure 2.9: Time misalignment of dynamic characterisation.

lated switching loss of SiC MOSFETs as shown in Fig. 2.9b [68]. Therefore, the measured signals must be deskewed to compensate the time misalignment due to mismatched propagation delays between probes [69, 70].

The V_{DS} and V_{GS} waveforms can be calibrated by measuring the propagation delays of V_{DS} and V_{GS} probes. Two probes can be connected to the same reference source from the oscilloscope. The reference source generates periodical square waveform. Using one of the two probes as a baseline, the propagation delay of another probe can be compensated in the oscilloscope channel until the signals measured by two probes match. However, the same method cannot be used to calibrate the I_{DS} waveform because the current probe cannot be connected to the same reference source. Instead, a post-processing method was proposed in [71] to calibrate the V_{DS} and I_{DS} waveforms. It is based on the voltage drop due to the stray inductance during the turn-on transition. The current channel is adjusted until the initial drop of V_{DS} is graphically aligned to the calculated voltage drop of Ldi/dt on the oscilloscope.

Turn-on loss and turn-off loss of SiC MOSFETs can be easily calculated from the integral of $I_{DS} \times V_{DS}$ during the turn-on and turn-off transients:

$$E_{on} = \int_{on} I_{DS} V_{DS} dt \tag{2.4}$$

$$E_{off} = \int_{off} I_{DS} V_{DS} dt \tag{2.5}$$

Figure 2.10: The B1505A power device analyser/curve tracer [73].

However, it is found in [72] that the above equations are not accurate. During the turn off transient, a portion of measured I_{DS} is used to charge the output capacitance C_{oss} ($C_{oss} = C_{DS} + C_{GD}$) of the SiC MOSFET. Therefore, part of the energy calculated by (2.5) is actually stored in C_{oss} and is not dissipated. Therefore, this part of energy (namely, E_{oss}) cannot be accounted for the turn-off loss. Likewise, during the turn on transient, in addition to the turn-off loss calculated by (2.4), the energy E_{oss} stored in C_{oss} is also dissipated but is not measured. Therefore, the following equations need to be used to correctly calculate the switching loss:

$$E_{on} = \int_{on} I_{DS} V_{DS} dt + E_{oss} \tag{2.6}$$

$$E_{off} = \int_{off} I_{DS} V_{DS} dt - E_{oss} \tag{2.7}$$

2.2.2 I-V Characterisation

I-V characterisation measures the steady-state relationships between drain-source current I_{DS}, drain-source voltage V_{DS} and gate-source voltage V_{GS}. A curve tracer as shown in Fig. 2.10 is usually used by manufacturers to measure the I-V characteristics as presented in the datasheet [73]. The curve tracer applies pulsed V_{GS} and V_{DS} voltages to the SiC MOSFET and measures the I_{DS}. With a curve tracer setup, the timing of the V_{GS} and V_{DS} pulses must be precisely tuned to accurately capture steady state behaviour in the I-V characterisation [54]. There are

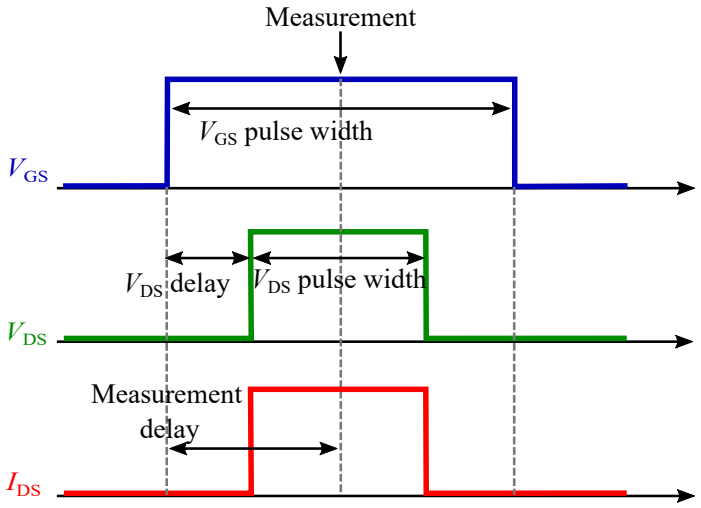
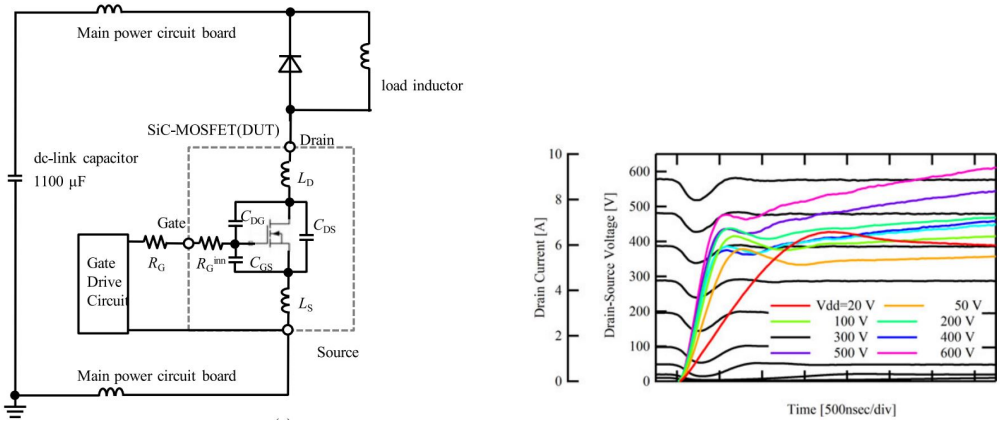


Figure 2.11: Pulsed waveforms and measurement timing for I-V characterisation.

five independent settings that should be considered in the pulse waveform timing: V_{GS} pulse width, V_{DS} pulse width, V_{DS} pulse delay, measurement delay, and pulse frequency. Fig. 2.11 shows the definitions of these terms. The V_{GS} pulse width, V_{DS} pulse width, V_{DS} pulse delay must be selected to avoid hard switching, which could impact the measurement or even cause damage to the device or equipment. The V_{DS} pulse must begin after the V_{GS} pulse, and only after the gate has had sufficient time to turn fully on. The V_{DS} and I_{DS} measurements can then be captured after a short measurement delay. Pulse frequency should be selected based on the potential for self-heating between pulses. There is no minimum frequency constraint, other than the experimenter's patience in waiting for a long sweep to finish. However, setting the frequency too high can cause thermal energy to gradually build up within the device, causing pulses later in the sweep to occur at higher temperature than earlier pulses. The final setting, measurement delay, can be more challenging to select. The measurement delay must be long enough so that V_{DS} has reached its steady state. However, the measurement delay cannot be too long to avoid significant self-heating. A measurement delay of about 100 μs is usually selected for the characterisation of SiC MOSFETs.

The I-V characteristics also have a strong junction temperature dependency [74]. Therefore, the I-V characterisation is usually performed under a fixed temperature. However, the curve tracer measures the I-V characteristics when the



(a) Schematic circuit diagram of a load-short-circuit-switching test.

(b) Experimental waveforms of V_{DS} and I_{DS} for V_{GS} of 7 V.

Figure 2.12: Load-short-circuit-switching test for I-V characterisation in high V_{DS} region [78].

SiC MOSFET is in on-state, which will generate conduction loss and cause self-heating, resulting in the rise of junction temperature. For I-V characterisation in low V_{DS} and low I_{DS} ranges, the low conduction loss causes negligible temperature rise and the impact of such a small temperature rise on the I-V characteristics can be ignored [75]. For I-V characterisation in high V_{DS} and high I_{DS} ranges, the large conduction loss can cause significant temperature rise, which will affect the results of I-V characterisation [76]. Besides, the temperature might exceed the safe operating area and damage the SiC MOSFET [77]. As a result, the V_{DS} range of the curve tracer for I-V characterisation is limited up to 40 V.

To measure the I-V characteristics in high-V_{DS} ranges (typically up to 800V for a 1200 V SiC MOSFET), many studies have been done in the literature [31,78,79].

In [78], a load-short-circuit-switching test is performed. Fig. 2.12a shows the test circuit. A wire of 50 cm is used as the load inductor between the drain terminal of the SiC MOSFET and the high-side DC bus, which can be treated as short circuit. When a positive V_{GS} above the threshold voltage is applied to the SiC MOSFET, the drain-source current I_{DS} will quickly increase to the saturation current due to the short circuit condition. Fig. 2.12b shows the experimental waveforms of V_{DS} and I_{DS} for V_{GS} of 7 V when the dc-bus voltage is varied from 20 to 600 V. The I-V characteristics can be extracted when the waveforms of V_{DS}

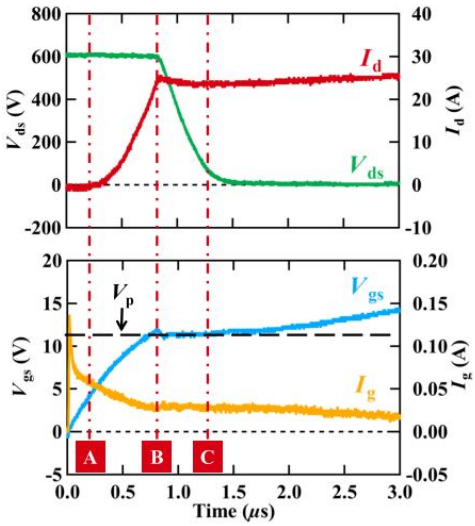


Figure 2.13: Turn-on waveforms of the SiC MOSFET for I-V characterisation in high V_{DS} region [31].

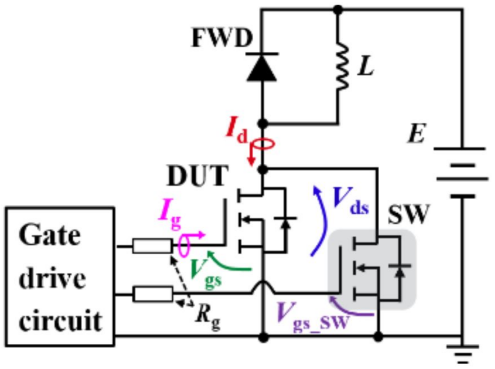


Figure 2.14: Modified DPT for I-V characterisation in high V_{DS} region [79].

recover to the dc-bus voltages and become stable. However, it can be observed in Fig. 2.12b that the waveforms of I_{DS} is not stable so that the accuracy of the measurement results are affected.

To improve the accuracy, a DPT-based measurement method is presented in [31]. The DPT shown in Fig. 2.6a is used for I-V characterisation in high V_{DS} region. A large gate resistor of 240 Ω is used in the gate driver to reduce the switching speed and oscillations so that the accuracy is improved. The turn-on waveforms of the SiC MOSFET can be obtained from the DPT as shown in Fig. 2.13 and the I-V characteristics under $V_{DS} = 600\,\text{V}$ and $I_{DS} = 25\,\text{A}$ can be extracted from Point B. It has been validated in [31] that the measured I-V characteristics can effectively improve the model accuracy of SiC MOSFETs for transient simulation. However, the self-heating caused by the operation of DPT in the presented DPT-based method is non-negligible for high current measurement, which will cause the rise of the junction temperature and induce errors to the measured I-V characteristics.

To reduce the self-heating of the DPT-based method, a modified DPT-based measurement method is presented in [79]. A modified DPT is proposed and shown

in Fig. 2.14. An additional switch is added in parallel with the device under test (DUT). By doing this, the charging current of load inductor in Fig. 2.14 can flow through the additional switch instead of the DUT. Therefore, there are no conduction loss and switching loss in the DUT during the charging stage the load inductor, resulting in a reduced self-heating of the DUT and thus more accurate I-V characterisation. The reduced self-heating can effectively improve the model accuracy. In average, the relative root-mean-square (RMS) error of the simulated switching waveforms is reduced from 12.3% to 7.8%.

Although the modified DPT-based measurement method presented in [79] can effectively reduce the self-heating of the SiC MOSFET for I-V characterisation in high V_{DS} region. However, this method requires an additional switch and complex gate driver circuit to drive the paralleled switches. Therefore, a simplified method for reducing the self-heating when measuring the I-V characteristics in high V_{DS} region need to be studied.

2.2.3 C-V Characterisation

The C-V characterisation measures the capacitances between any two terminals of the SiC MOSFET, including gate-source capacitance C_{GS}, drain-source capacitance C_{DS} and gate-drain capacitance C_{GD}. As is analysed in Section 2.1.4, these capacitances are variable capacitances depending on the bias voltages. Therefore, the capacitance-voltage relationships (i.e., C-V characteristics) need to be measured in the C-V characterisation step.

Although C_{GS}, C_{DS} and C_{GD} are straightforward to represent the physical origins of these capacitances between the three terminals of the SiC MOSFET, they are also often described using the following definitions [80]:

$$\begin{cases} C_{oss} = C_{DS} + C_{GD} \\ C_{iss} = C_{GS} + C_{GD} \\ C_{rss} = C_{GD} \end{cases} \tag{2.8}$$

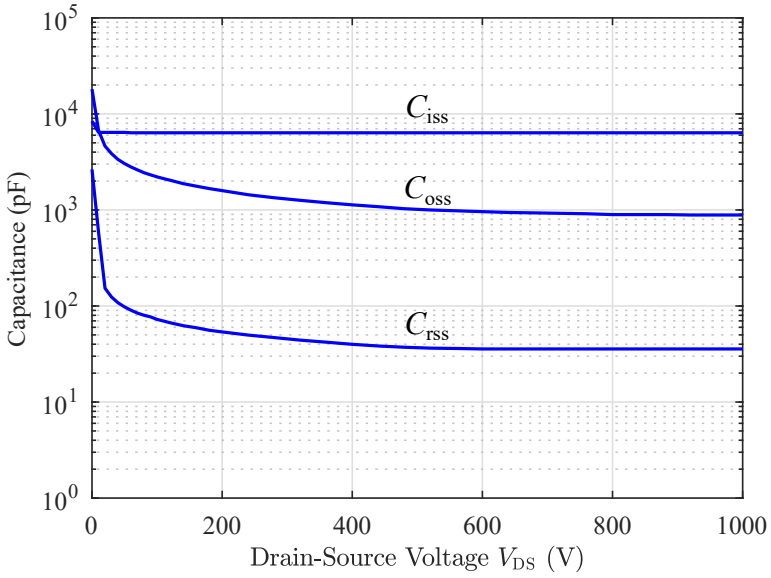


Figure 2.15: C-V characteristics of SiC MOSFET power module CAS120M12BM2 [43].

where C_{oss} is the output capacitance, representing the total capacitance seen at the drain terminal with the source and gate shorted together; C_{iss} is the input capacitance, representing the total capacitance seen at the gate terminal with the drain and source shorted together; C_{rss} is the reverse transfer capacitance, representing the capacitance seen between the gate and drain terminal with the source terminal floating.

The impedance analyser is the primary piece of equipment used for C-V characterisation [81]. Some curve tracers such as Keysight B1505A in Fig. 2.10 also have the same function as the impedance analyser for C-V characterisation [73]. The impedance analyser or the curve tracer measures the C_{oss}, C_{iss} and C_{rss} under DC bias voltage for V_{DS} from 0 V to 1000 V (for a 1200 V SiC MOSFET). The SiC MOSFET is kept off-state during measurement. The measured C-V characteristics based on the same method are often adopted by the SiC MOSFET manufacturers and provided in their device datasheets [12, 43, 82, 83]. An example obtained from the datasheet is presented in Fig. 2.15. The capacitances between terminals (i.e., C_{GS}, C_{DS} and C_{GD}) can be derived from the measured C_{oss}, C_{iss} and C_{rss} according to (2.8).

The conventional C-V characterisation method mentioned above only measures

the C-V characteristics in off-state under the bias voltage of V_{DS}. Many studies have been done in the literature to measure the additional C-V characteristics, which also have significant impact on the switching behaviour of SiC MOSFETs:

According to Fig. 2.15, the C_{GS}-V_{DS} characteristics measured by the conventional method is almost constant. However, according to the MOS structure of SiC MOSFETs, C_{GS} is a nonlinear capacitor that varies with the gate-source voltage V_{GS} [84]. In [32], the nonlinear C_{GS}-V_{GS} characteristics are measured by an LCR meter with V_{GS} of $[-15\,\mathrm{V}, 0\,\mathrm{V}]$. but the C_{GS}-V_{GS} characteristics with $V_{\mathrm{GS}} > 0\,\mathrm{V}$ are not measured. In [85], the C_{GS}-V_{GS} characteristics with V_{GS} of $[-15\,\mathrm{V}, -15\,\mathrm{V}]$ are measured by an LCR meter. It has been validated in [86] that the nonlinear C_{GS}-V_{GS} characteristics significantly the turn-on speed of the SiC MOSFET and thereby can improve the model accuracy.

As shown in Fig. 2.15, the gate-drain capacitance C_{GD} (i.e., C_{rss}) obtained from the conventional method is measured in the off-state (i.e., $V_{GS} = 0\,\mathrm{V}$). However, the C_{GD} characteristics during the on-state and dynamic switching transient are different with the off-state characteristics [31, 33, 78]. In [31], the S-parameter measurement method is introduced to obtain the on-state C_{GD} characteristics. It has been validated that the measured on-state C_{GD} characteristics can improve the model accuracy in the simulated turn-off waveforms. However, although S-parameter measurement has been widely used in radio frequency (RF) applications and can provide accurate results, they are still too complicated for power electronics designers, which requires a customised high-frequency-response evaluation board and an expensive vector network analyser (VNA). Besides, the S-parameter of the device package are required to extract the S-parameter of the bare die.

In addition to the on-state C_{GD} characteristics, it is investigated in [33] that the dynamic C_{GD} characteristics during the switching transient are also different with the off-state characteristics obtained from the conventional method. The dynamic charge Q_{GD} is measured by a gate charge evaluation circuit and the dynamic C_{GD} characteristics are derived from the measured Q_{GD} characteristics. It has been

validated in [33] that the SiC MOSFET model based on the measured dynamic C_{GD} characteristics can simulate the turn-on waveforms more accurately than the model based on the off-state C_{GS} characteristics in the datasheet.

In addition to the off-state C-V characteristics measured by the conventional method, it has been validated in the literature that the switching behaviour of SiC MOSFETs is influenced by the additional characteristics mentioned above, including nonlinear C_{GS}-V_{GS} characteristics, on-state C_{GD} characteristics and dynamic C_{GD} characteristics. Therefore, they are essential for the accurate modelling of SiC MOSFETs in transient simulation. Although various methods have been proposed in the literature to measure these additional characteristics, they require different measurement tools such as an LCR meter, a VNA and a gate charge measurement circuit, etc. As a result, it is very complicated and costly to measure all these characteristics. Therefore, a simplified measurement method to measure all these C-V characteristics need to be studied.

2.3 Modelling of SiC MOSFETs

2.3.1 Types of SiC MOSFET Models

Many modelling methods of SiC MOSFETs have been reported in previous literature and a review of SiC MOSFET models has been presented in [87]. The available modelling methods are for either physics-based, numerical or behavioural models. Among them, physics-based and numerical models can provide accurate simulation results based-on detailed semiconductor physics such as the carrier transportation in the channel and n^- drift region [88, 89]. Physics-based and numerical models are built based on the device geometry such as the channel length and width, the thickness of the gate oxide layer and n^- drift region, doping concentration of different regions, etc [90]. Therefore, the model built for one device can be extended to another device with different current or voltage levels by adjusting the physical parameters of the model [91]. But these models are complex and

have slow computation speed so are not suitable for transient simulation. Also, the information of device geometry is usually not available to users [92]. As a result, they are mostly used at the design stage of SiC MOSFETs by the device manufacturers [93]. Instead, behavioural models are widely used in transient circuit simulation due to their simplicity and fast computation speed [94], which is therefore the focus of this thesis.

2.3.2 Behavioural Modelling of SiC MOSFETs

Most existing behavioural models are based on the equivalent circuit model of the SiC MOSFET [95]. The on resistance and capacitances within the SiC MOSFET are presented in Fig. 2.16, which is a combination of Fig. 2.3b and Fig. 2.5. The equivalent circuit model of the SiC MOSFET can be derived from Fig. 2.16 [96].

As shown in Fig. 2.17, the equivalent circuit of the SiC MOSFET consists of the voltage-controlled current source I_{DS}, the gate-source capacitor C_{GS}, the gate-drain capacitor C_{GD}, the drain-source capacitor C_{DS}, the internal gate resistor R_G, and the body diode or anti-parallel Schottky diode D. The voltage-controlled current source I_{DS} is used to model the nonlinear on-resistance of the SiC MOSFET, i.e., the I-V characteristics. The current source I_{DS}, capacitors and diode are all nonlinear component, which are modelled by mathematical equations to match the device characteristics, such as I-V and C-V characteristics [97]. Complex nonlinear equations are firstly designed according to the device characteristics. Afterwards, the equation parameters are extracted using mathematical curve fitting methods [96].

Based on the sources of the device characteristics used for the model, the behavioural modelling methods can be categorised into two groups: the measurement-based modelling methods and the datasheet-based modelling methods:

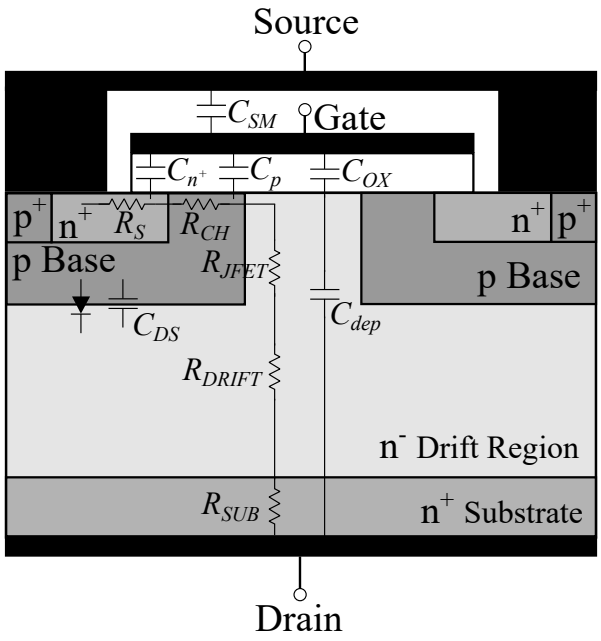


Figure 2.16: On resistance and capacitances within the SiC MOSFETs.

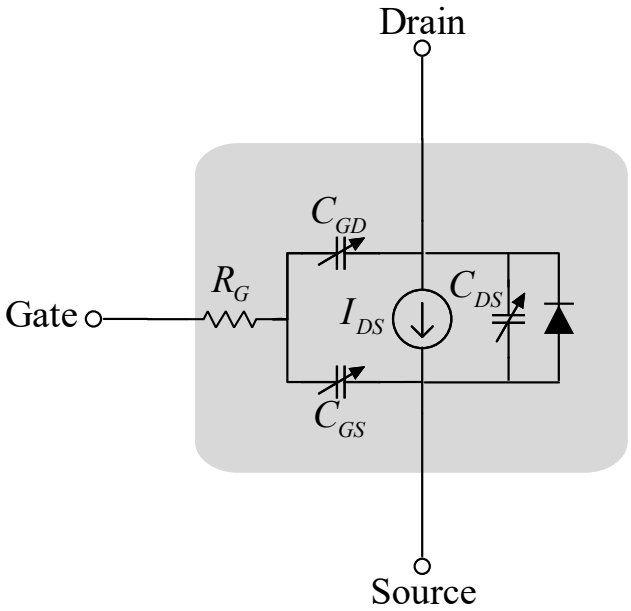


Figure 2.17: Equivalent circuit model of the SiC MOSFET.

Measurement-based behavioural modelling methods

The measurement-based modelling methods utilise measured device characteristics to model the SiC MOSFETs. In addition to the characteristics provided in the datasheet, additional characteristics presented in Section 2.2 can be measured to improve the model accuracy. These characteristics include I-V characteristics in high V_{DS} region, nonlinear C_{GS} characteristics, on-state C_{GD} characteristics and dynamic C_{GD} characteristics.

In [31], the I-V characteristics in high V_{DS} region and on-state C_{GD} characteristics are measured as additional characteristics to improve the model accuracy of the SiC MOSFET in transient simulation. To model these additional characteristics, a commercial Angelov model is modified accordingly [98]. In [78] and [33], the I-V characteristics in high V_{DS} region and the dynamic C_{GD} characteristics are measured for their models with modified equations. In [86], the nonlinear C_{GS} characteristics are measured and a new equation for C_{GS} is added in the original model. All the above measurement-based models have shown promising improvement of accuracy in transient simulation. However, none of them has considered all the additional I-V and C-V characteristics presented in Section 2.2 in their models.

In the existing literature, most existing behavioural models are implemented using mathematical equations to match the measured device characteristics. To accurately model these additional characteristics, either the original equations need to be modified or new equations need to be added. The design of these mathematical equations is a very complicated process. For example, some behavioural models like the Angelov model [98] have more than 80 parameters. Also, it is very difficult to extract these parameters even for users with expert experience. The parameter extraction method for the models provided by many manufacturers is not publicly available. To overcome this problem, a commercially available parameter extraction tool IC-CAP has been developed and based on Levenberg-Marquardt algorithm to automatically extract the parameters in the equations

to match the measured characteristics [99, 100]. However, the automatically extracted parameters are not be accurate enough and the parameters often need to be manually tuned, which is time-consuming and requires expert experience. In addition, the equations designed for the behavioural models often have limited generality due to the lack of physical information. Therefore, if behavioural models built for one device are used to model another device with different current or voltage levels, parameters of the models need to be extracted again based on device characteristics.

A new behavioural modelling algorithm based on artificial intelligence (AIs) has been proposed in [101–103] which aimed to give a simple and fast data-driven method. Thanks to the data-driven approach, such AI-based models can potentially overcome the aforementioned challenges of the conventional behavioural modelling methods. Complex equation design is avoided and the AI parameters can be extracted easily and automatically by training the AI using many well-developed toolboxes such as the Neural Net Fitting Toolbox in MATLAB. In addition, AIs have good adaptability to model SiC MOSFETs with different characteristics because they can approximate any mathematical functions [104]. However, the existing AI-based modelling methods are only suitable for static simulation but not for transient simulation due to the insufficient training dataset and inaccurate data-driven model. An AI-based model suitable for transient simulation need to be studied. Besides, AI-based modelling methods have two limitations. Firstly, they have poor extrapolation capability. Therefore, the training data that covers the whole operating range of the SiC MOSFETs must be measured. Secondly, they cannot accurately represent the physical behaviour of SiC MOSFETs such as the cut-off region. Therefore, the hybrid modelling method that incorporate AI models with behaviour-based equations is needed to overcome this drawback.

Datasheet-based behavioural modelling methods

The datasheet-based modelling method only utilise the characteristics obtained from the datasheet to model the SiC MOSFET [105]. Although the measurement-based modelling methods can provide accurate SiC MOSFET models based on the measured complete characteristics of SiC MOSFETs. However, additional measurement equipment and test circuits are required for these modelling methods, which might not be available for converter designers. From this perspective, a datasheet-based modelling approach without additional experimental measurements is preferred because it can be adopted by all designers [106].

A datasheet-based SiC MOSFET model is proposed in [107] with wide temperature range. Another accurate subcircuit model of SiC half-bridge modules is proposed in [49] for switching-loss optimization based on datasheet. However, both models used segmented capacitance models which might bring convergence problem [94]. To solve the convergence problem, a non-segmented model is proposed in [96]. In [108], the non-segmented model is extended to consider the third-quadrant *I-V* characteristics of SiC MOSFETs. Besides the models specifically designed for SiC MOSFETs, in [109] and [110], universal datasheet-based models are proposed for both SiC MOSFETs and GaN HEMTs.

The datasheet-based models usually contain complicated nonlinear equations and multiple parameters to accurately model the current and capacitance characteristics. Although the same model can be used for different SiC MOSFETs, the parameters in the model are distinct. Therefore, the model parameters should be extracted based on the datasheet of specific SiC MOSFETs. Although there are various models in the literature, the parameter extraction procedure of these models are either too complicated or not well-established, which hinders the application of the datasheet-based models for converter designers. Therefore, a detailed parameter extraction procedure for datasheet-based modelling methods need to be studied.

Both measurement-based models and datasheet-based models have been pro-

posed in the literature. However, there is a lack of comparison between these two types of models. A comprehensive comparison between datasheet-based models and measurement-based models need to be studied to provide a guidance for users to identify the suitable method for their own applications.

2.4 Summary

From the review of the operation principle of SiC MOSFETs, the physical origins of the on resistance and capacitances within the SiC MOSFET are identified. The analysis shows that the switching behaviour of the SiC MOSFETs is determined by the I-V characteristics (i.e., on resistance) and capacitances, which need to be characterised and modelled for transient simulation.

The I-V characterisation faces the challenge to measure the I-V characteristics in high V_{DS} region. The existing methods either present inaccurate results due to self-heating or require complicate measurement circuit. Therefore, a simplified measurement method with reduced self-heating need to be studied. The existing C-V characterisation methods are also too complicated, which requires different equipment to measure all required characteristics. A unified I-V and C-V characterisation method to simplify the measurement process need to be studied.

The modelling of SiC MOSFETs for transient simulation is another important aspect. For measurement-based modelling methods, an AI-based model suitable for transient simulation need to be studied to address the existing challenges of equation-based models, such as complex equation design, difficult parameter extraction, poor model adaptability, etc. For datasheet-based modelling methods, a detailed parameter extraction procedure need to be studied. Besides, there is a lack of comprehensive comparison between datasheet-based models and measurement-based models to identify their respective usage.

The research work in this thesis investigated the above challenges and proposed relevant solutions. A simplified I-V and C-V characterisation method was

proposed, which can simply extract all the dynamic-state I-V and C-V characteristics from the switching waveforms measured by a DPT. In this way, multiple measurement equipment and complex measurement process can be avoided. A hybrid data-driven modelling method was proposed as a new candidate of the measurement-based modelling methods for transient simulation to simplify the modelling process and improve the accuracy. A step-by-step datasheet-based modelling method was proposed and compared to the proposed measurement-based modelling method to provide a guidance for converter designers to identify suitable modelling methods for their own applications.

Chapter 3

Simplified Characterisation of SiC MOSFETs

In this chapter, the conventional static-state I-V and C-V characterisation methods are firstly introduced. Their inadequacy is analysed and the necessity of measuring the I-V and C-V characteristics in dynamic state for accurate modelling is presented. This chapter proposes a simplified characterisation method which can extract the dynamic-state I-V and C-V characteristics from the switching waveforms measured by the double pulse tester. These characteristics include the I-V characteristics in the high V_{DS} region, the nonlinear gate-source capacitance characteristics, the on-state and dynamic gate-drain capacitance characteristics. The proposed measurement method was established by analysing the relationship of these characteristics with the switching waveforms of SiC MOSFETs.

3.1 Introduction

The behavioural model is usually built based on the equivalent circuit of SiC MOSFETs [49]. As shown in Fig. 2.17, the equivalent circuit of the SiC MOSFET consists of the voltage-controlled current source I_{DS}, the gate-source capacitor C_{GS}, the gate-drain capacitor C_{GD}, the drain-source capacitor C_{DS}, the internal gate resistor R_G, and the body diode or anti-parallel Schottky diode D. The

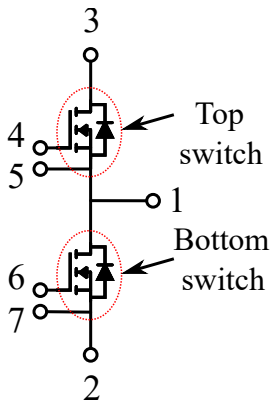


Figure 3.1: Half-bridge configuration of SiC power module CAS120M12BM2.

characteristics of each component in the equivalent circuit need to be obtained to model the SiC MOSFET accurately. The gate resistor and diode characteristics can be measured by a curve tracer. The I-V and C-V characteristics need to be measured firstly to model the channel current I_{DS} and parasitic capacitors (C_{GS}, C_{GD} and C_{DS}). An 1200V 120A SiC MOSFET power module CAS120M12BM2 [43] from Wolfspeed was selected to demonstrate the characterisation methods. The characteristics of the bottom SiC MOSFET in the power module as shown in Fig. 3.1 were measured.

The I-V and C-V characteristics of SiC MOSFETs have significant impact on the dynamic switching behaviour of SiC MOSFETs [46]. Therefore, accurate I-V and C-V characterisation is required for transient simulation models. However, many conventional characterisation methods in the literature only measure the I-V characteristics in static state with a voltage range far less than the actual blocking voltage of SiC MOSFETs. Besides, the C-V characteristics measured by many conventional methods only focus on static off-state relationship between the parasitic capacitances and the drain-source voltage. The datasheets and models provided by most manufacturers also only consider the static-state I-V and C-V characteristics. These characteristics are insufficient to accurately model the switching behaviour of SiC MOSFETs in transient simulation [111].

In addition to the conventionally-measured I-V and C-V characteristics in static state, it has been found in the literature that the I-V and C-V character-

istics in dynamic state have great impact on the accuracy of the model. Although various measurement methods have been proposed in the literature to measure these dynamic-state characteristics, these methods require many different measurement tools to measure all the required characteristics. Therefore, it is very complicated and costly for accurate device modelling using existing measurement methods.

In this chapter, a double-pulse-tester-based characterisation method was proposed to measure the I-V and C-V characteristics in dynamic state to simplify the measurement process. Although the measurement is simplified, the I-V and C-V characteristics measured by the proposed method can effectively improve the model accuracy. These dynamic-state characteristics include the I-V characteristics in the high V_{DS} region, the nonlinear gate-source capacitance characteristics, the on-state and dynamic gate-drain capacitance characteristics. The proposed method was established by analysing the relationship between these characteristics and the switching process. Compared to the existing methods to measure these dynamic-state characteristics, the proposed method has the following two contributions:

1. The relation of the dynamic-state I-V and C-V characteristics with the switching waveforms of SiC MOSFETs was analysed in detail. Based on the analysis, the proposed method can directly extract the dynamic-state I-V and C-V characteristics from the switching waveforms measured by a double pulse tester (DPT) to simplify the measurement process.

2. The proposed method reduces the self-heating of the SiC MOSFET when measuring the I-V characteristics in the high-voltage high-current ranges so that the errors induced by the increased junction temperature are reduced.

The rest of this chapter is organised as follows: Section 3.2 introduces the details of the conventional I-V and C-V characterisation methods in static state. The insufficiency of the conventional static-state methods and complexity of existing

dynamic-state methods are illustrated in Section 3.3. In Section 3.4, the DPT-based measurement method of the I-V characteristics in the high V_{DS} region is presented. Section 3.5 presents the proposed measurement method of the nonlinear C_{GS} characteristics. Section 3.6 presents the the proposed measurement method of the on-state and dynamic C_{GD} characteristics. The conclusions are summarised in Section 3.7.

3.2 Conventional Static-state I-V and C-V Characterisation

Conventionally, the I-V characteristics of SiC MOSFETs are usually measured in static state by a curve tracer to obtain the drain-source current I_{DS} under various gate-source voltages V_{GS} and drain-source voltages V_{DS}. The C-V characteristics are usually measured in static off-state by an impedance analyser or an LCR meter [54]. In this chapter, the conventional static-state I-V and C-V characterisation methods are demonstrated by using a Keysight B1505A power device analyser which combines the functions of a curve tracer and an impedance analyser [73].

3.2.1 Conventional Static-state I-V Characterisation

The simplified circuit to measure the I-V characteristics, including the I_{DS}-V_{DS} characteristics (i.e., output characteristics) and the I_{DS}-V_{GS} characteristics (i.e., transfer characteristics), is shown in Fig. 3.2. By applying certain V_{DS} and V_{GS}, the corresponding I_{DS} can be measured by a current meter. The I_{DS}-V_{DS} characteristics measure the drain current I_{DS} by sweeping the drain voltage V_{DS}, while the gate voltage V_{GS} is fixed. The I_{DS}-V_{DS} characteristics can be measured under different gate voltages. The I-V characteristics of a SiC MOSFET power module CAS120M12BM2 from Wolfspeed were measured in this thesis. The measurement was performed with V_{DS} between [0, 40] V in steps of 0.8 V and V_{GS} between [0, 20] V in steps of 1 V. The I_{DS}-V_{GS} characteristics measure I_{DS} by sweeping V_{GS},

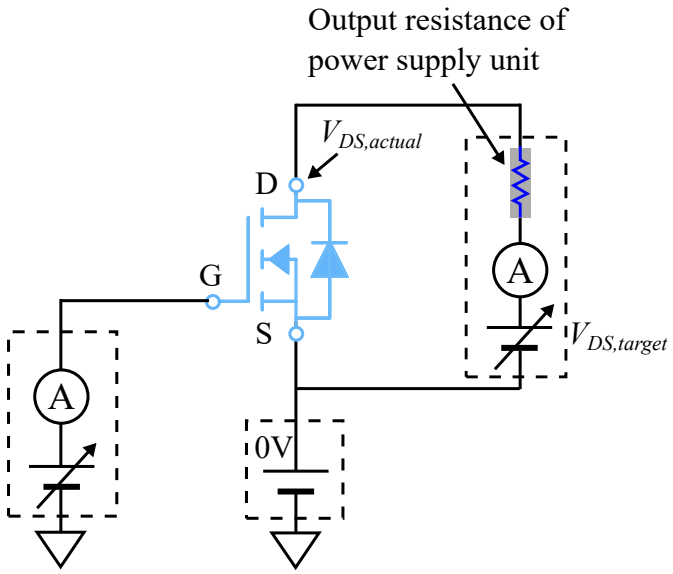
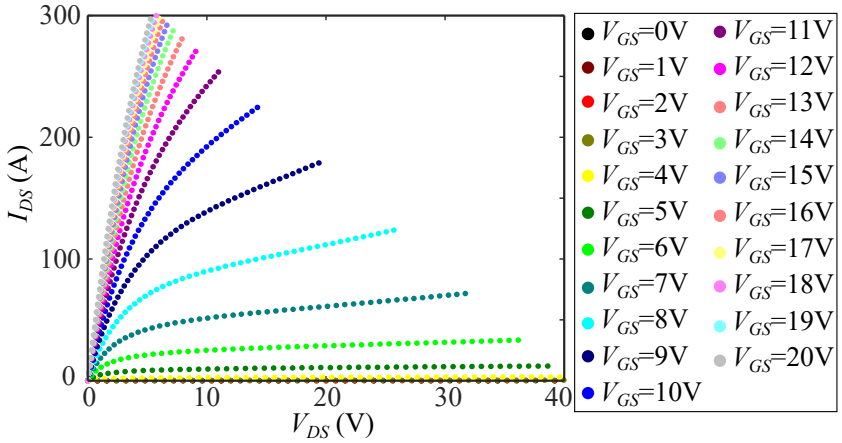


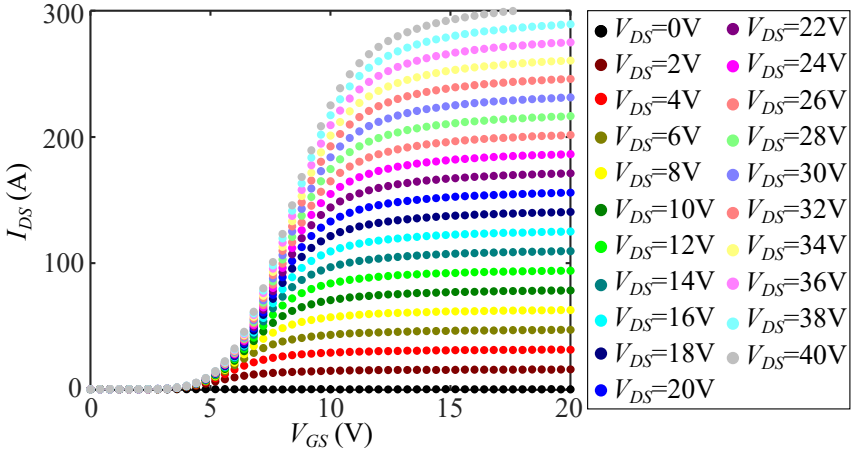
Figure 3.2: Configuration of a B1505A curve tracer to measure I-V characteristics.

while V_{DS} is fixed. The I_{DS}-V_{GS} characteristics can be measured under different drain voltages. In this study, the measurement was performed with V_{GS} between [0, 20] V in a step of 0.4 V and V_{DS} between [0, 40] V in a step of 2 V. The circuit to measure the I-V characteristics using the B1505A curve tracer is shown in Fig. 3.2. It should be noticed that the power supply unit connected to the drain and source terminals of the SiC MOSFET has the output resistance of around 120 mΩ. Due to the voltage drop across this resistance, the actual drain voltage applied to the SiC MOSFET is lower than the targeted drain voltage. Therefore, it was necessary to measure the actual drain voltage via a Kelvin connection. Due to the limited power rating of the curve tracer and self heating of the device under test [31], the I-V characteristics can only be measured in the low V_{DS} region. For example, the Keysight B1505A curve tracer can only measure the I-V characteristics with $V_{DS} < 40$ V as shown in Fig. 3.3a [73].

The I-V characteristics of the SiC MOSFET power module CAS120M12BM2 were measured at the room temperature 25 °C. The measured I_{DS}-V_{DS} and I_{DS}-V_{GS} characteristics are shown in Fig. 3.3a and Fig. 3.3b, respectively. The I_{DS}-V_{DS} characteristics in Fig. 3.3a show the cut-off, ohmic and saturation regions of the SiC MOSFET [48]. When V_{GS} is below the threshold voltage V_{th}, the SiC



(a) I_{DS}-V_{DS} characteristics.



(b) I_{DS}-V_{GS} characteristics.

Figure 3.3: I-V characteristics of SiC power module CAS120M12BM2 at 25 °C.

MOSFET operates at cut-off region and $I_{DS} \approx 0\,\text{A}$. When V_{GS} is above V_{th} and V_{DS} is below $V_{GS} - V_{th}$, the SiC MOSFET operates at the ohmic region and I_{DS} is approximately proportional to V_{DS}. When V_{GS} is above V_{th} and V_{DS} is above $V_{GS} - V_{th}$, the SiC MOSFET operates at the saturation region and I_{DS} increases with V_{DS} due to the short channel effect [112], but the slope is much smaller compared to the ohmic region.

3.2.2 Conventional Static-state C-V Characterisation

As is mentioned in Section 2.1.4, parasitic capacitances C_{GS}, C_{GD} and C_{DS} are formed within the SiC MOSFET between any two terminals. They are more often measured as the output capacitance C_{oss}, the input capacitance C_{iss} and the

reverse transfer capacitance C_{rss}:

$$\begin{cases} C_{oss} = C_{DS} + C_{GD} \\ C_{iss} = C_{GS} + C_{GD} \\ C_{rss} = C_{GD} \end{cases} \tag{3.1}$$

Fig. 3.4 shows the test setups and AC equivalent circuits of the conventional C-V characterisation based on Keysight B1505A [73]. High frequency AC signal (1 MHz) is applied to the terminals of the SiC MOSFET to measure the complex impedance of the equivalent circuits. The capacitance of interest can then be derived from the measured impedance. To measure the bias-dependent C-V characteristics, DC bias voltage is applied to the drain terminal of the SiC MOSFET. For the power module CAS120M12BM2 rated at 1200 V, the bias voltage from 0 V to 1000 V is selected. In these circuits as shown in Fig. 3.4, C_1 and C_2 are relatively large capacitances (1 μF) which can be treated as AC shorts but DC open-circuits. Therefore, the high DC bias voltage can be applied to the drain terminal but blocked from the equipment. Besides, since the parasitic capacitances of SiC MOSFETs are typically in the pF range, the impedance of C_1 and C_2 only causes an error of 0.1% or less and can thereby be ignored [54].

The reverse transfer capacitance C_{rss} (i.e. C_{GD}) is measured in a different way compared to C_{oss} and C_{iss}. To avoid C_{GS} and C_{DS} in parallel with C_{GD} during the measurement, the source terminal of the SiC MOSFET is connected to the AC Guard terminal of B1505A. The AC Guard is the internal common ground of B1505A. Therefore, the AC current from C_{GS} and C_{DS} directly flows through the AC Guard and is not detected by the current meter so that it does not affect the measured impedance of C_{GD}.

The C-V characteristics of the SiC MOSFET power module CAS120M12BM2 were measured as shown in Fig. 3.5. It can be seen that both C_{oss} and C_{rss} are highly nonlinear with respect to drain voltage V_{DS} and their values decrease when

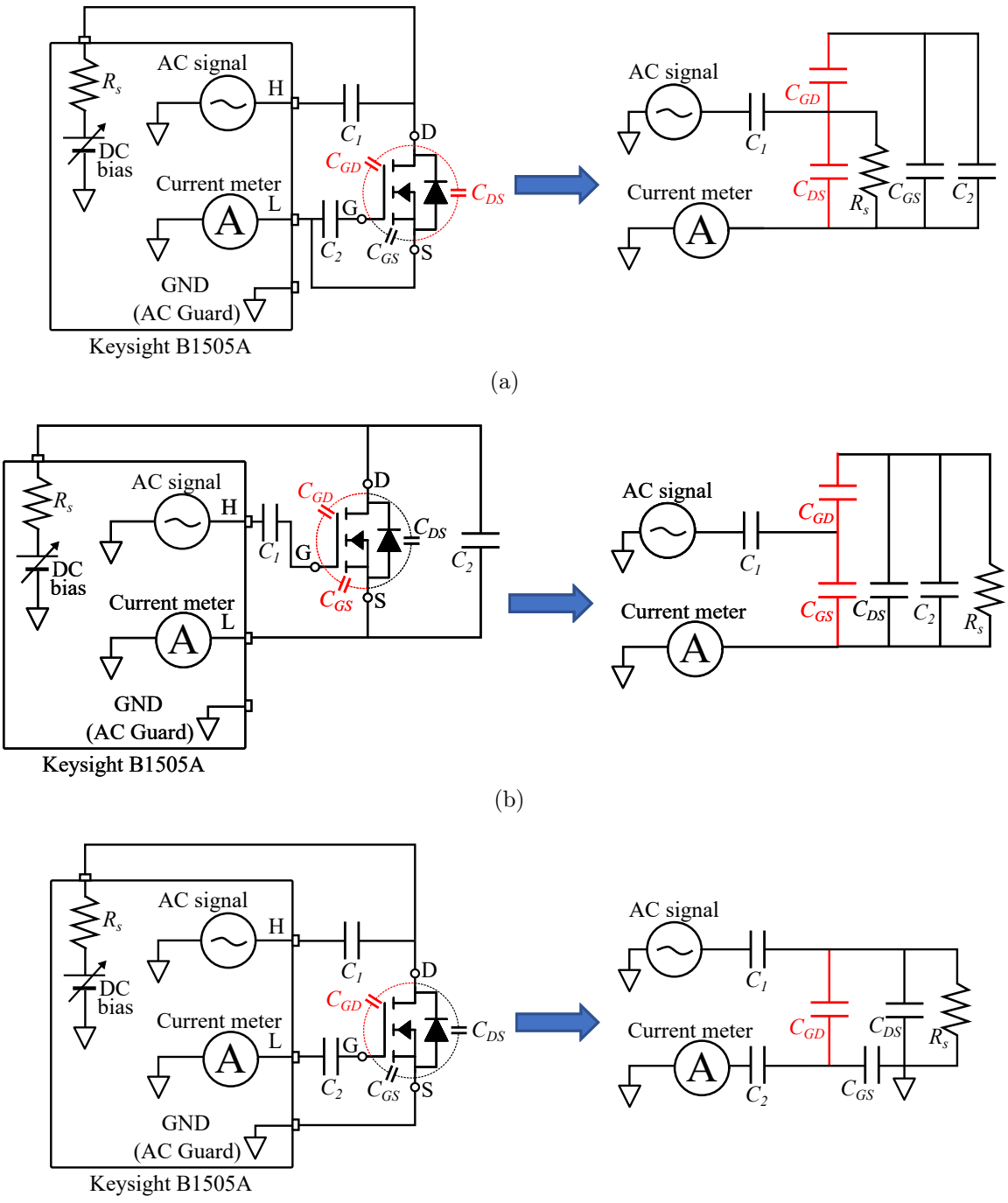


Figure 3.4: Test setups and AC equivalent circuits of the conventional C-V characterisation using Keysight B1505A. (a) Output capacitance C_{oss}, (b) input capacitance C_{iss}, and (c) reverse transfer capacitance C_{rss} [73].

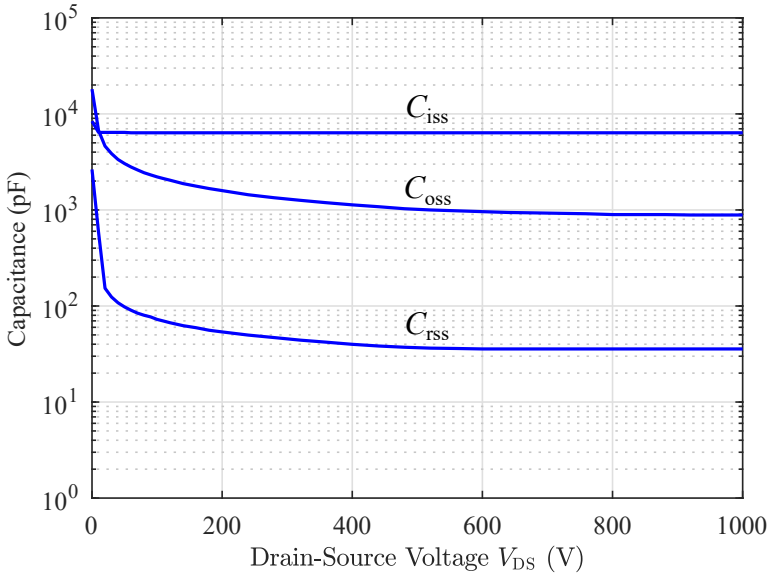


Figure 3.5: C-V characteristics of SiC MOSFET power module CAS120M12BM2.

V_{DS} increases. Compared to C_{oss} and C_{rss}, the C_{iss} curve is typically very flat except a small drop in the low voltage range.

3.3 Insufficiency of Conventional Static-state Methods and Research Motivation

Although the static-state I-V and C-V characteristics can be measured by the conventional methods presented above, additional dynamic-state characteristics are required to accurately simulate the transient behaviour of the SiC MOSFET.

3.3.1 Additional Dynamic-state Characteristics

I-V characteristics in high V_{DS} region

As shown in Fig. 3.3b and Fig. 3.3a, only the I_{DS}-V_{DS} characteristics in low-voltage low-current ranges ($V_{DS} < 40\,\text{V}$) are measured by the conventional static-state method. However, it has recently been found that the I_{DS}-V_{DS} characteristics in high V_{DS} region heavily affects switching behaviours of the SiC MOSFET [78] since it uses the whole V_{DS} region from 0 V to the maximum DC voltage (>600 V in this chapter) during switching transients. Due to the short-channel effect of SiC

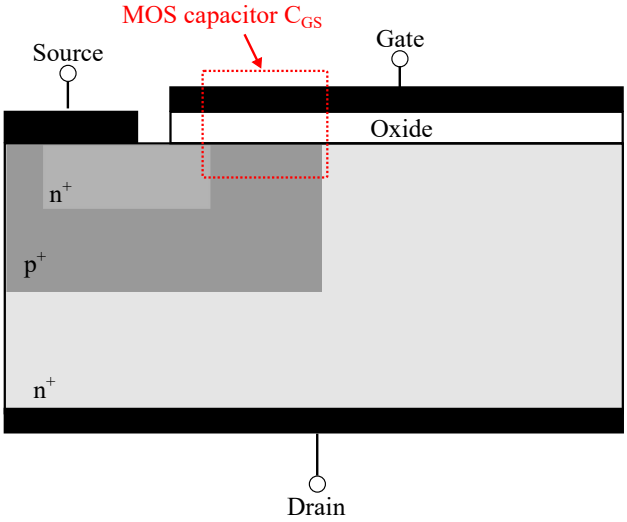
MOSFETs, the saturated drain current I_{DS} increases with V_{DS} in the high V_{DS} region [112]. However, the conventional curve tracer cannot be used to measure the I-V characteristics in the high V_{DS} region due to the limited power rating of the curve tracer and huge self-heating of the SiC MOSFET, which might damage the equipment and the device. As a result, the I-V characteristics in the high V_{DS} region can only be measured in dynamic state instead of static state.

Nonlinear C_{GS} characteristics

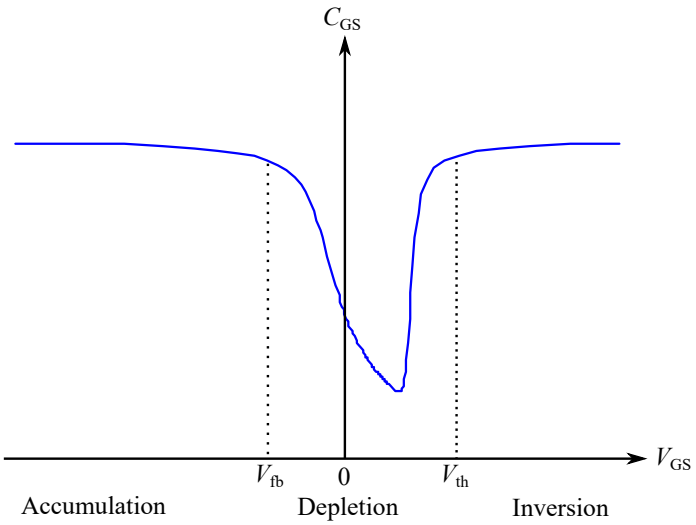
In the conventional static-state measurement, the C_{GS} characteristics are measured in static off-state with $V_{GS} = 0$ V. As a result, only the capacitance characteristics versus V_{DS} from 0 V to 1000 V are measured. It is shown in Fig. 3.5 that C_{GS} is almost constant with V_{DS}. However, during the dynamic switching transient, V_{GS} varies from turn-off gate voltage (< 0 V) to turn-on gate voltage (> 15 V). According to the metal-oxide-semiconductor (MOS) structure of SiC MOSFETs as shown in Fig. 3.6a, C_{GS} is a nonlinear capacitor that varies with the gate-source voltage V_{GS} as shown in Fig. 3.6b [113]. Therefore, the C_{GS}-V_{GS} characteristics need to be measured in dynamic state to model the SiC MOSFETs.

On-state and dynamic C_{GD} characteristics

C_{GD} is a nonlinear capacitor that varies with the drain-gate voltage V_{DG}. In the conventional method, the static off-state C_{GD}-V_{DS} characteristics are measured with $V_{GS} = 0$ V (i.e. V_{DG}=V_{DS}). Therefore, the C_{GD} characteristics versus V_{DG} from 0 V to 1000 V in the off state ($V_{GS} = 0$ V) can be characterised by the conventional method. However, during the dynamic switching transient, SiC MOSFETs switch from on-state to off-state and vice versa. In the on state of the SiC MOSFET, the on-state gate-source voltage V_{GS} is usually set as high as 20 V for CAS120M12BM2 to reduce the on-state resistance and the on-state drain-source voltage is lower than 3 V depending on the conduction current. Therefore,



(a) MOS structure of gate-source capacitor C_{GS}.



(b) Theoretical C_{GS}-V_{GS} characteristics [113].

Figure 3.6: MOS structure and characteristics of gate-source capacitor C_{GS}.

a negative V_{DG} is applied to C_{GD} in the on state. The C_{GD} characteristics with $V_{DG} < 0$ are not measured by the conventional static-state method, which is required for accurate device modelling. In addition to the on-state C_{GD} characteristics, it is investigated in [33] that the dynamic C_{GD} characteristics during the switching transient are different with the off-state characteristics. Therefore, the dynamic C_{GD} characteristics need to be measured to improve the model accuracy.

3.3.2 Motivation of the Proposed DPT-based Method

Various measurement methods have been proposed in the literature to measure these dynamic-state characteristics mentioned above. For example, switching-based measurement methods based on double pulse testers (DPTs) have been reported to measure the I-V characteristics in the high V_{DS} region, which greatly reduces the conduction time of the MOSFETs to reduce self-heating [31, 76, 114]. Nevertheless, these methods still exhibit non-negligible self-heating caused by the significant switching losses when the rated current of the MOSFET is high. In [32], the nonlinear C_{GS}-V_{GS} characteristics are measured by an LCR meter with V_{GS} of $[-15\,\mathrm{V}, 0\,\mathrm{V}]$, but the C_{GS}-V_{GS} characteristics with $V_{GS} > 0\,\mathrm{V}$ are not measured. S-parameter measurement with the vector network analyser (VNA) is presented in [31] for on-state C_{GD} characterisation and the gate charge measurement circuit is presented in [33] for dynamic C_{GD} characterisation. However, the proposed S-parameter measurement method is complicated, which requires a customised high-frequency-response evaluation board and an expensive VNA.

Besides the limitations of the existing methods, these methods require different measurement tools such as DPT, LCR meter, VNA and gate charge measurement circuit. Therefore, it is very complicated and costly to measure all these characteristics for accurate device modelling.

To address the above challenges, a DPT-based measurement method is proposed to measure all these dynamic-state characteristics mentioned above, including the I-V characteristics in the high V_{DS} region, the nonlinear C_{GS}-V_{GS} characteristics, the on-state and dynamic C_{GD} characteristics. These additional characteristics can be used as the complements of the conventionally-measured static-state I-V and C-V characteristics to improve the model accuracy of SiC MOSFETs. The proposed method was established by analysing the relation between these characteristics and the switching process to simplify the measurement process. Based on the analysis, the dynamic-state I-V and C-V characteristics can be directly extracted from the switching waveforms measured by a DPT. Because

the proposed method only requires a DPT which is commonly used by power electronics designers and can be built easily at low cost, the proposed measurement method can be widely adopted to improve the simulation accuracy of SiC MOSFETs in power electronics converter for power losses and EMI analysis.

3.3.3 Setup of the DPT

A DPT was set up to measure the I-V characteristics in the high V_{DS} region, the nonlinear C_{GS} characteristics, on-state and dynamic C_{GS} characteristics. The circuit diagram of the DPT is presented in Fig. 3.7. The switching waveforms of the bottom SiC MOSFET in CAS120M12BM2 was measured by the Oscilloscope, including the drain-source voltage, drain-source current, gate-source voltage and gate current. The gate current I_G cannot be measured directly. It was obtained by measuring the voltage drop on the gate driver resistor. Due to the existence of the internal gate resistance R_G in the subcircuit model of SiC MOSFET as shown in Fig. 2.17, the gate-source voltage V_{GS} on C_{GS} cannot be directly measured. Instead, the external gate-source voltage V'_{GS} was measured as shown in Fig. 3.7. V_{GS} can be calculated as follows:

$$V_{GS} = V'_{GS} - R_G I_G. \tag{3.2}$$

Since the switching waveforms of the SiC MOSFET are highly affected by the I-V and capacitance characteristics of the device, the measured switching waveforms are utilised to extract the additional I-V and capacitance characteristics that are not included in the conventional characterisation. However, due to the fast switching speed of the SiC MOSFET, the switching waveforms are also highly affected by the parasitic inductance in the package and the DPT circuit. The impact of the parasitic inductance will affect the accuracy of the extracted device characteristics. Therefore, a large external gate resistor $R_{G,ext} = 240\,\Omega$ was applied in the gate driver to make the switching speed slow so that the effect of the parasitic

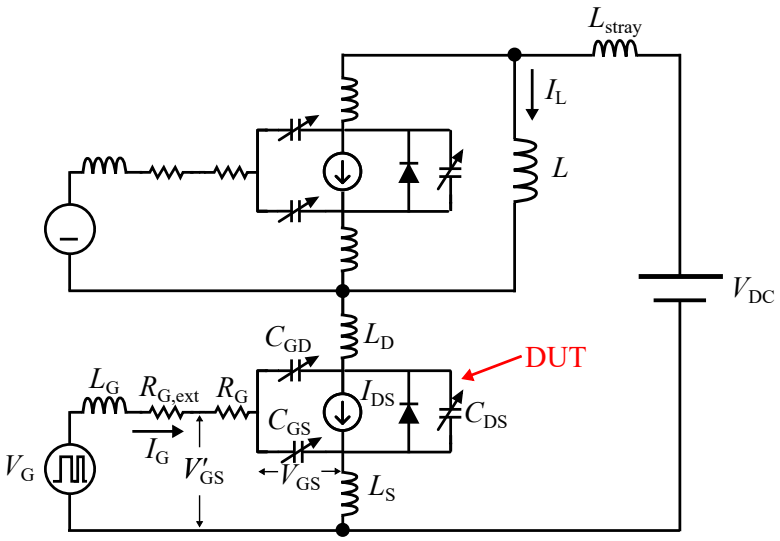


Figure 3.7: Circuit diagram of the double pulse tester.

inductance can be ignore and the device characteristics can be accurately observed. The measured turn-on and turn-off waveforms with $V_{DC} = 600\,\text{V}$ and $I_L = 100\,\text{A}$ are presented in Fig. 3.8 and Fig. 3.9, respectively, which show no oscillations caused by the parasitic inductance. The large gate resistor causes large switching losses and self-heating of the SiC MOSFET. This will not affect the accuracy of the measured C-V characteristics as the capacitance characteristics are not sensitive to the temperature. The I-V characteristics, however, are sensitive to the temperature and the accuracy is affected. Therefore, a method that can reduce the self-heating is proposed in Section 3.4 to measure the I-V characteristics.

3.4 DPT-based I-V Characterisation in High V_{DS} Region

Although exiting methods based on double pulse testers (DPTs) have been reported in [31, 76, 114], these methods exhibit non-negligible self-heating caused by the significant switching losses when the rated current of the MOSFET is high, which increases the junction temperature of the SiC MOSFET and cause inaccurate measurement results of the temperature-sensitive I_{DS}-V_{DS} characteristics [75]. To further reduce the self-heating, a method based on a modified DPT is presen-

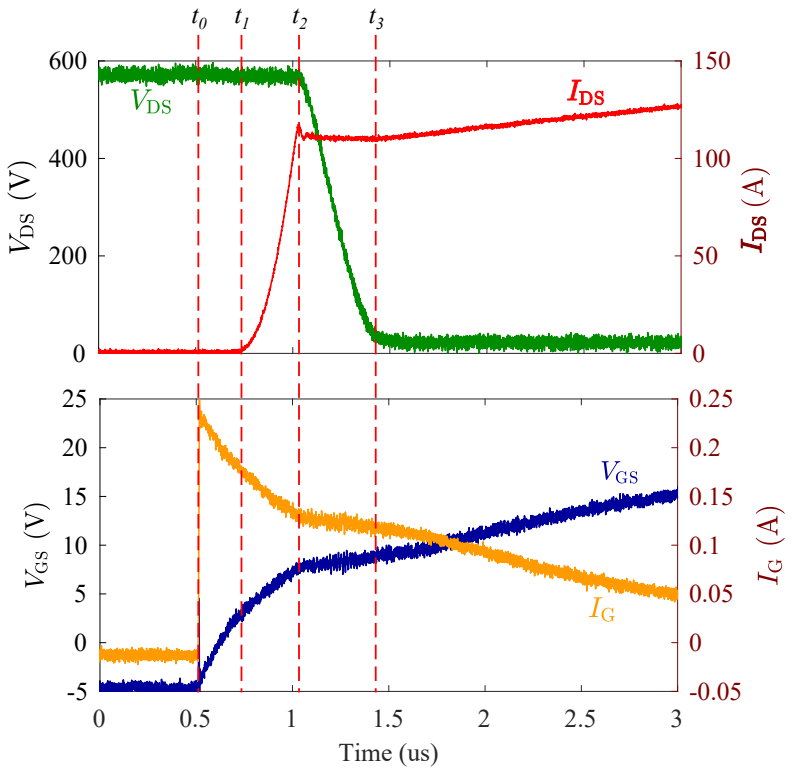


Figure 3.8: Turn-on waveforms measured by the DPT with $R_{G,ext} = 100\,\Omega$.

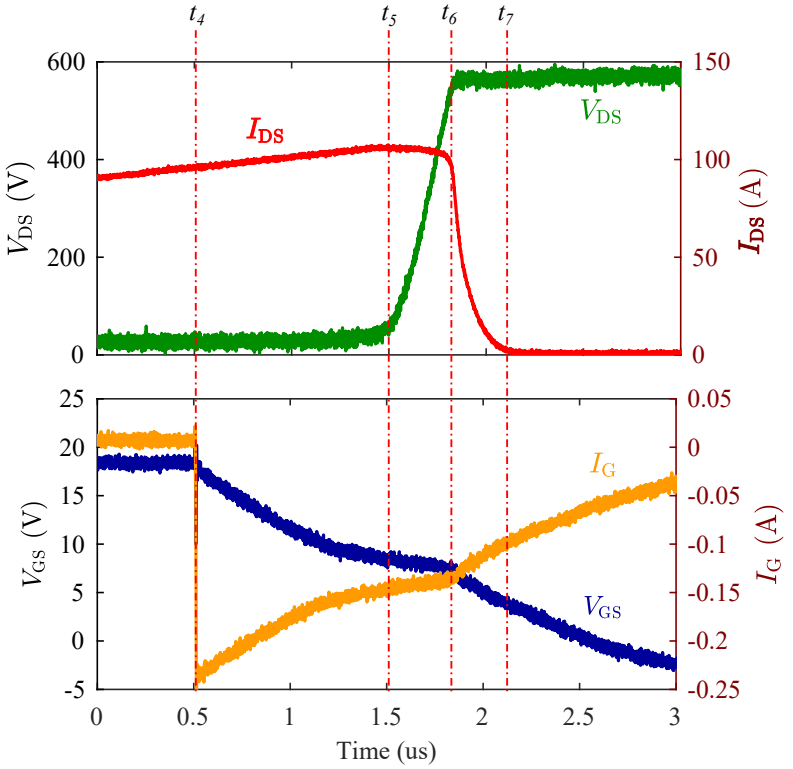


Figure 3.9: Turn-off waveforms measured by the DPT with $R_{G,ext} = 100\,\Omega$.

ted in [79]. However, it requires complex hardware modifications, including an additional power switch in parallel with the SiC MOSFET and a complex gate driver circuit to drive the paralleled switches.

In this section, an improved DPT-based method is proposed to measure the HVHC I_{DS}-V_{DS} characteristics of SiC MOSFETs, with the aim to reduce the self-heating. Firstly, a separate turn-off gate driver loop is added to modify the traditional DPT for HVHC I_{DS}-V_{DS} measurement to significantly reduce the turn-off loss. This is a lower-cost hardware modification to achieve the benefit of reduced self-heating, compared to [79]. Although the separate turn-off gate driver loop has been used in many other applications, its application to reduce the self-heating when measuring the HVHC I_{DS}-V_{DS} characteristics has not been reported before. Secondly, the gate driver signal of the modified DPT is designed to extend the cooling period of the SiC MOSFET to further reduce the self-heating. Consequently, the self-heating of the SiC MOSFET in the proposed method is up to 10 °C lower than that in the previous DPT-based method [31].

3.4.1 Proposed I-V Characterisation Method with Reduced Self-heating

As shown in Fig. 3.10, a modified DPT is proposed to reduce self-heating when measuring the HVHC I_{DS}-V_{DS} characteristics of the SiC MOSFET. Compared to the previous DPT-based method [31], the proposed method adds a separate turn-off gate driver loop to the DPT and extends the cooling period in the operation process of the DPT as shown in Fig. 3.11a. The detailed modifications are explained in this section.

In Fig. 3.11a, the HVHC I_{DS}-V_{DS} characteristics are measured during the turn-on transient in [t_3, t_4]. The turn-on waveforms are shown in Fig. 3.11b. At t_{sp}, V_{GS} reaches the gate plateau voltage, and the averaged V_{GS}, I_G, V_{DS} and I_{DS} are obtained during [t_{sp}, $t_{sp} + \triangle t$] to extract the I_{DS}-V_{DS} characteristics. $\triangle t = 30\,\text{ns}$ denotes the interval of the averaging process [31]. The turn-on waveforms of I_{DS}

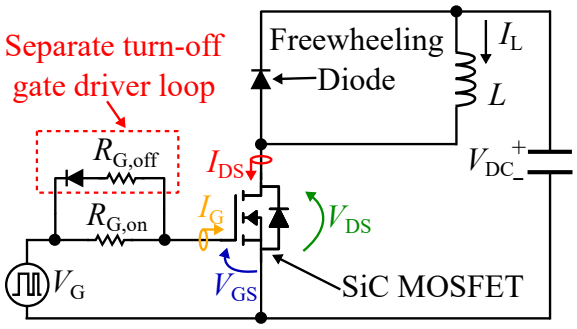


Figure 3.10: Circuit diagram of the double pulse tester.

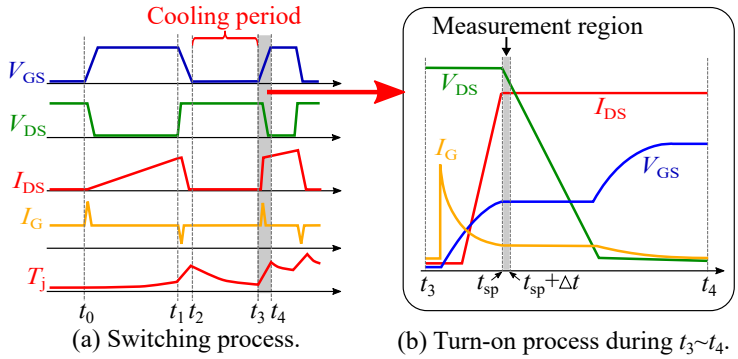
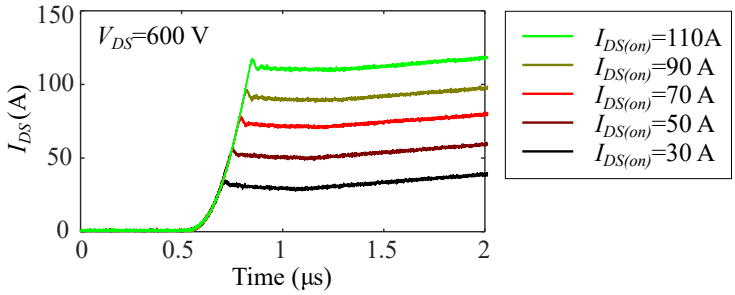


Figure 3.11: The switching process and self-heating of the SiC MOSFET in DPT.

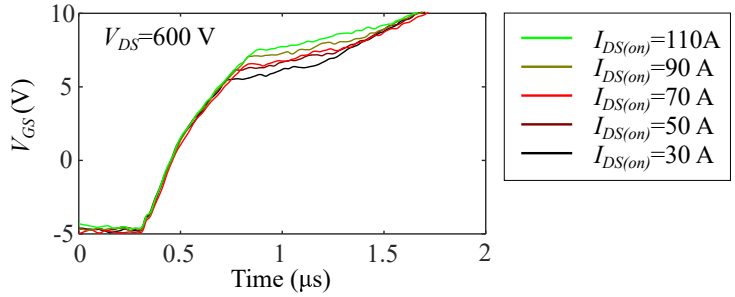
and V_{GS} with different turn-on currents under $V_{DC} = 600$ V is shown in Fig. 3.12.

The target of the proposed method is to reduce T_j at t_{sp} so that the errors of the measured I_{DS}-V_{DS} characteristics caused by the self-heating are reduced. During $[t_3, t_{\mathrm{sp}}]$, T_j is increased by the turn-on loss. However, to accurately measure the HVHC I_{DS}-V_{DS} characteristics at t_{sp}, a large turn-on gate resistor of 240 Ω must be adopted to reduce the switching speed so as to suppress the turn-on oscillations [79]. Therefore, the turn-on loss during $[t_3, t_{sp}]$ is inevitable. As a result, the proposed method focuses on reducing the self-heating before t_3.

In Fig. 3.11a, during $[t_0, t_1]$, the SiC MOSFET turns on and the inductor current I_L is charged by the DC bus voltage V_{DC} through the SiC MOSFET to a targeted value. T_j is increased by the conduction loss, which is determined by the charging time and the targeted inductor current. To measure the HVHC I_{DS}-V_{DS} characteristics at a certain $\{I_{DS}, V_{DS}\}$ point, the charging time and targeted inductor current cannot be changed. Therefore, the conduction loss during $[t_0, t_1]$ cannot be reduced.



(a) I_{DS}.

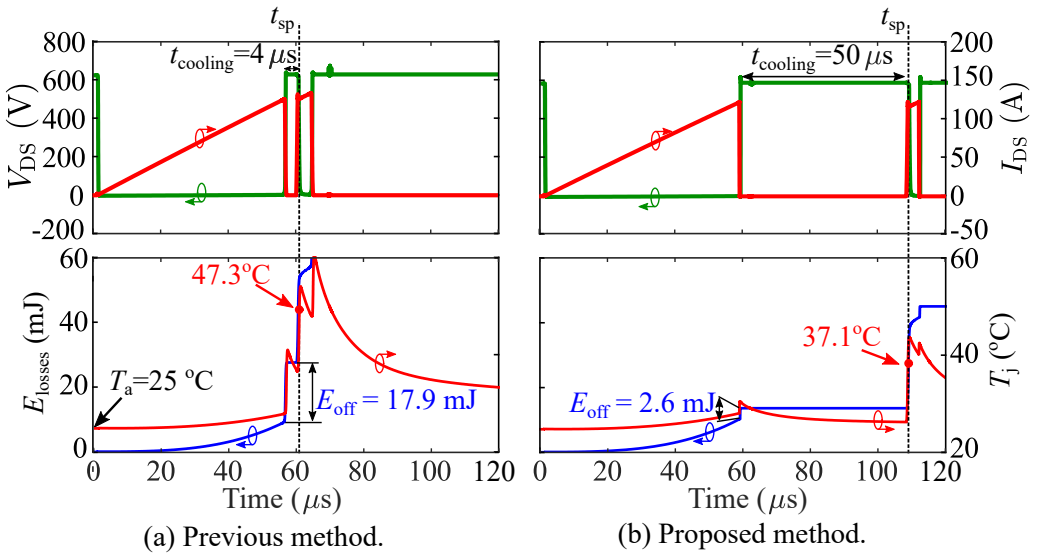


(b) V_{GS}.

Figure 3.12: Turn-on waveforms of I_{DS} and V_{GS} with different turn-on current under V_{DC} = 600 V. (The measured V_{GS} waveform is processed with a 20 MHz low pass filter to eliminate the jitter in the waveform.)

During [t_1, t_2], the SiC MOSFET turns off and T_j is increased by the turn-off loss. The turn-off loss is reduced by the proposed method by applying a separate turn-off gate driver loop as shown in Fig. 3.10. This is achieved by a surface mount resistor and a surface mount diode which cost less than $1 in total. In the existing DPT-based method [31], a 240 Ω resistor is used as the gate resistor for both turn-on and turn-off processes. In the proposed method, a much smaller turn-off gate resistor of 6.8 Ω is used, which is recommended by the datasheet of the SiC MOSFET to achieve low turn-off loss. As shown in Fig. 3.13, the turn-off losses E_{off} during [t_1, t_2] in the previous and proposed methods are 17.9 mJ and 2.6 mJ, respectively. The proposed method significantly reduces the turn-off loss E_{off} by 85%.

During [t_2, t_3], the load current I_L flows through the freewheeling diode so the power loss of the SiC MOSFET is zero. T_j decreases during this cooling period by dissipating heat to the ambient. In the proposed method, the gate driver signal is carefully designed to extend this cooling period. According to



(a) Previous method. (b) Proposed method.

Figure 3.13: DPT waveforms for measuring HVHC I_{DS}-V_{DS} characteristics with $V_{DS} = 600\,\text{V}$ and $I_{DS} = 120\,\text{A}$. The voltage, current and power losses are measurement results. The junction temperature T_j is simulated based on the measured power losses and thermal impedance model.

the transient thermal impedance model of the SiC MOSFET obtained from the datasheet, the cooling period is designed to 50 μs so that T_j is reduced close to the ambient temperature before t_3 as shown in Fig. 3.13. However, due to the total parasitic resistance R_{par} of the load inductor and the freewheeling diode, the inductor current I_L decreases during the cooling period. The decay factor of I_L can be calculated as: factor $= 1 - e^{-(t_3-t_2)\times R_{par}/L}$. In the experiment, a 270 μH load inductor with a parasitic resistance of 237 mΩ is used. The resistance of the body diode at the rated current is 46 mΩ according to the datasheet. Therefore, around 5% reduction of I_L occurs when the cooling period is 50 μs. This can be compensated by setting 5% longer charging time in $[t_0, t_1]$.

Due to significantly reduced turn-off loss and extended cooling period, the self-heating of the SiC MOSFET in the proposed method is up to 10 °C lower than that in the previous DPT-based method [31]. Compared to the method in [79], the reduced self-heating is achieved by the proposed method with simpler and lower-cost hardware.

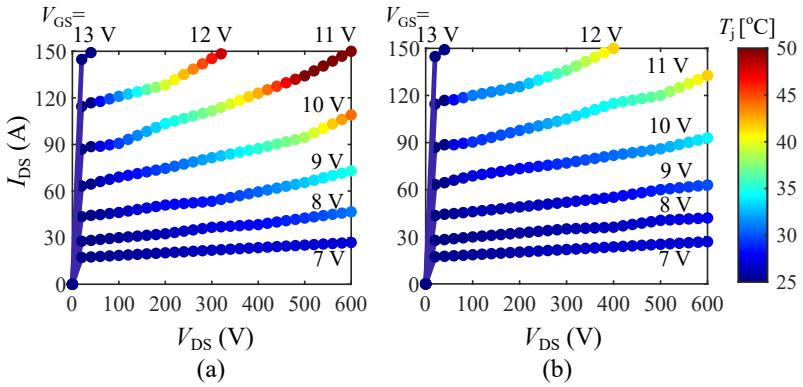


Figure 3.14: I_{DS}-V_{DS} characteristics in the high V_{DS} region measured by the (a) previous and (b) proposed method. The colour maps express the simulated T_j values at each I_{DS}-V_{DS}.

3.4.2 Measurement Results

The I_{DS}-V_{DS} characteristics in wide high V_{DS} region ($V_{DS} = 20-600\,\text{V}$ and $I_{DS} = 10-150\,\text{A}$) measured by the previous and proposed methods are presented in Fig. 3.14. The experiment was conducted at the ambient temperature $T_a = 25\,^{\circ}\text{C}$. The colour in the plots denotes the junction temperature T_j of the SiC MOSFET. Since T_j is very difficult to be measured by an infrared camera exactly at the time point of t_{sp} due to the short measurement period (less than 1 μs), it was simulated in PLECS based on the measured power losses and the thermal impedance model. The power losses of the SiC MOSFET were calculated by the time integral of $I_{DS} \times V_{DS}$. The thermal impedance of the SiC MOSFET was modelled based on the transient thermal impedance curve in the datasheet. It is indicated in Fig. 3.14 that the proposed method reduces T_j by up to 10 °C in the high V_{DS} region. In particular, the reduction is more effective when I_{DS} and V_{DS} are large.

The measured I_{DS}- V_{GS} characteristics with $V_{DS} = 600\,\text{V}$ are presented in Fig. 3.15. The measured data are curve fitted by the following equation:

$$I_{DS} = K(V_{GS} - V_{th})^P \tag{3.3}$$

where K, V_{th} and P are the curve fitting parameters. It is shown that the I-V characteristics measured by the proposed method is lower than those measured by the previous method in [31] due to reduced self-heating.

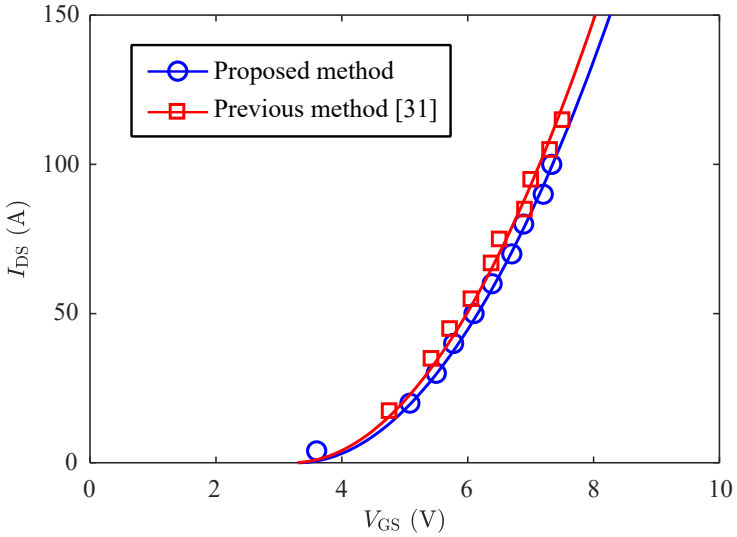


Figure 3.15: Measured I_{DS}-V_{GS} characteristics at $V_{DS} = 600\,\text{V}$.

Table 3.1: Relative RMS errors of simulated switching waveforms

	Turn on waveforms		Turn-off waveforms	
	Conventional model	Proposed model	Conventional model	Proposed model
I_{DS}	7.1%	5.7%	8.1%	3.4%
V_{DS}	15.1%	4.7%	8.0%	2.0%
V_{GS}	24.8%	20.3%	22.9%	17.1%

To evaluate the impact of reduced self-heating on the model accuracy, the SiC MOSFET was modeled based on the I_{DS}-V_{DS} characteristics measured by the previous and proposed methods. The modeling method based on artificial neural networks presented in [115] was used to build the models. Switching waveforms were simulated by the models and compared to the measured waveforms in Fig. 3.16, where the conventional and proposed models were built based on the I_{DS}-V_{DS} characteristics measured by the previous and proposed methods, respectively. It is shown that the proposed model presents more accurate simulation results than the conventional model.

The improved accuracy of the proposed model was quantified by calculating the relative RMS errors of the simulation results, the same as in [31]. The relative RMS errors of I_{DS}, V_{DS} and V_{GS} of both models are presented in Table 3.1. It is shown that the relative RMS errors of the proposed model are at least 18% smaller than those of the model based on the previous I_{DS}-V_{DS} measurement method.

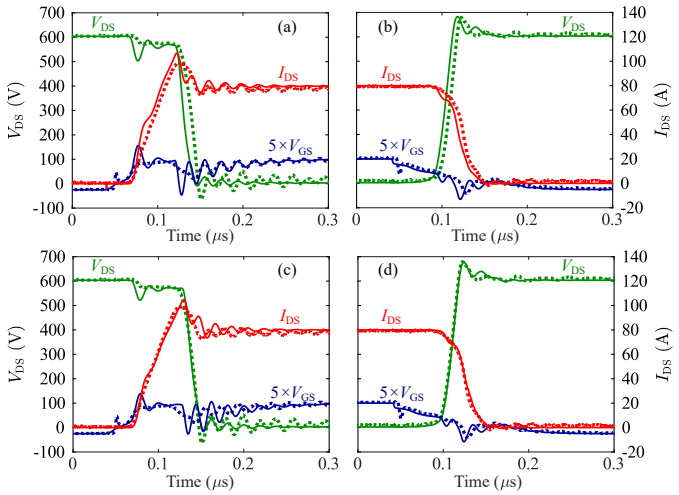


Figure 3.16: The measured and simulated switching waveforms. Dashed and solid lines denote the experimental and simulated waveforms, respectively. (a) Turn on by conventional model. (b) Turn off by conventional model. (c) Turn on by proposed model. (d) Turn off by proposed model.

3.5 DPT-based Measurement of Nonlinear C_{GS} Characteristics

In the conventionally-measured static-state C-V characteristics, C_{GS} is almost a constant value as shown in Fig. 3.5. However, due to the metal-oxide-semiconductor (MOS) structure, C_{GS} is a voltage-dependent capacitor, which varies with the capacitor voltage V_{GS} [48]. During the switching transient, the charging and discharging of C_{GS} will affect the switching behaviours. Therefore, the charging behaviour measured by the DPT during the turn-on process is analysed to measure the nonlinear C_{GS} characteristics.

3.5.1 Analysis of Turn-on Process and Nonlinear C_{GS}

The turn-on process can be divided into four stages as shown in Fig. 3.8. The turn-on delay stage ($t_0 \sim t_1$) and I_{DS} rising stage ($t_1 \sim t_2$) can be used to measure the nonlinear C_{GS} characteristics.

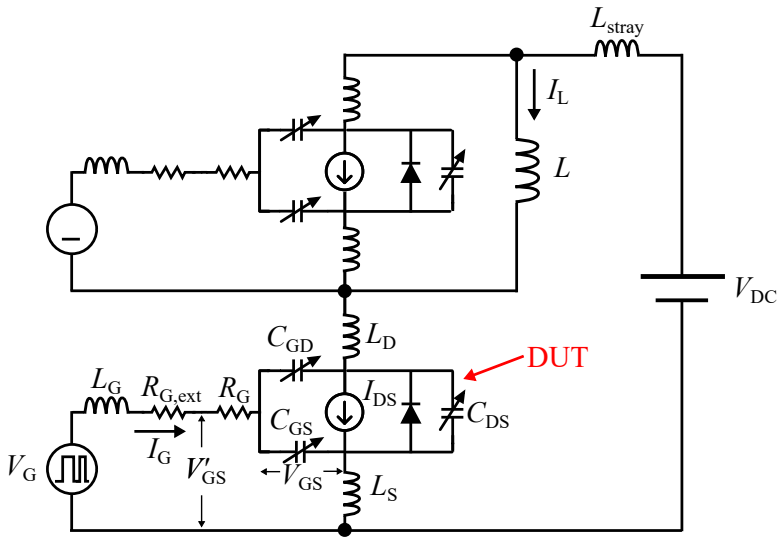


Figure 3.17: Circuit diagram of the double pulse tester.

Turn-on Delay Stage ($t_0 \sim t_1$)

At t_0, the gate driver of the bottom SiC MOSFET is triggered by the turn-on signal. The gate driver voltage V_G jumps from the turn-off gate voltage ($V_{G,off} = -5\,\mathrm{V}$) to the turn-on gate voltage ($V_{G,on} = 20\,\mathrm{V}$). The gate capacitors C_{GS} and C_{GD} are charged by the gate driver voltage. The bottom SiC MOSFET is not turned on because $V_{GS} < V_{GS,th}$, where $V_{GS,th}$ is the threshold voltage. Therefore, $I_{DS} \approx 0\,\mathrm{A}$ and $V_{DS} \approx V_{DC}$. The following equations can be obtained for this stage according to Fig. 3.17:

$$V_{G,on} = V_{GS}(t) + (R_{G,ext} + R_G)I_G(t) + (L_G + L_S)\frac{\mathrm{d}I_G(t)}{\mathrm{d}t} + L_S\frac{\mathrm{d}I_{DS}(t)}{\mathrm{d}t} \tag{3.4}$$

$$I_G(t) = (C_{GS} + C_{GD})\frac{\mathrm{d}V_{GS}(t)}{\mathrm{d}t} \tag{3.5}$$

Since a large gate resistor $R_{G,ext} = 240\,\Omega$ is selected to slow down the switching speed, the voltage drop on the parasitic inductors can be ignored. Therefore, (3.4) can be simplified as

$$V_{G,on} = V_{GS}(t) + (R_{G,ext} + R_G)I_G(t) \tag{3.6}$$

I_{DS} Rising Stage ($t_1 \sim t_2$)

At t_1, the gate-source voltage is charged to the threshold voltage $V_{GS,th}$. The bottom SiC MOSFET starts conducting current. The drain-source current is controlled by V_{GS} and V_{DS}: $I_{DS} = f(V_{GS}, V_{DS})$, where V_{DS} is clamped to V_{DC} at this stage because the anti-parallel diode of the upper SiC MOSFET is still conducting current. The gate-source voltage $V_{GS}(t)$ continues to be charged by V_G and the same charging equations in (3.4) and (3.5) can be obtained. The same simplified equation can be obtained as (3.6) by ignoring the parasitic inductors.

During $t_0 \sim t_2$, the charging behaviour of the gate capacitors is determined by (3.5) and (3.6). Since I_G and V_{GS} can be measured in the DPT, the gate capacitance can be calculated as:

$$C_{GS} + C_{GD} = I_G(t) / \frac{\mathrm{d}V_{GS}(t)}{\mathrm{d}t} \tag{3.7}$$

During $t_0 \sim t_2$, $V_{DS} \approx 600\,\mathrm{V}$ as shown in Fig. 3.8. According to the capacitance characteristics in the datasheet, $C_{GD} \approx 36\,\mathrm{pF}$ and $C_{GS} \approx 6300\,\mathrm{pF}$ at $V_{DS} = 600\,\mathrm{V}$. Therefore, C_{GD} can be ignored in (3.7) and the C_{GS}-V_{GS} characteristics can be obtained:

$$C_{GS} \approx I_G(t) / \frac{\mathrm{d}V_{GS}(t)}{\mathrm{d}t} \tag{3.8}$$

3.5.2 Measurement Results

In (3.8), the derivative of V_{GS} is used. However, the measured V_{GS} inevitably contains high-frequency and low-frequency noises, which are especially unwanted in the derivative calculation. It was found that the simple low-pass filter is not good enough to filter out the noises and brings the time delay to the signal. Instead, a curve fitting method was used to fit the turn-on waveforms of V_{GS} and I_{GS} during ($t_0 \sim t_2$) to filter out the noises. The artificial neural network (ANN) was selected as the curve fitting tools. The measured V_{GS} and I_{GS} were fed into the Neural Net Fitting Toolbox in MATLAB to train the ANN. The filtered V_{GS} and

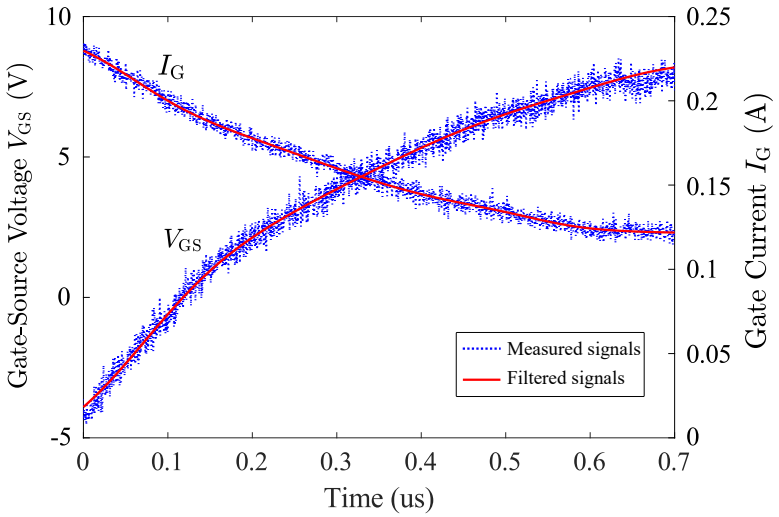


Figure 3.18: Turn-on waveforms ($t_0 \sim t_2$) filtered by artificial neural networks (ANNs).

I_{GS} waveforms are shown in Fig. 3.18. The nonlinear C_{GS}-V_{GS} characteristics can be then calculated as shown in Fig. 3.19. The nonlinear C_{GS}-V_{GS} characteristics are measured with V_{GS} between $[-4\,\mathrm{V}, 5\,\mathrm{V}]$. According to the characteristics of the MOS capacitor in the MOSFET [113], the value of C_{GS} with $V_{GS} > 5\,\mathrm{V}$ is assumed constant.

3.6 DPT-based Measurement of On-state and Dynamic C_{GD} Characteristics

C_{GD} is a nonlinear capacitor that varies with the drain-gate voltage V_{DG}. The static C_{GD}-V_{DS} characteristics are measured by the conventional method with $V_{GS} = 0\,\mathrm{V}$ (i.e. V_{DG}=V_{DS}). Therefore, the C_{GD} characteristics versus V_{DG} from 0 V to 1000 V in the off state ($V_{GS} = 0\,\mathrm{V}$) can be obtained according to Fig. 3.5. However, in the on state of the SiC MOSFET, the on-state gate-source voltage V_{GS} is usually set as high as 20 V for CAS120M12BM2 to reduce the on-state resistance, and the on-state drain-source voltage is lower than 3 V depending on the conduction current. Therefore, a negative V_{DG} is applied to C_{GD} in the on state. The on-state C_{GD} characteristics with $V_{DG} < 0$ are not provided in the datasheet,

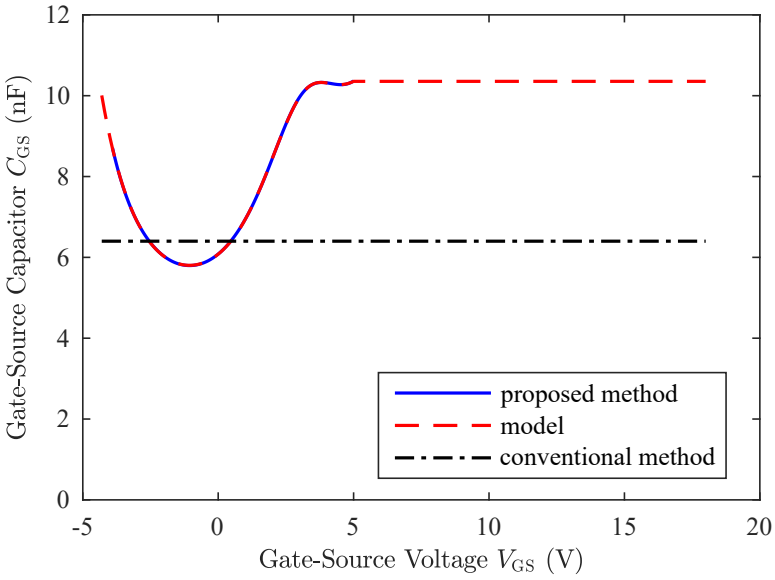


Figure 3.19: Calculated C_{GS}-V_{GS} characteristics based on DPT measurement.

which need to be measured for accurate device modelling. Besides, during the switching transient of SiC MOSFETs, it is found in [33] that the dynamic C_{GD} characteristics are also different with the static C_{GD} characteristics .

3.6.1 Analysis of Turn-off Process and On-state C_{GD}

The turn-off waveforms measured by the DPT is analysed to extract the on-state C_{GD} characteristics. The turn-off process can be divided into four stages as shown in Fig. 3.9. The turn-off delay stage ($t_4 \sim t_5$) is used to measure the on-state C_{GD} characteristics.

In Fig. 3.9, at t_4, the gate driver is triggered by the turn-off signal. The gate driver voltage V_G jumps from the turn-on gate voltage ($V_{G,on} = 20\,\mathrm{V}$) to the turn-off gate voltage ($V_{G,off} = -5\,\mathrm{V}$). The gate capacitors C_{GS} and C_{GD} are discharged to the gate plateau voltage V_{gp} at t_5. During the turn-off delay stage, the bottom SiC MOSFET is still in on-state. With the discharging of C_{GD}, the drain-gate voltage changes from negative bias to positive bias. The discharging behaviour of the gate capacitance can be described by neglecting the parasitic inductors:

$$V_{G,off} = V_{GS}(t) + (R_{G,ext} + R_G)I_G(t) \tag{3.9}$$

$$I_G(t) = C_{GS}\frac{\mathrm{d}V_{GS}(t)}{\mathrm{d}t} - C_{GD}\frac{\mathrm{d}V_{DG}(t)}{\mathrm{d}t} \tag{3.10}$$

The on-state C_{GD}-V_{GD} characteristics with negative bias voltage V_{DG} can be obtained as:

$$C_{GD} = \left(C_{GS}\frac{\mathrm{d}V_{GS}(t)}{\mathrm{d}t} - I_G(t)\right) / \frac{\mathrm{d}V_{DG}(t)}{\mathrm{d}t} \tag{3.11}$$

where $V_{DG} = V_{DS} - V_{GS}$. Since C_{GS} has been measured as shown in Fig. 3.19, the on-state C_{GD} characteristics can be obtained by measuring V_{GS}, I_G and V_{DG} during the turn-off delay stage.

3.6.2 Analysis of Turn-off Process and Dynamic C_{GD}

In the turn-off process shown in Fig. 3.9, the V_{DS} rising stage ($t_5 \sim t_6$) can be used to measure the dynamic C_{GD} characteristics. At t_5, V_{GS} reaches the gate plateau voltage V_{gp}. C_{GD} and C_{DS} are charged and V_{DS} starts rising. The charging equation on C_{GD} can be written as:

$$I_G(t) = C_{GS}\frac{\mathrm{d}V_{GS}(t)}{\mathrm{d}t} - C_{GD}\frac{\mathrm{d}V_{DG}(t)}{\mathrm{d}t} \tag{3.12}$$

During $t_5 \sim t_6$, the charging behaviour of C_{GD} is determined by (3.12). Since I_G, V_{GS} and V_{DS} can be measured in the DPT and C_{GS}-V_{GS} characteristics has been obtained in Fig. 3.8. The dynamic C_{GD}-V_{DG} characteristics during the V_{DS} rising stage can be calculated as:

$$C_{GD} = \left(C_{GS}\frac{\mathrm{d}V_{GS}(t)}{\mathrm{d}t} - I_G(t)\right) / \frac{\mathrm{d}V_{DG}(t)}{\mathrm{d}t} \tag{3.13}$$

where $V_{DG} = V_{DS} - V_{GS}$.

3.6.3 Measurement Results of On-state and Dynamic C_{GD}

On-state C_{GD}

In (3.11), the derivatives of V_{GS} and V_{DG} are used to calculate the on-state C_{GD}. The measured V_{GS} and I_G during the turn-off delay stage inevitably contains high-frequency and low-frequency noises, which were fitted by the ANN as shown in Fig. 3.20.

V_{DS} can also be measured by the oscilloscope. However, during the turn-off delay stage, V_{DS} only changes several volts while the measurement range of the voltage probe for V_{DS} is over 600 V. Therefore, the slight change of V_{DS} during the turn-off delay stage cannot be accurately measured by the probe considering the measurement error and noises. In this thesis, instead of using the measured V_{DS}, V_{DS} during the turn-off stage is estimated based on the I-V characteristics as shown in Fig. 3.3a, where the relation between V_{DS} and V_{GS} with $I_{DS} = 100\,\text{A}$ can be found. The V_{DS}-V_{GS} curve is then fitted by polynomial functions as shown in Fig. 3.21. The V_{DS} waveform can be estimated based on the V_{GS} waveform in Fig. 3.20. The on-state C_{GD}-V_{DG} characteristics can be then calculated.

Dynamic C_{GD}

The calculation of the dynamic C_{GD} requires the measured V_{GS}, I_G and V_{DG} during the turn-off process ($t_5 \sim t_6$). Firstly, the ANNs were applied to fit the measured waveforms to filter out the noises. The filtering results are shown in Fig. 3.22. Afterwards, the dynamic C_{GD} can be calculated according to (3.13).

The calculated on-state and dynamic C_{GD}-V_{DG} characteristics are shown in Fig. 3.23. Comparing to the static C_{GD} characteristics measured by a B1505A, the measured on-state C_{GD} characteristics covers the negative V_{DG} region from -20 V to 0 V. It is also shown that the measured dynamic C_{GD} characteristics are larger than the static C_{GD} characteristics. This is consistent with the conclusion in [116], which shows that the dynamic Q_{GD} during the turn-on transient is larger than the static Q_{GD} based on the static C_{GD} characteristics.

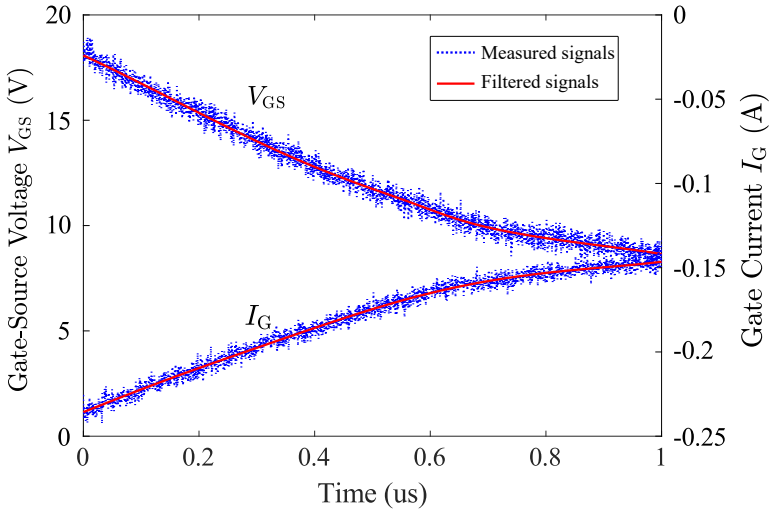


Figure 3.20: Turn-off waveforms ($t_4 \sim t_5$) filtered by ANNs.

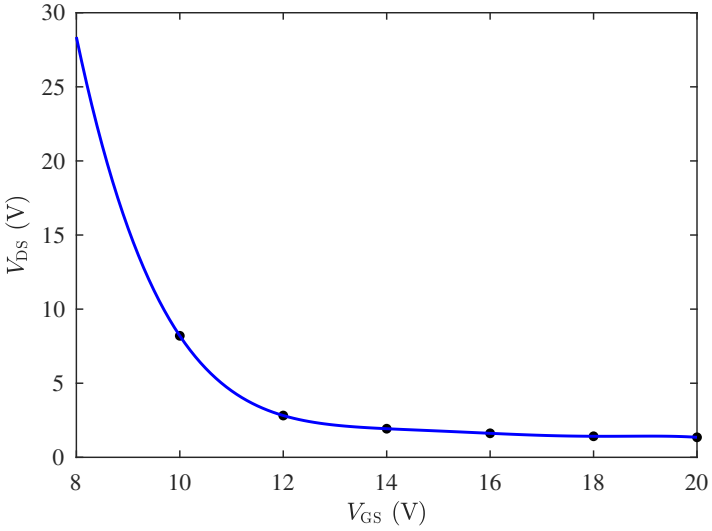


Figure 3.21: V_{DS}-V_{GS} curve with $I_{DS} = 100\,\text{A}$.

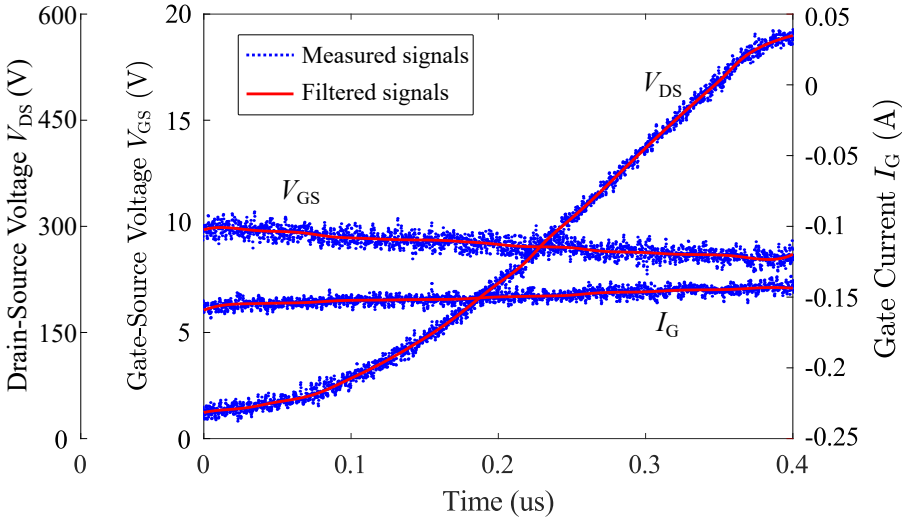


Figure 3.22: Turn-off waveforms ($t_5 \sim t_6$) filtered by ANNs.

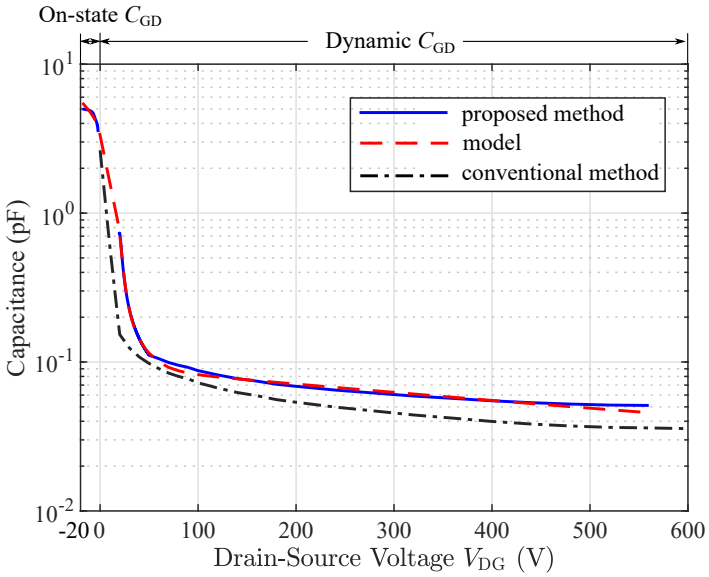


Figure 3.23: Modeling of C_{GD}-V_{DG} characteristics.

3.7 Summary

The conventional static-state I-V and C-V characterisation methods based on the Keysight B1505A power device analyser can only measure the I-V characteristics in the low V_{DS} region and C-V characteristics in the static off-state. It was identified that these characteristics are insufficient for accurate simulation of the dynamic switching of SiC MOSFETs according to the semiconductor physics analysis. Therefore, a DPT-based measurement method was proposed to characterise additional dynamic-state characteristics as complements of the conventionally-measured I-V and C-V characteristics in order to accurately simulate the switching behaviour of the SiC MOSFETs. These additional characteristics include the I-V characteristics in the high V_{DS} region, nonlinear C_{GS} characteristics, on-state and dynamic C_{GD} characteristics. The relation of these characteristics with the switching waveforms of SiC MOSFETs was analysed in detail. Based on the analysis, the solid-state I-V and C-V characteristics were directly extracted from the switching waveforms measured by a DPT. Compared to previous dynamic-state measurement methods presented in the literature, the proposed method only utilised a DPT for the measurement, which significantly simplified the characterisa-

tion process of the SiC MOSFET. Besides, the proposed method can significantly reduce the self-heating of the SiC MOSFET when measuring the I-V characteristics in the high V_{DS} region to reduce the errors caused by the increased junction temperature.

The dynamic-state I-V and C-V characteristics that have significant impact on the switching waveforms of the SiC MOSFET have been measured by the proposed DPT-based measurement method. In the next step, the effectiveness of the measured characteristics to improve the model accuracy of the SiC MOSFET in transient simulation need to be validated. The validation will be conducted in the next chapter.

Chapter 4

Measurement-based Accurate Modelling of SiC MOSFETs

This chapter presents a measurement-based modelling method of SiC MOSFETs, i.e., a hybrid data-driven behavioural modelling methodology based on artificial neural networks. The hybrid modelling methodology is proposed because the pure data-driven model cannot accurately model the cut-off region of SiC MOSFETs. The model is built based on the I-V and C-V characteristics measured in Chapter 3. This proposed modelling method can overcome the challenges of the conventional behavioural modelling methods, such as complex equation design, difficult parameter extraction, poor model adaptability, limited accuracy, slow simulation speed, etc. The effectiveness of the proposed modelling method is verified through comparison with a commercial modelling method based on the Angelov model. The characterisation methods proposed in Chapter 3 are also verified based on the proposed hybrid data-driven model.

4.1 Introduction

Measurement-based models are widely used in transient circuit simulation. Most measurement-based models are behavioural models, which are implemented using mathematical equations to match the measured device characteristics, such

as I-V and C-V characteristics [97]. Complex nonlinear equations are firstly designed according to the device characteristics. Afterwards, the equation parameters are extracted using mathematical curve fitting methods [96]. As is mentioned in Chapter 2, the existing behavioural models have the following issues: 1) The design of mathematical equations and the extraction of parameters are complicated; 2) The equations cannot accurately match the complex characteristics of the SiC MOSFET; 3) The designed mathematical equations lack adaptability to model different SiC MOSFETs with different characteristics accurately. 4) The complicated models have slow simulation speed.

A new behavioural modelling algorithm based on artificial neural networks (ANNs) was proposed in [101–103] which aimed to give a simple and fast data-driven method. Thanks to the data-driven approach, such ANN-based models can potentially overcome the aforementioned challenges of the conventional behavioural modelling methods. Complex equation design is avoided and the ANN parameters can be extracted easily and automatically by training the ANN using many well-developed toolboxes such as the Neural Net Fitting Toolbox in MATLAB. Also, the complex characteristics of the SiC MOSFETs can be accurately modelled by well-trained ANNs. In addition, ANNs have good adaptability to model SiC MOSFETs with different characteristics because ANNs can approximate any mathematical functions [104]. However, the existing ANN-based modelling methods are only suitable for static simulation but not for transient simulation due to the insufficient training dataset and inaccurate data-driven models.

In this chapter, a new measurement-based modelling method, i.e., the hybrid data-driven behavioural modelling methodology, was proposed to achieve fast and accurate transient simulation. At its core, an ANN-based data-driven model was used to model the I-V and C-V characteristics in the whole operation region, which was overlaid with behaviour-based equations to accurately model the cutoff region. A SiC MOSFET module CAS120M12BM2 was used to validate the proposed modelling methodology for accuracy and repeatability. The training data-

set of ANNs and the transient switching waveforms were measured from the same module. The accuracy of the proposed hybrid modelling method was verified by comparing simulated and measured switching waveforms from the SPICE simulator SIMetrix and a double pulse tester (DPT), respectively. The proposed model was also compared with the Angelov model in [111]. It is shown that the proposed model can achieve $1.5 \sim 3$ times less errors and better adaptability than the Angelov model. Besides, the computation time of the proposed model was compared with the Angelov model through simulating the same DPT circuit in SIMetrix. The runtime of the proposed model is found to be 30% faster than the Angelov model.

Besides, the DPT-based measurement methods proposed in Chapter 3 were further validated in this chapter. The model based on the dynamic-state characteristics measured by the proposed DPT-based measurement method was compared to the model based on the characteristics measured by the conventional static-state method. The simulation results show that the accuracy of the simulated switching waveforms is significantly improved after considering the dynamic-state characteristics measured by the proposed DPT-based measurement method.

The main contribution of this chapter is that, for the first time, an ANN-based hybrid data-driven modelling method is proposed and verified for accurate transient simulation of SiC MOSFETs. The proposed method improves accuracy of SiC MOSFET models. It is found that simply using the data measured from a curve tracer to train the ANNs cannot generate an accurate transient model of SiC MOSFET. The accuracy of the model is largely determined by two factors, i.e., high-quality training dataset and proper data-driven model, which are detailed as follows:

1. For the training dataset of the I-V characteristics, compared to existing methods [101], it is identified that the I-V characteristics in the high voltage region (i.e. saturation region up to the maximum DC voltage across the MOSFETs) must be included to obtain accurate simulation results across

the whole operation region of SiC MOSFETs in transient simulation.

2. It is identified that a proper data-driven model is critical for accurate modelling of the I-V characteristics. Since the cut-off region of the I-V characteristics is hard to be modelled correctly by a pure data-driven model presented in existing methods, a hybrid data-driven model is proposed to model the cutoff region accurately.

3. The training dataset and proper data-driven model are also identified for the C-V characteristics which are not considered in existing methods. The C-V characteristics are measured in the whole V_{DS} region in logarithmic scale as the training dataset, and logarithmic transformation is applied in ANN models for accuracy.

As a result, the proposed modelling method improves the accuracy of transient simulation, which in turn can be used for accurate analysis of power losses and EMI in computer-aided design of power converters based on SiC MOSFETs.

The rest of this chapter is organised as follows: Section 4.2 reviews the existing ANN-based modelling method and its limitations for accurate transient simulation. To improve the existing ANN method, a hybrid data-driven modelling method is proposed in Section 4.3. In Section 4.4, the accuracy of the proposed hybrid data-driven model is verified by comparing the simulation and experimental results. Section 4.5 compares the proposed model with a conventional Angelov model to verify the advantages of the proposed modelling method over conventional methods. Section 4.6 utilises the proposed modelling method to verify the effectiveness of the DPT-based measurement method presented in Chapter 3. The conclusions are summarised in Section 4.7.

4.2 Review of the Existing ANN Model

It was noted in the conclusions of [101] that the existing ANN model is not suitable for transient simulation. In this section, the existing ANN model is reviewed from

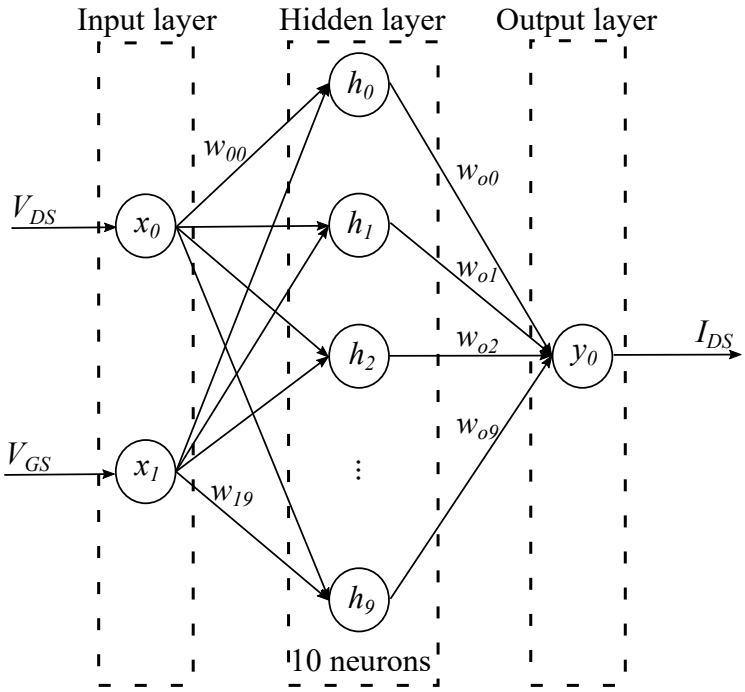


Figure 4.1: ANN topology.

its structure to the limitations on transient simulation. A 1200V 120A module CAS120M12BM2 from Wolfspeed was selected to facilitate the analysis.

4.2.1 Structure of Artificial Neural Network

As shown in Fig. 4.1, a single-hidden-layer ANN was used to model the I-V characteristics of SiC MOSFETs. The single-hidden-layer ANN consists of an input layer, a hidden layer and an output layer. The input layer has two neurons to receive two input variables: the drain-to-source voltage V_{DS} and gate-to-source voltage V_{GS}. The output layer has one neuron which outputs the drain-to-source current I_{DS}. The hidden layer has 10 neurons. Each neuron in one layer is connected with each neuron in the next layer. Each connection has a weight. Each neuron computes the sum of the weighted inputs and the bias. Afterwards, it uses an activation function (e.g. sigmoid function) to compute the output of the neuron and sent the output to the next layer. The ANN can be represented

by the following mathematical equation:

$$I_{DS} = f_{ANN}(V_{DS}, V_{GS}) = \sum_{j=0}^{9} (w_{oj} h_j) + b_o \tag{4.1}$$

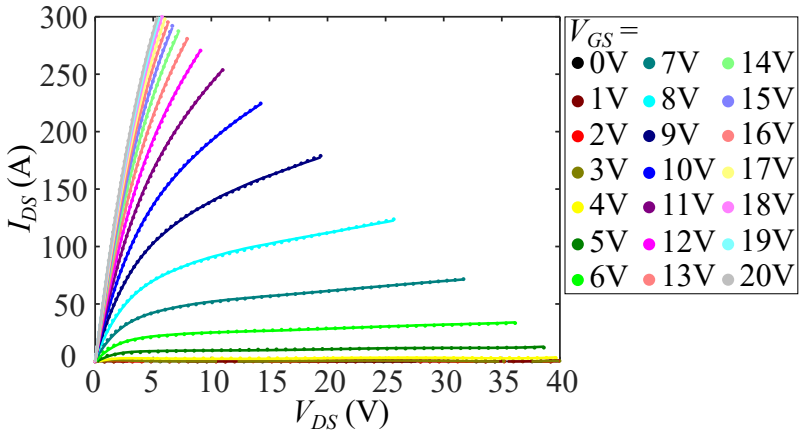
where $\begin{bmatrix} x_0 & x_1 \end{bmatrix} = \begin{bmatrix} V_{DS} & V_{GS} \end{bmatrix}$; w_{oj} is the weight between the j-th hidden-layer neuron and the output neuron; b_o is the bias of the output neuron; h_j is the output of the j-th hidden-layer neuron; b_j is the bias of the j-th hidden-layer neuron; w_{ij} is the weight between the i-th input neuron and the j-th hidden-layer neuron. A sigmoid function is used as the activation function in the hidden layer: $sigmoid\,(x) = \frac{1}{1+e^{-x}}$.

The training process is to tune the weights and biases in the ANN to fit the training data, which are a set of measured characteristics of SiC MOSFETs. A back-propagation algorithm is widely used in the training process [117]. Many software programs have toolboxes to automatically train the ANN, such as the Neural Net Fitting Toolbox in MATLAB.

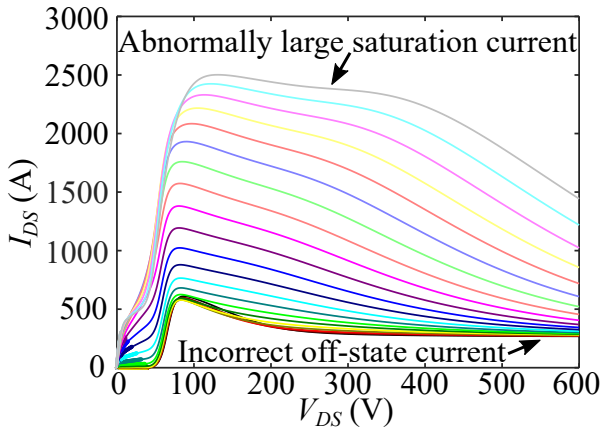
4.2.2 Limitations of the Existing ANN Model

In the existing ANN model for static simulation [101], the I-V characteristics in a low V_{DS} region are measured by a curve tracer to train the ANN. As shown in Fig. 4.2a, the ANN model can match the measurement data accurately, which is adequate for static simulation. However, for accurate transient simulation, the model has the following three limitations.

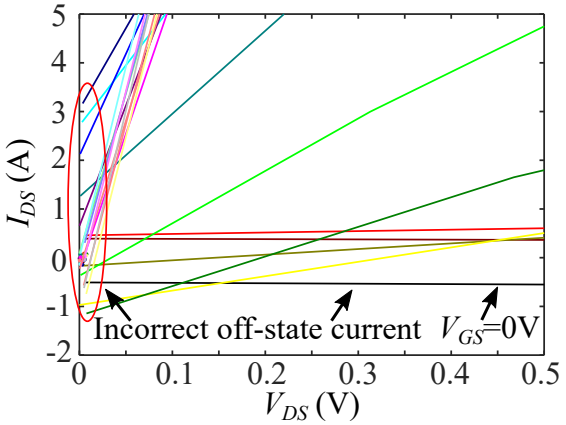
Firstly, the existing ANN model is trained by the I-V characteristics measured in a low V_{DS} region only (0-40 V). However, due to the poor extrapolation ability of the used ANN, the I-V characteristics in the high V_{DS} region from 40 V to the maximum DC voltage ($\geq$ 600 V for CAS120M12BM2) cannot be accurately modelled, which causes inaccurate transient simulation. As shown in Fig. 4.2b, the existing ANN model has abnormally large saturation current and incorrect off-



(a) Performance in low V_{DS} region.



(b) Performance in whole V_{DS} region.



(c) Performance in cutoff region.

Figure 4.2: Existing ANN model presented in [101] that is trained with measured I-V characteristics in a low V_{DS} region. (Solid lines denote the simulated data. Dots denote the measured data.)

state current in high V_{DS} region, which are physically wrong for SiC MOSFETs.

Secondly, the off-state, i.e., the cutoff region cannot be accurately modelled. The existing ANN has large errors in the cutoff region as shown in Fig. 4.2c. There is still significant (even negative) I_{DS} when $V_{DS} = 0\,\mathrm{V}$ or V_{GS} is lower than threshold voltage $V_{GS(th)}$, which is physically wrong according to the physical characteristics of SiC MOSFETs in cutoff region. This is because the ANN is a data-driven model without considering any specific physical characteristics. Also, the training process of ANN is an optimisation process to minimize overall error but the local error at a specific region, e.g., cutoff region where I_{DS} is zero, can still be very large.

Thirdly, the C-V characteristics are not considered in the existing ANN model, which are essential for transient simulation. The large variations of C-V characteristics in the whole V_{DS} region must be considered in the modelling method for accuracy.

4.3 Proposed Hybrid Modelling Methodology for Transient Simulation

A hybrid modelling methodology is proposed to correspondingly solve the aforementioned three limitations of the existing ANN model described in [101]. The subcircuit model of SiC MOSFETs is presented in Fig. 2.17. The I-V characteristics of SiC MOSFETs are modelled by the voltage-controlled current source I_{DS} in the subcircuit model. The C-V characteristics are modelled by three variable capacitors C_{GS}, C_{GD}, C_{DS}. Drain-source current I_{DS} and the variable capacitors

are modelled as functions of voltages:

$$\begin{cases} I_{DS} &= f_{IV}(V_{DS}, V_{GS}) \\ C_{GS} &= f_{C_{GS}}(V_{DS}) \\ C_{GD} &= f_{C_{GD}}(V_{DS}) \\ C_{DS} &= f_{C_{DS}}(V_{DS}). \end{cases} \tag{4.2}$$

In this thesis, the above functions are modelled by the proposed hybrid data-driven method and then applied in SPICE simulator SIMetrix using Verilog-A language.

4.3.1 Data-driven Modelling of I-V Characteristics in the Whole V_{DS} Region

The I-V characteristics of the SiC MOSFET were measured using the methods introduced in Chapter 3. The I-V characteristics in the low voltage ranges ($V_{DS} < 40\,\text{V}$), including the I_{DS}-V_{DS} characteristics and the I_{DS}-V_{GS} characteristics, were measured by a curve tracer (B1505A; Keysight Technologies, Inc.). In this study, the I_{DS}-V_{DS} characteristics were measured with V_{DS} between [0, 40] V in steps of 0.8 V and V_{GS} between [0, 20] V in steps of 1 V. The I_{DS}-V_{GS} characteristics were measured with V_{GS} between [0, 20] V in a step of 0.4 V and V_{DS} between [0, 40] V in a step of 2 V.

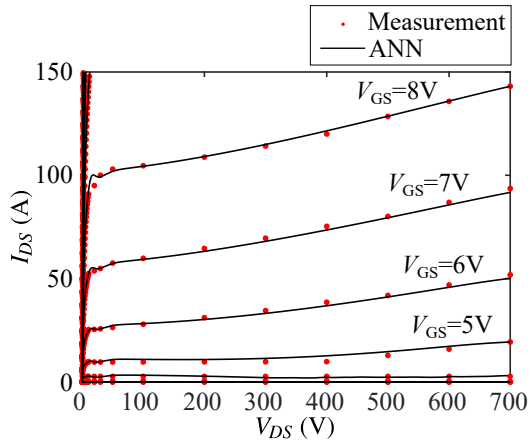
The I-V characteristics in the high V_{DS} region (up to the maximum DC voltage across the MOSFETs) have significant impact on the transient simulation [78, 79, 111, 116]. It is shown in Fig. 4.2b that the existing ANN model cannot simulate the high V_{DS} region correctly. This is caused by the poor extrapolation ability of the data-driven-based ANN. The output of the ANN is not reliable when the ANN works beyond the region of the training data. The measurement method presented in Chapter 3 was used to measure the I-V characteristics in the high V_{DS} region during the turn-on transients. The I-V characteristics in the high voltage region with $V_{DS} = 50, 100, 200, 300, 400, 500, 600, 700\,V$ and $V_{GS} = 4, 5, 6, 7, 8\,\text{V}$ were

used as training data. Each data point requires one double pulse test. Therefore, 40 double pulse tests are required in total to obtain the training data. It is worth mentioning that although the breakdown voltage of the device under test is 1200 V, the I-V characteristics at $V_{DS} = 1200\,\text{V}$ cannot be measured using this method because the overshoot voltage during the switching transient might exceed the breakdown voltage and damage the device. In practice, the maximum allowable DC voltage across the device is de-rated to avoid breakdown. Therefore, the I-V characteristics up to the designed maximum DC voltage were measured. In this thesis, the DC source voltage is 600 V. The I-V characteristics up to 700 V were measured and used to train the model considering the voltage overshoot.

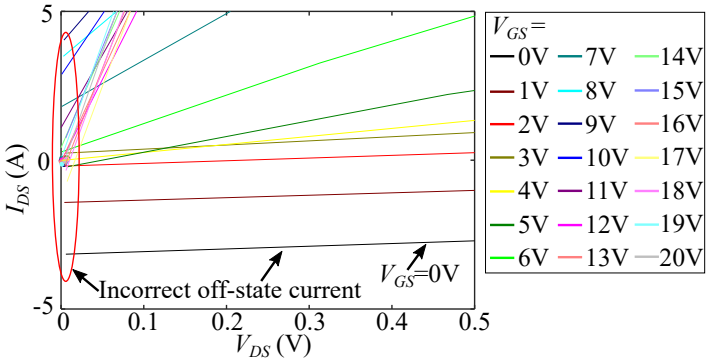
The measured I-V characteristics in the whole operation region (i.e., both low and high V_{DS} regions) were used to train the ANN model in Fig. 4.1. The Neural Net Fitting Toolbox in MATLAB based on backpropagation algorithm was used. The performance of the trained ANN model is shown in Fig. 4.3. In Fig. 4.3a , it can be seen that the trained ANN model can match the I-V characteristics in the whole V_{DS} region. However, the cutoff region still cannot be correctly modelled in Fig. 4.3b.

4.3.2 Hybrid Modelling with Behaviour-based Model for Cutoff Region

As discussed in Section 4.2, the cutoff region cannot be modelled correctly by the ANN shown in Fig. 4.1. One possible solution is to increase the number of neurons to reduce the errors, but it might cause overfitting problems which will be discussed in Section 4.3.4. Instead of the ANN model which is purely data-driven without considering any physical behaviours, simple equations are very suitable for cutoff region due to the simple physical characteristics in this region. Therefore, we propose a hybrid modelling method that uses equations to model the low-voltage cutoff region and a DPT-data-based ANN to model the high voltage behaviour. According to the semiconductor characteristics of SiC MOSFETs, the



(a) Performance in whole V_{DS} region.



(b) Performance in cutoff region.

Figure 4.3: ANN model trained with I-V characteristics in whole V_{DS} region. (Solid lines denote the simulated data. Dots denote the measured data.)

cutoff region can be divided into two parts:

1) Part I: $V_{GS} < V_{GS(th)}$

When $V_{GS} < V_{GS(th)}$, the drain-to-source current is pinched off since a conductive current channel is not formed due to the insufficient gate-to-source electrical field. To incorporate this physical behaviour with the ANN model, a hyperbolic function is used to model the cutoff region when $V_{GS} < V_{GS(th)}$:

$$I_{DS} = f_{ANN}\left(V_{DS}, V_{GS}\right) \cdot f_{cutoff}\left(V_{GS}\right). \tag{4.3}$$

$$f_{cutoff}\left(V_{GS}\right) = \frac{1}{2}\left(1 + \tanh\left(\alpha\left(V_{GS} - V_{GS(th)}\right)\right)\right). \tag{4.4}$$

The threshold voltage can be measured by a curve tracer. The hyperbolic function is used to keep the model continuous. α is set large enough ($\alpha = 10$) to make sure

that $I_{DS} \approx 0$ when $V_{GS} < V_{GS(th)}$ and $I_{DS} \approx f_{ANN}(V_{DS}, V_{GS})$ when $V_{GS} > V_{GS(th)}$.

2) Part II: $V_{DS} = 0\,\mathrm{V}$

I_{DS} should be zero when $V_{DS} = 0\,\mathrm{V}$. To model this physical behaviour, the linear region where V_{DS} is close to $0\,\mathrm{V}$ is modelled together. According to the physical characteristics of SiC MOSFETs, when $V_{GS} > V_{GS(th)}$ and V_{DS} is smaller than the saturation voltage V_{sat}, the MOSFET operates like a resistor controlled by V_{GS}. Therefore, the linear region can be modelled by the following proportional function:

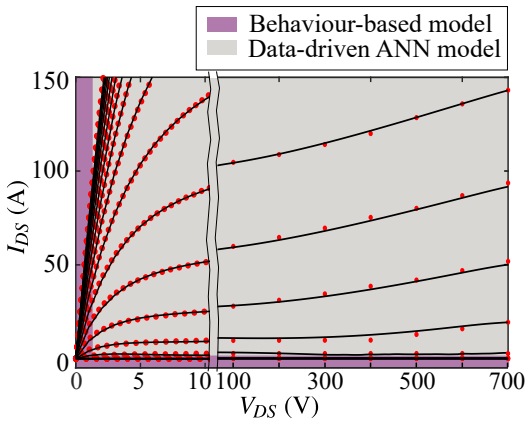
$$I_{DS} = \frac{f_{ANN}(V_{sat}, V_{GS})}{V_{sat}} \cdot V_{DS} \quad \text{if } 0 \leq V_{DS} < V_{sat}. \tag{4.5}$$

For the selected power module CAS120M12BM2, the linear region is $0\,\mathrm{V} \leqslant V_{DS} \leqslant 2\,\mathrm{V}$. Therefore, $V_{sat} = 2\,\mathrm{V}$ is selected. This equation is valid in the linear region of the SiC MOSFET and it can also guarantee that the SiC MOSFET is cut off when $V_{DS} = 0\,\mathrm{V}$. $f_{ANN}(V_{sat}, V_{GS})/V_{sat}$ is used as the slope of the proportional equation to keep it continuous with the ANN model for convergence of the whole model.

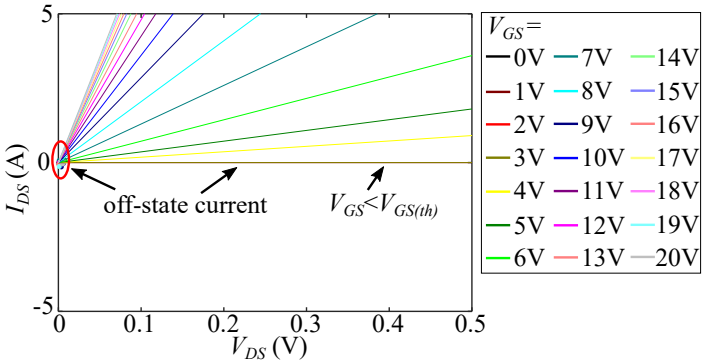
Finally, the hybrid data-driven model for I-V characteristics can be built by combining (4.4) and (4.5) with the ANN model in (4.1). The hybrid model is written as follows:

$$I_{DS} = \begin{cases} f_{ANN}(V_{DS}, V_{GS}) \cdot f_{cutoff}(V_{GS}), & \text{if } V_{DS} \geq V_{sat}, \\ f_{ANN}(V_{sat}, V_{GS}) \cdot \frac{V_{DS}}{V_{sat}} \cdot f_{cutoff}(V_{GS}), & \text{if } 0\,\mathrm{V} \leq V_{DS} < V_{sat}. \end{cases} \tag{4.6}$$

As shown in Fig. 4.4a, the I-V characteristics where $0\,V \leq V_{DS} < V_{sat}$ or $V_{GS} < V_{GS(th)}$, i.e., the region in purple, is modelled by behaviour-based model. The remaining part, i.e., the region in gray, is modelled by data-driven ANN model. As shown in Fig. 4.4, the I-V characteristics in the whole V_{DS} region and cutoff region can be accurately modelled by the proposed hybrid method.



(a) Hybrid I_{DS} model.

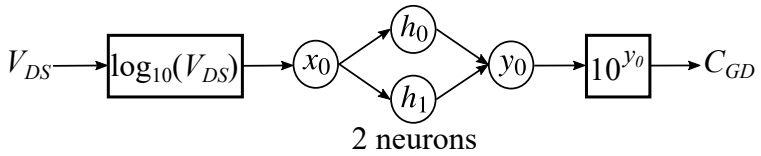


(b) Performance in cutoff region.

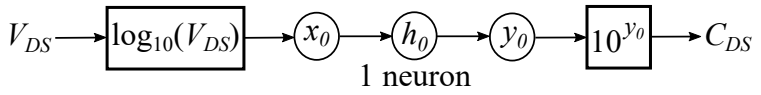
Figure 4.4: Performance of the proposed hybrid modelling methodology.

4.3.3 Modelling of C-V Characteristics

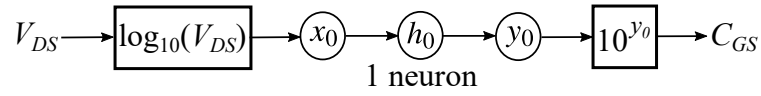
C-V characteristics are essential for transient simulation [46], which were built with ANNs in this study for accuracy and adaptability. It is worth noting that the measured C_{GD} reduces by almost 20 times from 2600 pF to 150 pF when V_{DS} changes from 0 V to 20 V but has only minor variations when $V_{DS} > 20$ V. The characteristics of C_{DS} are similar. Therefore, for model accuracy, the training data were measured in logarithmic scale and the logarithmic transformation is adopted in the ANN models to balance large data variations. The ANN models with logarithmic transformation are shown in Fig. 4.5. The number of neurons in the hidden layer to model C_{GD}, C_{GS} and C_{DS} are 2, 1 and 1 respectively. The C-V characteristics were measured using the curve tracer B1505A. The input capacitance C_{iss}, output capacitance C_{oss} and reverse transfer capacitance C_{rss} were measured as a function of V_{DS} from 0.01 V to 1000 V in logarithmic scale with



(a) C_{GD} model.



(b) C_{DS} model.



(c) C_{GS} model.

Figure 4.5: ANN capacitance models trained in logarithmic scale.

251 data points. The gate-to-source capacitance C_{GS}, gate-to-drain capacitance C_{GD} and drain-to-source capacitance C_{DS} can be calculated accordingly:

$$\begin{cases} C_{GD} & = C_{rss} \\ C_{GS} & = C_{iss} - C_{rss} \\ C_{DS} & = C_{oss} - C_{rss}. \end{cases} \tag{4.7}$$

The calculated C_{GD}, C_{GS} and C_{DS} were used as training data to train the ANN models. Besides, the nonlinear C_{GS} characteristics, on-state and dynamic C_{GS} characteristics measured by the proposed DPT-based measurement method in Chapter 3 were also added to the training dataset. As shown in Fig. 4.6, Fig. 4.7 and Fig. 4.8, the ANN models can simulate the capacitance characteristics accurately.

4.3.4 Modelling Flowchart and Neural Network Selection

The flowchart of the proposed modelling methodology is summarised in Fig. 4.9. The *I-V* characteristics were measured by a curve tracer and DPT to train the ANN model. A behaviour-based model for cutoff region was built with measured $V_{GS(th)}$ and V_{sat}. The hybrid I_{DS} model was built by combining the behaviour-

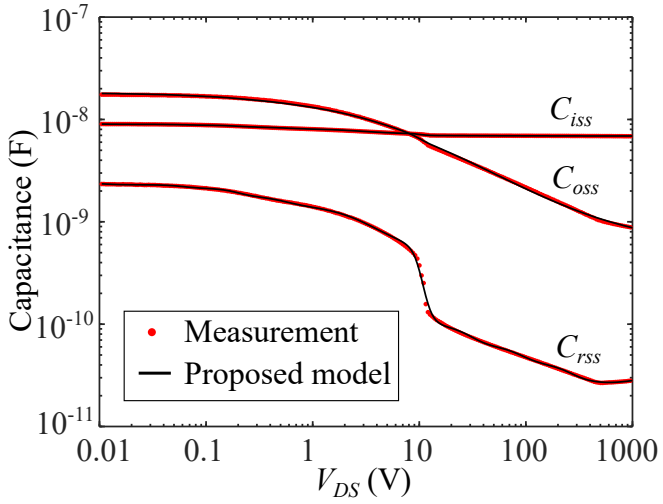


Figure 4.6: Results of ANN capacitance models trained in logarithmic scale.

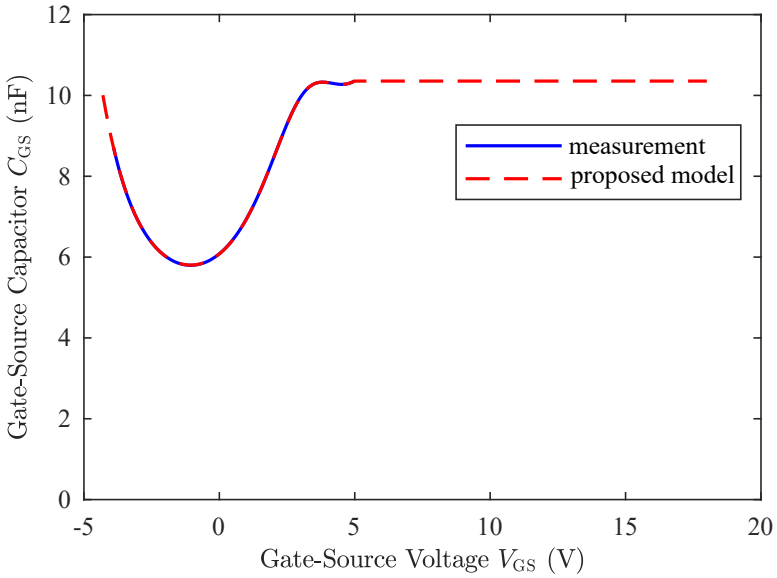


Figure 4.7: Modelling of the nonlinear C_{GS}-V_{GS} characteristics measured by the proposed DPT-based measurement method.

based model with ANN model. C-V characteristics were measured to train the ANN models of C_{GD}, C_{DS} and C_{GS} in logarithmic scale.

For the neural network selection, there is no exact standard to follow to determine the number of layers and neurons of the ANN for a certain application [101]. In this study, it is shown that ANNs with single hidden layer are sufficient to model the nonlinear I-V and C-V characteristics of SiC MOSFETs. The analytical formulas of single-hidden-layer ANNs can also be obtained straightforwardly. ANNs with more than one hidden layer can also be used, but the analytical formulas

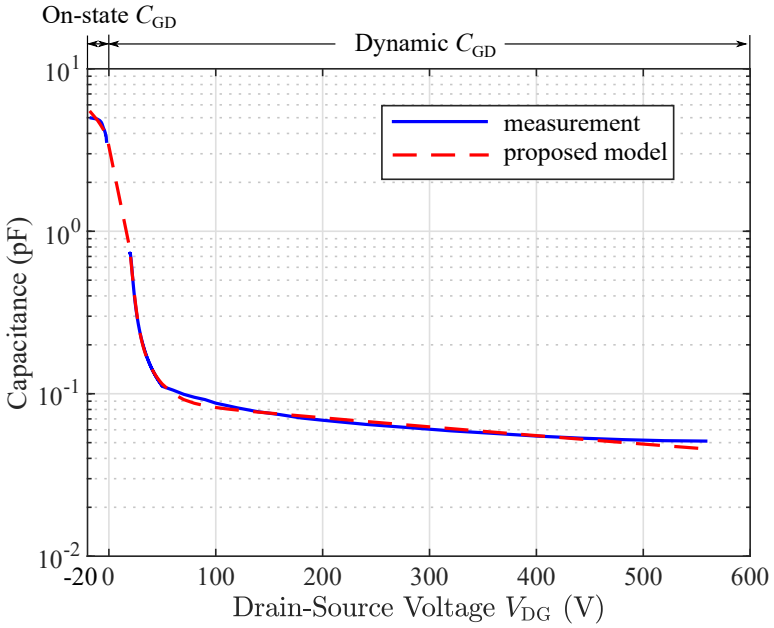


Figure 4.8: Modelling of on-state and dynamic C_{GD}-V_{DG} characteristics measured by the proposed DPT-based measurement method..

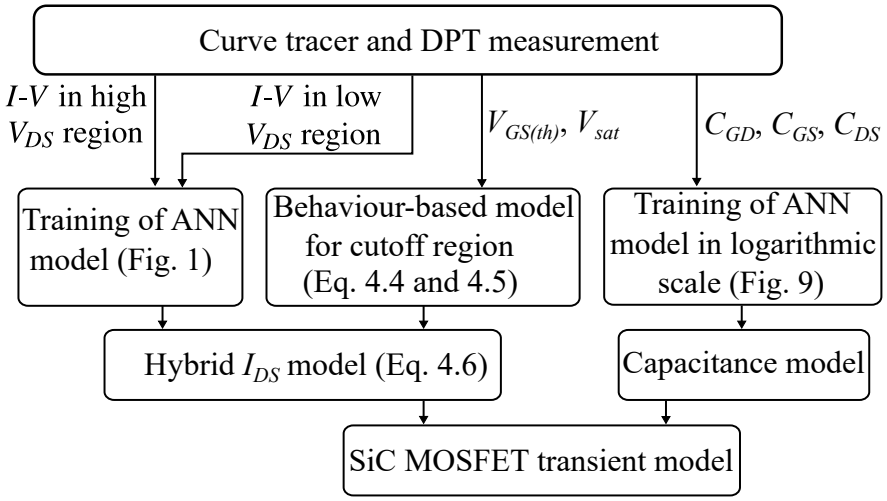


Figure 4.9: Flowchart of the proposed hybrid modelling methodology.

become more complex. The investigation of ANN models with different numbers of hidden layers is beyond the scope of this thesis.

After the single-hidden-layer ANN was selected, the number of neurons in the hidden layer should be chosen. The trial-and-error method was used, which was achieved by training ANNs with different numbers of neurons and selecting the minimum number of neurons that can provide accurate approximation. Although using more neurons can help reduce the training errors of ANNs, it will increase the computation time and might cause overfitting problems of ANNs [118]. The

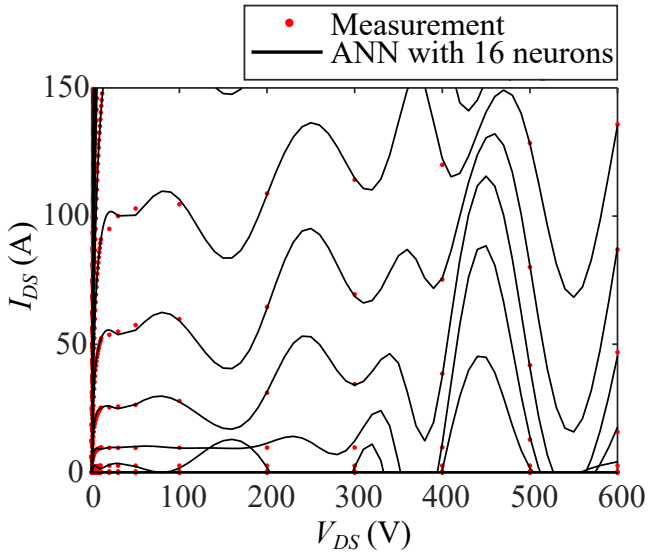
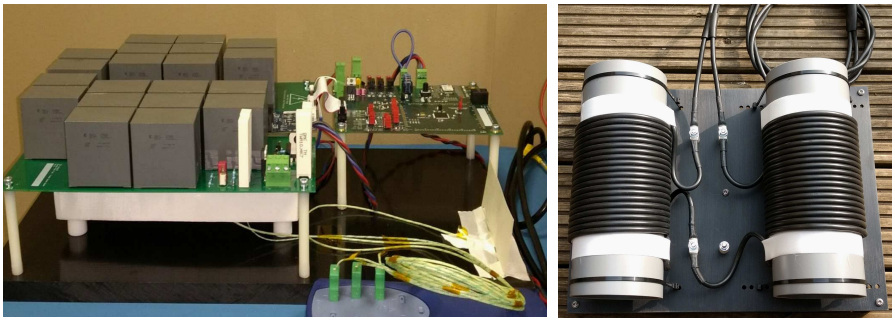


Figure 4.10: Overfitting of ANN with excessive hidden neurons.

overfitting phenomenon of the ANN with 16 hidden neurons to model the I-V characteristics is shown in Fig. 4.10. Although each measurement data (i.e., training data) can be accurately matched, the ANN cannot predict the the I-V characteristics correctly. In this thesis, single-hidden-layer ANN with 10 neurons was selected to model the I-V characteristics. ANNs with 2, 1 and 1 neurons were selected to model C_{GD}, C_{GS} and C_{DS} of a SiC MOSFET module, respectively. It is expected that a similar number of neurons is enough to model any SiC MOSFETs as they have similar shapes of I-V and C-V characteristics, although voltage and current levels are distinct.

Note that temperature characteristics of SiC MOSFETs are not considered here. The I-V characteristics, C-V characteristics and the switching transients of SiC MOSFETs were all measured at 25 °C. The temperature characteristics can be easily added into the model through adding a third input node to the ANN model in Fig. 4.1 and then training the model with temperature-dependent I-V data, which can be measured using a curve tracer and DPT.



(a) Double pulse tester. (b) Load inductor.

Figure 4.11: Experimental setup.

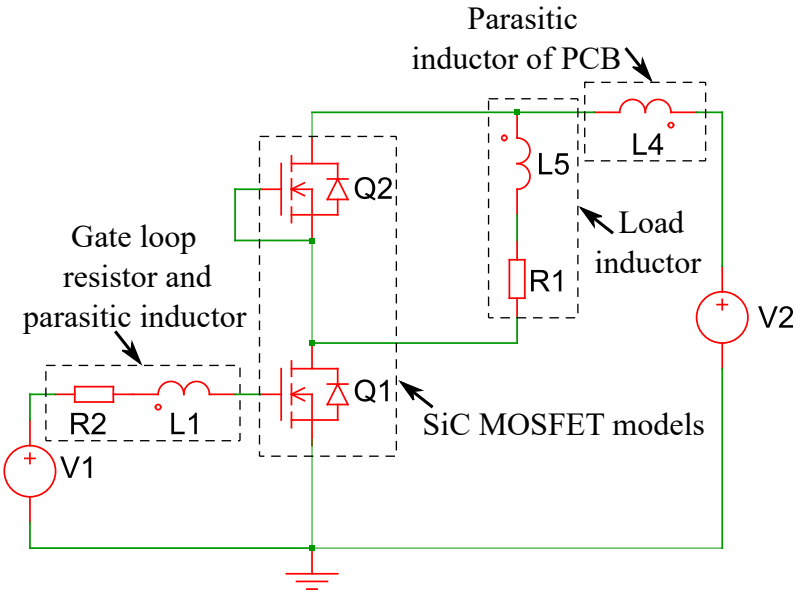


Figure 4.12: Simulation circuit of DPT in SIMetrix.

4.4 Experimental Model Verification

In this section, the simulated and experimental waveforms of the switching transients of SiC MOSFETs were compared using a double-pulse tester (DPT) to verify the proposed modelling method. To demonstrate the repeatability of the proposed modelling method, an 1200 V SiC half-bridge modules from Wolfspeed, i.e., CAS120M12BM2, was used to facilitate the verification. It was used to measure the training dataset. The training dataset was then used to train the ANN-based model. After the model was trained, the switching transients of SiC MOSFETs were simulated and compared with the switching waveforms measured from the same module.

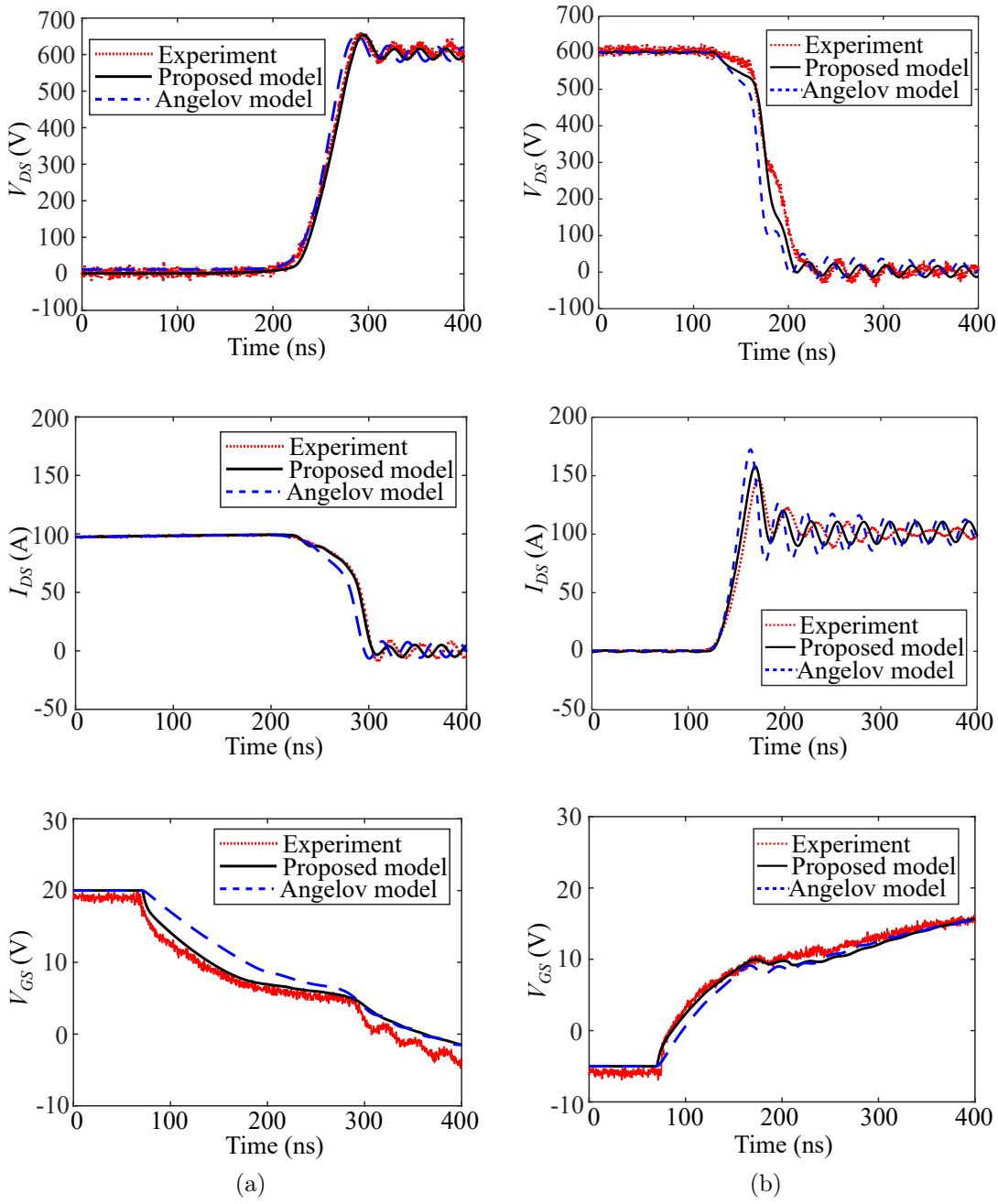


Figure 4.13: Measured and simulated (a) turn-off and (b) turn-on transients.

The proposed modelling method can be adopted in widely-used simulation tools such as SPICE simulators. A transient model of CAS120M12BM2 was built based on the proposed hybrid modelling method. It was then implemented in SIMetrix using Verilog-A language. Verilog-A is a widely-used modelling language for analog circuits, which can be used in a SPICE environment [119]. It is flexible with user defined functions and variable data types like arrays [120]. As a result, the matrix-based analytical equations in the trained ANN and cut-off region models can be easily implemented using Verilog-A. The anti-parallel diode model in [49] and the stray inductance of CAS120M12BM2 in [121] were used in the model. The internal gate resistor is 1.8 Ω measured using the Keysight curve tracer B1505A. Experiment and simulation platforms of DPT were built to verify the proposed modelling method for transient simulation.

In the experimental platform shown in Fig. 4.11a, a DPT with low stray inductance was designed for the half-bridge module CAS120M12BM2. A commercial gate driver CGD15HB62P1 for half-bridge module from Wolfspeed was used. Two air-core inductors were designed and connected in series as the load inductor as shown in Fig. 4.11b. For this inductor, the total inductance is 55.7 μH with a 0.064 Ω equivalent series resistance and an 140 pF equivalent parallel capacitance.

The DPT circuitry was simulated using SPICE simulator SIMetrix as shown in Fig 4.12. Q_1 and Q_2 are the proposed SiC MOSFET models. The DC-bus stray inductance was obtained by simulating the S-parameters of the PCB board in the schematic of Keysight Advanced Design System. The proposed model was simulated and then compared with the experimental results from DPT. As shown in Fig. 4.13, the simulated turn-on and turn-off waveforms of the proposed model can match the experimental results accurately. The turn-on/off delay time $T_{d(on)}$ and $T_{d(off)}$, rise/fall time T_r and T_f, turn-on/off losses E_{on} and E_{off} of the proposed model and the Angelov model were calculated and compared with experimental results in Table 4.1 and Table 4.2, respectively. The errors of the proposed model are all within 11%, which are much smaller than the the Angelov model.

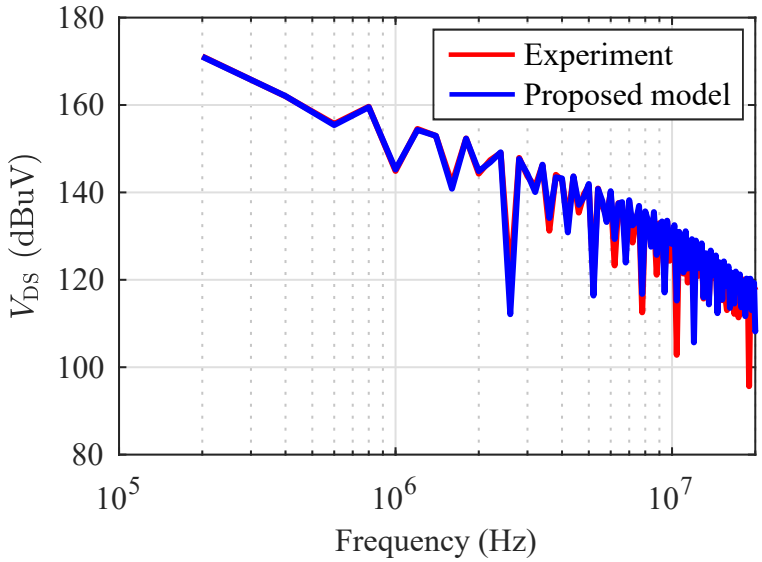


Figure 4.14: Comparison of Drain-Source voltage spectra of experimental and simulation results for EMI analysis.

To conduct the EMI analysis, the EM noise induced by the switching transients needs to be calculated in the frequency domain [122]. For this purpose, the simulated and experimental switching waveforms of the Drain-Source voltage presented in Fig. 4.13 were used for spectrum analysis. The spectra of the experimental and simulated Drain-Source voltage waveforms were computed via fast Fourier transformation in MATLAB. The comparison of the Drain-Source voltage spectra is shown in Fig. 4.14. The red line represents the spectrum of experimental result, and the blue one represents the spectrum of the simulation result derived from the proposed model. It is found that the simulated spectrum by the proposed model matches well with the experimentally obtained spectrum. The relative RMS error of the simulated spectrum extracted using the proposed model is 2.82%, which is calculated according to (4.8).

4.5 Comparisons with Angelov Model

In this section, the proposed hybrid data-driven model was compared with the commercial Angelov model proposed in [111] to further demonstrate the accuracy and speed of the proposed model. The Angelov model was selected for comparison

Table 4.1: Switching characteristics simulated by the proposed model.

Test conditions	Experiment	Proposed model	Errors of proposed model
Turn on	$T_{d(on)} = 87.6$ ns	$T_{d(on)} = 78.6$ ns	10.27%
	$T_r = 44.0$ ns	$T_r = 48.7$ ns	10.68%
	E_{on} =2.649 mJ	E_{on} =2.818 mJ	6.39%
Turn off	$T_{d(off)} = 155.5$ ns	$T_{d(off)} = 156.1$ ns	0.39%
	$T_f = 46.3$ ns	$T_f = 45.2$ ns	2.38%
	E_{off} =1.556 mJ	E_{off} =1.637 mJ	5.21%

Table 4.2: Switching characteristics simulated by the Angelov model.

Test conditions	Experiment	Angelov model	Errors of Angelov model
Turn on	$T_{d(on)} = 87.6$ ns	$T_{d(on)}$ =57.1 ns	34.82%
	$T_r = 44.0$ ns	$T_r = 53.0$ ns	20.45%
	E_{on} =2.649 mJ	E_{on} =2.072 mJ	21.87%
Turn off	$T_{d(off)} = 155.5$ ns	$T_{d(off)}$ =126.3 ns	18.78%
	$T_f = 46.3$ ns	$T_f = 43.5$ ns	6.05%
	E_{off} =1.556 mJ	E_{off} = 1.738 mJ	11.70%

because it is a standard industry behavioural model from Keysight to simulate transient waveforms of SiC MOSFETs accurately [79]. Besides, compared to other models from manufacturers and researchers, a modelling software IC-CAP has been developed by Keysight to automatically extract the model parameters of the Angelov model for a SiC MOSFET. To facilitate the comparison, the same measured data were used to build the proposed model and the Angelov model. The parameters of the Angelov model were extracted in IC-CAP. Although the parameters of the Angelov model can be automatically extracted in IC-CAP by fitting the simulated data to the measured data, the accuracy of the fitting results was not satisfactory. The parameters still need to be tuned manually to achieve the required accuracy. Afterwards, the Angelov model is used as Q_1 and Q_2 in

Fig. 4.12 to simulate the switching transient waveforms in a DPT circuit.

4.5.1 Model Accuracy

The transient simulations of both models are compared in Fig. 4.13, against experimental results from DPT. It can be seen that the proposed model is more accurate than the Angelov model comparing to the experimental turn-on/off waveforms. The turn-on/off delay time $T_{d(on)}$ and $T_{d(off)}$, rise/fall time T_r and T_f, turn-on/off losses E_{on} and E_{off} of both models were calculated and compared with experimental results in Table 4.1. The comparison shows that the proposed model has smaller errors than Angelov model. The errors of the proposed model are reduced by at least two times comparing to the Angelov model.

The relative root-mean-square (RMS) error were used to quantitatively compare the accuracy of switching waveforms of these two models. The relative RMS Error can be calculated as follows:

$$\text{Relative RMS Error} = \sqrt{\frac{\sum_{i=1}^{N} |m_i - s_i|^2}{\sum_{i=1}^{N} |m_i|^2}} \times 100\%. \tag{4.8}$$

where m_i and s_i denote the measured and simulated values (V_{DS}, V_{GS} and I_{DS} in Fig. 4.13) at the i-th data point, respectively; N denotes the total number of data points.

The calculated relative RMS errors of the simulated switching waveforms in Fig. 4.13 are shown in Table 4.3. The relative RMS errors of the proposed model are $1.5 \sim 3$ times smaller than those of the Angelov model.

In Fig. 4.14, the relative RMS error of the simulated Drain-Source voltage spectrum obtained via the proposed model is 2.82%. As a comparison, the RMS error of the simulated spectrum obtained via the Angelov model is 4.26%, which is about 1.5 times higher compared to the proposed model.

Although both models were built with the same measured I-V and C-V characteristics, the proposed model is more accurate than the Angelov model in transient

Table 4.3: Relative RMS errors of switching transients.

Test conditions	Transient waveforms	Proposed model	Angelov model
Turn off	V_{DS}	3.84%	5.96%
	I_{DS}	3.43%	12.07%
	V_{GS}	4.04%	15.24%
Turn on	V_{DS}	6.33%	13.76%
	I_{DS}	6.21%	20.80%
	V_{GS}	3.99%	11.85%

Table 4.4: Relative RMS errors of C-V and I-V characteristics.

	C_{iss}	C_{oss}	C_{rss}	I_{DS}
Proposed model	0.37%	1.7%	1.8%	2.81%
Angelov model	1.31%	4.99%	10.02%	9.63%

simulation. This is because the proposed model can match the measured I-V and C-V data more accurately than the Angelov model. The simulated I-V and C-V characteristics of the proposed model and Angelov model were compared with the measured characteristics in Fig. 4.15 and Fig. 4.16, which show that the proposed model can match the measured data more accurately than the Angelov model.

The relative RMS errors of the C-V and I-V characteristics of the proposed model and Angelov model are calculated according to Fig. 4.15 and Fig. 4.16 and the results are shown in Table 4.4. The relative RMS errors of the proposed model are much smaller than those of the Angelov model. Consequently, the proposed model can provide more accurate transient simulation results for switching losses and EMI analysis.

4.5.2 Computation Time

The computation time of the proposed model was compared with the Angelov model through simulating the same DPT circuit in SIMetrix for 40 μs. The runtime of the simulations was recorded, which was directly captured by SIMetrix.

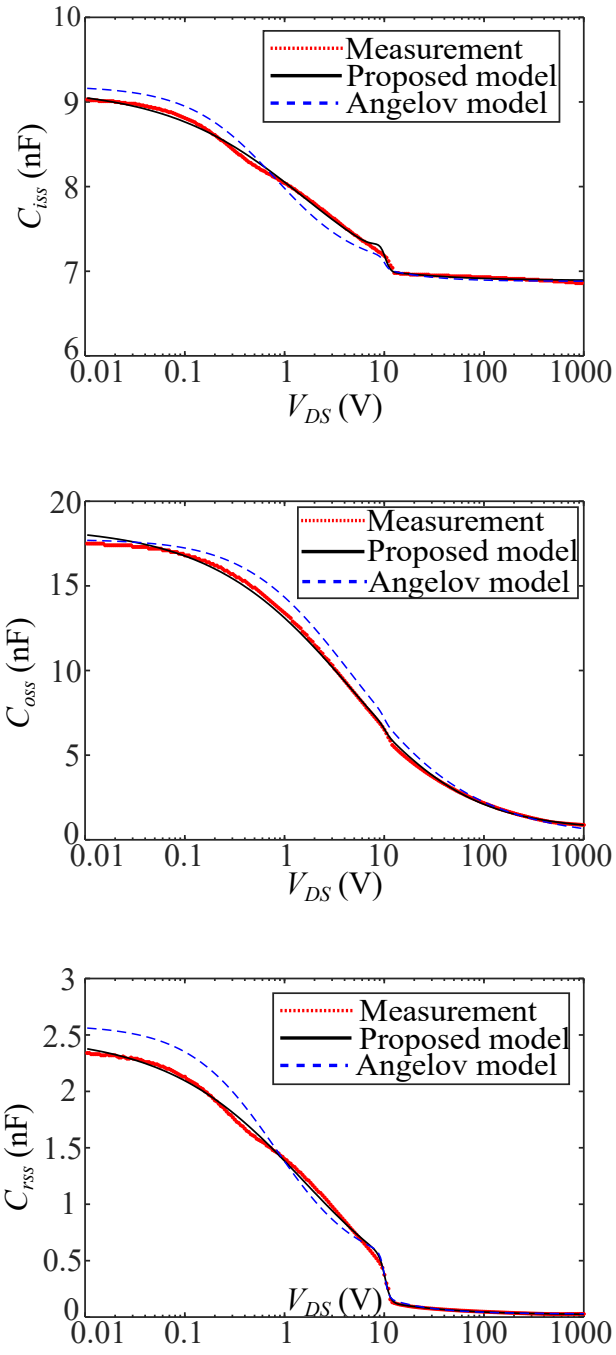


Figure 4.15: Comparison of C-V characteristics of proposed model and Angelov model.

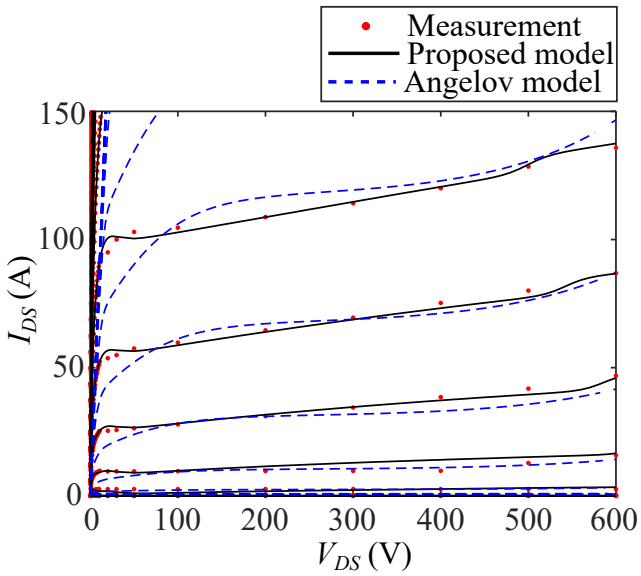


Figure 4.16: Comparison of I-V characteristics of proposed model and Angelov model.

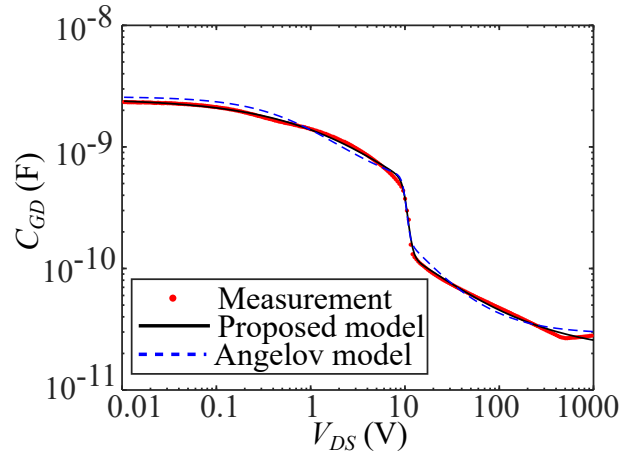
Table 4.5: Computation time of the proposed model and Angelov model.

	Proposed model	Angelov model
Simulation runtime (s)	3.13	4.46

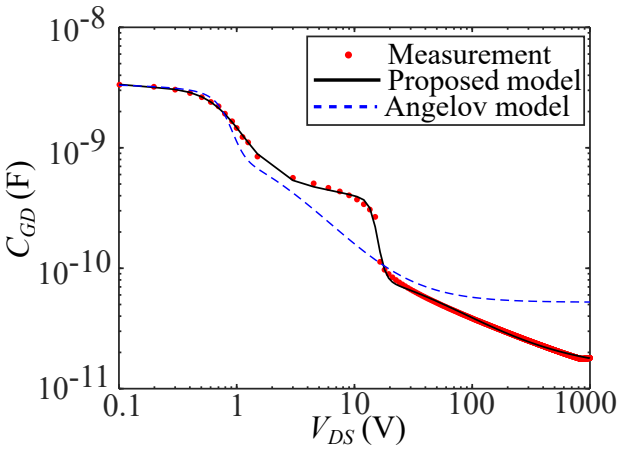
For accuracy, the simulation of each model was repeated 20 times in SIMetrix and the average runtime was used. The computer configuration used for the comparison is: Intel Core i7-8650U CPU@1.9GHz, 16-GB RAM. The version of SIMetrix is 8.00g and the default solver parameters of SIMetrix were used. It is shown in Table 4.5 that the runtime of the proposed model when simulating the DPT circuit is about 30% less compared to the Angelov model.

4.5.3 Model Adaptability

SiC MOSFETs from different manufacturers might have different device characteristics due to technology differences. Although both the proposed model and Angelov model can be used to model different SiC MOSFETs, the parameters of both models must be adjusted according to the characteristics of each MOSFET. For the proposed model, the weights and biases of the ANNs are trained by different device characteristics according to the flowchart in Fig. 4.9. For the Angelov



(a) CAS120M12BM2 from Wolfspeed.

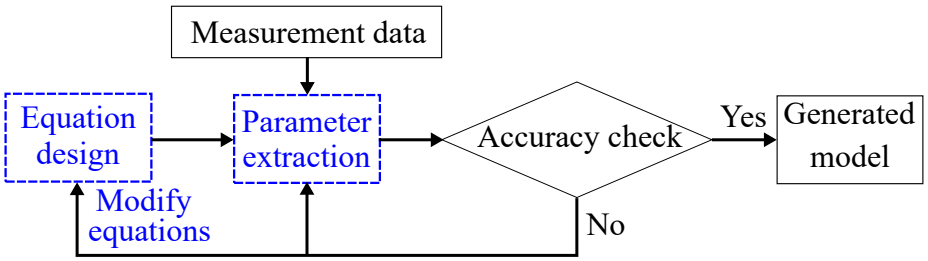


(b) MSC025SMA120S from Microsemi.

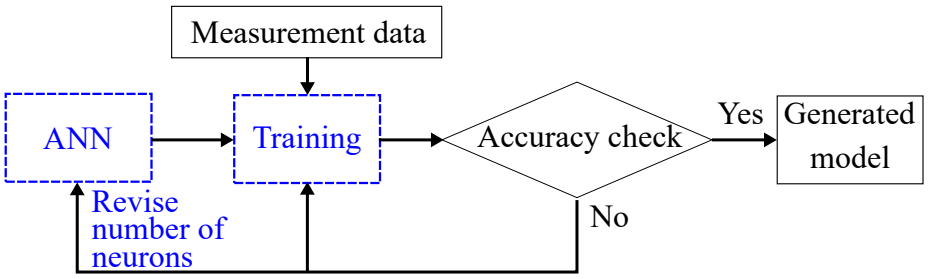
Figure 4.17: Simulated and measured C_{GD} characteristics of two different devices.

model, the parameters are extracted based on the curve fitting method to match specific device characteristics.

In Fig. 4.17, the C_{GD} characteristics of two SiC MOSFETs were measured and modelled by the proposed model and the Angelov model. The first device is CAS120M12BM2 from Wolfspeed and the second one is MSC025SMA120S from Microsemi. It is shown that these two devices have different C_{GD} characteristics. As the conventional behavioural model, the Angelov model can well match the C_{GD} characteristics of CAS120M12BM2, but it failed to accurately match the C_{GD} characteristics of MSC025SMA120S. The proposed ANN-based model has much better adaptability comparing to the Angelov model. The different C_{GD} characteristics of both devices can be simulated accurately by the proposed model.



(a) Angelov model.



(b) Proposed ANN-based model.

Figure 4.18: Modelling processes of Angelov and proposed ANN-based model.

4.5.4 Modelling Process

Both Angelov and the proposed ANN-based models are parameter based models. Parameters of the proposed model are more difficult to be manually altered because there are no clear relationship between the ANN parameters and the model behaviour. However, thanks to the well-developed Neural Net Fitting Toolbox in MATLAB, the parameters of the ANN-based model can be trained automatically. The general modelling processes of the Angelov model and the proposed ANN-based model are shown in Fig. 4.18. The difference between the modelling processes of two models is highlighted in blue dashed blocks.

For the Angelov model, the mathematical equations are firstly designed according to the device characteristics. Afterwards, the parameters of the equations are extracted. If the parameter extraction results are not accurate enough after the manual tuning, the equations in the original Angelov model need to be modified and the parameters need to be extracted again. As a result, there is potentially a lot of manual work, which is time-consuming and requires expert experience.

On the other hand, for the proposed ANN-based model, the single-hidden-layer ANN is used so there is no need to design complicated equations. The training

of ANN is fully automatic based on Neural Net Fitting Toolbox in MATLAB. If the training results are not accurate enough, the ANN model can be modified by simply revising the number of neurons in the hidden layer and the modified model can be trained quickly. Comparing to the conventional modelling process, the ANN-based modelling process requires less manual work so is more time-efficient.

4.6 Verification of Proposed DPT-based Measurement Method

4.6.1 Experimental Verification

In Chapter 3, the DPT-based measurement method was proposed to measure the dynamic-state characteristics. The measured dynamic-state characteristics, together with the conventionally-measured static-state I-V and C-V characteristics were used to built the model in order to accurately simulate the switching behaviour of the SiC MOSFETs. These dynamic-state characteristics include the I-V characteristics in the high V_{DS} region in Fig. 4.3a, nonlinear C_{GS} characteristics in Fig. 4.7, on-state and dynamic C_{gd} characteristics in 4.8. The effectiveness of the proposed DPT-based method on improved simulation accuracy is validated in this section.

The method was verified by comparing the simulated and experimental waveforms of the switching transients of SiC MOSFETs using a DPT. The comparisons are shown in Figs. 4.19-4.23 under the operating conditions of $V_{DC} = 600\,\text{V}$, $I_L = 100\,\text{A}$, $R_{G,ext} = 10\,\Omega$ and $L = 55.7\,\mu\text{H}$. The switching waveforms of V_{DS}, V_{GS} and I_{DS} were obtained using an oscilloscope (MSO58; Tektronix; Bandwidth: 1 GHz). In Figs. 4.19-4.23, the left figures show the turn-on waveforms and the right figures show the turn-off waveforms. The dotted lines represent the experimental waveforms while the solid lines represent the simulated waveforms.

The comparison was made step-by-step to clearly show the impact of the pro-

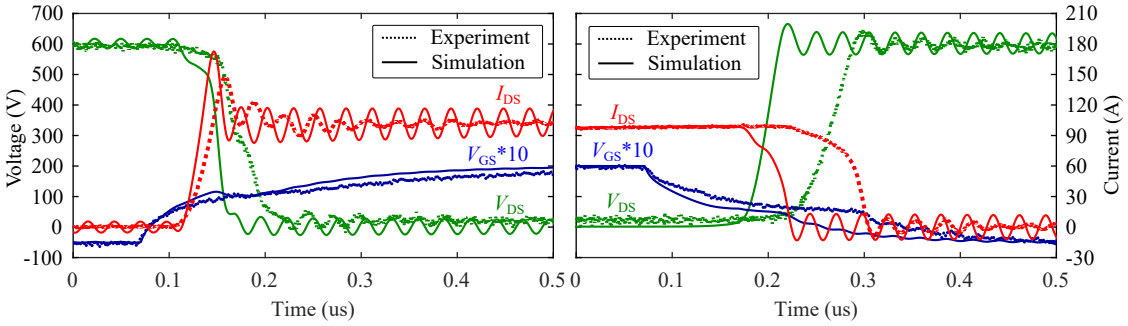


Figure 4.19: Simulated and experimental turn-on (left) and turn-off (right) waveforms. The device is modelled based on the datasheet.

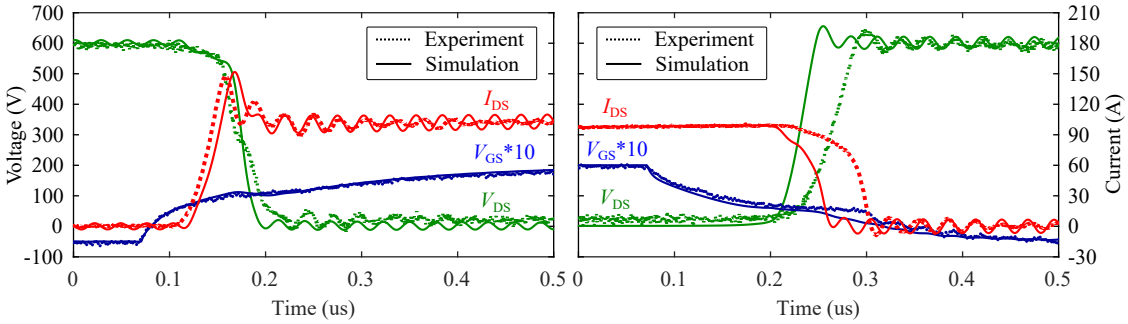


Figure 4.20: Simulated and experimental turn-on (left) and turn-off (right) waveforms. The device is modelled with measured nonlinear C_{GS}.

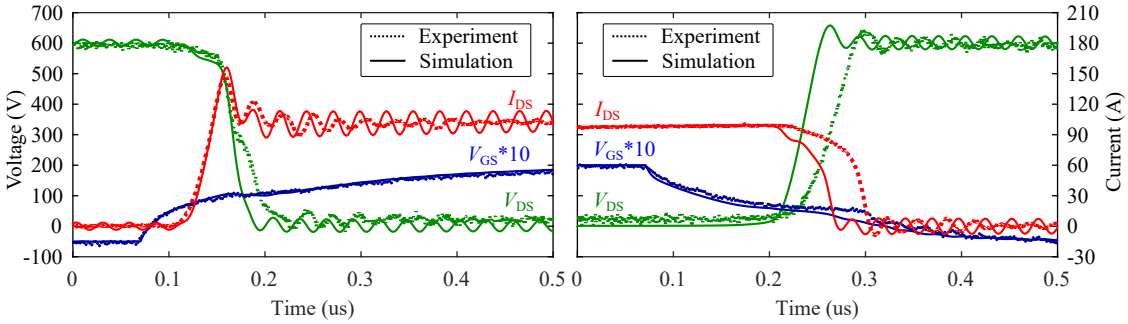


Figure 4.21: Simulated and experimental turn-on (left) and turn-off (right) waveforms. The device is modelled with measured nonlinear C_{GS} and I-V characteristics in the high V_{DS} region.

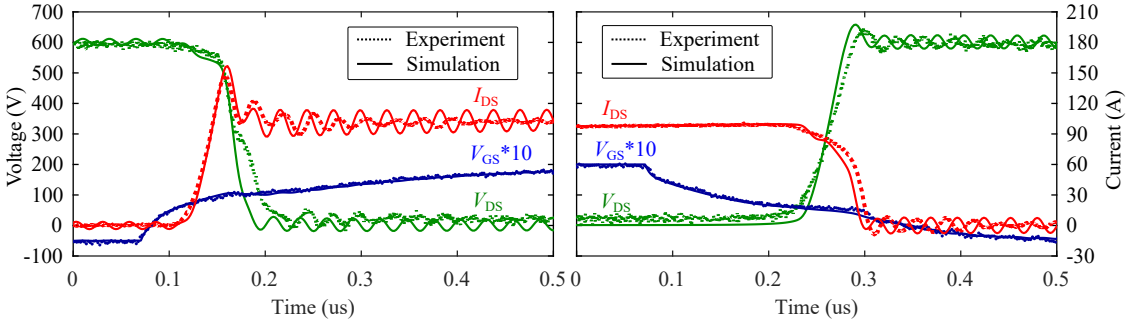


Figure 4.22: Simulated and experimental turn-on (left) and turn-off (right) waveforms. The device is modelled with measured nonlinear C_{GS}, I-V characteristics in the high V_{DS} region and on-state C_{GD}.

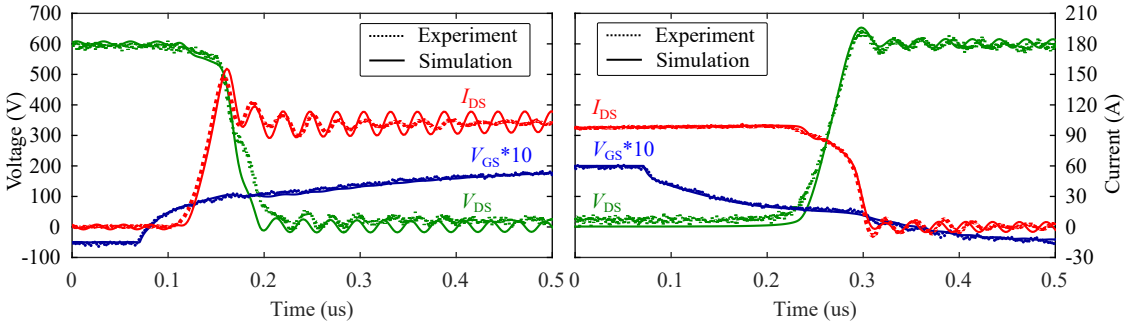


Figure 4.23: Simulated and experimental turn-on (left) and turn-off (right) waveforms. The device is modelled with all measured characteristics.

posed DPT-based measurement method on the model accuracy. Firstly, the conventional model was built without using any dynamic-state characteristics measured by the proposed DPT-based measurement method. In other words, the conventional model was built based on the static-state I-V and C-V characteristics as shown in Fig. 4.2a and Fig. 4.6, which were measured by the conventional method based on Keysight B1505A power device analyser. The simulated switching waveforms of the conventional model were compared to the experimental results in Fig. 4.19. The comparison shows significant mismatch between simulation and experiment.

Secondly, the conventional model was improved by considering the nonlinear C_{GS} characteristics measured by the proposed DPT-based method. The results are shown in Fig. 4.20. It can be seen that the simulated V_{GS} during the turn-on transient can match the experimental results accurately. As a result, the simulated V_{DS} and I_{DS} also get closer to the experimental results. This is because the turn-on process depends on the charging process of C_{iss} ($C_{iss} = C_{GS} + C_{GD}$). At the beginning of the turn-on process under high V_{DS}, C_{GD} is negligible comparing to C_{GS}. Therefore, the simulated turn-on waveforms can be improved by considering the nonlinear C_{GS} characteristics.

Thirdly, the model further considered the I-V characteristics in the high V_{DS} region measured by the proposed DPT-based method. The simulated switching waveforms are compared with the experimental results in Fig. 4.21. It is shown that after considering the I-V characteristics in the high V_{DS} region, the turn-on

Table 4.6: Relative RMS errors of switching transients.

Test conditions	Transient waveforms	Improved model	Datasheet-based model
Turn off	V_{DS}	3.84%	45.93%
	I_{DS}	3.43%	47.70%
	V_{GS}	4.04%	31.66%
Turn on	V_{DS}	6.33%	27.93%
	I_{DS}	6.21%	20.32%
	V_{GS}	3.99%	14.60%

waveforms, especially the I_{DS} waveform during the turn-on transient can match the experimental results accurately. However, it can be seen that the simulated turn-off waveforms still has large errors. The accuracy of the simulated turn-off waveforms can be improved in the following steps by considering the measured on-state and dynamic C_{GD} characteristics.

Fourthly, the on-state C_{GD} measured by the proposed DPT-based method was further considered in the model. As a result, the simulated V_{GS} during the turn-off transient can also match the experimental results accurately as shown in Fig. 4.22. This is because the turn-off process depends on the discharging process of C_{iss}, where C_{GD} is non-negligible under low V_{DS}. Since the device is still in on state at the beginning of the turn-off process, the on-state C_{GD} has to be considered in the model. In Fig. 4.22, due to the accurate simulation of V_{GS} in the turn-off transient, the simulated turn-off waveforms of V_{DS} and I_{DS} also become more accurate compared to the results in Fig. 4.21.

Finally, the dynamic C_{GD} measured by the proposed DPT-based method was added in the model so that all the measured data by the proposed measurement methods were modelled. It can be seen from the results shown in Fig. 4.23 that by considering the dynamic C_{GD} in the model, the model accuracy is further improved. Especially, the simulated turn-off waveforms can match the experimental results accurately.

4.6.2 Comparison with Conventional Measurement Method

The model which only considers the conventionally-measured I-V and C-V characteristics is denoted as the conventional model. The model which considers all the measured data by the proposed DPT-based measurement method is denoted as the improved model. The simulated switching waveforms of both models have been compared in Fig. 4.19 and Fig. 4.23. The relative root-mean-square (RMS) error presented in (4.8) were used to quantitatively analyse the accuracy of the models [31].

The relative RMS errors of the simulation waveforms of V_{DS}, V_{GS} and I_{DS} are calculated and compared according to (4.8). As shown in Table 4.6, the relative RMS errors of the improved model are at least 3 times smaller than those of the conventional model. The proposed measurement method can improve the model accuracy effectively so that the model can successfully predict the switching waveforms of SiC MOSFETs in power electronics converters.

4.7 Summary

In this chapter, a hybrid data-driven modelling methodology has been proposed to model SiC MOSFETs for accurate and fast transient simulation. To accurately model the high-speed switching transients, the required training dataset were identified and then measured to train the proposed ANN model. The trained ANN was combined with the behaviour-based equations to accurately model the cut-off region and to avoid overfitting the ANN model. In addition, the C-V characteristics were modelled in logarithmic scale using ANNs for accuracy. The accuracy of the proposed modelling method have been verified through modelling and testing a SiC MOSFET module CAS120M12BM2. The simulated transient waveforms were compared with the experimental turn on/off waveforms from a DPT to demonstrate the accuracy of the proposed modelling methodology.

To further demonstrate the accuracy and speed of the proposed model, it has

been compared with the Angelov model in detail. The switching transients of the proposed model are $1.5 \sim 3$ times closer to the experimental results compared to the Angelov model. The runtime of both models was compared through simulating the same DPT circuit in SPICE simulator SIMetrix. The simulation runtime of the proposed hybrid model is found to be 30% reduced compared to the Angelov model. Besides, the proposed hybrid data-driven modelling method has better adaptability to model devices from different manufacturers and the modelling process of the proposed method is more convenient and time-efficient.

Besides, the proposed modelling method was used to validate the effectiveness of the DPT-based characterisation method proposed in Chapter 3. The comparison results show that the simulation accuracy is increased by at least 3 times after considering the dynamic-state characteristics measured by the DPT-based method.

Chapter 5

Datasheet-based Fast Modelling of SiC MOSFETs

In this chapter, a datasheet-based modelling approach is proposed with a step-by-step parameter extraction procedure that can be easily followed by users. The model is completely based on the characteristics of the SiC MOSFET obtained from the datasheet without the need of further data or equipment so that it provides a more cost and time-efficient process for converter designers to quickly develop the model and validate their converter design. The datasheet-based modelling method is also compared with the measurement-based modelling method proposed in Chapter 4 to provide a guidance for converter designers to choose the proper method for their own applications.

5.1 Introduction

Although the measurement-based modelling method can deliver an accurate model for transient simulation based on measured characteristics, in some cases, measurement of SiC MOSFET is not achievable due to limited resources and high cost. From this perspective, a datasheet-based modelling approach without the need of measurement equipment is preferred because it can be adopted by all designers to quickly develop their models. Many manufacturers have provided transient simu-

lation models along with the datasheets for their discrete devices. These models can be directly used by designers. However, the models for SiC MOSFETs power modules are currently not provided by manufacturers. There is a need to build models for these power modules based on the datasheets provided by manufacturers.

The datasheet-based models are usually based on mathematical equations developed by manufacturers or power electronics designers. The equation parameters need to be extracted based on the I-V and C-V characteristics provided by a datasheet. The datasheet-based models usually contain complicated nonlinear equations and multiple parameters to accurately model the I-V and C-V characteristics [49, 96, 105, 106, 108]. Although the same model can be used for different SiC MOSFETs, the parameters in the model are distinct. Therefore, the model parameters should be extracted based on the datasheet of the specific SiC MOSFET. Although there are various models in the literature, the parameter extraction procedure of these models are either too complicated or not well-established, which hinders the application of the models for converter designers. Therefore, a step-by-step parameter extraction procedure is required.

To address the above challenges of existing datasheet-based modelling methods, this chapter proposed a step-by-step datasheet-based modelling approach for SiC MOSFETs. The drain-to-source current, anti-parallel diode and parasitic capacitors were accurately modelled based on datasheet. The temperature dependency was considered. A SPICE model for a commercial SiC MOSFET power module was built based on the proposed modelling approach. The established model was verified by comparing experiment and PSpice simulation results of the same double pulse tester (DPT).

The contributions of this chapter include:

1. A step-by-step parameter extraction procedure of the model equations was introduced. By doing this, this modelling approach can be easily followed by converter designers to model other SiC MOSFETs quickly and accurately.

(a) (b)

Figure 5.1: A 1200-V 120-A SiC MOSFET half-bridge power module CAS120M12BM2: (a) package, (b) schematic.

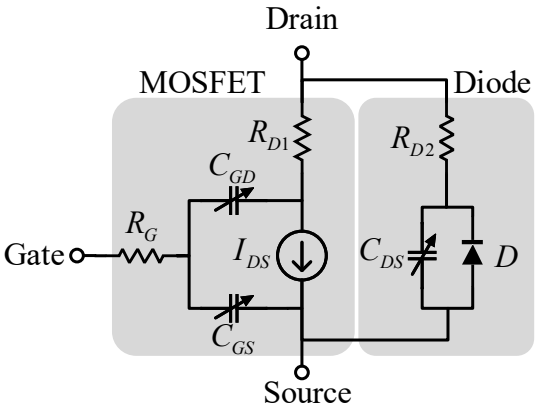


Figure 5.2: Subcircuit model of a pair of SiC MOSFET and anti-parallel diode in the power module.

2. A comprehensive comparison was made between the datasheet-based modelling method proposed in this chapter and the measurement-based model proposed in Chapter 4, in terms of accuracy, complexity and usage. This can provide a guidance for converter designers to choose the proper model for their own applications.

The rest of this chapter is organised as follows: Section 5.2 provides the detailed description of the datasheet-based model. The step-by-step modelling approach are illustrated in Section 5.3. In Section 5.4, the datasheet-based model is verified by comparing the simulation results with the experimental results. Section 5.5 compares the datasheet-based model with the measurement-based model. The conclusions are summarised in Section 5.6.

5.2 Model Description

A 1200V 120A SiC half-bridge module CAS120M12BM2 [43] from Wolfspeed is used to explain the proposed modelling approach. The same approach can be used for other SiC MOSFETs. The power module is shown in Fig 5.1a. As shown in Fig. 5.1b, the half-bridge module is packaged with two pairs of SiC MOSFETs and anti-parallel SiC Schottky diodes. Fig. 5.2 shows the subcircuit model of a pair of SiC MOSFET and anti-parallel diode in the module. The model consists of three major parts: drain-to-source current I_{DS} model, diode model and capacitance models. These three parts are modelled respectively.

The hybrid data-driven model proposed in Chapter 4 requires a complete training dataset of I-V characteristics covering the whole operation region of V_{DS} (e.g., from 0 V to 800 V for a 1200 V SiC MOSFET) to train the ANN models. However, the I-V characteristics provided in the datasheet only covers the low V_{DS} region from 0 V to 10 V as shown in Fig. 5.3a. Therefore, the hybrid data-driven model presented in Chapter 4 is only suitable for the measurement-based modelling method and not for the datasheet-based modelling method. As a result, an equation-based model is used in this chapter [49]. The detailed model equations are described as follows:

5.2.1 I_{DS} Model

In Fig. 5.2, a voltage-controlled current source I_{DS} and a series resistor R_{D1} are used to model the drain-to-source current of the SiC MOSFET. The model is based on the standard MOSFET level 1 SPICE model [123]:

if $V_{DS} < 0$ or $V_{GS} < V_{GS(th)}$,

$$I_{DS} = 0 \tag{5.1}$$

if $0 < V_{DS} < V_{GS} - V_{GS(th)}$,

$$I_{DS} = K_p \left(V_{GS} - V_{GS(th)} - \frac{V_{ch}}{2} \right) V_{ch} \left(1 + \lambda V_{ch} \right) \tag{5.2}$$

if $V_{DS} > V_{GS} - V_{GS(th)}$,

$$I_{DS} = K_p \frac{\left(V_{GS} - V_{GS(th)} \right)^2}{2} \left(1 + \lambda V_{ch} \right) \tag{5.3}$$

$$K_p = K_{p1} + K_{p2} \left(V_{GS} - 10 \right) \tag{5.4}$$

$$V_{ch} = V_{DS} - R_{D1} I_{DS} \tag{5.5}$$

where V_{GS} and V_{DS} are the gate-to-source and the drain-to-source voltages respectively; V_{ch} is the channel voltage applied to the voltage-controlled current source I_{DS}; $V_{GS(th)}$ is the gate threshold voltage; λ is the coefficient of short-channel effect; K_p is the transconductance coefficient, which is modelled as a linear function of V_{GS} with two parameters K_{p1} and K_{p2} in (5.4). In the I_{DS} model, K_{p1}, K_{p2}, $V_{GS(th)}$, R_{D1} and λ are the parameters that need to be extracted according to datasheet. Furthermore, to consider the temperature characteristics, K_{p1}, K_{p2}, $V_{GS(th)}$ and R_{D1} are modelled as linear or quadratic functions of temperature: $K_{p1}(T)$, $K_{p2}(T)$, $V_{GS(th)}(T)$ and R_{D1}(T), based on the curve fitting results. The detailed modelling approach will be described in Section 5.3.

5.2.2 Diode Model

In Fig. 5.2, a voltage-controlled current source I_D and a series resistor R_{D2} are used to model the current behaviour of the anti-parallel diode. The model can be described in the following equations:

$$I_D = I_S \left(\exp \left(\frac{qV_D}{kT} \right) - 1 \right) \tag{5.6}$$

$$V_D = V_{SD} - R_{D2} I_D \tag{5.7}$$

where V_{SD} is the source-to-drain voltage; V_D is the diode voltage applied to the voltage-controlled current source I_D; I_S is the reverse saturation current; $q = 1.602 \times 10^{-19}$ C is the electronic charge; $k = 1.3806488 \times 10^{-23}$ J/K is the Boltzmann's constant; T is the Kelvin temperature.

5.2.3 Capacitance Models

In Fig. 5.2, three capacitors, C_{GS}, C_{GD} and C_{DS}, are used to model the parasitic capacitors of the SiC MOSFET. C_{GS} is modelled as a constant capacitor. C_{DS} and C_{GD} are modelled as nonlinear capacitors as shown in (5.8) [49] and (5.9) [124].

$$C_{DS} = C_{DS0} \left(\frac{V_{bi}}{V_{DS} + V_{bi}} \right)^{M_{CDS}} \tag{5.8}$$

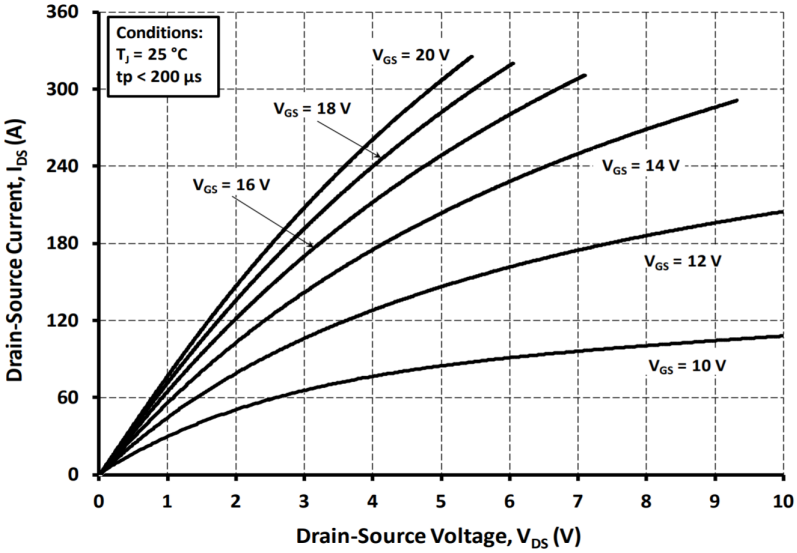
$$C_{GD} = \frac{C_{GD0}}{\left(1 + V_{DG} \left(1 + k_1 \frac{1+\tanh(k_2(V_{DG}-V_T))}{2}\right)\right)^{M_{CGD}}} \tag{5.9}$$

where V_{DG} is the drain-to-gate voltage; C_{DS0}, V_{bi}, M_{CDS} are the parameters for C_{DS}; C_{GD0},M_{CGD}, k_1, k_2 and V_T are the parameters for C_{GD}.

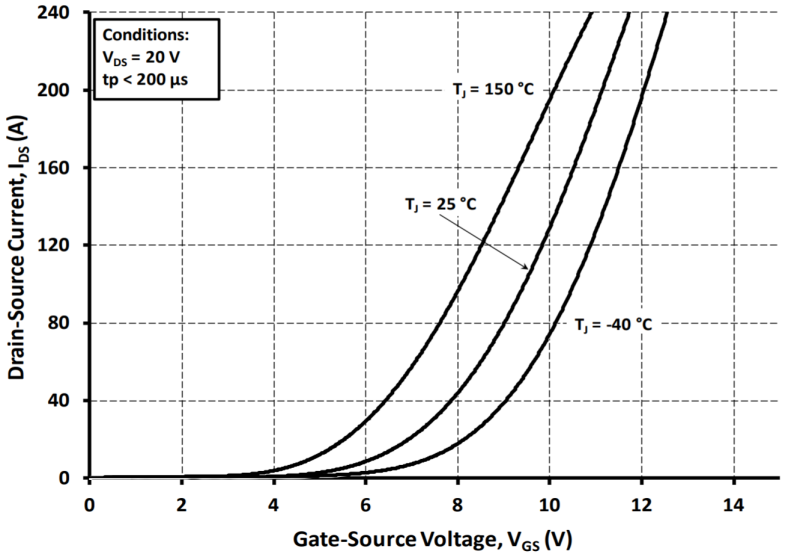
5.3 Step-by-step Modelling Approach

5.3.1 Modelling Approach of I_{DS} at 25 °C

Firstly, the modelling approach of I_{DS} at 25 °C is described. The same modelling approach can be used for I_{DS} model at different temperatures. The parameters K_{p1}, K_{p2}, $V_{GS(th)}$, R_{D1} and λ need to be extracted based on the I_{DS}–V_{GS} transfer characteristics and I_{DS}–V_{DS} output characteristics at 25 °C from the datasheet as shown in Fig. 5.3. In the datasheets, the I-V and C-V characteristics are usually provided in graphs such as Fig. 5.3. The software GetData Graph Digitizer is



(a) I_{DS}–V_{DS} output characteristics at 25 °C.



(b) I_{DS}–V_{GS} transfer characteristics.

Figure 5.3: I_{DS} characteristics of CAS120M12BM2 in the datasheet.

an effective tool to converter these graphs into digital data and works well with all types of datasheets. It is used to convert the graphs of I_{DS} characteristics in the datasheet into digital data. MATLAB curve fitting toolbox is used to do the curve fitting to extract parameters.

Coefficient of short-channel effect λ

Due to the short-channel effect, the channel length modulation occurs in SiC MOSFETs, which makes the positive current slope in the saturation region [125].

The short channel effect can be observed in Fig. 5.3a in the saturation region when $V_{GS} = 10\,\text{V}$. In the saturation region, V_{ch} is the dominant factor of V_{DS} due to the high channel resistance when the channel is pinched off. The voltage drop on R_{D1} can be ignored. It can be assumed that $V_{ch} \approx V_{DS}$. Therefore, V_{ch} in (5.3) can be replaced with V_{DS}. (5.3) can be simplified as:

$$I_{DS} = A(1 + \lambda V_{DS}) \tag{5.10}$$

where $A = K_p \frac{\left(V_{GS} - V_{GS(th)}\right)^2}{2}$ is a constant value when $V_{GS} = 10\,\text{V}$. λ can be extracted by curve fitting to fit (5.10) to the saturation region of I_{DS}–V_{DS} curve when $V_{GS} = 10\,\text{V}$ in Fig. 5.3a.

Gate threshold voltage $V_{GS(th)}$

The gate threshold voltage is defined as the gate-to-source voltage when the MOSFET starts to conduct a certain small amount of current. However, different MOSFETs and manufacturers might have different criteria of this current magnitude from 1 mA up to 50 mA. Therefore, it is better to extract the $V_{GS(th)}$ for the model although it is already provided in the datasheet [49]. In the datasheet, the transfer characteristics, i.e. the I_{DS}–V_{GS} curve, are usually measured with a high drain-to-source voltage bias so that I_{DS} is saturated. For example, in the datasheet of CAS120M12BM2, $V_{DS} = 20\,\text{V}$ is used to measure the transfer characteristics as shown in Fig. 5.3b. In the saturation region, $V_{ch} \approx V_{DS}$ can be assumed since V_{ch} is the dominant factor of V_{DS} . Therefore, V_{ch} in (5.3) can be replaced with $V_{DS} = 20\,\text{V}$. (5.3) can be simplified as:

$$I_{DS} = B \frac{\left(V_{GS} - V_{GS(th)}\right)^2}{2} \tag{5.11}$$

where $B = K_p(1 + \lambda V_{DS})$ is a constant value when $V_{DS} = 20\,\text{V}$. $V_{GS(th)}$ can be extracted by curve fitting to fit (5.3) to the I_{DS}–V_{GS} curve in Fig. 5.3b.

Table 5.1: Extracted K_p with different V_{GS}.

V_{GS}	10 V	12 V
K_p	4.886	5.450

Transconductance coefficient K_p

Two sets of I_{DS}–V_{DS} curves are required since the transconductance coefficient is modelled with two parameters K_{p1} and K_{p2} in (5.4). The I_{DS}–V_{DS} curves when $V_{GS} = 10\,\text{V}$ and $12\,\text{V}$ are chosen due to the high channel resistance at low gate-to-source voltage. Therefore, the voltage drop on R_{D1} can be ignored and $V_{ch} \approx V_{DS}$ can be assumed. In this case, V_{ch} in (5.2) can be replaced with V_{DS}. (5.2) can be rewritten as:

$$I_{DS} = K_p \left(V_{GS} - V_{GS(th)} - \frac{V_{DS}}{2} \right) V_{DS} \left(1 + \lambda V_{DS}\right) \tag{5.12}$$

K_p can be extracted by curve fitting to fit (5.2) to the linear region of I_{DS}–V_{DS} curves when $V_{GS} = 10\,\text{V}$ and $12\,\text{V}$ in Fig. 5.3a respectively. Two different values of K_p can be extracted with $V_{GS} = 10\,\text{V}$ and $12\,\text{V}$ respectively as shown in Table 5.1. Afterwards, (5.4) can be used to fit Table 5.1 to extract K_{p1} and K_{p2}.

Series resistance R_{D1}

In the model shown in Fig. 5.2, the on-state resistance $R_{DS(on)}$ consists of the channel resistance R_{ch} of the current source I_{DS} and the series resistance R_{D1}. $R_{DS(on)}$ is provided in the datasheet at specific conditions. For example, in the datasheet of CAS120M12BM2, $R_{DS(on)} = 13\,\text{m}\Omega$ when $V_{GS} = 20\,\text{V}$ and $I_{DS} = 120\,\text{A}$. The channel voltage V_{ch} can be calculated under the same V_{GS} and I_{DS} condition according to (5.2). R_{ch} and R_{D1} can be then calculated as:

$$R_{ch} = \frac{V_{ch}}{I_{DS}} \tag{5.13}$$

$$R_{D1} = R_{DS(on)} - R_{ch} \tag{5.14}$$

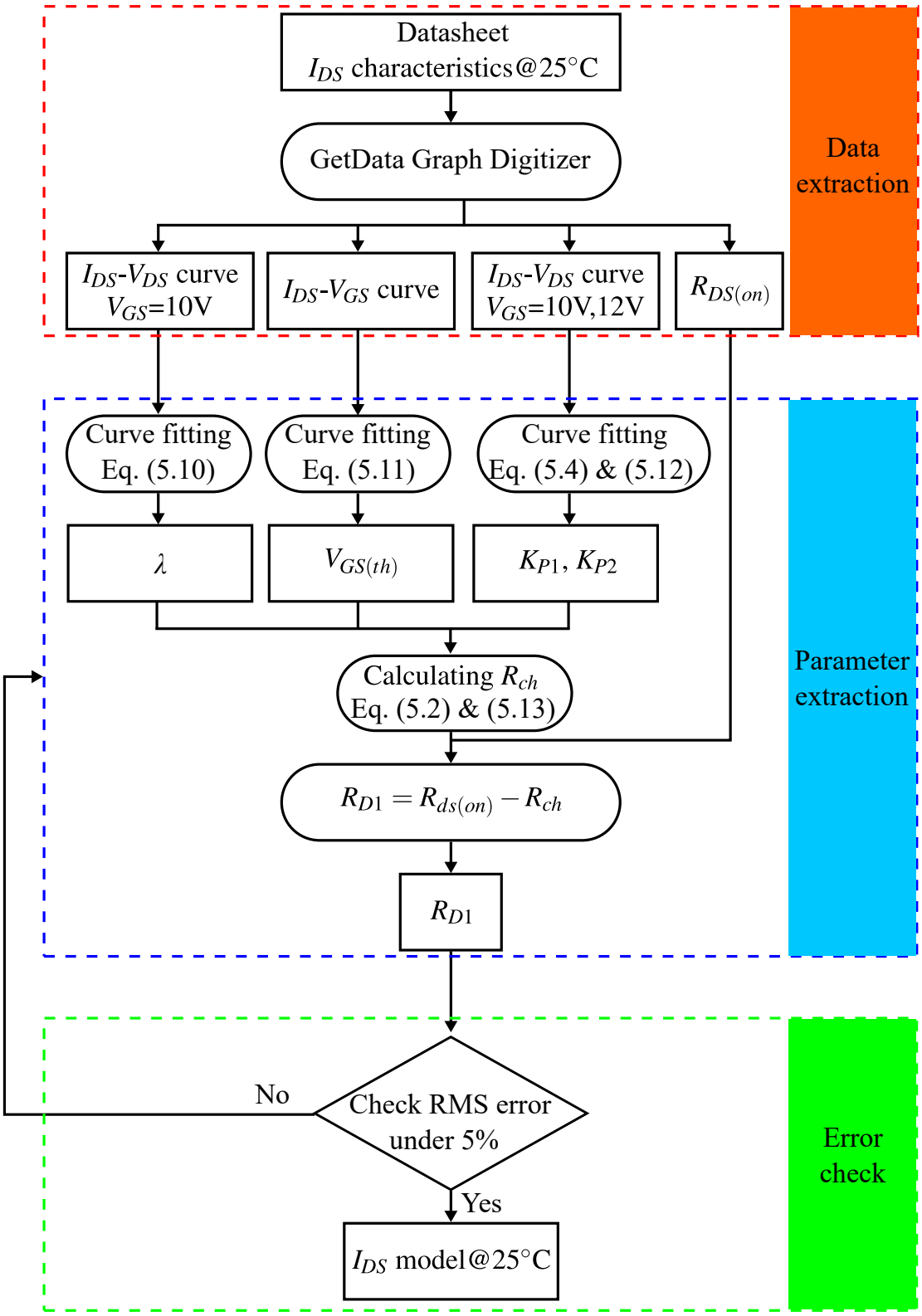


Figure 5.4: Modelling approach of I_{DS} at 25 °C.

Table 5.2: Parameters of I_{DS} at 25 °C.

K_{P1}	K_{P2}	$V_{GS(th)}$ (V)	R_{D1}(mΩ)	λ
4.886	0.2818	3.992	6.001	0.043

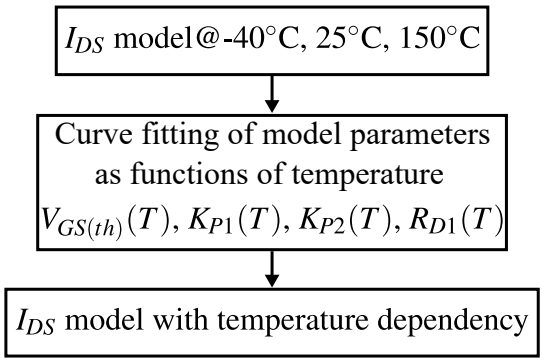


Figure 5.5: Modelling approach of I_{DS} with temperature dependency.

RMS error check

After all the parameters are extracted, the accuracy of the model is checked by comparing the simulated $I_{DS} - V_{DS}$ characteristics with the characteristics in the datasheet. The root mean square (RMS) error is calculated using the following equation [111]:

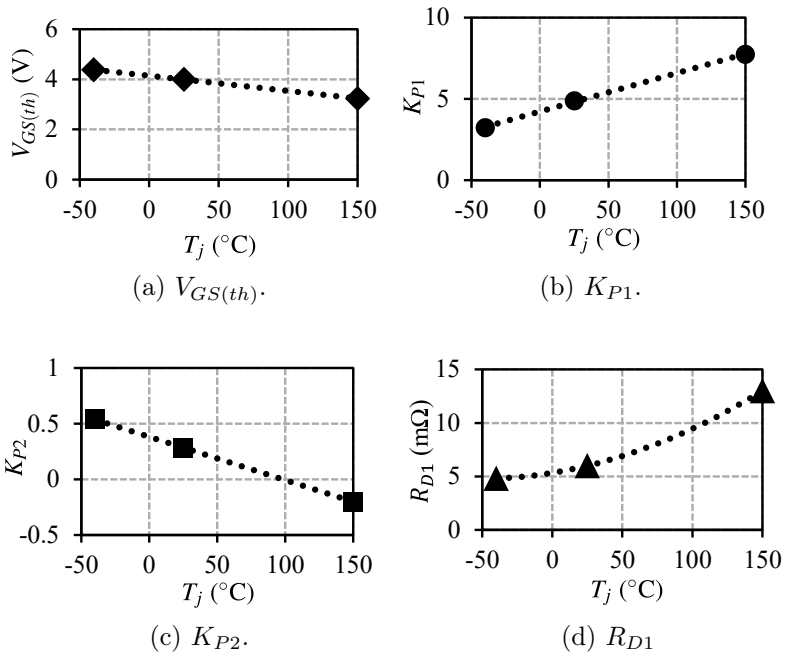
$$RMS = \sqrt{\frac{\sum_{i=1}^{N} \mid m_i - s_i \mid^2}{N}} \times 100\% \tag{5.15}$$

where N, m_i and s_i denote the number of data, measured and simulated values of I_{DS}. If the calculated RMS error exceeds 5%, the parameter extraction procedure will be done again until the RMS error is lower than 5%.

The step-by-step modelling approach of I_{DS} is summarized in Fig. 5.4. The extracted parameters are shown in Table 5.2.

5.3.2 Modelling Approach of I_{DS} with Temperature Dependency

In the datasheet of CAS120M12BM2, the I_{DS} characteristics at −40 °C, 25 °C and 150 °C are provided, which can be used to model the temperature dependency. The parameters K_{p1}, K_{p2}, $V_{GS(th)}$ and R_{D1} are modelled as linear or quadratic



(a) $V_{GS(th)}$. (b) K_{P1}.

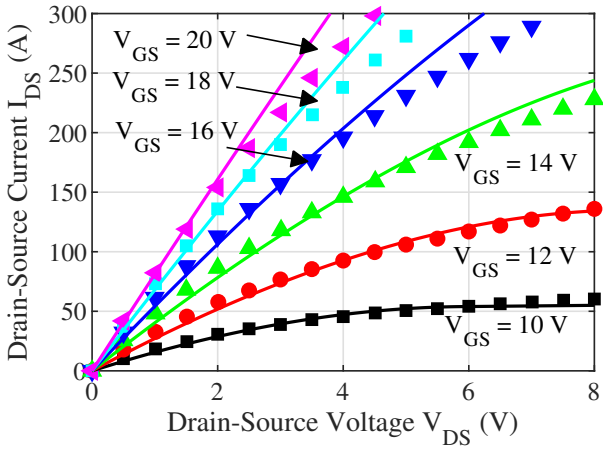
(c) K_{P2}. (d) R_{D1}

Figure 5.6: Temperature dependency of model parameters.

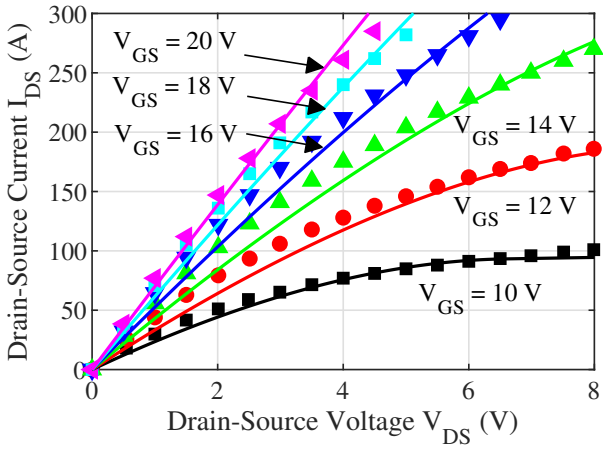
functions of temperature: $K_{p1}(T)$, $K_{p2}(T)$, $V_{GS(th)}(T)$ and $R_{D1}(T)$. Firstly, the parameters are extracted following the same approach in Fig. 5.4 at different temperatures. Secondly, the linear or quadratic functions are used to fit the values of each parameter at different temperatures. The modelling approach is summarized in Fig. 5.5. The temperature dependency of the parameters are shown in Fig. 5.6. The equations to describe the temperature dependency are:

$$\begin{cases} V_{GS(th)} = -0.006T + 4.1416 \\ K_{P1} = 0.0237T + 4.2227 \\ K_{P2} = -0.0039T + 0.3816 \\ R_{D1} = 0.0002T^2 + 0.0214T + 5.3409 \end{cases} \tag{5.16}$$

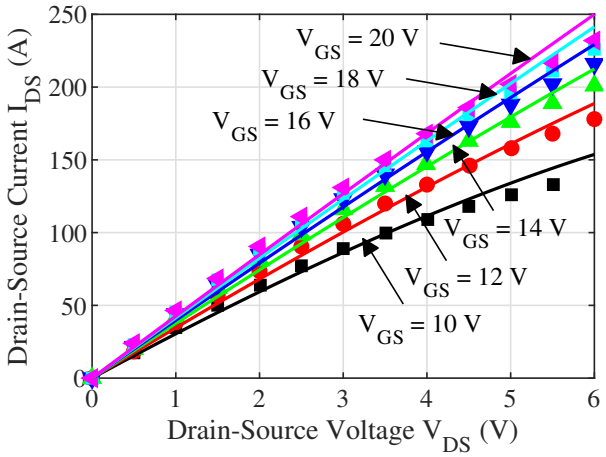
The comparison between the I_{DS} model with the datasheet is shown in Fig. 5.7. It can be seen that the simulated I_{DS} characteristics match the datasheet very well, which can verify the effectiveness of the proposed modelling approach.



(a) -40 °C.



(b) 25 °C.



(c) 150 °C.

Figure 5.7: I_{DS}–V_{DS} characteristics at different temperatures compared to datasheet. The coloured dots denote the results from the datasheet. The coloured lines denote the results from the model.

Table 5.3: Parameters of diode model.

I_S (A)	$R_{D2}(m\Omega)$
1.925e-14	4.66

5.3.3 Modelling Approach of Diode

The diode model described in (5.6) and (5.7) contains two parameters that need to be extract: R_{D2} and I_S. The parameters are extracted according to diode characteristics in the datasheet.

Series resistance R_{D2}

According to (5.6), the differential resistance of the voltage-dependent current source I_D can be calculated as:

$$R_D = \frac{\mathrm{d}V_D}{\mathrm{d}I_D} = \frac{kT}{q} \cdot \frac{1}{I_D + I_S} \tag{5.17}$$

According to (5.17), $R_D << R_{D2}$ can be assumed when I_{DS} is larger than 100 A. Therefore, the slope of the diode characteristics in the high current linear region can be used to extract the series resistance R_{D2}.

Reverse saturation current I_S

After R_{D2} is extracted, the I_D–V_D characteristics can be obtained from the I_D–V_{SD} diode characteristics according to (5.7). I_S can be then extracted by fitting (5.6) to the I_D–V_D characteristics.

The extracted parameters of the diode are listed in Table 5.3. The step-by-step modelling approach is summarized in Fig. 5.8. In Fig. 5.9, the diode model matches the diode characteristics in the datasheet very well, which can verify the effectiveness of the proposed modelling approach.

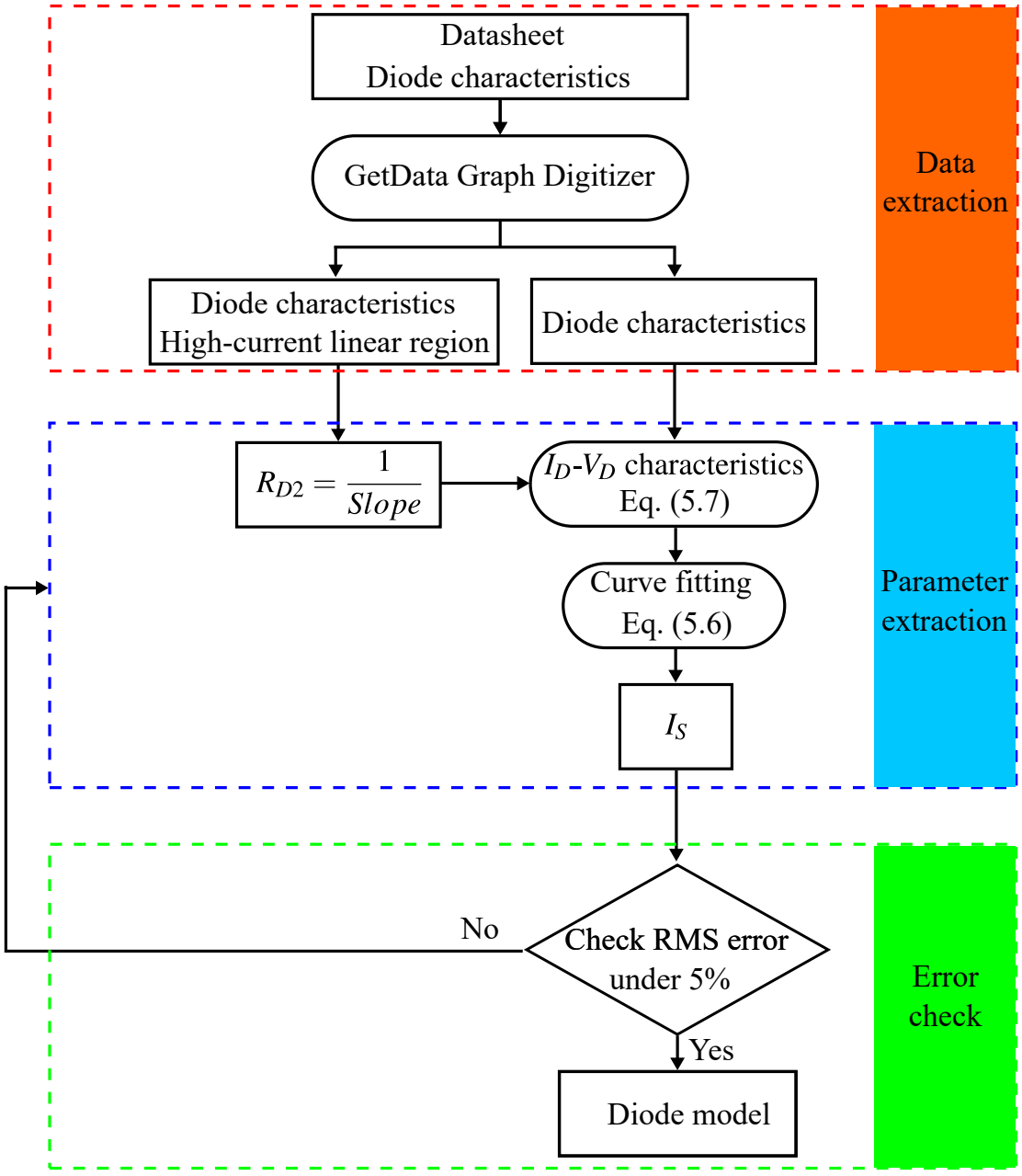


Figure 5.8: Modelling approach of diode.

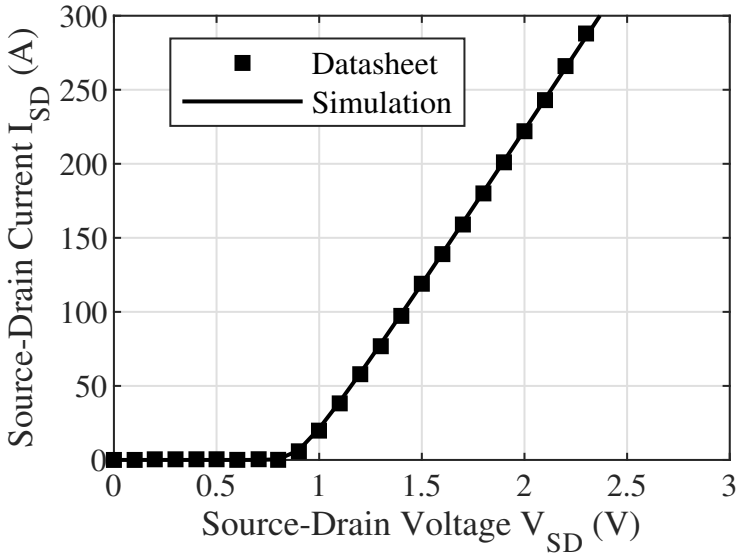


Figure 5.9: Diode characteristics compared to datasheet.

Table 5.4: Parameters of capacitance model.

C_{GS}(pF)	C_{DS0}(pF)	V_{bi} (V)	M_{CDS}	C_{GD0}(pF)	V_T(V)	k_1	k_2	M_{CGD}
6319	15500	1.622	0.478	2646	13.52	40.51	0.3815	0.4295

5.3.4 Modelling Approach of Parasitic Capacitors

In the datasheet, the input capacitance C_{iss}, output capacitance C_{oss} and reverse transfer capacitance C_{rss} are given as the capacitance characteristics as shown in Fig. 5.10. C_{GS}, C_{GD} and C_{DS} can be calculated by C_{iss}, C_{oss} and C_{rss} according to (5.18):

$$\begin{cases} C_{GS} = C_{iss} - C_{rss} \\ C_{DS} = C_{oss} - C_{rss} \\ C_{GD} = C_{rss} \end{cases} \tag{5.18}$$

C_{GS}:

A constant value is used to model C_{GS}. It can be easily extracted by subtracting C_{rss} from C_{iss} according to (5.18). C_{GS} = 6319 pF can be obtained for CAS120M12BM2.

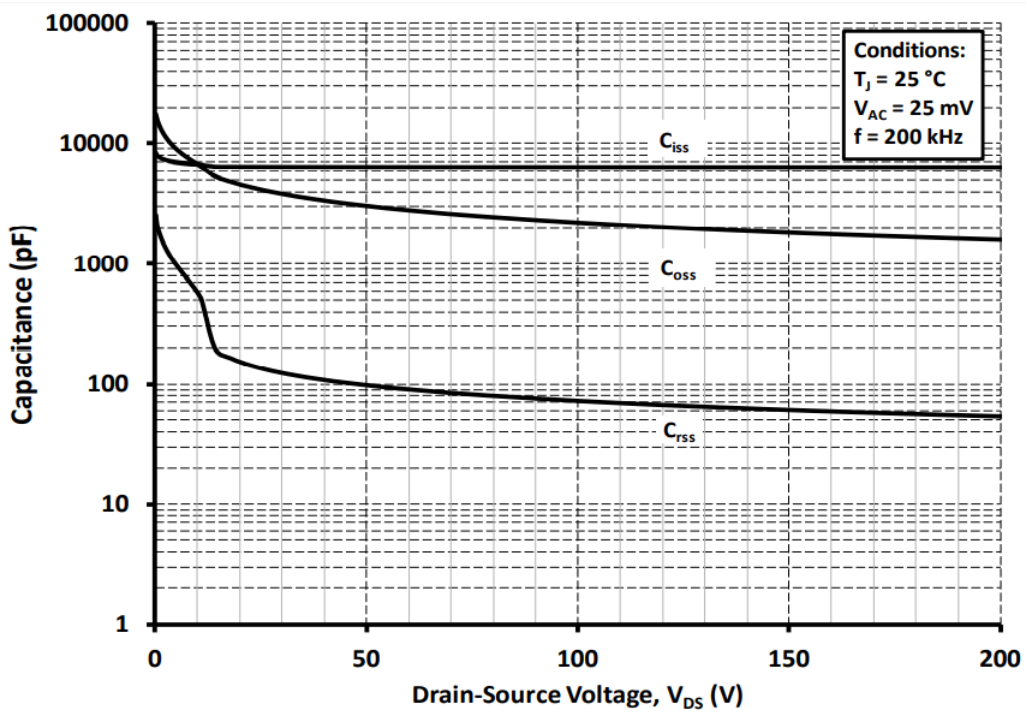


Figure 5.10: Capacitance characteristics of CAS120M12BM2 in the datasheet.

C_{DS}:

C_{DS} is a nonlinear capacitor varying with drain-to-source voltage V_{DS}. The C_{DS}–V_{DS} curve can be derived from the datasheet using (5.18). C_{DS0}, V_{bi}, M_{CDS} can be easily extracted by curve fitting using (5.8) and the C_{DS}–V_{DS} curve.

C_{GD}:

C_{DS} is a more complicated nonlinear capacitor varying with drain-to-gate voltage V_{DG}. The C_{rss}–V_{DS} curve in the datasheet can be used to extract the parameters of C_{GD}. In Fig. 5.10, two significantly different slopes can be observed in the C_{rss}–V_{DS} curve. V_T can be firstly extracted as the transition voltage of these two slopes. In (5.9), a hyperbolic tangent function is used to model the transition of slopes in C_{rss}–V_{DS} curve . When $V_{DG} < V_T$, (5.9) can be approximated as:

$$C_{GD} = \frac{C_{GD0}}{(1 + V_{DG})^{M_{CGD}}} \tag{5.19}$$

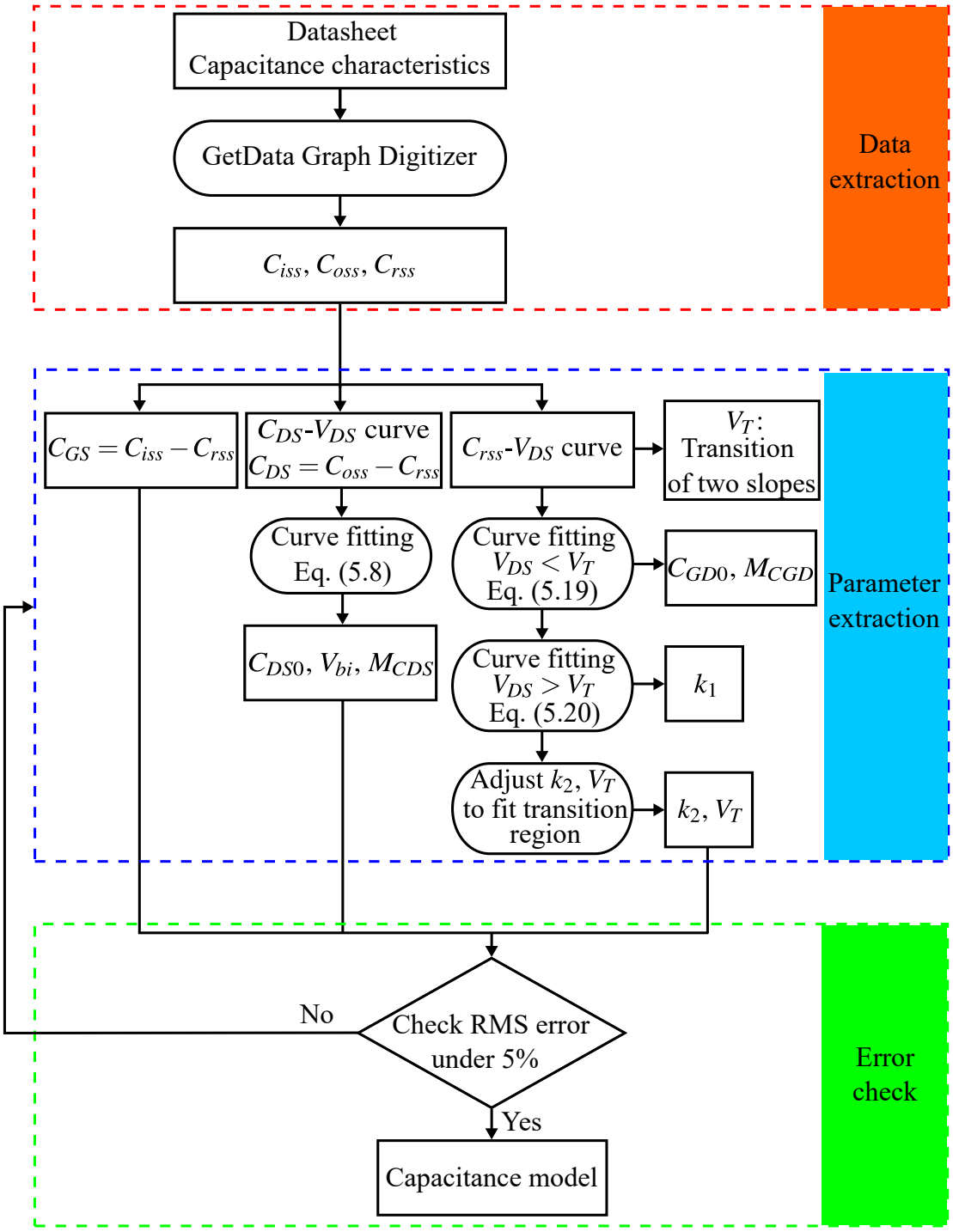


Figure 5.11: Modelling approach of parasitic capacitors.

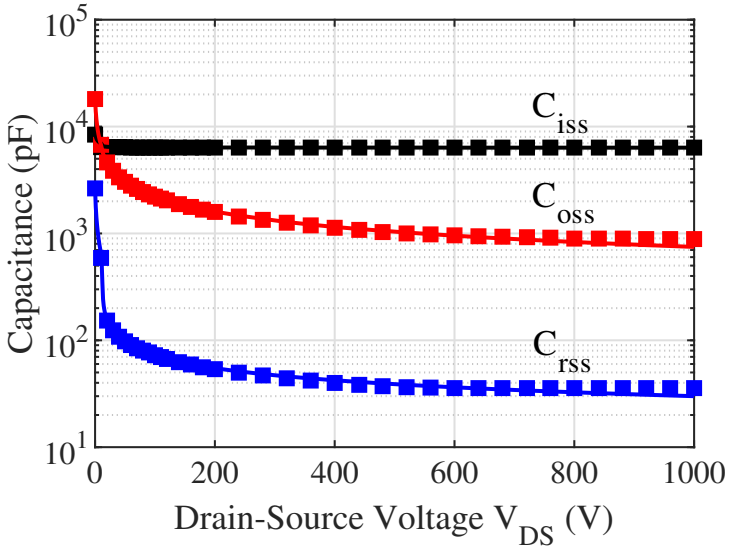


Figure 5.12: Capacitance characteristics compared to datasheet. The coloured dots denote the results from the datasheet. The coloured lines denote the results from the model.

C_{GD0} and M_{CGD} can be extracted by curve fitting to fit (5.19) to C_{rss}–V_{DS} curve when $V_{DS} < V_T$.

When $V_{DG} > V_T$, (5.9) can be approximated as

$$C_{GD} = \frac{C_{GD0}}{(1 + V_{DG}\,(1 + k_1))^{M_{CGD}}} \tag{5.20}$$

k_1 can be extracted by curve fitting to fit (5.20) to C_{rss}–V_{DS} curve when $V_{DS} > V_T$.

Finally, k_2 and V_T are adjusted to accurately fit the transition region of two different slopes of the C_{rss}–V_{DS} curve.

The step-by-step modelling approach of parasitic capacitors is summarized in Fig. 5.11. The extracted parameters are listed in Table 5.4. The comparison between the capacitance model with the datasheet is shown in Fig. 5.12, which shows a good match.

5.4 Model Verification

A SPICE model is built for CAS120M12BM2B using the subcircuit model and extracted parameters. Both experimental platform and simulation platform of

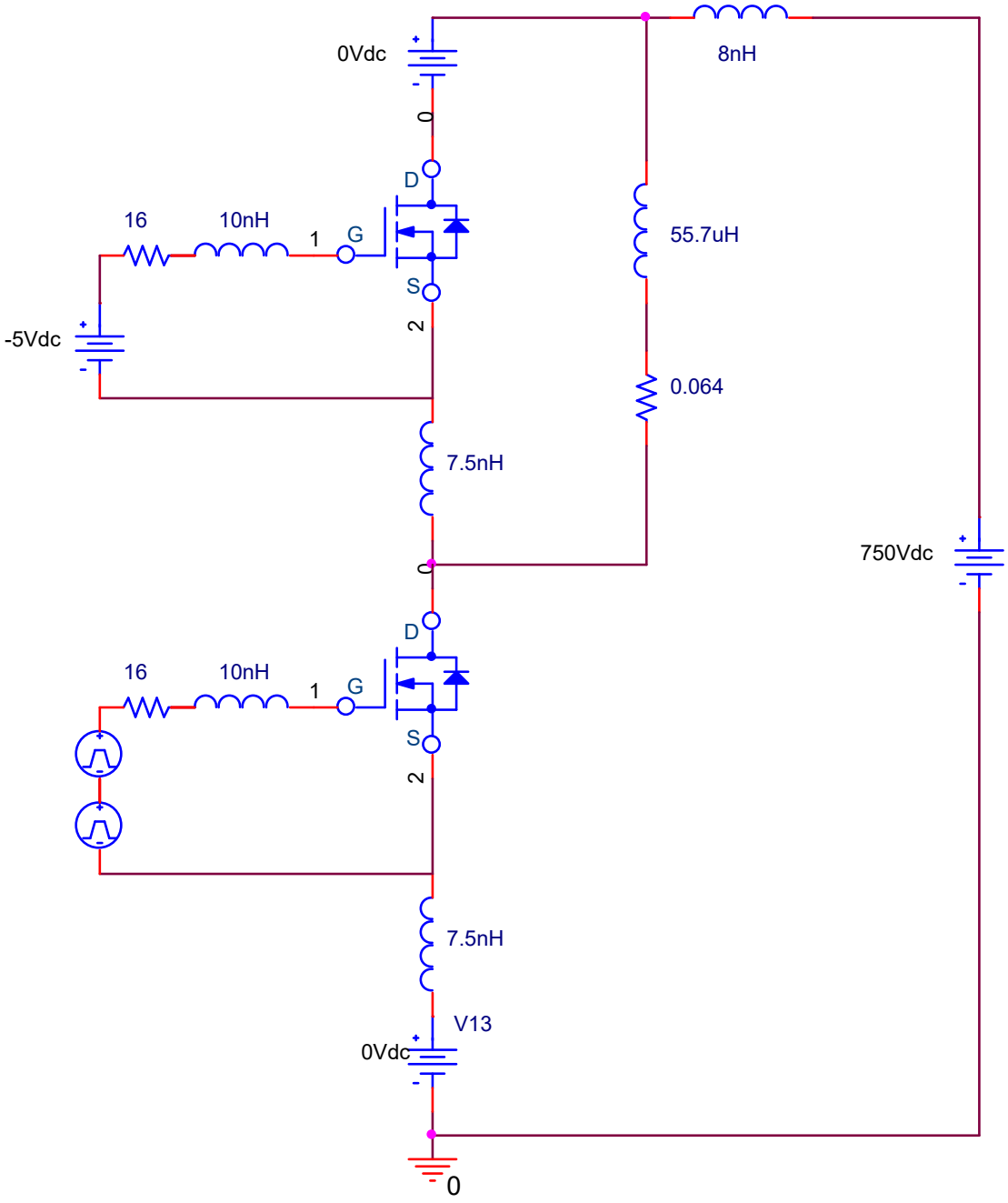
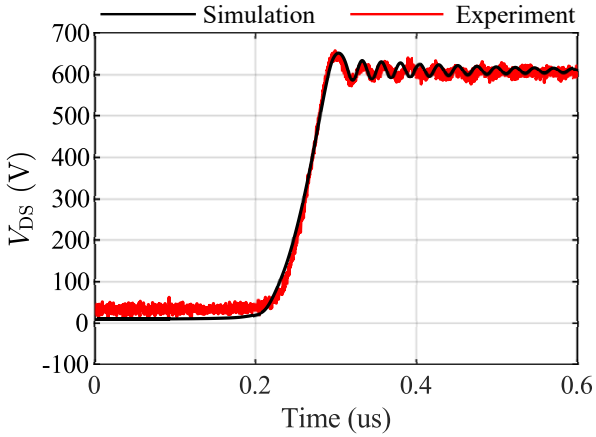
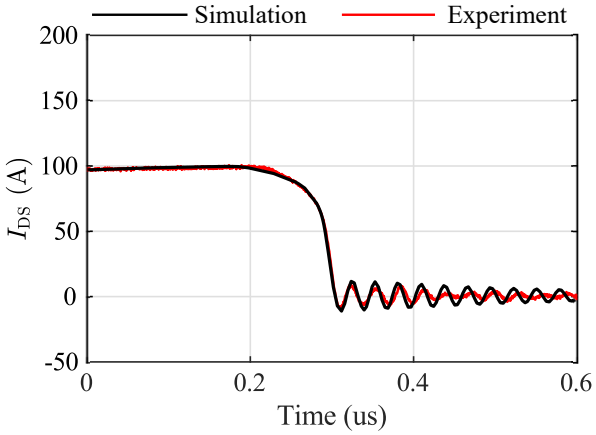


Figure 5.13: Simulation circuit of DPT in PSpice.



(a) Turn-off voltage V_{DS}.

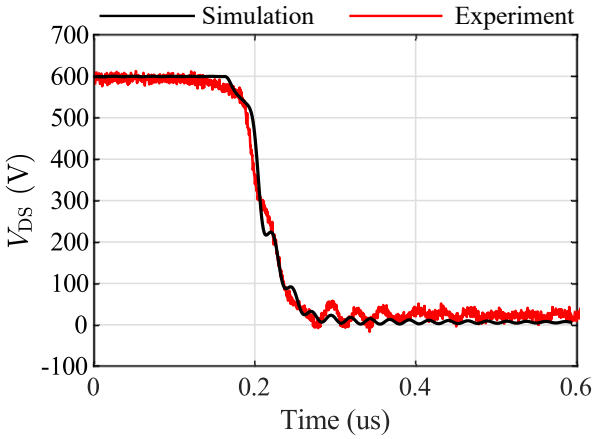


(b) Turn-off voltage I_{DS}.

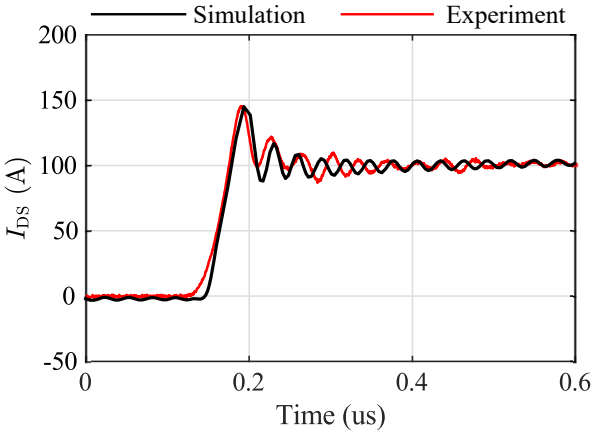
Figure 5.14: Comparison of turn-off waveforms by simulation and experiment.

double pulse tester (DPT) are built to verify the proposed SPICE model. The experimental platform of DPT is built. A PCB board with low parasitic inductance is designed as the main circuit. A commercial gate driver CGD15HB62P1 for half-bridge module from Wolfspeed is used [126]. The upper switch is always off and the lower switch is controlled by the DPT signal generated by the DSP control board. A 55.7 μH inductor with low equivalent parallel capacitance is designed as the load. The equivalent series resistance of the load inductor is measured as 0.064 Ω. The voltage and current of the lower switch is measured by high-bandwidth differential voltage probes and high-bandwidth current probes.

The same simulation circuit of DPT is built in PSpice as shown in Fig. 5.13. The 5 nH DC-bus stray inductance is obtained by simulating the S-parameter of the PCB board including all the stray inductance of the DC capacitors in Pathwave Advanced Design System (ADS) [127]. The stray inductance in the power module



(a) Turn-on voltage V_{DS}

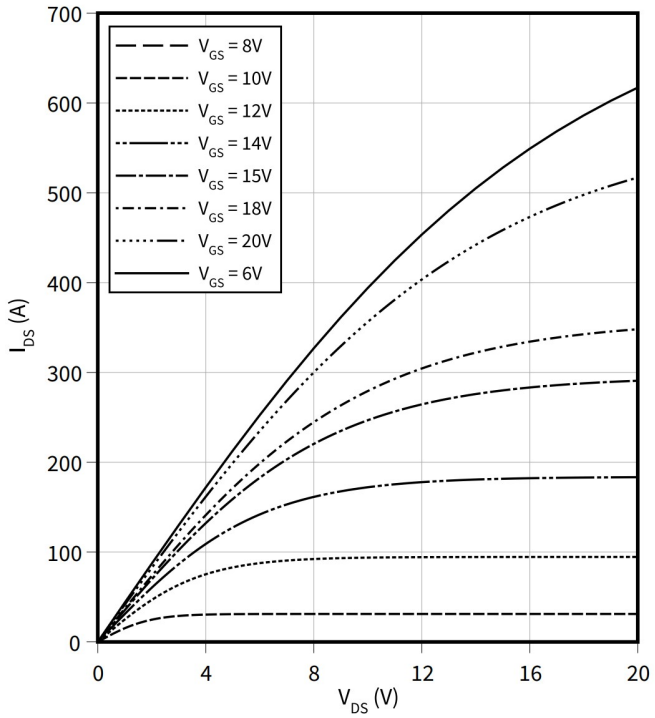


(b) Turn-on voltage I_{DS}

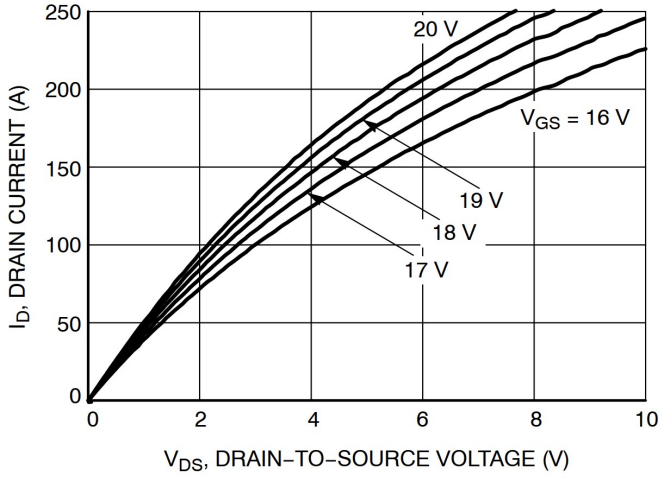
Figure 5.15: Comparison of turn-on waveforms by simulation and experiment.

is 15 nH according to the datasheet. Two 7.5 nH inductors are added to the drain terminals of upper and lower SiC MOSFETs in the half-bridge module respectively to represent this stray inductance. The gate loop resistance of 16 Ω is obtained by calculating the time constant of the measured gate-to-source voltage [49]. Both simulation and experiment are conducted at 25 °C. The DPT results in both simulation and experiment are shown in Fig. 5.14 and Fig. 5.15. The simulation of the turn-on and turn-off transients shows good agreement with the experiment.

It is worth mentioning that the robustness of datasheet-based model depends on the quality of the datasheet provided by the manufacturers. For example, Fig. 5.16a and Fig. 5.16b present the I-V characteristics provided by the datasheets of two SiC MOSFETs from different manufacturers. Fig. 5.16a is provided by Infineon for their product IMW120R020M1H [128]. Fig. 5.16b is provided by



(a) I-V characteristics of IMW120R020M1H.



(b) I-V characteristics of NTBG020N120SC1.

Figure 5.16: Comparison of I-V characteristics in two datasheets.

Onsemi for their product NTBG020N120SC1 [129]. Fig. 5.16a presents the I-V characteristics with V_{GS} varies from 6 V to 20 V. Fig. 5.16b presents the I-V characteristics with V_{GS} only varies from 17 V to 20 V. Since the I-V characteristics provided by Fig. 5.16b lack the information when with $V_{GS} < 17$ V. The model based on Fig. 5.16b will be less accurate than the model based on Fig. 5.16a.

5.5 Comparison with Measurement-based Modelling Method

5.5.1 Complexity

The complexity of the proposed measurement-based and datasheet-based modelling methods are compared from three perspectives: required data, parameter extraction, computation time:

1. The measurement-based modelling method requires additional measurement data of the I-V and C-V characteristics, while the required data for the datasheet-based modelling method can be more easily obtained from the datasheet.

2. The parameter extraction process for both modelling methods are simple and easy. The parameter extraction of the proposed measurement-based modelling method can be automatically done by the Neural Net Fitting Toolbox in MATLAB as presented in Chapter 4. The parameters of the proposed datasheet-based modelling method can also be easily obtained by the step-by-step parameter extraction process presented in this chapter.

3. The computation time of SiC MOSFET models reflect the model complexity in transient simulation. The computation time of the measurement-based model and the datasheet-based model are compared through simulating the same DPT circuit in SIMetrix for 40 μs. It is shown in Table 5.5 that the runtime of the datasheet-based model when simulating the DPT circuit is about 15% less compared to the measurement-based model.

In summary, the proposed datasheet-based modelling method is less complex compared to the proposed measurement-based modelling method in terms of required data and computation time.

Table 5.5: Computation time of the proposed measurement-based and datasheet-based models.

	Measurement-based model	Datasheet-based model
Simulation runtime (s)	3.13	2.66

Simulation platform: SIMetrix 8.00g.
Computer: Intel Core i7-8650U CPU@1.9GHz, 16-GB RAM.

5.5.2 Accuracy

The datasheet only provides the I-V and C-V characteristics as shown in Fig. 5.3 and Fig. 5.10. These characteristics are measured in static state by the curve tracer. The datasheet does lack the dynamic-state I-V and C-V characteristics which are measured by the proposed method in Chapter 3. These dynamic-state characteristics include the I-V characteristics in the high V_{DS} region in Fig. 3.14, the nonlinear gate-source capacitance characteristics in Fig. 3.19, the on-state and dynamic gate-drain capacitance characteristics in Fig. 3.19. It has been verified in Section 4.6 that these characteristics have significant impact on the model accuracy.

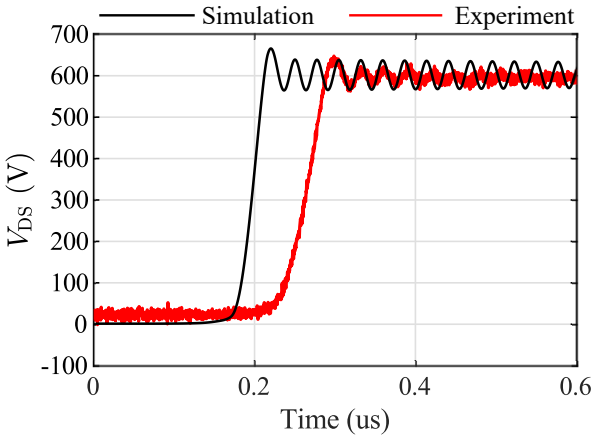
The switching waveforms of the SiC MOSFET simulated by the proposed measurement-based model have been presented in Fig. 4.13 and compared to the experimental waveforms. The switching waveforms of the SiC MOSFET simulated by the proposed datasheet-based model have been presented and compared to the experimental waveforms in Fig. 5.14 and Fig. 5.15. To quantitatively analyse the accuracy of both models, the relative RMS errors of the simulation waveforms of V_{DS} and I_{DS} are calculated and compared according to (4.8). As shown in Table 5.6, the relative RMS errors of the measurement-based model are at least 24% smaller than those of the datasheet-based model. The measurement-based modelling method is more accurate because more complete data of the I-V and C-V characteristics are measured and modelled.

Table 5.6: Relative RMS errors of switching transients.

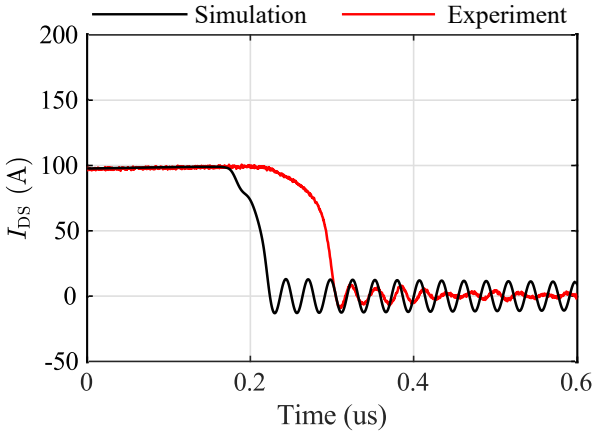
Test conditions	Transient waveforms	Errors of Measurement-based model	Errors of Datasheet-based model
Turn off	V_{DS}	3.84%	5.37%
	I_{DS}	3.43%	4.57%
Turn on	V_{DS}	6.33%	10.92%
	I_{DS}	6.21%	8.15%

5.5.3 Gate Driver Resistor

In the experiment of DPT for the validation of both the proposed measurement-based and datasheet based model, a gate driver resistor of 10 Ω is used. The same gate driver resistor is used in the simulation results of the proposed measurement-based model presented in Fig. 4.13. However, in the simulation results of the datasheet-based model presented in Fig. 5.14 and Fig. 5.15, a gate driver resistor of 16 Ω is used. This is because the datasheet-based model cannot accurately model the gate capacitors (C_{GS} and C_{GD}) due to the lack of nonlinear C_{GS}-V_{GS} characteristics, on-stage and dynamic C_{GD} characteristics. As shown in Fig. 5.17 and Fig. 5.18, the datasheet-based model will present significant errors if the same gate resistor of 10 Ω is used in simulation. To compensate the errors, a larger gate resistor of 16 Ω must be applied in simulation, resulting in a mismatch between the gate driver resistors in simulation and experiment. This limits the application of the proposed datasheet-based model in design and optimisation of gate drivers because the gate driver used in simulation does not represent the gate driver used in practice. It is highly recommended that the manufacturers can add the nonlinear C_{GS}-V_{GS} characteristics in their datasheets because the nonlinear C_{GS}-V_{GS} characteristics can be easily measured and can effectively improve the accuracy of the model and the gate driver resistor as presented in Fig. (4.20).



(a) Turn-off voltage V_{DS}.



(b) Turn-off voltage I_{DS}.

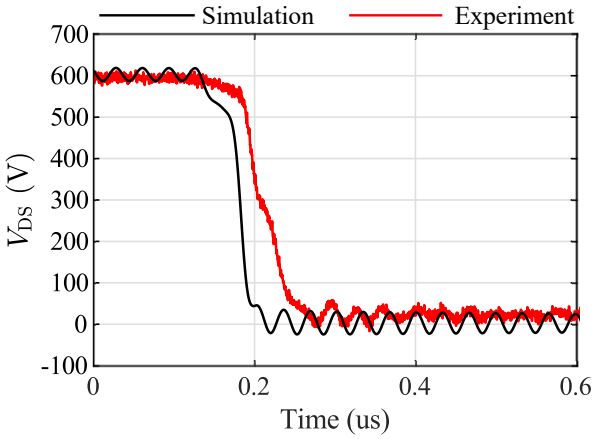
Figure 5.17: Simulated turn-off waveforms of the datasheet-based model with a gate driver resistor of 10 Ω.

5.5.4 Comparison Results

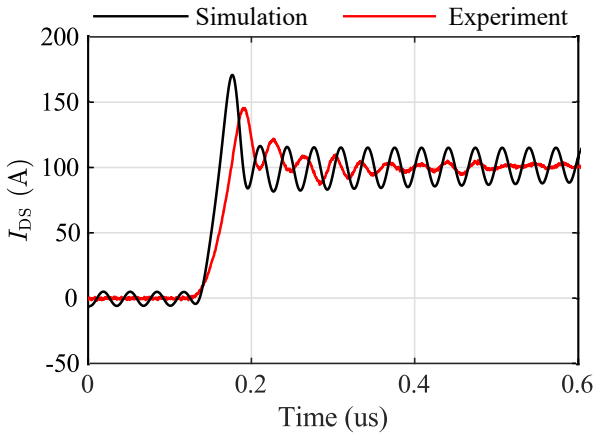
According to the above comparison, the advantages and disadvantages of the proposed measurement-based and datasheet-based modelling methods are summarised in Table 5.7:

5.6 Summary

A step-by-step datasheet-based modelling approach for SiC MOSFETs has been proposed. The proposed modelling approach significantly reduces time and efforts of converter designers to develop their own models for transient simulation and converter design. Subcircuits and equations of SiC MOSFETs were firstly introduced to model the drain-to-source current, antiparallel diode, parasitic ca-



(a) Turn-on voltage V_{DS}



(b) Turn-on voltage I_{DS}

Figure 5.18: Simulated turn-on waveforms of the datasheet-based model with a gate driver resistor of 10 Ω.

pacitance and temperature dependency accurately. Then, a step-by-step parameter extraction approach based on datasheet was proposed, which can be easily used to model other SiC MOSFETs. As an example, a SPICE model was built based on the proposed modelling approach for a commercial SiC MOSFET power module. A good agreement on switching on/off waveforms is achieved between simulation and experiment results, which verifies the accuracy of the proposed datasheet-based modelling approach.

The datasheet-based modelling method was compared to the measurement-based modelling method, including complexity, accuracy and gate drivers. Due to the incomplete data of I-V and C-V characteristics in the datasheet, the datasheet-based modelling method presents 24% more RMS errors in transient simulation and cannot accurately match the gate driver resistors used in practical

Table 5.7: Advantages and disadvantages of the proposed measurement-based and datasheet-based modelling methods.

Modelling methods	Advantages	Disadvantages
Measurement-based modelling method	• More accurate due to complete I-V and C-V characteristics. • Suitable for gate driver design.	• More complicated measurement of of I-V and C-V. • Longer computation time.
Datasheet-based modelling method	• No measurement is required. • Shorter computation time.	• Less accurate than measurment-based modelling method. • Not suitable for gate driver design.

application. However, the datasheet-based modelling method is much simpler because no measurement is needed for the model. The datasheet-based model also features 15% less computation time than the measurement-based modelling method. Therefore, the datasheet-based modelling method is a more cost and time-efficient solution for fast modelling and simulation of SiC MOSFETs to quickly validate the converter design.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

SiC MOSFETs can significantly improve the efficiency and power density of power electronics converters. However, to fully exploit the potential of SiC MOSFET and to optimise the converter design, accurate transient simulation of SiC MOSFETs is required to analyse the switching behaviour of SiC MOSFETs. The research work in this thesis investigated the characterisation and modelling of SiC MOSFETs for transient simulation, including accurate characterisation of SiC MOSFETs, measurement-based modelling of SiC MOSFETs and datasheet-based modelling of SiC MOSFETs. The proposed methods can provide the power electronics designers with simpler, more accurate and faster measurement and modelling of SiC MOSFETs. The proposed methods can help non-expert power electronics designers to build their own SiC MOSFET models. The impact of this thesis is to provide simpler and more accurate characterisation and modelling methods to facilitate the simulation-based design optimisation of power electronics converters.

6.1.1 Simplified Characterisation of SiC MOSFETs

A characterisation method based on a double pulse tester (DPT) is proposed to simplify the characterisation process and improve the accuracy of the simulated

switching behaviour of the SiC MOSFETs. The dynamic-state I-V and C-V characteristics that have significant impact on the switching waveforms of the SiC MOSFET were measured by the proposed DPT-based measurement method. These characteristics include the I-V characteristics in the high V_{DS} region, nonlinear C_{GS} characteristics, on-state and dynamic C_{GD} characteristics.

- The proposed method significantly reduces the self-heating of the SiC MOSFET when measuring the I-V characteristics in the high V_{DS} region to reduce the errors caused by the increased junction temperature.

- Analytical equations of the switching process were derived to analyse the relationship between the switching waveforms and the gate capacitances (i.e., C_{GS} and C_{GD}). The nonlinear C_{GS} characteristics, on-state and dynamic C_{GD} characteristics were directly extracted from the switching waveforms measured by the DPT based on the analytical equations.

- The measured characteristics were used to improve the model accuracy of SiC MOSFETs. The simulation results show that the simulation accuracy is increased by at least 3 times after considering all the characteristics measured by the proposed DPT-based method.

- Compared to previous methods presented in the literature, the proposed method only utilises a DPT to measure all the dynamic-state I-V and C-V characteristics, which significantly simplifies the characterisation process of the SiC MOSFET.

6.1.2 Measurement-Based Accurate Modelling of SiC MOSFETs

A measurement-based hybrid data-driven modelling methodology has been proposed to model SiC MOSFETs for accurate and fast transient simulation. To accurately model the high-speed switching transients, the required training dataset were identified and then measured to train the proposed ANN model. The

trained ANN was combined with the behaviour-based equations to accurately model the cut-off region and to avoid overfitting the ANN model. In addition, the C-V characteristics were modelled in logarithmic scale using ANNs for accuracy.

- Compared to the conventional equation-based modelling methods, the proposed hybrid data-driven method can model the measured I-V and C-V characteristics with improved accuracy, resulting in more accurate transient simulation of SiC MOSFETs. The hybrid data-driven model was compared with a commercial Angelov model. The switching transients of the hybrid data-driven model are $1.5 \sim 3$ times closer to the experimental results compared to the Angelov model.

- The proposed hybrid data-driven modelling method also enables faster modelling process and faster transient simulation. Since ANNs are used to model the I-V and C-V characteristics of SiC MOSFETs, there is no need to design complicated equations in the modelling process. The model parameters can also be automatically extracted by the well-established neural network training toolboxes, such as Neural Net Fitting Toolbox in MATLAB, which significantly simplifies the modelling process. Besides, the simulation time of the proposed hybrid data-driven model is found to be 30% reduced compared to the equation-based Angelov model.

- The proposed hybrid data-driven modelling method has good adaptability to model devices from different manufacturers. The parameters of the hybrid data-driven model can be adjusted for different SiC MOSFETs. The ANNs in the hybrid data-driven modelled can be easily retrained by the measured characteristics of different SiC MOSFETs.

6.1.3 Datasheet-based Fast Modelling of SiC MOSFETs.

A step-by-step datasheet-based modelling approach for SiC MOSFETs were proposed. The datasheet-based model was built based on the characteristics obtained

from the datasheet without the need of any further measurement. Therefore, the proposed datasheet-based modelling approach significantly reduces time and efforts of converter designers to develop their own models for transient simulation and converter design.

- A step-by-step parameter extraction approach was proposed to extract the model parameters based on the I-V characteristics with temperature dependency, C-V characteristics and diode characteristics obtained from the datasheet. This parameter extraction approach can be easily followed by non-expert users to develop their own models for other SiC MOSFETs.

- The proposed datasheet-based modelling method was compared to the proposed measurement-based modelling method, including complexity, accuracy and gate drivers. The comparison shows that the datasheet-based modelling method presents 24% more RMS errors and cannot accurately match the gate driver resistor used in practical experiment. However, the datasheet-based modelling method features simpler modelling process and 15% faster simulation speed so provides a more cost and time-efficient process for converter designers to quickly validate their converter design.

6.2 Future Work

The following future work were identified to extend the work reported in this thesis:

6.2.1 Characterisation and Modelling of Temperature Dependency

In this thesis, due to the limitation of the DPT setup, the I-V characteristics were only characterised and modelled at 25 °C. As a result, the proposed measurement-based modelling method did not model the temperature dependency of SiC MOSFETs due to the lack of measured data. In practice, SiC MOSFETs might operate

at various junction temperatures and the I-V characteristics have a strong temperature dependency. Therefore, a DPT with a temperature controller and an infrared camera need to be developed to measure the I-V characteristics at different junction temperatures (from -40 °C to 150 °C). As mentioned in Chapter 4, the proposed measurement-based modelling method can be easily adapted to model the temperature dependency by adding another input neuron as temperature input in the artificial neural network. The measured I-V characteristics with temperature dependency can be used to train the adapted artificial neural network. Besides, the thermal impedance model of SiC MOSFETs need to be established and combined with the electrical model built in this thesis to provide an accurate electro-thermal simulation.

6.2.2 Verification and Application of Models in Converter Design and Optimisation

One of the main applications of SiC MOSFET models is for converter design and optimisation. The thesis mainly focused on the characterisation and modelling methodologies of SiC MOSFETs to provide accurate transient simulation. The effectiveness of the proposed methods and models have been verified in this thesis by comparing the simulated switching waveforms with the measured switching waveforms acquired from a DPT. The effectiveness of the proposed methods and models in simulating power electronics converters need to be further verified. The impact of the improved model accuracy on the design optimisation of the power electronics converters needs to be quantified. The next step is to use the model to analyse the converter performance such as efficiency and EMI. To do this, the whole converter need to be modelled, including the passive components, the heatsink and the parasitics of the printed circuit board (PCB). The simulated converter performance can firstly be compared to the measured performance of an experimental prototype to verify the effectiveness of the simulation models. Afterwards, the models can be used for virtual prototyping to optimise the converter

performance.

6.2.3 Development of Modelling Tools with User Interface

In this thesis, both measurement-based and datasheet-based modelling methods were proposed and verified. The next step is to develop a well-established modelling tool with friendly user interface to facilitate the wide adoption of the proposed modelling methods. For example, the proposed measurement-based modelling method is based on artificial neural network. A modelling tool based on Python can be developed by utilising the well-established open-source machine learning library in Python such as Keras library. The graphical user interface can be developed for users to import the characteristics of SiC MOSFETs. The model can be automatically trained by the imported characteristics. After the model is trained, a SPICE model can be generated by the modelling tool and can be directly used for transient simulation in SPICE simulators.

References

[1] R. Rajamony, S. Wang, R. Navaratne, and W. Ming, "Multi-objective design of single-phase differential buck inverters with active power decoupling," *IEEE Open Journal of Power Electronics*, vol. 3, pp. 105–114, 2022.

[2] National Aeronautics and Space Administration, "The effects of climate change," Aug. 2021, Accessed: Nov. 28, 2021. [Online]. Available: https://climate.nasa.gov/effects/.

[3] United Nation, "The Paris Agreement," Dec. 2015, Accessed: Nov. 28, 2021. [Online]. Available: https://unfccc.int/process-and-meetings/the-paris-agreement/the-paris-agreement.

[4] European Commission, "A European Green Deal," Dec. 2019, Accessed: Nov. 28, 2021. [Online]. Available: https://ec.europa.eu/info/strategy/priorities-2019-2024/european-green-deal.

[5] Department for Business, Energy and Industrial Strategy, UK, "The Net Zero Strategy," Oct. 2021, Accessed: Nov. 28, 2021. [Online]. Available: https://www.gov.uk/government/publications/net-zero-strategy.

[6] ——, "The ten point plan for a green industrial revolution," Nov. 2020, Accessed: Nov. 28, 2021. [Online]. Available: https://www.gov.uk/government/publications/the-ten-point-plan-for-a-green-industrial-revolution.

[7] X. She, A. Q. Huang, O. Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, 2017.

[8] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, 2014.

[9] P. Roussel, "SiC market and industruy update," presented at the Int. SiC Power Electron. Appl. Workshop, Kista, Sweden, 2012.

[10] F. Wang, Z. Zhang, T. Ericsen, R. Raju, R. Burgos, and D. Boroyevich, "Advances in power conversion and drives for shipboard systems," *Proc. IEEE*, vol. 103, no. 12, pp. 2285–2311, 2015.

[11] "Power SiC: Materials, device and applications 2020 report," Yole Devélopment, 2020.

[12] Wolfspeed, "C2M0025120D 1200-V SiC MOSFET Datasheet," Accessed: Aug. 10, 2021. [Online]. Available: http://www.wolfspeed.com/downloads/dl/file/id/161/product/8/c2m0025120d.pdf

[13] ——, "C2M0045170D 1700-V SiC MOSFET Datasheet," Accessed: Aug. 10, 2021. [Online]. Available: https://assets.wolfspeed.com/uploads/2020/12/C2M0045170D.pdf

[14] GeneSiC, "G2R1000MT33J 3300-V SiC MOSFET Datasheet," Accessed: Aug. 10, 2021. [Online]. Available: https://www.genesicsemi.com/sic-mosfet/G2R1000MT33J/G2R1000MT33J.pdf

[15] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99sic-based 7 kv/400 v dc transformer for future data centers," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 753–767, 2019.

[16] P. Neudeck, R. Okojie, and L.-Y. Chen, "High-temperature electronics - a role for wide bandgap semiconductors?" *Proc. IEEE*, vol. 90, no. 6, pp. 1065–1076, 2002.

[17] Z. Zhang, "Characterization and modeling of high-switching-speed behavior of sic active devices," 2009.

[18] A. S. Abdelrahman, Z. Erdem, Y. Attia, and M. Z. Youssef, "Wide bandgap devices in electric vehicle converters: A performance survey," *Can. J. Electr. Comput. Eng.*, vol. 41, no. 1, pp. 45–54, 2018.

[19] R. Lai *et al.*, "A systematic topology evaluation methodology for high-density three-phase PWM AC-AC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2665–2680, 2008.

[20] J. Liu, K. L. Wong, S. T. Allen, and J. Mookken, "Performance evaluations of hard-switching interleaved DC-DC boost converter with new generation silicon carbide MOSFETs," 2013.

[21] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched all-Si, Si-SiC, and all-SiC device combinations," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2393–2407, 2014.

[22] Z. Fang, D. Jiang, Z. Shen, and R. Qu, "Impact of application of SiC devices in motor drive on EMI," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2017, pp. 652–658.

[23] C. M. DiMarino, R. Burgos, and B. Dushan, "High-temperature silicon carbide: characterization of state-of-the-art silicon carbide power transistors," *IEEE Ind. Electron. Mag.*, vol. 9, no. 3, pp. 19–30, 2015.

[24] A. Bolotnikov *et al.*, "Overview of 1.2kv - 2.2kv SiC MOSFETs targeted for industrial power conversion applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2015, pp. 2445–2452.

[25] P. Ning, Z. Liang, and F. Wang, "Double-sided cooling design for novel planar module," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2013, pp. 616–621.

[26] J. Biela, J. W. Kolar, A. Stupar, U. Drofenik, and A. Musing, "Towards virtual prototyping and comprehensive multi-objective optimisation in power electronics," in *Proc. PCIM Europe*, 2010.

[27] L. Xie, X. Yuan, and W. Wang, "Thermal modeling of fan-cooled plate-fin heatsink considering air temperature rise for virtual prototyping of power electronics," *IEEE Trans. Compon. Packaging Manuf. Technol.*, vol. 10, no. 11, pp. 1829–1839, 2020.

[28] ——, "Thermal-flow network modeling for virtual prototyping of power electronics," *IEEE Trans. Compon. Packaging Manuf. Technol.*, vol. 11, no. 8, pp. 1282–1291, 2021.

[29] R. M. Burkart and J. W. Kolar, "Comparative η-ρ-σ pareto optimization of Si and SiC multilevel dual-active-bridge topologies with wide input voltage range," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5258–5270, 2017.

[30] Y. Mukunoki *et al.*, "An improved compact model for a silicon-carbide MOSFET and its application to accurate circuit simulation," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9834–9842, 2018.

[31] H. Sakairi, T. Yanagi, H. Otake, N. Kuroda, and H. Tanigawa, "Measurement methodology for accurate modeling of SiC MOSFET switching behavior over wide voltage and current ranges," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7314–7325, Sept. 2018.

[32] Y. Mukunoki *et al.*, "Characterization and modeling of a 1.2-kV 30-A silicon-carbide MOSFET," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4339–4345, 2016.

[33] Z. Dong, X. Wu, H. Xu, N. Ren, and K. Sheng, "Accurate analytical switching-on loss model of SiC MOSFET considering dynamic transfer characteristic and [qgd]," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12 264–12 273, 2020.

[34] Wolfspeed, "Wolfspeed C3M SiC 1200V MOSFETs," June. 2020, Accessed: Dec. 01, 2021. [Online]. Available: https://www.mouser.co.uk/new/wolfspeed/wolfspeed-c3m-1200vsic-mosfets/.

[35] Infineon, "Silicon Carbide CoolSiC MOSFETs," Nov. 2021, Accessed: Dec. 01, 2021. [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/silicon-carbide/.

[36] Rohm, "Trench-structure SiC-MOSFETs and Actual Products," Jan. 2018, Accessed: Dec. 01, 2021. [Online]. Available: https://techweb.rohm.com/knowledge/sic/s-sic/04-s-sic/6574.

[37] *Unipolar Power Switching Devices*. John Wiley & Sons, Ltd, 2014, ch. 8, pp. 301–352. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/9781118313534.ch8

[38] B. Baliga, *Silicon Carbide Power Devices*. World Scientific Publishing Company, 2006. [Online]. Available: https://books.google.co.uk/books?id=M87ICgAAQBAJ

[39] K. T. McDonald, "Electric field distribution in a reverse-biased p-n junction," Sept. 2015, Accessed: Dec. 1, 2021. [Online]. Available: https://www.hep.princeton.edu/~mcdonald/examples/diode.pdf.

[40] K. Han and B. J. Baliga, "Operation of 1.2-kV 4H-SiC accumulation and inversion channel split-gate (SG) MOSFETs at elevated temperatures," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3333–3338, 2018.

[41] B. Nel and S. Perinpanayagam, "A brief overview of SiC MOSFET failure modes and design reliability," *Procedia CIRP*, vol. 59, pp. 280–285,

2017, proceedings of the 5th International Conference in Through-life Engineering Services Cranfield University, 1st and 2nd November 2016. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2212827116309593

[42] B. J. Baliga, *Advance power MOSFET concept.* Springer Science & Business Media, 2010.

[43] Wolfspeed, "CAS120M12BM2 1200 V 120 A SiC MOSFET power module, Datasheet," Accessed: Dec. 01, 2021. [Online]. Available: https://www.wolfspeed.com/media/downloads/179/CAS120M12BM2.pdf.

[44] S. Jahdi, O. Alatise, C. Fisher, L. Ran, and P. Mawby, "An evaluation of silicon carbide unipolar technologies for electric vehicle drive-trains," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 3, pp. 517–528, 2014.

[45] S. B. Ben Streetman, *Solid state electronic devices, 6th edition.* Pearson, 2006.

[46] K. Chen, Z. Zhao, L. Yuan, T. Lu, and F. He, "The impact of nonlinear junction capacitance on switching transient and its modeling for SiC MOSFET," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 333–338, 2015.

[47] K. Krisch, J. Bude, and L. Manchanda, "Gate capacitance attenuation in MOS devices with thin gate dielectrics," *IEEE Electron Device Lett.*, vol. 17, no. 11, pp. 521–524, 1996.

[48] B. J. Baliga, *Fundamentals of power semiconductor devices.* Springer Science & Business Media, 2010.

[49] S. Yin *et al.*, "An accurate subcircuit model of SiC half-bridge module for switching-loss optimization," *IEEE Trans. Ind. Appl.*, vol. 53, no. 4, pp. 3840–3848, July-Aug. 2017.

[50] N. Arora, *SPICE Diode and MOSFET Models and Their Parameters.* Vienna: Springer Vienna, 1993, pp. 536–562. [Online]. Available: https://doi.org/10.1007/978-3-7091-9247-4_11

[51] A. Marzoughi, R. Burgos, and D. Boroyevich, "Characterization and performance evaluation of the state-of-the-art 3.3 kV 30 A full-SiC MOSFETs," *IEEE Trans. Ind. Appl.*, vol. 55, no. 1, pp. 575–583, 2019.

[52] J. Wang, H. Chung, and R. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, pp. 573–590, 2013.

[53] Z. Zeng and X. Li, "Comparative study on multiple degrees of freedom of gate drivers for transient behavior regulation of SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8754–8763, 2018.

[54] Fei (Fred) Wang, Zheyu Zhang, and Edward A. Jones, *Characterization of Wide Bandgap Power Semiconductor Devices.* Institution of Engineering and Technology, 2018. [Online]. Available: https://digital-library.theiet.org/content/books/po/pbpo128e.

[55] X. Chen, S. Jiang, Y. Chen, H. Gou, Q. Xie, and B. Shen, "Transient modeling and loss analysis of SiC MOSFETs at cryogenic and room temperatures," *IEEE Trans. Appl. Supercond.*, vol. 31, no. 8, pp. 1–4, 2021.

[56] H. Gui *et al.*, "Characterization of 1.2 kV SiC power MOSFETs at cryogenic temperatures," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, 2018, pp. 7010–7015.

[57] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Instability in half-bridge circuits switched with wide band-gap transistors," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2380–2392, 2014.

[58] Z. Zhang, B. Guo, F. F. Wang, E. A. Jones, L. M. Tolbert, and B. J. Blalock, "Methodology for wide band-gap device dynamic characterization," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9307–9318, 2017.

[59] Tektronix, "ABCs of Probes Primer," Accessed: Dec. 3, 2021. [Online]. Available: https://uk.tek.com/document/primer/abcs-probes-primer.

[60] ——, "High Voltage Differential Probes," Accessed: Dec. 3, 2021. [Online]. Available: https://uk.tek.com/probes-and-accessories/high-voltage-differential-probes.

[61] ——, "Passive Probe," Accessed: Dec. 3, 2021. [Online]. Available: https://uk.tek.com/passive-probe.

[62] ——, "IsoVu Isolated Probes," Accessed: Dec. 3, 2021. [Online]. Available: https://uk.tek.com/isolated-measurement-systems.

[63] T & M research product, "SSDN series coaxial shunt," Accessed: Dec. 3, 2021. [Online]. Available: http://www.tandmresearch.com/.

[64] N. Kondrath and M. K. Kazimierczuk, "Bandwidth of current transformers," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 6, pp. 2008–2016, 2009.

[65] D. A. Ward and J. Exon, "Using Rogowski coils for transient current measurements," *Engineering Science and Education Journal*, vol. 2, pp. 105–113, 1993.

[66] W. Zhang, Z. Zhang, and F. Wang, "Review and bandwidth measurement of coaxial shunt resistors for wide-bandgap devices dynamic characterization," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, 2019, pp. 3259–3264.

[67] Z. Chen, "Characterization and realization of high switching-speed capability of sic power devices in voltage source converter," Master's thesis, University of Tennessee, 2015.

[68] Z. Zhang *et al.*, "Methodology for switching characterization evaluation of wide band-gap devices in a phase-leg configuration," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 2534–2541.

[69] S. Yin *et al.*, "Automatic V - I alignment for switching characterization of wide band gap power devices," in *2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, 2018, pp. 75–78.

[70] D. Garrido, I. Baraia-Etxaburu, J. Arza, and M. Barrenetxea, "Simple and affordable method for fast transient measurements of SiC devices," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2933–2942, 2020.

[71] E. A. Jones *et al.*, "Characterization of an enhancement-mode 650-V GaN HFET," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, 2015, pp. 400–407.

[72] X. Li *et al.*, "Achieving zero switching loss in silicon carbide MOSFET," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12 193–12 199, 2019.

[73] Keysight, "B1505A power device analyser User Mannual," Accessed: Sept. 26, 2021. [Online]. Available: https://www.keysight.com/gb/en/assets/9018-01849/user-manuals/9018-01849.pdf

[74] P. Sun *et al.*, "An online junction temperature monitoring correction method for SiC MOSFETs at different parasitic parameters," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, pp. 1–1, 2021.

[75] C. Salcines, A. Kruglov, and I. Kallfass, "A novel characterization technique to extract high voltage - high current IV characteristics of power mosfets from dynamic measurements," in *proc. IEEE 6th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Oct. 2018, pp. 1–6.

[76] T. Yanagi, H. Sakairi, H. Otake, N. Kuroda, K. Nakahara, and H. Tanigawa, "Measurement scheme to model an SiC MOSFET for simulating its switching

behaviors," in *Proc. Inter. Expo. Conf. Power Elec. (PCIM)*, May 2017, pp. 811–815.

[77] M. Riccio, V. d'Alessandro, G. Romano, L. Maresca, G. Breglio, and A. Irace, "A temperature-dependent SPICE model of SiC Power MOSFETs for within and out-of-SOA simulations," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 8020–8029, 2018.

[78] Y. Mukunoki *et al.*, "An improved compact model for a Silicon-Carbide MOSFET and its application to accurate circuit simulation," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9834–9842, Nov. 2018.

[79] Y. Nakamura, N. Kuroda, T. Yanagi, H. Sakairi, and K. Nakahara, "High-voltage and high-current Id-Vds measurement method for power transistors improved by reducing self-heating," *IEEE Electron Device Lett.*, vol. 41, no. 4, pp. 581–584, April 2020.

[80] Vrej Barkhordarian, "Power MOSFET Basics," Accessed: Dec. 4, 2021. [Online]. Available: https://www.infineon.com/dgdl/mosfet.pdf?fileId=5546d462533600a4015357444e913f4f.

[81] Keysight Technologies, "E4990A Impedance Analyzer," Accessed: Dec. 4, 2021. [Online]. Available: https://www.keysight.com/gb/en/product/E4990A/impedance-analyzer-20-hz-10-20-30-50-120-mhz.html.

[82] Rohm, "SCT3080KL 1200 V 31 A SiC MOSFET, Datasheet," Accessed: Dec. 3, 2021. [Online]. Available: https://fscdn.rohm.com/en/products/databook/datasheet/discrete/sic/mosfet/sct3080kl-e.pdf.

[83] Infineon, "IMBG120R045M1H 1200 V 47 A SiC MOSFET, Datasheet," Accessed: Dec. 3, 2021. [Online]. Available: https://www.infineon.com/dgdl/Infineon-IMBG120R045M1H-DataSheet-v02_02-EN.pdf?fileId=5546d462749a7c2d0174b0ecc4e83263.

[84] Z. Zhu, G. Gildenblat, C. C. McAndrew, and I.-S. Lim, "Modeling the frequency dependence of MOSFET gate capacitance," in *2011 IEEE ICMTS International Conference on Microelectronic Test Structures*, 2011, pp. 13–18.

[85] Y. Mukunoki *et al.*, "Modeling of a silicon-carbide MOSFET with focus on internal stray capacitances and inductances, and its verification," *IEEE Trans. Ind. Appl.*, vol. 54, no. 3, pp. 2588–2597, 2018.

[86] Z. Duan, T. Fan, X. Wen, and D. Zhang, "Improved SiC power MOSFET model considering nonlinear junction capacitances," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2509–2517, 2018.

[87] H. A. Mantooth, K. Peng, E. Santi, and J. L. Hudgins, "Modeling of wide bandgap power semiconductor devices—Part I," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 423–433, 2015.

[88] R. Fu, A. Grekov, J. Hudgins, A. Mantooth, and E. Santi, "Power SiC DMOSFET model accounting for nonuniform current distribution in JFET region," *IEEE Trans. Ind. Appl.*, vol. 48, no. 1, pp. 181–190, 2012.

[89] S. K. Powell, N. Goldsman, J. M. McGarrity, J. Bernstein, C. J. Scozzie, and A. Lelis, "Physics-based numerical modeling and characterization of 6h-silicon-carbide metal–oxide–semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 92, no. 7, pp. 4053–4061, 2002.

[90] V. Talesara *et al.*, "Dynamic switching of SiC power MOSFETs based on analytical subcircuit model," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9680–9689, Sept. 2020.

[91] C. He *et al.*, "A physically based scalable SPICE model for silicon carbide power MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2017, pp. 2678–2684.

[92] Y. Xu, C. Ho, A. Ghosh, and D. Muthumuni, "Design, implementation, and validation of electro-thermal simulation for SiC MOSFETs in power electronic systems," *IEEE Trans. Ind. Appl.*, pp. 1–1, 2021.

[93] K. Han, B. J. Baliga, and W. Sung, "Split-gate 1.2-kv 4h-sic mosfet: Analysis and experimental validation," *IEEE Electron Device Lett.*, vol. 38, no. 10, pp. 1437–1440, 2017.

[94] Z. Duan, T. Fan, X. Wen, and D. Zhang, "Improved SiC power MOSFET model considering nonlinear junction capacitances," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2509–2517, 2018.

[95] H. A. Mantooth, K. Peng, E. Santi, and J. L. Hudgins, "Modeling of wide bandgap power semiconductor devices − Part I," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 423–433, 2015.

[96] H. Li, X. Zhao, K. Sun, Z. Zhao, G. Cao, and T. Q. Zheng, "A non-segmented PSpice model of SiC MOSFET with temperature-dependent parameters," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4603–4612, May 2019.

[97] A. Rashid, M. M. Hossain, A. Emon, and H. E. C. A. Mantooth, "Datasheet-driven compact model of silicon carbide power MOSFET including third quadrant behavior," *IEEE Trans. Power Electron.*, pp. 1–1, 2021.

[98] Keysight Technologies, Angelov model. [Online]. Available: https://edadocs.software.keysight.com/pages/viewpage.action?pageId=5692701

[99] W. Jouha, A. E. Oualkadi, P. Dherbécourt, E. Joubert, and M. Masmoudi, "Silicon carbide power MOSFET model: An accurate parameter extraction method based on the levenberg-marquardt algorithm," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9130–9133, 2018.

[100] Keysight, "PathWave Device Modeling (IC-CAP)," Accessed: Dec. 3, 2021. [Online]. Available: https://www.keysight.com/gb/en/assets/7018-06692/technical-overviews/5965-7742.pdf.

[101] D. Chiozzi, M. Bernardoni, N. Delmonte, and P. Cova, "A neural network based approach to simulate electrothermal device interaction in SPICE environment," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4703–4710, May 2019.

[102] S. Hatami, M. Azizi, H. Bahrami, D. Motavalizadeh, and A. Afzali-Kusha, "Accurate and efficient modeling of SOI MOSFET with technology independent neural networks," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 23, no. 11, pp. 1580–1587, 2004.

[103] H. B. Hammouda, M. Mhiri, Z. Gafsi, and K. Besbes, "Neural-based models of semiconductor devices for SPICE simulator," *Am. J. Appl. Sci.*, vol. 5, no. 4, pp. 385–391, 2008.

[104] G. Cybenko, "Approximations by superpositions of a sigmoidal function," *Math. of Con.l, Signals, and Syst.*, vol. 2, pp. 183–192, 1989.

[105] Y. Xu, C. N. M. Ho, A. Ghosh, and D. Muthumuni, "A datasheet-based behavioral model of SiC MOSFET for power loss prediction in electromagnetic transient simulation," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, 2019, pp. 521–526.

[106] M. Mudholkar, S. Ahmed, M. N. Ericson, S. S. Frank, C. L. Britton, and H. A. Mantooth, "Datasheet driven silicon carbide power MOSFET model," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2220–2228, 2014.

[107] K. Sun, H. Wu, J. Lu, Y. Xing, and L. Huang, "Improved modeling of medium voltage SiC MOSFET within wide temperature range," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2229–2237, May 2014.

[108] A. Rashid, M. M. Hossain, A. Emon, and H. E. C. A. Mantooth, "Datasheet-driven compact model of silicon carbide power MOSFET including third quadrant behavior," *IEEE Trans. Power Electron.*, pp. 1–1, 2021.

[109] A. Endruschat, C. Novak, H. Gerstner, T. Heckel, C. Joffe, and M. Marz, "A universal SPICE field-effect transistor model applied on SiC and GaN transistors," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9131–9145, Sep. 2019.

[110] L. Xiao, J. Zhao, B. Zhang, D. Chen, and L. Wu, "A unified electrothermal behavior modeling method for both SiC MOSFET and GaN HEMT," *IEEE Trans. Ind. Electron.*, pp. 1–1, 2020.

[111] H. Sakairi, T. Yanagi, H. Otake, N. Kuroda, and H. Tanigawa, "Measurement methodology for accurate modeling of SiC MOSFET switching behavior over wide voltage and current ranges," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7314–7325, 2018.

[112] M. Noborio, Y. Kanzaki, Jun Suda, and T. Kimoto, "Experimental and theoretical investigations on short-channel effects in 4H-SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 1954–1962, 2005.

[113] B. Van Zeghbroeck, "Principles of semiconductor devices," *Colarado University*, vol. 34, 2004.

[114] Z. Chen, D. Boroyevich, R. Burgos, and F. Wang, "Characterization and modeling of 1.2 kV, 20 A SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sept. 2009, pp. 1480–1487.

[115] P. Yang, W. Ming, J. Liang, I. Ludtke, S. Berry, and K. Floros, "Hybrid data-driven modelling methodology for fast and accurate transient simulation of SiC MOSFETs," *IEEE Trans. Power Electron.*, pp. 1–1, Aug. 2021, (Early Access).

[116] Z. Dong, X. Wu, H. Xu, N. Ren, and K. Sheng, "Accurate analytical switching-on loss model of SiC MOSFET considering dynamic transfer characteristic and Qgd," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12 264–12 273, Nov. 2020.

[117] G. F. Luger, *Artificial intelligence: structures and strategies for complex problem solving.* Pearson education, 2005.

[118] Y. Liu, J. A. Starzyk, and Z. Zhu, "Optimized approximation algorithm in neural networks without overfitting," *IEEE Trans. Neural Netw.*, vol. 19, no. 6, pp. 983–995, 2008.

[119] C. C. McAndrew, "SPICE modeling in verilog-A: Successes and challenges: Invited paper," in *Proc. 47th Eur. Solid-State Device Res. Conf. (ESSDERC)*, 2017, pp. 22–25.

[120] F. García-Redondo, R. P. Gowers, A. Crespo-Yepes, M. López-Vallejo, and L. Jiang, "SPICE compact modeling of bipolar/unipolar memristor switching governed by electrical thresholds," vol. 63, no. 8, pp. 1255–1264, 2016.

[121] Y. Liu, K. Y. See, S. Yin, R. Simanjorang, A. K. Gupta, and J. Lai, "Equivalent circuit model of high power density SiC converter for common-mode conducted emission prediction and analysis," *IEEE Electromagn. Compat. Mag.*, vol. 8, no. 1, pp. 67–74, 2019.

[122] Y. Wu, S. Yin, H. Li, and W. Ma, "Impact of *RC* snubber on switching oscillation damping of SiC MOSFET with analytical model," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 163–178, 2020.

[123] *Pspice A/D Reference Guide, Version 16.5*, Cadence Design System, Portland, OR, USA, 2011.

[124] *Wolfspeed, LTspice and PLECS Models.* [Online]. Available: http://go.wolfspeed.com/all-models.

[125] M. Noborio, Y. Kanzaki, Jun Suda, and T. Kimoto, "Experimental and theoretical investigations on short-channel effects in 4H-SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 1954–1962, 2005.

[126] *CGD15HB62P1 – Gate driver board for 1200 V SiC MOSFET power modules*. [Online]. Available: https://www.wolfspeed.com/cgd15hb62p1

[127] *PathWave Advanced Design System*. [Online]. Available: https://www.keysight.com/gb/en/products/software/pathwave-design-software/pathwave-advanced-design-system.html

[128] Infineon, "IMW120R020M1H 1200 V 20 mohms SiC MOSFET, Datasheet," Accessed: Apr. 03, 2022. [Online]. Available: www.infineon.com/dgdl/Infineon-IMW120R020M1H-DataSheet-v01_00-EN.pdf?fileId=8ac78c8c7f2a768a017f8767f7bb318f.

[129] Onsemi, "NTBG020N120SC1 1200 V 20 mohms SiC MOSFET, Datasheet," Accessed: Apr. 03, 2022. [Online]. Available: www.onsemi.com/pdf/datasheet/ntbg020n120sc1-d.pdf.