Load-Pull Data Analysis of a GaN on SiC HEMT Targeting Multi Bias Doherty Design

Ehsan M. Azad[1], Roberto Quaglia[1], James J. Bell[1], Kauser Chadhary[1], Anh Nghiem[2], Komo Sulaksono[2], and Paul J. Tasker[1]
[1]Cardiff University, Cardiff, UK (mailto: azadem@cardiff.ac.uk)
[2]Ampleon Netherlands B.V., Nijmegen, The Netherlands

***Abstract*—This paper presents an analysis of load-pull measurement data of a GaN on SiC high electron mobility transistor (HEMT) at 3.6 GHz, oriented to aid the design of Doherty power amplifiers with multiple DC supply voltages. Fundamental load-pull data in class AB configuration are analyzed to realize the optimum load modulation for the design of the "Main" amplifier at DC bias levels of 28 V and 50 V.**

***Index Terms*—Load-pull, Gallium nitride, Power amplifier.**

I. Introduction

THE complexity of modern communication signals and their high peak-to-average power ratio (PAPR) has led to overall power-inefficiency of classical linear power amplifiers (PAs) structures (e.g. class A and class AB PAs). Hence, efficiency enhancement solutions such as Doherty power amplifier (DPA) have become very popular to achieve high efficiency at output back-off power (OBO) levels [1], [2].

The principal of the Doherty power amplifiers (DPAs) is based on active load modulation of the "Main" PA (typically biased in class AB) via an "Auxiliary" PA (usually biased in class C). At OBO, when the Auxiliary PA is OFF, the Main PA is terminated at higher resistive load (two times the optimum load for classical DPA with 6 dB OBO) to achieve higher efficiency. Once the input drive passes the OBO threshold, the Auxiliary PA switches ON and begins contributing to the overall output power, as well as actively modulating the Main PA's load to a lower level (optimum load).

By adapting the DC supply voltage of a conventional DPA to the average power (for example at different traffic conditions), its dynamic range can be improved such that efficiency is maintained at lower OBO levels, see [3] and [4] for examples. However, this adds further complexity to the design, which needs detailed characterization to realize successful practical implementation.

This paper focuses on experimental characterization of gain and efficiency of a GaN-on-SiC HEMT based on load-pull measurement data, aiming to provide a tailored framework for design of the Main PA of a multi-bias DPA.

II. Measurement Strategy

Fundamental load-pull measurements were performed at 3.6 GHz at 4 different DC supply voltages $V_{ds} = 20, 30, 40$ and 50 V using a hybrid load-pull set up. The device under test (DUT) was a 10 W GaN-on-SiC packaged device from Ampleon. The load-pull grid was selected in a way to capture the optimum load points at all the V_{ds} levels, as shown in Fig. 1.

The DC-dependent Cardiff behavioral model [5] was used to generate a model from the measurement data which was then imported into the ADS computer-aided design (CAD) simulator for further analysis. For this analysis two widely used drain supply voltages for GaN HEMTs (28 V, and 50 V) are considered. To negate the effect of output capacitance, associated with the package, the reference plane was moved to the die plane by the de-embedding process.

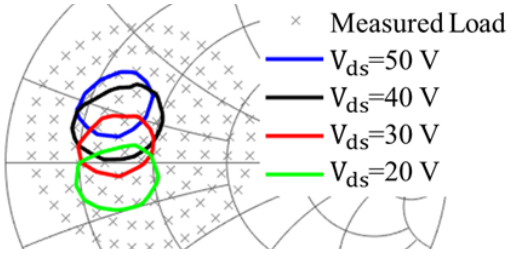


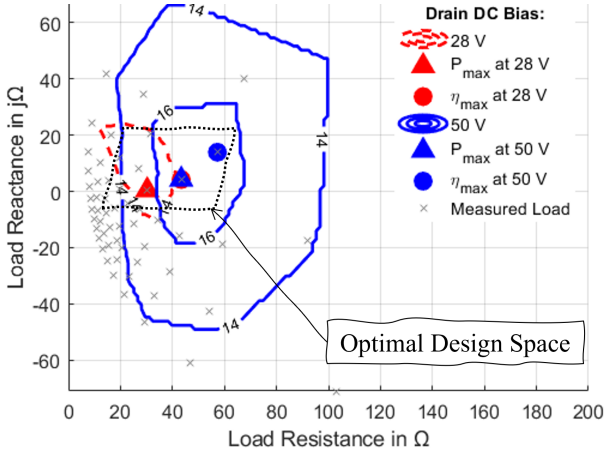
Fig. 1. Load-pull grid and 0.5 dB power contours at different V_{ds} levels at the package reference plane. The load-pull grid was selected in a way to cover the area around the optimum loads at all the drain bias levels.

III. Load-pull Data Analysis

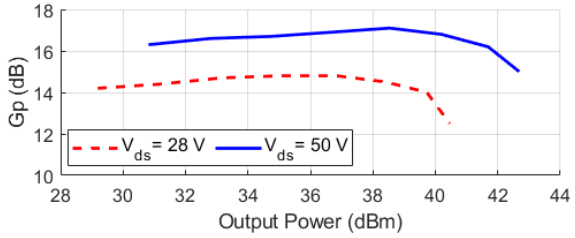
A. Gain

Although the concept of achieving higher efficiency by reducing the DC supply voltage in PAs might be considered straightforward, there are other practical considerations which have restrained the large-scale utilization of this method. One of the main challenges is the strong gain reduction that can occur with reducing DC supply voltage, as it was studied in [6] for GaN HEMTs. Our strategy is to try to minimize this gain reduction.

Note, at this stage in our analysis, to eliminate the effect of input match, power gain (G_p) is preferred over transducer gain (G_t). As illustrated by the gain contours in Fig. 2. (a), DUT's gain is susceptible to the load impedance. The same plot shows the optimum loads for maximum power and efficiency at both DC supply voltages. Therefore, the area identified as "Optimal Design Space" refers to the range of load-impedances which can be selected to achieve a desired gain performance at different supply voltages while operating in a Doherty design space.



(a)



(b)

Fig. 2. Gain (G_P) characterization of the DUT at 28 V and 50 V. (a) 14 dB and 16 dB G_P contours and optimum load impedances for both supply voltages at the die reference plane. (b) G_P vs output power (P_{out}) at the optimum load of each supply voltage.

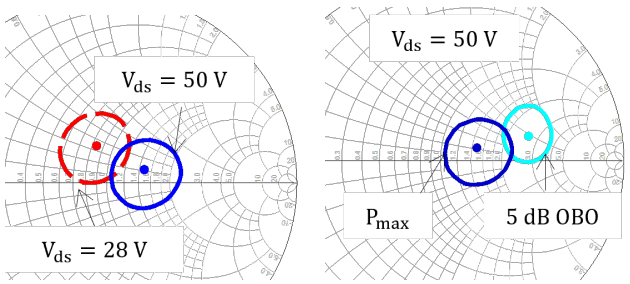
Fig. 2 (b) shows the G_p performance vs output power for both supply voltages at their respective optimum load impedance for power. Since we are aiming to achieve maximum gain at each supply voltage, the information in Fig. 2 (b) will be used as benchmark to compare the final design's gain performance.

B. Efficiency

The efficiency's optimum load resistance of the Main PA changes respective to the available power P_{av}. The goal of designing a DPA is to correctly track this change and establish a load modulation scheme as a function of P_{av} ($\Gamma_{L,opt} = f(P_{av})$). For design's involving multiple supply voltages, an additional dimension needs to be considered in the load modulation scheme as the optimum load is now also dependent on the supply voltage ($\Gamma_{L,opt} = f(P_{av}, V_{ds})$). Fig. 3 (a) illustrates the dependency of the optimum load on changes in supply voltages, where its dependency on P_{av} is depicted in Fig. 3 (b).

As shown in Fig. 3 (a), the optimum load has a tendency toward the lower resistive load as the V_{ds} is reduced. On the other hand, as shown in Fig. 3 (b) for $V_{ds} = 50$ V, larger resistive load is needed for an efficient Main PA at OBO. Fig. 4 comprehensively pictures the dependency of optimum load on both supply voltage and drive level ($\Gamma_{L,opt} = f(P_{av}, V_{ds})$).

The behavior illustrated in Fig. 4 can provide a benchmark to design a load-modulation scheme to achieve optimal efficiency performance at OBO at various supply voltages.



(a) (b)

Fig. 3. 3% efficiency contours at the die reference plane. (a) maximum drive level at $V_{ds} = 28$ V, 50 V. (b) is $V_{ds} = 50$ V at maximum drive level and 5 dB OBO.

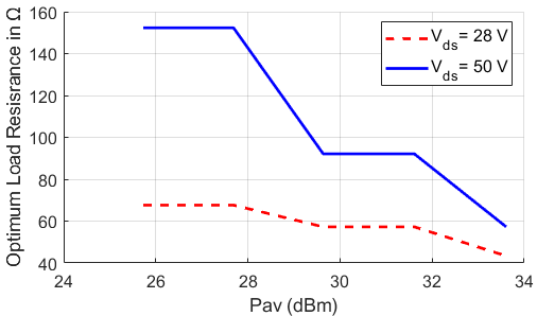


Fig. 4. Optimum load resistance at the die reference plane vs P_{av} at $V_{ds} = 28$ V, 50 V.

IV. Simulation Results

Based on the information presented in Fig. 2 and Fig. 4 a simulation template was designed to investigate the PA's behavior under different load-modulation scenarios. To do so, a look-up indexing table, similar to that shown in Table I, was imported into the simulator environment providing the source power and corresponding load conditions.

TABLE I
EXAMPLE OF LOOK-UP INDEXING TABLE TO, PASSIVELY, MODULATE THE MAIN PA'S LOAD AS A FUNCTION OF INPUT DRIVE LEVEL.

index	P_{av}	Z_L
1	P_1	Z_1
2	P_2	Z_2
3	P_3	Z_3
⋮	⋮	⋮
N	$P_N = max$	Z_N

As illustrated in Fig. 4, in order to achieve peak efficiency at each supply voltage, a different load modulation would be preferred. However, this is impractical in a real Doherty where same or similar load modulation can be expected at different bias voltages since the current ratios between Main and Auxiliary are, in principle, not impacted by supply voltage, and the Doherty combiner is passive. Therefore, we can use the "look-up table" method proposed here to test load modulation trajectories maintained equal vs. bias conditions against the optimum, independent trajectories.

As an example, Fig. 5 shows a series of different load modulations, with an OBO of ∼5 dB, compared to the "Ideal" load trajectory. The "Ideal" refers to the simulation setup where separate load modulations were used at each supply voltage to achieve the best Doherty performance at each supply voltage. The "Optimum" refers to the preferable performance under a more practical simulation setup, where the same load trajectory was used for both supply voltages.

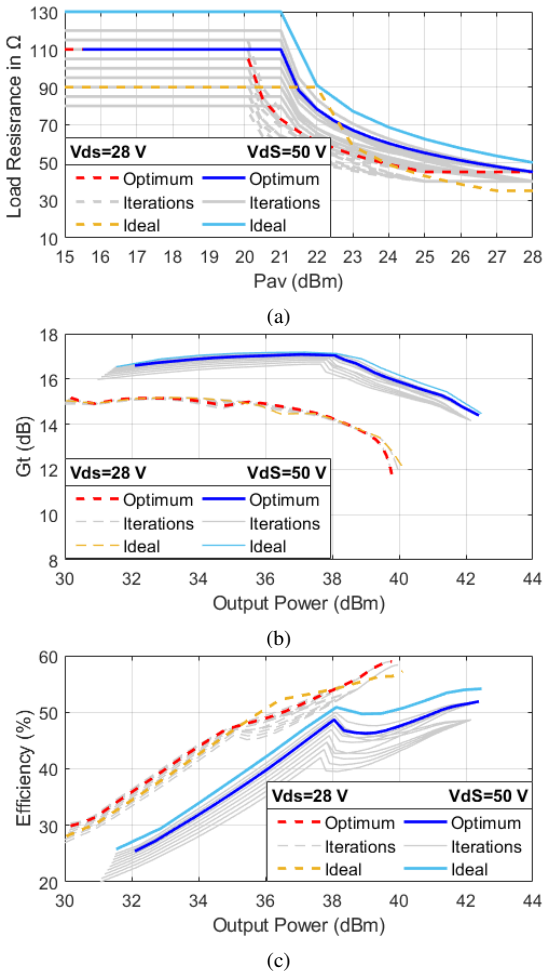


Fig. 5. Simulation results of an example PA (Microstrip component design). (a) tested load modulations using a look-up table similar format to Table I and (b) gain; (c) Efficiency.

As can be seen from Fig. 5 using the proposed look-up indexing simulation method, the behaviour of the Main PA can be investigated under many "Iterations" of the load trajectory. In this example, the "Optimum" load trajectory, ranging from 110 Ω to 45 Ω, provides the best compromise between the gain and efficiency at both supply voltages.

Note, as we are only observing the Main device, there is no contribution to the output power from an Auxiliary PA, therefore OBO is less than 5 dB. However, this analysis sets a firm expectation on the performance of the Auxiliary PA to provide a desired load modulation for the Main PA.

To this point, our analysis was based on the data at the de-embedded reference plane. To evaluate the load trajectories at the package plane, Fig. 6 shows the "Optimum" load modulation superimposed to the 3% efficiency contours of the DUT at maximum power level and OBO for both 28 V and 50 V supply voltages.

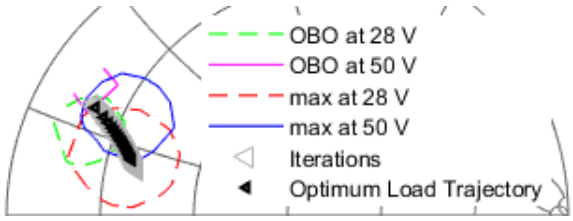


Fig. 6. Load modulations superimposed to efficiency contours at package reference plane for both 28 V and 50 V supply voltages.

As shown in Fig. 6 the optimum modulation follows a path from optimal efficiency contour at OBO to the one at maximum power level.

However, at the package reference plane the information has lost their link to the theoretical explanation of DPAs (now the optimum load resistance at OBO is lower than at maximum power). On the other hand, as shown in Fig. 6 it is impossible to distinguish between different iterations and identify the optimum trajectory. Therefore, one might struggle to justify their choice of design solely on the information given at the package reference plane.

V. Conclusion

Work presented in this paper provided a practical framework for optimal design of the Main PA of a Doherty power amplifier under multiple supply voltages. At each stage of the analysis, the optimal characterization of the DUT was identified to enable designers to understand how far their design have deviated from the optimal performance.

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