GaN-based Single-phase Differential PV Inverters

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Abstract

Differential PV inverters have the benefits of second-order ripple elimination and leakage current suppression. Therefore, the need for additional components such as switch, inductor, capacitor, and transformer to achieve the power decoupling function and galvanic isolation can be avoided. In recent years, GaN devices used to improve the performance of differential PV inverters, which have the advantages of high switching frequency, high operating temperature, and high operating voltage. However, using GaN devices cannot guarantee better performance of inverters because the GaN device performance depends on the design parameters, such as switching frequency and operating temperature. To fully utilise the benefits of the GaN device, the design challenges and the complex trade-offs between components associated with inverters need to be addressed. Therefore, this thesis investigates impacts of GaN devices-based single-phase differential PV inverters with the aim to optimise inverter efficiency, power density, and cost using systematic design and control approaches.

In single-phase differential inverters, active power decoupling methods are often aimed to reduce the total capacitance as much as possible, which sacrifices the overall efficiency and volume of the inverter. To address that, a trade-off analysis of all the active and passive components of the GaN-based differential buck inverters is developed through detailed mathematical modelling. Then, a multi-objective optimisation method based on geometric programming is presented to optimise the efficiency and power density. The design method is based on power loss and volume of the inverter by considering the dominant design parameters. As a result, the maximum limit of design trends can be obtained, which gives more freedom to choose the best design.

The aforementioned multi-objective optimisation methods require extensive mathematical models and more system information to find an optimal design. It increases the computational complexity, needs multiple conditions to eliminate unwanted solutions, and requires more time to choose the optimal design. Therefore, an ANN-based multi-objective design method

is developed to improve accuracy and reduce computational burdens. A buck-type differential inverter is used to verify the ANN-based design method in both simulation and experiment.

The previous two studies are based on buck-type differential inverters, which need an additional front-end DC-DC converter for solar PV application to meet the wide voltage requirements. This inverter requires an additional hardware controller, reduces efficiency and power density, and increases cost. Single-stage inverters are widely popular in industrial and commercial applications because of their higher efficiency and simple control. A novel single-stage buck-boost inverter topology based on GaN devices is proposed, simulated, and experimentally verified the performances. It has been observed that the maximum efficiency of the prototype is 97.89%, the power density is improved to 3.5kW/dm^3 and the components cost of the prototype is £136.16.

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List of Abbreviations

AC - Alternating Current

AI - Artificial Intelligence

ANN - Artificial Neural Network

CCS - Code Composer Studio

DC - Direct Current

FET - Field-effect transistor

FFT - Fast Fourier Transform

GA - Genetic Algorithm

GaN - Gallium Nitride

GP - Geometric Programming

kW - Kilowatts

MPPT - Maximum Power Point Tracking

MW - megawatt

PI - Proportional Integral

PLL - Phase-Locked Loop

PR - Proportional-Resonant

PSO - Particle Swarm Optimisation

PV - Photovoltaic

PWM - Pulse-width Modulation

RMS - Root Mean Square

Si - Silicon

SiC - Silicon-carbide

THD - Total Harmonic Distortion

TI - Texas Instrument

UK - United Kingdom

UPS - Uninterruptible Power Supply

VAT - Value-added tax

WBG - Wide-Bandgap

List of Symbols

A_{sw}	Switch area
C_{oss}	Output capacitance of GaN FET
$f_{2\omega}$	Second-order ripple power frequency
f_{sw}	Switching frequency
$G_{i_{\mathrm{dc}}}(s)$	Second-order ripple controller
$G_{i_{\mathrm{La}}}(s)$	Inductor current controller
$G_{v_{\mathrm{ab}}}(s)$	Output voltage controller
i_{comp}	Second-order ripple current component
I_{g}	Peak value of injected grid current
$I_{\mathrm{RMS,C}}$	RMS current flow through the capacitor
k_P	Proportional gain
k_I	Integral gain
k_r	Fundamental resonant control gain
k_{rh}	*h*-order resonant controller gain
P_{bd}	Bode diode loss
P_{cap}	Capacitor power loss
P_{cond}	Conduction loss

P_{const} Constant power

$P_{\mathrm{C_{oss}}}$ Output capacitor loss

P_{D} Power dissipated by GaN FET

P_{g} Gate loss

P_{ind} Inductor power loss

P_{rr} Reverse recovery loss

P_{sw} Switching loss

P_{out} Output power of the inverter

p_{r} Second-order ripple power

Q_{g} Gate charge

R Fitness value

$R_{\mathrm{DS,on}}$ ON-state resistance of GaN FET

$R_{\mathrm{\theta CS}}$ Thermal resistance from case to mounting surface

$R_{\mathrm{\theta JC}}$ Thermal resistance of junction-to-case

T Target value

$\tan\delta$ Capacitor loss factor

t_{CR} Current rise time of GaN FET

t_{CF} Current fall time of GaN FET

t_{rr} Reverse recovery time

t_{VR} Voltage rise time of GaN FET

t_{VF} Voltage fall time of GaN FET

V_{dc} DC-link voltage

V_{g} Peak value of grid voltage

V_{GS} Gate-source voltage

vol_{cap} Capacitor volume

$vol_{\mathrm{heat\,sink}}$ Heat sink volume

vol_{ind} Inductor volume

vol_{sw} Volume of switch

$V_{\theta\mathrm{SA}}$ Volumetric resistance

Y Output value

ΔV_{dc} DC-link voltage peak-to-peak ripple

Δi_{L} Inductor current ripple

ΔT_{j} Change in junction temperature

ω_0 Angular frequency

φ Phase angle

Σ_{switch} Cost of switch

$\Sigma_{\mathrm{inductor}}$ Cost of inductor

$\Sigma_{\mathrm{capacitor}}$ Cost of capacitor

$\Sigma_{\mathrm{heat\,sink}}$ Cost of heat sink

Chapter 1 Introduction

1.1 Background

Renewable energy is a fast-growing source of energy. It contributes significantly to generation capacity and, when integrated with other sources of energy, renewables can help to meet global energy needs. In the United Kingdom (UK), the contribution of renewable energy sources to electricity generation increased by 13% between 2019 and 2020 [1]. Figure 1.1 shows the contribution of renewable energy sources to electricity generated. Among the renewable energy sources, solar energy is one of the most reliable and it plays an important role in the UK generation mix. In Figure 1.1, it can be seen that generation from solar photovoltaic (PV) increased by 4.6% in this period. In the first quarter of 2021, the installed capacity of solar PV was 175 megawatt (MW) and the total UK solar capacity will be expected to increase 2,711MW by 2023 [2] and [3]. Furthermore, solar PV can be installed in a wide variety of locations, such as roofs top, commercial and industrial properties and on the ground.

Small-scale solar PV systems have drawn attention because they enable domestic customers and businesses to independently generate electricity. Figure 1.2 shows the annual installation capacity of micro-generation in the UK. From 2016 to 2020, almost all of the newly installed micro-generation capacity was solar PV [1]. According to the Solar Trade Association (trading as Solar Energy UK since April 2021), around 900,000 British homes have installed solar PV panels [3]. Despite the end of the feed-in-tariff in April 2019 and the increase in value-added tax (VAT) for solar installations, the market continues to grow. According to GreenMatch [3], 2,375 new sub-4 kilowatt (kW) solar panel installations were approved in June 2021.

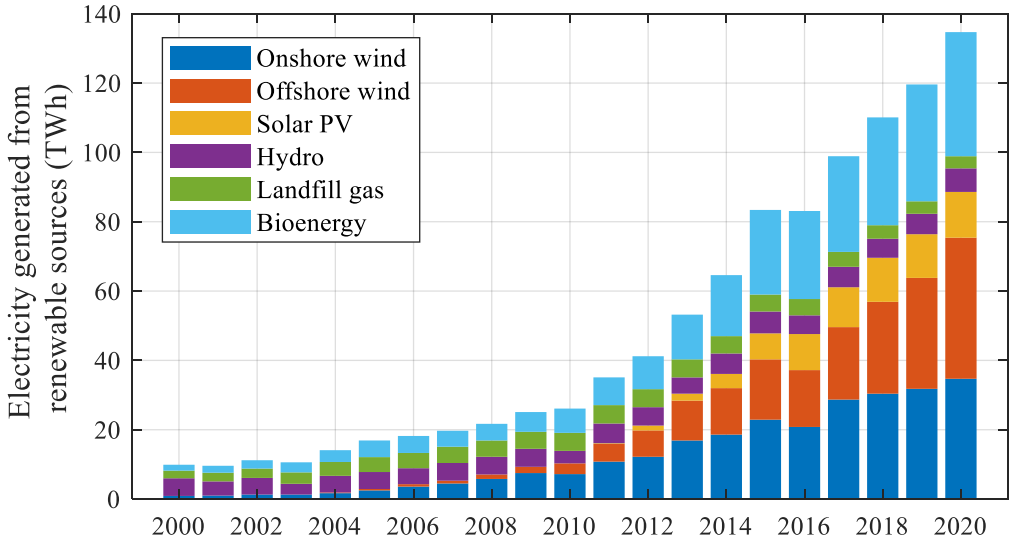


Figure 1.1: Contribution of renewable energy sources to electricity generated.

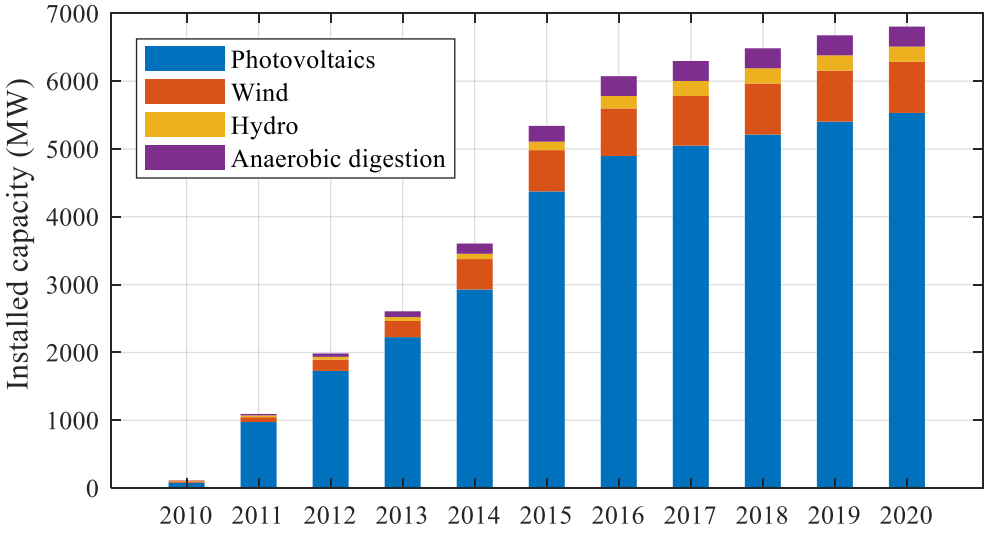


Figure 1.2: Annual installation of micro-generation capacity.

Power electronic inverters are a key component of solar PV systems, and they are used to interface the PV to the grid, extract the maximum power from PV panels, and maintain high quality output. Solar panel efficiency is very low, they can only convert 15% to 22% of solar energy into actual electricity [4]. Therefore, the solar PV inverter should be high efficiency to

reduces the system's power losses. Moreover, power density, cost and reliability are the other key factors to improve the overall system performance. Therefore, power electronics research has focused on developing a PV inverter with high efficiency, power density, reliability, and reduced cost.

The performance of PV inverters has improved in three ways: 1) new inverter topologies have been developed, 2) control methods have advanced, and 3) wide bandgap (WBG)-based semiconductor devices have been used. Furthermore, innovative topologies that provide higher efficiency and reduce the number of components [5] have been developed. Different control methods have been investigated to extract the maximum power from the PV panels [6]. WBG semiconductor devices have superior properties than Silicon (Si)-based semiconductors devices [7] and [8]. However, the design challenges of inverter topologies and the impacts of integration of WBG devices have led to trade-offs being made between the system components. Therefore, there is a clear need to address the design challenges and the impacts of WBG devices in PV inverter topologies.

1.2 Research Objectives

This thesis investigates a Gallium Nitride (GaN)-based single-phase differential inverter for PV applications. Compared to many other PV inverter topologies, the differential inverter can reduce second-order ripple power and leakage current without adding extra active or passive components. Optimal design and control methods were employed to fully utilise the benefits of GaN devices and solve the challenges associated with single-phase inverters. The main objectives of this research are to:

- Investigate the single-phase buck-type differential GaN inverter to understand the trade-off between the power decoupling capacitance, power loss, and power density. In addition, a detailed modelling approach needs to be developed to realise the tendency of performance parameters.
- Design a control scheme to eliminate the second-order ripple using the active power decoupling method. Besides, a systematic approach to be required to select the optimal control parameters.

- Investigate a simple and efficient design method to select the optimal components for the inverter. The optimal design needs to be identified with more accurate and less computation complexity.
- Identify a single-phase differential GaN inverter without increasing the power loss, volume, and cost. Transfer the knowledge of efficient design methods to design the identified final inverter topology.
- Performance of the design, control methods and the inverter topologies need to be ensured by conducting simulation and experimental studies.

1.3 Thesis Outline

Chapter 2: Literature Review

This chapter reviews the existing inverter topologies and identifies their limitations and research gaps. The single-phase inverter topology and the inherent challenges are overviewed. Different types of power decoupling methods are reviewed, and their benefits in solving the second-order ripple problem are discussed. In addition, the WBG-based single-phase inverters are reviewed, and the design challenges are discussed. Then, different design methods are reviewed, and the need for the optimal design method is discussed.

Chapter 3: Design and Control of Single-phase Differential Buck Inverters for Power decoupling

This chapter presents the design and control methods of a GaN-based single-phase inverter. The differential buck-type inverter is used as an example to explore the benefits of active power decoupling functions. A mathematical model is developed for all the active and passive components of the inverter. The Geometric Programming (GP) method is presented to identify the optimal design parameters. The controller's design is then discussed in detail. The design method is implemented in MATLAB, and the trade-offs between efficiency and power density are analysed. The performance of the design method is verified using a 1kW prototype.

Chapter 4: Artificial Intelligence-based Fast and Accurate Design Method for Single-phase Differential Buck Inverters

An Artificial Neural Network (ANN)-based design method is presented to reduce the computational burdens and improve accuracy. The performance and computational time of the ANN-based design method are compared with the numerical model and GP-based design method. The outcome of the design method is experimentally verified by designing a buck-type of differential inverter. Using the experimental setup, the performance of the inverter is evaluated both without and with using a power decoupling controller.

Chapter 5: High-efficiency and High-power Density Design of a Single Stage Buck-boost Differential Inverter

In this chapter, a single-stage buck-boost differential inverter is presented. The operating principle and mathematical modelling of the inverter are explained. An ANN-based optimal design method is used to select the active and passive components. The structure of the controller is presented, and the detailed operation is explained. The inverter design method and the controller are implemented in MATLAB/Simulink. The efficiency, power density and specific cost are examined to verify the performance.

Chapter 6: Experimental Verifications of Buck-boost Differential Inverters

A laboratory prototype is built to verify the experimental performance of the buck-boost inverter. The experiments are conducted in both standalone and grid-connected systems. The results are verified both with and without using the power decoupling function. The efficiency and Total Harmonic Distortion (THD) responses are obtained to validate the effectiveness of the inverter. The benefits of the proposed topology are compared with the existing inverter topologies.

Chapter 7: Conclusions and Future Work

This chapter presents the conclusion and summary of the thesis. Some recommendations for future work are also listed.

1.4 Contributions of the Research Work

The contributions of this thesis are as follows:

- Developed a mathematical model of a single-phase buck-type GaN inverter to understand the trade-off between the power decoupling function, power loss and efficiency. Formulated and implemented a multi-objective design method using GP to select an optimal inverter design while considering the second-order ripple. Design a control scheme for the selected optimal inverter design. Experimentally validated the design method.

- Developed an ANN-based multi-objective design method to reduce the repeated use of mathematical models and computational complexity. Compared the results with existing design methods, such as numerical model and GP method. Verified the accuracy and computational time for different designs. Validated the results with a laboratory prototype.

- Presented a single-stage GaN-based buck-boost inverter to achieve a wide voltage range and power decoupling functions. Developed a multi-objective design approach to optimise the efficiency, power density and component costs. A detailed description of the operation and component selections is presented. The performance is studied using simulation and experimental results. Standalone and grid-connected tests are conducted to verify the inverters performance.

1.5 List of Publications

Journal Papers

a) **R. Rajamony**, S. Wang, R. Navaratne and W. Ming, "Multi-Objective Design of Single-Phase Differential Buck Inverters with Active Power Decoupling," IEEE Open Journal of Power Electronics, vol. 3, pp. 105-114, 2022.
b) **Rajesh Rajomony**, Wenlong Ming, Sheng Wang," Artificial Neural Networks-based Multi-Objective Design Methodology for Wide-bandgap Power Electronics Converters" (To be submitted)

Conference Papers

a) **R. Rajamony**, W. Ming and S. Wang, "Artificial Neural Networks based Multi-Objective Design Approach for Single-phase Inverters," 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), 2020, pp. 409-416.
b) **R. Rajamony** and W. Ming, "Improved Hold-Up Time for WBG-based Single-Phase Converters," 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), 2019, pp. 1-9.

Chapter 2 Literature Review

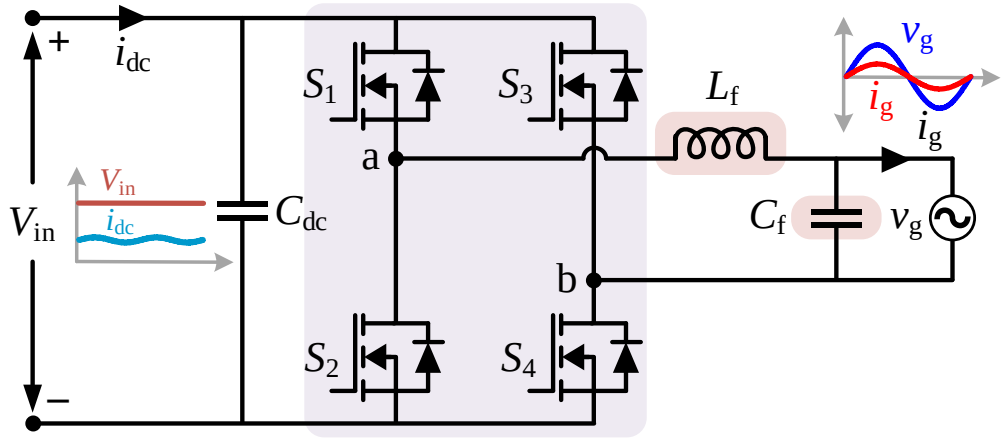
2.1 Introduction

A literature review of single-phase inverter with power decoupling and design methods is presented. The operating principle and the second-order ripple challenges are discussed. The concept of power decoupling functions and different types of active and passive power decoupling methods are presented. The benefits of differential inverters and their second-order ripple elimination capabilities are reviewed. The advantages of WBG devices and the application for power converter design are discussed. Finally, the challenges associated with power converter design and different design methods are reviewed.

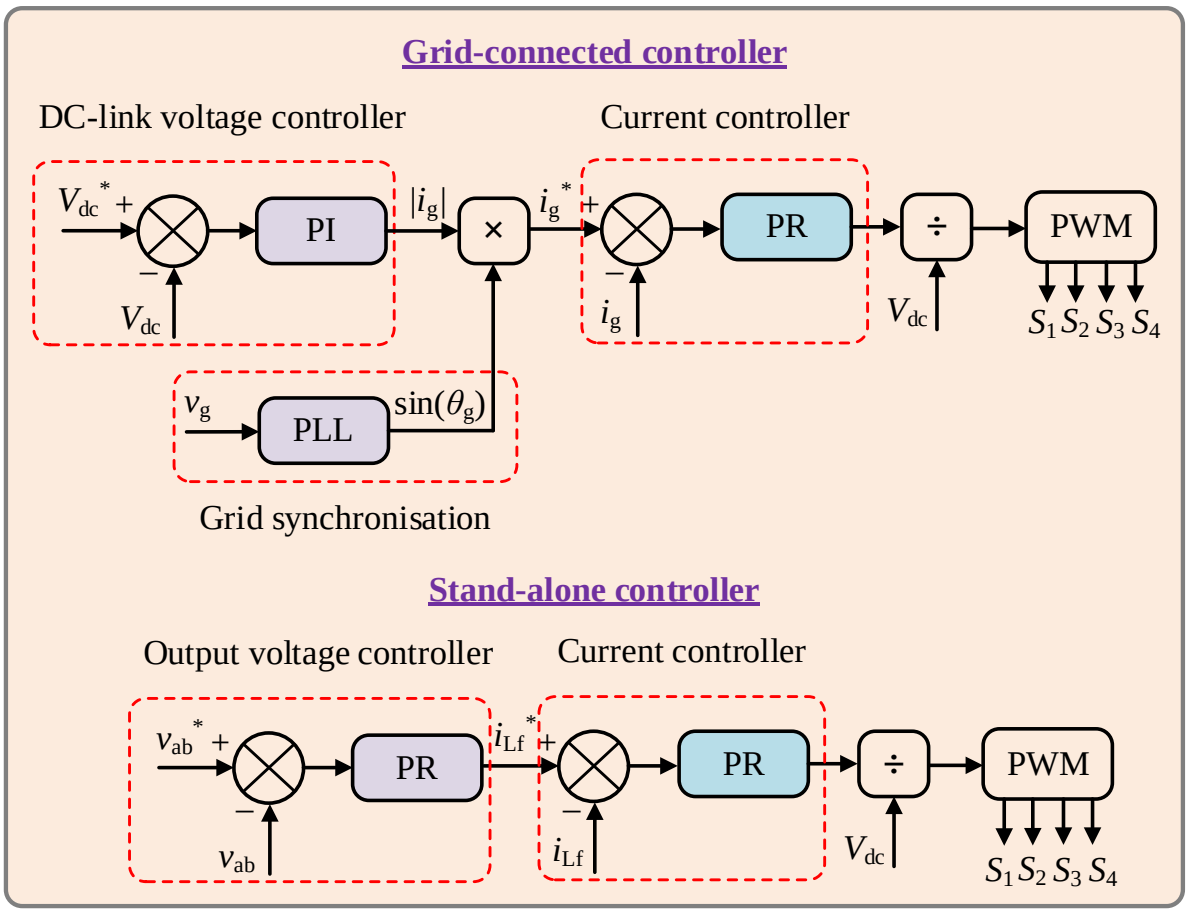
2.2 Single-phase Inverter

Figure 2.1 shows the topology and control scheme of a single-phase inverter [9-11]. This inverter consists of four switches. The switch devices S_1, S_2 and S_3, S_4 are operated in complement to achieve a sinusoidal output voltage. The switches are connected with an anti-parallel diode to protect them from a reverse current, which the switching device turns OFF. The positive cycle of the output voltage is generated when the switches S_1, S_4 are ON, and S_2, S_3 are OFF. Similarly, the negative cycle of the output voltage is generated when the switches S_1, S_4 are OFF, and S_2, S_3 are ON. The output filter inductor L_f and capacitor C_f are used to remove the switching harmonics and produce a pure sinusoidal output voltage.

Two type control schemes can be used: a grid-connected controller [10] and a standalone controller [11]. Figure 2.1 (b) shows the control structure of grid-connected and standalone controllers. These are voltage-current closed loop controllers, which is one of the most popular control schemes. These controllers are developed using the well-known Proportional-



(a)



(b)

Figure 2.1: Conventional single-phase inverter: (a) Topology, and (b) Control scheme.

Integral (PI) and Proportional-Resonant (PR) controllers. When compared to the PI controller, the PR controller with a harmonic compensator can provide good performance in terms of accurate tracking and fast dynamic response. The transfer functions of the PI and PR controllers [12] are represented as,

$$G_{\mathrm{PI}}(s) = k_{\mathrm{P}} + \frac{k_{\mathrm{I}}}{s} \tag{2.1}$$

$$G_{\mathrm{PR}}(s) = k_{\mathrm{P}} + \sum_{r=1,3,5,\ldots} \frac{k_{rh} s}{s^2 + (h\omega_0)^2} \tag{2.2}$$

where k_P is the proportional gain, k_I is the integral gain, k_r is the fundamental resonant control gain, k_{rh} is the control gain for h-order resonant controller and ω_0 is the fundamental frequency. Adding harmonic compensators with appropriate gain can efficiently decrease the harmonics at the corresponding resonant points

2.2.1 Grid-connected Controller

Grid-connected inverters are mainly used for renewable energy applications, such as solar PV systems, wind energy systems, and fuel cells. A grid-connected controller is used to control the inverters for such applications, which consists of a Direct Current (DC) link voltage controller, grid synchronisation and current controller. The DC-link controller is designed by a PI controller to regulate the voltage from a variable DC-source. The output of the DC-link controller is the magnitude of the grid current $|i_{\mathrm{g}}|$. The reference grid current i_{g}^* is generated by multiplying the output of the DC-link controller $|i_{\mathrm{g}}|$ and the output of the Phase-locked loop (PLL) $\sin(\theta_{\mathrm{g}})$. PLL is used to synchronise the phase angle of reference grid current i_{g}^* to the grid voltage v_{g}. The advantages of PLL include the better rejection of grid harmonics, notches, and other kind of disturbances. Hence, the quality of the current injected into the grid can be improved [13]. The current controller is designed based on PR controllers, which has responsibilities for the power quality issues and current protection of the inverter. The harmonics order r is selected based on the need for grid current quality.

2.2.2 Stand-alone Controller

Standalone inverters are mainly used for applications, such as uninterruptible power supply (UPS), and storage systems. The standalone controller is used to control the inverters for these applications. The standalone controller consists of the output voltage controller and current controller. The voltage and current controllers are designed using a PR controller. The voltage controller controls the output voltage v_{ab} of the inverter based on the reference voltage v_{ab}^{*}. Normally, the reference voltage is equal to the grid voltage, and it can be changed in some applications. The output of the voltage controller is the reference current flow through the inductor i_{Lf}^{*}. The current controller is designed by the PR controller, which has the responsibility to protect the current of the inverter. The compensator of the current control is designed based on the need for harmonic elimination.

2.3 DC-link Second-order Ripple

Figure 2.1(a) shows the topology of a single-phase inverter. The output voltage and current of single-phase inverter are given as,

$$v_{\mathrm{g}} = V_{\mathrm{g}} \sin(\omega t) \tag{2.3}$$

$$i_{\mathrm{g}} = I_{\mathrm{g}} \sin(\omega t + \varphi) \tag{2.4}$$

where, V_{g} and I_{g} are the peak values of the grid voltage and injected grid current. ω is the angular frequency and φ is the phase difference between the voltage and current. Generally, the instantaneous power of DC and Alternating Current (AC) sides must be equal. However, the inherently unbalanced nature of single-phase systems causes the ripple power which creates the mismatch between the DC and AC power. To understand this point more clearly, the instantaneous power at the DC side can be written as,

$$p_{\mathrm{dc}} = p_{\mathrm{g}} = v_{\mathrm{g}} i_{\mathrm{g}} \tag{2.3}$$

$$p_{\mathrm{dc}} = V_{\mathrm{g}} \sin(\omega t)\, I_{\mathrm{g}} \sin(\omega t + \varphi)$$

$$= \frac{V_g I_g}{2}(\cos(\omega t - \omega t - \varphi) - \cos(\omega t + \omega t - \varphi))$$

$$p_{dc} = \frac{V_g I_g}{2}\cos\varphi - \frac{V_g I_g}{2}\cos(2\omega t - \varphi)$$

$$P_{const} = \frac{V_g I_g}{2}\cos\varphi \quad \text{and} \quad p_r = -\frac{V_g I_g}{2}\cos(2\omega t - \varphi)$$

$$p_{dc} = P_{const} + p_r \tag{2.4}$$

where, P_{const} is the constant power and p_r is the ripple power. From equation (2.4), the instantaneous DC power consists of constant power P_{const} and ripple power p_r. The frequency of the ripple is twice 2ω the line frequency.

2.3.1 Effects of Second-order Ripple

In solar PV applications, the second-order ripple shifts the operating point from the maximum power point during Maximum Power Point Tracking (MPPT) operations [14–16]. In fuel cells, the second-order ripple causes fuel starvation and stress on the membrane of the fuel cell [17] and [18]. In battery systems, the second-order ripple increases the battery temperature, affecting the electrodes, increasing the voltage/current stress and reducing efficiency [19] and [20]. The second-order ripple can be reduced by choosing an adequate DC-link capacitor. The DC-link capacitance C_{dc} can be calculated [21] as,

$$C_{dc} = \frac{P_{out}}{\omega V_{dc} \Delta V_{dc}} \tag{2.5}$$

where, P_{out} is the output power, V_{dc} is the DC-link voltage and ΔV_{dc} is the peak-to-peak ripple. From equation (2.5), a large value of the DC-link capacitance can reduce the peak-to-peak ripple. Electrolytic capacitors are widely used in the DC-link of single-phase inverters because of their lower cost. However, electrolytic capacitors reduce the efficiency, power density and reliability of the inverter [22] and [23]. Film capacitors can be used instead, which have a much longer lifetime [24]. However, film capacitors cannot directly replace electrolytic capacitors because of their large volume and high cost [25]. Consequently, power

decoupling methods are used to reduce the size of the DC-link capacitance and the effects of second-order ripple [26] and [27].

2.4 Power Decoupling Methods

Figure 2.2 shows the concepts of the power decoupling. The inverter requires constant power P_{const} and eliminates the ripple power p_{r} from the DC-link power p_{dc}. The main objective of the decoupling method is to divert the ripple power p_{r} from the DC-link capacitor into an auxiliary circuit. The auxiliary circuit is developed using active or passive components. Hence, small-sized, and long lifetime film capacitors can be used. The power decoupling method can be categorised into an active decoupling method [28] and a passive decoupling method [29]. In active power decoupling methods, the auxiliary circuit is made using switches, inductors, and capacitors, which needs an additional control method to control the active devices. The passive power decoupling methods use an inductor and capacitors. Based on the configurations of the auxiliary circuit, the power decoupling methods are categorised into series and parallel. Figure 2.3 gives an overview of the series and parallel power decoupling methods. The details of series and power decoupling methods are reviewed in more detail in the following sections.

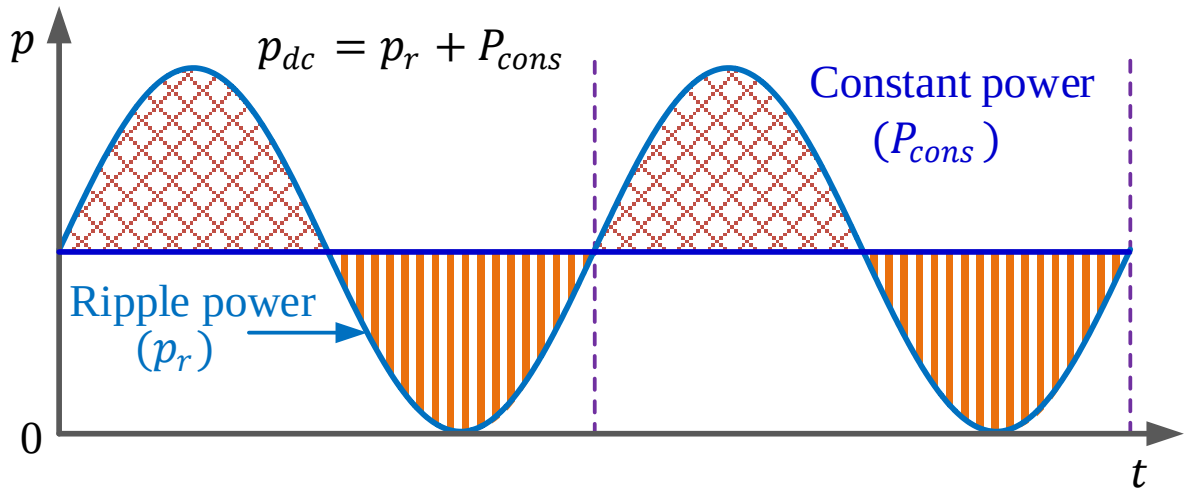


Figure 2.2: Concepts of power decoupling.

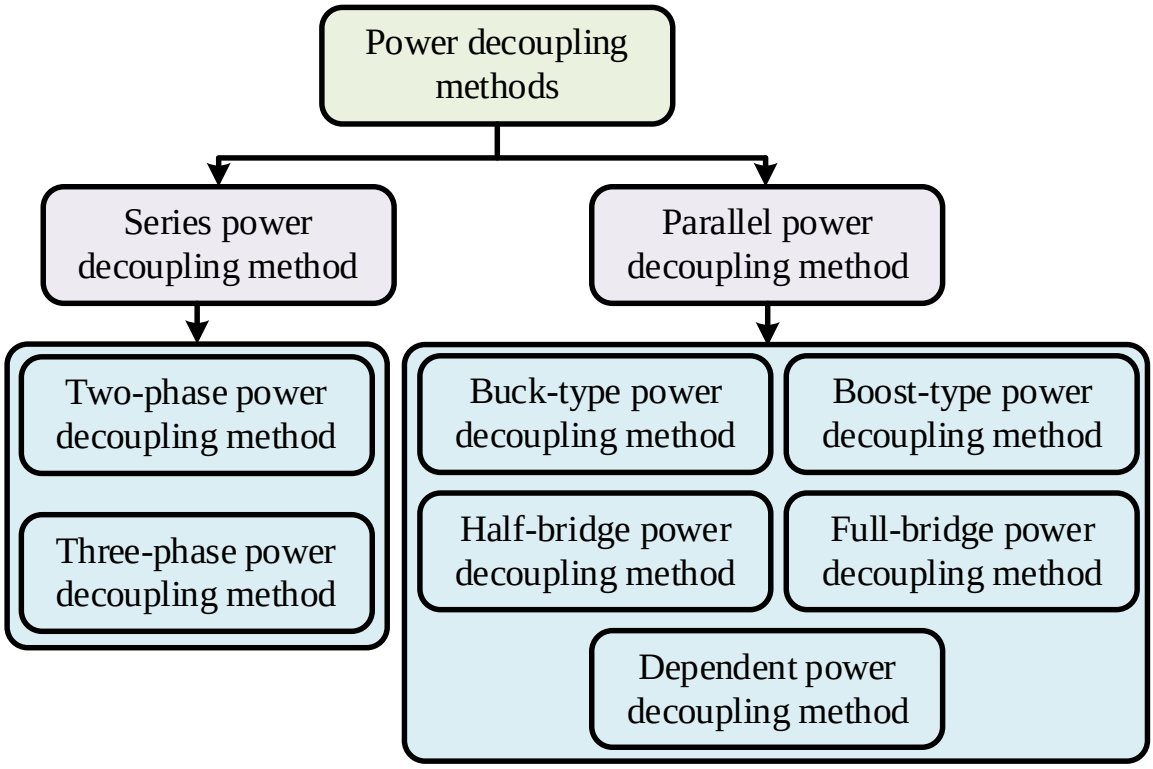


Figure 2.3: Overview of different power decoupling methods.

2.4.1 Series Power Decoupling Methods

Figure 2.4 shows a single-phase inverter with series power decoupling methods. The series power decoupling method is developed by adding active and passive components between the DC-source and inverter. When the DC-link current flows through the power decoupling circuit, the second-order ripple power is diverted into the storage components of the decoupling circuit. To extract the second-order ripple components, the decoupling circuit can be controlled using appropriate control methods. Hence, the current that flows through the inverter will only have the DC-components.

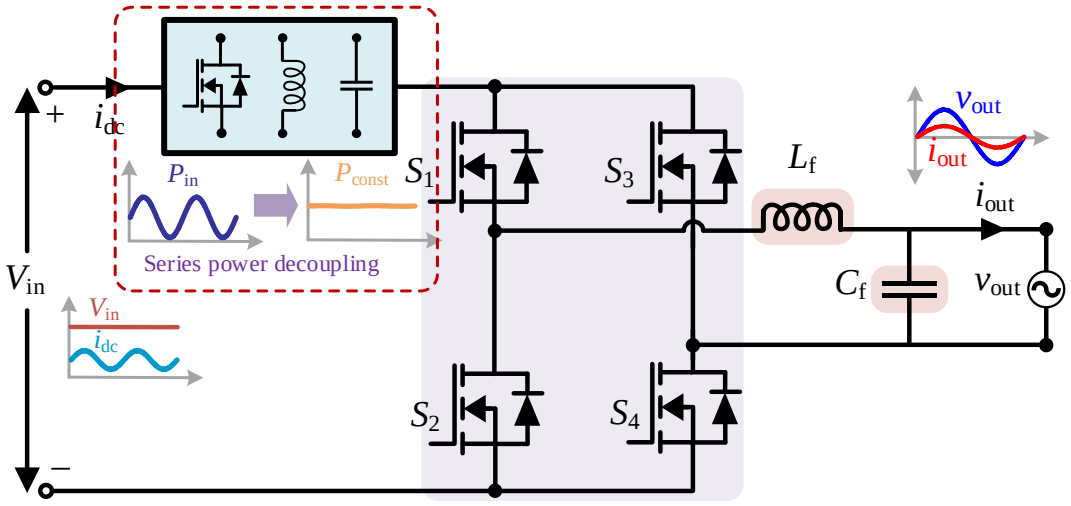


Figure 2.4: Single-phase inverter with series power decoupling.

In [30] and [31], a series power decoupling method has been presented to reduce the DC-link capacitance. The voltage ripple in the DC-link capacitor was compensated by connecting a two-phase series voltage source converter in the DC-bus line. The need for a sizeable DC-link capacitor was reduced using this decoupling method, which allows a long lifetime film capacitor to be used. In [32], the same power decoupling method was used for a grid-tie solar PV inverter to reduce a low voltage ripple. The two-phase method was effective in terms of reducing the second-order ripple. However, the series voltage source converter requires a slightly higher value capacitor to reduce the ripple completely. Therefore, a three-phase power decoupling method was introduced in [21] and [33] to reduce the need for extra capacitors without compensating performance of low ripple elimination. This method can achieve an 89% reduction of the DC-link capacitance.

2.4.2 Parallel Power Decoupling Methods

Figure 2.5 shows a single-phase inverter with parallel power decoupling methods. The parallel power decoupling method is developed by connecting active and passive components across the positive and negative terminal of the DC-bus line. Using appropriate control methods, the second-order ripple power is diverted into the storage components of the decoupling circuit. The current that flows through the inverter will only have the DC-

components, which reduces the losses that are caused by the ripple power. The parallel power coupling methods are configured in different types, such as buck, boost, half-bridge and full-bridge converters.

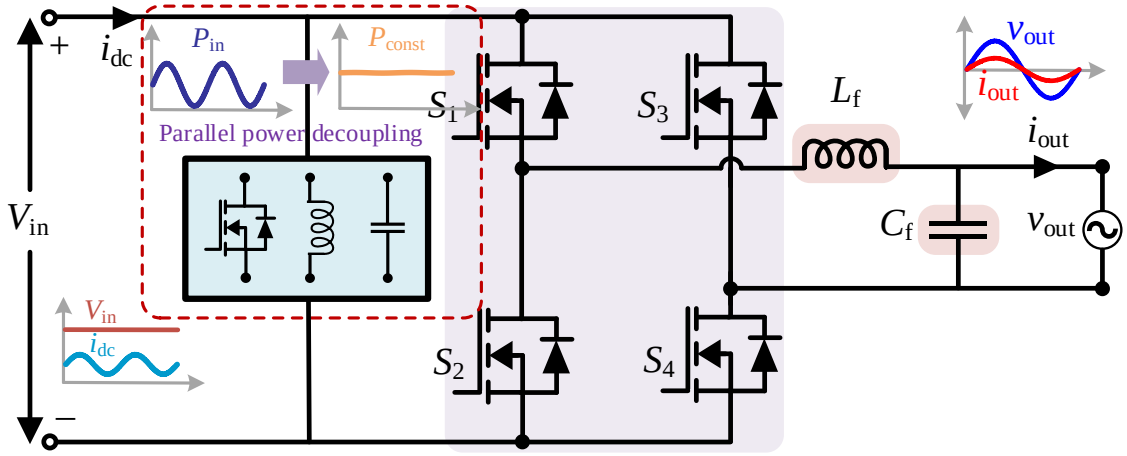


Figure 2.5: Single-phase inverter with parallel power decupling.

Buck Type Power Decoupling

In [34], a bidirectional buck-type DC-DC converter-based active power decoupling method was introduced to reduce the effect of ripple power. The bidirectional active power decoupling circuit was integrated into the DC-bus line of the inverter. In [35], a buck-type active power decoupling method was used in a boost inverter to reduce the effects of low-frequency ripples for fuel-cell applications. In [36] and [37], the same power decoupling method was used in a buck-boost inverter to improve the performance of fuel cells. Using these methods, the need for large DC-link capacitors was prevented, and the performance was verified using simulation and experimental results. The performance of the buck-type active power decoupling method was investigated without using any additional magnetic components for PV applications in [38]. The decoupling method was reduced the second-order ripple on the DC-link current by 90.2% and achieved the maximum efficiency of 96%. In addition, in [39] and [40], the low-frequency oscillation of modular multilevel converter was eliminated using the buck-type power decoupling method. This substantially reduced the submodule voltage ripple and the total capacitance.

Boost Type Power Decoupling

The boost-type active power decoupling method is commonly used to reduce the second-order ripple by injecting continuous compensation current into the DC-link. The decoupling capacitor voltage of this method is relatively high, and hence this decoupling function is suitable for application with lower DC-link voltage. In [41] and [42], a boost-type parallel power decoupling approach was used to enhance the power generation of the PV systems. The elimination of the low-frequency ripple helped to operate the PV module close to the maximum power and enhance the efficiency of these systems. In [24], the control performance of the boost-type decoupling method was investigated using a virtual capacitance controller and DC-link voltage controller. The performance of the controller was evaluated in module integrated PV inverters and low-frequency oscillation was eliminated.

Continuous operation of the boost-type active power decoupling function increases the power loss of PV power conversion systems. To address this problem, in [43] the authors presented a partial power decoupling technique to improve the inverters efficiency over a wide power output range. A detailed power loss model was developed to identify the factors that reduce the system efficiency. The trade-off between the power decoupling functions and the overall efficiency was then studied. This approach was verified through experimental results and the improvement of conversion efficiency was validated.

In [44], a virtual capacitor-based boost-type active low-frequency ripple control method was introduced to build integrated PV applications. Using an integrator compensator, the virtual capacitor concept was added into the control loop. The virtual capacitor-based control method achieved better ripple control over the low frequencies. The component selection of boost-type active power decoupling is more important to achieve high-power density. Therefore, the procedure to select the passive components was investigated in [45] and [46] for a switched boost inverter. Using this method, the low-frequency ripple on the inductor current and the capacitor voltage of the switched boost inverter were reduced.

Buck-boost Type Power Decoupling

The buck- and boost-type active power decoupling methods are only beneficial for applications where the decoupling capacitor voltage is lower or higher than the DC-link voltage. To overcome this limitation, a buck-boost converter-based active power decoupling method was investigated in [47]. Using this method, the average decoupling capacitor voltage was controlled based on the variation of the DC-link voltage. In addition, the low-frequency ripple on the DC-link eliminated the need for total capacitance.

Half-bridge Type Power Decoupling

The half-bridge-based active power decoupling method is used to reduce low-frequency and high-frequency ripples. In [17], the half-bridge-based decoupling method was used to improve the stack efficiency and durability of fuel cells. A symmetrical half-bridge with split capacitor was introduced in [48] and [49] to eliminate the low-frequency oscillation and the need for large passive components. Using this method, a ten times reduction in the total capacitance was achieved and the converter output was regulated using small DC-link capacitors [50].

These active power decoupling methods required additional active and passive components. However, adding more active devices increases the control complexity and the component costs. Therefore, independent active power decoupling methods are widely used to reduce the number of control devices. In [51], a symmetrical half-bridge-based dependent active power decoupling topology was presented that had only used two switches and one small filtering inductor, while DC-link capacitors were used to absorb the ripple power. In [52] and [53], an improved active power decoupling was introduced that used two split capacitors to store the low-frequency ripple. Consequently, the need for active devices is avoided and the current stress of the switches is reduced.

Full-bridge Type Power Decoupling

In [54] and [55], the full-bridge converter-based parallel active power decoupling circuit was introduced to buffer the ripple current and minimise the DC-link capacitance. The full-bridge converter was connected across the DC-bus line. In [56] and [57], a smaller capacitor was connected in series with the full-bridge compensator to reduce the effects of the DC-link

voltage ripple. The full-bridge parallel ripple compensator reduced the volume of the protype by 16% compared to the conventional ripple elimination method, while the efficiency of the inverter was reduced by around 1%. A comparison study of the same full-bridge decoupling compensator was presented in [58] and the results were verified using an experimental study.

Dependent Power Decoupling

The dependent power decoupling method has been formulated using either active or passive components. In [59], an active power decoupling was formed using the one arm of a H-bridge circuit with one additional switch, diode, and an energy storage inductor. The need for a storage inductor of the half-bridge circuit was eliminated by adding two diodes in DC-bus line. The voltage stress of the decoupling circuit was reduced to half that of the DC-link voltage in [60]. A three-phase leg decoupling method was presented in [61–63], which used two additional switches and an auxiliary capacitor to store the ripple energy. In [64–66], another topology was introduced that used only one auxiliary capacitor and no additional switches. The auxiliary capacitor stored the low-frequency ripples, and an independent control scheme was presented to achieve the power decoupling functions. The performance of the decoupling methods was verified using simulation and experimental results.

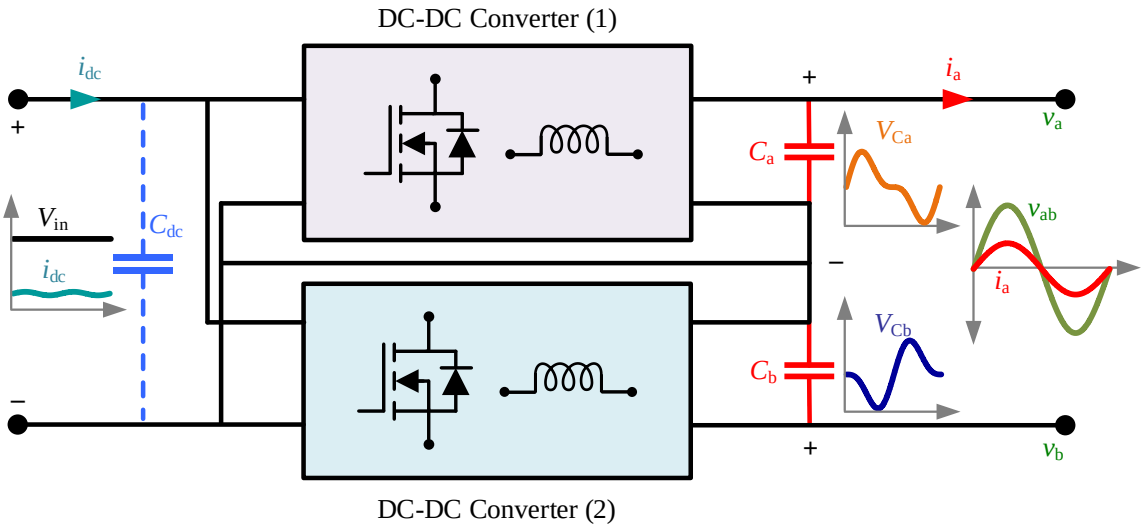
2.4.3 Differential Inverters with Power Decoupling Function

Differential inverters can achieve an active power decoupling function without adding extra active or passive components, which avoids the need for additional control. This has been classified into the buck, boost, or buck-boost inverters, which are developed using two identical DC-DC converters [67]. The output capacitor of the DC-DC converters is used for the power decoupling function. The inductor and capacitor filter the switching frequency, and no dedicated output filter is required to produce a pure sinusoidal output. Figure 2.6 shows the concepts of the power decoupling method in differential inverters, and DC-DC converters are used to develop the differential inverters.

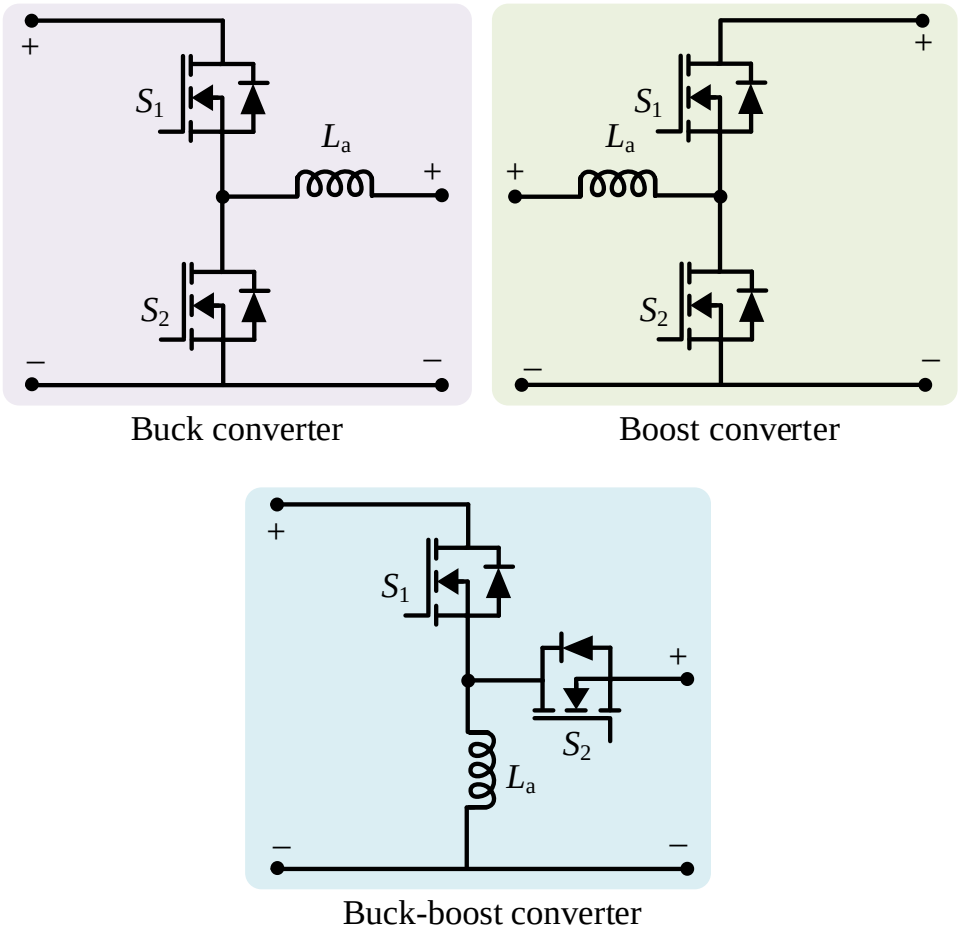
In [29], a buck-type inverter was used to reduce the ripple from the DC-link using a decoupling control method. Consequently, the amplitude of second-order ripple in the DC-link current was reduced by more than seven times. The same inverter was used for grid-

connected PV applications by applying a common-mode conducting loop to reduce the leakage current caused by parasitic capacitance and to minimise the second-order pulsating power. It was confirmed that ground leakage current and the pulsating power problems are solved without adding extra active components [68]. The mismatch of the decoupling capacitors of differential buck inverters was resolved using a comprehensive common-mode control [69].

In [70], a waveform control-based ripple mitigation method was introduced for a boost-type inverter to eliminate the instability in the fuel-cell system. In [71] and [72], the waveform control method was improved using rule-based and feed-back current controllers for boost inverter-based grid-connected battery storage systems. In [73], an energy-based power decoupling control method was introduced for a buck-boost inverter to mitigate the second-order ripple in the input DC current. Consequently, the low-frequency ripple was eliminated. This enables film capacitors to be used instead of electrolytic capacitors. Although the efficiency and power density of the differential inverters are not considered while reducing the size of the decoupling capacitors, in practice they are the essential parameters that need to be considered.



(a)



(b)

Figure 2.6: (a) Concepts of power decoupling method in differential inverters, and (b) Types of DC-DC converters.

Table 2.1 summarises the power decoupling methods. This summary is given based on the types of power decoupling, power rating, number of components used to develop the power decoupling, efficiency, power density and the method's features. Series power decoupling can be achieved in two ways: two-phase and three-phase methods. Many additional components are required to develop series power decoupling. Meanwhile, parallel decoupling methods have many different configurations. Among them, buck and full-bridge type decoupling methods are more efficient when compared to the other methods. In addition, the dependent decoupling methods minimised the number of active components. However, this

method also requires passive components. The use of additional components reduces the efficiency and power density of the overall system. In contrast, differential inverters do not require any additional components to achieve active power decoupling. Therefore, a differential inverter is a good option for a single-phase inverter with power decoupling functions.

Table 2.1: Summary of the power decoupling methods

Decoupling method	Reference	Power rating	Additional components		Efficiency	Volume	Features
			Active	Passive			
Two-phase power decoupling	[30]	600W	4 Switches	2 Inductors 2 Capacitors	-	-	-Independent operation -Additional control required -No impact on the DC-link voltage
	[31]	3kW			-	-	
	[32]	2kW			-	-	
Three-phase power decoupling	[33]	2kW		2 Inductors 2 Capacitors	95%	-	
	[21]	2kW	6 Switches		95%	0.6 dm^3	
Buck type power decoupling	[34]	15kW	2 Switches	1 Inductor 1 Capacitor	93.2%	11.4 dm^3	-Independent operation -Additional control required -Good option for high power rating
	[35]	1kW			82%	-	
	[36]	1.2kW			-	-	
	[37]	1.2kW			88%	-	
	[38]	1kW			96%	0.42 dm^3	
	[39]	1kW			97.13%	19.6 dm^3	
	[40]	5kW			-	-	
Boost type power decoupling	[41]	110 W	2 Switches	1 Inductor 1 Capacitor	-	-	-Independent operation -Additional control required -Good option for high power rating -Higher voltage stress on power decoupling
	[42]	110 W			90.5%	-	
	[24]	4kW			97.4%	-	
	[43]	1kW			93.25%	-	
	[44]	2kW			-	-	
	[45]	-			-	-	
	[46]	250W			91.8%	-	
Buck-boost type power decoupling	[47]	1kW	2 Switches	1 Inductor 1 Capacitor	-	-	-Flexible control of decoupling capacitor voltage
	[17]	5kW	2 Switches	1 Inductor	92.4%	-	-Independent operation -Additional control
	[48]	1kW			-	-	

Half-bridge type power decoupling	[49]	1kW	2 Switches	2 Capacitors	-	-	required -Two energy storage capacitors are used for active power decoupling -Good option for high power rating
	[50]	1.5kW			-	-	
	[51]	1kW		1 Inductor 2 Capacitors	95.8%	-	
	[52]	1kW	-	1 Inductor	95%	-	
	[53]	1kW		2 Capacitors	96%	-	
Full-bridge type power decoupling	[55]	600 W	4 Switches	1 Inductor 1 Capacitor	-	-	-Independent operation -Additional control required -Good option for high power rating
	[56]	-	4 Switches	2 Inductors	-	-	
	[57]	2kW		2 Capacitors	94%	0.5 dm^3	
	[58]	2 kW	4 Switches	1 Inductor 2 Capacitors	98.9%	-	
Dependent decoupling	[59]	200W	1 Switch 1 Diode	1 Inductor	-	-	
	[60]	1kW	2 Switches 2 Diodes	2 Capacitors	-	-	-Dependent operation -Additional control not required -Good option for high power rating
	[61]	4kW	2 Switches	1 Capacitor	-	-	
	[63]	-	2 Switches	1 Inductor 1 Capacitor	92.7%	-	
	[64]	-			-	-	
	[65]	1kW	-	1 Capacitor	91.5%	-	
	[66]	540W			94%	-	
Differential inverter type power decoupling	[29]	1kW	-	-	92.5%	-	-Dependent operation -Additional control not required - Additional components are not required -Good option for high power rating
	[68]	500W			96%	-	
	[69]	800W			-	-	
	[70]	170W			84%	-	
	[71]	20W			-	-	
	[72]	20W			-	-	
	[73]	400W			88%	-	

2.5 WBG Devices in Power Electronics

The power decoupling method of a single-phase inverter always has a trade-off between efficiency and power density. The benefits of WBG devices are enabling to improve the efficiency and power density by reducing the power loss and volume of the inverter. WBG

devices, such as Silicon Carbide (SiC) and GaN, have superior electrical properties for power electronics than conventional Si (as shown in Figure 2.7). The electrical properties have been characterised by the electric field, energy gap, electron velocity, electron mobility, and thermal conductivity [74]. These electric properties enable the WBG devices to operate at high voltage, high temperature, and high switching frequency.

Power switches based on WBG semiconductors have better switching and conduction performance over a wide range of temperatures than Si-based devices. For instance, they have faster switching speed, lower switching losses, higher breakdown voltages and higher operating temperatures. Therefore, WBG devices are considered to be promising solutions for high-efficient power electronic converter designs. In single-phase inverters, the WBG devices SiC and GaN provide a performance improvement over Si under wide load, temperature and switching frequency conditions. When comparing the switching performance of the three technologies, the GaN device has the best performance and provides high efficiency at high-frequency applications [75].

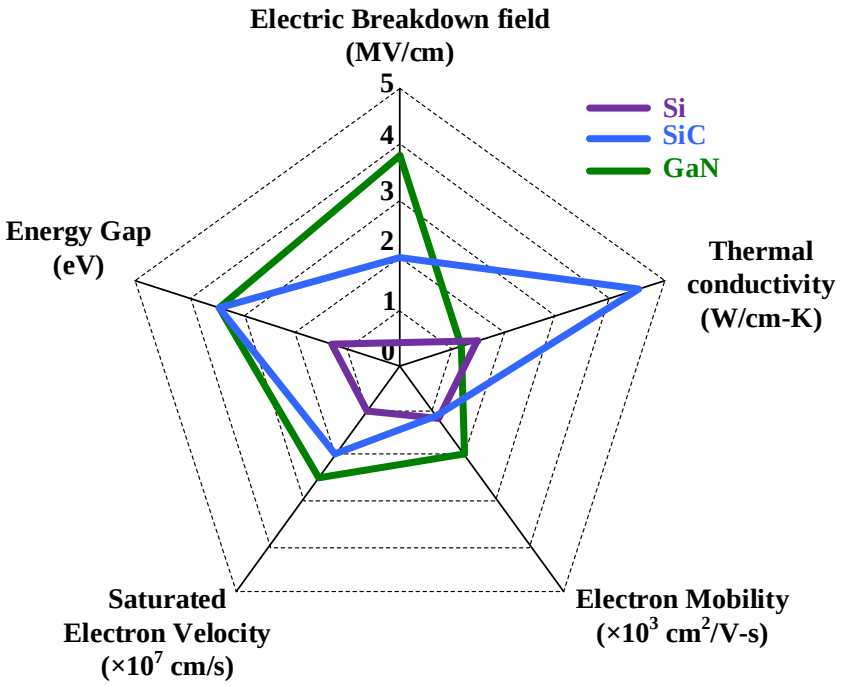


Figure 2.7: Comparison of Si, SiC and GaN semiconductors properties.

2.5.1 SiC-based Single-phase Inverters

The advantages of SiC devices were explored in [76] using a doubly grounded single-phase inverter topology with active power decoupling method. The inverter and power decoupling circuit were developed using the C2M0080120D and C2D05120A SiC devices. The inverter was operated at a 100kHz switching frequency, which improved the efficiency 95.8%. In [21], a series and parallel combination of power decoupling method was presented for a 2kW SiC inverter. The efficiency and power density were achieved as 96% and 55W/in^3. In [77], a T-type common grounded transformer-less 1kVA single phase inverter was developed using C2M0040120D SiC MOSFETs. The peak efficiency of 98.2% was achieved at switching frequency 50kHz. In [78], a 100W single-phase inverter was designed using C2M0080120D SiC MOSFETs with an efficiency of 94.4%. A 1kW single-phase grid-connected inverter was presented in [79] using SiC MOSFETs with an efficiency of 95.4%. In [80], an industrial design approach was presented for a SiC-based single-phase inverter. The design was focused on the objectives of Google Little Box Challenge. The experiment was performed for 2kVA inverter design, which enhanced the efficiency and power density of 97.7% and 100 W/in^3. In [81], a practical design approach was presented for a 2kVA SiC-based single-phase inverter, which enhanced the efficiency and power density of 98.3% and 58 W/in^3. The SiC-based inverters provided performance enhancement under different temperature and switching frequency conditions. In terms of switching performance, the inverter design can be improved using GaN devices, which allows high efficiency in high-frequency applications [75].

2.5.2 GaN-based Single-phase Inverters

This section will review GaN-based single-phase inverters, and the improvement in efficiency and power density by employing the GaN devices. In [82] and [83], the benefits of GaN devices were investigated using a single-phase inverter with the H-bridge active power decoupling method. The inverter and power decoupling circuit were developed using the EPC2033 and EPC2016C GaN devices. The inverter was operated at a 120kHz switching frequency, which improved the efficiency and power density to 97.6% and 216W/in^3. The same parallel H-bridge active power decoupling was validated using a 5kW EPC9203 GaN inverter [84]. In [85], a doubly grounded GaN-based single-phase inverter was introduced to

eliminate the common-mode leakage current and the second-order ripple power. This inverter was developed using the GS66516T GaN device and operated at 100kHz switching frequency. The inverter was tested at 1kW power rating, and an efficiency of 95.1% was achieved.

The buck-boost type active power decoupling method was developed using EPC2034 GaN devices for residential PV microinverters [86]. The double-line frequency ripple power of a quasi-Z-source PV inverter was eliminated using a ripple suppression control method. The inverter was developed using TPH3006PS GaN devices and it was operated at 100kHz switching frequency to improve the efficiency [87]. In [88] and [89], the performance of three-phase dependent active power decoupling methods was studied using a GS66508P GaN-based 2kW single-phase inverter. The efficiency and power density were improved to 98% and 55.8W/in^3. A GS66508T GaN-based 2kW single-phase inverter design was developed for the Google Little Box Challenge and operated at 100kHz switching frequency. The efficiency and power density were improved to 96.9% and 102W/in^3 [90]. The power loss model of the GaN-based single-phase inverter was developed to improve the design efficiency. The model was validated by developing a 4.5kW inverter design using the IGOT60R070D1 GaN device [91]. However, the trade-off between the components limits the performance of the GaN device. In [92], a trade-off study was performed between the output filter and heatsink to reduce the volume of the inverter. The study was validated using a 1.6kW design, and the inverter volume was reduced 1.16 times of the actual design.

The switching losses limited the advantage of operating the GaN devices at high switching frequency. Therefore, the triangular current mode control method was introduced in [93], and the performance was validated using GS66516T GaN device. Using this method, the inverter was operated at 300kHz switching frequency, achieved 98.1% efficiency and it improved the power density to 151W/in^3 for a 2.4kW design. In [94] and [95], a hybrid triangular current mode control method was introduced to increase the switching frequency without affecting the efficiency and power density. The hybrid control method was evaluated in a 1kW GS66502B GaN device-based buck-type differential inverter. The efficiency and power density were improved to 98% and 135W/in^3. For a grid-connected GaN-based PV inverter, the harmonics of the injected grid current is one of the main concerns when it operates at a

high switching frequency. A feed-forward discontinuous current mode control scheme was introduced in [96], which reduced the THD from 7.3% to 4.5%.

In [97], a high step-up single-phase inverter with active power decoupling was introduced for PV applications. The PV output voltage is step-upped using a high gain boost converter to match the DC-link voltage. Two DC-link capacitors were used to share the double-link frequency, and therefore the need for sizeable DC-link capacitance was avoided. A 300W hardware prototype was developed using GS66508T GaN devices and operated at a switching frequency of 100 kHz. A 97.45% peak efficiency was achieved, and the overall system's efficiency achieved 94.43%. In [98], a single-stage cascade buck-boost PV inverter was introduced to improve the overall system efficiency and power density. A 2kW prototype was developed using a GS66508P GaN device, which improved the efficiency and power density to 97.8% and 5.8 W/in^3.

2.6 Design Methods of Power Electronic Inverters

The power decoupling methods discussed in Section 2.4 mainly focused on the reduction of total capacitance, which becomes a trade-off between the efficiency and power density of the inverter. In addition, most of the power decoupling methods only aim to improve the efficiency (Table 2.1). GaN-based design can achieve high efficiency and power density (Section 2.5.1). However, using GaN devices cannot directly give higher efficiency or power density because the performance of the device depends on several factors, such as switching frequency, and operating temperature.

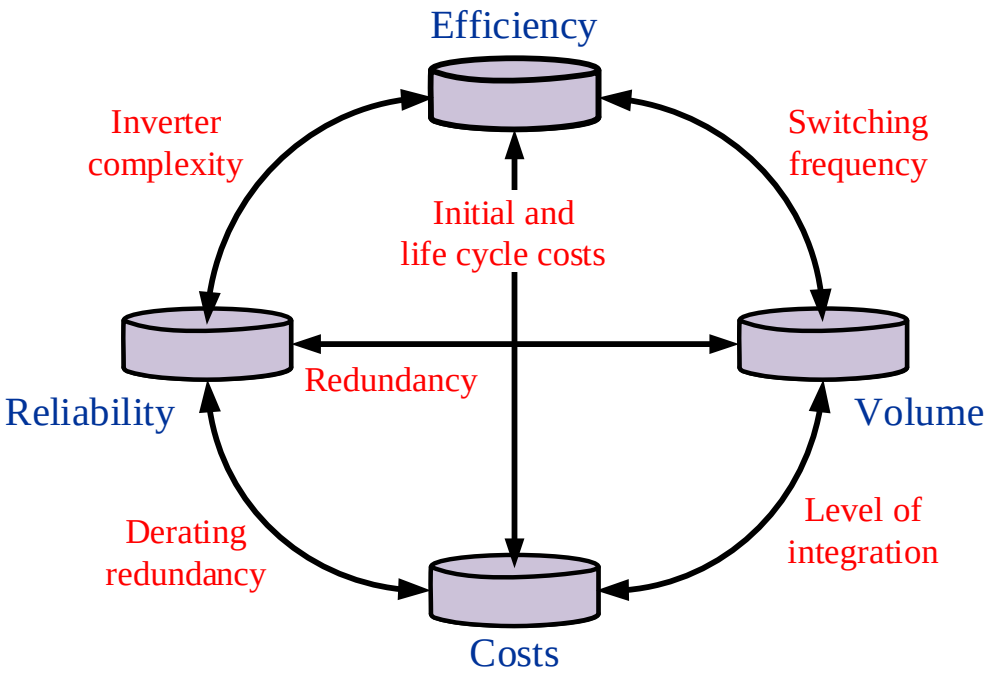


Figure 2.8: Trade-off between the performance parameters.

A well-designed power electronic inverter should have high efficiency, small volume and light weight, low cost, and low failure rate. However, the challenge is to balance these performance measures. Typical technical performance measures are efficiency, volume, cost, and reliability (as depicted in Figure 2.8). For example, a design that only focuses on achieving higher efficiency impacts the power density, reliability, and cost. These measures are mainly determined by the design of converter, including selections of topology, modulation scheme, components, and layout. By carefully designing the converter, it can have high-power density, reduced volume, weight, and cost. Therefore, the design method needs to select the optimal design parameters to improve performance. Figure 2.9 shows the design methods of power electronic converters. The design methods are broadly classified into conventional methods, optimisation methods and AI-based methods.

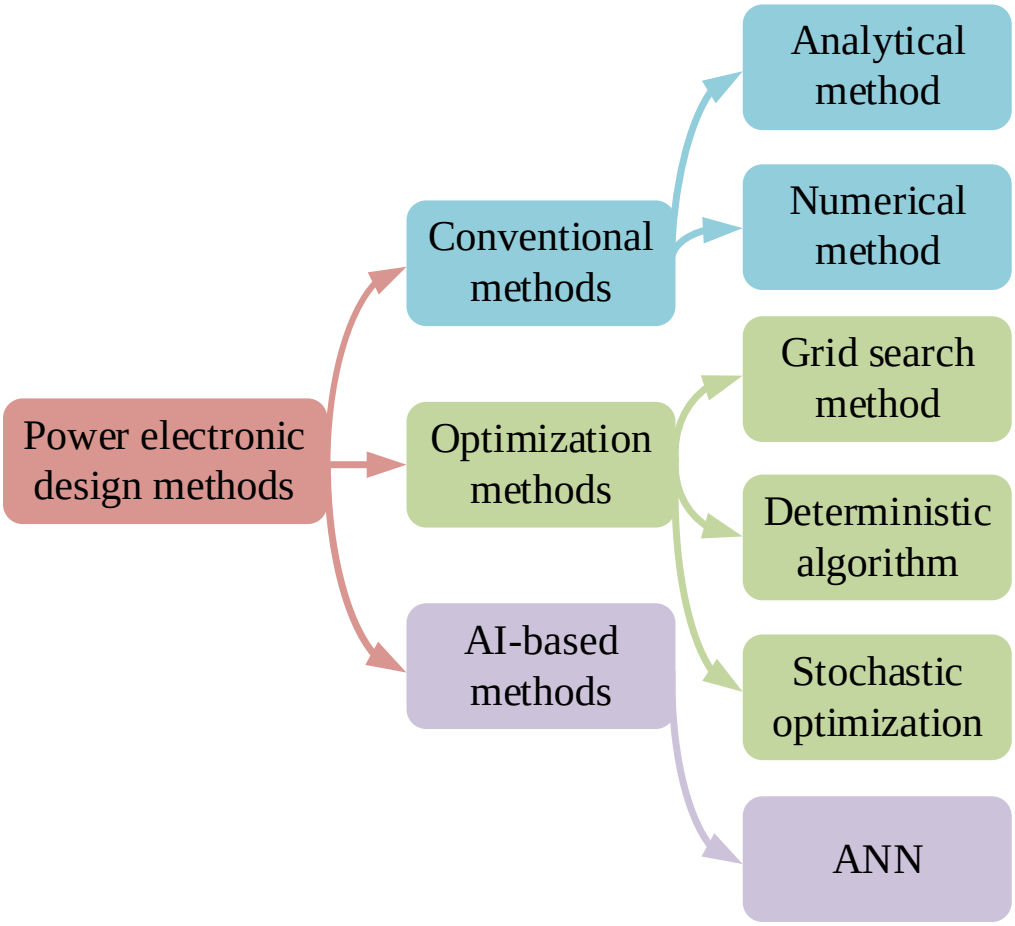


Figure 2.9: Design method of power electronic converters.

2.6.1 Conventional Methods

Analytical Method

The analytical method is based on the analytical equation of the power converter. The power loss model of the semiconductor was developed in [99] to evaluate the efficiency of the inverter for motor applications. In [100], the analytical modelling approach optimised the power density of a single-phase dual active bridge for aircraft application. This model was developed based on the switching frequency and leakage inductance, which was minimised to total loss and the volume of the design. In [101], the analytical model of power loss and the thermal models of the inverter was developed for electric vehicle drivetrains. Although

analytical models are simple to develop, their accuracy is lower compared to the final prototype.

Numerical Method

Numerical methods are based on the analytical equations and use interactive functions to choose the solutions. In [102], sequential unconstrained minimisation and the augmented Lagrangian penalty function methods were introduced to optimise a cost-effective design for a switching regulator. The same method was extended to minimise the weight and volume of a half-bridge DC-DC power converter [103] and [104]. In [105] and [106], multiple design parameters (e.g., switching frequency, ripple and change of temperature) are used to maximise the efficiency of buck and buck-boost converters. From these works, the converter design can be optimised for the desired performance as long as the design parameters are bounded. Moreover, if the number of iterations is lower, then the computation can be completed without converging to the solutions, which reduces the efficacy of the designs.

2.6.2 Optimisation Methods

Grid Search Method

In the grid search method, the combination of design parameters is mapped onto the performance parameters of the converter. A multi-objective design method was introduced to identify the rectifier's Pareto-front of efficiency and power density [107]. The simulation results of the search method were verified using a laboratory prototype, which ensured high efficiency and power density design. In [108], an optimisation method achieved 99% efficiency for a 5kW DC-DC converter design. An optimisation tool was presented in [109] to maximise the power density of an inverter. In addition, a design methodology was presented to optimise the losses associated with the medium frequency transformer [110]. However, while these methods are relatively simple, the number of design parameters is exponential with the number of variables.

Deterministic Algorithm

The deterministic algorithm computes the mathematical functions of the design and performance parameters of the optimisation problems. The mathematical function produces the output for a given objective [111]. In [112], a GP-based optimisation approach was presented to optimise the power loss and volume of the inductors. A simplex modelling approach was presented in [113] to optimise the components of a Cuk converter. The efficiency and power density of a DC-DC converter was optimised using the GP method and polynomial functions [114] and [115]. Although these algorithms converge to the optimal solutions, additional constraints are required, and this increases complexity.

Stochastic Optimisation

The stochastic optimisation methods are based on mathematical functions with random variables. A genetic algorithm (GA) based constrained optimisation framework was presented to understand the trade-offs involved in the flyback converter design [116]. A multi-objective optimisation approach was presented in [117] to minimise the power loss and cost of the PV systems. In [118], particle swarm optimisation (PSO) method was presented to minimise the power loss of a DC-DC converter. The complexity of the optimisation methods is higher due to large number of constraints and iterations. In addition, the optimal solutions can be diverged due to the random variables.

2.6.3 AI-based Methods

Artificial Intelligence (AI) methods have been used to compute the optimal design of power converter. An ANN-based design method has been introduced to develop the reliability model for the single-phase inverters. The reliability model is developed by considering the switches and ac filters of the systems. This method is highly accurate, requires less computational time, and has improved competence [119]. The potential of an ANN-based design was used to model and optimise the inductor of the DC-DC converter [120]. The ANN-based method improved the accuracy and reduced the computation time.

2.7 Summary

This chapter has presented a detailed review of single-phase inverters with power decoupling function and the design methods. Conventional single-phase inverters are popularly used for grid-connected and standalone renewable energy applications. However, a conventional inverter requires a large DC-link capacitor to store the inherent second-ripple power. Therefore, active power decoupling methods were introduced to reduce the need for sizeable DC-link capacitance. Most of the decoupling methods were developed using additional active and passive components, which require different control schemes. Differential inverters eliminate the DC-link ripple power without using additional components. Nevertheless, these methods only focus on improving efficiency, which reduces the power density.

WBG devices improve the inverters efficiency and power density. The GaN-based power decoupling methods are designed using direct approaches, which limits the full utilisation of the design freedom. Meanwhile, systematic design approaches can identify the optimal design of power electronic converters. The conventional and optimisation design methods required more information and computational time. In contrast, ANN-based design methods find the optimal design with less computational time and with better accuracy. However, the system-level design was not studied using ANN-based methods.

Chapter 3 Design and Control of Single-phase Differential Buck Inverters for Power Decoupling

3.1 Introduction

The design of single-phase differential buck inverters has two important considerations, including reducing second-order ripple power using decoupling capacitors and increasing inverter performances. Using larger decoupling capacitors will improve the performance of ripple power reduction and efficiency while reducing power density. The previous literature has often aimed to reduce the total capacitance as much as possible, which leads to reduced volume. However, a smaller decoupling capacitor will increase the second-order ripple circulating current, which reduces the inverters efficiency because decoupling capacitance and efficiency are mutually coupled. Such trade-off has not been fully modelled and investigated, leading to the sub-optimal design of inverters. To address that,

- A mathematical model of power loss and volume of each component within the inverter is developed in Section 3.2. A trade-off analysis of all the active and passive components of the inverter is studied through detailed modelling.
- Section 3.3 will conduct an in-depth analysis of the relationship between the efficiency and power density of the decoupling capacitor. GaN field-effect transistors (FETs) are adopted within the design approach to ensure the high efficiency and high power density of the designed inverters.
- Then, a multi-objective optimisation method based on GP is proposed in Section 3.4 to optimise the efficiency and power density. The proposed design approach is based on

detailed modelling of power loss and volume by considering the dominant inverter design parameters.

- ❖ The design of voltage, current and second-order controllers is discussed in Section 3.5.
- ❖ Section 3.6.1 will discuss how the outcome of the design approach can be used for the optimal selection of decoupling capacitors associated with other components, including inductors, heatsinks, and power switches.
- ❖ A laboratory prototype is developed in Section 3.6.2 to verify the effectiveness of the proposed design approach.

3.2 Modelling of Power Loss and Volume of the Buck Inverter

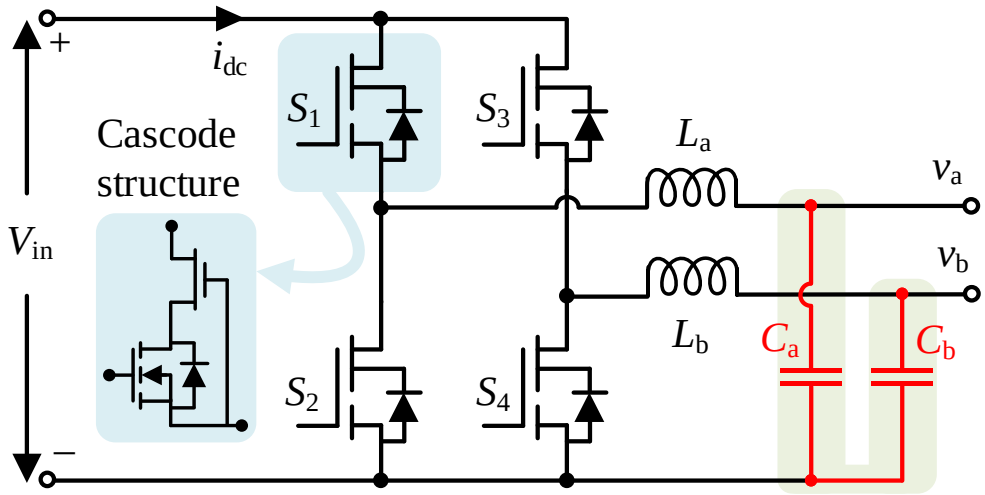


Figure 3.1: Single-phase differential buck inverter with power decoupling function.

The detailed modelling of the differential buck inverter topology is presented (see Figure 3.1). A mathematical model is essential to explore the efficiency and power density of the inverters. In general, the models of power electronics components include different design variables. For example, the switching loss of a power switch depends on a design variable switching frequency. This component-level model will only give the power loss of an individual component. Although the total losses can be calculated by aggregating the

individual component-level losses, this will reduce the efficacy of the modelling approach. Therefore, an accurate system-level modelling approach is required, which needs to consider all of the design variables.

The detailed system-level power loss and volume model of each component are derived based on the active power decoupling approach. From this, the efficiency and power density are further determined. The design variables including switching frequency f_{sw} the inductor ripple Δi_{L}, the switch area A_{sw}, and the junction temperature ΔT_{j} are used to calculate the power loss and volume. The major components are considered, including power GaN FETs, inductors, capacitors, and heat sinks.

3.2.1 Power GaN FET

The power loss models of the GaN FET are derived based on the on-state resistance $R_{\mathrm{DS,on}}$, the output capacitance C_{oss}, and the thermal junction-to-case resistance $R_{\mathrm{\theta JC}}$ of the switches. These variables are scaled by their reference values with respect to the area of the switch. The switching losses of the inverter are the sum of the turn-on and turn-off loss of all of the switches [121]. The switching losses of the higher side switch $P_{\mathrm{S_H,sw}}(\mathrm{H}=1,3)$ (see Figure 1) are obtained as follows,

$$\begin{aligned} P_{S_{\mathrm{H}},\mathrm{sw}} = \frac{V_{\mathrm{in}} f_{\mathrm{sw}}}{2}\Bigg\{&\left(I_{\mathrm{out}}\sin(\omega t) + i_{\mathrm{comp}} - \frac{\triangle\, i_{\mathrm{L_a}}}{2}\right)(t_{\mathrm{CR}} + t_{\mathrm{VF}}) \\ &+ \left(I_{\mathrm{out}}\sin(\omega t) + i_{\mathrm{comp}} + \frac{\triangle\, i_{\mathrm{L_a}}}{2}\right)(t_{\mathrm{VR}} + t_{\mathrm{CF}})\Bigg\} \end{aligned} \tag{3.1}$$

where i_{comp} is the second-order current component and $\Delta i_{\mathrm{L_a}}$ is the inductor current ripple. t_{CR} and t_{CF} are the rise and fall times for the current in the switch. t_{VR} and t_{VF} are the rise and fall times for the voltage in the switch.

The switching loss of the lower side switches S_2 and S_4 is lower because it is based on the diode voltage drop V_{SD}. The switching losses of the lower side switch $P_{\mathrm{S_L,sw}}(\mathrm{L}=2,4)$ can be derived as follows,

$$P_{S_{\mathrm{L}},\mathrm{sw}} = \frac{V_{\mathrm{SD}} f_{\mathrm{sw}}}{2}\left\{\left(I_{\mathrm{out}}\sin(\omega t) + i_{\mathrm{comp}} + \frac{\triangle\, i_{\mathrm{L_a}}}{2}\right)(t_{\mathrm{CR}} + t_{\mathrm{VF}}) + \left(I_{\mathrm{out}}\sin(\omega t) + i_{\mathrm{comp}} - \frac{\triangle\, i_{\mathrm{L_a}}}{2}\right)(t_{\mathrm{VR}} + t_{\mathrm{CF}})\right\} \tag{3.2}$$

From equation (3.1) and (3.2), the total switching losses $P_{\mathrm{tot,sw}}$ of the inverter can be calculated as the sum of $P_{S_{\mathrm{H}},\mathrm{sw}}$ and $P_{S_{\mathrm{L}},\mathrm{sw}}$.

The conduction loss depends on the Root Mean Square (RMS) current flowing through the switch $I_{\mathrm{RMS,sw}}$, the on-state resistance $R_{\mathrm{DS,on}}$ and the change in junction temperature ΔT_{j}. It will vary according to the duty cycle of the switches $S_1 - S_4$. After applying the mathematical simplifications, the total conduction loss $P_{\mathrm{tot,cond}}$ can be written as,

$$P_{\mathrm{tot,cond}} = \left(\frac{R^*_{\mathrm{DS,on}} A^*_{\mathrm{sw}}}{A_{\mathrm{sw}}}\right)(1 + \triangle\, T_{\mathrm{j}})\left\{\left(I^2_{\mathrm{out}}\sin^2(\omega t) + i^2_{\mathrm{comp}} + \frac{\triangle i^2_{\mathrm{L_a}}}{12}\right) + \left(I^2_{\mathrm{out}}\sin^2(\omega t + \pi) + i^2_{\mathrm{comp}} + \frac{\triangle i^2_{\mathrm{L_b}}}{12}\right)\right\} \tag{3.3}$$

The power losses of the output capacitance C_{oss}, depend on the input voltage and the switching frequency, which can be expressed as,

$$P_{\mathrm{tot,C_{oss}}} = 2\left(\frac{C^*_{\mathrm{oss}} A_{\mathrm{sw}}}{A^*_{\mathrm{sw}}}\right) V^2_{\mathrm{in}} f_{\mathrm{sw}} \tag{3.4}$$

The reverse recovery loss of the lower side switches is not negligible for cascode devices. The total reverse recovery loss $P_{\mathrm{tot,rr}}$ is calculated as,

$$P_{\mathrm{tot,rr}} = 2\left(\frac{Q^*_{\mathrm{rr}} A_{\mathrm{sw}}}{A^*_{\mathrm{sw}}}\right) V_{\mathrm{in}} f_{\mathrm{sw}} \tag{3.5}$$

The gate losses depend on the switching frequency, the gate-source voltage V_{GS} and the gate charge Q_{g}. The total gate loss of four switches $P_{\mathrm{tot,g}}$ is calculated as,

$$P_{\mathrm{tot,g}} = 4\left(\frac{Q^*_{\mathrm{g}} A_{\mathrm{sw}}}{A^*_{\mathrm{sw}}}\right) V_{\mathrm{GS}} f_{\mathrm{sw}} \tag{3.6}$$

In cascode GaN FETs, the body diode of the lower side switches incurs a conduction loss during the reverse recovery time t_{rr} [121]. The total power loss $P_{tot,bd}$ of the body diodes can be written as,

$$P_{tot,bd} = 2V_{SD}f_{sw}t_{rr}\left(I_{out}(\sin(\omega t) + \sin(\omega t + \pi)) + 2i_{comp}\right) \tag{3.7}$$

The volume of the switches can be calculated as,

$$vol_{sw} = 4h_{sw}A_{sw} \tag{3.8}$$

where h_{sw} is the height of the switch package.

3.2.2 Output Inductors

The inductor power losses consist of the core losses, the AC and DC losses. The AC and DC losses occurred due to the harmonics and the ripple current. The inductor power losses can be expressed as [122],

$$P_{ind} = a_{L1}f_{sw}^{\alpha} \triangle i_L^{\beta} + a_{L2}f_{sw} \triangle i_L^{\gamma} + a_{L3}I_{out}^2 \triangle i_L^{\lambda} \tag{3.9}$$

where a_{L1}, α, and β are the Steinmetz coefficients; a_{L2} and a_{L3} are the constants which are used to approximate the values of winding resistance; γ and λ are the real values that are used to reduce the non-linearity.

The approximated inductor volume is calculated as,

$$vol_{ind} = a_{L4}L\left(I_{peak,a}^2 + I_{peak,b}^2\right) + a_{L5}L\left(I_{peak,a} + I_{peak,b}\right) + a_{L6}\left(I_{peak,a} + I_{peak,b}\right) \tag{3.10}$$

$$I_{peak,a} = I_{out}\sin(\omega t) + i_{comp} + \frac{\triangle i_{L_a}}{2} \tag{3.11}$$

$$I_{peak,b} = I_{out}\sin(\omega t + \pi) + i_{comp} + \frac{\triangle i_{L_b}}{2} \tag{3.12}$$

where a_{L4}, a_{L5}, and a_{L6} are the polynomial coefficients of the inductor which must be a positive value. L is the inductor value $(L = L_a = L_b)$. $I_{peak,a}$ and $I_{peak,b}$ are the peak current of the inductors.

The inductor selection is associated with the value of the inductor and the maximum output current. The required value of the inductor is calculated by the following expression,

$$L = \frac{rV_{\text{in}}}{\Delta i_{\text{L}} f_{\text{sw}}} \tag{3.13}$$

where r is the ripple coefficient of the inductor, which can be selected to between 20% to 35% of the maximum output current. The current flow through the inductor contains switching ripple due to the switches ON and OFF. In equation (3.13), the ripple current can be reduced by increasing the value of the inductor. However, the preferred solution of the inductor is the lower value and smaller size. To decrease the inductance value, the switching frequency needs to be optimised accordingly.

3.2.3 Power Decoupling Capacitors

The power loss of the capacitor is calculated as,

$$P_{\text{cap}} = \frac{I_{\text{RMS,C}}^2 \tan\delta}{2\pi f_{2\omega} C} \tag{3.14}$$

where $I_{\text{RMS,C}}$ is the RMS current flow through the capacitor, $\tan\delta$ is the loss factor, $f_{2\omega}$ is the frequency of second-order ripple power and C is the value of the capacitance.

In practical design, the capacitance volume is varied by different manufacturers; for that reason, an approximated model is used. The total box volume of the capacitors vol_{cap} are calculated as,

$$vol_{\text{cap}} = a_{\text{C1}} C\left(V_{\text{C}_\text{a}}^2 + V_{\text{C}_\text{b}}^2\right) + a_{\text{C2}} C\left(V_{\text{C}_\text{a}} + V_{\text{C}_\text{b}}\right) + a_{\text{C3}}\left(V_{\text{C}_\text{a}} + V_{\text{C}_\text{b}}\right) \tag{3.15}$$

where a_{C1}, a_{C2}, and a_{C3} are the polynomial coefficients of the capacitor which must be a positive value. C is the output capacitor ($C = C_{\text{a}} = C_{\text{b}}$). V_{C_a} and V_{C_b} are the voltage across the output capacitors. The capacitor voltages V_{C_a} and V_{C_b} are represented as,

$$V_{\mathrm{C_a}} = \frac{V_{\mathrm{out}}}{2}(1 + \sin(\omega t)) + v_{\mathrm{comp}} \tag{3.16}$$

$$V_{\mathrm{C_b}} = \frac{V_{\mathrm{out}}}{2}(1 + \sin(\omega t + \pi)) + v_{\mathrm{comp}} \tag{3.17}$$

The output capacitor selection is the biggest challenge, which requires a trade-off to be made between the second-order ripple, power loss and volume. The details of the output capacitor selection are discussed in Section 3.

3.2.4 Heat sinks

The volume of the heat sink is calculated [123] as,

$$vol_{\mathrm{heat\ sink}} = \frac{V_{\theta\mathrm{SA}}}{P_{\mathrm{D}}}\left(\Delta T_{\mathrm{j}} - P_{\mathrm{D}}(R_{\theta\mathrm{JC}} + R_{\theta\mathrm{CS}})\right) \tag{3.18}$$

where $V_{\theta\mathrm{SA}}$ is the volumetric resistance, P_{D} is the power dissipated by the GaN FETs, ΔT_{j} is the temperature difference between the junction and the ambient, $R_{\theta\mathrm{JC}}$ is the thermal resistance from junction-to-case of the semiconductor, and $R_{\theta\mathrm{CS}}$ is the thermal resistance from case to the mounting surface of the semiconductor. The values of $R_{\theta\mathrm{JC}}$ and $R_{\theta\mathrm{CS}}$ are provided by the manufacturer. The value of $R_{\theta\mathrm{JC}}$ is considered to be one of the design parameters of the heat sink because it is attached to the heat source. Several other parameters need to be considered when selecting heat sinks, such as thermal resistance, volumetric resistance, and fin spacing. The extruded radial fins type heat sink is the better choice for the given design because it allows two switches to be mounted in one heat sink.

3.3 Trade-offs Between the Decoupling Capacitance, Power Loss and Power Density

The trade-off between the decoupling capacitance and the total power losses of the inverter are analysed in detail. The impacts of capacitance on the switching and conduction loss of GaN FETs are reflected in (3.1) to (3.3). The capacitor's power loss is calculated by (3.14).

The capacitance will also influence the power loss of the inductor by affecting the value of I_{out} in (3.9). It is then vital to derive the expression of the total capacitance, as follows.

The decoupling capacitors reduce the second-order ripples at the DC-link by buffering the second-order power. Hence, the second-order component is processed by the decoupling capacitors. The power balance equation of the decoupling capacitor can be written as,

$$2C\frac{dV_C^2}{dt} = \frac{V_{\text{out}}I_{\text{out}}}{2}\cos(2\omega t) \tag{3.19}$$

where V_{out} and I_{out} are the output voltage and current, ω is the angular frequency. Then, the capacitor voltage can be written as,

$$V_{\text{C}} = \frac{V_{\text{out}}}{2}(1+\cos(\omega t)) + v_{\text{comp}} \tag{3.20}$$

where v_{comp} is the second-order ripple compensation voltage. Integrating (3.19) and substituting V_{C} into (3.19) will give the expression of the total required capacitance as,

$$C = \frac{V_{\text{out}}I_{\text{out}}\sin(2\omega t)}{8\omega\left(\frac{V_{\text{out}}}{2}(1+\cos(\omega t)) + v_{\text{comp}}\right)^2} \tag{3.21}$$

Simplifying this equation with respect to the peak value yields the minimum required capacitance,

$$C_{\text{min}} = \frac{V_{\text{out}}I_{\text{out}}}{4\omega\left(V_{\text{out}} + v_{\text{comp}}\right)^2} \tag{3.22}$$

From (3.22), the minimum required capacitance C_{min} is calculated to be 28μF. A sensitivity analysis is performed to vary the total capacitance from its minimum required value of 28μF (Case I) to 6.6 times larger or 185μF (Case II) to investigate its impact on the power loss of the inverter. The results are given in Figure 3.2.

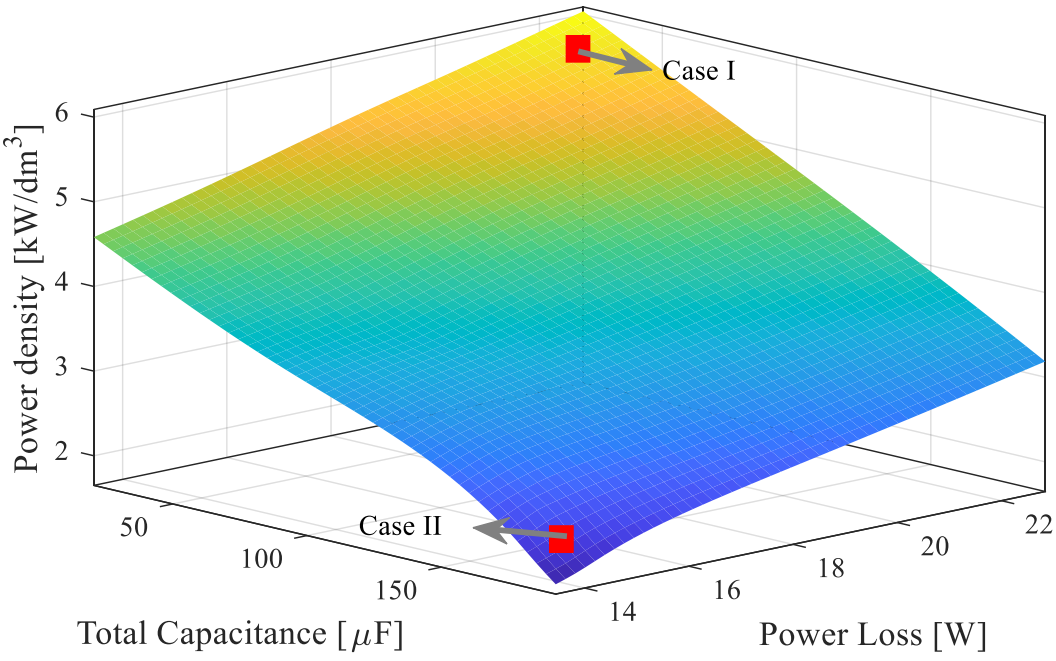


Figure 3.2: Relationship between total capacitance vs. inverter power loss vs. power density.

It can be observed that the power loss reduces non-linearly with the increase of capacitance. In Case I, the capacitance is minimised and hence results in a large amplitude of second-order ripple in the decoupling capacitors of inverters. This second-order ripple raises the total power loss to 23W, see Figure 3.2. In Case II, the capacitance is maximised, and the total power loss is reduced to only 13.8W. This happens because the large decoupling capacitor buffers the second-order ripple current, which minimises the effects on the circulating second-order current. However, arguably, such a big capacitor is not a good option because the power density of the inverter will be reduced to 2.07kW/dm^3. Moreover, the amount of change in power loss is less when the capacitance becomes larger. For instance, power loss reduces from 23W to 17W when the capacitance increases from 28μF to 55μF. The power density is changed from 5.84kW/dm^3 to 4.61kW/dm^3. However, the power loss is only reduced from 17W to 13.8W when the capacitance increases from 55μF to 185μF. A suitable capacitance would be in the range of 40μF to 55μF, where the average rate of change of power loss per capacitance is the highest, around 0.22W/μF. Meanwhile, above 55μF, the

average rate is 10 times less, around 0.025W/μF. In addition, the higher power density can be achieved.

To further acquire precisely optimised results considering both the total power loss and volume of the inverter, a multi-objective design method needs to be developed. The analysis of the trade-off between power loss and capacitance is integrated as part of the multi-objective design method.

3.4 Multi-objective Design Using GP

GP is a mathematical method that can be used to solve optimisation problems. The advantages of this method are that the global optimum solution always be achievable, and the mathematical operations do not exceed the dimension of the problem. GP has been applied to optimise the topology and components of power electronics converters [108]. The GP is used to find the global minimum of power loss and volume for the set of design inputs.

An overview of the proposed multi-objective design approach is presented in Figure 3.3. The multi-objective design approach is based on GP, which is a non-convex optimisation algorithm that is formulated using the monomial and posynomial function [124]. The GP can be expressed as follows,

$$\text{minimize } f_i(y) = \sum_{q=1}^{n} \left(a_{iq} y_1^{m_{iq1}} y_2^{m_{iq2}} \dots y_n^{m_{iqn}} \right)$$

subject to,

$$h_j(y) = \sum_{q=1}^{n} \left(a_{jq} y_1^{m_{jq1}} y_2^{m_{jq2}} \dots y_n^{m_{jqn}} \right) = 1 \quad j = 1, \dots, p$$

$$g_k(y) = \sum_{q=1}^{n} \left(a_{kq} y_1^{m_{kq1}} y_2^{m_{kq2}} \dots y_n^{m_{kqn}} \right) \leq 1 \quad k = 1, \dots, r \tag{3.23}$$

where $y = (y_1, y_2, \dots y_n)$ is the vector of the design variables, $f_i(y)$ is the objective function to be minimised, and $h_j(y)$ and $g_k(y)$ are the equality and inequality constraints, respectively, which must be satisfied by the solution. Using the logarithmic function, $f_i(y)$, $h_j(y)$ and $g_k(y)$ can be transformed into convex functions. The input variables y must be a non-zero real positive numbers and, the coefficients (a_i, a_j, a_k), and exponents (m_i, m_j, m_k) must be real numbers. The design variable y is replaced by its natural logarithm. Then, equation (3.23) becomes,

$$\text{minimize} \quad \log\left(f_i(e^x)\right)$$

subject to,

$$\log\left(h_j(e^x)\right) = 0 \quad j = 1, \dots, p$$

$$\log\left(g_k(e^x)\right) \leq 0 \quad k = 1, \dots, r \tag{3.24}$$

To formulate the GP for the multi-objective design approach, the total power loss $P_{\text{tot,loss}}$ and volume vol_{tot} are formulated as,

$$P_{\text{tot,loss}} = P_{\text{tot,sw}} + P_{\text{tot,cond}} + P_{\text{tot,C}_{\text{oss}}} + P_{\text{tot,rr}} + P_{\text{tot,g}} + P_{\text{tot,bd}} + P_{\text{ind}} + P_{\text{cap}} \tag{3.25}$$

$$vol_{\text{tot}} = vol_{\text{sw}} + vol_{\text{ind}} + vol_{\text{cap}} + vol_{\text{heat sink}} \tag{3.26}$$

Using equations (3.25) and (3.26), the objective function and inequality constraints can be obtained as,

$$\text{minimise} \quad f\left(P_{\text{tot,loss}}, vol_{\text{tot}}\right)$$

$$\text{subject to} \quad f_{\text{sw,min}} \leq f_{\text{sw}} \leq f_{\text{sw,max}}$$

$$A_{\text{sw,min}} \leq A_{\text{sw}} \leq A_{\text{sw,max}}$$

$$\Delta i_{\text{L,min}} \leq \Delta i_{\text{L}} \leq \Delta i_{\text{L,max}}$$

$$\Delta T_{\text{j,min}} \leq \Delta T_{\text{j}} \leq \Delta T_{\text{j,max}} \tag{3.27}$$

From (3.27), the optimal value of the power loss and volume of the inverters can be determined after several iterations. The optimised efficiency and power density of the design is then calculated. The outcome of the multi-objective design is the Pareto-front, which shows the optimised efficiency and power density of the designed inverter. In addition, the selection of the components can achieve optimised solutions.

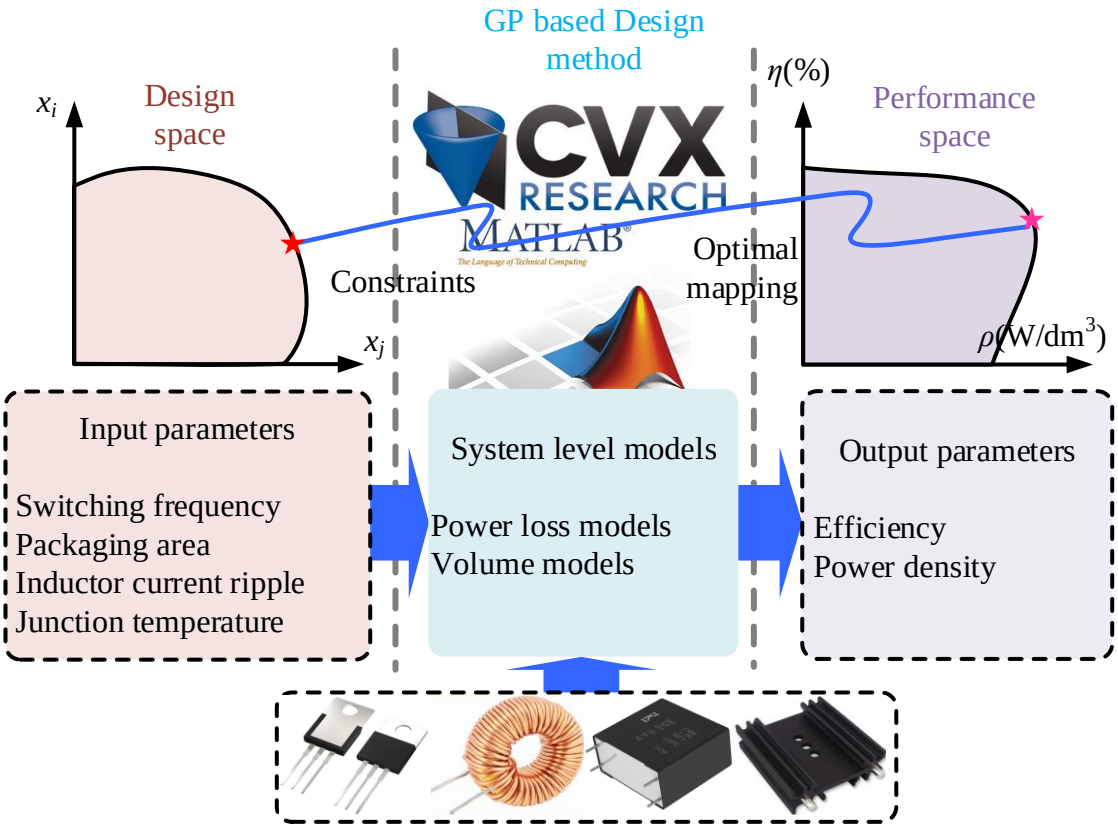


Figure 3.3: Overview of multi-objective design using GP-based design method.

3.5 Control of Differential Buck Inverter

The control of a differential buck converter is performed by supplying a sinusoidal voltage to the load and diverting the second-order ripple from the DC-link current. Figure 3.4 illustrates the inverter control with power decoupling scheme. $G_{v_{\mathrm{ab}}}(s)$, $G_{i_{\mathrm{La}}}(s)$ and $G_{i_{\mathrm{dc}}}(s)$ are the output voltage controller, inductor current controller and second-order ripple controller of the

inverter, respectively. These controllers are developed using the PR controller. From equations (3.28), (3.29) and (3.30), the targeted control frequency of the PR controller can be realised. The control objectives and the design details will be discussed in the following section.

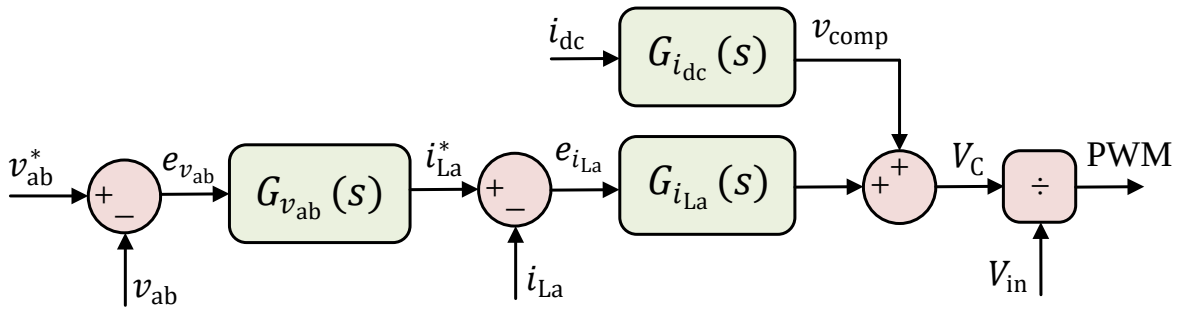


Figure 3.4: Control scheme of the inverter.

3.5.1 Output Voltage Controller

The voltage controller aims to control the fundamental frequency of the inverter. However, the output voltage can be affected by the odd and even order harmonics when considering the power decoupling functions. Therefore, the voltage controller includes odd and even harmonics compensators to reduce the effects of unwanted harmonic components and produce a pure sinusoidal voltage. The transfer function of the output voltage controller is expressed as follows:

$$G_{v_{ab}}(s) = k_{v_{ab}} + \sum_{r=1,2,3,4,5} \frac{2k_{rv_{ab}} s}{s^2 + \omega_r^2} \tag{3.28}$$

where $k_{v_{ab}}$ and $k_{rv_{ab}}$ are the proportional and resonant voltage controller gains; r is the target frequency; and ω_r is the resonant frequency, which allows any phase delay to be cancelled when following a sinusoidal signal. The proportional gain determines the bandwidth of the controller. The controller's gains are selected using a bode plot that is obtained from the system's open-loop transfer function. The minimum stability margin is then obtained. The bode diagram of a voltage control loop is given in Figure 3.5. Consequently, the optimal

value of the proportional gain $k_{v_{ab}}$ is obtained as 0.13 and the integral gain $k_{1v_{ab}}$, $k_{2v_{ab}}$, $k_{3v_{ab}}$, $k_{4v_{ab}}$ and $k_{5v_{ab}}$ are obtained as 100, 80, 50, 60, and 40. A minimum stability phase margin of 82.5^{o} and gain margin of 17.7dB are obtained.

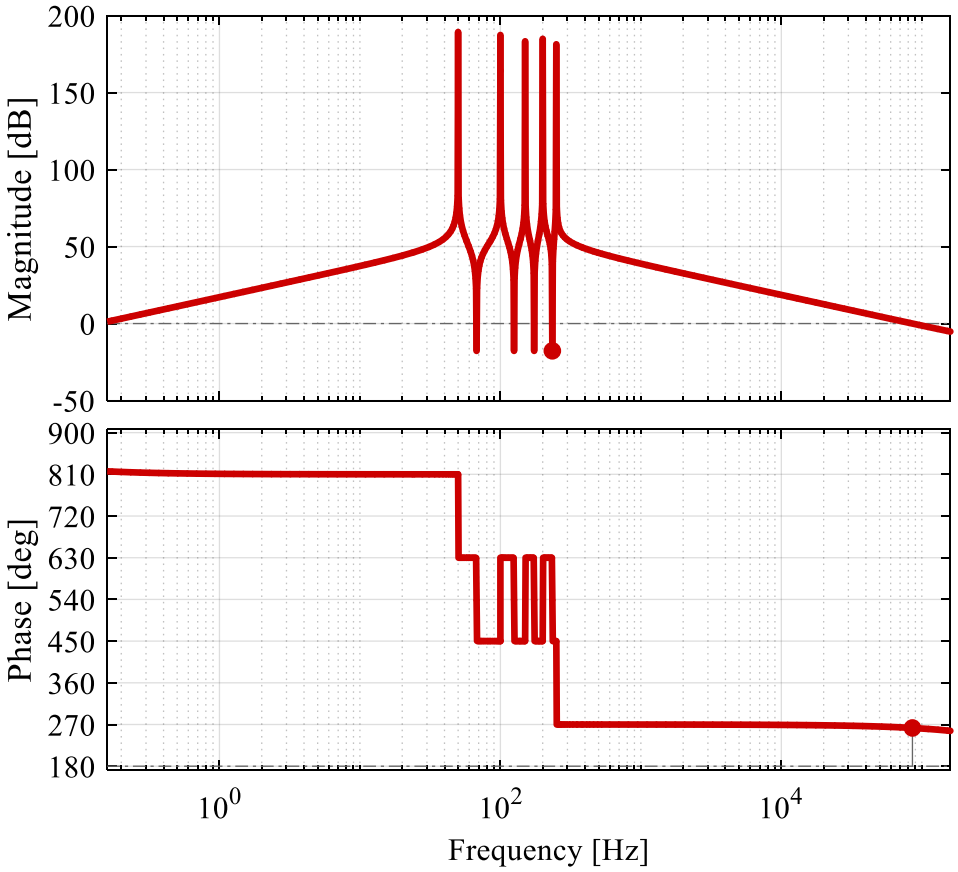


Figure 3.5: Bode diagram of the open loop linearised system $e_{v_{ab}}$ to v_{ab}.

3.5.2 Inductor Current Controllers

The inductor current controller tracks the fundamental frequency and limits the odd harmonics. Therefore, it includes the fundamental component and odd harmonic compensators. These compensators act according to the output of the voltage controller. The compensator of odd harmonics selected up to 7th orders, which is based on the harmonics of the output current. The transfer function of the inductor current controller is expressed as follows:

$$G_{i_{\mathrm{La}}}(s) = k_{i_{\mathrm{La}}} + \sum_{r=1,3,5,7} \frac{2k_{ri_{\mathrm{La}}}s}{s^2 + \omega_r^2} \tag{3.29}$$

where $k_{i_{\mathrm{La}}}$ and $k_{ri_{\mathrm{La}}}$ are the proportional and resonant current controller gains. The proportional gain determines the bandwidth of the controller. The controller gains are selected using a bode plot that is obtained from the system's open-loop transfer function, and the stability margin is confirmed. A bode diagram of the inductor current control loop is given in Figure 3.6. The optimal value of the proportional gain $k_{i_{\mathrm{La}}}$ is obtained as 1.4 and the integral gain $k_{1i_{\mathrm{La}}}$, $k_{3v_{\mathrm{ab}}}$, $k_{5i_{\mathrm{La}}}$ and $k_{7i_{\mathrm{La}}}$ are obtained as 15, 12, 8, and 5. A minimum stability phase margin of 66.4$^{\mathrm{o}}$ and gain margin of 7.96dB are obtained.

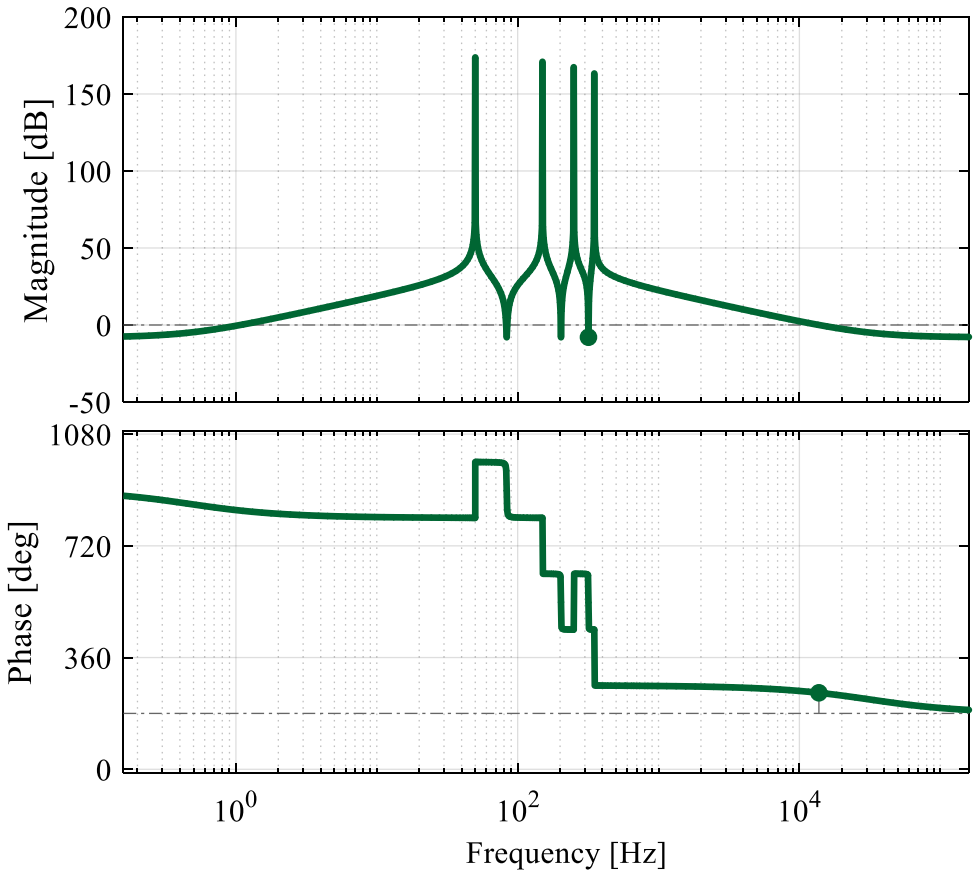


Figure 3.6: Bode diagram of the open loop linearised system $e_{i_{\mathrm{La}}}$ to i_{La}.

3.5.3 DC-link Ripple Controller

The DC-link ripple controller aims to remove the second-order ripple and the ripple residuals presented in the DC-link current. The controller consists of even harmonic compensators to cancel the even harmonics on the DC-link current. The transfer function of the second-order ripple controller is expressed as follows:

$$G_{i_{\mathrm{dc}}}(s) = k_{i_{\mathrm{dc}}} + \sum_{r=2,4,6} \frac{2k_{ri_{\mathrm{dc}}}s}{s^2 + \omega_r^2} \tag{3.30}$$

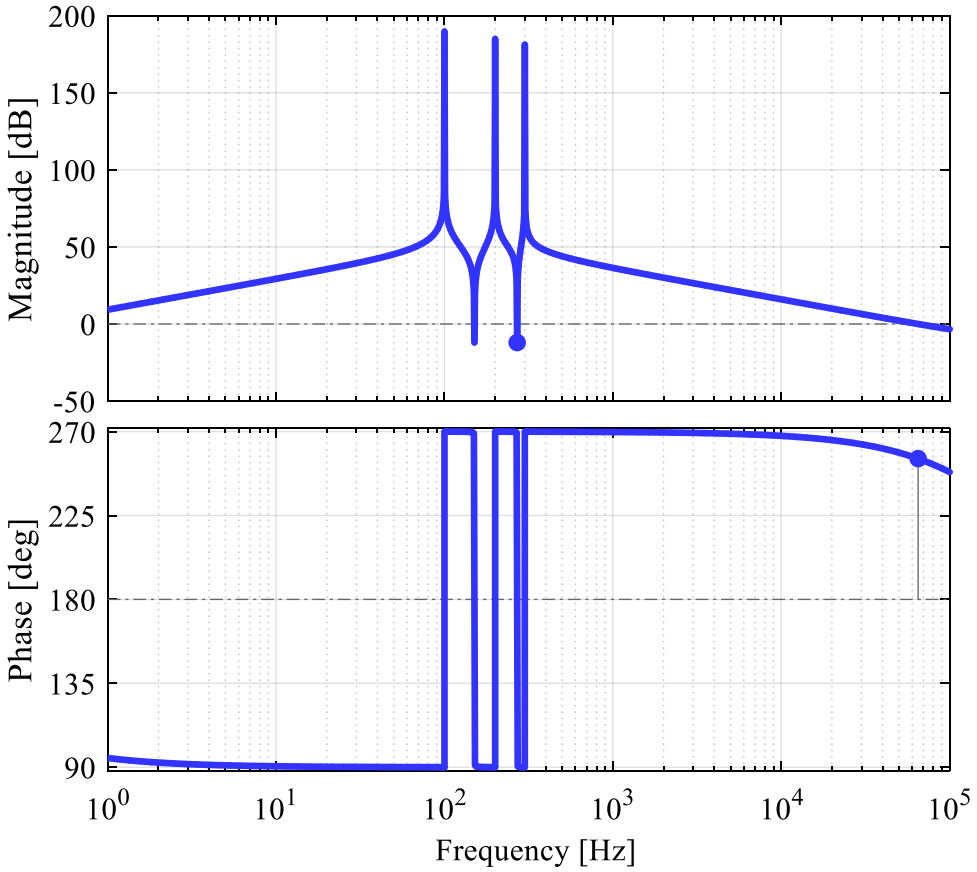


Figure 3.7: Bode diagram of the open loop linearised system $e_{i_{\mathrm{dc}}}$ to i_{dc}.

A bode plot of the linearised open-loop system is used to analyse the stability of the DC-link ripple controller, see Figure 3.7. The optimal value of the proportional gain $k_{i_{\mathrm{dc}}}$ is obtained as 0.25 and the integral gains $k_{2i_{\mathrm{dc}}}$, $k_{4i_{\mathrm{dc}}}$ and $k_{6i_{\mathrm{dc}}}$ are obtained as 105, 60 and 30, respectively. A minimum stability phase margin of 75.5$^{\mathrm{o}}$ and gain margin of 12dB are obtained.

3.6 Results and Discussions of the GP-based Design

The proposed design approach was developed in MATLAB/Simulink and validated by prototyping a 1kW GaN-based inverter. The performance of the inverter was evaluated in terms of efficiency and power density. The minimum and maximum values of the design variables that were used for the multi-objective design are given in Table 3.1. The values of design variables are selected following the industrial design standards. 900V GaN FET was used to build the prototype and the device is manufactured by Transphorm. The characteristic of the GaN FET devices is given in Table A.1. P11T60 series of high current toroid type fixed inductors were used, which were designed by MPS Industries. MKP1848C series of polypropylene film capacitors from Vishay BC Components were used. The values of the maximum output current $I_{\mathrm{out,max}}$ and reference switching area A^{*}_{sw} are 6.15A and 45.6 mm^2. The value of the inductor is $L = 390\,\mu$H, the capacitor is $C = 48\,\mu$F and the switching frequency is $f_{\mathrm{sw}} = 100$kHz. These values are selected according to the outcome of the multi-objective design approach. The coefficients that were used to obtain the inductor and capacitor volume are tabulated in Table 3.2.

Table 3.1: Design constraints of the GP method

Design variable	**Min. value**	**Max. value**
Switching frequency f_{sw}	10kHz	200kHz
Current ripple Δi_{L}	$0.1I_{\mathrm{out,max}}$	$0.45I_{\mathrm{out,max}}$
Switch area A_{sw}	$0.94A^{*}_{\mathrm{sw}}$	$1.07A^{*}_{\mathrm{sw}}$
Change in temperature ΔT_{j}	1$^{\mathrm{o}}$C	25$^{\mathrm{o}}$C

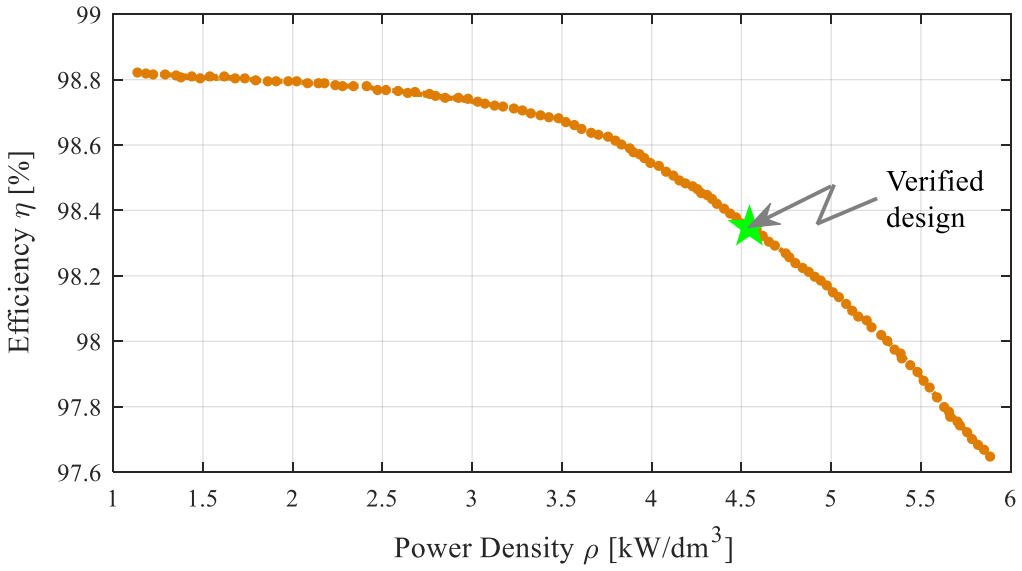
Table 3.2: Coefficients of inductor and capacitor volume

Coefficients	a_{L4}	a_{L5}	a_{L6}	a_{C1}	a_{C2}	a_{C3}
Value	3.2	7.8	1.069	0.011	0.06	0.03

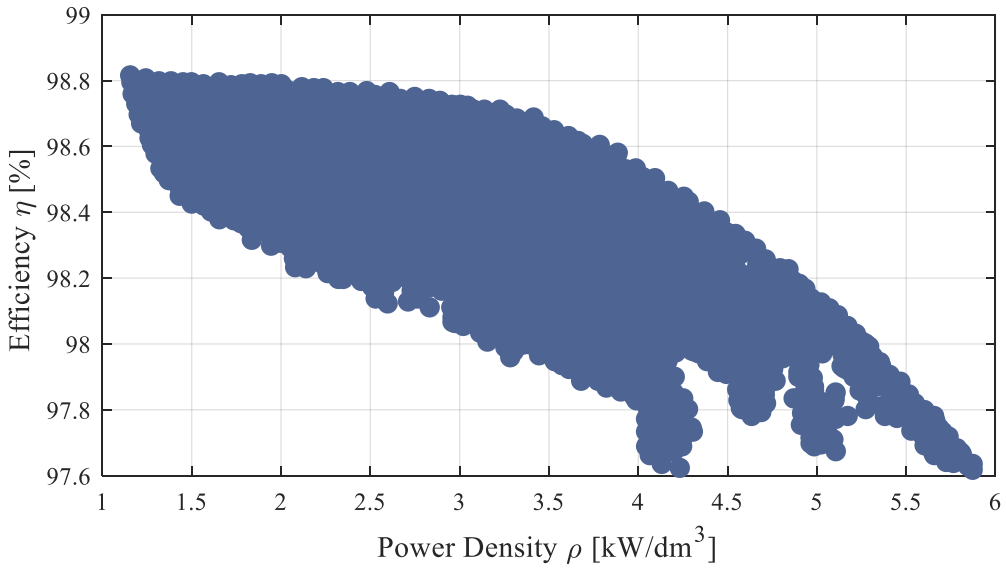
3.6.1 Performance Evaluation

The Pareto-front performance of the efficiency and power density ($\eta - \rho$) of the power inverter is generated by the multi-objective design and is given in Figure 3.8(a). Meanwhile, a numerical model is built to identify the optimal design boundary by scanning all of the achievable combinations of efficiency and power density of the inverter. The optimised design boundaries that are obtained by both methods are identical. However, the GP-based multi-objective design is much faster (16 *mins*) than the numerical model because it has more conditions and generates only optimised solutions. In contrast, the numerical model-based method takes 45 *mins* to scan all combinations, including generating optimised solutions and also the unwanted suboptimal solutions, see Figure 3.8(b).

The next step is to select one design from the Pareto-front performance and hence to validate the proposed method. The efficiency and power density of the selected design are 98.4% and 4.5kW/dm^3, which are favoured by the current PV inverter market. For the corresponding design, the power loss and volume are obtained as 15.93W and 218.32cm^3. The breakdown power loss and volume of each component are given in Figure 3.9. With the total power losses, semiconductors contributed 51.85%, inductors contributed 33.15% and capacitors contributed 15%. Likewise, with the total volume, heat sinks and switches occupied 34.18%, inductors occupied 33.57%, and capacitors occupied 32.25%.

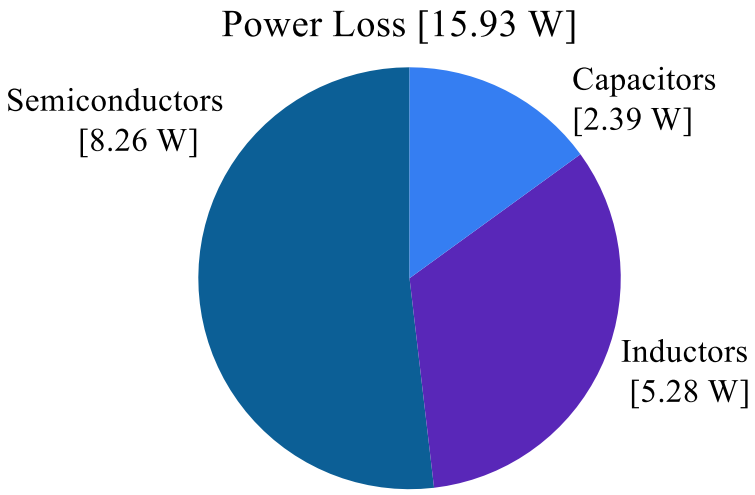


(a)

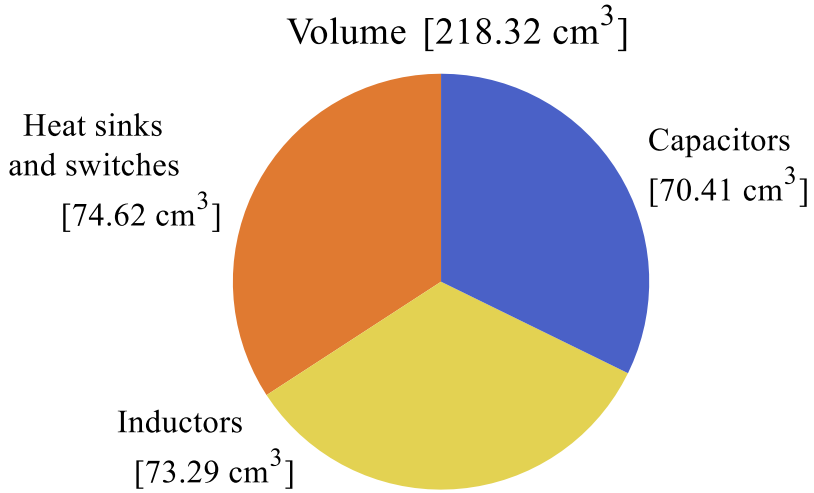


(b)

Figure 3.8: Efficiency vs. Power density: (a) Geometric program, and (b) Numerical model.

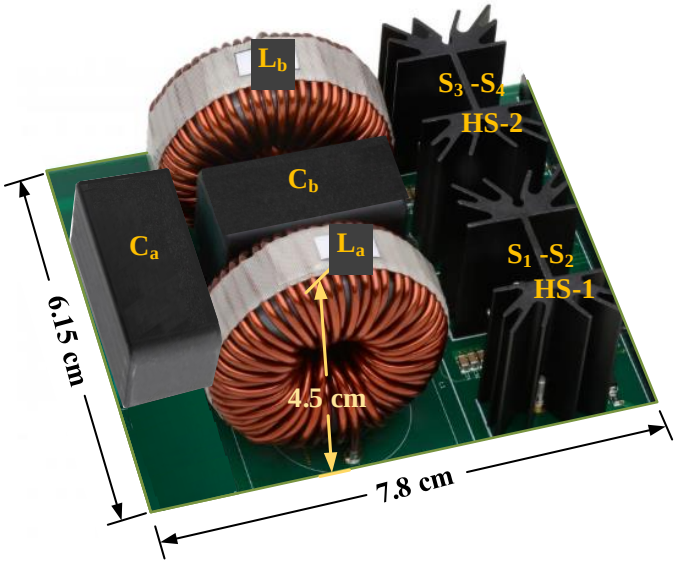


(a)

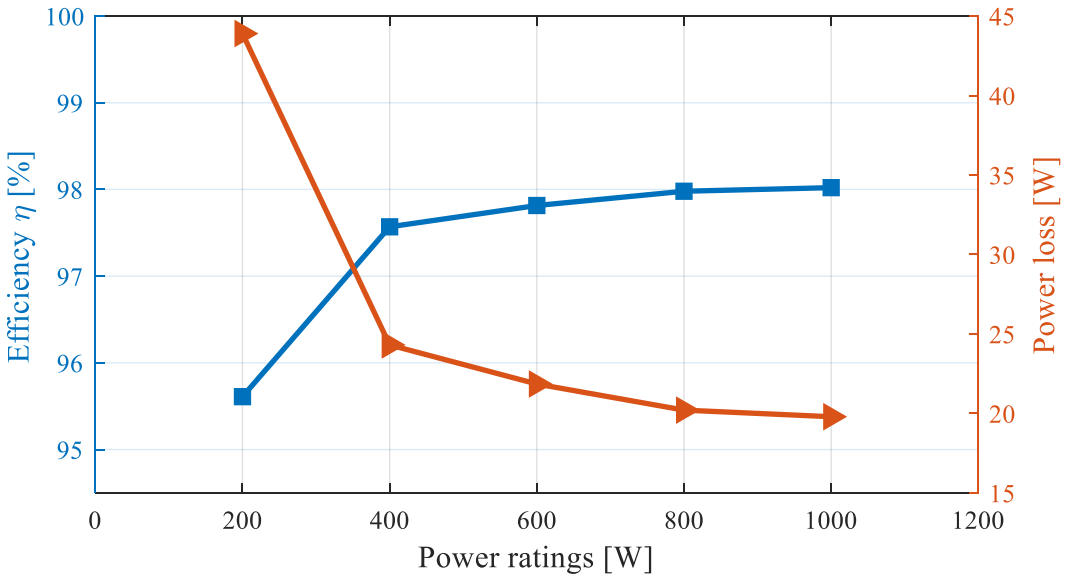


(b)

Figure 3.9: Results of GP: (a) Power loss, and (b) Volume.



(a)



(b)

Figure 3.10: Differential buck inverter: (a) Hardware prototype, and (b) Efficiency and power loss.

3.6.2 Experimental Verification

To verify the model, a prototype of the inverter has been built using the same components obtained by the selected design, as given in Figure 3.10(a). The prototype was examined at

different output power levels to obtain the response of efficiency vs output power, and power loss vs. output power, which are given Figure 3.10(b). A Yokogawa WT1806E precision power analyser was used to measure the efficiency. It has been observed that the maximum efficiency of the prototype is 98.02%. The power density is obtained as 4.54kW/dm^3 from the volume of the inverter, which is given in Figure 3.10(a). Therefore, the efficiency and power density match the results of the proposed design approach. Compared to the prototype, the efficiency and power density error obtained is only 0.38% and 0.06kW/dm^3. In conclusion, the multi-objective design approach is useful for an inverter with multiple design goals and its computation speed is much faster than the numerical modelling.

3.7 Summary

A design and control approach has been proposed to optimise the efficiency and power density of single-phase inverters with a power decoupling function. This approach has been developed based on detailed mathematical modelling of each component within the inverter. A trade-off study between the decoupling capacitor and the inverter power loss has been discussed and a sensitivity analysis was used to select the optimal capacitor value. The Pareto-front curve of efficiency versus power density was given for a different set of design requirements, which helps to understand the trade-off between the performance measures. This allows inverter designers to easily identify the optimum design parameters without compromising the total power loss or volume of the inverters much. Compared to the numerical model, the design approach is more effective in terms of computational complexity and convergence. In particular, the computational time of the proposed approach is 64.4% faster than the numerical model. Inverter designers can use the proposed design technique to quickly develop an overall optimum system design by considering the performance parameters with the design objective of maximising either efficiency or power density.

Chapter 4 A Fast and Accurate Artificial Intelligence-based Design Method for Single-phase Differential Buck Inverters

4.1 Introduction

The design method used in Chapter 3 largely rely on complex mathematical models which significantly increases the computational time, and complexity. With a larger number of design specifications, higher-performance computers are required; also, more constraints and conditions of computation are needed which further lead to problems including poor constraint handling capabilities, inaccurate design, difficult parameter tuning and inadequate problem dimension. These all could generate sub-optimal designs and make the whole design process meaningless. Therefore, a fast and accurate design method is required. To address these problems, this chapter has covered:

- An ANN-based design approach is proposed to design a single-phase inverter with a power decoupling function (Section 4.2).
- The power loss and volume of the switches, heat sinks, inductors, and capacitors are developed using mathematical equations. The training datasets for the ANN are generated using mathematical models. The input of the ANN is the design parameters, and the target is the performance parameters (Section 4.3).
- A back-propagation training algorithm is used to train the network. The well-known Levenberg-Marquardt optimisation updates the weights and bias values (Section 4.4).
- The performance of the ANN-based design is verified in terms of efficiency and power density. The results are compared with the existing design methods, such as a numerical model and the GP method (Section 4.5.1).

- ❖ The accuracy of the method is compared with the existing design methods. The computational time of different ANN designs are compared with the numerical model and GP method (Section 4.5.2 and 4.5.3).
- ❖ The outcome of the ANN design approach is also verified using experiments. The design parameters of the prototype are selected to meet the requirements of the PV inverter applications (Section 4.5.4).

4.2 Overview of ANN-based Design Method

Figure 4.1 gives an overview of an ANN-based design of a single-phase inverter. A mathematical model of the differential buck inverter topology was given in Chapter 3 (see Section 3.2), and thus will not be repeated. The mathematical models are used to generate the training datasets for the ANN. The flow chart in Figure 4.1 explains the process of how the dataset generation was trained. The generated data are fed into the neural network to train the network, as per the input and target. Once the network is trained, it can produce the efficiency and power density for any set of inputs. The power loss and volume of each component can then be obtained, and the optimal design can be selected.

4.3 Structure of the ANN for the Proposed Design

ANNs are an AI technique that can be used to design power converters accurately. They can predict the performance of an inverter based on the design parameters with less computation time [119]. The structure of the ANN that is used for the proposed design approach is given in Figure 4.2. It consists of three layers: the input layer, hidden layer, and output layer. The layers are interconnected through artificial neurons, and the neuron is called a node or unit. The number of input and output nodes are selected based on the application. However, the selection of hidden nodes is a little complicated and a proper sensitivity study is required to choose the number of hidden nodes.

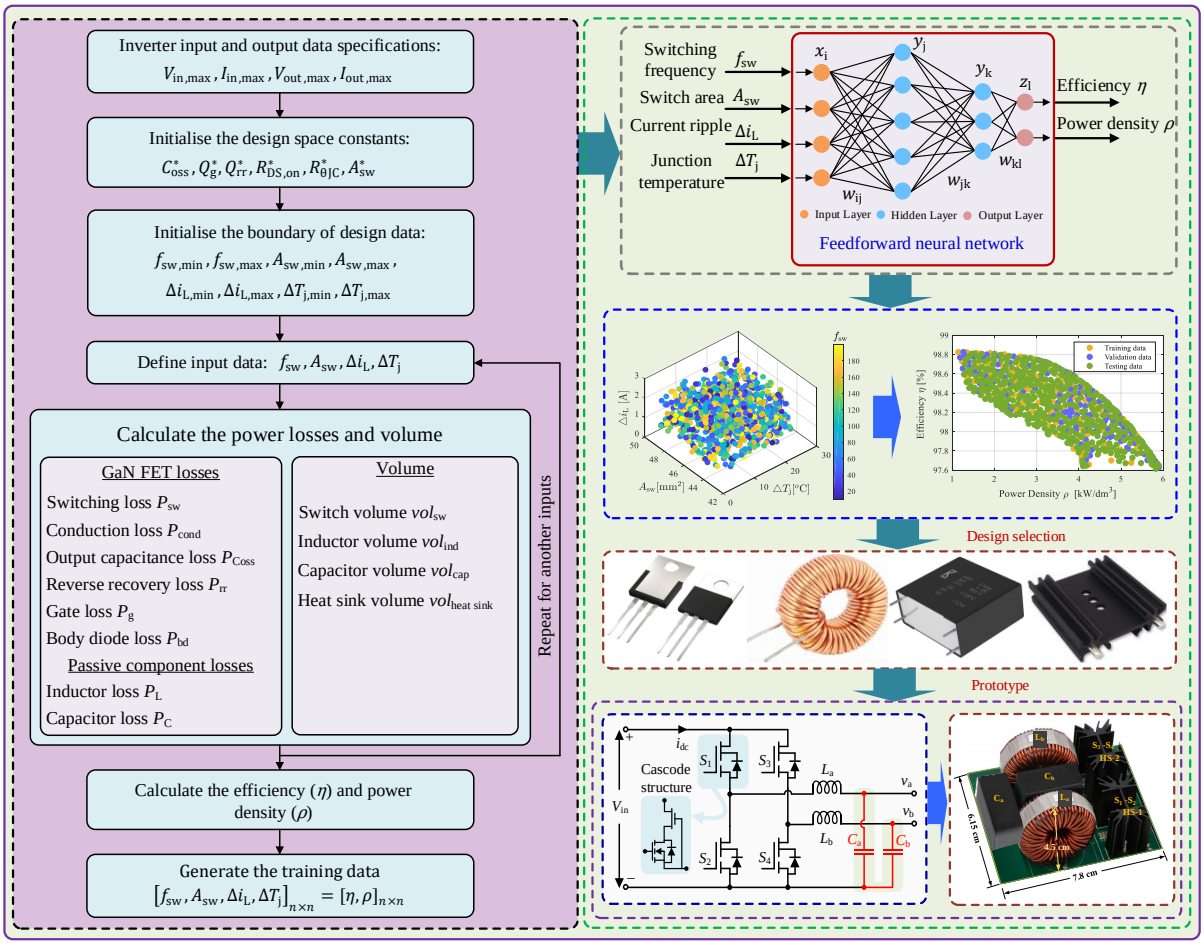


Figure 4.1: An overview of ANN for the proposed design method.

The complications are that the use of fewer hidden units will reduce the learning ability of the required function. However, this will significantly reduce the training time of the network. Therefore, proper validation is required to ensure network accuracy. The connections between nodes are associated with a weight, which sets the threshold value of each node. The weights between the input and hidden layer are represented by w_{ij}, and the weights between the hidden and the output layer are represented by w_{jk}. The initial value of the weight is selected randomly. It will then be changed during the training to reach the correct target. The switching frequency, area of the switch, inductor current ripple, and change of temperature are considered as the inputs. The efficiency and power density are considered as the targets.

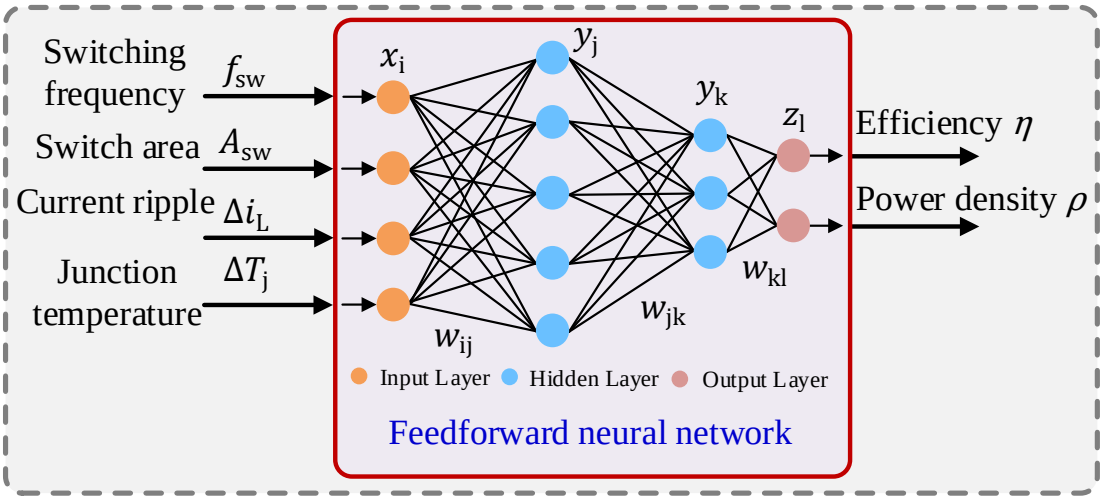


Figure 4.2: Structure of the ANN for the proposed design approach.

4.3.1 Input Layer

The first layer of the network is the input layer, which is denoted as $x_i, i = 1,2 \dots n$. The switching frequency, area of the switch, inductor current ripple and change of temperature are the inputs of ANN, which are represented as follows:

$$x_i = \left[f_{sw}\ A_{sw}\ \triangle i_L\ \triangle T_j\right] \tag{4.1}$$

4.3.2 Hidden Layer

The second layer of the network is the hidden layer, which is denoted as $y_j, j = 1,2 \dots n$ and $y_k, k = 1,2 \dots n$. Although the hidden layer and the neurons can be selected in any number, adding more neurons will increase the computational time and reduce the network effectiveness. Therefore, a sensitivity analysis is carried out to select the number of hidden layers and neurons. The analysis has been performed by changing the number of hidden layers and the neurons. Then, the regression response of the network is verified. Based on this, two hidden layers are chosen: the number of neurons is in the first layer, and the second hidden layer is chosen as 5 and 3. The weights between the input and the hidden layers y_j are represented by w_{ij}; and the weights between two hidden layers y_j and y_k are represented by

w_{jk}. The nodes of the hidden layers are made by a threshold function, which decides the output of each hidden node. The threshold function can be a step or a tangent sigmoid transfer function. The tangent sigmoid function is used, which is expressed as follows:

$$\phi(h) = \frac{1}{1 + e^{-h}} \tag{4.2}$$

where h is the weighted sum of the input to the hidden nodes. The output of the hidden layer is calculated as,

$$y_j = \phi\left(\sum_{i=1}^{n} w_{ij}\, x_i\right) = \frac{1}{1 + e^{-\sum_{i=1}^{n} w_{ij} x_i}} \tag{4.3}$$

$$y_k = \phi\left(\sum_{j=1}^{n} w_{jk}\, y_j\right) = \frac{1}{1 + e^{-\sum_{j=1}^{n} w_{jk} y_j}} \tag{4.4}$$

4.3.3 Output Layer

The last layer of the network is the output layer, which is denoted by $z_l, l = 1,2 \ldots n$. The efficiency and the power density are the output of the network. The weights between the hidden and output layers are represented by w_{kl}. The output of the network is calculated as,

$$z_l = \sum_{k=1}^{n} w_{kl}\, y_k \tag{4.5}$$

The output of z_l is applied to the tangent sigmoid function to approximate the output within the threshold limits.

4.4 Training the Network

Training is an iterative process to match the design parameters of the inverter to the performance parameters. The network is trained by a Levenberg-Marquardt back-propagation algorithm. While training, the network weights are adjusted in every iteration to achieve the

desired targets. The training process involves an optimisation approach to find the optimal weight, which consists of four steps: feed-forward computation, back-propagation to the output layer, back-propagation to the hidden layer, and updating the weights. The details of the steps are explained in the following subsections.

4.4.1 Feed-forward Computation

In this step, the network is initialised by the inputs, targets, and weights. The feed-forward computation can be realised from equations (4.1) to (4.5). The initial values of the weights are assigned randomly and will be updated on the next iteration. At the end of the computation, the derivative of the tangent sigmoid function is evaluated and stored at each node.

4.4.2 Back-propagation to the Output Layer

After the feed-forward computation, the fitness of the network is evaluated using the back-propagation error of the stored value. The back-propagation error of the output layer is calculated as,

$$z_{\mathrm{l,error}} = z_{\mathrm{l,out}}\left(1 - z_{\mathrm{l,out}}\right)\left(z_{\mathrm{l,target}} - z_{\mathrm{l,out}}\right) \tag{4.6}$$

where $z_{\mathrm{l,error}}$ is the error of output layer, $z_{\mathrm{l,out}}$ is the actual output, and $z_{\mathrm{l,target}}$ is the target output. Based on equation (4.6), the error efficiency η_{error} and power density ρ_{error} can be written as,

$$\eta_{\mathrm{error}} = \eta_{\mathrm{out}}(1 - \eta_{\mathrm{out}})\left(\eta_{\mathrm{target}} - \eta_{\mathrm{out}}\right) \tag{4.7}$$

$$\rho_{\mathrm{error}} = \rho_{\mathrm{out}}(1 - \rho_{\mathrm{out}})\left(\rho_{\mathrm{target}} - \rho_{\mathrm{out}}\right) \tag{4.8}$$

where η_{out} and ρ_{out} are the actual output of efficiency and power density. η_{target} and ρ_{target} are the target output of efficiency and power density.

4.4.3 Back-propagation to the Hidden Layer

The back-propagation errors of the hidden layers y_{k} and y_{j} are now calculated. The propagated error of each hidden node must be computed through the possible backward paths. The back-propagation errors of the hidden layers y_{k} and y_{j} are calculated as,

$$y_{\text{k,error}} = y_{\text{k,out}}\left(1 - y_{\text{k,out}}\right)\sum_{k=1}^{n} w_{\text{jk}}\, y_{\text{j}} \tag{4.9}$$

$$y_{\text{j,error}} = y_{\text{j,out}}\left(1 - y_{\text{j,out}}\right)\sum_{j=1}^{n} w_{\text{ij}}\, x_{\text{i}} \tag{4.10}$$

4.4.4 Updating Weights

The new weight of the network is adjusted based on the values of back-propagation error. The new weights are determined by the values of the old weights $w_{\text{kl,old}}$ and the change of weights. The change of weight is calculated by the partial derivative of the network error with a learning factor. The changes of weights and the new weights of the output layers are calculated as,

$$\triangle w_{\text{kl}} = \xi[\eta_{\text{error}}\, \rho_{\text{error}}]y_{\text{k}} \tag{4.11}$$

$$w_{\text{kl,new}} = w_{\text{kl,old}} + \triangle w_{\text{kl}} \tag{4.12}$$

The change of weight in the hidden layers are updated as,

$$\triangle w_{\text{jk}} = \xi y_{\text{k,error}} y_{\text{j}} \tag{4.13}$$

$$\triangle w_{\text{ij}} = \xi y_{\text{j,error}}\left[f_{\text{sw}}\ A_{\text{sw}}\ \ \triangle i_{\text{L}}\ \ \triangle T_{\text{j}}\right] \tag{4.14}$$

The new weights of the hidden layers are updated as,

$$w_{jk,new} = w_{jk,old} + \triangle w_{jk} \tag{4.15}$$

$$w_{ij,new} = w_{ij,old} + \triangle w_{ij} \tag{4.16}$$

where ξ is the learning rate, which decides the step length of weight correction. The iterations are repeated until the back-propagation error reaches the stopping criteria. After the training process, the fitness of the network is evaluated through statistical measures. Regression analysis is one of the most popular measures to evaluate the network. Once the evaluation is completed, the network is suitable to determine the power converter design parameters for any given input.

4.5 Results and Discussions of the ANN-based Design

The proposed ANN-based design approach was implemented in the MATLAB/Simulink software platform. To train the feed-forward network, 2000 design data were obtained from the mathematical model. For each design, the power loss and volume are calculated. Then, the corresponding efficiency and power density are obtained. The dataset was used in different ways to train, validate, and test the network. Out of the 2000 data, 30% of the data are used for training, 10% of the data are used for validation and the remaining 60% data are used for testing. The regression analysis of training, validation, and testing data of the network is given in Figs. 4.3 (a), (b), and (c). From the figures, the legend Y represents the fitness of the output and T is the target of the network. The output and target have the best fitness of linear regression for all the cases. In particular, the relationship between the output and target data are realised from the fitness value of R. The value of R is equal to that for the training, validation, and testing data, which indicates that the output and target data have a linear correlation.

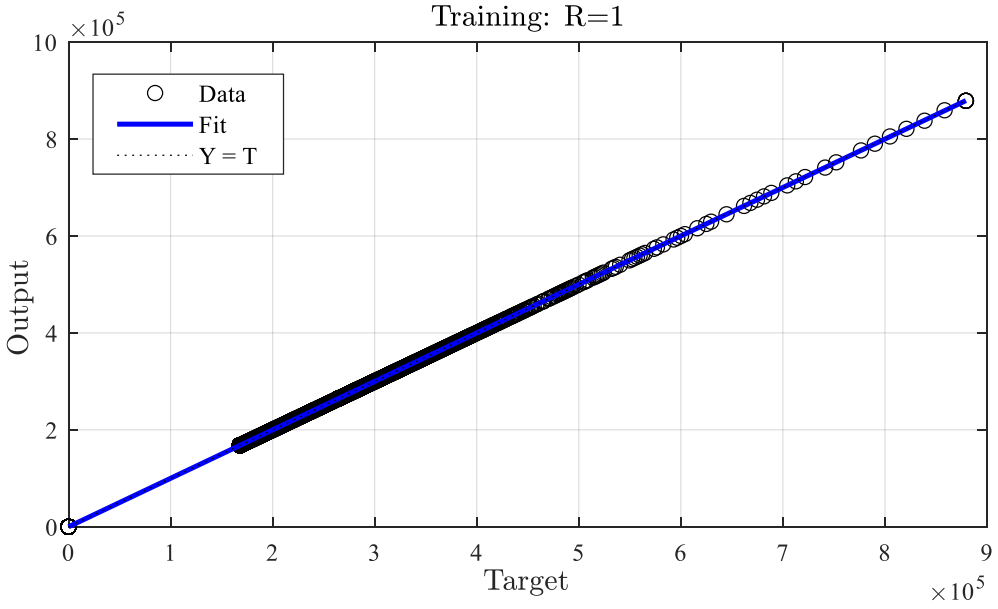
4.5.1 Performance Evaluation

The proposed design method was focused on a 1kW solar PV inverter application. The minimum and maximum values of the design space variables $f_{sw,min}$, $f_{sw,max}$, $\Delta i_{L,min}$, $\Delta i_{L,max}$,

$A_{\text{sw,min}}$, $A_{\text{sw,max}}$, $\Delta T_{\text{j,min}}$, and $\Delta T_{\text{j,max}}$ are given in Table 4.1. The performance of the inverter is examined in terms of efficiency and power density. Multiple design combinations are generated, and the best design is selected based on the design specifications. Then, the combinations of design space parameters are applied to the network and the corresponding performance space parameters are mapped into a 2D space. Using these performance space parameters, the Pareto-front response is plotted, and the trade-off between the performance parameter is obtained. The obtained design can provide a large degree of freedom to choose the required design parameters such as switching frequency, the value of the passive components and the semiconductor area.

Table 4.1: Design parameters of the ANN method

Design variable	**Min. value**	**Max. value**
Switching frequency f_{sw}	10 kHz	200 kHz
Current ripple Δi_{L}	$0.1I_{\text{out,max}}$	$0.45I_{\text{out,max}}$
Switch area A_{sw}	$0.94A_{sw}^{*}$	$1.07A_{sw}^{*}$
Change in temperature ΔT_{j}	1°C	25°C



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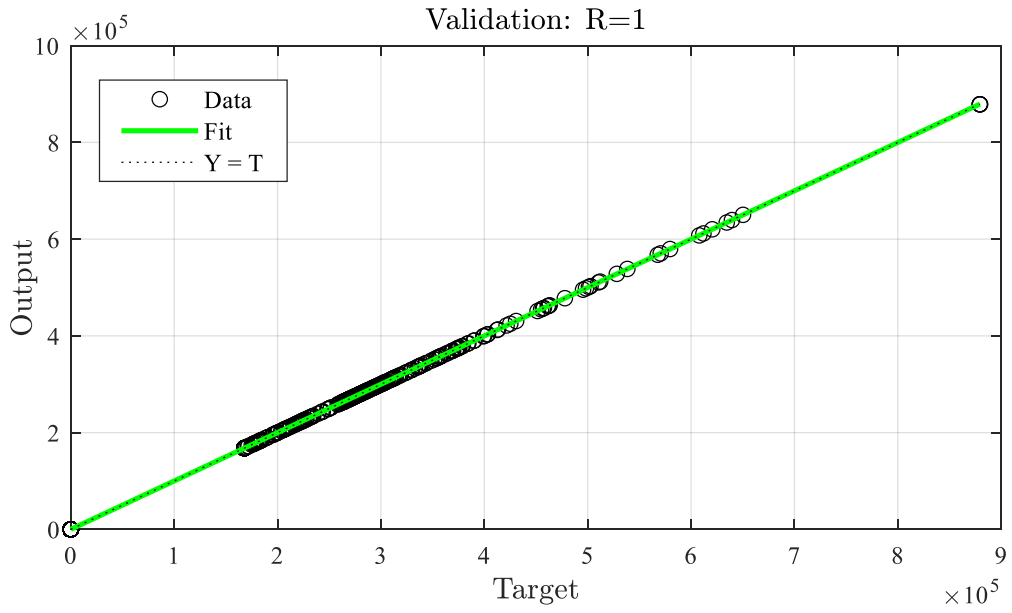

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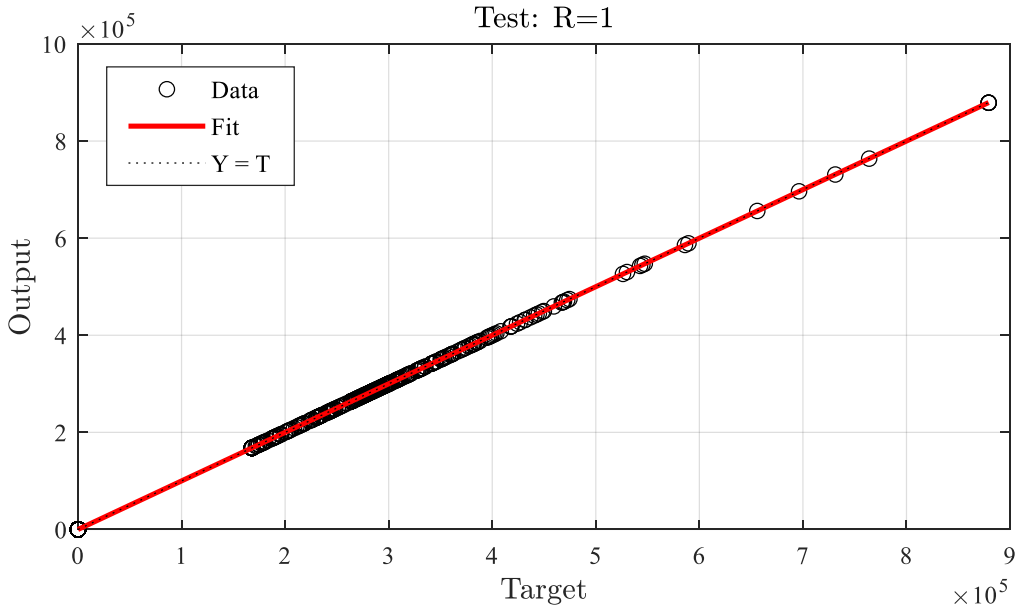
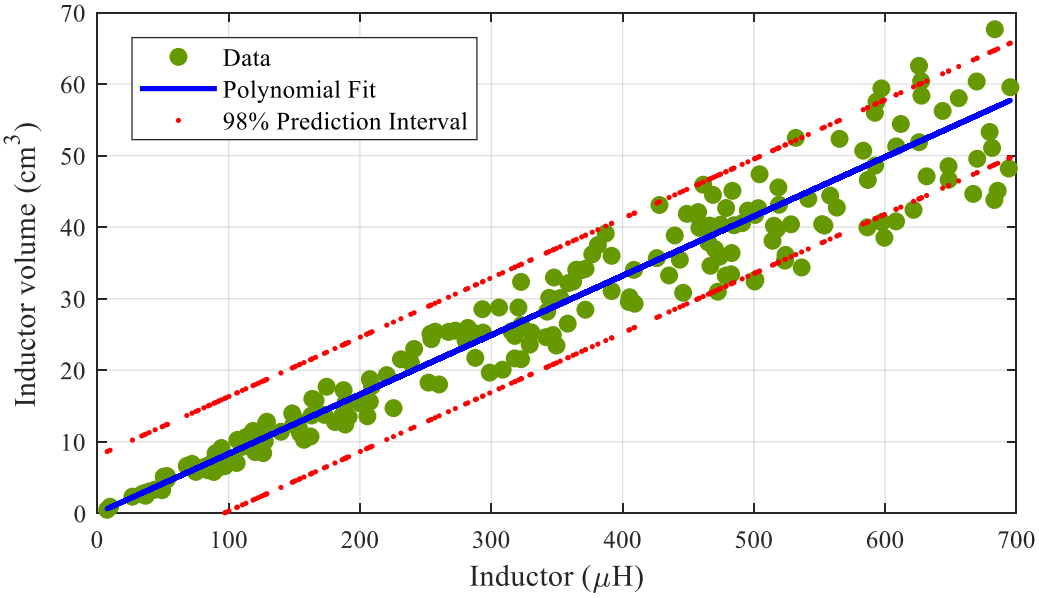
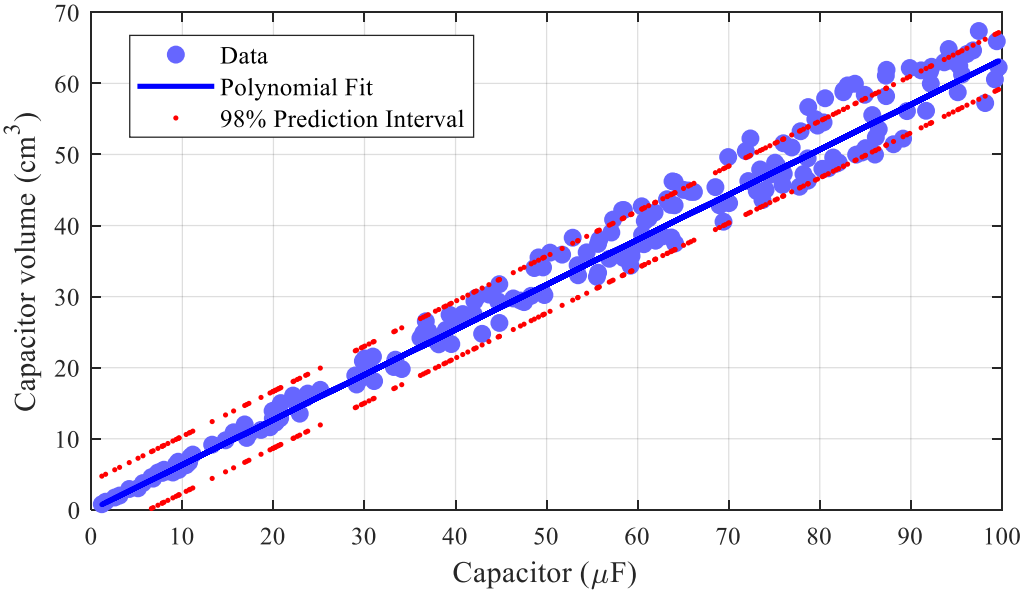


(c)

Figure 4.3: Regression of the network: (a) Training (b) Validation and (c) Testing.



(a)



(b)

Figure 4.4: Box volume of: (a) Inductor and (b) Capacitor.

The boxed volume of the inductance and the capacitance are given in Figs. 4.4 (a) and (b). To improve the design freedom, the design selection area is expanded by estimating the standard

error σ. The values of σ is calculated by the polynomial fit. From that, 95% of the prediction interval is chosen, which is calculated as follows:

$$vol_{\text{ind}} \pm 2\sigma \quad \text{and} \quad vol_{\text{cap}} \pm 2\sigma \tag{4.17}$$

The prediction interval improves the design flexibility and helps the designer to select the required volume of the inductor and capacitor. The inductor current ripple and the switching frequency are the dominant parameters related to the inductor and capacitor values. Based on these parameters, the volume of these components is computed from the ANN output. The boxed volume of the inductor and capacitor are obtained as 35.9 cm^3 and 34.6 cm^3.

Figure 4.5 shows the input datasets used to train, validate, and test the neural network. The $\eta - \rho$ Pareto-front performance of the efficiency and power density of the inverter is given in Figure 4.6. The trade-off between the efficiency and power density has differed as the design variables changed. To validate the proposed method, one design is selected for the given application criteria. The efficiency and power density of the selected design are $\eta = 98.4\%$ and $\rho = 4.57\,\text{kW/dm}^3$. For the selected design, the volume and power loss are obtained as 215.33cm^3 and 16W. The breakdown volume and power loss of each component are given in Figs. 4.7(a) and (b). With a total volume 215.33cm^3, heat sinks and switches occupied 34.46%, inductors occupied 33.42%, and capacitors occupied 32.12%. Similarly, with a total power losses 16W, switches contributed 44.89%, inductors contributed 36.27% and capacitors contributed 22.44%.

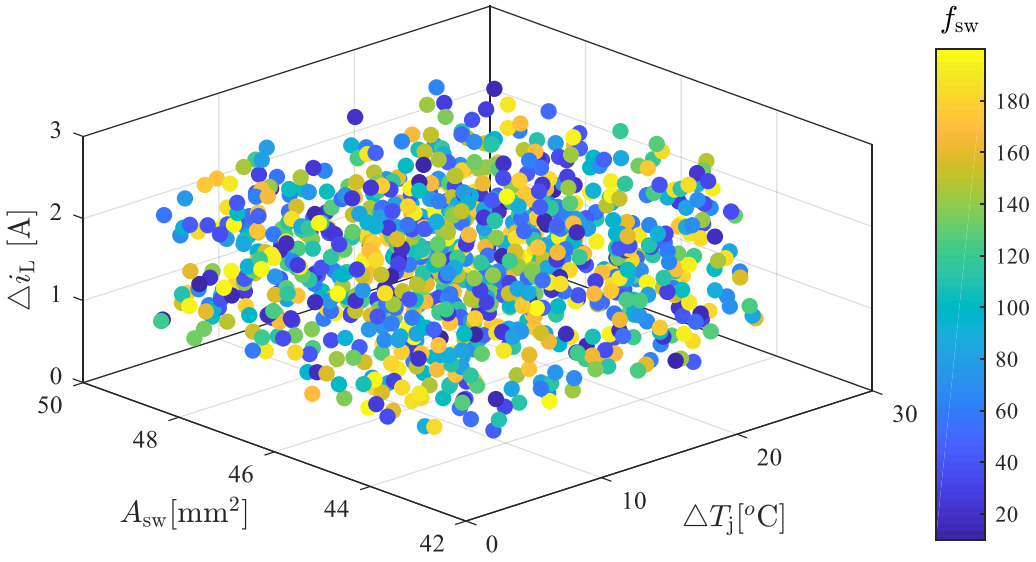


Figure 4.5: Input datasets were used to train, validate, and test the neural network.

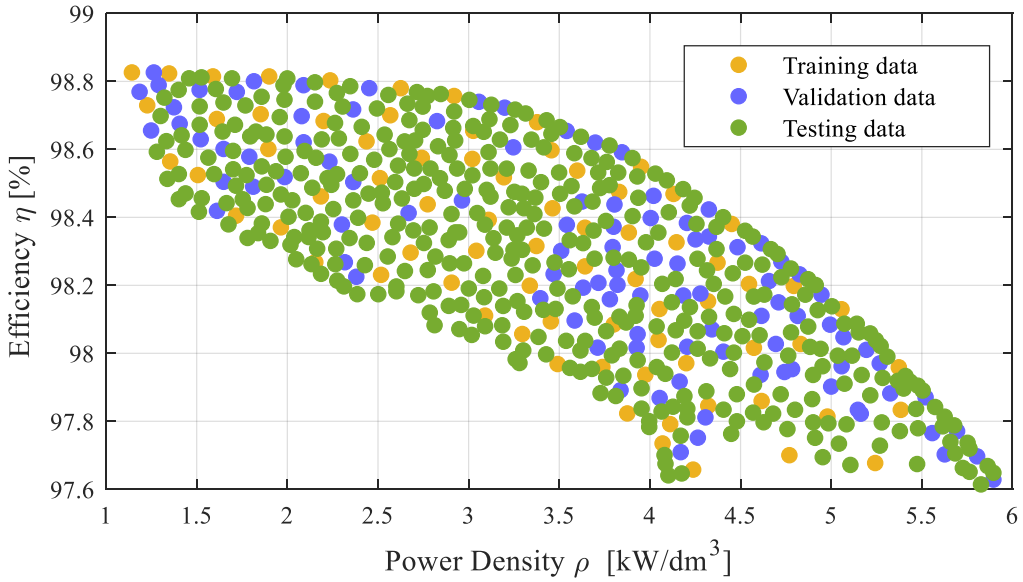


Figure 4.6: Efficiency vs. Power density of the ANN-based design approach.

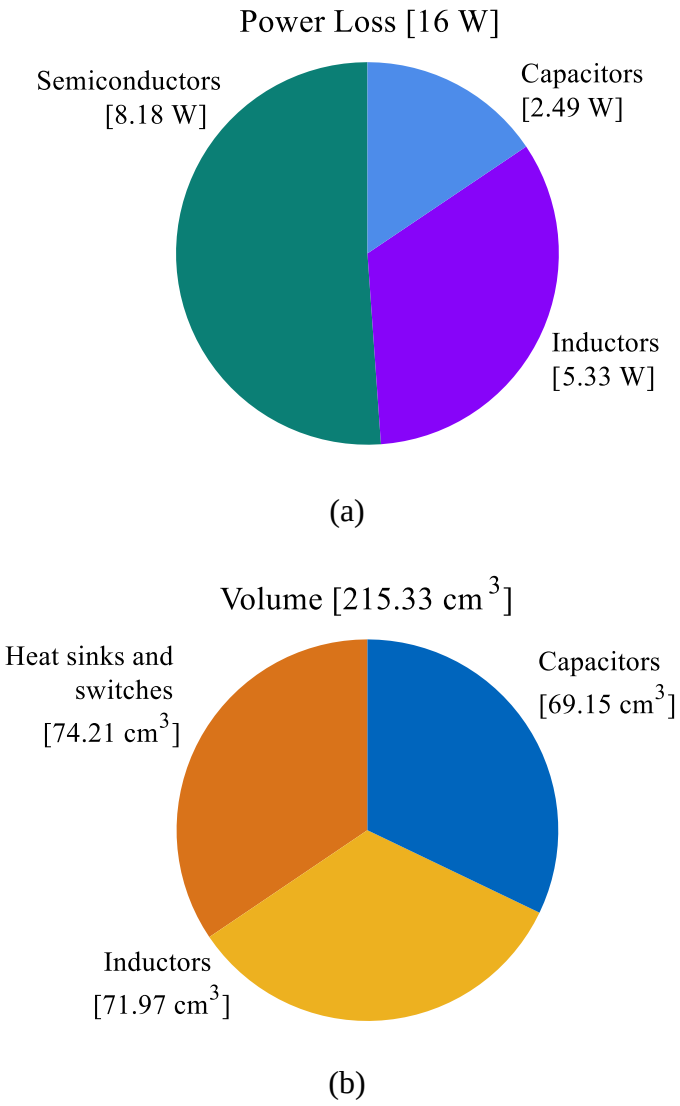


Figure 4.7: Results of ANN: (a) Power loss, and (b) Volume.

4.5.2 Comparison of ANN with Exiting Design Methods

The accuracy of the ANN-based design is compared with the numerical model and GP method. The efficiency vs. power density design boundary of the three methods is compared using 20 different designs. Figure 4.8 illustrates a comparison of the performance boundary against different methods. When comparing the design boundary of ANN and GP methods with the numerical model, both methods are determined using the same design boundary

without any errors. However, the designs inside the boundary are mismatched with the numerical model. The mismatch differences are quantified to compare the accuracy. The overall results of the ANN method are 97.3% accurate with the numerical model whereas the accuracy of the GP method is only 88.63%. Hence, the ANN-based design method is more accurate than the GP-based design method.

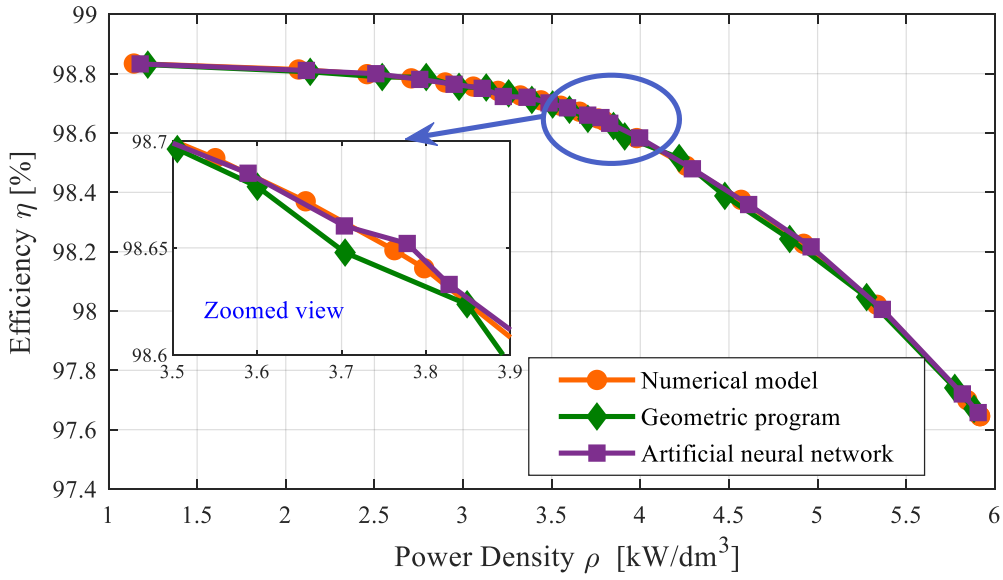


Figure 4.8: Comparison of performance boundary against different methods.

4.5.3 Comparison of Computational Time

The computational time of the proposed ANN-based design approach is compared with the numerical model and GP method. The computational time is calculated using an Intel(R) Core(TM) i7-6500U CPU @ 2.50GHz and the installed RAM 16.0GB. Five sets of design cases (i.e., 500, 1000, 1500, 2000, and 2500) are chosen to validate the computational time. In each design case, the computational time of GP and ANN are calculated, and the comparison results are given in Figure 4.9. From Figure 4.9. the effectiveness of ANN can be visualised. When the number of designs is increased to 2500, the numerical model takes a computational duration of 4 hrs and 56 mins the GP approach takes a computational duration of 3 hrs 52 mins. For the same case, the ANN-based design method takes less time (i.e., 1 hr 15 mins). The time duration includes both dataset generation and training time. In the testing

phase, the required design is predicted from the trained network; hence it is not required to generate the training data repeatedly for the next new test design. Overall, this significantly reduces the computational complexity of the ANN. However, in the numerical model and GP method, the process needs to be repeated. Therefore, the proposed design method takes less computational time to select the inverter design.

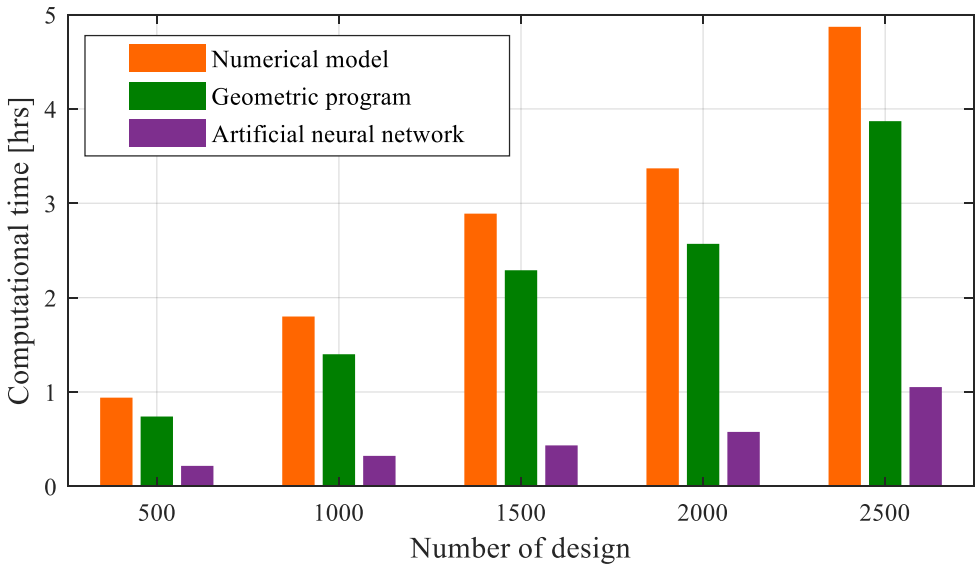


Figure 4.9: Comparison of computational time against different methods.

4.5.4 Experimental Verification

To ensure the benefits of the proposed design, a 1kW hardware prototype was built using the GaN FET devices. The experimental setup of the proposed design is given in Figure 4.10. The proposed design was examined with different values of power ratings, and the corresponding efficiency and power losses were obtained. A Yokogawa WT1806E precision power analyser was used to examine the efficiency of the inverter. From the prototype, the maximum efficiency was obtained as 98.02%, which is acknowledged with the ANN-based design results (98.4%). This confirms the accuracy of the ANN-based design approach.

The power decoupling capability of the proposed design was then verified, both with and without using the second-order ripple controller. Figure 4.11 shows the experimental results

of the input voltage V_{in}, DC-link current i_{dc}, output voltage v_{ab}, output current i_a, and decoupling capacitor voltages V_{Ca}, V_{Cb} without a second-order ripple controller. Figure 4.12 shows the experimental results of input voltage V_{in}, DC-link current i_{dc}, output voltage v_{ab}, output current i_a, and decoupling capacitor voltages V_{Ca}, V_{Cb} with a second-order ripple controller.

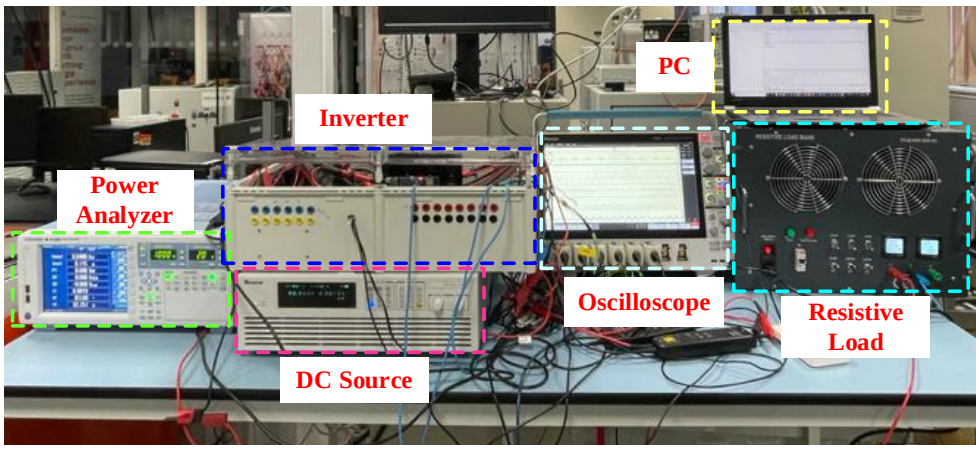


Figure 4.10: Experimental setup of a differential buck inverter.

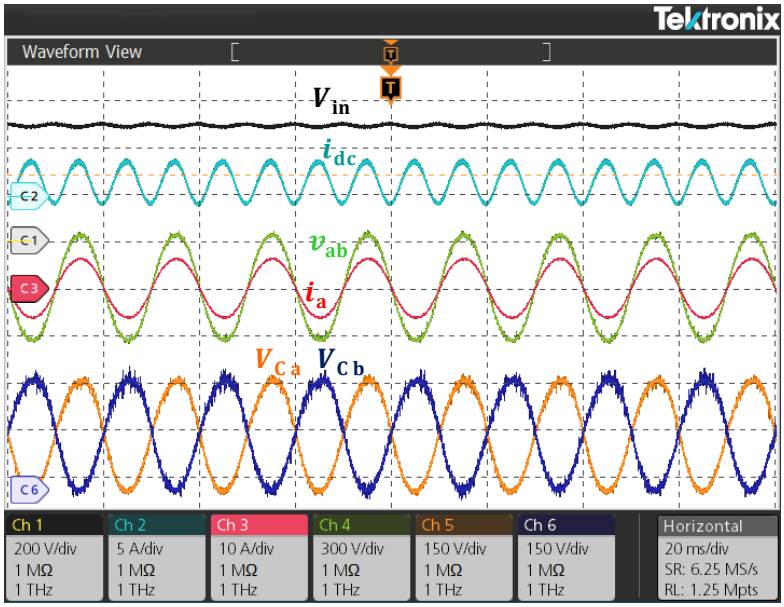


Figure 4.11: Steady-state waveforms at 1kW without a second-order ripple controller (V_{in}: 200V/div, i_{dc}: 5A/div i_a: 10A/div, v_{ab}: 300V/div, V_{ca}, V_{cb}: 150V/div).

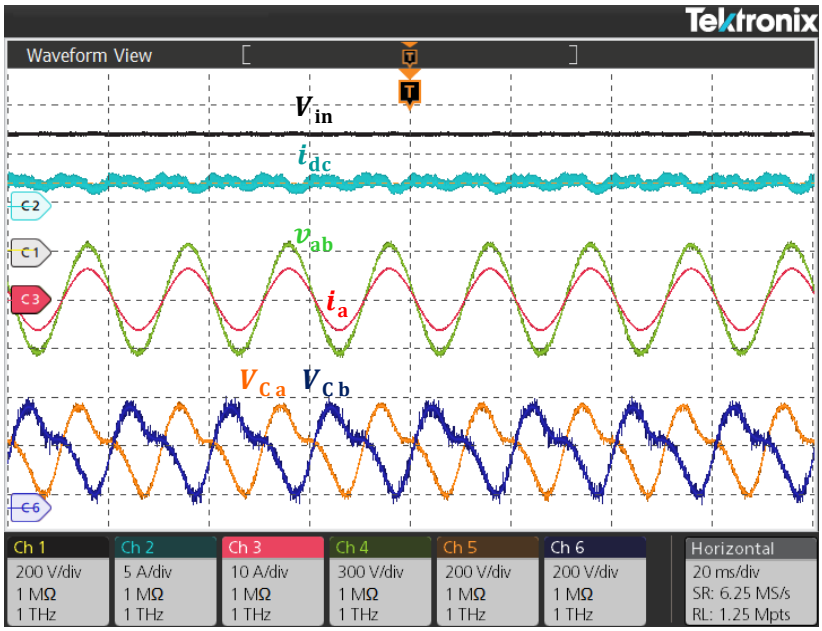


Figure 4.12: Steady-state waveforms at 1kW with second-order ripple controller (V_{in}: 200V/div, i_{dc}: 5A/div i_a: 10A/div, v_{ab}: 300V/div, V_{ca}, V_{cb}: 200V/div).

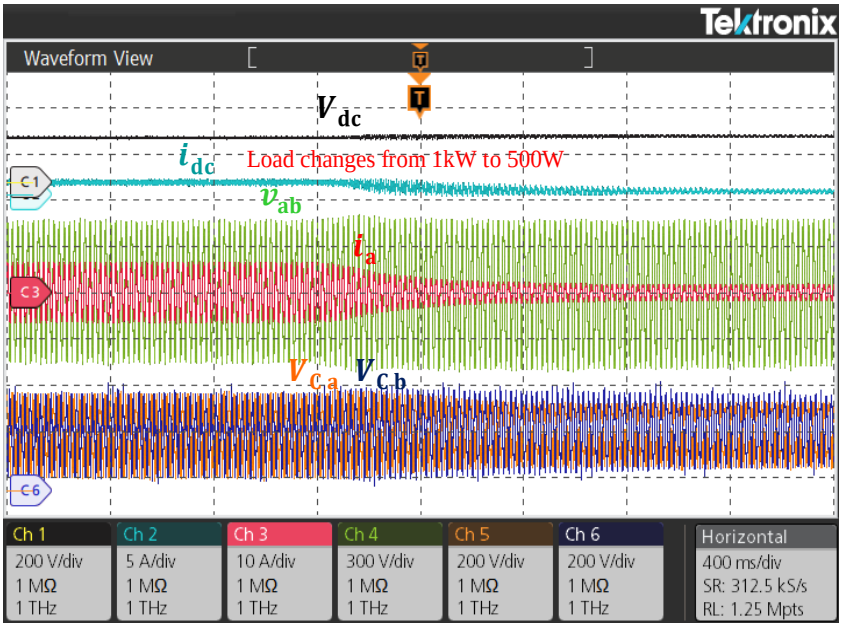
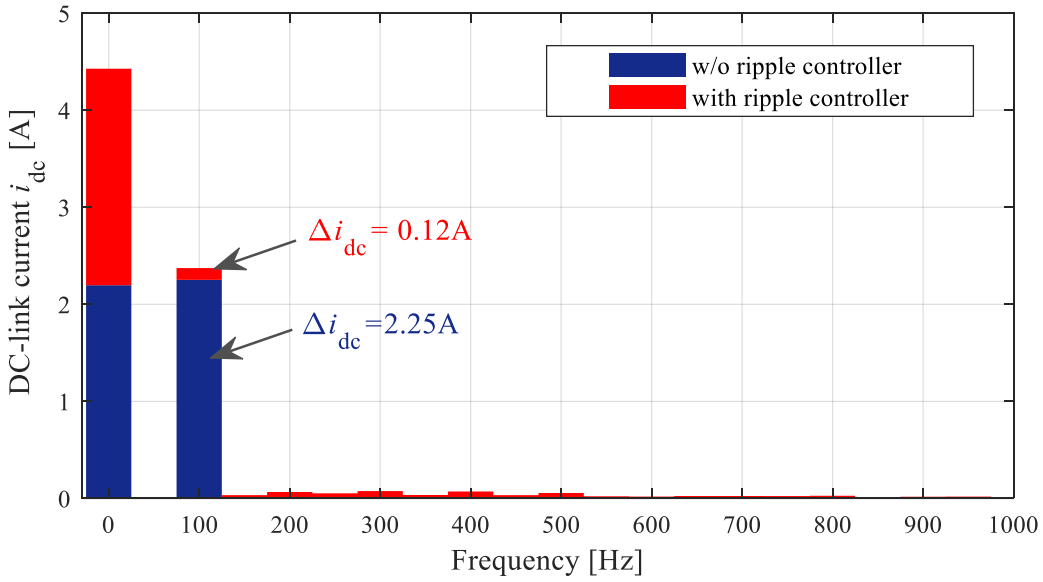
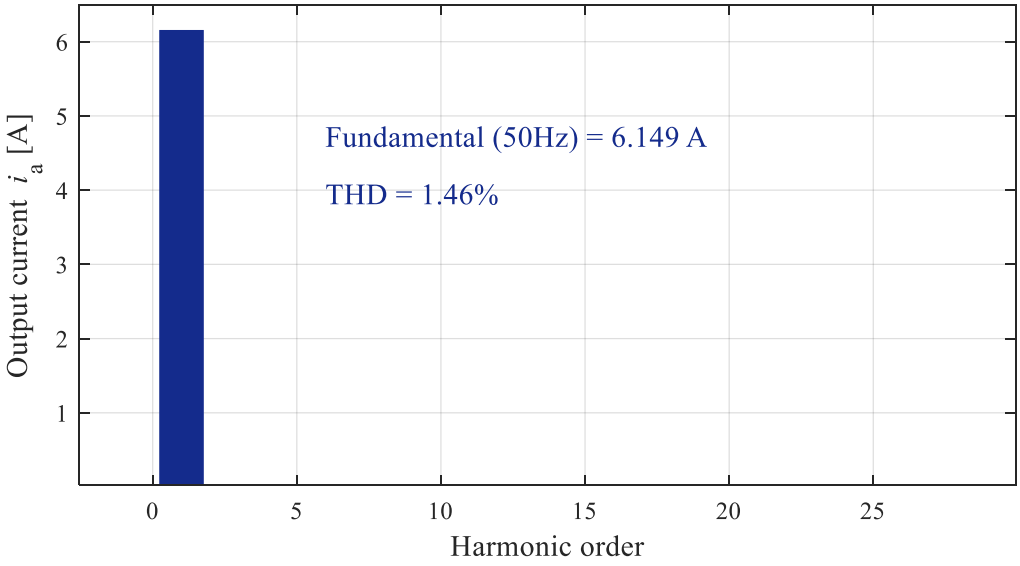


Figure 4.13: Experimental results when the load changes from 1kW to 500W (V_{in}: 200V/div, i_{dc}: 5A/div i_a: 10A/div, v_{ab}: 300V/div, V_{ca}, V_{cb}: 200V/div).



(a)



(b)

Figure 4.14: FFTs of (a) DC-link current with and without second-order ripple controller, and (b) Output current.

The dynamic response of the inverter is examined by changing the load from 1kW to 500W. Figure 4.13 shows the dynamic response of the inverter, which ensures the stable operation of the inverters changing the load. The elimination capability of the proposed prototype is quantified using the Fast Fourier Transform (FFT) approach. The FFTs of DC-link current with and without using the ripple controller are given in Figure 4.14(a). From this, the amplitude of second-order ripple in the DC-link current is 2.25A, which is reduced to 0.27A after using the ripple controller. The THD of the output current is obtained as 1.46%, which is given in Figure 4.14(b). The FFT results show that the proposed prototype performed well against the second-order ripple without affecting the output current.

4.6 Summary

An ANN-based design approach has been proposed to enhance the design performance of wide-bandgap power electronics converters. The ANN can be easily trained using a back-propagation algorithm and then be applied for the design process. The approach generates optimal designs located on the efficiency - power density Pareto-front curve. This ensures the best trade-off between the output performance parameters and allows the designer to quickly identify the optimum design parameters.

The proposed method has significant advantages in the reduction of computation time. It reduces around 78% and 67% computation time compared to the numerical model and GP methods when processing 2500 design cases. Hence, more processing time will be saved with the increasing number of design cases. The accuracy of the ANN-based design approach is also very high, its design accuracy for twenty designs has been tested to be 97.3% with an average mismatch of 2.73% while the GP method has only 88.63%.

The design approach has been further validated through experimental tests on a GaN-based single-phase differential inverter which was designed to have an efficiency of 98.4% and a power density of 4.57kW/dm^3. The tested efficiency and power density are 98.02% and 4.54kW/dm^3, which is well matched to the designed values, with an error of 0.38%, and 0.03kW/dm^3. Thus, the accuracy of the design approach has been further validated.

It is foreseeable that the ANN will be gradually used more for converters designs due to the advantages of fast computation and high accuracy, and the presented methods is well and timely contributed.

Chapter 5 A High Efficiency and High-Power Density Design for Single-Stage Buck-boost Differential Inverters

5.1 Introduction

The buck type differential inverter presented in Chapter 4 is a good option for applications where the DC-link voltage (400V) is higher than the output voltage. For a residential PV application, the input voltage is lower than the DC-link voltage. A DC-DC converter is needed between the source and the DC-link to step up the DC-link voltage. Such DC-DC converter requires a high current inductor and high voltage switches, which increases the additional losses, volume, and design costs. Meanwhile, an additional control is required to drive the switches. Therefore, a high efficiency and high-power density single-stage differential inverter is required. This chapter has covered:

- A single-stage buck-boost differential inverter is proposed, which can achieve the active power decoupling function without adding extra components. (Section 5.2).
- The different modes of buck-boost operation of the inverter are explained using the key waveform (Section 5.3).
- The details of the inverter component design are discussed (Section 5.4).
- The mathematical models of power loss, volume, and cost of each component within the inverter are developed. A multi-objective design approach is then developed using ANN to identify the optimal design parameters (Section 5.5).
- The output voltage controller, the inductor current controller and the second-order ripple controller are explained (Section 5.6).

❖ The proposed inverter and the ANN design approaches are implemented in MATLAB/Simulink platform and simulation results are verified (Section 5.7).

5.2 Overview of the Proposed Buck-boost Differential Inverter

Figure 5.1 shows the configuration of the buck-boost inverter. The topology is formulated by integrating two identical non-inverting buck-boost DC-DC converters. It consists of two inductors L_a and L_b, two capacitors C_a and C_b, and eight switches S_1-S_8. The switches S_1, S_2 and S_5, S_6 are dedicated to achieving buck operation and, S_3, S_4 and S_7, S_8 are dedicated to achieving boost operation respectively. The input voltage and current are denoted as V_{in} and i_{dc}, and the output voltage current are denoted as v_{ab} and i_a. The output of the inverter is based on the voltage across the capacitors V_{Ca} and V_{Cb}. The input, capacitor voltage and output responses are highlighted in Figure 5.1. Therefore, each converter needs to be operated independently to achieve the sinusoidal output.

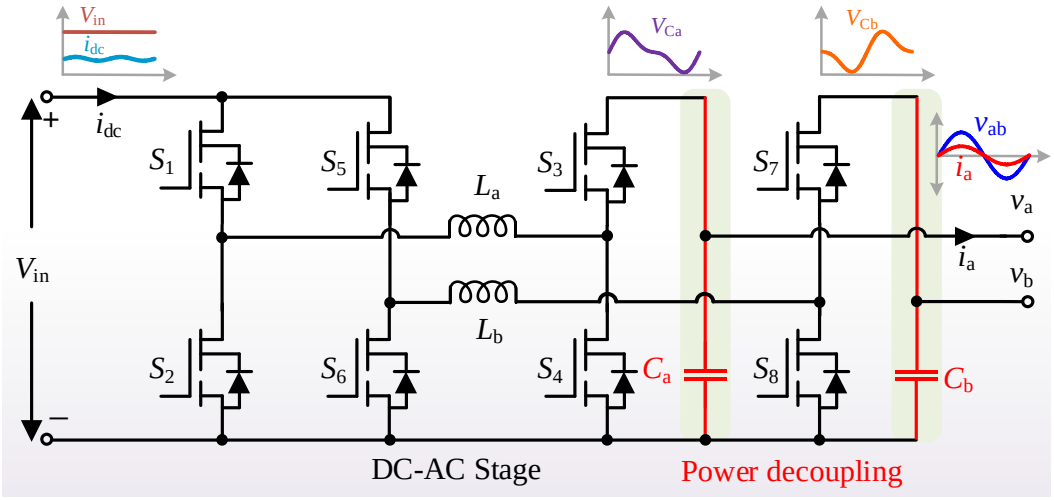


Figure 5.1: Single stage buck-boost inverter topology.

5.3 Operation of the Buck-boost Inverter

Figure 5.2 shows the key waveform of the buck-boost inverter. The inverter operates in the same manner as conventional buck-boost converters with the required offset. Hence, the capacitor voltages are purely controlled as DC. To generate a sinusoidal output voltage v_{ab}, the voltage across the capacitors is controlled with sinusoidal voltage with and offset (see V_{Ca} and V_{Cb} in Figure 5.2). The voltage across the capacitors V_{Ca} and V_{Cb} can be represented as follows:

$$V_{\mathrm{Ca}} = \frac{V_{\mathrm{ab}}}{2}(1 + \sin \omega t) + v_{\mathrm{comp}} \tag{5.1}$$

$$V_{\mathrm{Cb}} = \frac{V_{\mathrm{ab}}}{2}(1 + \sin(\omega t + \pi)) + v_{\mathrm{comp}} \tag{5.2}$$

The output voltage can be written as,

$$v_{\mathrm{ab}} = V_{\mathrm{Ca}} - V_{\mathrm{Cb}} \tag{5.3}$$

By substituting (5.1) and (5.2) in equation (5.3), we get:

$$v_{\mathrm{ab}} = \frac{V_{\mathrm{ab}}}{2}(1 + \sin \omega t) + v_{\mathrm{comp}} - \frac{V_{\mathrm{ab}}}{2}(1 + \sin(\omega t + \pi)) - v_{\mathrm{comp}} \tag{5.4}$$

$$v_{\mathrm{ab}} = \frac{V_{\mathrm{ab}}}{2}(\sin \omega t - \sin(\omega t + \pi))$$

$$v_{\mathrm{ab}} = V_{\mathrm{ab}} \sin \omega t \tag{5.5}$$

where V_{ab} is the amplitude of the output voltage and v_{comp} is the second-order ripple compensated voltage. The power decoupling method and the calculation of v_{comp} are explained in Appendix B.

5.3.1 Mode of Operation

The key waveforms for the mode of operations of the inverter are shown in Figure 5.2. Four modes are used to achieve required operation of the inverter, which is given Figure 5.3.

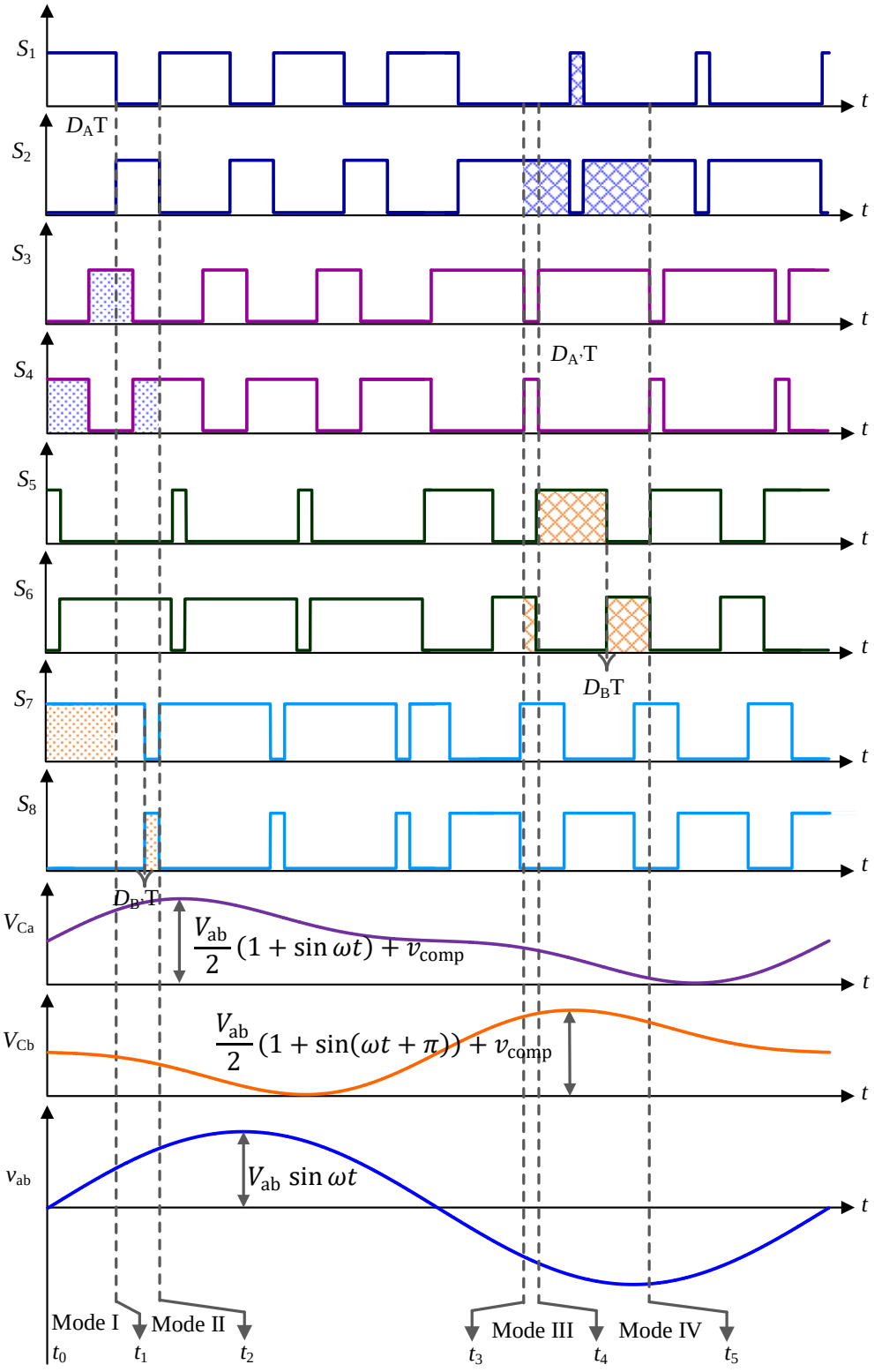


Figure 5.2: Key waveforms of the buck-boost inverter.

Mode I $[t_0 - t_1]$, Figure 5.3(a): When the switch S_1 is ON, the inductor L_a current increases rapidly and the current flows through switches S_3 and S_4. Based on the duty cycle of switches S_3 and S_4, the boost operation can be achieved. The change of inductor current L_a can be represented as follows:

$$\frac{V_\mathrm{in}}{L_\mathrm{a}} D_{\mathrm{A}'} + \left(\frac{V_\mathrm{in} - V_\mathrm{Ca}}{L_\mathrm{a}}\right)(1 - D_{\mathrm{A}'}) = 0 \tag{5.6}$$

Mode II $[t_1 - t_2]$, Figure 5.3(b): In this mode, the switch S_3 is ON, the inductor L_a current flows through the load. Then, based on the duty cycle of switches S_1 and S_2, the buck operation can be achieved. The change of inductor current L_a can be represented as follows:

$$\left(\frac{V_\mathrm{in} - V_\mathrm{Ca}}{L_\mathrm{a}}\right) D_\mathrm{A} - \frac{V_\mathrm{Ca}}{L_\mathrm{a}}(1 - D_\mathrm{A}) = 0 \tag{5.7}$$

Mode III $[t_3 - t_4]$, Figure 5.3(c): When switch S_5 is ON, the inductor L_b current increases rapidly and the current flows through switches S_7 and S_8. Based on the duty cycle of switches S_7 and S_8, the boost operation can be achieved. The change of inductor current L_b can be represented as follows:

$$\frac{V_\mathrm{in}}{L_\mathrm{b}} D_{\mathrm{B}'} + \left(\frac{V_\mathrm{in} - V_\mathrm{Cb}}{L_\mathrm{b}}\right)(1 - D_{\mathrm{B}'}) = 0 \tag{5.8}$$

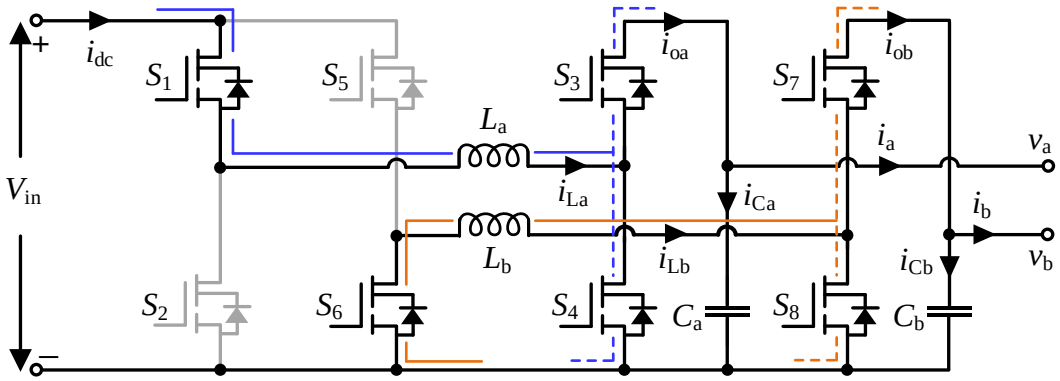
Mode VI $[t_4 - t_5]$, Figure 5.3(d): In this mode, the switch S_7 is ON, the inductor L_b current flows through the load. Then, based on the duty cycle of switches S_5 and S_6, the buck operation can be achieved. The change of inductor current L_b is represented as follows:

$$\left(\frac{V_\mathrm{in} - V_\mathrm{Cb}}{L_\mathrm{b}}\right) D_\mathrm{B} - \frac{V_\mathrm{Cb}}{L_\mathrm{b}}(1 - D_\mathrm{B}) = 0 \tag{5.9}$$

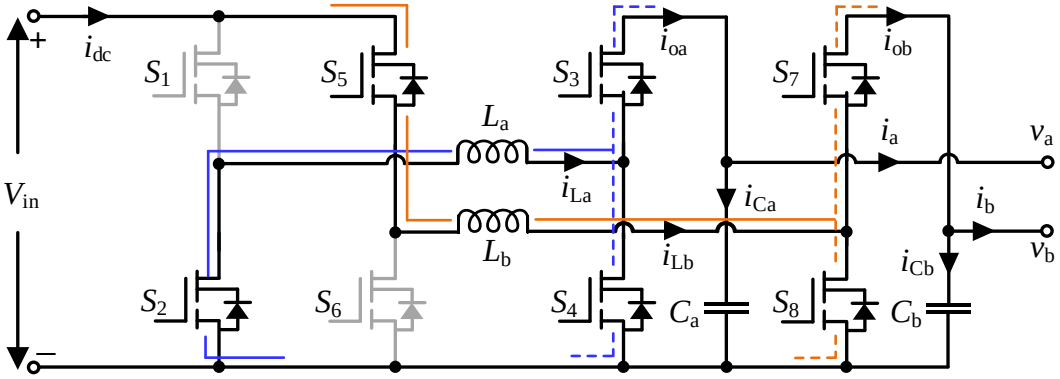
From equations (5.6) to (5.9), the buck and boost mode of the inverter can be realised. The output voltage v_{ab} is calculated as,

$$v_\mathrm{ab} = \frac{D_\mathrm{A} D_\mathrm{B} V_\mathrm{in}}{(1 - D_{\mathrm{A}'})(1 - D_{\mathrm{B}'})} \tag{5.10}$$

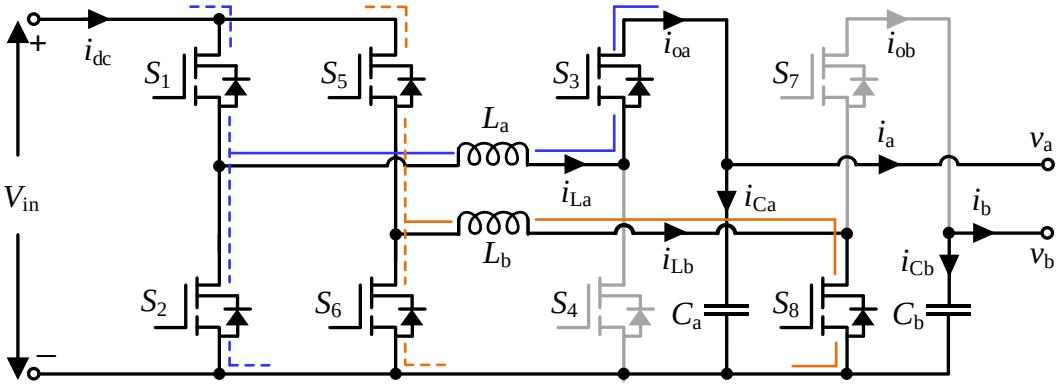
where D_A is the duty cycle of switches S_1 and S_2. $d_{A'}$ is the duty cycle of switches S_3 and S_4. D_B is the duty cycle of switches S_5 and S_6. $d_{B'}$ is the duty cycle of switches S_7 and S_8.



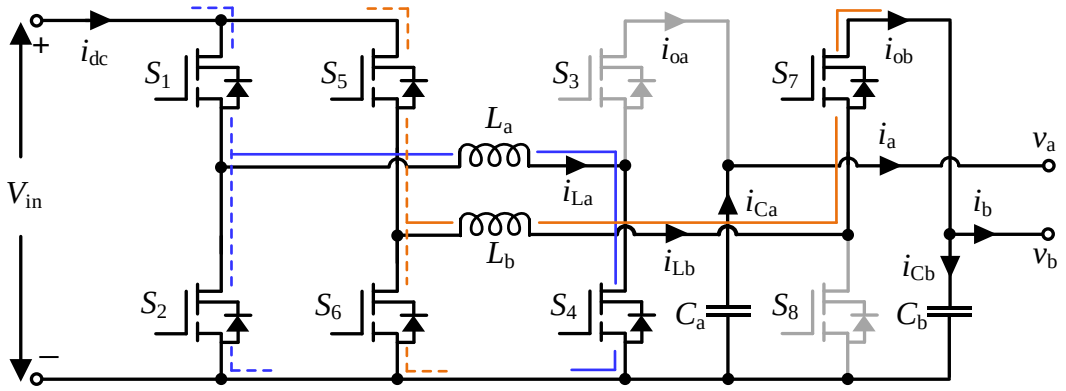
(a)



(b)



(c)



(d)

Figure 5.3: Mode of operation of the inverter: (a) Mode I, (b) Mode II, (c) Mode III, (d) and Mode IV.

5.4 Modelling of Power Loss, Volume, and Cost of the Buck-boost Inverter

The detailed modelling of the differential buck-boost inverter topology (see Figure 5.1) is presented. The detailed system-level power loss, volume, and cost models of each component are derived based on the active power decoupling approach. From this, the efficiency, power density, and specific cost are further determined. The design variables including switching frequency f_{sw} the inductor ripple Δi_L, the switch area A_{sw}, and the junction temperature ΔT_j are used to calculate the power loss and volume. Then, the component costs are modelled based on the outcome of the power loss and volume models.

5.4.1 Power GaN FETs

The power loss models of the GaN FETs are derived based on the on-state resistance $R_{DS,on}$, the output capacitance C_{oss}, and the thermal junction-to-case resistance $R_{\theta JC}$ of the switches. These variables are scaled by their reference values with respect to the area of the switch. The switching losses of the inverter are the sum of the turn-on and turn-off losses of all of the

switches [115][121]. The switching losses of the buck side switches S_1, S_2, S_5 and S_6 are calculated as,

$$P_{\text{sw, buck}} = f_{\text{sw}}\left\{\left(I_a \sin(\omega t) + i_{\text{comp}} - \frac{\triangle i_{\text{L}_\text{a}}}{2}\right)(V_{\text{in}} t_{\text{on}} + V_{\text{SD}} t_{\text{off}}) + \left(I_{\text{a}} \sin(\omega t) + i_{\text{comp}} + \frac{\triangle i_{\text{L}_\text{a}}}{2}\right)(V_{\text{in}} t_{\text{off}} + V_{\text{SD}} t_{\text{on}})\right\} \tag{5.11}$$

The switching losses of the boost side switches S_3, S_4, S_7 and S_8 are calculated as,

$$P_{\text{sw, boost}} = f_{\text{sw}}\left\{\left(I_a \sin(\omega t) + i_{\text{comp}} + \frac{\triangle i_{\text{L}_\text{a}}}{2}\right)(V_{\text{Ca}} t_{\text{on}} + V_{\text{SD}} t_{\text{off}}) + \left(I_{\text{a}} \sin(\omega t) + i_{\text{comp}} - \frac{\triangle i_{\text{L}_\text{a}}}{2}\right)(V_{\text{Ca}} t_{\text{off}} + V_{\text{SD}} t_{\text{on}})\right\} \tag{5.12}$$

where i_{comp} is the second-order current component and $\triangle i_{\text{L}_\text{a}}$ is the inductor current ripple. t_{on} and t_{off} are the ON and OFF time of the switches. From equations (5.11) and (5.12), the total switching losses $P_{\text{tot,sw}}$ of the inverter can be calculated as the sum of $P_{\text{sw, buck}}$ and $P_{\text{sw, boost}}$.

The conduction loss depends on the RMS current flowing through the switch $I_{\text{RMS,sw}}$, the on-state resistance $R_{\text{DS,on}}$ and the change in junction temperature $\triangle T_{\text{j}}$. It will vary according to the duty cycle of the switches $S_1 - S_8$. After applying the mathematical simplifications, the total conduction loss $P_{\text{tot,cond}}$ can be written as,

$$P_{\text{tot,cond}} = 2\left(\frac{R^*_{\text{DS,on}} A^*_{\text{sw}}}{A_{\text{sw}}}\right)(1 + \triangle T_{\text{j}})\left\{\left(I_{\text{a}}^2 \sin^2(\omega t) + i_{\text{comp}}^2 + \frac{\triangle i_{\text{L}_\text{a}}^2}{12}\right) + \left(I_{\text{a}}^2 \sin^2(\omega t + \pi) + i_{\text{comp}}^2 + \frac{\triangle i_{\text{L}_\text{b}}^2}{12}\right)\right\} \tag{5.13}$$

The power losses of the output capacitance C_{oss}, depending on the input voltage and the switching frequency, which can be expressed as,

$$P_{\mathrm{tot,C_{oss}}} = \left(\frac{C^*_{\mathrm{oss}} A_{\mathrm{sw}}}{A^*_{\mathrm{sw}}}\right)(2V_{\mathrm{in}}^2 + V_{Ca}^2 + V_{Cb}^2) f_{\mathrm{sw}} \tag{5.14}$$

The reverse recovery losses occur during the body diode transitions from the on-state to the off-state. For cascode devices, a small amount of reverse recovery losses occurs in the lower side switches which is not negligible. The total reverse recovery loss $P_{\mathrm{tot,rr}}$ is calculated as,

$$P_{\mathrm{tot,rr}} = \left(\frac{Q^*_{\mathrm{rr}} A_{\mathrm{sw}}}{A^*_{\mathrm{sw}}}\right)(2V_{\mathrm{in}} + V_{\mathrm{Ca}} + V_{\mathrm{Cb}}) f_{\mathrm{sw}} \tag{5.15}$$

The gate losses depend on the switching frequency, the gate-source voltage V_{GS} and the gate charge Q_{g}. The total gate loss of four switches $P_{\mathrm{tot,g}}$ is calculated as,

$$P_{\mathrm{tot,g}} = 8\left(\frac{Q^*_{\mathrm{g}} A_{\mathrm{sw}}}{A^*_{\mathrm{sw}}}\right) V_{\mathrm{GS}} f_{\mathrm{sw}} \tag{5.16}$$

In cascode GaN FETs, the body diode of the lower side switches incurred by the conduction loss during the reverse recovery time t_{rr} [121]. The total power loss $P_{\mathrm{tot,bd}}$ of the body diodes can be written as,

$$P_{\mathrm{tot,bd}} = 4V_{\mathrm{SD}} f_{\mathrm{sw}} t_{\mathrm{rr}} \left(I_{\mathrm{out}}(\sin(\omega t) + \sin(\omega t + \pi)) + 2i_{\mathrm{comp}}\right) \tag{5.17}$$

The volume of the switches is calculated as,

$$vol_{\mathrm{sw}} = 8h_{\mathrm{sw}} A_{\mathrm{sw}} \tag{5.18}$$

where h_{sw} is the height of the switch package.

The total cost of the switches is calculated as,

$$\Sigma_{\mathrm{switch}} = n_{\mathrm{switch}}\left(a_1 + b_1 I_{\mathrm{sw,\,rated}}\right) \tag{5.19}$$

where n_{switch} is the total number of switches, a_1 is the cost per switch £, b_1 is the cost per rated ampere (£/A) and $I_{\mathrm{sw,\,rated}}$ is the rated current of the switch (A).

5.4.2 Output Inductors

The inductor power losses consist of the core losses, the AC and DC losses which can be expressed as [122],

$$P_{\text{ind}} = a_{\text{L1}} f_{\text{sw}}^{\alpha} \Delta i_{\text{L}}^{\beta} + a_{\text{L2}} f_{\text{sw}} \Delta i_{\text{L}}^{\gamma} + a_{\text{L3}} I_{\text{a}}^{2} \Delta i_{\text{L}}^{\lambda} \tag{5.20}$$

where a_{L1}, α, and β are the Steinmetz coefficients; a_{L2} and a_{L3} are the constants, which are used to approximate the values of winding resistance; γ and λ are the real values, which are used to reduce the non-linearity.

The approximated inductor volume is calculated as,

$$vol_{\text{ind}} = a_{\text{L4}} L\left(I_{\text{peak,a}}^{2} + I_{\text{peak,b}}^{2}\right) + a_{\text{L5}} L\left(I_{\text{peak,a}} + I_{\text{peak,b}}\right) + a_{\text{L6}}\left(I_{\text{peak,a}} + I_{\text{peak,b}}\right) \tag{5.21}$$

$$I_{\text{peak,a}} = I_{\text{out}} \sin(\omega t) + i_{\text{comp}} + \frac{\Delta i_{\text{L}_\text{a}}}{2} \tag{5.22}$$

$$I_{\text{peak,b}} = I_{\text{out}} \sin(\omega t + \pi) + i_{\text{comp}} + \frac{\Delta i_{\text{L}_\text{b}}}{2} \tag{5.23}$$

where a_{L4}, a_{L5}, and a_{L6} are the polynomial coefficients of the inductor which must be a positive value. L is the inductor value ($L = L_{\text{a}} = L_{\text{b}}$). $I_{\text{peak,a}}$ and $I_{\text{peak,b}}$ are the peak current of the inductors.

The total cost of the inductors is calculated as,

$$\Sigma_{\text{inductor}} = a_2 + b_2 I_{\text{ind, rated}} \tag{5.24}$$

where a_2 is the constant cost £, b_2 is the cost per volume (£/cm^3) and $I_{\text{ind, rated}}$ is the rated current of the inductor.

5.4.3 Power Decoupling Capacitors

The power loss of the capacitor is calculated as,

$$P_{\text{cap}} = \frac{I_{\text{RMS,C}}^2 \tan\delta}{2\pi f_{2\omega} C} \tag{5.25}$$

where $I_{\text{RMS,C}}$ is the RMS current flow through the capacitor, $\tan\delta$ is the loss factor, $f_{2\omega}$ is the frequency of the second-order ripple power and C is the value of the capacitance.

In a practical design, the capacitance volume varies by different manufacturers. Consequently, an approximated model is used. The total box volume of the capacitors vol_{cap} are calculated as,

$$vol_{\text{cap}} = a_{\text{C1}} C\left(V_{\text{C}_\text{a}}^2 + V_{\text{C}_\text{b}}^2\right) + a_{\text{C2}} C\left(V_{\text{C}_\text{a}} + V_{\text{C}_\text{b}}\right) + a_{\text{C3}}\left(V_{\text{C}_\text{a}} + V_{\text{C}_\text{b}}\right) \tag{5.26}$$

where a_{C1}, a_{C2}, and a_{C3} are the polynomial coefficients of the capacitor which must be a positive value. C is the output capacitor ($C = C_{\text{a}} = C_{\text{b}}$). V_{C_a} and V_{C_b} are the voltage across the output capacitors. The output capacitor selection is the biggest challenge, which has a trade-off between the second-order ripple, power loss and volume. The details of the output capacitor selection are discussed in Section 3.3.

The total cost of the capacitors is calculated as,

$$\Sigma_{\text{capacitor}} = a_3 + b_3 V_{\text{rated}} + c_3 C_{\text{rated}} \tag{5.27}$$

where a_3 is the constant cost £, b_3 is the cost per rated voltage (£/V), c_3 is the cost per capacitance (£/μF) and C_{rated} is the rated value of capacitance (μF).

5.4.4 Heat Sinks

The volume of the heat sink is calculated as [123],

$$vol_{\text{heat sink}} = \frac{V_{\theta\text{SA}}}{P_{\text{D}}}\left(\Delta T_{\text{j}} - P_{\text{D}}\left(R_{\theta\text{JC}} + R_{\theta\text{CS}}\right)\right) \tag{5.28}$$

where $V_{\theta\text{SA}}$ is the volumetric resistance, P_{D} is the power dissipated by the GaN FETs, ΔT_{j} is the temperature difference between the junction and the ambient, $R_{\theta\text{JC}}$ is the thermal

resistance from junction-to-case of the semiconductor, and $R_{\theta CS}$ is the thermal resistance from case to the mounting surface of the semiconductor. The values of $R_{\theta JC}$ and $R_{\theta CS}$ are provided by the manufacturer.

The total cost of the heat sinks is calculated as,

$$\Sigma_{\text{heat sink}} = a_4 + b_4 vol_{\text{heat sink}} \tag{5.29}$$

where a_4 is the constant cost (£), b_4 is the cost per volume (£/cm^3) and $vol_{\text{heat sink}}$ is the volume of the heat sink.

5.5 Selection of Components

5.5.1 Voltage and Current Stress of the GaN FETs

The evaluation of voltage and current stress of the GaN FETs is used to select the optimal power rating of the devices. The voltage and current stress are calculated individually for both the buck and boot mode of the inverter. The voltage stress of the switches S_1, S_2 and S_5, S_6 depends on the input voltage, and the duty cycles D_{A} and D_{B}. The voltage stress of the switches S_3, S_4 and S_7, S_8 depends on the voltage across the output capacitors. Therefore, the maximum voltage stress on the switches $V_{\text{sw,max,buck}}$ and $V_{\text{sw,max,boost}}$ are represented as,

$$V_{\text{sw,max,buck}} = \begin{cases} V_{\text{in}} D_{\text{A,max}} \ \in \ S_1, S_2 \\ V_{\text{in}} D_{\text{B,max}} \ \in \ S_5, S_6 \end{cases} \tag{5.11}$$

$$V_{\text{sw,max,boost}} = \begin{cases} D_{\text{A}',\text{max}} \left(\frac{V_{\text{ab,max}}}{2} (1 + \sin \omega t) + v_{\text{comp}} \right) \ \in \ S_3, S_4 \\ D_{\text{B}',\text{max}} \left(\frac{V_{\text{ab,max}}}{2} (1 + \sin(\omega t + \pi)) + v_{\text{comp}} \right) \ \in \ S_7, S_8 \end{cases} \tag{5.12}$$

where $D_{\text{A,max}}$ and $D_{\text{B,max}}$ are the maximum duty cycles, and $V_{\text{ab,max}}$ is the maximum peak voltage. The switches S_1, S_2 and S_5, S_6 reach maximum voltage stresses at maximum duty cycles $D_{\text{A,max}}$ and $D_{\text{B,max}}$. Similarly, the switches S_3, S_4 and S_7, S_8 reach maximum voltage stresses at maximum peak voltage $V_{\text{ab,max}}$. However, the voltage stress on the switches S_1, S_2 and S_5, S_6 are reduced by half compared to S_3, S_4 and S_7, S_8.

The current stress depends on the maximum switching current flowing through the switches which differs for both the buck and boost mode. The maximum switching current of the buck mode $I_{\mathrm{sw,max,buck}}$ is calculated as,

$$I_{\mathrm{sw,max,buck}} = \begin{cases} \dfrac{V_{\mathrm{Ca}}(1-D_{\mathrm{A}})}{2f_{\mathrm{sw}}L_{\mathrm{a}}} + I_{\mathrm{a}} \\ \dfrac{V_{\mathrm{Cb}}(1-D_{\mathrm{B}})}{2f_{\mathrm{sw}}L_{\mathrm{b}}} + I_{\mathrm{b}} \end{cases} \tag{5.13}$$

Similarly, the maximum switching current of the boost mode $I_{\mathrm{sw,max,boost}}$ is calculated as,

$$I_{\mathrm{sw,max,boost}} = \begin{cases} \dfrac{V_{\mathrm{in}}D_{\mathrm{A}'}}{2f_{\mathrm{sw}}L_{\mathrm{a}}} + \dfrac{V_{\mathrm{Ca}}I_{\mathrm{a}}}{V_{\mathrm{in}}} \\ \dfrac{V_{\mathrm{in}}D_{\mathrm{B}'}}{2f_{\mathrm{sw}}L_{\mathrm{b}}} + \dfrac{V_{\mathrm{Cb}}I_{\mathrm{b}}}{V_{\mathrm{in}}} \end{cases} \tag{5.14}$$

where f_{sw} is the switching frequency of the inverter. I_{a} and I_{b} are the output currents. From equation (5.13) and (5.14), maximum switching current depends on the maximum inductor ripple current and the output current. The voltage and current rating of the GaN FETs is selected based on the voltage and current stress.

5.5.2 Selecting the Inductors

The inductors of the inverter should be selected to achieve both buck and boost mode because one inductor is shared for both modes. The allowable ripple current is one of the most important factors to be considered when selecting the inductor value. The higher value of the inductor reduces the ripple current, and the maximum output current can be achieved. However, a lower inductor value helps to reduce the design size. Therefore, the inductor value is selected with a low value and high current rating.

In buck mode, the selected inductor should satisfy the following condition,

$$L_{\mathrm{a}} > \frac{D_{\mathrm{A}}(V_{\mathrm{in}} - V_{\mathrm{Ca}})}{0.25f_{\mathrm{sw}}I_{\mathrm{a}}} \tag{5.15}$$

$$L_{\mathrm{b}} > \frac{D_{\mathrm{B}}(V_{\mathrm{in}} - V_{\mathrm{Cb}})}{0.25 f_{\mathrm{sw}} I_{\mathrm{b}}} \tag{5.16}$$

In boost mode, the selected inductor should satisfy the following condition,

$$L_{\mathrm{a}} > \frac{(1 - D_{\mathrm{A}'})^2 (V_{\mathrm{Ca}} - V_{\mathrm{in}})}{0.25 f_{\mathrm{sw}} I_{\mathrm{a}}} \tag{5.17}$$

$$L_{\mathrm{b}} > \frac{(1 - D_{\mathrm{B}'})^2 (V_{\mathrm{Cb}} - V_{\mathrm{in}})}{0.25 f_{\mathrm{sw}} I_{\mathrm{b}}} \tag{5.18}$$

For the given inverter topology, the inductor current ripple is allowed between 20% to 35% of the maximum output current. In addition, the inductor value can be minimised by optimising the switching frequency.

5.5.3 Selecting the Capacitors

In buck mode, the required capacitor is calculated as,

$$C_{\mathrm{a}} = \frac{0.5 (x I_{\mathrm{a}})^2 L_{\mathrm{a}}}{D_{\mathrm{A}} V_{\mathrm{in}} \Delta V_{\mathrm{Ca}}} \tag{5.19}$$

$$C_{\mathrm{b}} = \frac{0.5 (x I_{\mathrm{b}})^2 L_{\mathrm{b}}}{D_{\mathrm{B}} V_{\mathrm{in}} \Delta V_{\mathrm{Cb}}} \tag{5.20}$$

In boost mode, the required capacitor is calculated as,

$$C_{\mathrm{a}} = \frac{I_{\mathrm{a}} (V_{Ca} - V_{\mathrm{in}})}{2 f_{\mathrm{sw}} V_{\mathrm{Ca}} \Delta V_{\mathrm{Ca}}} \tag{5.21}$$

$$C_{\mathrm{b}} = \frac{I_{\mathrm{b}} (V_{Cb} - V_{\mathrm{in}})}{2 f_{\mathrm{sw}} V_{\mathrm{Cb}} \Delta V_{\mathrm{Cb}}} \tag{5.22}$$

where x is the coefficient that determines the amount of ripple presented in the output current. The output capacitor needs to handle the second-order ripple components diverted from the DC bus. Therefore, the output capacitors are selected to have a much higher value with a high voltage rating.

5.6 ANN-based Design Approach

The ANN-based design of the buck-boost inverter is discussed. The design approach is developed using the mathematical models from the previous section. Initially, the datasets are generated using the mathematical models to train the network. Figure 5.4 shows the flow chart that was used to generate the training datasets. The switching frequency, area of the switch, inductor current ripple, and change of temperature are considered as inputs of the ANN. The efficiency, power density and specific cost are considered as the targets. Figure 5.5 shows the structure of ANN for the proposed design approach.

5.6.1 Training the Network

The training consists of four steps, which are the feed-forward computation, the error back-propagation, and the updating weights. The details of these steps follow:

Feed-forward computation

In this step, the inputs, targets, and weights of the networks are initialised. The initial values of the weights are assigned randomly, and they will update on the next iteration. At the end of the computation, the derivative of the network function (tangent sigmoid function) is evaluated and stored in the memory of each unit.

Error back-propagation

After the feed-forward computation, the fitness of the network is evaluated using the back-propagation error of the stored value. The back-propagation error of the output layer is calculated as,

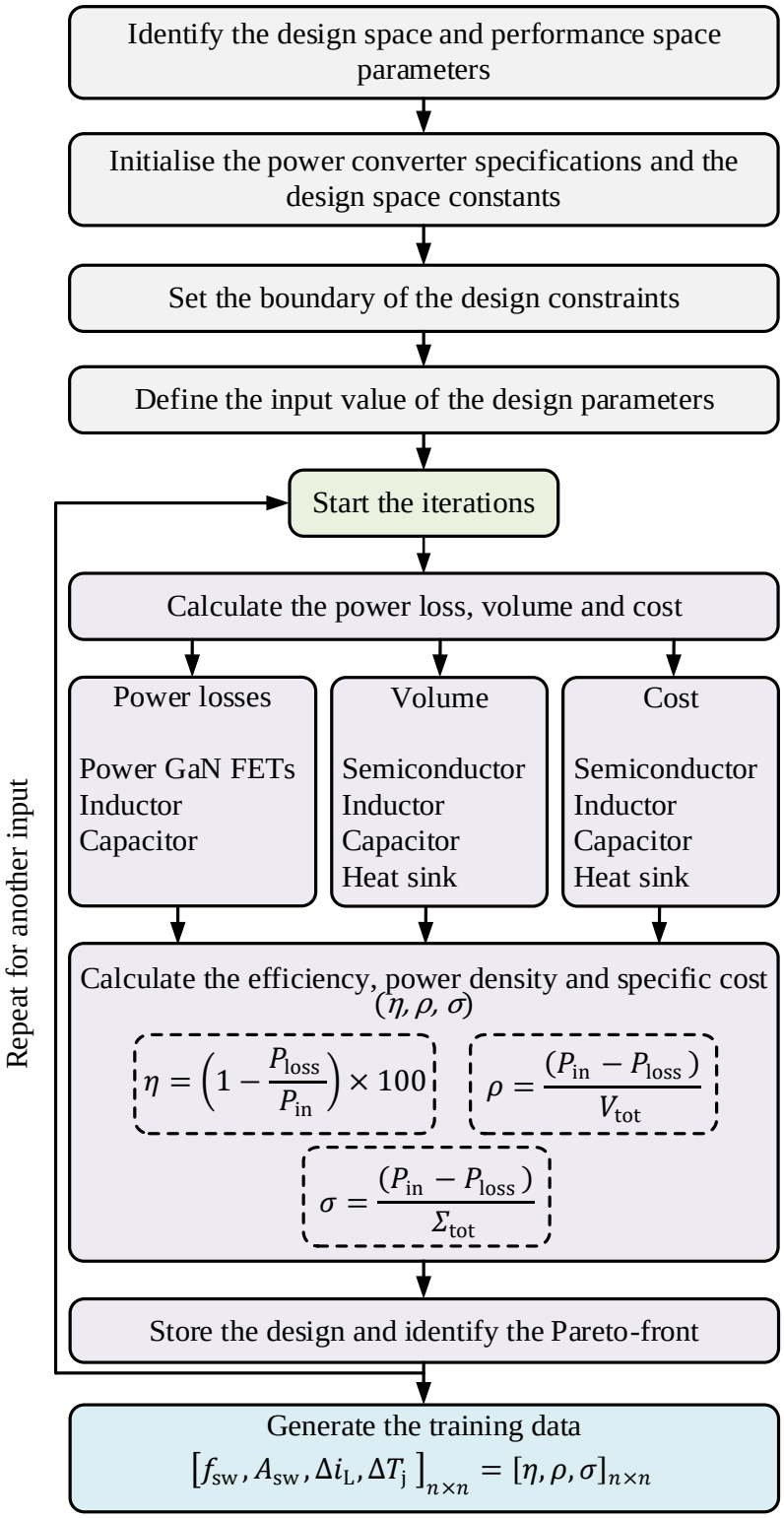


Figure 5.4: Flow diagram of the proposed design approach.

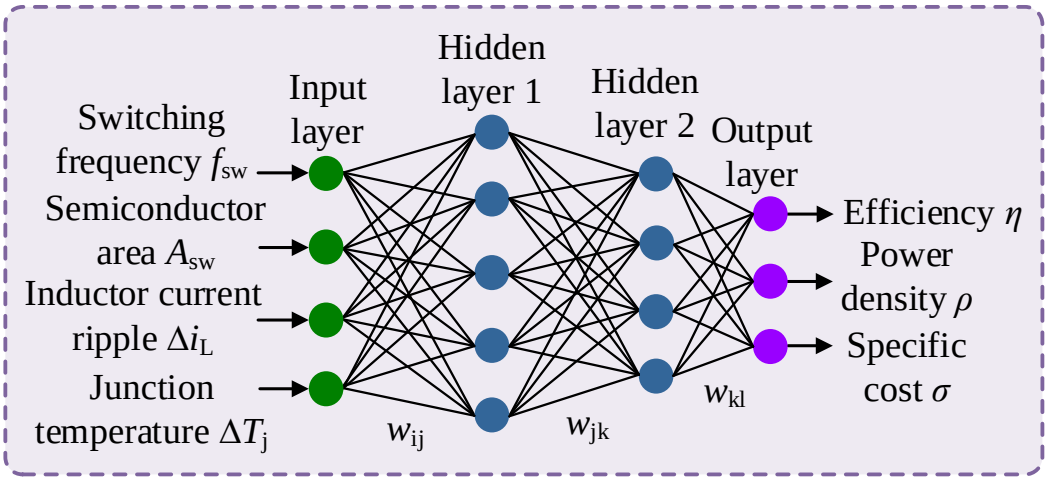


Figure 5.5: Structure of the ANN for the proposed design approach.

$$z_{l,error} = z_{l,out}(1 - z_{l,out})(z_{l,target} - z_{l,out}) \tag{5.29}$$

where $z_{l,error}$ is the error of output layer, $z_{l,out}$ is the actual output, and $z_{l,target}$ is the target output.

Two hidden layers y_k and y_j are used. The back-propagation error of the hidden layer $y_{k,error}$ is calculated as,

$$y_{k,error} = y_{k,out}(1 - y_{k,out}) \sum_{k=1}^{n} w_{jk}\, y_j \tag{5.29}$$

where $y_{k,out}$ is the actual output, and w_{jk} is the weight of the hidden layer.

Updating weight

The new weight is determined by the values of the old weight $w_{kl,old}$ and the change of weight. The change of weight is calculated by the partial derivative of the network error with a learning factor. The change of weight and the new weight of the output layer are calculated as,

$$\Delta w_{\mathrm{kl}} = \xi z_{\mathrm{l,error}} y_{\mathrm{k}} \tag{5.29}$$

$$w_{\mathrm{kl,new}} = w_{\mathrm{kl,old}} + \Delta w_{\mathrm{kl}}$$

The change of weight of the hidden layers are updated as,

$$\Delta w_{\mathrm{jk}} = \xi y_{\mathrm{k,error}} y_{\mathrm{j}} \tag{5.29}$$

$$\Delta w_{\mathrm{ij}} = \xi y_{\mathrm{j,error}} x_{\mathrm{i}}$$

where ξ is the learning rate, which decides the step length of the weight correction. After the training process, the fitness of the network is evaluated. Once the evaluation is completed, the network is suitable to predict the inverter design parameters for any given input.

5.7 Design of the Controllers

Figure 5.6 shows the control diagram of the buck-boost inverter. The controllers are classified into the voltage controller $K_V(s)$, inductor current controller $K_I(s)$ and second-order ripple controller $K_{2\omega}(s)$. PR controller is used to design the controllers. The transfer function of the PR controller is represented as,

$$K(s) = k_p + \sum_{r=1,2,3,4,5,\ldots} \frac{2k_r s}{s^2 + \omega_r^2} \tag{3.28}$$

where k_p and k_r are the proportional and resonant voltage controller gains. Meanwhile, r is the target frequency. ω_r is the resonant frequency. The detailed design of the controller is presented in Section 3.5.

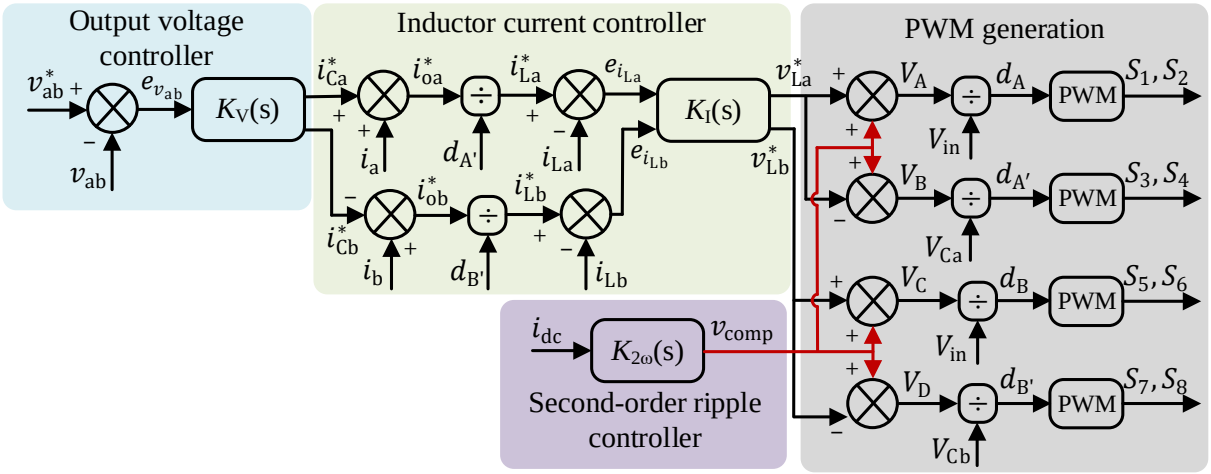


Figure 5.6: Control diagram of the buck-boost inverter.

The output voltage controller is used to regulate the voltage across the load. The target frequency is selected to track the fundament frequency and eliminate the odd and even harmonics. The current controller is used to control the output current and the inductor current. The target frequency of the current controller is selected to track the fundament frequency and eliminate the odd harmonics. The second-order ripple controller acts as a decoupling controller, which controls the second-order ripple in the DC-link current. The ripple controller is used to reduce the second-order ripple and the residuals of the second-order ripple on the DC-link current. Therefore, the target frequency of the decoupling controller is selected to eliminate the even harmonics.

5.8 Results and Discussions of Buck-boost Inverter

5.8.1 Performance Evaluation

The ANN-based design approach was implemented in MATLAB/Simulink and verified with a 1 kW GaN-based inverter. The feed-forward network was trained using 2000 design data, which were obtained from the mathematical models. For each design data, the corresponding

efficiency, power density and specific cost are obtained. The dataset was used in different ways to train, validate, and test the network. Out of 2000 data, 30% of the data are used for training, 10% of the data are used for validation and the remaining 60% data are used for testing. The minimum and maximum values of the design parameters $f_{\text{sw,min}}$, $f_{\text{sw,max}}$, $\Delta i_{\text{L,min}}$, $\Delta i_{\text{L,max}}$, $A_{\text{sw,min}}$, $A_{\text{sw,max}}$, $\Delta T_{\text{j,min}}$, and $\Delta T_{\text{j,max}}$ are given in Table 5.1. The coefficients of components cost models are given in Table 5.2. The coefficients are calculated based on the current market price of the components [125], [126]. The combinations of the design parameters are applied to the network and the corresponding performance parameters are mapped into a 2D space. The Pareto-front response is plotted using these performance parameters, which provides the trade-off between the performance parameters. The obtained design can provide a large degree of freedom to choose the required design parameters, such as switching frequency, the value of the passive components and the semiconductor area.

Table 5.1: Design constraints of the inverter

Design variable	**Min. value**	**Max. value**
Switching frequency f_{sw}	10 kHz	200 kHz
Current ripple Δi_{L}	$0.1I_{\text{out,max}}$	$0.45I_{\text{out,max}}$
Switch area A_{sw}	$0.94A_{sw}^{*}$	$1.07A_{sw}^{*}$
Change in temperature ΔT_{j}	1°C	25°C

Table 5.2: Cost coefficients of the components

Switch		**Inductor**		**Capacitor**			**Heat sink**	
a_1	b_1	a_2	b_2	a_3	b_3	c_3	a_4	b_4
4.5	3.9	1.23	0.5	-7.6	0.5	0.0032	0.056	0.045

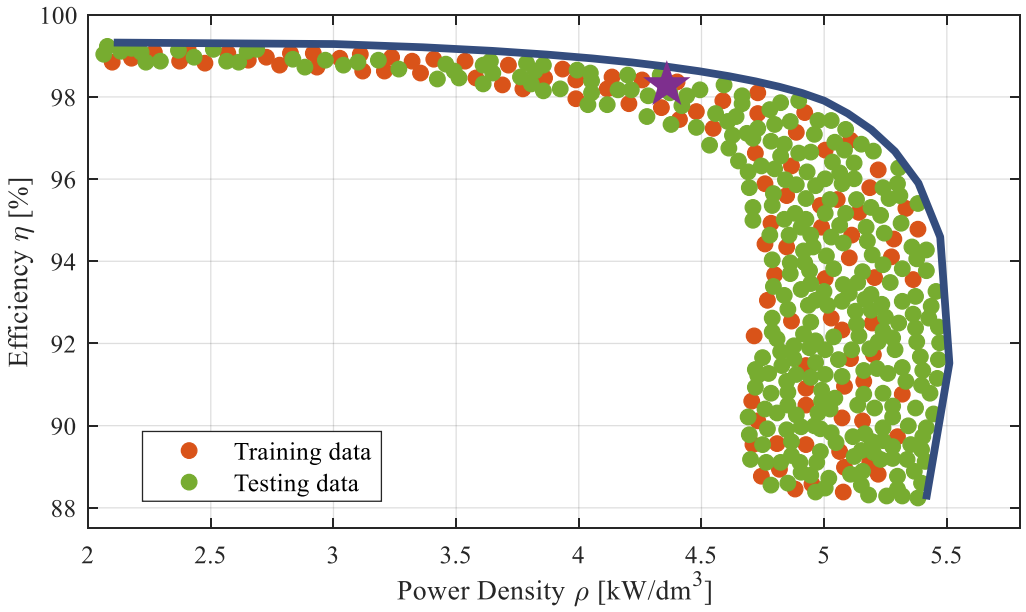


Figure 5.7: Efficiency vs. Power density of the buck-boost inverter.

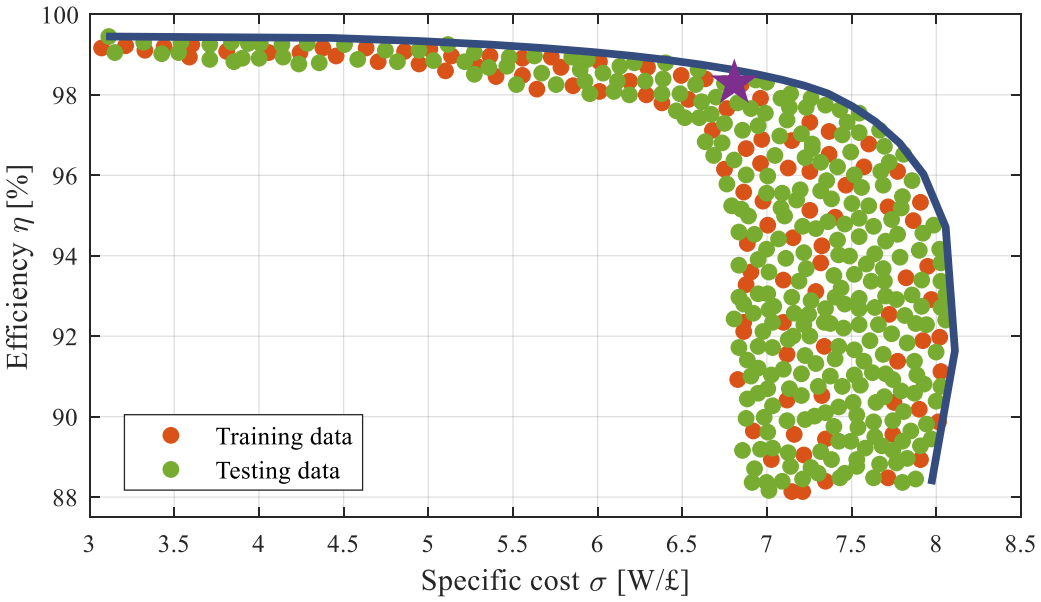


Figure 5.8: Efficiency vs. Specific cost of the buck-boost inverter.

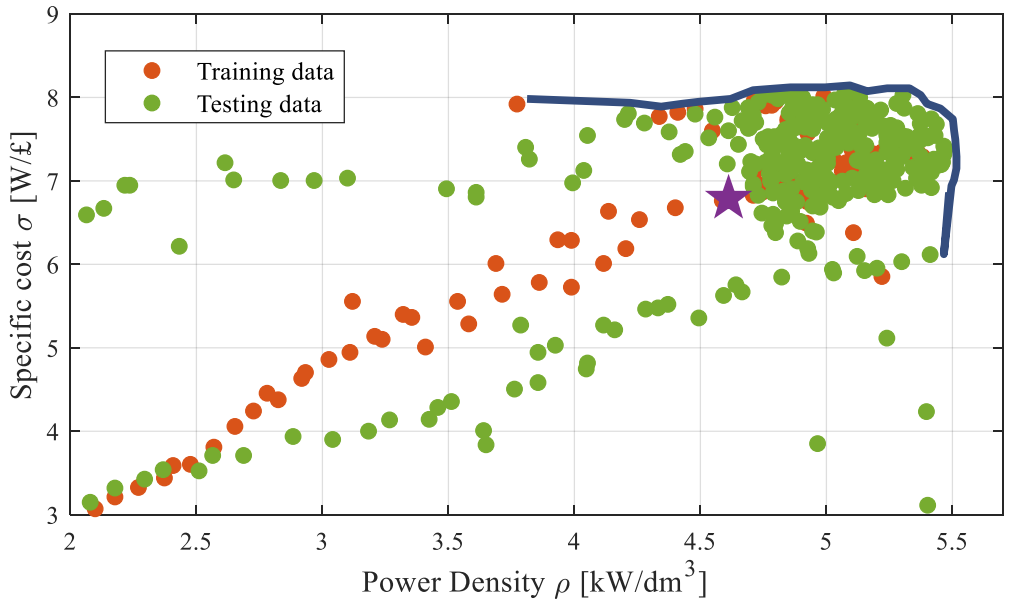


Figure 5.9: Specific cost vs. Power density of the buck-boost inverter.

The Pareto-front ($\eta - \rho - \sigma$) performance of efficiency, power density and specific cost of the power inverter is next examined. Figure 5.7 shows the performance of the efficiency and power density of the inverter. Figure 5.8 shows the performance of the efficiency and specific cost of the inverter. Figure 5.9 shows the performance of the specific cost and power density of the inverter. Figure 5.10 shows the performance of the efficiency, power density, and specific cost of the inverter. From these figures, it can be seen that the trade-off between the efficiency specific cost, and power density have differed as the design variables have changed. To validate the proposed inverter, one design is selected for the given application criteria. The efficiency, power density and specific cost of the selected design are obtained as $\eta = 98.3\%$, $\rho = 4.36\,\mathrm{kW/dm^3}$ and $\sigma = 6.8\,\mathrm{W/£}$. For the design, the power losses, volume, and cost are obtained as 17.01W, 225.53cm^3 and £144.4. The power losses, volume, and cost breakdown of each component are given in Figs. 5.11(a), (b) and (c). With the total power losses 17.01W, switches contributed 58%, inductors contributed 30% and capacitors contributed 12%. With the total volume 225.53cm^3, heat sinks occupied 38%, switches occupied 6%, inductors occupied 30%, and capacitors occupied 26%. Similarly, with the total cost £144.4, heat sinks added 11%, switches added 45%, inductors added 23% and capacitors

added 23%. The performance study gives an understanding of the power losses, volume, and cost of the inverter before going to the prototype. In addition, this design method is more flexible in comparison to other designs.

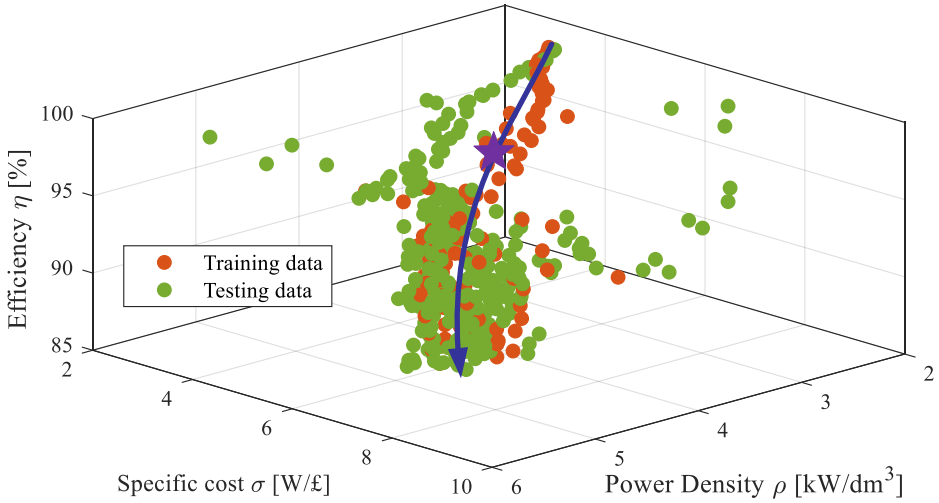
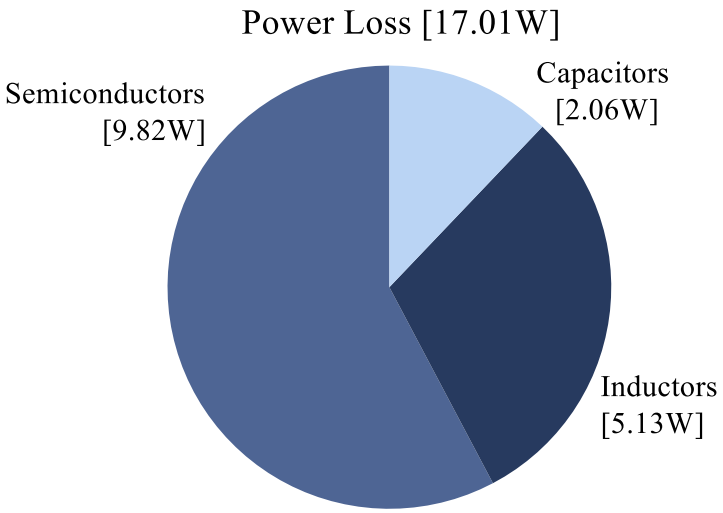
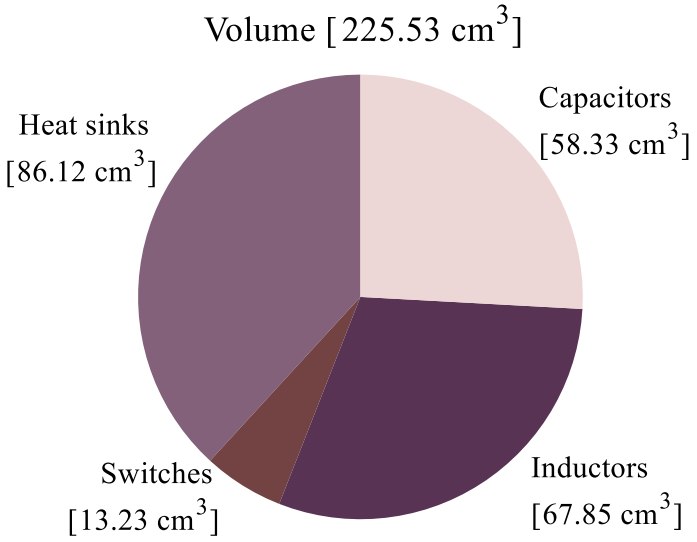


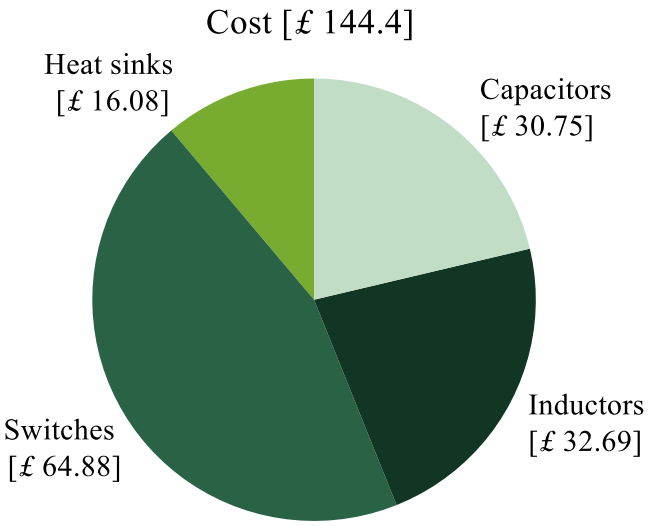
Figure 5.10: Efficiency vs. Specific cost vs. Power density of the buck-boost inverter.



(a)



(b)



(c)

Figure 5.11: (a) Power loss, (b) Volume, and (c) Cost breakdown of buck-boost inverter.

5.8.2 Simulation Verifications

The performance of the buck-boost inverter was verified using simulation results. The inverter and the controller are implemented in MATLAB/Simulink. The simulation parameters for 1kW design are given in Table 5.3. Then, the simulation results of the buck-boost inverter are verified, both without and with enabling the second-order ripple controller. Figs. 5.12 and 5.13 show the response of the input voltage V_{in}, DC-link current i_{dc}, output voltage v_{ab}, output current i_{a}, capacitor voltage V_{Ca}, capacitor voltage V_{Cb}. The input voltage V_{in} is changed from 250V to 300V, which does not affect the inverters output due to the buck-boost features. The results ensured that the inverter operates at low voltage without using any DC-DC converters.

Table 5.3: Simulation parameters of the buck-boost inverter

Parameters	Values
Input voltage V_{in}	250V
Output voltage v_{ab}	230V
Line frequency f	50Hz
Switching frequency f_{sw}	100kHz
Inductors L_{a} and L_{b}	150 μH
Capacitors C_{a} and C_{b}	60 μF

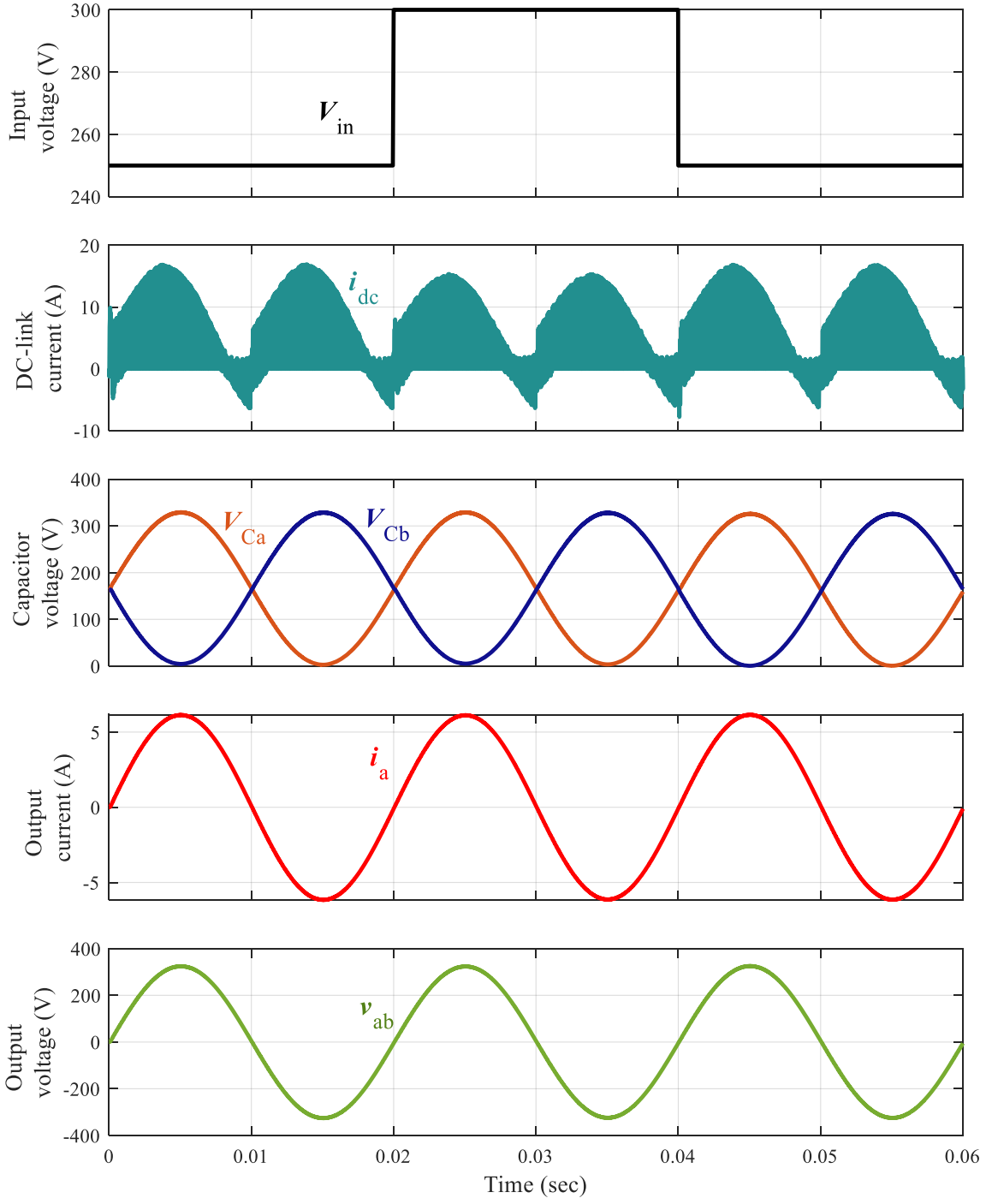


Figure 5.12: Simulation results of the buck-boost inverter without second-order ripple controller.

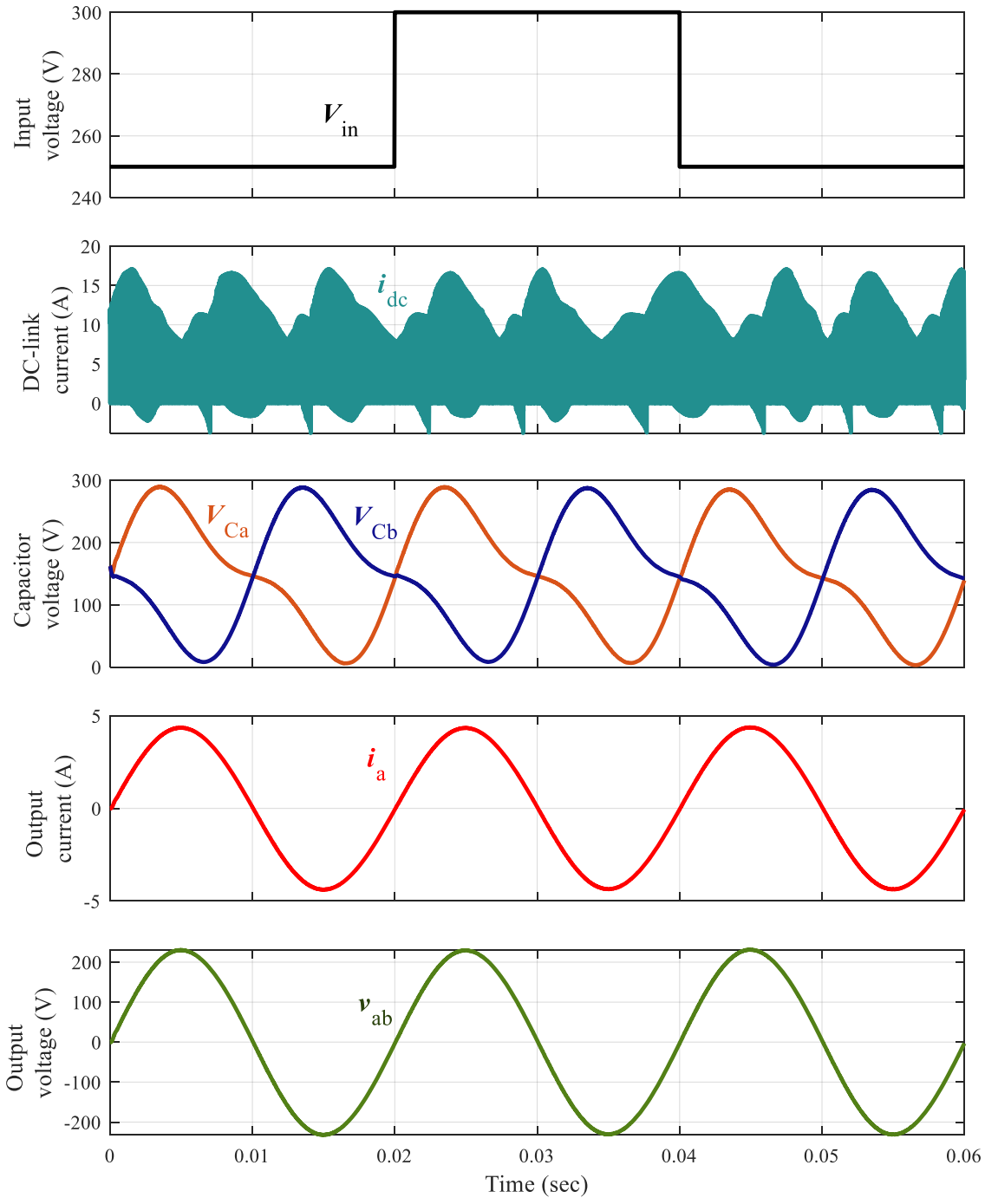


Figure 5.13: Simulation results of the buck-boost inverter with second-order ripple controller.

The ripple elimination capability of the buck-boost inverter is evaluated using a low pass filter. The low pass filter measures the 100Hz components in the DC-link current. Fig 5.14 shows the comparison results of the magnitude of the second-order ripple, both with and without using the ripple controller. From this figure, it can be seen that the amplitude of second-order ripple in the DC-link current Δi_{dc} is 6.25A and 5.2A for the input voltage 250V and 300V. This is reduced to 0.93A and 0.49A after enabling the ripple controller, which is 7 and 11 times lower than without using the ripple controller. Therefore, this advantage has prevented the need for large DC-link capacitors.

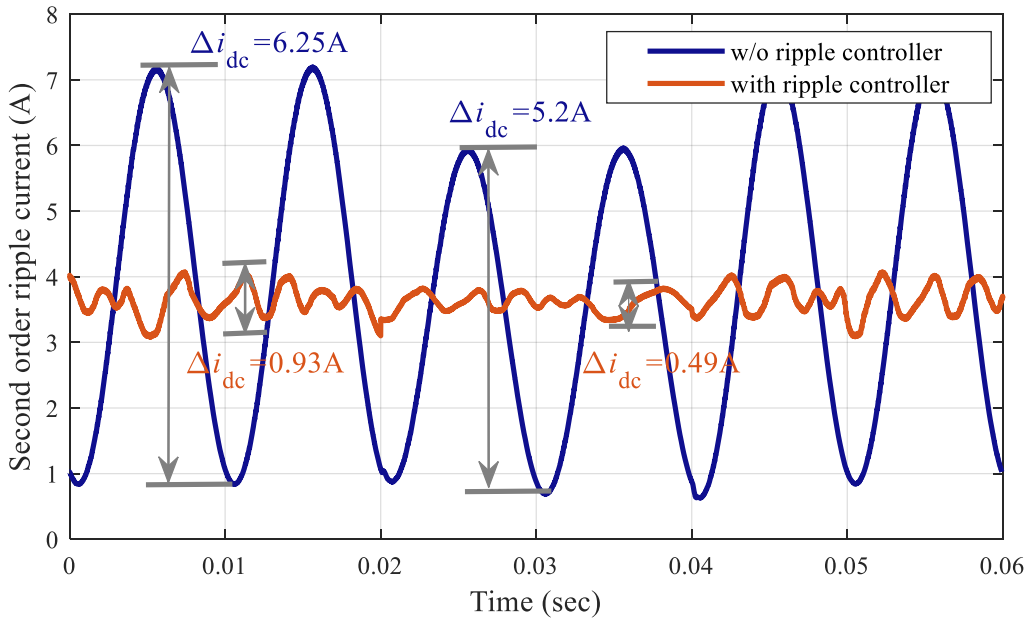


Figure 5.14: Comparison of the second-order ripple on the DC-link current.

5.9 Summary

This chapter introduced a high efficiency, high-power density, and low-cost single-stage GaN-based buck-boost inverter with a power decoupling function. The detailed operation of the inverter was explained using the key waveform and the mode of operations. Detailed mathematical modelling of the power loss, volume, and cost of all the components of the inverter was presented. An ANN-based optimal design approach was used to select a high

efficiency, high-power density, and low-cost design. The voltage and current stress of the switches and the procedure to choose the components are discussed. The control scheme of the inverter and the objectives of the controller were then discussed. The Pareto-front performance of efficiency, power density and specific cost was obtained for a different set of design requirements, which helps to understand the trade-off between the performance measures. This allows inverter designers to quickly identify the optimum design parameters without negotiating much of the inverters total power loss, volume, and design cost. A simulation study was then presented to evaluate the performance of the inverter. Consequently, the second-order ripple elimination proficiency of the inverter was verified, which reduces ripple in DC-link current more than 10 times.

Chapter 6 Experimental Verifications of Buck-boost Differential Inverters

6.1 Introduction

The inverter topology that was introduced in the previous chapter will be experimentally verified. The experiment is performed in both standalone and grid-connected systems. A 1kW prototype is developed to evaluate the standalone operations and a 1.8kW prototype is developed to evaluate grid-connected operations. Finally, the proposed buck-boost inverter is compared with existing buck-boost inverter topologies.

The rest of the chapter is organised as follows. Section 6.2 will give an overview of the experimental system. Section 6.3 will discuss the experiments of the standalone system and the outcome. Then, Section 6.4 will describe the experiments of the grid-connected systems, the grid-connected controller, and the performance. Finally, Section 6.5 will present a comparison study of the proposed buck-boost.

6.2 Overview of Experimental Systems

Figure 6.1 gives an overview of the experiments for both standalone and grid-connected systems. The experimental system consists of a DC-source simulator, GaN inverter, power amplifier, resistive load, power analyser and oscilloscope. The devices that are used for the experiments are listed in Table 6.1. The DC-source simulator produces the input voltage to the inverter. The GaN inverters are controlled by a Texas Instrument (TI) controller to achieve the control objectives. The controller is implemented in MATLAB/Simulink and the C code is generated to deploy into the hardware. The code is generated using the Simulink

build option. Then, the generated code is compiled in code composer studio (CCS) software once ensured the communication between the control card (TI Delfino F2837xD) and the computer. The power amplifier is used to achieve the grid-connected systems and the resistive load us used for standalone systems. The current and voltage signals of the inverter are measured using the Tektronix oscilloscope. A high precision power analyser is used to measure the efficiency and the output current harmonics of the inverter.

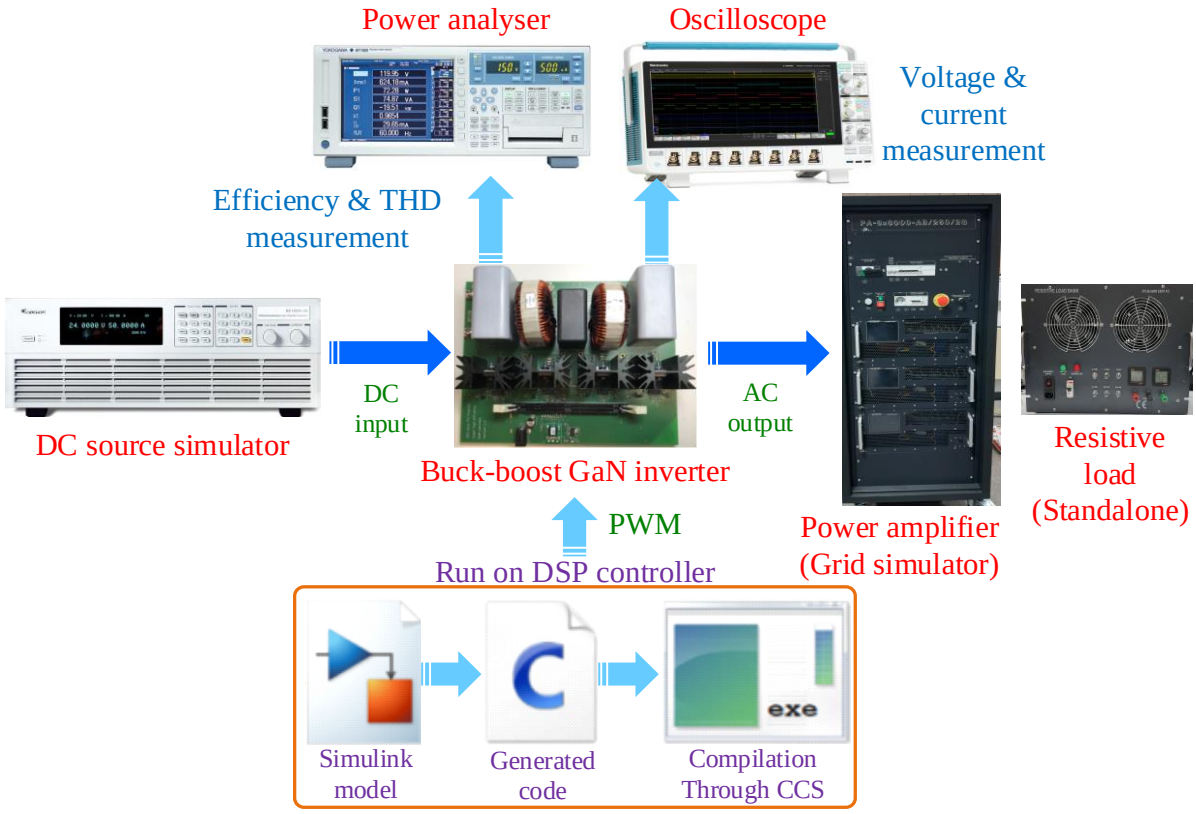


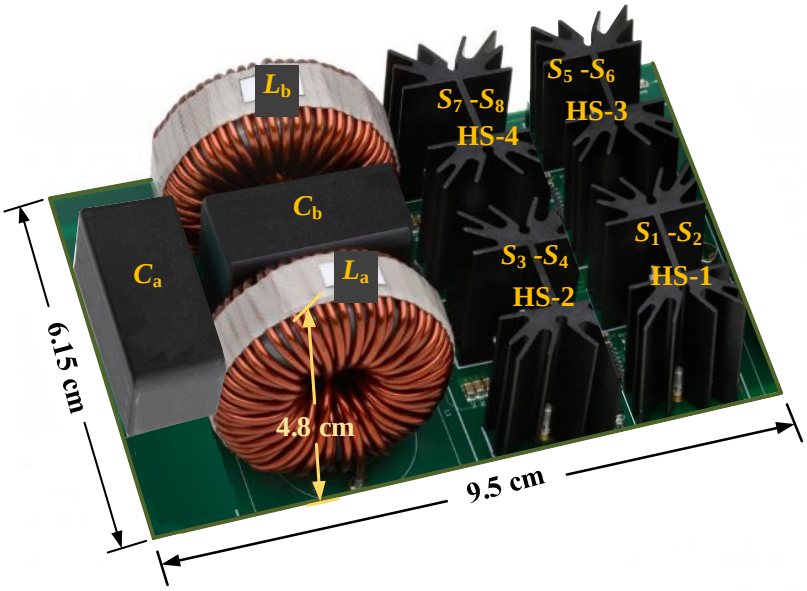
Figure 6.1: Overview of the experimental systems.

Table 6.1: Experimental device and type

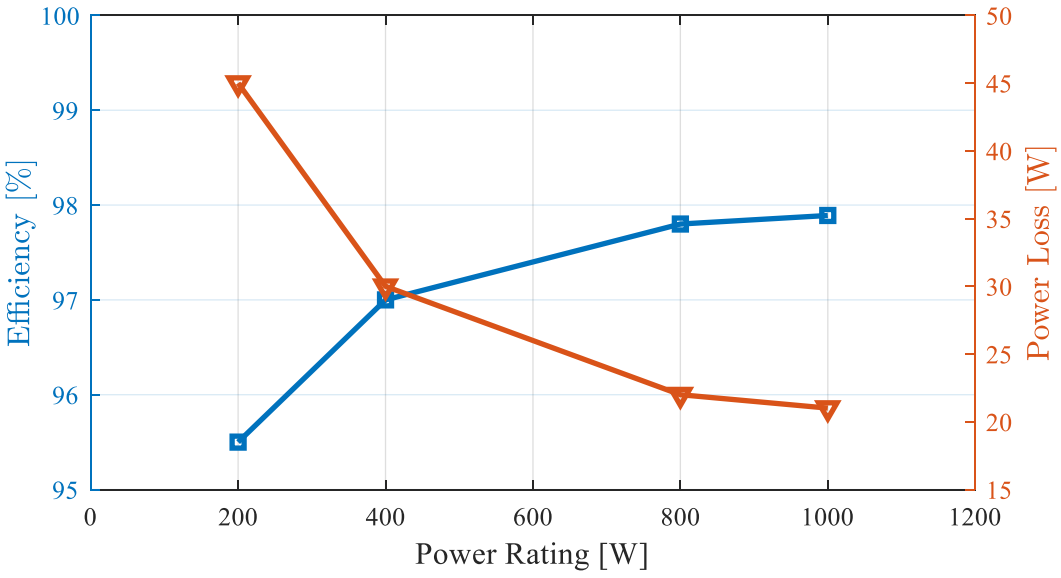
Device	Type
DC source simulator	MODEL 62000H-S SERIES
GaN inverter	1kW and 1.8kW
TI controller	Delfino F2837xD
Power amplifier	PA-3x3000-AB/260/2G
Resistive load	FFLB-5KW 230V
Power analyser	Yokogawa WT1800
Oscilloscope	Tektronix 8-channel MSO58

6.3 Experimental Verification of Stand-alone Systems

For verification, the 1kW prototype of the buck-boost inverter has been built using the results obtained by the design method presented in the previous chapter. Figure 6.2(a) shows the prototype of the selected design. A 900 V GaN FET (TP90H180PS) was used to build the prototype, which is manufactured by Transphorm. Meanwhile, P11T60 series of high current toroid type fixed inductors were used, which were designed by MPS Industries. MKP1848C series polypropylene film capacitors from Vishay BC Components were used. The value of the inductor is $L_a = L_b = 440\mu$H, the capacitor is $C_a = C_b = 60\mu$F and the switching frequency is $f_{\text{sw}} = 50$kHz. The prototype was examined at different output power levels to obtain the response of efficiency vs output power, and power loss vs output power, which are given Figure 6.2(b). It has been observed that the maximum efficiency of the prototype is 97.89%. The power density is obtained as 3.5kW/dm^3 from the volume of the inverter, which is given in Figure 6.2(a). The components cost of the prototype is £136.16. Compared to the outcome of the design method, the efficiency and power density and cost error obtained are only 0.4%, 0.86kW/dm^3 and £8.24.



(a)



(b)

Figure 6.2: Buck-boost inverter: (a) Hardware prototype, and (b) Efficiency and power loss.

The power decoupling capability of the proposed design is then verified, both with and without using the second-order ripple controller. Figure 6.3 shows the experimental results of

the input voltage V_{in}, DC-link current i_{dc}, output voltage v_{ab}, output current i_a, and decoupling capacitor voltages V_{Ca}, V_{Cb} before and after enabling the second-order ripple controller. Figs. 6.4 and 6.5 shows the experimental results of input voltage V_{in}, DC-link current i_{dc}, output voltage v_{ab}, output current i_a, and decoupling capacitor voltages V_{Ca}, V_{Cb} without and with a second-order ripple controller. The input voltage of the inverter is 300V. The amplitude of the ripple was reduced after enabling the second-order ripple controller. The elimination capability of the proposed prototype is quantified using the FFT approach. The FFTs of the DC-link current with and without using the ripple controller are given in Figure 6.6. In Figure 6.6, the amplitude of second-order ripple in the DC-link current is 1.52A, which is reduced to 0.31A after using the ripple controller. The FFT results ensured that the proposed prototype performed well against the second-order ripple without affecting the output current.

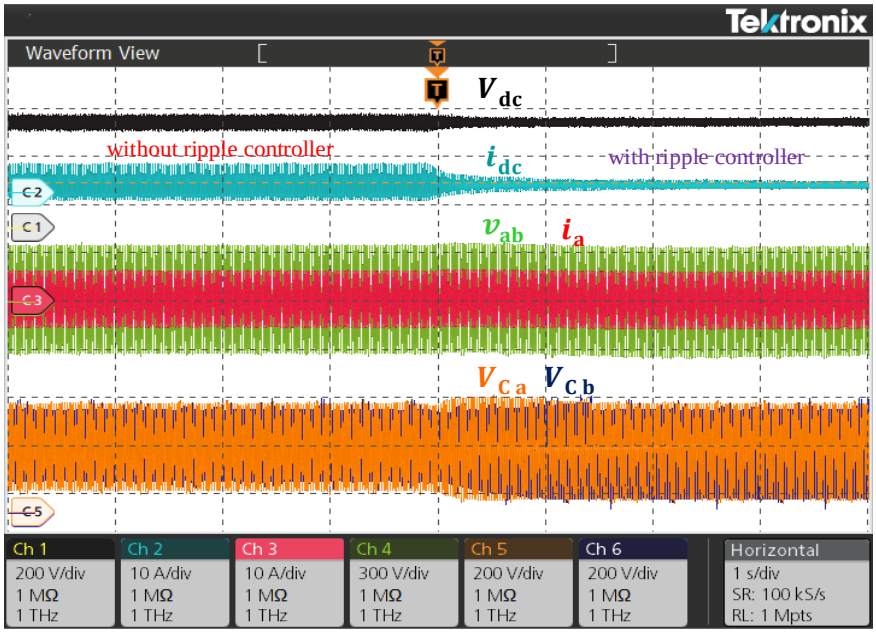


Figure 6.3: Experimental results of the standalone system at 1kW before and after enabling second-order ripple controller (V_{in}: 200V/div, i_{dc}, i_a: 10A/div, v_{ab}: 300V/div, V_{ca}, V_{cb}: 200V/div).

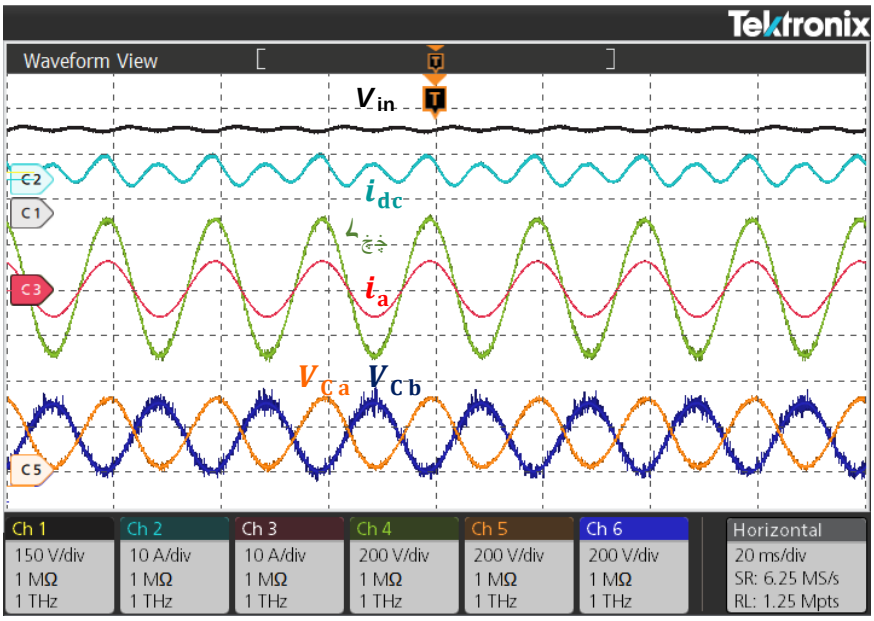


Figure 6.4: Experimental results of the standalone system at 1kW without second-order ripple controller (V_{in}: 150V/div, i_{dc}, i_a: 10A/div, v_{ab}, V_{ca}, V_{cb}: 200V/div).

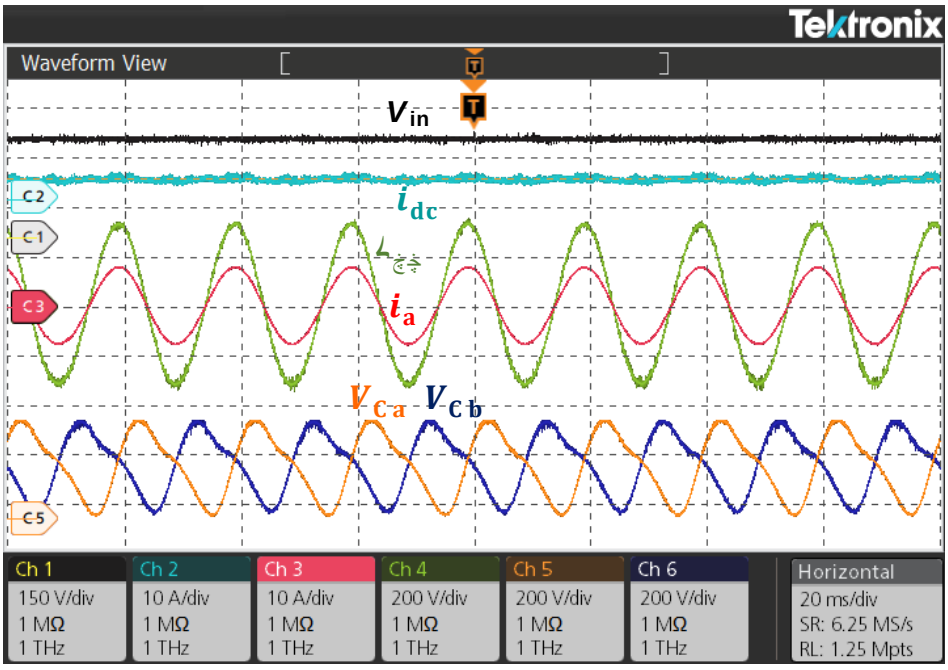


Figure 6.5: Experimental results of the standalone system at 1kW with second-order ripple controller (V_{in}: 150V/div, i_{dc}, i_a: 10A/div, v_{ab}, V_{ca}, V_{cb}: 200V/div).

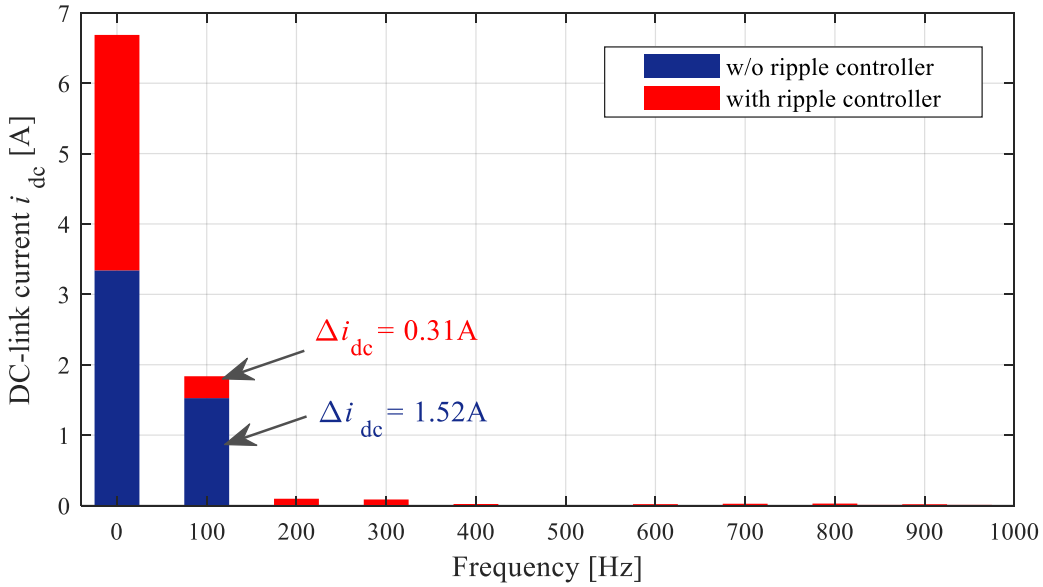


Figure 6.6: FFTs of the DC-link current with and without second-order ripple.

6.4 Experimental Verification of Grid-connected Systems

The grid-connected experiment of the inverter is conducted using a 1.8kW prototype. The 650V GaN FET (TP65H035WS) was used to build the prototype. The value of the inductor is $L_a = L_b = 440\mu$H, capacitor is $C_a = C_b = 80\mu$F and switching frequency is $f_{sw} = 50$kHz. Figure 6.7 shows the 1.8kW prototype of the inverter. Figs. 6.7 and 6.8 show the prototype and grid-control of the buck-boost inverter. Using the prototype, the power decoupling feature of the inverter is verified with and without using the second-order ripple controller.

Figure 6.9 shows the experimental results of the input voltage V_{in}, DC-link current i_{dc}, output voltage v_{ab}, output current i_a, and decoupling capacitor voltages V_{Ca}, V_{Cb} without second-order ripple controller. Meanwhile, Figure 6.10 shows the experimental results of input voltage V_{in}, DC-link current i_{dc}, output voltage v_{ab}, output current i_a, and decoupling capacitor voltages V_{Ca}, V_{Cb} with second-order ripple controller. As already discussed, the second-order ripple in the DC-link current is reduced after enabling the ripple controller. The wide voltage operation of the inverter is then verified by changing the input voltage from 300V to 400V. After increasing the voltage, the performance of the inverter is not affected.

This confirms that the inverter performed well in both buck and boost mode. Figure 6.11 shows the responses of the inverter after changing the input voltage.

The efficiency of the inverter is calculated for different power ratings. The maximum efficiency of the inverter is 97.78% at 990W. Figure 6.12 shows the power analyser results of maximum efficiency. The European efficiency of the inverter is then calculated. Figure 6.13 shows the response of the European efficiency. The European efficiency of the inverter is calculated as 96.3%. Furthermore, the European efficiency is an averaged operating efficiency over a yearly power distribution corresponding to the middle-European climate. This was proposed by the Joint Research Center (JRC/Ispra), based on the Ispra climate (Italy), and is now referenced on almost any inverter datasheet. The European efficiency is calculated as follows [127]:

$$\text{Euro Eff} = 0.03\text{Eff}_{5\%} + 0.06\text{Eff}_{10\%} + 0.13\text{Eff}_{20\%} + 0.1\text{Eff}_{30\%} + 0.48\text{Eff}_{50\%} + 0.2\text{Eff}_{100\%} \quad (6.1)$$

where $\text{Eff}_{5\%}$ is 5% of the nominal power.

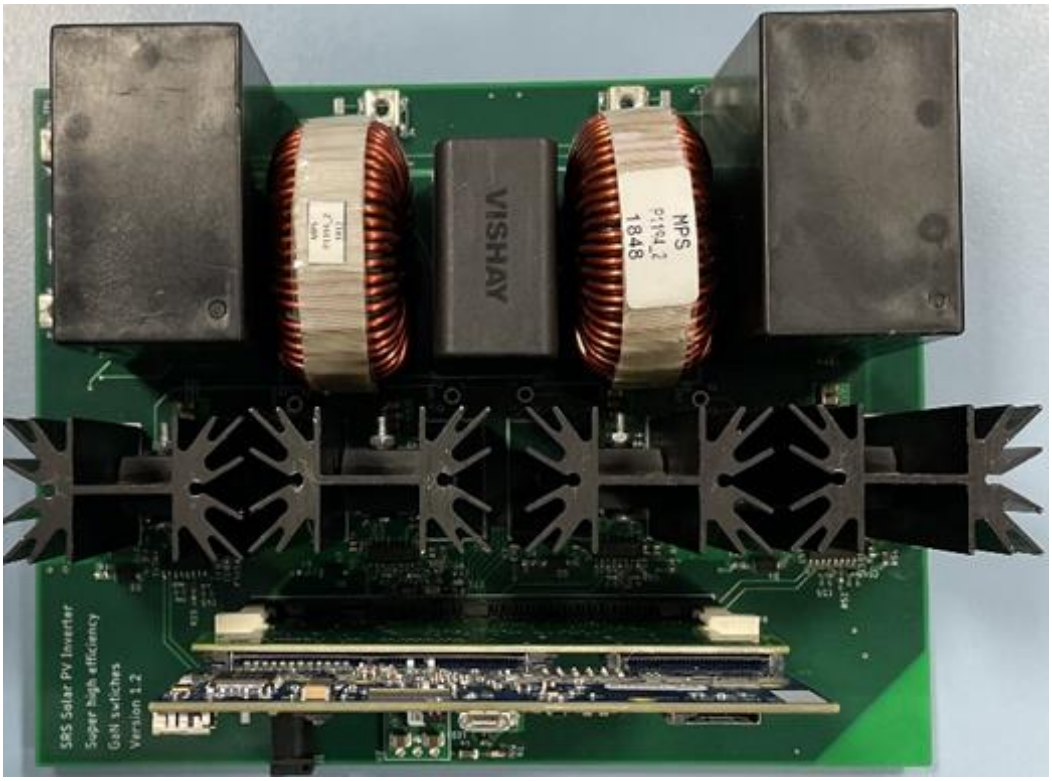


Figure 6.7: Prototype of the buck-boost inverter (1.8kW).

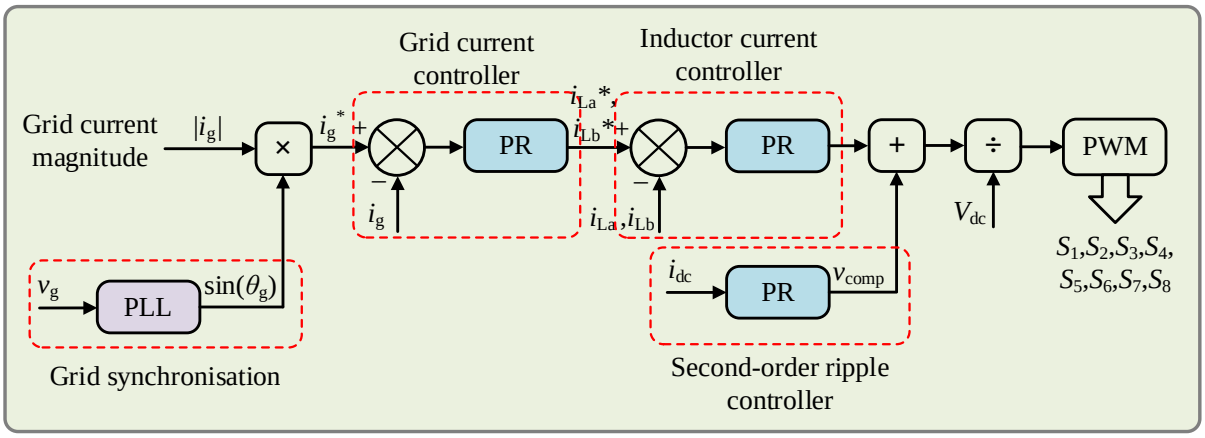


Figure 6.8: Grid-connected controller for a buck-boost inverter.

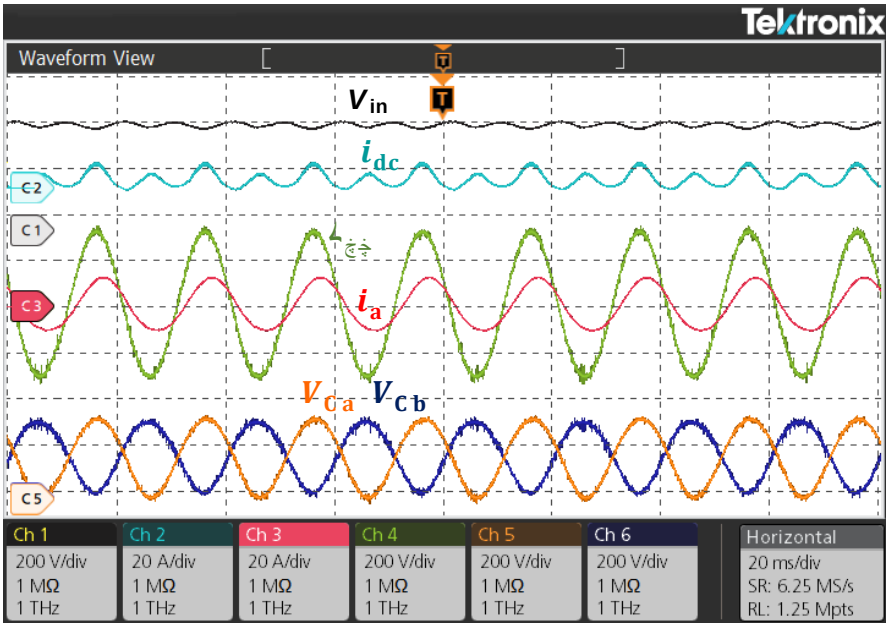


Figure 6.9: Experimental results for a grid-connected system at 1.8kW without a second-order ripple controller (V_{in}: 200V/div, i_{dc}, i_a: 20A/div, v_{ab}, V_{ca}, V_{cb}: 200V/div).

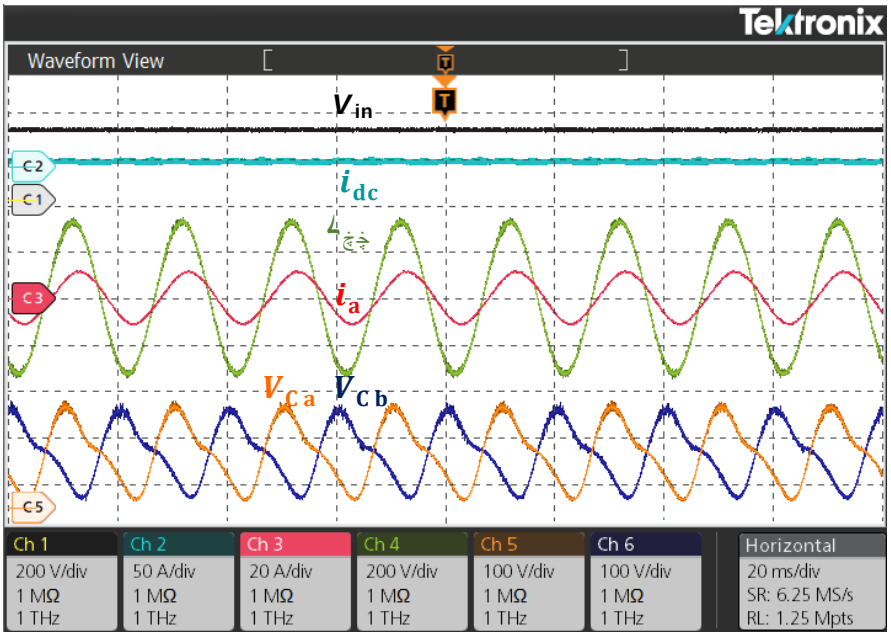


Figure 6.10: Experimental results for a grid-connected system at 1.8kW with a second-order ripple controller (V_{in}: 200V/div, i_{dc}: 50A/div i_a: 20A/div, v_{ab}: 200V/div, V_{ca}, V_{cb}: 100V/div).

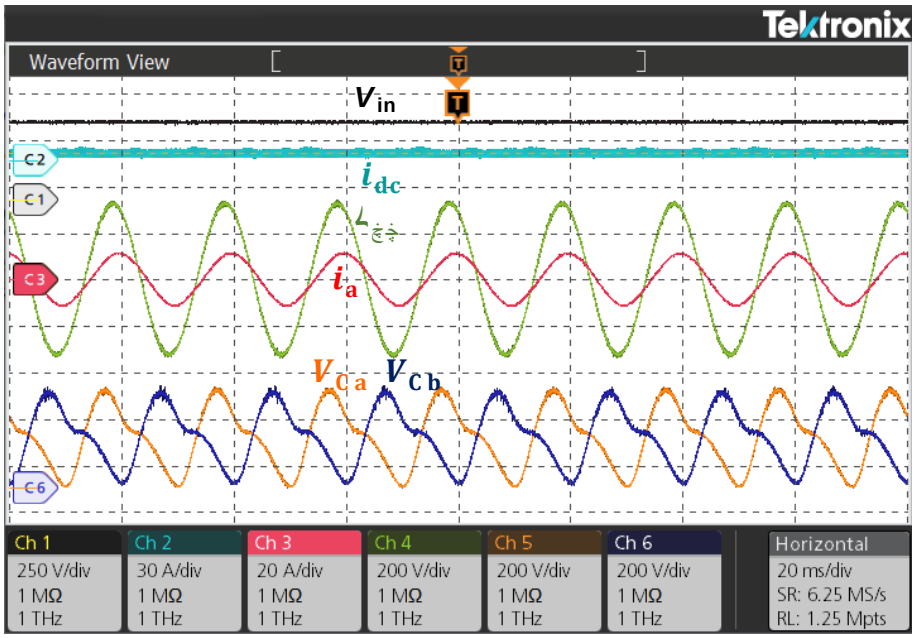


Figure 6.11: Experimental results for a grid-connected system at 1.8kW with a second-order ripple controller (V_{in}: 250V/div, i_{dc}: 30A/div, i_a: 20A/div, v_{ab}, V_{ca}, V_{cb}: 200V/div).

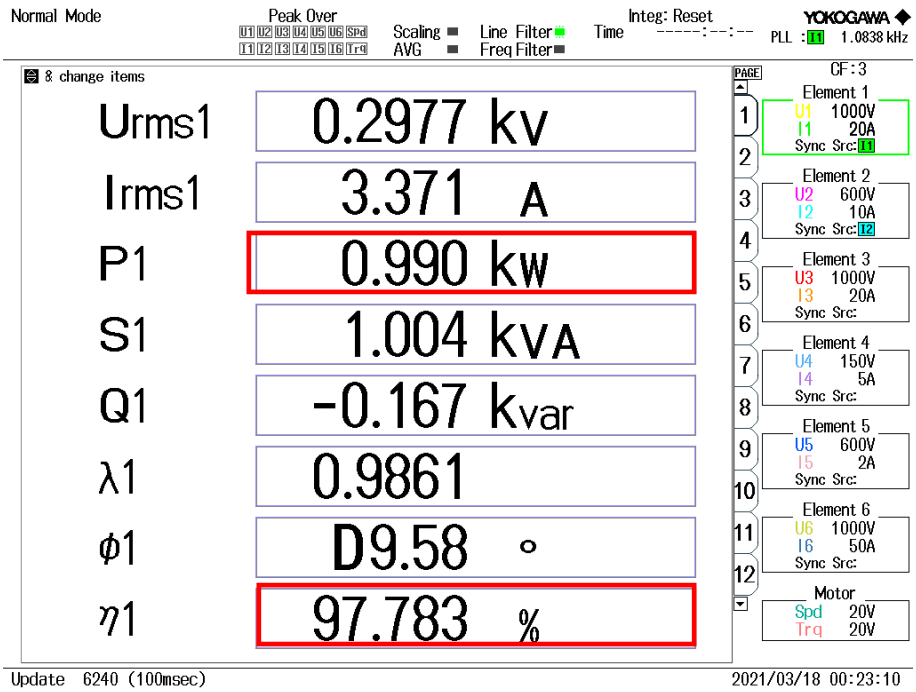


Figure 6.12: Maximum efficiency of the buck-boost inverter.

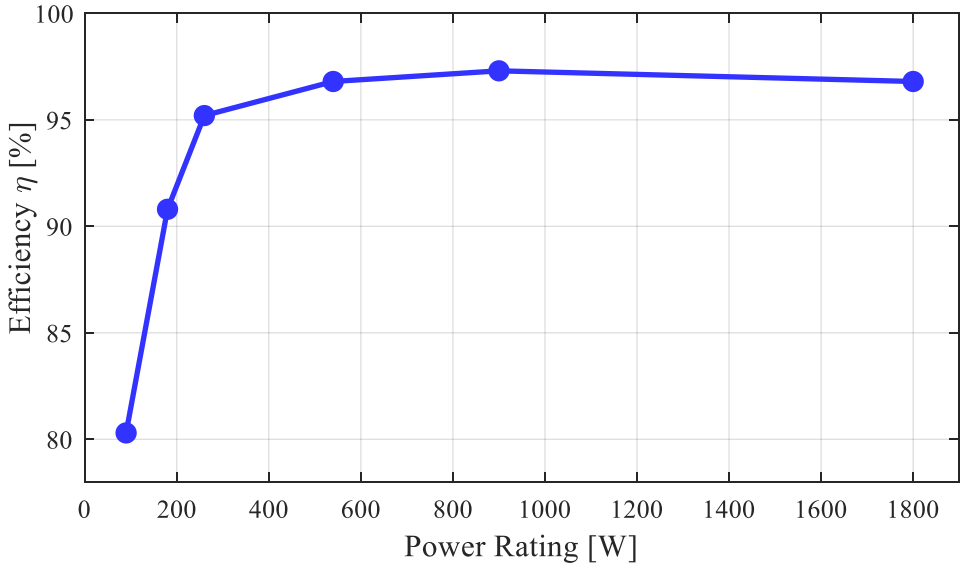


Figure 6.13: Efficiency of grid-connected inverters.

6.5 Topology Comparison

The proposed buck-boost inverter is compared with other buck-boost inverter topologies. The power rating, efficiency, switching frequency, type of devices, number of inductors, number of capacitors, number of diodes, and number of switches are compared, as shown in Table 6.2.

Table 6.2: Comparison of existing buck-boost inverter topologies

Topology	Power rating (W)	Efficiency (%)	Switching frequency (kHz)	Type of devices	No. of inductors	No. of capacitors	No. of diodes	No. of switches
[128]	500	93	40	Si	3	3	0	4
[129]	300	87	10	Si	3	2	2	4
[130]	170	87	10	Si	2	2	3	5
[131]	500	96.5	20	Si	1	2	0	8
[132]	500	95.5	10	Si	1	2	0	6
[133]	300	95.7	50	-	3	3	0	4
[134]	300	94.5	50	-	3	3	0	5
[135]	300	97.4	50	-	6	3	4	4

[136]	400	87	12	Si	2	2	0	4
[137]	400	95.9	30	Si	1	3	0	6
[138]	800	95.7	20	Si & SiC	2	1	0	6
Proposed inverter	1800	97.8	50	GaN	2	2	0	8

The power ratings are lower than the proposed topology for all of the topologies that are listed in Table 6.2. This will affect the system of a high-power rating design. Then, the efficiency of most of the topologies is decreased by the DC-side second-order harmonics. This will affect the efficiency of MPPT, PV lifetime and amplifies odd harmonics on the grid side [128], [135], [137], [138]. In most of the topologies, the second-order ripple was eliminated by using large DC-link capacitors. This will also reduce the efficiency and power density of the inverter. However, in some of the topologies, a low switching frequency is used to control the switch, which reduces the conversion gain and the efficiency [129], [130], [136]. Moreover, many of the topologies use conventional Si-based devices. The switching frequency of these devices is lower than that of the GaN devices. This will increase the volume of passive components and reduce the output waveform quality. In [129], [133], [134], [135], [137], the number of inductor and capacitor are higher than the other topologies. The number of passive components makes a significant contribution to the total power losses and the inverter volume. A comparison shows that the existing topologies are not efficient when it comes to the number of components and efficiency. However, the proposed buck-boost inverter has eight switches. Among them, four are operated at low voltage stress. This can reduce power losses and increase efficiency.

6.6 Summary

The experimental verifications of the buck-boost inverter topology were presented. The experiment was conducted in both standalone and grid-connected systems. A 1kW prototype was developed to evaluate the standalone operations. The efficiency, power density and specific cost of the protype were verified and the outcomes were matched with the design

method. In addition, the grid-connected performance of the inverter was verified using a 1.8kW prototype. The maximum and European efficiency of the inverter was satisfactory compared to the commercial inverters. Finally, the proposed buck-boost inverter was compared with existing buck-boost inverter topologies. Compared to the existing topologies, the GaN-based buck-boost inverter has achieved higher efficiency and has eliminated the DC-link current ripple with minimum passive components.

Chapter 7 Conclusion and Future Work

7.1 Introduction

GaN-based solar PV inverters have attracted attention because they operate at high switching frequencies, high temperatures, and high voltage. However, these benefits are not directly achievable because the trade-offs between the performance parameters of the inverter. For example, operating at a higher switching frequency reduces the volume of the passive components and increases the switching losses. Consequently, the inverters efficiency and power density will be changed. Therefore, to optimise the benefits of GaN devices, the design challenges and trade-offs between components associated with single-phase inverter topologies need to be addressed. This thesis has investigated the impacts of GaN-based single-phase differential PV inverter topologies in terms of efficiency, power density, and cost using systematic design and control approaches. This chapter aims to draw conclusions from the work that was carried out as part of this thesis, and it will make some recommendations for future work.

7.1.1 Design and Control of Single-phase Differential Buck Inverters

In Chapter 3, the challenges and control methods of designing a single-phase inverter with a second-order ripple power decoupling function were investigated. A GP-based multi-objective design approach was introduced to design the inverter by considering the efficiency and power density. The proposed design approach was developed based on detailed mathematical modelling of each component within the inverter. A trade-off study was conducted between the decoupling capacitor and the inverter power loss to select the optimum power decoupling capacitors. The Pareto-front curve of efficiency versus power density was obtained from the design approach, which was helpful to understand the trade-off

between the performance measures. This quickly identified the optimum design parameters without affecting the inverters total power loss or volume. A detailed control scheme for the differential inverter was discussed. The presented approach design approach was used to develop a 1kW prototype for a GaN-based inverter. The components were selected based on the outcome of the multi-objective design approach. The tested efficiency and power density of the prototype were 98.02% and 4.54kW/dm^3. Compared to the numerical model, the design approach is more effective when the computational complexity and convergence are concerned. The computational time of the proposed approach was 64.4% faster than the numerical model. In addition, the second-order ripple in the DC-link current was reduced more than eight times.

7.1.2 Fast and Accurate Design of Single-phase Inverters

The GP-based multi-objective design method required more mathematical models and more system information to find the optimal design. In addition, the design approach increased the computational complexity, needed more conditions to eliminate unwanted solutions, and required more time to choose the optimal design. Therefore, in Chapter 4 an ANN-based multi-objective design method was developed to minimise the use of mathematical models and improve the performance boundary accuracy. A simulation study was performed to ensure the effectiveness of the ANN-based design method. The ANN method has an accuracy of 97.3% when compared to the numerical model, i.e. an average mismatch of 2.73% over the twenty designs; while the accuracy of GP method is only 88.63% with an average mismatch of 11.37%. Hence, the ANN-based design method is more accurate than the GP based design method. In addition, it is worth mentioning the accuracy of ANN remains similarly high for obtaining designs not on the Pareto-front while the GP methods become more inaccurate for those designs. The numerical model takes a computational duration of 4 hrs and 56 mins, while the GP approach takes a computational duration of 3 hrs 52 mins. For the same case, the ANN-based design method takes less than 1 hr 15 mins. The time duration included both dataset generation and training time. Finally, the performance of the ANN-based design method was verified by developing a 1kW GaN-based buck-type inverter with power decoupling functions. The experiment was conducted to ensure the second-order ripple

elimination capability of the designed inverter. From the FFT results, 88% of the second-order ripple current in the DC-link was removed, and the low output current THD was obtained as 1.46%.

7.1.3 High-efficiency and High-power Density Design of PV Inverters

A buck-type differential inverter was needed for front-end DC-DC converters for solar PV application to handle the wide voltage requirements. Meanwhile, a front-end converter was required additional control components, which reduced the overall efficiency and power density, and increased the system costs. Therefore, a GaN-based single-stage buck-boost inverter topology was introduced, which enabled the inverter to operate at higher or lower input voltage. An ANN-based multi-objective design method was used to identify the optimal efficiency value, power density and components cost. The buck-boost operation and the ripple elimination feature of the inverter were examined using simulation and experimental laboratory studies. Then, the standalone performance of the inverter was validated using a 1kW prototype, and the grid-connected performance was validated using a 1.8kW prototype. The experimental results proved that the inverter achieved wide voltage operations, eliminated low-frequency ripples, and had high output current quality. The proposed inverter topology was compared with existing buck-boost inverter topologies, which shows that the proposed topology has better characteristics than the existing topologies.

7.2 Future Work

Some recommendations for future work follow:

- The presented GP and ANN-based multi-objective design methods considered the performance measures of efficiency, power density and costs. This can be extended in future research by including the reliability performance measure to achieve a complete inverter design.

- The inverter topologies that are presented in this thesis are hard switching GaN-based inverters. Therefore, the good efficiency only remains at 50–100 kHz switching

frequency. Soft switching GaN-based inverters are required to further increase the 27switching frequency and achieve system-level benefits. In future work, the soft switching of the presented topologies can be achieved using the triangular current modulation (TCM) technique. Using TCM, the switching frequency of GaN-based inverters can be extended to a megahertz range of switching frequency, and high efficiency can be achieved.

- The topology proposed in Chapter 5 suffered from higher current stress. The peak value of the inductor current has doubled the value of the output current to achieve the buck-boost operations. For high-power applications, higher current rating GaN devices are required. Therefore, future work could introduce advanced control methods to reduce the inductor current.

- Dual MPPT operation is one of the essential features of commercial PV inverters, which helps to harvest more energy from the PV panel. To achieve this feature in a single-stage topology, multiple inverters are required. Therefore, dual MPPT operation of the buck-boost inverter topology should be investigated in future work.

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Appendix A GaN FETs Data

The characteristics of the 900 V GaN FETs (TP90H180PS) are listed in Table A.1.

Table A.1: Characteristics of the GaN FETs.

Parameter	Value
Drain-source voltage V_{DS}	900 V
Drain-source resistance ref. R^{*}_{DS}	205 mΩ
Output capacitance ref. C^{*}_{oss}	41 pF
Switch area ref. A^{*}_{sw}	45.6 mm^2
Total gate charge ref. Q^{*}_{g}	10 nC
Reverse recovery charge ref. Q^{*}_{rr}	49 nC
Thermal Res. Junction-to-case ref. $R^{*}_{\mathrm{\theta JC}}$	1.6 ^{o}C/W
Thermal Res. Junction-to-amb. $R_{\mathrm{\theta JA}}$	62 ^{o}C/W
Gate to source voltage V_{GS}	10 V
Forward voltage V_{SD}	1.6 V
Fall time for voltage t_{VF}	5 ns
Fall time for current t_{CF}	7.4 ns
Rise time for current t_{CR}	26 ns
Rise time for voltage t_{VR}	40 ns

Appendix B Buck-boost Inverter Power Decoupling Method

B.1 Second-order Ripple Compensation Voltage Calculation

From Figure 5.1, the output voltage and current of the inverter can be represented as,

$$v_{\mathrm{ab}} = V_{\mathrm{ab}} \sin \omega t \tag{C.1}$$

$$i_{\mathrm{a}} = I_{\mathrm{a}} \sin(\omega t + \varphi) \tag{C.2}$$

where V_{ab} and I_{a} are the amplitude of output voltage and current, and φ is the phase angle. The output power p_{ac} can be defined as follows,

$$p_{\mathrm{ac}} = v_{\mathrm{ab}} \times i_{\mathrm{a}} \tag{C.3}$$

$$p_{\mathrm{ac}} = \frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{2} (\cos \varphi - \cos(2\omega t + \varphi)) \tag{C.4}$$

According to power balance equation, $p_{\mathrm{ac}} = p_{\mathrm{dc}}$. The dc-link instantaneous power p_{dc} have the constant power P_{const} and ripple power p_{ripple}. The frequency of the ripple power is twice the fundamental frequency 2ω.

$$p_{\mathrm{dc}} = V_{\mathrm{in}} i_{\mathrm{dc}} = \frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{2} (\cos \varphi - \cos(2\omega t + \varphi)) \tag{C.5}$$

$$P_{\mathrm{const}} = \frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{2} \cos \varphi \tag{C.6}$$

$$p_{\mathrm{ripple}} = -\frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{2} \cos(2\omega t + \varphi) \tag{C.7}$$

Generally, large dc-link capacitor is required to reduce the effects of ripple power. The buck-boost inverter topology can reduce the DC-link ripple power using the output capacitors V_{Ca} and V_{Cb}. Hence, the need of large DC-link capacitors can be reduced. Now the capacitors voltage can be written as follows:

$$V_{\mathrm{Ca}} = \frac{V_{\mathrm{ab}}}{2}(1 + \sin \omega t) + v_{\mathrm{comp}} \tag{C.8}$$

$$V_{\mathrm{Cb}} = \frac{V_{\mathrm{ab}}}{2}(1 + \sin(\omega t + \varphi)) + v_{\mathrm{comp}} \tag{C.9}$$

where v_{comp} is the compensated voltage require to eliminate the second-order ripple component. The output capacitors stored the second order ripple component. The instantaneous power of the capacitors is equal to the ripple components, which can be written as follows:

$$V_{\mathrm{Ca}} i_{\mathrm{Ca}} + V_{\mathrm{Cb}} i_{\mathrm{Cb}} = -\frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{2}\cos(2\omega t + \varphi) \tag{C.10}$$

$$V_{\mathrm{Ca}}\left(\mathrm{Ca}\frac{dV_{\mathrm{Ca}}}{dt}\right) + V_{\mathrm{Cb}}\left(\mathrm{Cb}\frac{dV_{\mathrm{Cb}}}{dt}\right) = -\frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{2}\cos(2\omega t + \varphi) \tag{C.11}$$

$$\mathrm{Ca}\frac{d(V_{\mathrm{Ca}})^2}{dt} + \mathrm{Cb}\frac{d(V_{\mathrm{Cb}})^2}{dt} = -\frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{2}\cos(2\omega t + \varphi) \tag{C.12}$$

The value of output capacitors is equal i.e., $\mathrm{Ca} = \mathrm{Cb}$, Then, the equation (C.12) can be written as follows:

$$\frac{d(V_{\mathrm{Ca}})^2}{dt} + \frac{d(V_{\mathrm{Cb}})^2}{dt} = -\frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{2\mathrm{Ca}}\cos(2\omega t + \varphi) \tag{C.13}$$

Substitute equations (C.8) and (C.9) to equation (C.13),

$$\frac{d\left(\frac{V_{\mathrm{ab}}}{2}(1 + \sin \omega t) + v_{\mathrm{comp}}\right)^2}{dt} + \frac{d\left(\frac{V_{\mathrm{ab}}}{2}(1 + \sin(\omega t + \varphi)) + v_{\mathrm{comp}}\right)^2}{dt} = -\frac{V_{\mathrm{ab}} I_{\mathrm{a}}}{2\mathrm{Ca}}\cos(2\omega t + \varphi) \tag{C.14}$$

$$d\left\{2\left(\frac{V_{\mathrm{ab}}}{2}+v_{\mathrm{comp}}\right)^{2}+\left(\frac{V_{\mathrm{ab}}}{2}\sin\omega t+\frac{V_{\mathrm{ab}}}{2}\sin(\omega t+\varphi)\right)^{2}\right\}+ = -\frac{V_{\mathrm{ab}}I_{\mathrm{a}}}{2\mathrm{Ca}}\cos(2\omega t+\varphi)\,dt \tag{C.15}$$

Integrating both the side of the equation,

$$2\left(\frac{V_{\mathrm{ab}}}{2}+v_{\mathrm{comp}}\right)^{2}+\left(\frac{V_{\mathrm{ab}}}{2}\sin\omega t+\frac{V_{\mathrm{ab}}}{2}\sin(\omega t+\varphi)\right)^{2} = -\frac{V_{\mathrm{ab}}I_{\mathrm{a}}}{4\omega\mathrm{Ca}}\sin(2\omega t+\varphi)+C \tag{C.16}$$

$$v_{\mathrm{comp}}=\sqrt{\left(-\frac{V_{\mathrm{ab}}I_{\mathrm{a}}}{8\omega\mathrm{Ca}}\sin(2\omega t+\varphi)-\left(\frac{V_{\mathrm{ab}}}{4}\sin\omega t+\frac{V_{\mathrm{ab}}}{4}\sin(\omega t+\varphi)\right)^{2}+\frac{C}{2}\right)} -\frac{V_{\mathrm{ab}}}{2} \tag{C.17}$$

where C is an integral constant which makes the values of quare root to be positive. From equation (C.17), the compensated voltage v_{comp} can be determined. The required amplitude of ripple compensated voltage is generated by second-order ripple controller.