Compact Real-time Simulator with Spatial-temporal Parallel Design for Large-scale Wind Farms

Hao Fu, Peng Li, *Member, IEEE*, Xiaopeng Fu, *Member, IEEE*, Jinyue Yan, Zhiying Wang, Kun Wang, Jianzhong Wu, *Member, IEEE*, and Chengshan Wang, *Senior Member, IEEE*

Abstract—Real-time simulation of large-scale wind farms with detailed modeling can provide accurate insights into system transient behaviors, but entails challenges in computing resources. This paper develops a compact real-time simulator based on the field programmable gate array (FPGA) for large-scale wind farms, in which the spatial-temporal parallel design method is proposed to address the huge computation resource demand associated with detailed modeling. The wind farm is decoupled into several subsystems based on model consistency, and the electrical system and control system of each subsystem are solved in parallel. Both the module-level pipeline technique and superscalar pipeline technique are introduced to the wind farms' simulation to effectively improve the utilization of hardware resources. In case studies, real-time simulations of two modified wind farms are separately carried out on a single FPGA, including one with 13 permanent magnet synchronous generators under a time-step of 11 µs, and the other with 30 squirrel-cage induction generators under a time-step of 8 µs. Simulation tests, under different scenarios, are implemented to validate the numerical performance of the real-time simulator, and a comparison with the commercial tool PSCAD/EMTDC demonstrates the accuracy and effectiveness of the proposed design.

Index Terms—Real-time simulation, FPGA, wind farm, spatial-temporal parallelism, hardware design.

NOMENCLATURE

A. Variables

i_{dc}	Control signal for the controlled current source in DC side.
i_{qs}, i_{ds}	Current of the stator in the q axis and d axis.
i_{qr}, i_{dr}	Current of the rotor in the q axis and d axis.
$i_{a,m}$, $i_{c,m}$	Phase-A and phase-C current of the MSC.
$i_{a,g}$, $i_{c,g}$	Phase-A and phase-C current of the GSC.
$\boldsymbol{I}_{hist}$	History current source vector of branches.

$\boldsymbol{I}'_{b\_dev}$	Branch current vector of the *dev* element type.
$\boldsymbol{I}_b$, $\boldsymbol{I}_n$	Branch current vector and nodal injection current vector of the electrical subsystem.
$\boldsymbol{I}_{h\_dev}$, $\boldsymbol{I}'_{n\_dev}$	History current source vector and nodal injection current vector of the *dev* element type.
K_a, K_b, K_c	Three-phase PWM signals for the upper arms in the MSC.
L_m	Mutual inductance between the stator and rotor windings.
L_{ls}, L_{lr}	Self-inductance of the stator and rotor windings.
L_d, L_q	Inductance of the stator windings in dq axes.
R_s, R_r	Resistance of the stator and rotor windings.
S_a, S_b, S_c	Three-phase PWM signals for the upper arms in the GSC.
T_e, T_m	Electromagnetic torque and mechanical torque of the generator.
u_{dc}	DC-side voltage of the BTB converter.
u_{ds}, u_{qs}	Terminal voltage in dq axes.
$u_{ab,m}$, $u_{bc,m}$	Control signals for the controlled AC voltage sources of the MSC.
$u_{ab,g}$, $u_{bc,g}$	Control signals for the controlled AC voltage sources of the GSC.
$\boldsymbol{U}'_{b\_dev}$	Branch voltage vector of the *dev* element type.
$\boldsymbol{U}_b$, $\boldsymbol{U}_n$	Branch voltage and nodal voltage vector of the electrical subsystem.
ω, ω_r	Electrical angular velocity and the generator rotational speed.
λ	Permanent magnet flux linkage.
λ_{ds}, λ_{qs}	Flux linkage of the stator in dq axes.
λ_{dr}, λ_{qr}	Flux linkage of the rotor in dq axes.

B. Parameters

d	Matrix dimension of $\boldsymbol{G}^{-1}$.
f	Driven clock frequency of the FPGA.
F	Damping coefficient of the rotor.
$\boldsymbol{G}$	Conductance matrix of the electrical subsystem.
$\boldsymbol{G}'_{eq\_dev}$	Equivalent branch conductance matrix of the *dev* element type.
J	Moment of inertia.
K	Number of the subsystems decomposed from the wind farm.

m	Capacity of the storage space allocated for each subsystem.
$\boldsymbol{M}$, $\boldsymbol{M}'_{dev}$	Coefficient matrix of the electrical subsystem and a particular electrical element type.
N	Number of the WECSs decomposed from the wind farm.
P	Pole pair number.
t_3	Inherent time of a multiplication and addition.
T_{sum}, T_{sum}^*	Simulation time of the entire wind farm in the conventional design and proposed design.
T_1, T_2, T_3 and T_3^*	Solution time of **Step 1**, **Step 2**, **Step 3**, and **Step 3***.

I. Introduction

IN recent years, wind power generation, especially offshore wind farms, has attracted more and more attention around the world [1]. At the same time, many concerns, e.g., the sub-/super-synchronous oscillations [2] and the strong uncertainties of wind power generation [3], have also emerged, threatening the secure and stable operation of a power system with wind farm integration [4], [5]. To enhance our understanding of these phenomena, wind farms must be studied via transient simulations for grid integration assessment [6]. Meanwhile, novel control schemes and protection strategies have to be verified to ensure their effectiveness before their application for wind farms [7], [8]. Real-time simulation, equipped with the hardware-in-the-loop (HIL) test, provides a valuable tool to evaluate the performance of various external devices under extreme conditions [9].

However, it is challenging to implement the real-time simulation of large-scale wind farms. The switching frequency of power converters in wind farms is becoming much higher [10], which requires smaller time-steps to accurately reproduce the action moments of power electronic switches [11]. Wind farms are equipped with large numbers of basic electrical components, hundreds of wind turbine generators (WTGs) equipped with controllers of nonlinear structures. Such a large simulation scale creates significant computational difficulties when emulated under microsecond-level time-steps [12]. This conflict between the real-time requirements and the computational burden poses a significant challenge to real-time simulators based on limited hardware resources.

Efforts have been made on equivalent modeling of wind farms to reduce the computational burden [13]. It's worth noting that the equivalence is a good idea for studying the overall performance of wind farms on external systems, but fails to simulate various internal transient processes. The stability issues due to parallel voltage source converters [14], as well as the oscillatory modes related to the collector network [15] and the dynamic responses of different fault locations within the wind farm, emphasize the need for more detailed modeling of wind farms. Detailed modeling inevitably entails the difficulty of solving high-dimensional models, but this difficulty has been alleviated with the help of acceleration algorithms. Reference [16] achieves large-scale wind farm simulation with a multiscale algorithm based on the matrix exponential function. In [17], accelerated with Krylov subspace approximation, an exponential integration algorithm can cover the whole range of wind farm simulation demands. However, these two algorithms are both implemented in an iterative manner, and the uncertain number of iterations imposes limitations in the context of real-time simulation. Shifted frequency analysis (SFA), which eliminates the time-step constraint, is another effective way in solving high dimensional models [18]. But the computational cost of operating with complex numbers and transferring between shifted-frequency and time domains is relatively high, which may ultimately demand more hardware resources for real-time simulations.

With excellent simulation performance, parallel design methods have won the favor of various commercial real-time simulators. To improve the modeling capabilities of large-scale systems, RT-LAB has developed complete I/O capabilities to share large Simulink models over multiple CPUs and even several simulators [19]. In another real-time simulator RTDS, a similar multicores-multichassis modular hardware architecture is designed to enhance a large-scale real-time simulation [20]. In [21], a PC-cluster-based real-time simulator is introduced to simulate a grid-connected wind farm with ten DFIGs. To improve the performance, the above real-time simulators utilize the spatial parallel design method, in which different parts of the simulated systems are modeled with dedicated hardware resources. Due to its wide scalability and fast calculation, it brings high computational costs as the simulation scale increases, and may sometimes be infeasible for the real-time simulation of large-scale wind farms. In contrast, the temporal parallel design method, represented by the pipeline technique, requires fewer computation resources [22]. This is because it allows simulations of multiple systems with consistent models but different parameters to run concurrently on different slice cuts from the same procedure, thereby improving the utilization of hardware resources. However, this approach has strict constraints on model consistency, requiring necessary decoupling of the simulated system and detailed slicing of the simulation procedure.

Although wind farms are equipped with dozens or even hundreds of wind energy conversion systems (WECSs), these WECSs generally employ the same type of WTGs and associated devices. With this observation in mind, this paper presents a novel spatial-temporal parallel simulation design method, in which pipeline techniques are introduced, for the first time, into wind farm real-time simulation. To accelerate the real-time simulation of wind farms, dedicated hardware resources are allocated to the control system and electrical system for their spatial parallel calculation. Meanwhile, the entire wind farm is decomposed into multiple WECSs and a network subsystem, using the Bergeron line model. Instead of spending dedicated computational resources on repeatedly modeling each WECS, model consistency allows WECSs to be simulated in turn with the same solving pipelines inside the control system and electrical system. Moreover, FPGA is employed as the underlying hardware to speed up the instruction execution. Unlike sequential processors, the intrinsic massive parallel architecture of FPGA can be partitioned and configured into a large number of parallel processing units, which support the real-time simulator to achieve circuit

simulation at the nanosecond level [23].

The major contributions of this paper can be summarized as follows:

1) A real-time simulation architecture is developed for fixed speed WECSs and variable speed WECSs, in which the model features are fully exploited to achieve parallel processing. The modeling methods for electrical elements and controller units are both described. The designed simulator has been validated to reproduce various dynamic behaviors with the same numerical accuracy as an offline commercial tool.

2) A novel spatial-temporal parallel design method is presented for the real-time simulation of large-scale wind farms. The control system and electrical system of the wind farm are solved in parallel to accelerate the simulation. In addition, the module-level pipeline architecture of the nodal-analysis framework is established, and the superscalar pipeline technique is embedded in the control system simulation to improve the utilization of hardware resources. Based on the proposed method, real-time simulations of two modified wind farms have been separately achieved on a single FPGA. One wind farm is with 13 PMSGs under a time-step of 11 μs, and the other is with 30 squirrel-cage induction generators (SCIGs) under 8 μs.

The remainder of this paper is organized as follows. Section II implements the detailed real-time modeling and simulation of the fixed speed WECSs and variable speed WECSs. Section III introduces the proposed simulation design method based on the pipeline technique and parallel calculation. Two modified wind farms are employed in Section IV to validate the performance of the designed real-time simulator, followed by conclusions in Section V.

II. Modeling and Real-time Simulation Architecture of WECS

Modeling of typical WECSs is the basis for real-time simulations of wind farms. Primarily, there are two types of WECSs, based on the controllability of a WTG's rotational speed, i.e., fixed speed WECS and variable speed WECS [24]. Fixed speed WECSs—due to their merits of low cost and high reliability—have been the mainstream application in the early stages of wind power generation [25]. However, this system structure consumes large amounts of reactive power, which deteriorates the voltage stability of the connected grid. Thus, variable speed WECSs have been developed and gradually applied in wind farms. Owing to advances in power electronics technology and PMSGs, PMSG-based WECSs have become one of the most popular variable speed WECSs in recent years [26]. In light of this fact, modeling of PMSGs is employed in this section to introduce the real-time simulation design of WECSs, and the detailed model and hardware implementation of fixed speed WECSs are elaborated in the Appendix to avoid redundancy.

A. Modeling of PMSG-based WECSs

The electromagnetic transient (EMT) model of PMSG-based WECSs consists of an aerodynamic system, a PMSG,

a back-to-back (BTB) converter, and related controllers. Considering the decoupling structure between electrical components and controllers, the entire system is partitioned into an electrical subsystem and a control subsystem, as shown in Appendix B. It's worth mentioning that, under the time-delay current sources model, the solution of PMSGs is implemented in the control subsystem, and controlled current sources are employed to interface with the electrical subsystem. For more details on the aerodynamic model, refer to [27], which is not included here due to the space limitation.

1) PMSG Model

The PMSG model is derived in synchronous rotating coordinates, in which the terminal voltages are expressed by (1) and (2), and mechanical equations are depicted by (3) and (4).

$$u_{ds} = L_d \frac{di_{ds}}{dt} + R_s i_{ds} - P\omega_r L_q i_{qs} \tag{1}$$

$$u_{qs} = L_q \frac{di_{qs}}{dt} + R_s i_{qs} + P\omega_r (L_d i_{ds} + \lambda) \tag{2}$$

$$T_e = 1.5P[\lambda i_{qs} + (L_d - L_q)i_{ds}i_{qs}] \tag{3}$$

$$J\frac{d\omega_r}{dt} = P(T_m - T_e) - F\omega_r \tag{4}$$

2) Modeling of BTB Converter and Controller

The converter model is a non-negligible consideration in the real-time simulation of WECSs. In some real-time simulators (e.g., RTDS), power electronic components are represented by the associated discrete circuit (ADC) model to maintain an unchanged conductance matrix [28]. However, this model is usually applied in simulations with a time-step of smaller than 2 μs; otherwise, it may lead to the significant loss of numerical accuracy [29]. This paper adopts the switching-function model to represent the BTB converter, as shown in Appendix C. Control signals are given by the following equations.

$$\begin{bmatrix} u_{ab,m} \\ u_{bc,m} \\ u_{ab,g} \\ u_{bc,g} \end{bmatrix} = \begin{bmatrix} K_a - K_b \\ K_b - K_c \\ S_a - S_b \\ S_b - S_c \end{bmatrix} u_{dc} \tag{5}$$

$$i_{dc} = \frac{1}{u_{dc}}(u_{ab,g}i_{a,g} - u_{bc,g}i_{c,g} + u_{ab,m}i_{a,m} - u_{bc,m}i_{c,m}) \tag{6}$$

The switching-function model may not be able to reflect the detailed action moments of power electronic switches, but it can truly reproduce the various dynamic behaviors at the system level. More importantly, the switching-function model still has high simulation accuracy and numerical stability even with larger time-steps, making it more suitable for the real-time simulation of large-scale wind farms.

Additionally, two independent units, the MSC controller and GSC controller, are integrated into the BTB converter. As shown in Appendix B, both the MSC controller and the GSC controller possess a dual control loop, which is suitable for solving in parallel.

B. Simulation Framework of the Electrical System

The EMT simulation of electrical subsystems is a numerical solution to the differential algebraic equations (DAE) describing various electrical elements and their network topologies.

In this paper, the nodal-analysis method is adopted as the simulation framework [30] using the following steps.

Step 1: Calculating the history current sources of various electrical elements in the form of (7), and forming the nodal injection current vector of the electrical subsystem.

$$I_{\text{h}\_dev}(t) = \alpha_{dev}U_{\text{b}}(t - \Delta t) + \beta_{dev}I_{\text{b}}(t - \Delta t) \quad (7)$$

$$I'_{\text{n}\_dev}(t) = M'_{dev}I_{\text{h}\_dev}(t) \quad (8)$$

$$I_{\text{n}}(t) = I'_{\text{n}\_\text{RLC}}(t) + \cdots + I'_{\text{n}\_\text{Line}}(t) \quad (9)$$

where I_{h_dev} and I'_{n_dev} are the historic current source vector and the nodal injection current vector of a particular electrical element type, denoted as dev, where dev iterates over all element types appearing in the studied system; α_{dev} and β_{dev} are solution coefficient matrices which are determined by the integration methods and element type; M'_{dev} is a $n \times k$ coefficient matrix, where n is the node number in the subsystem and k is the element number in the dev element type.

Step 2: Calculating the node voltages with the equation $U_{\text{n}}(t) = G^{-1}I_{\text{n}}(t)$. It's worth mentioning that all inverse conductance matrices are pre-stored in the FPGA, and the one that's used is selected to participate in the calculation based on the breaker state [31].

Step 3: Updating the branch voltage vector and the branch current vector of all electrical elements with $U_{\text{n}}(t)$, and forming those of the whole electrical subsystem by (12) and (13), respectively.

$$U'_{\text{b}\_dev}(t) = {M'_{dev}}^{\text{T}}U_{\text{n}}(t) \quad (10)$$

$$I'_{\text{b}\_dev}(t) = G'_{\text{eq}\_dev}U'_{\text{b}\_dev}(t) + I_{\text{h}\_dev}(t) \quad (11)$$

$$U_{\text{b}}(t) = [U'_{\text{b}\_\text{RLC}}(t) \quad \cdots \quad U'_{\text{b}\_\text{Line}}(t)]^{\text{T}} \quad (12)$$

$$I_{\text{b}}(t) = [I'_{\text{b}\_\text{RLC}}(t) \quad \cdots \quad I'_{\text{b}\_\text{Line}}(t)]^{\text{T}} \quad (13)$$

For the hardwire implementation of this simulation loop, an architecture based on functional modules is established for the electrical system solution shown in Fig. 1, in which an equation solving module for **Step 2** and multiple element units for **Step 1** and **Step 3** are designed on a FPGA. It's worth noting that different element units in **Step 1** and **Step 3** are implemented in parallel.

C. Implementation of the Control System Simulation

In the designed real-time simulator, both the WTIG subsystem in the fixed speed WECS and the control subsystem in the PMSG-based WECS (described in Section II-B) are simulated by the control system solver. As shown in Fig. 1, the control subsystem of the PMSG-based WECS is taken as an example to present its hardware design, in which the entire subsystem is described by functioning blocks in terms of sequential solving relationships, e.g., the wind turbine block and the PMSG block, etc.

To illustrate the implementation of different controller blocks, Appendix D depicts the detailed hardware design of a dual-loop control structure. The pseudo-nonlinearization method is adopted in the control system, in which nonlinear equations, resulting from the relationships between the blocks, are transformed into linear equations by adding a time-step delay [23]. This method is appropriate in the real-time simulation of the control subsystem because the time-step is usually at the microsecond level. Meanwhile, this method can promote a fully parallel solution instead of iterative operations, making it suitable for implementing with a superscalar pipeline. More details about real-time simulation based on a superscalar pipeline will be discussed in the next section.

III. Spatial-temporal Parallel Simulation Design for Large-scale Wind Farms

A. Basic Idea

The proposal of a spatial-temporal parallel design method for the real-time simulation of large-scale wind farms is primarily inspired by two aspects. One aspect is the excessive resource consumption of wind farms under the spatial parallel design method; the other aspect is the model consistency of WECSs within wind farms.

For the spatial parallel design method, the electrical part of the wind farm is solved as a whole by the nodal-analysis framework, and the control part is simulated by constructing the c orresponding functional modules with dedicated hardware resources [32]. Fig. 2(a) illustrates the conventional FPGA design using the spatial parallel method, in which N control system solving units are built for the controllers of
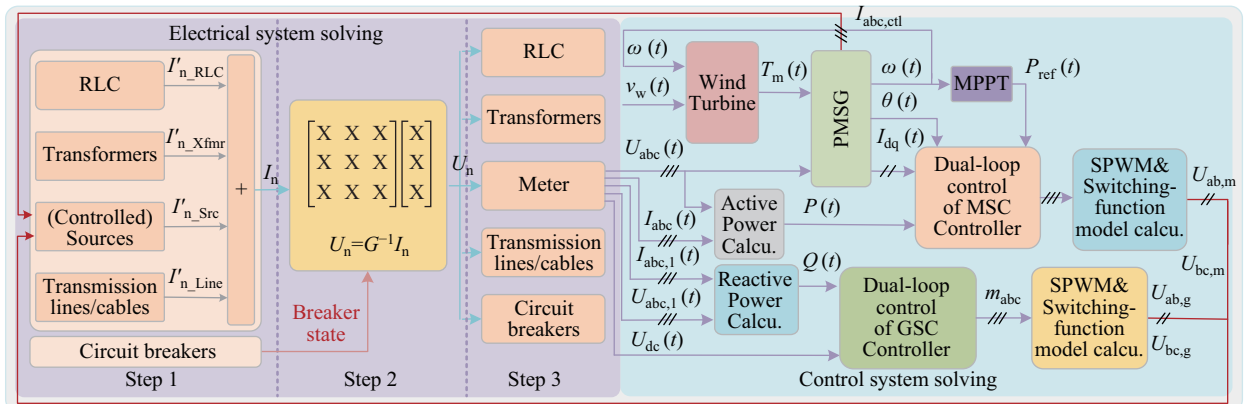

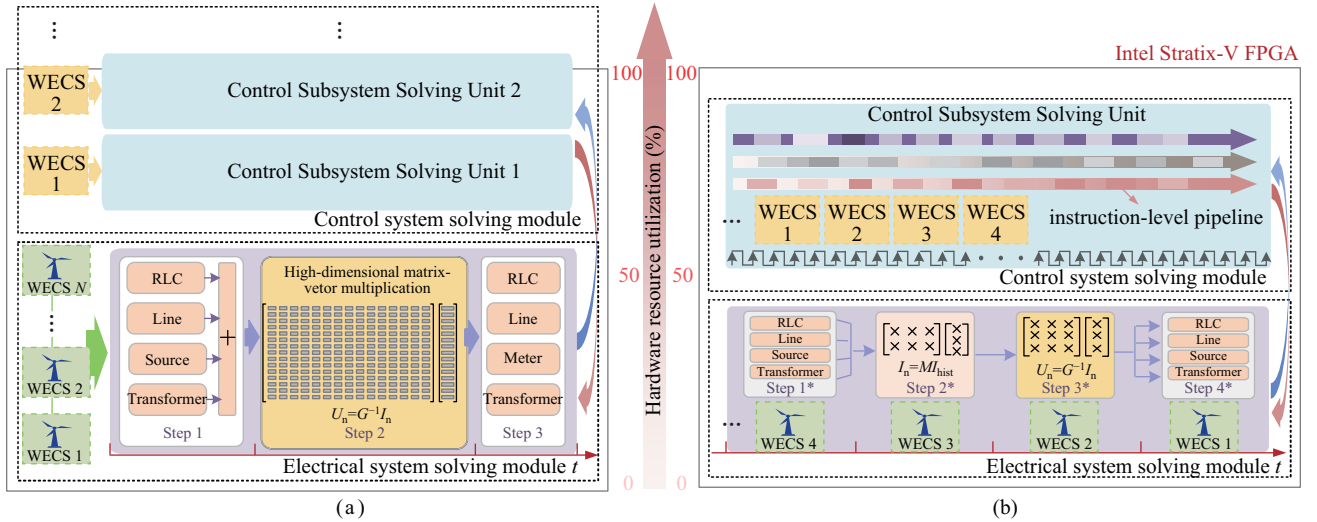Fig. 1.   FPGA implementation of the PMSG-based WECS.

Fig. 2. FPGA implementation of large-scale wind farms. (a) Conventional design. (b) Spatial-temporal parallel design.

different WTGs, and a three-step simulation loop is designed to simulate all electrical elements. Although compatible with various WECS controllers, this design faces huge hardware resource challenges from two factors, i.e., large numbers of control subsystem solving units, and high-dimensional equations solving in the electrical system. Specifically, for the PMSG-based WECS depicted in Fig. 1, it is impossible to achieve detailed modeling of two WECSs on the Intel Stratix® V 5SGSMD5K2F40C2N FPGA.

Considering that WTGs of the same type are commonly employed in a wind farm, this paper proposes a spatial-temporal parallel design, as shown in Fig. 2(b). To accelerate the real-time simulation of each WECS, dedicated hardware resources are allocated to its electrical and control subsystem for the spatial parallel calculation. The nodal analysis loop is re-divided and pipelined in the electrical system simulation, and the solution instructions are parallelized in the control system solving unit. Instead of spending dedicated computational resources on repeatedly modeling each WECS, the proposed design allows WECSs to be simulated in turn with the same solving pipelines composed of modules or instructions, thus greatly improving the resource utilization.

It can be seen from Fig. 2 that the spatial parallel design method has wider scalability, especially for the real-time simulation of power systems with different types of distributed generators (DGs). For large-scale systems with many identical complex components, such as photovoltaic power plants and wind farms, the proposed method can effectively conserve hardware resources, compared to conventional design methods.

B. Module Pipeline Design

1) Module-level Pipeline Architecture

As mentioned in Section II-C, the electrical system is simulated with the nodal-analysis framework, and each step is implemented by a basic solving module. Since the types of electrical elements in WECSs have been covered by the network subsystem, all subsystems can be simulated by the same solving modules, thus paving a way for electrical system

simulation based on the module-level pipeline technique. However, the electrical system in the conventional design cannot be simulated directly based on the pipeline technique. This is because the calculation tasks of the nodal-analysis method are not evenly divided, and differences in the respective solution time of different steps may lead to pipeline hazards [33] or low efficiency in the pipeline calculation. In addition, the same memory accessing-storing instructions will not only fail to achieve the parameter configuration of different WECSs, but also lead to serious data overwriting in the pipeline process.

In the module-level pipeline architecture, the first step of the nodal-analysis method is further divided into two steps, i.e., **Step 1*** and **Step 2***, then the original second and third step become **Step 3*** and **Step 4*** in the modified simulation loop, respectively. This is primarily based on the following considerations: 1) The more sections the same pipeline is divided into, the shorter the simulation time for all subsystems; 2) The entire pipeline should be divided as evenly as possible to avoid pipeline hazards. In addition to the uniform partitioning of the simulation loop, the mechanism of the module-level pipeline is also related to pipeline hazards and simulation efficiency. In this paper, an identical execution time (called the simulation period) is assigned to each step in the modified simulation loop. Assuming that the electrical subsystem i needs $s(i, j)$ to complete the solving of **Step j***, $\forall i = 1, 2, \cdots, N + 1$, $j = 1, 2, 3, 4$, the simulator takes the maximum value of $s(i, j)$ as the simulation period to ensure the completion of each step. And the number of simulation periods within one time-step is not less than that of subsystems plus three, otherwise real-time performance cannot be achieved.

Step 1*: Calculating the history current sources of various electrical elements by (7), and forming the history current source vector of branches by (14).

$$\boldsymbol{I}_{\text{hist}}(t) = [\boldsymbol{I}_{\text{h\_RLC}}(t) \quad \cdots \quad \boldsymbol{I}_{\text{h\_Line}}(t)]^{\text{T}} \tag{14}$$

Step 2*: Forming the nodal injection current vector of the electrical subsystem in the form of (15).

$$\boldsymbol{I}_{\text{n}}(t) = \boldsymbol{M}\boldsymbol{I}_{\text{hist}}(t) \tag{15}$$

Here, M is a $n \times u$ coefficient matrix with the form of (16), and u denotes the number of all elements in the electrical subsystem.

$$M = [M'_{\text{RLC}} \quad \cdots \quad M'_{\text{Line}}] \tag{16}$$

Taking each step in the simulation loop as a section of the pipeline, the electrical system simulation of wind farms can be realized using the module-level pipeline, as shown in Fig. 3. In simulation period n, the real-time simulator simultaneously solves **Step 1*** of electrical subsystem i, **Step 2*** of electrical subsystem $(i-1)$, **Step 3*** of electrical subsystem $(i-2)$, and **Step 4*** of electrical subsystem $(i-3)$. In this way, different steps of multiple electrical subsystems are simultaneously solved in each simulation period, until the last electrical subsystem completes the calculation of all four steps.
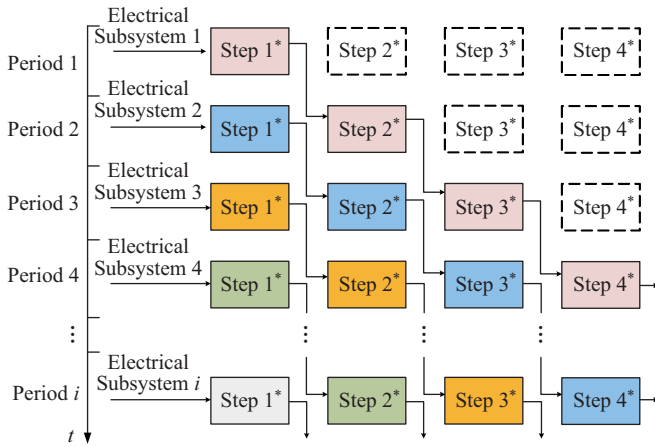

Fig. 3.   Space-time diagram of the module-level pipelined simulation.

The execution time of the module-level pipeline is another consideration for real-time simulation. Here, a comparison with conventional design is conducted under the premise of equal resource consumption. For a studied case decoupled into K subsystems, if the matrix G^{-1} of each subsystem has the same dimension d, the dimension of the entire wind farm will be Kd. In the module-level pipeline simulation, each subsystem employs d multipliers and accumulators to solve d rows of linear equations in parallel, and the calculation within each row is performed in the form of a pipeline. In this case, the solution time of **Step 3***, denoted as T_3^*, can be expressed by (17), where t_3 is the inherent time of a multiplication and addition. Considering that **Step 3*** is the most time-consuming step in the simulation loop, each period of the pipeline should be assigned with T_3^*, hence the simulation time of the entire wind farm in the proposed design is expressed by (18).

$$T_3^* = t_3 + d - 1 \tag{17}$$
$$T_{\text{sum}}^* = T_3^*(K + 3) = (t_3 + d - 1)(K + 3) \tag{18}$$

To ensure equal resource consumption, the Kd-dimensional equations of the wind farm should also be solved using d multipliers and accumulators in the conventional design. The time required to solve **Step 2** in the multiplexed form is

expressed by (19), and the execution time of the simulation loop in the conventional design can be expressed by (20).

$$T_2 = t_3 + K^2 d - 1 \tag{19}$$
$$T_{\text{sum}} = T_1 + (t_3 + K^2 d - 1) + T_3 \tag{20}$$

From (18) and (20), it can be seen that the simulation time of the wind farm based on the proposed design has a linear relationship with the number of subsystems, while the conventional solution design has a square relationship with K. This comparison shows that the proposed design can effectively accelerate the solution of large numbers of WTGs, so it is more suitable for the real-time simulation of large-scale wind farms.

2) Implementation of Module-level Pipeline

Appropriate scheduling of simulation data is critical for implementing the module-level pipeline, and its essence lies in managing memory units. In the electrical system solving unit, ROM units are primarily used to store constant electrical parameters and inverse conductance matrix G^{-1}, and RAM units are used for electrical variables that are updated during the simulation. To avoid accessing conflicts between subsystems, three different dynamic accessing-storing strategies based on varying addresses are proposed for constant parameters, G^{-1} and electrical variables.

Figure 4(a) demonstrates the dynamic access of constant parameters, in which Addr_n means the initial accessing address generated in period n. In pre-storing parameters into ROM units, the initial storing address of the first subsystem is set to 0, and adjacent subsystems are separated by m, where m is the capacity of dedicated storage spaces allocated for each subsystem. Assuming that the first subsystem starts to access pre-storing parameters in **Step n***, its initial accessing address should be set to 0 in period n. As the simulation period increases, this initial address is incremented by m to achieve accurate positioning of the accessed data. Meanwhile, the number of accessing addresses is also dynamically updated following the simulation period.

The dynamic access of G^{-1} is shown in Fig. 4(b), in which var_v and acc_v represent the address offset and accumulation of the vth electrical subsystem respectively, and $g_{i,u,v}$ means the ith row vector of G^{-1} corresponding to the uth topology of the vth electrical subsystem. It is worth noting that each ROM unit only stores the same row of matrices corresponding to all possible topologies of all subsystems. In other words, the storage of G^{-1} requires the same number of ROM units as the dimension of the matrix G^{-1}. When accessing the row vector $g_{i,u,v}$, the initial accessing address can be determined by acc_v and var_v, and the number of accessing addresses is dynamically updated following the simulation period. Here, the address offset acc_v is read from the pre-stored ROM units as Fig. 4(a), and var_v is determined using a lookup table based on the state of all breakers in the subsystem. The number of accessing addresses is dynamically updated following the simulation period. Since the wind farm is partitioned into multiple subsystems, the dimension of the pre-stored matrices is reduced. Meanwhile, the number of pre-stored matrices of the subsystem is only related to the number
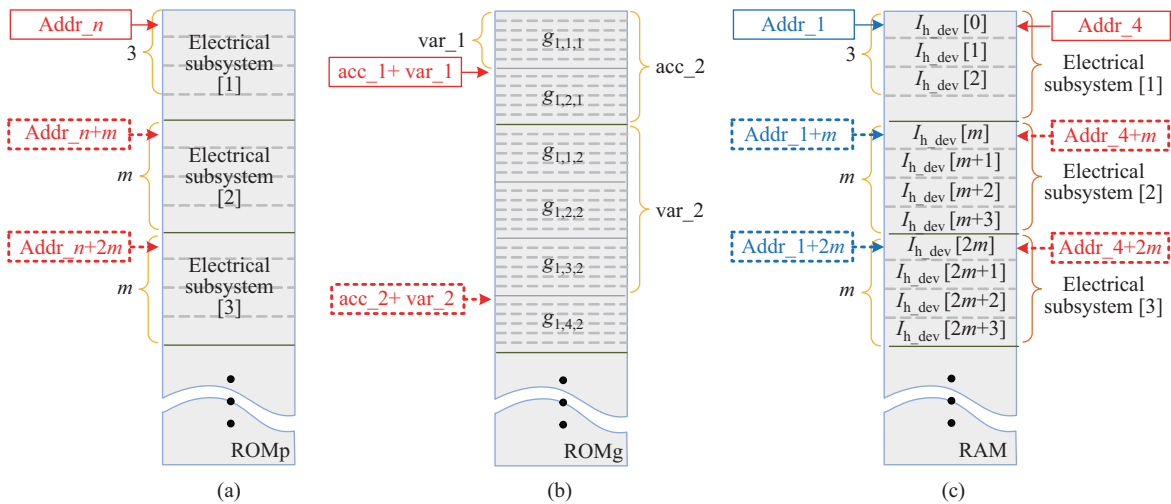
Fig. 4.   (a) Dynamic access of parameters. (b) Dynamic access of $\boldsymbol{G}^{-1}$. (c) Cross-period access of $\boldsymbol{I}_{\mathrm{h}\_dev}$.

of its included breakers, more breakers can be allowed in the proposed design compared to the conventional design. Using Intel Stratix® V 5SGSMD5K2F40C2N FPGA as an example, up to 9 breakers can be included in a wind farm with thirteen PMSG-based WECSs.

Using the cross-period access of $\boldsymbol{I}_{\mathrm{h}\_dev}$ as an example, the dynamic accessing and storing of RAM units are shown in Fig. 4(c), where address pointers with blue and red borders denote the initial storing and accessing addresses, respectively. During the calculation of the electrical system, updating of the branch current vector $\boldsymbol{I}'_{\mathrm{b}\_dev}$ in **Step 4*** will use the history current source vector $\boldsymbol{I}_{\mathrm{h}\_dev}$ calculated in **Step 1***, resulting in the cross-period access of simulation data. In response to this demand, the initial storing address of $\boldsymbol{I}_{\mathrm{h}\_dev}$ is set to 0 in simulation period 1, and the initial accessing address is set to 0 in the fourth period. After that, both initial accessing and storing addresses are incremented by m with the simulation period advancing. At the same time, the number of addresses for accessing and storing $\boldsymbol{I}_{\mathrm{h}\_dev}$ is also updated following the simulation period, so as to achieve the accurate access to the simulation data of different subsystems.

C. Superscalar Pipeline Design

Although the performance of real-time simulators has been significantly improved by employing the module-level pipeline, the control system simulation of large-scale wind farms also requires suitable hardware design based on the pipeline. There is an important constraint: sections in a pipeline should be guaranteed to have the same execution time. Considering the obvious time differences existing between the functional modules and basic arithmetic units in the controllers of WECSs, it is not appropriate to take each functional module or each arithmetic unit as a section. However, the underlying instruction operations of various arithmetic units in an FPGA, e.g., logic gate operation, all require the same execution time of one clock cycle, which can be considered as a pipeline section at the instruction level.

To further accelerate the real-time simulation of the control subsystem, as uperscalar pipeline architecture combining

parallel calculation and instruction-level pipelined execution is presented. Fig. 5 illustrates the superscalar pipeline design of the control system of PMSG-based wind farms, in which the control system models seen in Fig. 1 are employed. It can be seen that three parallel instruction-level pipelines are designed to carry out the control system simulation. And in each pipeline, multiple WECSs simultaneously execute different sections (i.e., instruction operations) in each clock cycle until the last WECS completes all instruction operations. At the end of instruction-level pipelines, different WECSs will sequentially output the simulation results of their control systems at a pace of one clock cycle. That is to say, for a wind farm with N WECSs, the proposed design only consumes $(N-1)$ clock cycles more than the conventional design. Thus, the superscalar pipeline architecture not only conserves hardware resources, but has very little impact on simulation time.

For the superscalar pipeline design, several improvements require attention in the process of pipelining and parallelizing. To avoid being overwritten by the next WECS, the intermediate variables in the instruction-level pipeline should be sequentially stored in the system memory if they are still required in later instruction operations. In addition, the length of multiple parallel pipelines should be kept as equal as possible to shorten the simulation time of the control system. For this purpose, it may be necessary to introduce a time-step delay for artificial decoupling. The flexible configuration of control parameters is another problem that cannot be ignored. In the control system solving unit, each important control variable is configured with a dedicated ROM or RAM unit. The initialization parameters and simulation data of different controllers can be stored in this memory unit, and the solving unit will continuously read from the memory when the control variable is applied.

D. Spatial Parallel Design and Data Communication

Compared with serial algorithms [30], parallel algorithms [34] can effectively shorten the solution time of an EMT iteration and are adopted in the proposed design. To
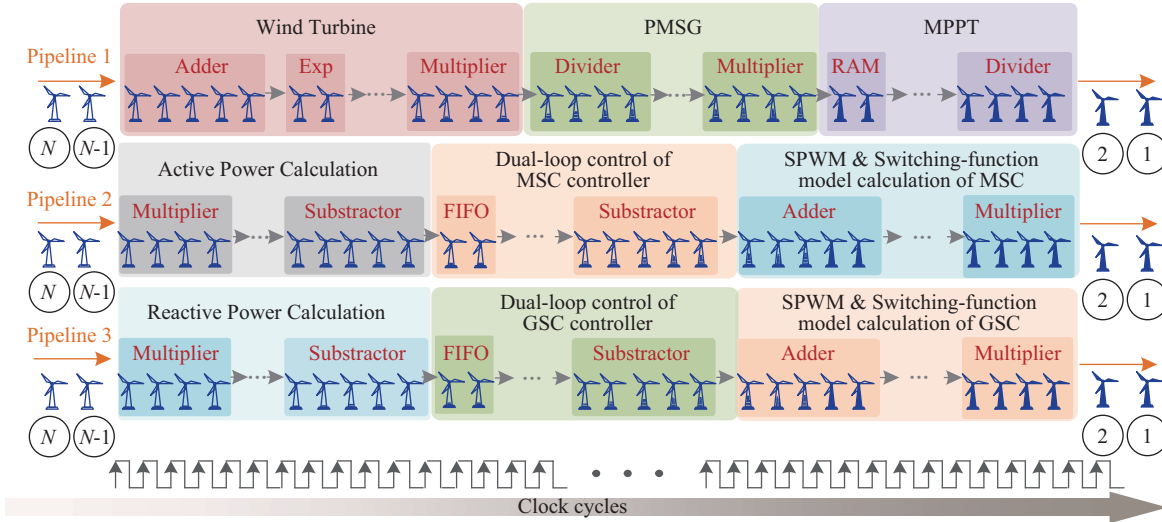
Fig. 5.   Superscalar pipeline design of the control system of PMSG-based wind farms.
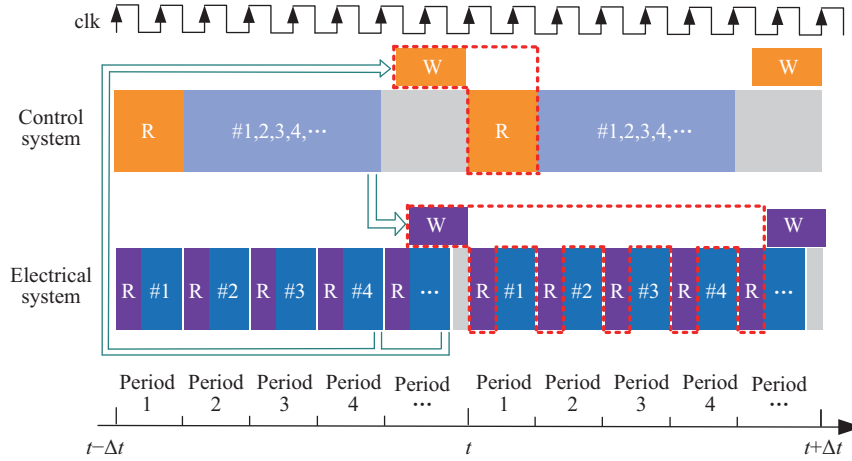

Fig. 6.   Diagram of parallel simulation and data communication.

accelerate the real-time simulation of large-scale wind farms, dedicated hardware resources are allocated to the control system and electrical system for their spatial parallel calculation. In parallel simulation, data communication should be properly implemented. Due to the different pipeline levels, i.e., module-level pipeline for the electrical system versus instruction-level pipeline for the control system, the control system outputs the controlled currents and voltages of different WECSs continuously and densely with the clock cycle, whereas the electrical subsystem output results at a pace of simulation periods. To access simulation results with different output paces, an interaction mechanism suitable for pipelined simulation is presented, as shown in Fig. 6. In this diagram, '#1, 2, . . .' denotes the different WECSs, 'R' is short for reading data from RAM units, and 'W' is for writing into RAM units. In the process of transferring control variables to the electrical system, the controlled currents and voltages of different WECSs are stored into the source module at an initial-address interval of m. Since the control system reads the currents or voltages of adjacent subsystems continuously with the clock cycle, continuous storing addresses across the

periods are required to ensure that the measured variables are continuously stored into the control system.

The format of the simulation data is an important factor affecting the accuracy of the real-time simulator. From experience, different electrical variables may vary greatly in order of magnitude [35], and the transfer function components in the control system are sensitive to numerical precision. The double-precision floating-point (FP) format is applied in the electrical system solving unit and the sub-modules containing transfer function components in the control system solving unit for improving the precision. Other control sub-modules without transfer function components still use the single-precision FP format to decrease the consumption of hardware resources.

E. Global Controller Design

The global controller in the designed simulator has the following functions: 1) To start and reset each time-step; 2) To advance simulation periods in the time-step; 3) To generate and update the initial storing-accessing addresses.

To start and reset each time-step simulation in (1), a counter

with the counting period of $t \cdot f$ is employed in the global controller to generate two pulse-signals one after another. When the counter accumulates to $t \cdot f$, the simulation end signal of each time-step is also generated to verify the real-time performance. An alarm will be issued if the EMT solution or data communication cannot be completed within a time-step.

As for (2) and (3), a finite state machine depicted in Fig. 7 is employed in the global controller, in which '*Addr_n*' means the initial storing-accessing address generated in simulation period n. Since the modified simulation loop of the electrical system consists of four steps, four initial addresses are generated to meet the demand of the cross-period access of data. At the beginning of each state, the finite state machine not only automatically advances the simulation periods using an accumulator, but updates the initial storing-accessing addresses in two situations. In detail, the superposition of generated addresses at interval m is implemented in S5, while new initial addresses are also generated from S1 to S4.

IV. CASE STUDIES

In this section, a PMSG-based wind farm and a SCIG-based wind farm, modified from a real system [36], are both simulated on the designed real-time simulator, in which only one Stratix® V Edition DSP development board is employed. The advantage of the spatial-temporal parallel design is demonstrated with regard to resource utilization, and the simulation results are compared with the commercial tool PSCAD/EMTDC to validate the numerical performance of the proposed design.

A. Test System 1: PMSG-based Wind Farm

1) Test Case

In this section, a wind farm with thirteen 1.5 MW PMSG-based WECSs is tested, as shown in Appendix E. The entire wind farm is decomposed into 13 PMSG-based WECSs and a network subsystem with the Bergeron line model, whose detailed parameters are shown in Appendix F and Appendix H, respectively. According to the parameter-setting principles described in Section III-B, each simulation period for solving

electrical subsystems is set to 80 clock cycles, and at least 17 simulation periods are required per time-step. To ensure the completion of data communication, an interaction time should be added to the larger solution time of the control system and electrical system for determining the time-step. In this case, a time-step of 11 μs driven by a 125 MHz clock is set to implement the real-time simulation.

Parameters of different PMSGs can be set individually in the designed real-time simulator; for simplicity, each simulated WECS is subjected to the same condition. A crowbar circuit has been installed in each WECS to improve the low-voltage ride through (LVRT) capability [37]. To validate the effectiveness of the crowbar protection, a symmetrical grid voltage sag as low as 0.2 p.u. in 2.4–2.6 s is considered for fast dynamic simulation.

2) Resource Utilization

The comparison of the main resources utilized by the tested case under the proposed design and the conventional design is shown in Table I. It's noted that the resource requirement of the conventional solution design far exceeds the resources configured on the development board. Therefore, the resources theoretically utilized by this system with the conventional solution design are estimated based on the consumed resources of a WECS.

TABLE I
COMPARISON OF THE RESOURCES USED WITH DIFFERENT HARDWARE DESIGNS FOR TEST SYSTEM 1

Hardware Design	Logic Resources (172,600)	DSP Blocks (1590)	Memory Bits (41,246,720)
Proposed Design	94%	43%	63%
Conventional Design	> 1066%	> 482%	> 61%

As can be seen from Table I, the logic resources and DSP blocks utilized by the test case under the conventional solution design are over 11 times greater than those based on the proposed design. The reason why the resource consumption ratio between these two designs is not 13 is because the network subsystem is also simulated in the proposed design. Since the simulation parameters of each subsystem all need to be pre-stored in ROM units, these two designs have similar
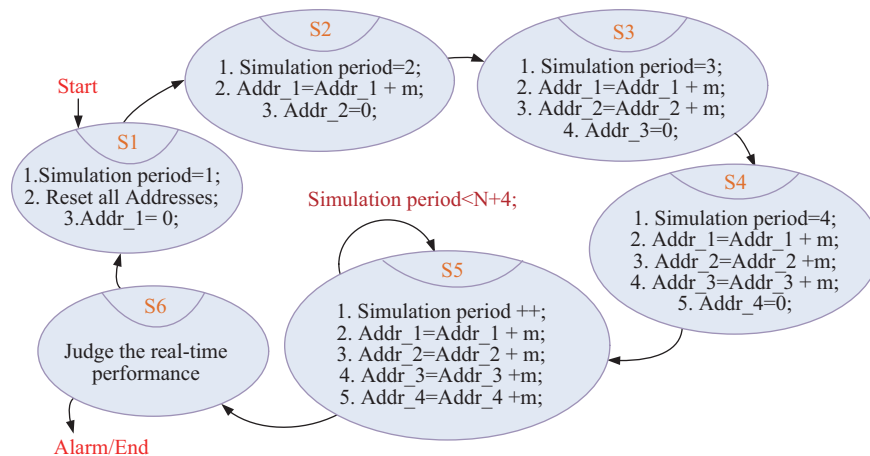

Fig. 7.   Finite state machine of the global controller.

consumption of storage resources. In summary, the proposed design has higher resource utilization and can greatly conserve hardware resources.

It's worth pointing out that the test system consumes almost all the logic resources of the designed wind farm real-time simulator, in which condition timing is at higher risk of failure. Generally speaking, reducing the operating frequency of FPGA is effective when timing closure becomes problematic, and a 125 MHz operating frequency applied in this case is selected by this means. In addition, several design measures were taken to tackle timing problems throughout the design process. The electrical properties of all I/O pins and the critical logic in the proposed design have both been clearly defined, and the proper and correct timing constraints have also been created for the design. In addition, complex combined circuits have been decomposed into several simple combined circuits connected with flip–flops for improving circuit timing. What's more, source registers were duplicated into multiple sub-source registers closer to the destinations when being found to have a high fan-out and large interconnect delay, so as to reduce the total interconnect and make the path faster.

3) Accuracy Validation

The simulation results of the voltage of Phase-A at PCC, as well as the DC-link voltage, electrical power and rotational speed of PMSG in WECS 1, are depicted in Fig. 8, respectively. As the GSC cannot deliver all the generated power into the grid under the low-voltage condition, the surplus power

continuously charges the DC-link capacitor, thereby increasing its voltage and enabling the crowbar circuit, as shown in Fig. 8(b). From Fig. 8(c) and (d), it can be seen that the electrical power and rotational speed of the PMSG almost remain constant during the voltage sag. This is because the PMSG continues its power generation in the same manner, and the crow-bar resistance eliminates the excess of active power production.

To make clear the accuracy performance of the designed simulator, the 2-norm relative error is used for indicating the error level, which is defined as [38]:

$$\varepsilon(f) = \|\tilde{f} - f\|_2 / \|f\|_2 \tag{21}$$

Here, $\tilde{f}$ and f represent the given numerical solution and its reference solution. The 2-norm relative error of the voltage of Phase-A at PCC is 8.8e-4, meeting the recognized requirement in real-time simulation research that the index is less than 1e-3 [39], [40]. In contrast to PSCAD/EMTDC, the errors of the FPGA-based simulator incorporate the following aspects: (i) Part modules inside the control system use the single-precision floating-point data format to decrease the consumption of hardware resources. (ii) The power electronic circuits in the FPGA are represented with the switching-function model, which is different from the $R_{\text{on}}/R_{\text{off}}$ model in PSCAD/EMTDC. (iii) One-step delay, introduced in the hardware design for improving simulation parallelism, also reduces the accuracy.
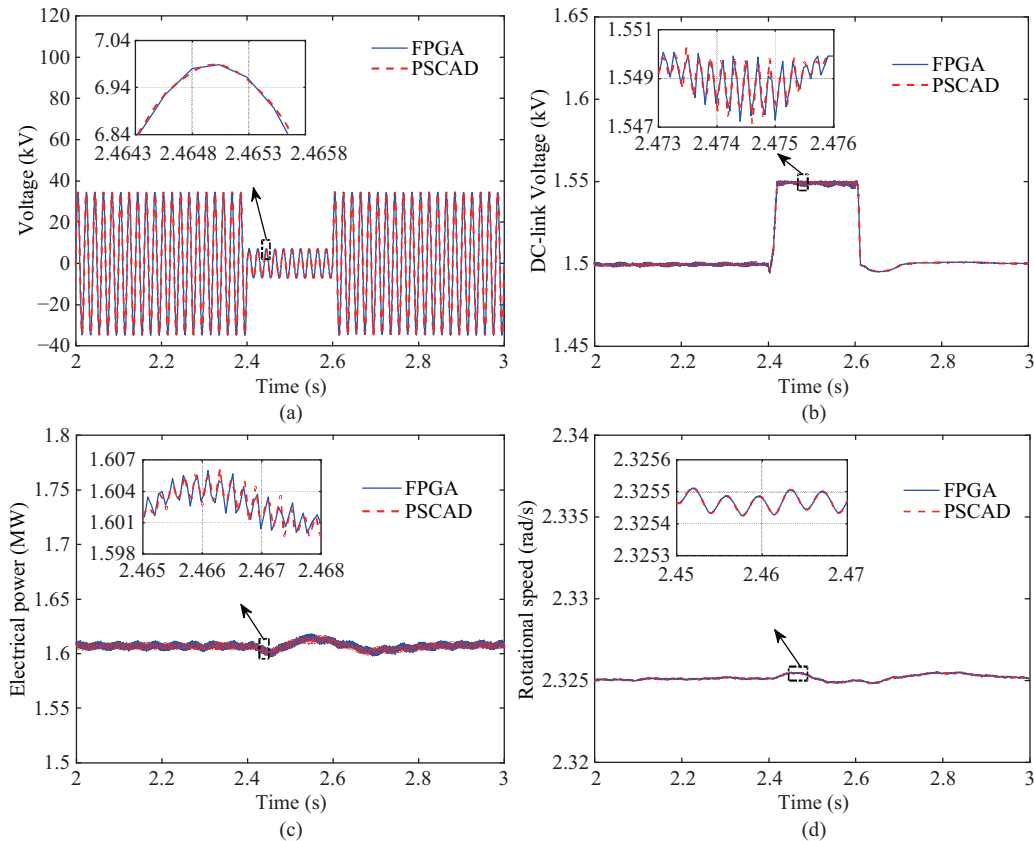

Fig. 8.   Simulation results of Test case 1. (a) Voltage of Phase-A at PCC. (b) DC-link voltage of WECS 1. (c) Electric power of the PMSG in WECS 1. (d) Generator rotational speed of WECS 1.

B. Test System 2: SCIG-based Wind Farm

1) Test Case

A large-scale wind farm with 30 fixed speed WECSs is studied in this section, and its schematic diagram is depicted in Appendix E. In order to implement real-time simulation with the proposed design, the entire system is decomposed into 30 WECSs and a network subsystem, whose detailed parameters are shown in Appendix G and Appendix H, respectively. Based on the aforementioned principles, the simulation period is set to 35 clock cycles, i.e., 0.234 μs for a 150 MHz simulation clock, and at least 34 simulation periods are required per time-step. Taking into account data communication, a time-step of 8 μs is determined to implement the real-time simulation of the wind farm. To further demonstrate the effectiveness of the design, a grid voltage sag as low as 0.8 p.u. in 3.1–3.3 s while considering different wind velocities for different SCIGs is considered in this case.

2) Resource Utilization

Table II shows the comparison of the computational resources utilized by this tested case under these two designs. It's noted that, under the conventional solution design, at most four SCIGs can be simulated on a single FPGA, and the resource consumption listed in Table II is a theoretical estimate based on the resources utilized by four SCIGs. From this table, we can see that the real-time simulation based on the proposed design almost consumes all the logic resources of the FPGA. In other words, this system is the largest scale

TABLE II
RESOURCE UTILIZATION FOR TEST SYSTEM 2 WITH DIFFERENT
HARDWARE DESIGNS

Hardware Design	Logic Resources (172,600)	DSP Blocks (1590)	Memory Bits (41,246,720)
Proposed Design	96%	34%	47%
Conventional Design	> 660%	> 240%	> 51%

of wind farms simulated on a single FPGA under the current time-step. In addition, it can be seen from the table that, under the conventional solution design, the consumed logic resources and DSP blocks are about 7 times greater than those consumed under the proposed design, which strongly illustrates the high resource utilization of the proposed design.

3) Accuracy Validation

The same case is simulated on the PSCAD/EMTDC under 8 μs, and its simulation results serve as the reference to validate the numerical performance. Fig. 9(a) and (b) show the voltage and current of Phase-A at PCC, respectively. To illustrate the simulation accuracy, the current of Phase-A at PCC is selected to evaluate the error performance, and its 2-norm relative error reaches 7.9e-4. This error level is within the acceptable range of real-time simulation, which verifies the accuracy and correctness of the proposed hardware design.

The generator rotational speed and active power of the WECSs are depicted in Fig. 9(c) and Fig. 9(d), respectively. It can be seen that several wind turbines with high wind velocities will be instable during the grid voltage sag. This
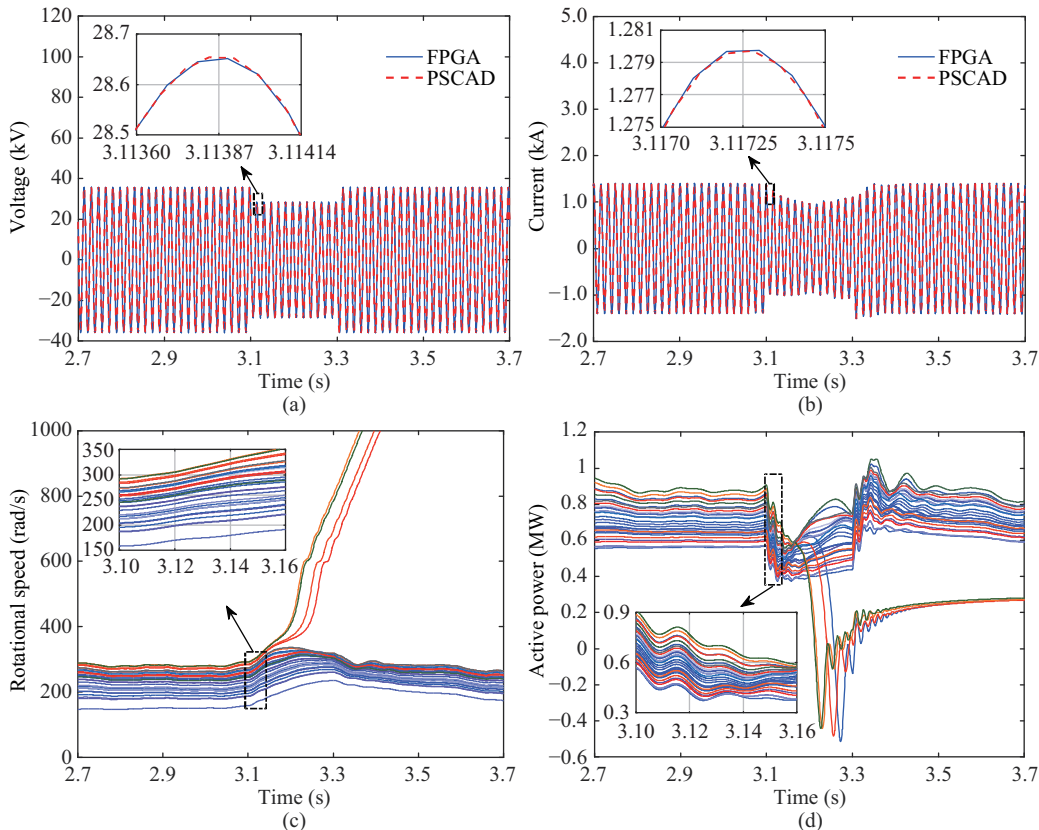

Fig. 9. Simulation results of Test system 2. (a) Voltage of Phase-A at PCC. (b) Current of Phase-A at PCC. (c) Generator rotational speeds of the WECSs. (d) Active power of the WECSs.

is because the active power transferred to the grid is very limited under the low voltage, and the captured wind energy is accumulated, thus speeding up the generator rotational speed. This phenomenon may not be fully reproduced in the simulation based on equivalent modeling, which demonstrates the merits of the spatial-temporal parallel design. Since the detailed models of WECSs and collector networks are available, simulations of various internal transient processes, including different fault types and different fault locations within the wind farm, can be implemented.

V. Conclusion

This paper presents a spatial-temporal parallel design of real-time simulators based on field programmable gate array, which is suitable for the accurate simulation of large-scale wind farms. The overall wind farm is represented by several typical subsystems considering model consistency, and for the first time, both module-level pipelines and superscalar pipelines are proposed for the real-time simulation of subsystems. Taking into full consideration the solution characteristics of the control system and the electrical system, these methods enable small time-step simulations and yield high resource utilization. Corresponding global controller design and data communication strategies are also proposed to enhance the pipeline implementation. The real-time simulation of wind farms with wind turbines numbering up to 30 SCIGs or 13 PMSGs has been achieved on a single FPGA, and different scenarios are employed to validate the accuracy and stability. Comparison results verify that the proposed design is capable of realizing the high-accuracy real-time simulation of wind farms with less computational resources.

In the future, further research needs to be carried out to improve the performance of the designed real-time simulator, primarily focusing on the following aspects.

1) In the designed real-time simulator, the layout of wind farms in different terrain environments has not been considered, which may not reflect the impact of wake effects on the transient processes of wind farms. Some advanced wake models, e.g., the three-dimensional (3D) Jensen-Gaussian wake model, have been developed to forecast the actual wind speed of different WECSs. By combining wake models with the EMTmodel of the wind farm, a more powerful real-time simulator can be implemented in future investigations.

2) Hardware-in-the-loop (HIL) testing has been considered the most important application of real-time simulators, in which control equipment and protection devices can be evaluated under real-time conditions. With the integration of reliable high-speed communicationinterfaces, a dedicated HIL platform for wind farms will be developed based on the designed real-time simulator in the future.

Appendix

A. Modeling of Fixed Speed WECS.

A classic topology of fixed speed WECSs is depicted in Fig. A1(a), where the SCIG is connected to the grid via a
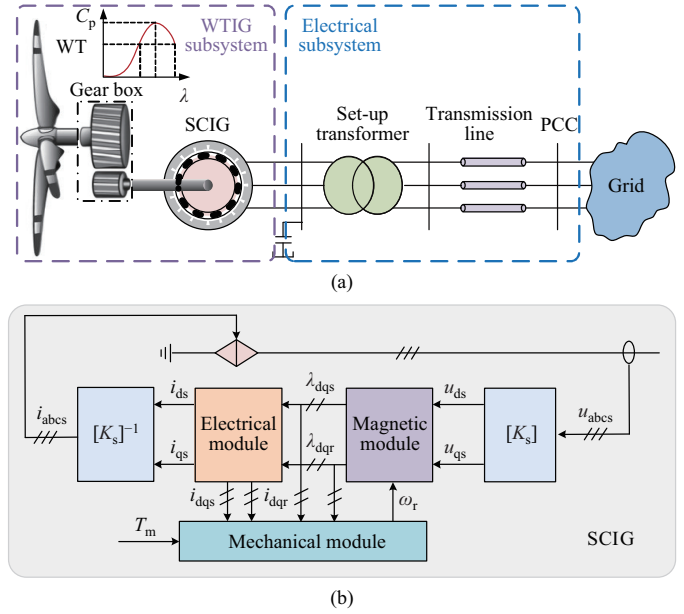

Fig. A1. (a) Configuration of the fixed speed WECS. (b) Block diagram of SCIG model.

transformer and transmission lines, and a gearbox is needed to transfer the wind energy from wind turbines (WTs) to SCIGs. The entire system is partitioned into (1) a wind turbine and induction generator (WTIG) subsystem and (2) an electrical subsystem, for parallel solution in the real-time simulation. The SCIG is equivalent to a Norton current source, which bridges the gap between the electrical subsystem and the WTIG subsystem. The aerodynamic system has been modeled in fixed speed WECSs, and you can refer to [27] for more details.

Various induction generator models, such as the quadrature-direct (q-d) model [41], the phase-domain (PD) model [42], and the voltage-behind-reactance (VBR) model [43], have been proposed in literature. Considering the advantages of linear operations and the potential of parallel simulations, the q-d model is employed in this paper to represent SCIGs, in which the induction generator can be expressed by the following equations, derived in the synchronous rotating dq0 frame.

$$
p\begin{bmatrix} \lambda_{qs} \\ \lambda_{ds} \\ \lambda_{qr} \\ \lambda_{dr} \end{bmatrix} = \begin{bmatrix} u_{qs} \\ u_{ds} \\ 0 \\ 0 \end{bmatrix} - \begin{bmatrix} \frac{L_b R_s}{L_a} & \omega & -\frac{L_m R_s}{L_a} & 0 \\ -\omega & \frac{L_b R_s}{L_a} & 0 & -\frac{L_m R_s}{L_a} \\ -\frac{L_m R_r}{L_a} & 0 & \frac{L_c R_r}{L_a} & \omega - \omega_r \\ 0 & -\frac{L_m R_r}{L_a} & \omega_r - \omega & \frac{L_c R_r}{L_a} \end{bmatrix}
$$
$$
\begin{bmatrix} \lambda_{qs} \\ \lambda_{ds} \\ \lambda_{qr} \\ \lambda_{dr} \end{bmatrix} \tag{A1}
$$

$$
\begin{bmatrix} i_{qs} \\ i_{ds} \\ i_{qr} \\ i_{dr} \end{bmatrix} = \begin{bmatrix} \frac{L_a + L_m^2}{L_a L_c} & 0 & -\frac{L_m}{L_a} & 0 \\ 0 & \frac{L_a + L_m^2}{L_a L_c} & 0 & -\frac{L_m}{L_a} \\ -\frac{L_m}{L_a} & 0 & \frac{L_c}{L_a} & 0 \\ 0 & -\frac{L_m}{L_a} & 0 & \frac{L_c}{L_a} \end{bmatrix} \begin{bmatrix} \lambda_{qs} \\ \lambda_{ds} \\ \lambda_{qr} \\ \lambda_{dr} \end{bmatrix}
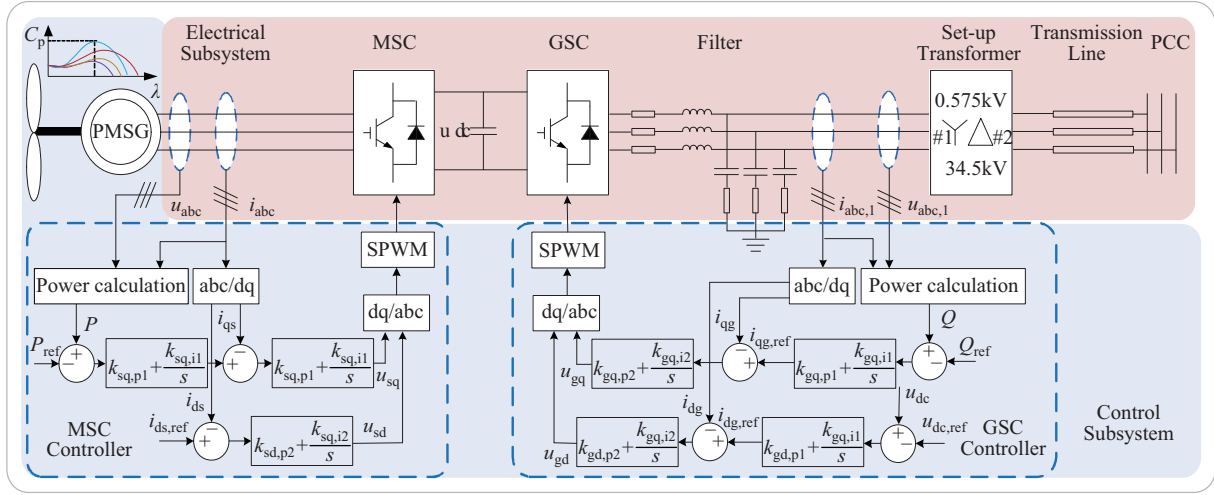$$
$$
\tag{A2}
$$

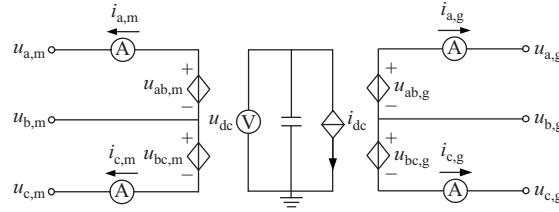Fig. A2.   Detailed Structure of the PMSG-based WECS.

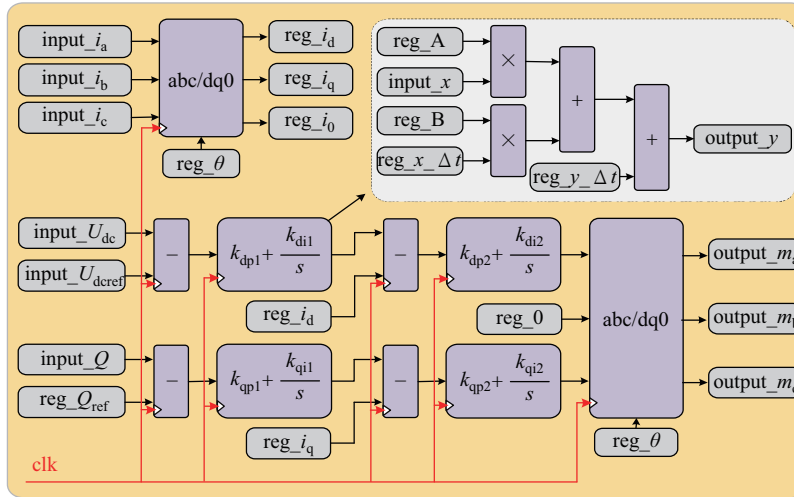Fig. A3.   Switching-function Model of the BTB Converter.

Fig. A4.   Hardware Design of the Dual-loop Control Structure.

$$T_{\mathrm{e}} = \frac{3P}{4}(\lambda_{\mathrm{ds}}i_{\mathrm{qs}} - i_{\mathrm{ds}}\lambda_{\mathrm{qs}}) \qquad (A3)$$

$$J\frac{\mathrm{d}\omega_{\mathrm{r}}}{\mathrm{d}t} = P(T_{\mathrm{m}} - T_{\mathrm{e}}) - F\omega_{\mathrm{r}} \qquad (A4)$$

where p is the differential operator, and $L_{\mathrm{a}} = L_{\mathrm{lr}}L_{\mathrm{ls}} + L_{\mathrm{m}}(L_{\mathrm{ls}} + L_{\mathrm{lr}})$, $L_{\mathrm{b}} = L_{\mathrm{m}} + L_{\mathrm{lr}}$, and $L_{\mathrm{c}} = L_{\mathrm{m}} + L_{\mathrm{ls}}$ are all intermediate variables for simplified representations.

The above equations reveal a tightly-coupled structure of the induction generator, which requires an iterative solution to achieve an accurate calculation. However, the uncertain number of iterations limits its application in real-time simulation. In order to avoid the iterative solution of WTIG subsystems,

a time-step delay of ω_{r} is introduced in (A1) to decompose the solving loop, thereby allowing the sequential solution of the model. The hardware design of the SCIG is shown in Fig. A1(b), in which three function modules are designed. The magnetic module is established for the calculation of flux linkages, and can be expressed with (A1). The electrical module is responsible for the currents solving with (A2), and the mechanical module is defined directly in terms of flux linkages, currents, and torques, by (A3) and (A4). To achieve the switching between the abc and the dq0 coordinate systems, two coordinatet ransformation modules are also established in our design.
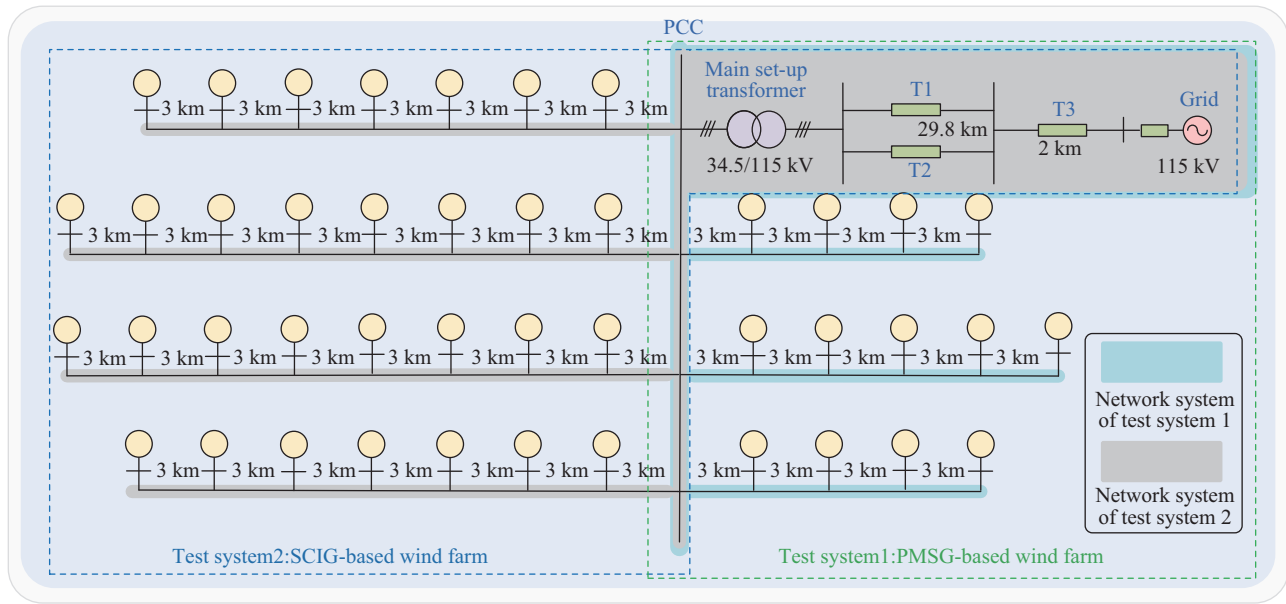
Fig. A5.   Schematic Diagram of the Large-scale Wind Farm Test Systems.

TABLE AI
DETAILED PARAMETERS OF THE PMSG-BASED WECS

Device	Parameter	Value
Transformer	Ratio	0.575 kV / 34.5 kV
	Nominal Power	2 MVA
	Leakage impedance	0.002+j0.050 Ω
	Magnetizing impedance	500+j500 Ω
Filter	Impedance	0.020 +j0.236 Ω
	Capacitive reactance	36.172 Ω
PMSG	Moment of inertia	10^5 kgm ^{2}
	Number of pole pairs	120
	Diameter of turbine blades	34 m
	Stator resistant	0.008 Ω
	Permanent flux	2.458 Wb
	Nominal power	1.500 MVA
BTB converter	Carrier frequency	5000 Hz
	Rated DC bus voltage	1500 V
	Capacitance of the DC bus capacitor	55 mF

TABLE AII
DETAILED PARAMETERS OF THE SCIG-BASED WECS

Device	Parameter	Value
Transformer	Ratio	0.575 kV / 34.5 kV
	Nominal Power	2 MVA
	Leakage impedance	0.002+j0.050 Ω
	Magnetizing impedance	500+j500 Ω
Shunt Capacitor	Capacitive Power	400 kVar
SCIG	Nominal power	1.667 MVA
	Stator impedance	0.006+j0.134 Ω
	Rotor impedance	0.005+j0.182 Ω
	Magnetizing impedance	6.320 Ω
	Combined Inertial	5.040 s

TABLE AIII
DETAILED PARAMETERS OF THE NETWORK SUBSYSTEM

Device		Parameter	Value
Grid		Impedance	0.145+j2.897 Ω
115 kV overhead line	T1, T2	Series impedance	0.081+j0.462 Ω/km
		Capacitive shunt reactance	0.148 MΩ*km
	T3	Series impedance	0.162+j0.923 Ω/km
		Capacitive shunt reactance	0.295 MΩ*km
34.5 kV overhead line		Series impedance	0.128+j0.391 Ω/km
		Capacitive shunt reactance	0.239 MΩ*km

REFERENCES

[1] X. Costoya, M. deCastro, D. Carvalho, and M. Gómez-Gesteira, "On the suitability of offshore wind energy resource in the United States of America for the 21st century," *Applied Energy*, vol. 262, pp. 114537, Mar. 2020.

[2] Y. N. Chi, B. J. Tang, J. B. Hu, X. S. Tian, H. Y. Tang, Y. Li, S. J. Sun, L. Shi, and L. Shuai, "Overview of mechanism and mitigation measures on multi-frequency oscillation caused by large-scale integration of wind power," *CSEE Journal of Power and Energy Systems*, vol. 5, no. 4, pp. 433–443, Dec. 2019.

[3] Y. F. Wang, C. Lu, L. P. Zhu, G. L. Zhang, X. Li, and Y. Chen, "Comprehensive modeling and parameter identification of wind farms based on wide-area measurement systems," *Journal of Modern Power Systems and Clean Energy*, vol. 4, no. 3, pp. 383–393, Jul. 2016.

[4] T. Jiang, Y. F. Mu, H. J. Jia, N. Lu, H. Y. Yuan, J. H. Yan, and W. F. Li, "A novel dominant mode estimation method for analyzing inter-area oscillation in China southern power grid," *IEEE Transactions on Smart Grid*, vol. 7, no. 5, pp. 2549–2560, Sep. 2016.

[5] B. Sahoo, S. K. Routray, and P. K. Rout, "Integration of wind power generation through an enhanced instantaneous power theory," *IET Energy Systems Integration*, vol. 2, no. 3, pp. 196–206, Sep. 2020.

[6] I. Zubia, J. X. Ostolaza, A. Susperregui, and J. J. Ugartemendia, "Multi-machine transient modelling of wind farms: an essential approach to the study of fault conditions in the distribution network," *Applied Energy*, vol. 89, no. 1, pp. 421–429, Jan. 2012.

[7] X. S. Tian, W. S. Wang, X. Li, Y. N. Chi, Y. Li, and H. Y. Tang, "Fault ride through strategy of DFIG using rotor voltage direct compensation control under voltage phase angle jump," *CSEE Journal of Power and Energy Systems*, vol. 5, no. 4, pp. 515–523, Dec. 2019.

[8] O. Noureldeen and I. Hamdan, "Design of robust intelligent protection technique for large-scale grid-connected wind farm," *Protection and Control of Modern Power Systems*, vol. 3, no. 1, pp. 17, Jun. 2018.

[9] F. Huerta, R. L. Tello, and M. Prodanovic, "Real-time power-hardware-in-the-loop implementation of variable-speed wind turbines, *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 1893–1904, Mar. 2017.

[10] J. Z. Xu, C. X. Gao, J. P. Ding, M. K. Feng, X. T. Wang, and C. Y. Zhao, "Electromagnetic transient acceleration simulation methods and prospects of high-frequency isolated power electronic transformer," *Proceedings of the CSEE*, vol. 41 no. 10, pp. 3466–3479, May 2021.

[11] Y. Zhang, H. Ding, and R. Kuffel, "Key techniques in real time digital simulation for closed-loop testing of HVDC systems," *CSEE Journal of Power and Energy Systems*, vol. 3, no. 2, pp. 125–130, Jun. 2017.

[12] J. Xu, K. Y. Wang, P. Wu, and G. J. Li, "FPGA-based sub-microsecond-level real-time simulation for microgrids with a network-decoupled algorithm," *IEEE Transactions on Power Delivery*, vol. 35, no. 2, pp. 987–998, Apr. 2020.

[13] W. J. Teng, X. F. Wang, Y. Q. Meng, and W. H. Shi, "An improved support vector clustering approach to dynamic aggregation of large wind farms," *CSEE Journal of Power and Energy Systems*, vol. 5, no. 2, pp. 215–223, Jun. 2019.

[14] B. Wen, D. Dong, D. Boroyevich, R. Burgos, P. Mattavelli, and Z. Y. Shen, "Impedance-based analysis of grid-synchronization stability for three-phase paralleled converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 26–38, Jan. 2016.

[15] L. P. Kunjumuhammed, B. C. Pal, C. Oates, and K. J. Dyke, "Electrical oscillations in wind farm systems: analysis and insight based on detailed modeling," *IEEE Transactions on Sustainable Energy*, vol. 7, no. 1, pp. 51–62, Jan. 2016.

[16] C. S. Wang, X. P. Fu, P. Li, J. Z. Wu, and L. W. Wang, "Multiscale simulation of power system transients based on the matrix exponential function," *IEEE Transactions on Power Systems*, vol. 32, no. 3, pp. 1913–1926, May 2017.

[17] X. P. Fu, C. S. Wang, P. Li, and L. W. Wang, "Exponential integration algorithm for large-scale wind farm simulation with Krylov subspace acceleration," *Applied Energy*, vol. 254, pp. 113692, Nov. 2019.

[18] P. Zhang, J. R. Marti, and H. W. Dommel, "Shifted-frequency analysis for EMTP simulation of power-system dynamics," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no.9, pp. 2564–2574, Sep. 2010.

[19] Opal-RT Technologies [Online]. [accessed 02.17.21]. Available: https://www.opal-rt.com/software-rt-lab-2/

[20] Real Time Digital Simulator (RTDS) [Online]. [accessed 02.17.21]. Available: https://www.rtds.com/technology/simulation-hardware/

[21] V. Jalili-Marandi, L. F. Pak, and V. Dinavahi, "Real-time simulation of grid-connected wind farms using physical aggregation," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 9, pp. 3010–3021, Sep. 2010.

[22] D. Kim, M. Ciesielski, and S. Y. Yang, "MULTES: Multilevel temporal-parallel event-driven simulation," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, no. 6, pp. 845–857, Jun. 2013.

[23] Z. Y. Wang, C. S. Wang, P. Li, X. P. Fu, and J. Z. Wu, "Extendable multirate real-time simulation of active distribution networks based on field programmable gate arrays," *Applied Energy*, vol. 228, pp. 2422–2436, Oct. 2018.

[24] S. Bhamu and T. S. Bhatti, "State-space modelling of an interconnected system of renewable energy sources and grid for rural electrification," *IET Energy Systems Integration*, vol. 1, no. 2, pp. 74–85, Jun. 2019.

[25] E. S. Abdin and W. Xu, "Control design and dynamic performance analysis of a wind turbine-induction generator unit," *IEEE Transactions on Energy Conversion*, vol. 15, no. 1, pp. 91–96, Mar. 2000.

[26] F. Blaabjerg, M. Liserre, and K. Ma, "Power electronics converters for wind turbine systems," *IEEE Transactions on Industry Applications*, vol. 48, no. 2, pp. 708–719, Mar./Apr. 2012.

[27] J. G. Slootweg, S. W. H. de Hanan, H. Polinder, and W. L. Kling, "General model for representing variable speed wind turbines in power system dynamics simulations," *IEEE Transactions on Power Systems*, vol. 18, no. 1, pp. 144–151, Feb. 2003.

[28] T. Maguire and J. Giesbrecht, "Small time-step ($<2\mu$ Sec) VSC model for the real time digital simulator," in *International Conference on Power System Transients (IPST)*, Montreal, Canada, 2005, pp. 1–6.

[29] K. Y. Wang, J. Xu, G. J. Li, N. L. Tai, A. P. Tong, and J. X. Hou, "A generalized associated discrete circuit model of power converters in real-time simulation," *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2220–2233, Mar. 2019.

[30] H. W. Dommel, "Introduction of EMTP," in *Electromagnetic Transients Program (EMTP), Theory Book*, Portland: Bonneville Power Administration, 1986, pp. 1–6.

[31] Z. Y. Wang, F. P. Zeng, P. Li, C. S. Wang, X. P. Fu, and J. Z. Wu, "Kernel solver design of FPGA-based real-time simulator for active distribution networks, *IEEE Access*, vol. 6, pp. 29146–29157, May 2018.

[32] P. Li, Z. Y. Wang, C. S. Wang, X. P. Fu, and Y. Song, "Design of parallel architecture for multi-FPGA based real-time simulator of active distribution network," *Automation of Electric Power Systems*, vol. 43, no. 8, pp. 174–182, Apr. 2019.

[33] A. Shrivastava, E. Earlie, N. D. Dutt, and A. Nicolau, "Retargetable pipeline hazard detection for partially bypassed processors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, no. 8, pp. 791–801, Aug. 2006.

[34] P. Li, C. D. Ding, C. S. Wang, F. Gao, H. Yu, H. T. Li, and X. Y. Huang, "A parallel algorithm of transient simulation for distributed generation system based on multi-core CPU," *Proceedings of the CSEE*, vol. 33, no. 16, pp. 171–178, Jun. 2013.

[35] J. Xu, K. Y. Wang, P. Wu, Z. R. Li, Y. D. Liu, G. J. Li, and W. J. Zheng, "FPGA-based submicrosecond-level real-time simulation of solid-state transformer with a switching frequency of 50 kHz," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 4212–4224, Aug. 2021.

[36] D. N. Hussein, M. Matar, and R. Iravani, "A type-4 wind power plant equivalent model for the analysis of electromagnetic transients in power systems," *IEEE Transactions on Power Systems*, vol. 28, no. 3, pp. 3096–3104, Aug. 2013.

[37] D. G. Xu, W. Wang, and N. Chen, "Dynamic characteristic analysis of doubly-fed induction generator low voltage ride-through based on crowbar protection," *Proceedings of the CSEE*, vol. 30, no. 22, pp. 29–36, Aug. 2010.

[38] Y. Xia, Y. Chen, Y. K. Song, and K. Strunz, "Multi-scale modeling and simulation of DFIG-based wind energy conversion system," *IEEE Transactions on Energy Conversion*, vol. 35, no. 1, pp. 560–572, Mar. 2020.

[39] S. Ebrahimi, N. Amiri, and J. Jatskevich, "Interfacing of parametric average-value models of LCR systems in fixed-time-step real-time EMT simulations," *IEEE Transactions on Energy Conversion*, vol. 35, no. 4, pp. 1985–1988, Dec. 2020.

[40] F. Huerta, R. L. Tello, and M. Prodanovic, "Real-time power-hardware-in-the-loop implementation of variable-speed wind turbines," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 1893–1904, Mar. 2017.

[41] R. Hung and H. W. Dommel, "Synchronous machine models for simulation of induction motor transients," *IEEE Transactions on Power Systems*, vol. 11, no. 2, pp. 833–838, May 1996.

[42] Y. Xia, Y. Chen, Y. K. Song, S. W. Huang, Z. D. Tan, and K. Strunz, "An efficient phase domain synchronous machine model with constant equivalent admittance matrix," *IEEE Transactions on Power Delivery*, vol. 34, no. 3, pp. 929–940, Jun. 2019.

[43] L. W. Wang, J. Jatskevich, C. S. Wang, and P. Li, "A voltage-behind-reactance induction machine model for the EMTP-type solution," *IEEE Transactions on Power Systems*, vol. 23, no. 3, pp. 1226–1238, Aug. 2008.

Zhiying Wang (M'19) was born in Shuozhou, Shanxi, China, in 1990. She received the B.S. and Ph.D. degree in Electrical Engineering from Tianjin University, Tianjin, China, in 2013 and 2018, respectively. She is currently an engineer with the School of Electrical and Information Engineering, Tianjin University. Her current research interests include the real-time simulation and analysis of distributed generation system, microgrids, smart grid and active distribution network.

Hao Fu received his B.Sc. degree in Electrical Engineering from Tianjin University, Tianjin, China, in 2017. He is currently working toward the Ph.D. degree in Electrical Engineering with Tianjin University, Tianjin, China. His current research interests include real-time electromagnetic transient simulation of power system and distributed generation systems.
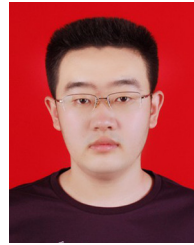
Kun Wang received his B.S. degrees in Electric Engineering from Tianjin University, Tianjin, China, in 2020. He is currently studying for the M.S. in Electric Engineering at Tianjin University. His current research interest is real-time electromagnetic transient simulation of active distribution networks.

Peng Li (M'11) received the B.S. and Ph.D. degree in Electrical Engineering from Tianjin University, Tianjin, China, in 2004 and 2010, respectively. He is currently a Professor with the School of Electrical and Information Engineering, Tianjin University. His current research interests include modelling and transient simulation of power system, operation optimization of distribution networks and integrated energy systems. He is the assistant editor of CSEE Journal of Power and Energy Systems and IET Energy Systems Integration, the young editorial board member for Proceedings of the Chinese Society for Electrical Engineering and Power System Protection and Control.

Jianzhong Wu (M'14) received the Ph.D. from Tianjin University, Tianjin, China, in 2004. From 2004 to 2006, he was at Tianjin University, where he is an Associate Professor. From 2006 to 2008, he was a Research Fellow at the University of Manchester, Manchester, U.K. He is currently a Professor with the Cardiff School of Engineering, Institute of Energy, London, U.K. His current research interests include energy infrastructure and smart grids. Dr. Wu is a member of the Institution of Engineering and Technology and the Association for Computing Machinery.

Xiaopeng Fu (S'14–M'16) received the B.S. and Ph.D. degrees in Electrical Engineering from Tianjin University, Tianjin, China, in 2011 and 2016, respectively. He was a Postdoctoral Fellow in Power Systems Department, Polytechnique de Montreal, Montréal, Canada, in 2007. He is currently an Associate Professor with the School of Electrical and Information Engineering, Tianjin University. His current research interests include analysis of distributed generation system, microgrid, and simulation of electromagnetic transients. Dr. Fu is a member of the Chinese Society for Electrical Engineering.

Chengshan Wang (SM'11) received the Ph.D. degree in Electrical Engineering from Tianjin University, Tianjin, China, in 1991. He is currently the Dean and a Professor of the School of Electrical and Information Engineering, Tianjin University, and the Director of the Key Laboratory of Smart Grid of Ministry of Education, Tianjin University. His research interests include distribution system analysis and planning, distributed generation system and microgrid, and power system security analysis. Prof. Wang is an Editorial Board Member of CSEE Journal of Power and Energy Systems, and an Academician of the Chinese Academy of Engineering.

Jinyue Yan received the Ph.D. degrees from Kungliga tekniska högskolan, Sweden, in 1995. Dr. Yan is a Professor of Energy Engineering, Royal Institute of Technology (KTH) and Mälardalen University, Sweden. He is the Editor-in-Chief of Applied Energy and Editor-in-Chief of Handbook of Clean Energy Systems (Wiley). He is an academician of European Academy of Sciences and Arts. Prof. Yan's research interests include simulation and optimization of advanced energy systems, advanced power generation and renewable energy.