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Impact of thermal oxidation uniformity on 150 mm GaAs- and Ge-substrate VCSELs

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Abstract
Vertical cavity surface emitting laser (VCSEL) devices and arrays are increasingly important in meeting the demands of today's wireless communication and sensing systems. Understanding the origin of non-uniform wet thermal oxidation across large-area VCSEL wafers is a crucial issue to ensure highly reliable, volume-manufactured oxide-confined VCSEL devices. As VCSEL wafer diameters approach 200 mm, germanium (Ge) is emerging as an alternative substrate solution. To this end, we investigate the uniformity of 940 nm-emitting VCSEL performance across 150 mm diameter GaAs- and Ge-substrates, comparing the oxidation method in each case. Nominally identical epitaxial structures are used to evaluate the strain induced wafer bow for each substrate type with Ge exhibiting a reduction of over 100 μm in the peak-to-valley distortion when compared with GaAs. This wafer bow is found to be the principal cause of centre-to-edge oxidation non-uniformity when utilising a conduction-heated chuck furnace, in comparison to a convection-heated tube furnace. Using on-wafer testing of threshold current, differential resistance, and emission wavelength, device performance is demonstrated for the first time across a 150 mm Ge wafer, and is shown to be comparable to performance on GaAs substrates, when the effects of oxidation uniformity are removed. These results provide evidence that there is a realistic path to manufacturing high yield VCSELs, over wafer diameters approaching those used in Si-photonics, via Ge substrates.

Keywords: VCSEL, thermal oxidation, wafer bow, Ge-substrate, GaAs-substrate

(Some figures may appear in colour only in the online journal)

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1. Introduction

High-volume consumer applications of vertical-cavity surface-emitting laser (VCSEL) arrays, especially facial recognition [1, 2] and, more recently light detection and ranging (LiDAR) enabled smart phones, have proliferated in recent years providing motivation for the semiconductor manufacturing industry to transition from 100 to 150 mm substrate sizes to cope with the expanding market. Emerging applications such as autonomous things, augmented/virtual reality and automotive LiDAR demand larger arrays, higher performance, and improved reliability [3, 4]. These new applications are the driving force for lower cost and increased manufacturability of VCSELs with the production of the world's first 200 mm VCSEL wafer already announced [5].

However, the design and epitaxial growth of the active layers on larger area substrates ($>$100 mm) are not trivial. It is widely accepted that gallium arsenide (GaAs) is lattice matched to AlGaAs [6], and for most applications this is a good assumption, however, there is a finite mismatch of 0.16% [7] between GaAs and AlAs. VCSELs have characteristically thick epitaxial layers, due to the large number of mirror pairs required in both upper and lower distributed Bragg reflectors (DBRs), leading to a large inherent compressive strain. It is this strain that induces a convex bow to the epitaxial wafer, creating manufacturability issues such as in photolithography [8] and oxidation processes, as well as unintended wafer breakage. Silicon nitride (SiN_x) can be deposited on the backside of a wafer to reduce, or counteract wafer bow [9], but this increases the number of back-end processes and overall manufacturing time. Other compensative processes that may be used during fabrication also tend to increase fabrication complexity and cost to the customer. The strain and resulting wafer bow increases with emission wavelength due to the increased thickness of the epitaxial layers required to achieve the requisite mirror reflectivity. The growth, design and cost constraints involved when moving towards longer wavelength VCSELs, and/or larger diameter wafers means VCSEL epitaxy on GaAs substrates becomes increasingly challenging for long-term, high-volume manufacturing $\geqslant$200 mm diameters.

Germanium (Ge) substrates are a potential route to high volume, larger area VCSEL manufacturing. One of the benefits of using Ge is that is has a lattice constant that sits between those of GaAs and AlAs [10], allowing for reduced overall structure strain, significantly lowering wafer bow. This makes it an ideal solution for the manufacture of >1.3 μm VCSELs, for future applications such as long-range LiDAR [11]. In terms of mechanical robustness, Ge has a higher fracture toughness value when compared to GaAs [12], and combined with the lower material strain, should result in higher wafer yields from a reduction in losses and breakages. Thermal conductivity, an important factor in device performance, is also not compromised by moving to Ge substrates. In fact, Ge provides roughly a 5% increase in thermal conductivity compared to GaAs [13] allowing for improvements in heat dissipation. Ge also offers advantages such as having perfect crystal quality (zero etch pit density) [14], removing the deleterious effect dislocations can have on device reliability, but also offering a greener alternative. Ge can be infinitely recycled, reducing waste, and allowing for significant cost recuperation per wafer [15]. Most importantly for imminent scale up, 200 and 300 mm Ge substrates are already available with an established, and ever-increasing, supply chain in place for current space-based, solar cell applications [16, 17]. Pushing wafer sizes larger than 150 mm allows for the possibility to fully utilise the advanced CMOS processing tools, bringing it on a par with the high-volume microLEDs-on-Si technology announced in recent years [18]. However, for large scale commercial uptake of Ge substrate structures, where there is resistance to change and working with less familiar materials, a clear demonstration of the benefits for manufacturing and an understanding of the origin of these benefits is necessary and we address that in this paper.

Growth of III–V layers on Ge substrates has been reported with great success recently for various applications [16, 19, 20]. About 980 and 940 nm emitting VCSELs have previously been demonstrated on 150 mm Ge substrates [21], with device performance at 940 nm comparable to GaAs substrate VCSELs, with fabrication completed only on small area tiles. Here, we characterise the difference in wafer bow of each substrate type and compare full 150 mm wafer-scale fabrication and device uniformity, in terms of oxide-aperture variation and performance, for nominally identical epitaxial structures grown on both GaAs and Ge substrates. Wet thermal oxidation of $Al_{0.98}GaAs$, used to create current confinement, is especially sensitive to temperature. Owing to the exponential dependence on temperature of the oxidation rate of buried high-Al content AlGaAs layers [22, 23], a temperature variation can result in a significant difference in oxidation extent across the wafer. Key operating characteristics of VCSELs, including threshold current, beam profile and spectral purity, are highly dependent on the lateral dimensions of the active volume, therefore a large deviation from the desired extent means large disparities in expected device performance. For applications that require single-mode or complex arrays for desired operation [24, 25], repeatable oxidation uniformity is paramount to ensuring scalability and high yields. We compare oxidation uniformity of VCSEL devices on GaAs and Ge substrates, using manufacturing tools that offer different heat transfer mechanisms, conduction, and convection heating, in each case. Conduction-heated furnaces typically offer advantages such as smaller area footprints and *in-situ* camera monitoring with automatic oxidation aperture tracking capabilities making them suitable for R&D applications, over both wafer and small area tiles, but also removing the need for an entire epitaxial wafer to be devoted to calibration purposes, currently standard practise in convection-based tools. This *in-situ* monitoring also allows for confident processing of unknown VCSEL epitaxial structures with no previous oxidation data. Convection-heated furnaces are based on quartz

vacuum tubes allowing multiple large area wafers to be oxidised at the same time, reducing the energy cost per wafer, but tight design tolerance and regular maintenance is required to ensure significant temperature fluctuations do not arise. Further to oxidation variations, there can be spatial variation in the composition and thickness of the high-Al content layer which are also important considerations for oxidation rate [26, 27]. Hence, we also consider the effect of these non-uniformities on final device apertures.

2. Methodology

2.1. Fabrication

The epitaxial structure of the VCSELs produced in this work is a proprietary generic p-i-n layout, designed for 940 nm emission wavelength, and is nominally identical on both n-doped GaAs- and Ge-substrate types. It consists of a multiple quantum-well gain medium sandwiched between upper p-doped AlGaAs/AlGaAs and lower n-doped AlAs/AlGaAs DBR mirrors. The lower DBR also contains a small number of repeats of AlGaAs/AlGaAs, between the active and the start of the AlAs layers. One $Al_{0.98}GaAs$ layer is included just above the active region in the upper DBR to act as a current confinement layer, following oxidation. Four VCSEL wafers in total were used in this work; two on GaAs and two on Ge substrate, with wafers of different substrate type produced in separate growth runs by IQE plc.

Planarisation-free oxide confined VCSELs are fabricated in this study, following a VCSEL quick fabrication process that was previously designed, and reported in detail, in [28]. The VCSEL mesas are defined by an inductively coupled plasma dry etch to just below the active region to allow for the formation of a current confining aperture by wet thermal oxidation. Top p-metal ohmic contacts and bond pads are patterned by a lift-off process of a Ti/Pt/Au stack, to allow for probing of each device individually. A back-side blanket-coat deposition of standard n-contact metals for both GaAs and Ge provides a global contact for each wafer. The process is finished for ohmic contacts on all wafers by an annealing step. The VCSELs were processed into groups of 10×10 arrays on a 250 μm pitch, with 16 groups per tile. Subsequently, full-wafer fabrication involved patterning 96 tiles over the 150 mm wafer.

The wet thermal oxidation step was carried out in either a convection- or conduction-heated furnace. The foremost difference between the tools is the orientation, and hence heating method, of the wafer during the oxidation process; the tube furnace allows up to 25 wafers to be stacked in a vertical position one behind the other, whereas the conduction-heated furnace positions the wafer horizontally onto a heated chuck. Two wafers, one GaAs and one Ge substrate, were oxidised in each tool with a target oxidation extent of 15 μm, measured at the centre of the wafer. Subsequently, the conduction-heated furnace and convection-heated furnace will simply be referred to as the chuck and tube furnace respectively.

2.2. Experimental

The wafer bow of the GaAs and Ge substrates, with the same epitaxial layers, was measured using the autofocus function on a direct-write lithography tool. The measurement was carried out at 351 points across the wafer prior to starting any fabrication processes. For the data produced in this work, all wafers were measured with the crystallographic notch positioned 45 degrees to the bottom left of the central vertical axis.

Monitoring of the oxidation length was carried out *in-situ* at the centre of each wafer using an infrared camera on the chuck furnace, and the wafers in the tube furnace were oxidised from a known oxidation rate after calibration. The oxidation extent at 96 different points across each 150 mm wafer was subsequently determined from current–voltage measurements of circular mesa structures of various diameters. Plotting conductance versus mesa diameter, and fitting with a relevant model allows the oxidation extent to be inferred from the x-intercept. The uncertainty in the oxidation length is given as ± 0.5 μm from the error of the fit.

Following completion of the fabrication, continuous wave power–current–voltage–wavelength (P–I–V–λ) measurements were performed on an automated wafer-prober equipped with a calibrated integrating sphere for light collection, providing measurements of true output powers across the 144 mm edge-to-edge diameter of each wafer.

3. Results and discussion

3.1. Wafer bow

A comparison of the measured wafer surface height, without a backside compensation layer, is shown in figure 1(a) for the VCSEL structures grown on both GaAs; A *(i)* and B *(ii)*, and Ge; A *(iii)* and B *(iv) reference plane for both (a) and (b).* Values reach 130.4 μm and 127.8 μm, for GaAs A and GaAs B respectively, at the very centre of the wafer relative to the edge, which is defined as zero. Here, the error in the height is given as the error in the measurement, ± 0.5 μm. This change in surface height is a concentric radial pattern, resulting in a convex wafer shape with respect to the reference plane, seen in figure 1(b). The black contour lines seen in figure 1 represent a change in surface height of 10 μm. The differences between A and B in each case are likely due to small compositional and layer thickness variations across the wafer affecting the overall level of compressive strain. The Ge wafers, Ge A and Ge B, exhibit a distinctly different shape to the GaAs wafers, with a 'saddle' profile. Here the peak-to-valley distortion, at $x = 0$, is 16.3 μm and 20.2 μm for Ge A and Ge B respectively meaning the Ge substrates have values that are approximately five times smaller than the GaAs, as can be seen in figure 1(b). This undulating height across the wafer is referred to as warp [29], unlike bow seen for GaAs. The magnitude of this height variation, and wafer shape, for Ge substrates with epitaxial layers, is comparable to that seen for a blank Si wafer [30].

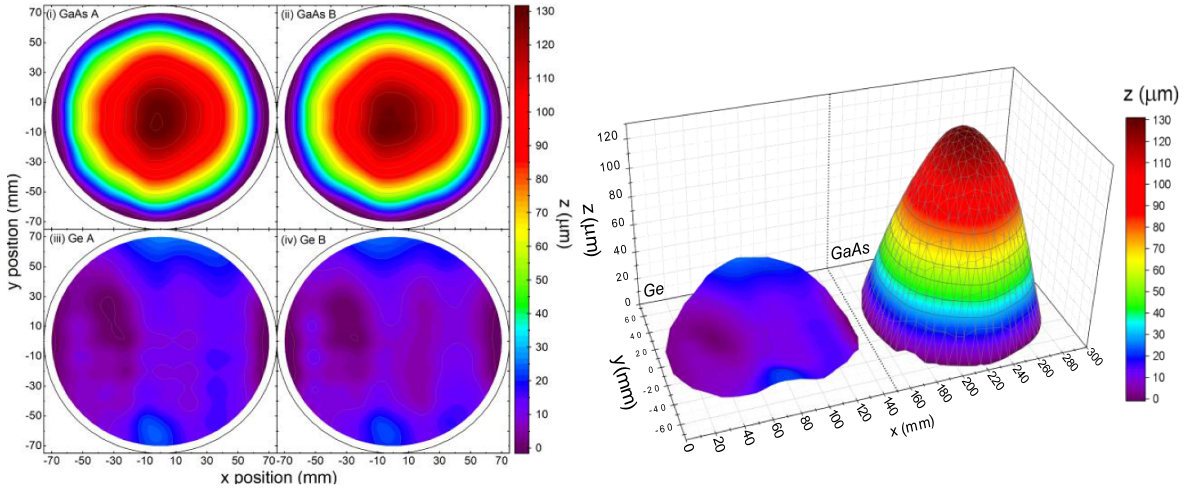

Figure 1. (a) 2D Contour plots showing measured wafer surface height of four nominally identical 940 nm VCSEL structures grown on both GaAs substrates (left); A (i) and B (ii) and Ge substrates; A (iii) and B (iv), and (b) 3D height profile of GaAs wafer A and Ge wafer A (right). The colour scale on the right indicates the surface height in microns.

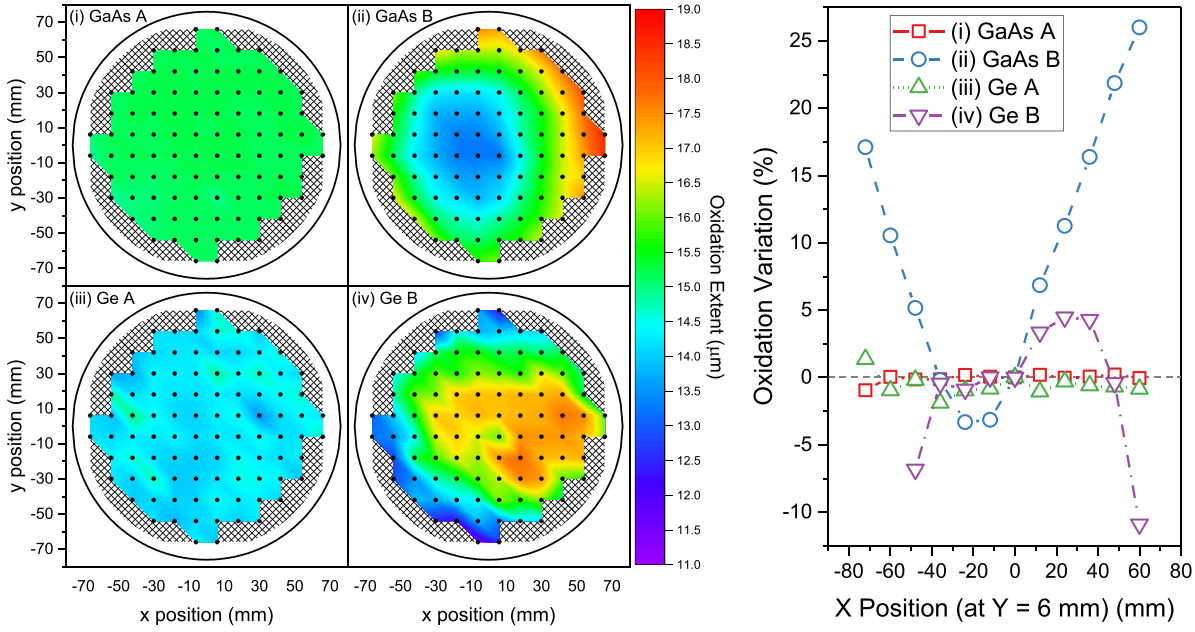

Figure 2. (a) Oxidation contour plots of four nominally identical 940 nm VCSEL structures on different substrate types, oxidised using different manufacturing tools (left). A convection-based furnace was used to oxidise wafers (i) and (iii), and a conduction-based furnace was used for wafer (ii) and (iv). The colour scale on the right indicates the oxidation extent in microns. (b) Line scan of normalised percentage oxidation variation measured across each wafer, measured at $y = 6$ (right).

3.2. Oxidation

We study the oxidation extent variation across each 150 mm wafer, comparing the two different manufacturing heating methods described.

Figure 2 depicts the results of this study when targeting a 15 μm oxidation extent at the centre of the wafer. However, due to inaccuracies, or lack of ability, in measuring the progression of the oxidation extent during the process, all wafers have small variations in the final measured oxide extent at the centre of the wafer. Wafers GaAs A and Ge A were oxidised in the tube furnace and wafers GaAs B and Ge B in the chuck furnace. Wafer GaAs B (ii), oxidised in contact with the heated chuck, shows a maximum centre-to-edge oxidation extent increase of 5.0 μm, or roughly 29%. The change in extent across the wafer has a very similar radial pattern to that seen in the surface height measurements, albeit not as radially uniform. Figure 3 depicts the distribution of the oxidation extent of the four wafers. GaAs A and Ge A both show a narrow distribution, with a standard deviation of 0.06 and 0.27 μm respectively, in comparison with both B wafers. This full wafer distribution correlates to the line scan, at a single point, $y = 6$, in figure 2(b). The distributions show a mean oxidation extent of 15.5, 15.2, 15.5 and 14.2 μm for GaAs A, GaAs B, Ge A and Ge B respectively.

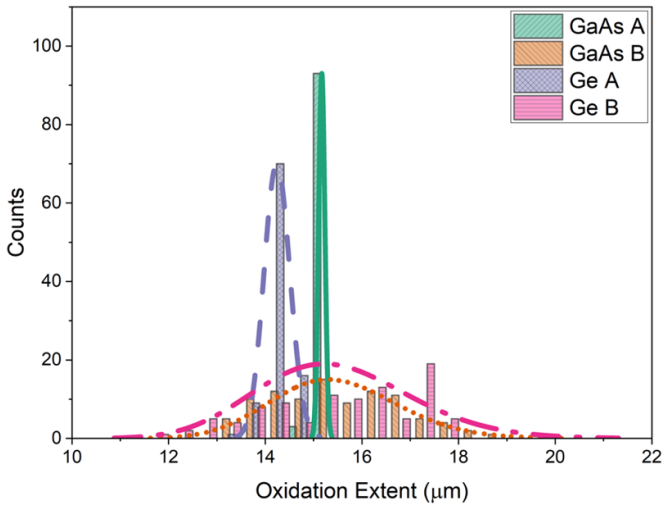

Figure 3. Oxidation extent distribution (histogram), with a normal distribution fit (dashed lines), plotted for each wafer.

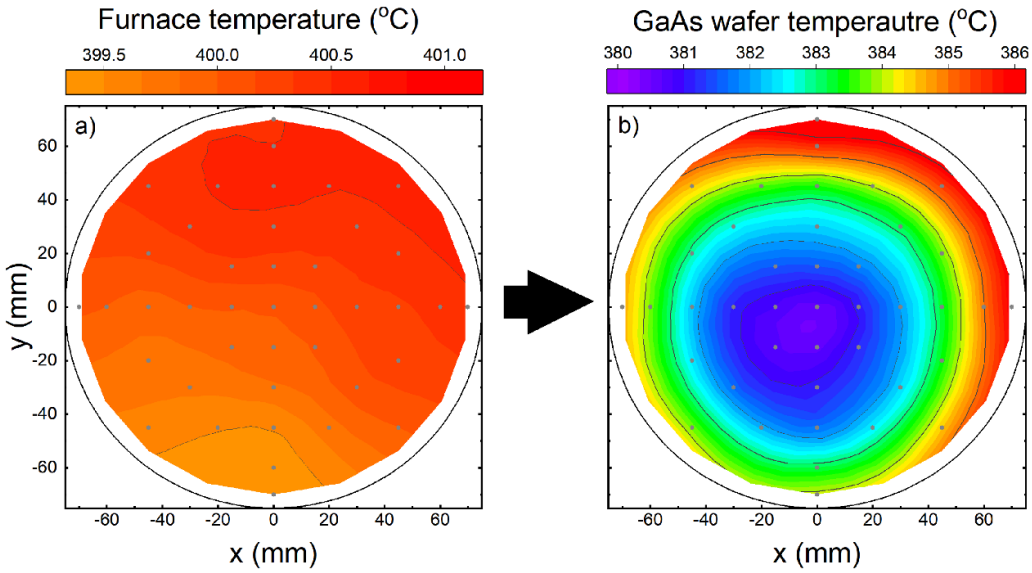

Figure 4. Contour plots of the temperature variation across (left) (a) oxidation furnace chuck with a setpoint of 400 degrees and (right) (b) the resulting GaAs wafer, after heating on (a), when measured with a calibration pyrometer.

Investigation of the furnace temperature across the 150 mm chuck, plotted in figure 4(a), indicates that there is less than 0.7% (2.5 °C) change in temperature, when measured with a pyrometer, at a temperature setpoint of 400 °C. It should be noted that the top and top right-hand edge of the chuck has the highest temperature compared with the other areas, and is, in most part, due to the positioning of the gas injection port at $x = 0$. When the GaAs wafer is placed in the furnace and measured in the same way, the wafer exhibits a 1.2% difference (4.5 °C) between centre to left-hand edge (figure 3(b)), but a 1.6% (6.0 °C) increase centre to right-hand edge due to the furnace temperature variation mentioned previously. With the magnitude of the bow seen on GaAs-substrate VCSELs in figure 1, and the radial temperature pattern of the wafer in figure 4, we conclude that the centre portion of the wafer sits above the furnace chuck, heated from a distance relative to the magnitude of the wafer bow. It follows that the increased oxidation extent seen at the edges of the wafer in figure 2(a) (ii) is due to increased thermal contact of the wafer with the heated chuck at this position compared to the centre regions of the wafer, leading to large variations in the oxidation rate of the $Al_{0.98}GaAs$ layer, a previously reported phenomenon [22, 23]. By investigating the temperature dependence of oxidation rate, of this furnace, we find there to be a difference in oxidation rate of 0.042 μm min^{-1} centre-to-edge, due to the variation in temperature. It should be noted that improvements could be made to this furnace with the addition of vacuum capabilities and other heating compensation or components, but that is outside the scope of this study.

GaAs A in figure 2(a) (i) oxidised in a tube furnace, is measured to have a 0.3 μm extent decrease from centre-to-edge, less than 2% variation. The setup of the wafer in a

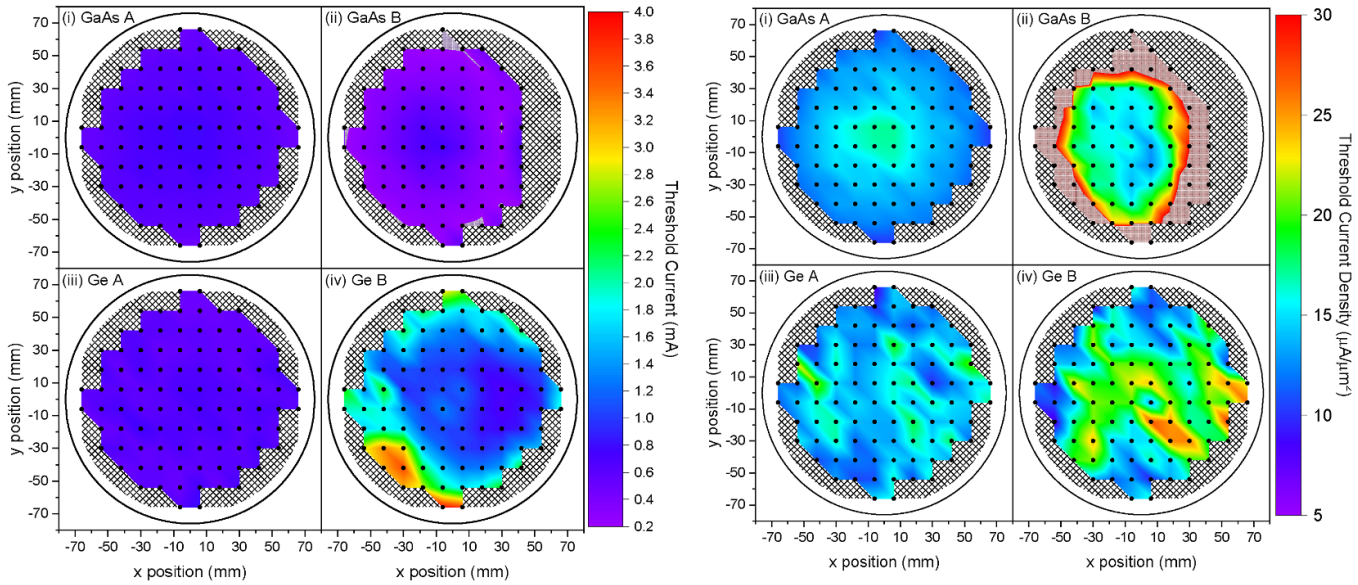

Figure 5. (a) Room temperature threshold current, *I*th, in mA (left) and (b) current density, *J*th, (right), corrected for oxide aperture diameters, in μA μm^{-2}. The red cross-hatched areas indicate areas in (b) indicated *J*th values >30 μm cm^{-2}.

tube furnace ensures a uniform wafer temperature, meaning effects of wafer bow are negligible. Therefore, the results seen in (a) (i) imply that centre-to-edge oxidation variation is driven by any small non-uniformity in the wafer epitaxial layers, rather than any other fabrication non-uniformities [31, 32]. The effect of wafer bow on the oxidation uniformity in GaAs B (ii) is severe enough to obscure these epitaxial non-uniformities in large diameter VCSEL wafers when using conduction heating to control process temperatures. In previous work [33], measurements on cleaved tiles, taken from different radial positions from the centre of the wafer, reported a similar decrease in oxidation extent towards the edge of the wafer.

Ge-substrate wafers show a smaller difference between the two types of oxidation tools. Wafer Ge A in figure 2(a) (iii), oxidised via tube furnace, has an overall oxidation extent difference of 0.5 μm, or 3% variation, whereas wafer Ge B, oxidised via the chuck furnace, has a difference of 2.5 μm or 14%. Here, with wafer bow removed from consideration, we see that the oxidation non-uniformity of Ge A is still driven by the similar small epitaxial non- uniformities as occurred with GaAs A. The variation seen in Ge B does suggest there is also a small non-uniformity contribution from a non-uniform wafer temperature during oxidation. It should also be noted that even with a nominally identical design, the oxidation rate for the epitaxy on Ge substrates is 0.03 μm min^{-1} faster than on GaAs. This was determined from measurements made on individually fabricated tiles (15 mm × 15 mm), to remove the effect of wafer bow and/or temperature with conduction heating. We believe this increase is largely due to the increase in thermal conductivity of Ge, but there may also be a very small contribution from a layer thickness or compositional variation, which is known to also affect oxidation rate [26, 27, 34]. Even so, this suggests that VCSELs grown on large area Ge-substrates can be manufactured with conduction-heated, chuck oxidation and still provide relevant information on the grown epitaxial layers rather than the fabrication process alone.

3.3. Device characteristics

Here, we characterise and outline the spatial dependence of laser performance due to the oxidation length and epitaxial variations. The role oxide aperture size plays in VCSEL characteristics is well understood and the measured room temperature threshold current, *I*th, of nominal 8 μm aperture VCSELs (8 μm diameter taken at the centre of each wafer particular mesa diameter) is plotted in figure 5(a). Wafers GaAs A, Ge A and Ge B all show a 20%–30% increase in threshold current towards the edge of the wafer. However, wafer GaAs B has values that significantly decrease, approximately radially, from centre-to-edge of the wafer, by around 70%. These centre-to-edge disparities, and regions of higher *I*th in Ge B, agree with the oxidation extent variations in figure 2.

Effects of non-equivalent oxide apertures, both across each wafer and between wafers, can be somewhat accounted for by calculating the threshold current density, *J*th. The spatial variation of *J*th is presented in figure 5(b), where each wafer has been corrected for by its relative oxidation extent at each point, for the same mesa diameter. After correction there is a more noticeable centre-to-edge variation in *J*th for both GaAs wafers; a decrease of 4.3 μA μm^{-2} and 15.3 μA μm^{-2} for GaAs A and B respectively. However, this variation in GaAs B does not include devices that have *J*th values significantly greater than 30 μA μm^{-2} which are indicated in figure 5(b) (ii) by the red crosshatched regions. There is a maximum variation of 10.2 μA μm^{-2} and 11.9 μA μm^{-2} for Ge A and Ge B respectively, however, the Ge wafers do not exhibit the same radial pattern in *J*th as GaAs. Correlating variations of oxide extent in figure 2 with those in *J*th, in figure 5(b), confirms,

however, that equivalent mesa diameters do not contain equivalent oxide aperture sizes across the wafer. This is especially true, on a large scale, for GaAs B. Due to the variation of *J*th with oxide aperture, the extremely high *J*th performance at the edge of the wafer is not representative of the overall material performance. Ge A has a mean *J*th value 3.1 μA μm^{-2} lower than Ge B and a standard distribution 4.1 μA μm^{-2} narrower. On the other hand, GaAs A has a mean *J*th value of 13.1 μA μm^{-2} which is 4.1 μA μm^{-2} smaller than GaAs B. The standard deviation of GaAs B is much larger than GaAs A, by 11.5 μA μm^{-2}, but this is a result of the larger spread of aperture sizes across wafer from the temperature gradient in the oxidation process, widening the distribution of measured *J*th values. A further consequence of the large centre-to-edge oxidation variation is the overall device yield, which is a crucial in manufacturing to enable a higher net throughput and a lower cost per wafer [28, 35]. At some edge points of GaAs B, the oxidation extent is long enough to restrict all, or almost all, current flow and reduces representative device yields on the wafer.

The cumulative yield presented in figure 6 of GaAs B indicates there are less than 65% of devices with *J*th values of up to 50 μA μm^{-2}. However, it should be noted that this percentage yield is relevant only for the mesa size and oxidation extent used for this study. A higher yield could theoretically be achieved for GaAs B if larger mesas or a shorter oxidation extent were chosen within the tolerance window required for this device design. In comparison, GaAs A and Ge A both reach 100% at much lower threshold current density, with Ge B having a 100% yield with all devices having *J*th below 30 μA μm^{-2}. Although the tube furnace has a significant advantage in terms of yield for highly bowed GaAs-substrate wafers, there is a much smaller difference between Ge A and Ge B, suggesting conduction-heated oxidation processes can be used for VCSEL manufacture with epitaxy grown on large area Ge-substrates. Similar distributions of *J*th are apparent regardless of absolute values. Differences like these, and between values measured for GaAs and Ge, for the same oxidation process, are largely due to changes in the epitaxial growth uniformity, such as gain peak-to-cavity resonance detuning [36, 37], between growth runs on GaAs and Ge rather than non-uniformities introduced by fabrication processes. Additionally, material composition and layer thickness variation in either of the DBRs can have repercussions on *I*th by altering the total mirror reflectivity of the design, and therefore its threshold gain requirement [35, 38].

Low electrical parasitics are desirable within a VCSEL device to ensure current-induced self-heating does not limit or alter its dynamic performance [39] and other characteristics such as maximum output power, for example. The differential resistance of nominally 8 μm aperture devices is mapped across each wafer in figure 7(a). The distribution of the data and subsequent overlayed normal distribution is plotted in figure 8(a). These have been calculated from individual device *I*–*V* measurements at 1.7 V for each. What is immediately noticeable is the vast difference in the resistance values of wafer (ii), which is the bowed GaAs wafer oxidised in the

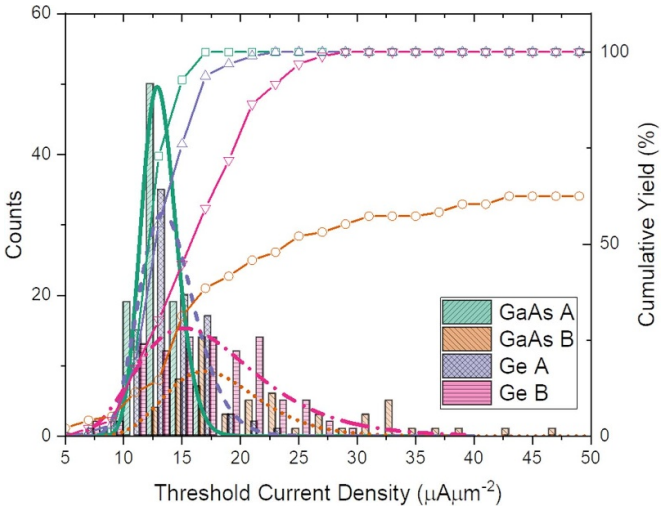

Figure 6. Threshold current density distribution (histogram), with a normal distribution fit (dashed lines) and cumulative percentage yield (open circles) plotted for each wafer.

chuck furnace, to all other wafers. The pattern resembles that seen in figure 5(b) of the threshold current density. This again is a direct result of the larger oxidation extents at the edges of the wafer brought about by the increased thermal contact of a bowed wafer. The red cross-hatched regions in wafer GaAs B indicates resistance values that are beyond the top of the scale bar to the right of figure 6(a), $\geqslant$500 Ω. There is only a very small area of the wafer that represents typical device resistance values when compared to the other wafers, and such high values beyond this region cause high junction temperatures [40], limiting extent of valid data collected for tracking wafer uniformity.

GaAs A has a standard deviation of just 3.8 Ω, whereas Ge A and Ge B have values of 13.8 and 32.4 Ω respectively. The narrow distribution of GaAs A is a direct result of the small oxidation spatial variation, which is also explains the results of Ge B, with low oxidation extent regions matching regions of low differential resistance. However, the results for Ge A are less clear. This wafer has mean differential resistance value of 168.8 Ω, with the previously mentioned standard deviation, of 13.8 Ω.

To ensure that no additional variation in differential resistance has arisen from metallisation, CTLM test structures for the p-contact were measured and characterised. All wafers exhibit an average specific contact resistance value of 1.3×10^{-6} Ω cm^{-2} with no trend on substrate type or oxidation method. These values are consistent with those expected for high-quality ohmic contacts [41]. However, from these structures, the sheet resistance of the highly p-doped GaAs cap layer can also be inferred and are shown for each wafer in figure 7(b). All wafers of the same substrate type show similar sheet resistance values and centre-to-edge uniformity, but wafers Ge A and B have significantly higher sheet resistance values at the centre of the wafer indicating a change in doping profile to GaAs A and B. The normal distribution of the data is plotted in figure 8(b). Here, the data shows that in

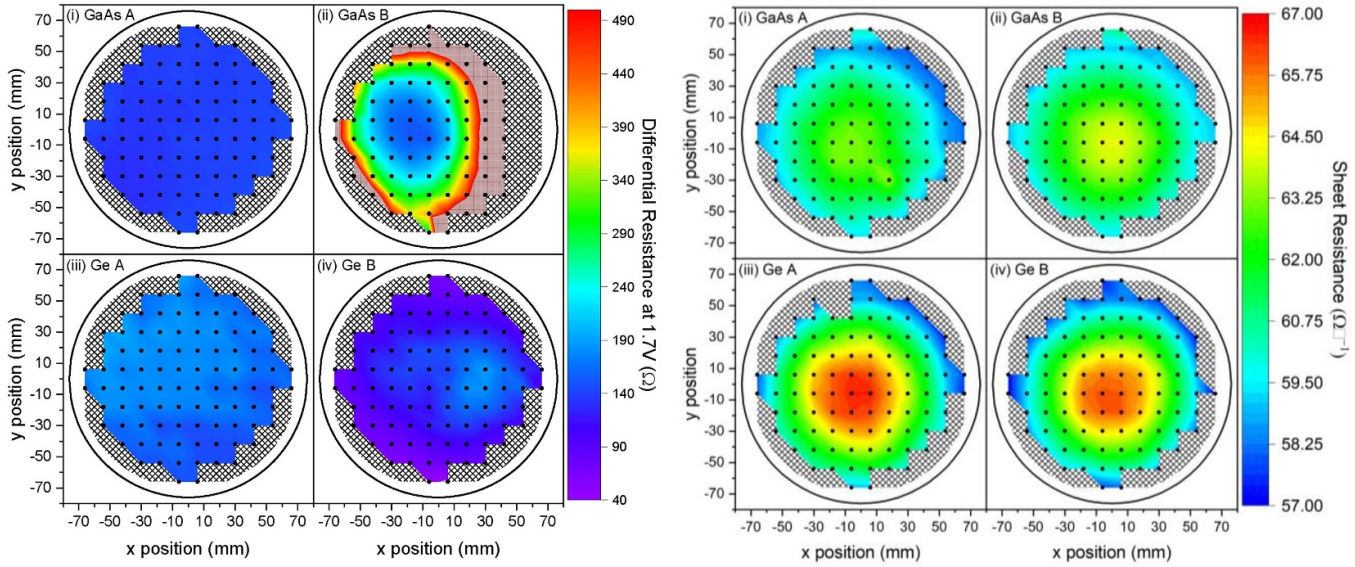

Figure 7. (a) Contour plots of the differential resistance at 1.7 V (left) and (b) sheet resistance (right) of each wafer measured from device *I*–*V* characteristics and CTLM test structures respectively. The red cross-hatched regions in (a) indicate values of differential resistance that are be yond the scale bar to the right, >500 Ω.

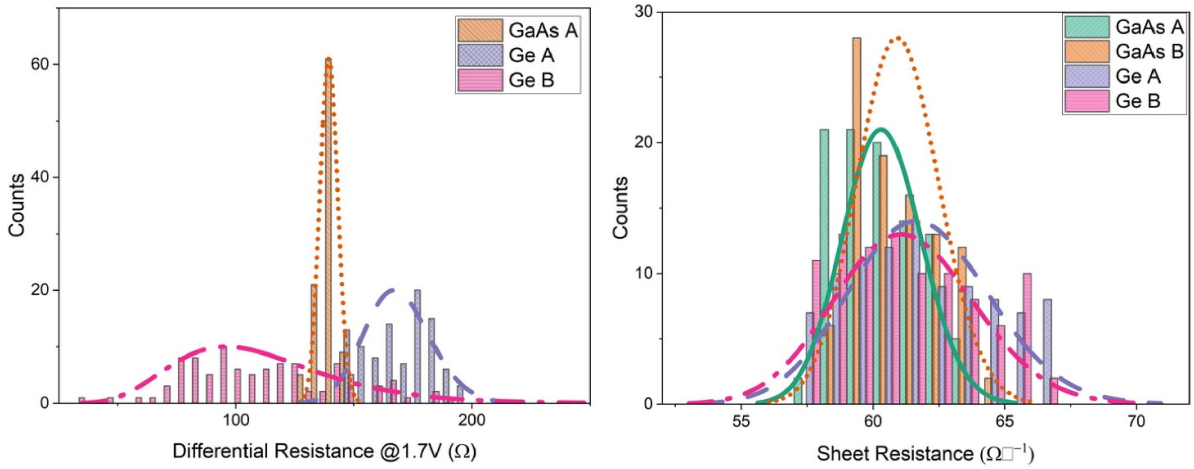

Figure 8. Distribution (hisotgram) of (a) specific contact resistance (left) and (b) sheet resistance (right) with a normal distribution fit (dashed lines) plotted for each wafer.

fact all wafers have mean sheet resistance within 1.4 $\Omega\bullet^{-1}$ of each other. However, the standard deviation varies between substrate type, with values of 1.5–2.7 $\Omega\bullet^{-1}$ for GaAs A to Ge A which also correlates to the results in figure 7(b). Growth conditions were kept constant for both substrate type wafers, minus nucleation [5], so heating and bow effects of Ge-substrate material have not been accounted for at this stage of development, which is likely to have an impact on the different trends in the uniformity of various device performance parameters seen here.

One of the most useful parameters in characterising epitaxial growth variations is the emission wavelength. Although the material cavity resonance wavelength can be measured directly from a wafer without any fabrication, the emission wavelength can differ to a small degree due to an induced red shift of the wavelength, owing to self-heating effects from electrical pumping [42]. The lasing wavelength of nominally 12 μm aperture devices is mapped across each wafer in figure 9(a).

Larger aperture devices are chosen here so that the lasing wavelength is unaffected by aperture size. All wafers exhibit radial emission wavelengths with a centre-to-edge decrease of 8.9 nm, 10.4 nm, 6.8 nm and 6.5 nm for GaAs A, GaAs B, Ge A and Ge B, respectively. From figure 10, the wafers have mean emission wavelengths of 936.8, 936.6, 938.1 and 940.2 nm for GaAs A, GaAs B, Ge A and Ge B, respectively. Further to the larger variations in *J*th and differential resistance between Ge A and Ge B, Ge B has emission wavelengths red shifted by

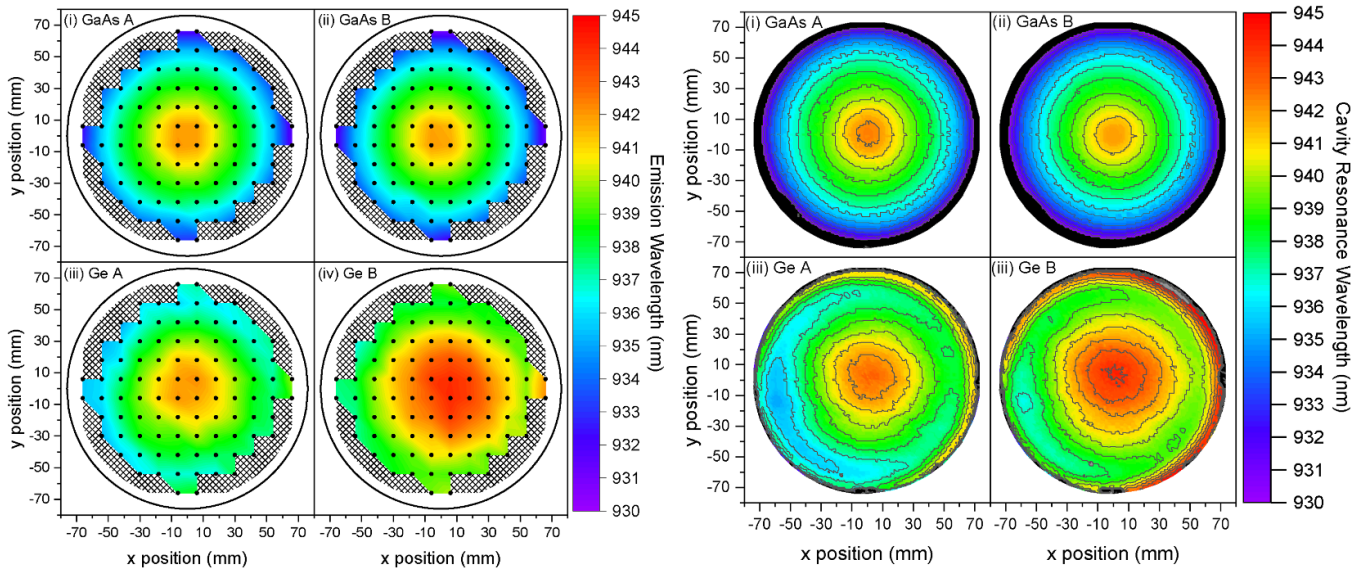

Figure 9. (a) Device emission wavelengths (left), and (b) reflectometry measurements of the cavity resonance wavelength (right), spatially mapped across each wafer.

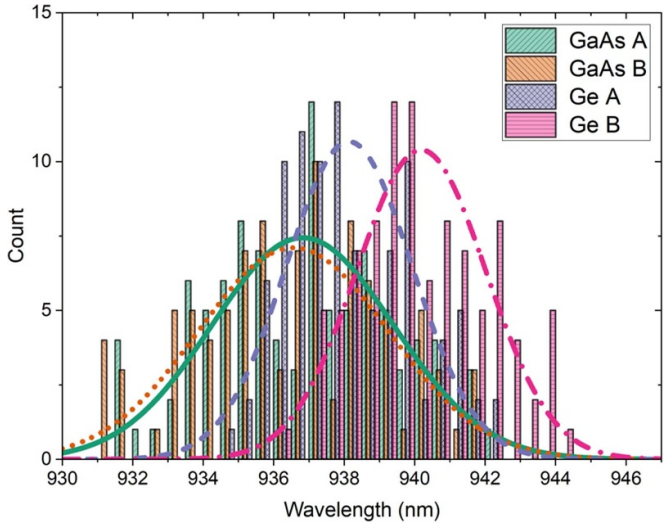

Figure 10. Wavelength distribution (histogram) with a normal distribution fit (dashed lines) plotted for each wafer.

$\sim$3.0 nm across the entire wafer. However, the spatial variation of this shift to longer wavelengths does not correlate to the same spatial variations seen in oxidation and differential resistance that may be a cause of this. The evidence presented so far for Ge B somewhat suggests that even though from the same growth run as Ge A, it has a change in the spatial variation of the material cavity resonance. This can be confirmed by using reflectivity data taken post growth to extract the spatial dependencies of the cavity resonance wavelength. The results of GaAs A and GaAs B are shown in figure 9(b) (i) and (ii) and Ge A and Ge B in figure 9(b) (iii) and (iv). The spatial variation trends of the cavity resonance seen for each wafer match well with the emission wavelength validating the argument that changes in emission wavelength are due to small changes in wafer-to-wafer uniformity [43] and not an artefact of the oxidation process or aperture size.

One further note is that although both Ge wafers have slight red shifts in the central emission wavelengths, the distribution across the wafer is somewhat narrower. Ge A and B have a standard deviation of 1.8 nm whereas GaAs A and B show deviations of 2.6 and 2.7 nm respectively. Currently, it cannot be specified if this distribution is in part to the growth conditions, substrate type itself or a combination of these and additional factors.

4. Conclusions

In summary, the impact of thermal oxidation uniformity on VCSEL performance has been demonstrated over 150 mm diameter wafers. We have compared different methods of thermal oxidation to create the current confinement on both GaAs- and Ge-substrate materials. Our findings confirm the importance of this oxidation process on overall device performance, and more importantly yield, especially on substrates with large amounts of wafer bow, when using a conduction-heated chuck furnace. Convection-based tube furnaces do provide advantages in these situations, but conduction-heated furnaces do still have a place in certain applications, such as where *in-situ* monitoring may be required. Parameters such as oxidation uniformity, threshold current density, differential resistance and emission wavelength are comparable between devices of different substrate type, however, Ge offers additional advantages to the widely used GaAs. These include a tolerance to the oxidation manufacturing process allowing for a wider range of customer markets due to the reduction in wafer bow, as well as a reduction in crystal defects and a potentially greener alternative for the imminent move to establish $\geqslant$200 mm VCSEL manufacturing.

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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