Active Control of Medium-Voltage Cascaded Three-level Neutral-Point-Clamped Converters

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A thesis submitted for the degree of

Doctor of Philosophy

December 2022

Acknowledgement

The PhD study now comes to an end luckily with lots of fruitful learnings and findings. I have gained and developed a lot during this period of time, which is invaluable for the rest of my life.

Firstly, I would like to express my sincere gratefulness to my main supervisor Dr. Wenlong Ming. He gave me a lot of insightful training during my research and helped me find the ideas and methods of doing research. His rigorous academic attitude and selfless work spirit have set a good example for my future career development.

I would like to express my great thankfulness to my co-supervisors Prof. Nick Jenkins and Prof. Carlos Ugalde-Loo. They gave me a lot of encouragement, and meanwhile, gave me a lot of suggestions worth thinking about in depth, which are very helpful for my future life.

I thank all the friends and colleagues that gave me help on either life or work during this time. In particular, I would like to thank Dr. Sheng Wang, Dr. Peng Yang and Miss Chen Li for their great help on my work.

I would like to thank Cardiff University for providing me the opportunity of study. I would also like to thank the projects FLEXIS, DEDSO and Supergen Energy Networks Hub for their funding on my research.

Finally, I would like to express my sincere thankfulness to my parents and all other family members. It is your warmth, encouragement and help that give me the love, courage and willpower to overcome one difficulty after another.

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Abstract

Three-Level Neutral-Point-Clamped (3L-NPC) converters have been widely used in the high-power motor drives. In recent years, a novel cascaded 3L-NPC converter has been developed and adopted in the ANGLE-DC project – a 30 MVA MVDC link demonstration project in North Wales, UK. This cascaded configuration provides exceptional waveform quality, modular design and a cost-effective solution to MVDC applications.

Although the control strategy for a single 3L-NPC converter has been well established, control of the cascaded 3L-NPC converter is still under-researched. The potential challenges to control strategy design arising from their cascaded connections need to be specifically explored. In particular, due to the series DC connection, the voltage imbalance across 3L-NPC submodules (SMs) may occur and influence the system stability. This issue may occur in converter stations where power is controlled in either point-to-point or multi-terminal systems. Beyond the electric characteristic, thermal characteristic is also vital to the performance of system. Thermal imbalance of 3L-NPC SMs may occur in a cascaded 3L-NPC converter even the voltage and power are equally shared, which poses great challenges to the system reliability.

To address aforementioned challenges, this thesis developed suitable control schemes for the cascaded 3L-NPC converter system and demonstrated their operation using a 30 kVA MVDC testbed based on the real ANGLE-DC project. The DC voltage imbalance was analysed through a small-signal model-based approach. Two DC voltage balancing methods with and without communications were presented. The PI-based method can automatically switch to the droop-based method upon failures of communication. The DC voltage imbalance of the cascaded 3L-NPC converter is further investigated in a three-terminal MVDC network in consideration together with the interactions of control characteristics between different converter stations and the power control accuracy. Then suitable control scheme was proposed. Multiple crossovers due to the interactions are avoided while DC voltage balance and power control accuracy are achieved as well. To mitigate the thermal imbalance, a thermal sharing controller was superposed on the DC voltage balancing controller to regulate the active and reactive power of each SM according to their individual junction temperatures. The thermal stresses are hence equally shared in presence of mismatched component parameters and cooling system failures. The effectiveness of presented methods in the thesis has been verified in MATLAB/Simulink simulation and experimentally validated.

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Nomenclature

Alternative-Current Circuit Breaker	ACCB
Carrier Disposition-based Sinusoidal PWM	CD-SPWM
Cascaded H-Bridge	CHB
Dual Active Bridge	DAB
Distributed Generator	DG
Direct-Current Circuit Breaker	DCCB
Discontinuous Pulse-Width Modulation	D-PWM
Full-Bridge	FB
High-Voltage Direct-Current	HVDC
High-Voltage Alternative -Current	HVAC
Half-Bridge	HB
High-Frequency	HF
Input-Series-Output-Parallel	ISOP
Input-Series-Output-Series	ISOS
Input Voltage Sharing	IVS
Low-Voltage Direct-Current	LVDC
Low-Voltage Alternative -Current	LVAC
Medium-Voltage Direct-Current	MVDC
Medium-Voltage Alternative-Current	MVAC
Multi-Terminal Direct-Current	MTDC
Modular Multilevel Converter	MMC
Model Predictive Control	MPC
Output Current Sharing	OCS
Photovoltaic	PV
Power Electronic Building Block	PEBB
Pulse-Width Modulation	PWM
Phase-Locked Loop	PLL
Quasi-Square-Wave	QSW
Quasi-Two-Level	Q2L

Resonant Modular Multilevel DC/DC Converter	RMMC
Return on Investment	ROI
Sub-Synchronous Resonance	SSR
Single-Phase-to-Ground	SPG
Submodule	SM
Sinusoidal PWM	SPWM
Space-Vector PWM	SVPWM
Switch Position	SP
Three-Level Neutral-Point-Clamped	3L-NPC
Total cost of the ownership	TCO
Voltage Source Converter	VSC

Chapter 1

Introduction

This chapter introduces the background, motivation, objectives, and contributions of this thesis. An outline of the thesis is also provided.

1.1 Background

In response to the growing demand for decarbonization and the implementation of net-zero policies, renewable energy technologies have experienced rapid advancements. Distributed generators and energy storage devices are increasingly being integrated into distribution networks. However, their successful integration necessitates precise and flexible control over power flow. Medium-voltage direct-current (MVDC) technology has emerged as a recent development that offers improved controllability of power flows, enhanced power transfer capabilities, and better control over network voltages. These advancements are made possible through the utilization of MVDC converters. Despite these advancements, the control and operation of MVDC converters remain areas of ongoing research. In-depth understanding of these aspects is crucial to ensure the safety and desired performance of MVDC operations.

1.1.1 Renewable Energy Collection and Integration

Renewable sources, such as wind and solar power, are gradually replacing conventional gas and petrol as clean energy alternatives. This shift not only contributes to carbon reduction targets but also helps mitigate the energy crisis by reducing reliance on non-renewable resources.

In recent years, the United Kingdom has witnessed a significant surge in renewable electricity generation and capacity, driven by its commitment to achieving net zero carbon emissions by 2050. Figure 1.1 illustrates the percentage share of UK's electricity generation during the period of 2015-2020.

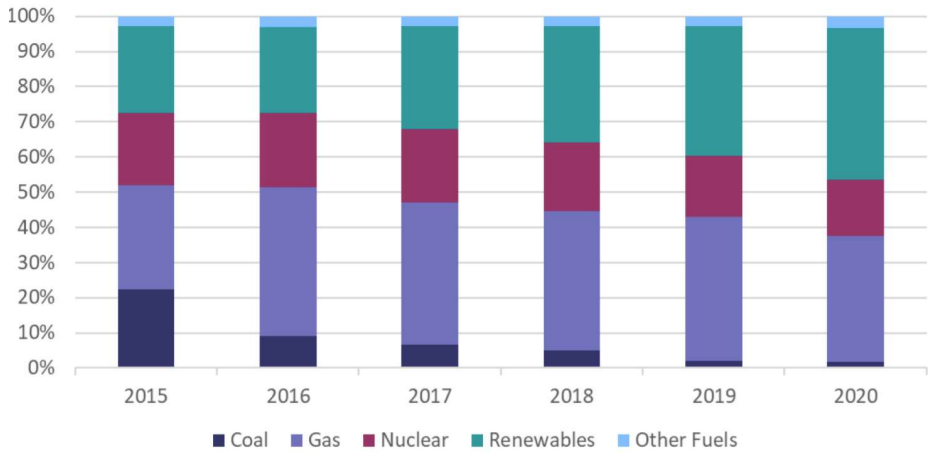


Figure 1.1. Shares of electricity generation by fuel [1].

For the first time in the recorded data series, renewable sources surpassed fossil fuels in their contribution to electricity generation in 2020. The proportion of renewable energy rose significantly, accounting for 43.1% of the total UK generation.

Figure 1.2 displays the distribution of renewable electricity generation by technology across different UK nations. It is evident that England and Scotland are the primary regions with concentrated renewable energy generation. In England, wind, solar, and bioenergy are the dominant sources, whereas in Scotland, wind, hydro, and bioenergy play a major role. Wind generation stands out prominently in both nations. As part of its commitment to achieving net zero carbon emissions by 2050, the UK plans to increase its offshore wind generation capacity to 40 GW by 2030, thereby surpassing 50 GW of overall wind capacity.

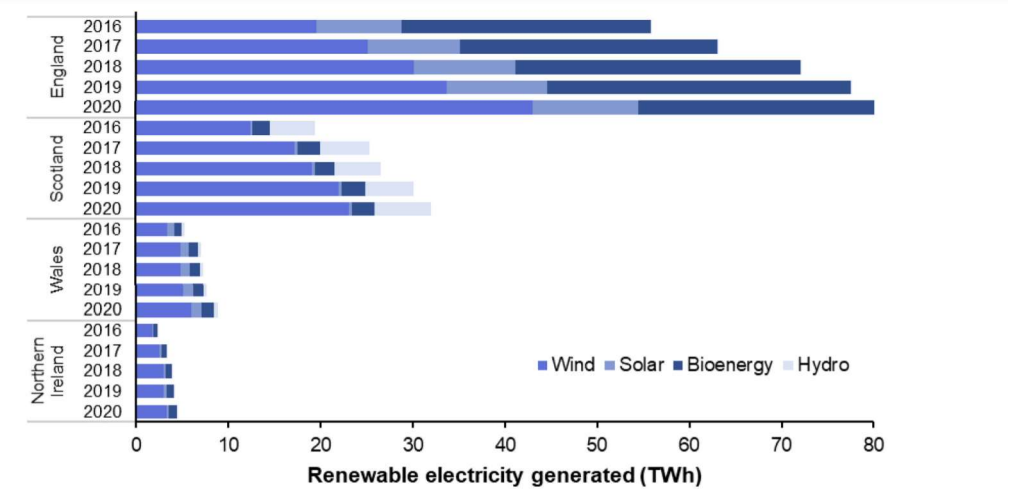


Figure 1.2. Renewable electricity generation by technology in each UK nation [2].

However, with the large-scale renewable energies and loads being integrated, the power quality and reliability may become concerned issues. These require suitable power distribution technology in place to participate in power transmission and regulation.

1.1.2 Development of MVDC Distribution Networks

Motivated by external and internal driving forces, the MVDC has become an important enabling technology in distribution networks. Figure 1.3 shows the distribution of the driving forces.

For external driving forces, the integration of distributed generators (DGs) and energy storage and growth of DC loads are two stimulating factors. Take an example of the solar photovoltaic (PV) integration (see Figure 1.4). In the conventional scheme in Figure 1.4(a), the low-voltage DC (LVDC) generated by different groups of PV panels are first transformed to low-voltage

AC (LVAC) through DC/AC converters. Then, a multi-winding transformer is used to boost the LVAC to Medium-Voltage Alternative-Current (MVAC). Therefore, the power from different groups of PVs are collected by the MVAC grid. To make connection with the grid at high voltage, a MV-to-HV transformer can be used. The alternative option using the MVDC collection is shown in Figure 1.4(b). As can be seen, The DC/DC converters collect the PV plants and connect to the MVDC grid, instead of the MVAC grid. For the connection between MVDC and HVDC grids, an MV-level DC/AC converter acts as the interface together with a booster transformer. In the conventional AC circuit, capacitive effect causes higher leakage currents through the insulation material of a cable, so that less load current will be delivered to the end user. Also, ccompared with the AC circuit, DC operation has better controllability on the AC voltage regulation by using power electronic converters. Thus DC operation has larger power supply capacity than traditional AC operation [3]. Also, as the skin effect, proximity effect and eddy current effect are reduced in DC system, the efficiency can be improved. For example, Skin effect occurs in conductors carrying high frequency AC currensts where the current tends to concentrate towards the surface of the conductor, reducing the effective cross-sectional area available for the current. This results in increased resistance and power loss in the conductor. Another external driving force is the growth of DC loads. As more and more loads are naturally supplied by DC, the transformation of DC to AC can be avoided compared with the traditional MVAC distribution.

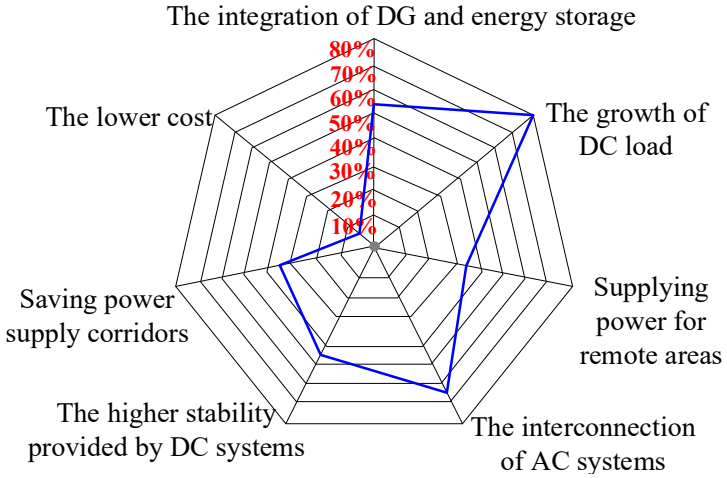


Figure 1.3. The most important driving forces for the development of DC power distribution (the percentage represents the weight of each factor) [3].

For internal driving forces, the MVDC can provide better performance of the power and voltage regulation. The main advantages include: the power and voltage control become more flexible as the AC grids at the DC terminals can be independently controlled regardless of the

mismatches of frequency, phase angle and voltage magnitude; the fault at one AC grid can be avoided to propagate to another side, thus improving the stability of the system; the power quality can be improved since the VSC can be used as the active power filter and reactive power compensator such as the STATCOM.

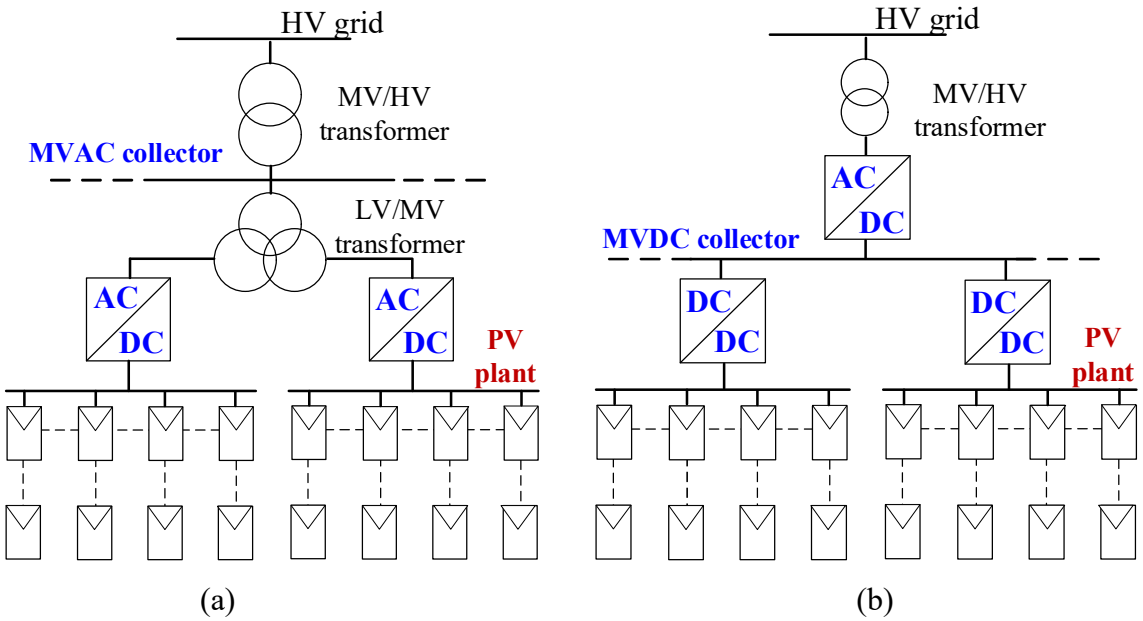


Figure 1.4. Collector grid topologies for a PV application: (a) MVAC collector grid; (b) MVDC collector grid [4].

The MVDC technology mainly includes stability analysis and control of MVDC power electronics, reliability evaluation and DC protection.

As large-scale distributed generators (DGs) and loads are integrated into the grid, the system's stability is impacted, primarily due to a reduction in system inertia. As more power electronic based devices are replacing the synchronous generators, the inertia provided by the synchronous generators is decreasing. The adverse impact is that the system transient and dynamic stability are influenced, thus the system is more susceptible to the disturbance of the grid frequency and voltage [5]. Also, as more DC links are integrated, the interactions between DC and AC system may pose concern of stability. The DC fault may propagate to AC side, and in this case, the voltage and frequency support from the MVDC link will be lost, thus leading to potential instability. Another stability issue is associated with the power electronic converters themselves. As more power electronic converters are connected in series or parallel, the interactions between converters may influence the system robustness. The stability issue requires detailed system modeling and a suitable control scheme. In addition, the coordinated control in the multi-terminal DC (MTDC) systems also attract attention. The voltage and

frequency supporting are supposed to be jointly undertaken by the parallel-connected DGs. The commonly used method is the droop-based control, where there is no centralized controller with communication. When suffering from a failure in one converter station, the others can still take over the power and voltage regulation. Besides, the grid-forming control in island operation, robustness of the power electronic converters and suppressing of the sub-synchronous resonance (SSR) are also attracting attentions from both academia and industry.

System reliability is another important branch. Mass penetration of DGs puts more power components at risk of damage. A key technique is reliability evaluation. The failure rate prediction model is established first. Then, the failure probability and lifetime can be evaluated through analytical and simulation methods. The Monte Carlo simulation is a widely used method due to its suitability for large and complex systems. How to improve computation efficiency is an existing challenge.

For the DC protection, the DC circuit breaker (DCCB) is an under-researched topic. For the conventional AC circuit breaker (ACCB), it takes approximately 40-100 ms until the current is interrupted after receiving the operating command signal from a controller [6]. However, the non-zero crossing of currents during DC faults brings design difficulty to the DCCB. For DC current interruption, it is necessary to intentionally create current zero points. The resonance-type breaker can create a zero crossing of current using an LC resonance circuit (see Figure 1.5(a)). The mostly adopted option is the hybrid type as shown in Figure 1.5(b). The power semiconductor and mechanical switches are used together, where the power semiconductors are used to rapidly interrupt the fault current and the mechanical switches to withstand high voltage difference between lines. Although the technologies of existing HVDC DCCBs are applicable for MVDC applications, the design and selection of MV DCCBs still require special attention to ensure that they are reliable, safe, and can withstand the specific challenges associated with MVDC systems [7], [8]. One of the challenges is the lower voltage level at which MV DCCBs operate. This means that their design and testing must be specific to the voltage level, taking into account the necessary insulation and switching requirements. Additionally, the smaller size of MV DCCBs compared to HV DCCBs can be a challenge, as they need to fit all necessary components within a compact design while still ensuring reliability and safety. Furthermore, compared to HV DCCBs, MV DCCBs are less commonly used and may have limited availability in the market. This may pose a challenge in sourcing and maintaining these components.

To date, limited practical MVDC links have been built [9]–[12]. At Eagle Pass (Texas, USA), a ±16-kV voltage source converter (VSC)-based DC link was built in 2003 to interconnect two distribution networks [9]. At Tangjiawan (Zhuhai, China), a three-terminal ±10-kV MVDC project was trialed in 2018 [10]. At Exebridge (Southwest England, U.K.), through the Network Equilibrium project, a "Flexible Power Link" consisting of two back-to-back VSCs was constructed in 2014 to connect two 33-kV distribution networks [11]. In North Wales, U.K., the ANGLE-DC project was launched in 2017 to adapt an MVAC circuit for MVDC operation. The ANGLE-DC is the first trial of an MVDC link in the Great Britain (GB) electrical power system. It is a demonstration project that enhances the power transfer capacity and thermal capability between the island of Anglesey and Bangor in North Wales by converting an AC transmission corridor into DC operation (see Figure 1.6).

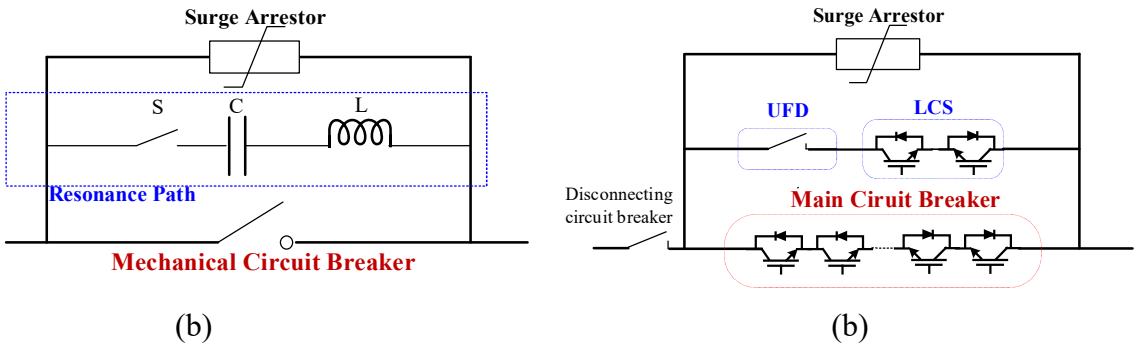


Figure 1.5. DC circuit breakers: (a) LC resonance circuit breaker; (b) Hybrid circuit breaker.

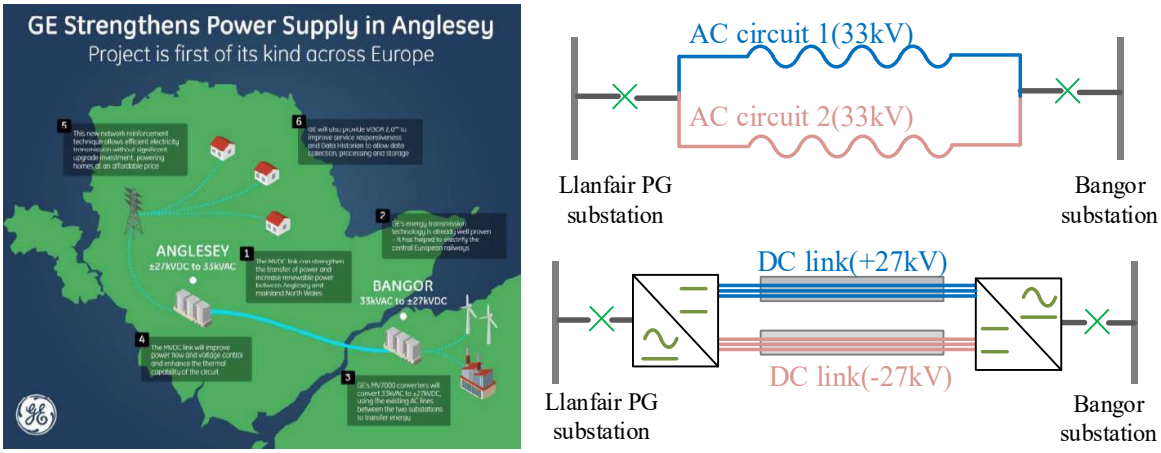


Figure 1.6. MVDC operation in the ANGLE-DC project: (a) MVDC circuit from Anglesey to Bangor (mainland North Wales) [12]; (b) conversion of existing double AC circuit to DC for MVDC operation.

This conversion allows an increased volume of renewable generation to flow mainland from Anglesey without exceeding the thermal limits of existing assets. By converting an existing twin AC circuit at 33 kV to ±27 kV DC, the power transfer capacity between the island of

Anglesey and Bangor (mainland) can be increased by more than 23%, enabling a more distributed generation to be connected on the island [12].

1.1.3 Development of MVDC Converters

The power electronic converter is the key enabler for the MVDC technology. The conventional 2L-VSC and 3L-NPC converter can be selected as the MVDC converter candidates. However, as a single IGBT cannot be able to withstand a high voltage, the IGBT devices are always connected in series to make up a device group, which is named as switch position (SP) [20]. The SP in the bridge arm is shown in Figure 1.7(a) and (b). An issue faced by this configuration is that if one device in the group is damaged, the whole converter will malfunction. From the perspective of the reliability, the power electronic building blocks (PEBBs) are used as the constituent components of converters. Each PEBB is a standardized and modularized submodule (SM), which can be bypassed and easy to maintain in fault conditions. The PEBB-based converter is preferred due to its exceptional waveform quality, compact, and modular design [20]. Such types of converters include input-series-output-parallel (ISOP) and input-series-output-series (ISOS) DC/DC converters, modular multi-level converters (MMCs) and cascaded two-level and three-level converters. Detailed discussions and comparisons regarding the PEBB-based converter topologies are given in Chapter 2.2.

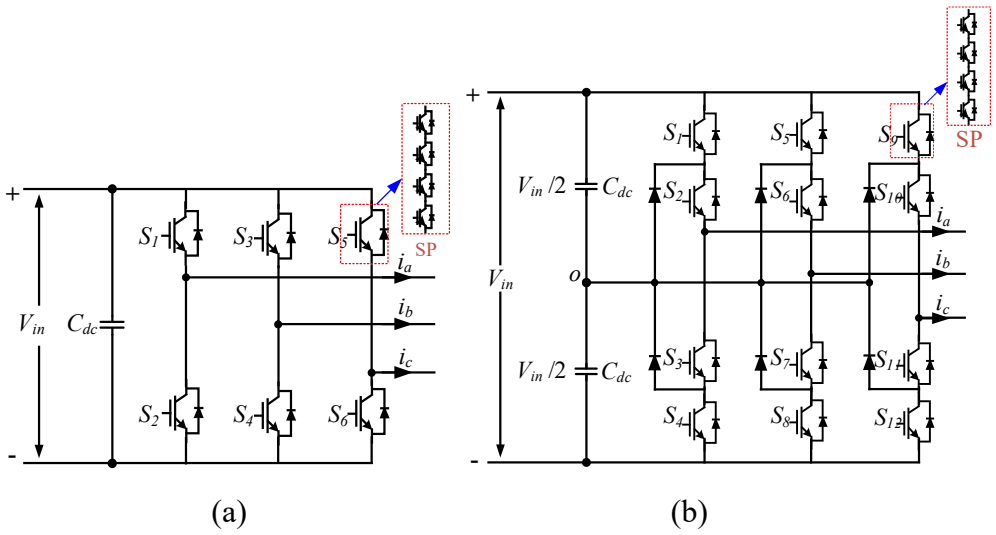


Figure 1.7. SP based 2L-VSC and 3L-NPC VSC: (a) 2L-VSC; (b) 3L-NPC VSC.

1.2 Research Motivation

As discussed in Section 1.1.2, the stability issue resulting from use of power electronic converters is of concern to DNOs. The mass quantities of power electronic devices influence the system reliability, thus leading to large times of maintenance and reduction of the system lifetime. Also, the number of existing MVDC demonstration project is limited, which provides limited lessons and experience to DNOs. The control and operation scheme for MVDC converters are not yet well developed.

Compared with MMCs, cascaded 3L-NPC converters use mature technologies employed for MV motor drives and, in addition, have a relatively low cost and a small footprint [21]. As practical applications are often price-driven, cascaded 3L-NPC converters thus represent an attractive alternative for real projects. For instance, such a converter topology was adopted in the recent ANGLE-DC project, which provides a 30 MVA MVDC transmission corridor in North Wales, UK, between Bangor and Anglesey [12]. The cascaded 3L-NPC converter system consists of *N* three-phase individual SMs. The DC terminals of the SMs are connected in series to build a medium-voltage (MV) level DC voltage, and the AC sides are connected in parallel. An isolation transformer with six windings is used for isolation at AC side. The challenges exhibited in the cascaded 3L-NPC converters are listed below.

1.2.1 Demonstration of an MVDC converter

There are two main challenges encountered when operating an MVDC link based on cascaded 3L-NPC converters. The first one is how to design a suitable control system to achieve a desired performance. As control methods are always topology-dependant and as the cascaded 3L-NPC converter is a novel topology, suitable control methods are still under research. The second one is how to develop an experimental demonstrator to de-risk the practical operation of the MVDC system, as techniques employed in engineering projects should be tested offline before being applied into real applications. Although there are previous efforts assessing the performance of the converter system, most work has been conducted through computer simulations [6], [12] and [14].

1.2.2 Stability Analysis of Cascaded 3L-NPC Converters

A special issue exhibited by cascaded 3L-NPC converters is DC voltage imbalance. As the DC terminals of Submodules (SMs) are connected in series, their shared DC voltages may be different. This may cause SM overvoltage and, potentially, an unstable system operation [15]. Although there are publications addressing the control of a single 3L-NPC converter, the DC

voltage imbalance within SMs of such converter has yet to be investigated and methods for balancing the DC voltages in a cascaded 3L-NPC converter have not been found in public resources. For MMCs, DC voltage imbalance may be also exhibited, but it is attributed to an unbalanced energy distribution in the SMs' capacitors during a fundamental period as these are plugged in and out in an alternating fashion. Since the cause for DC voltage imbalance is different, transferring control methods from MMCs to cascaded 3L-NPC converters to relieve this problem should be done with care.

1.2.3 Multiple Crossovers in a Multi-terminal MVDC System

As more renewable energies integrated into the MVDC networks, the point-to-point system may be expanded to a multi-terminal system. This may pose additional challenges beyond voltage imbalance to the cascaded converters. As the converter stations in the multi-terminal system will adopt different control strategies and hence exhibit different control characteristics, multiple potential operating points (named crossovers) may arise due to the interactions between different control characteristics so that the power and voltage will drift from the original setting points [16], [17]. This may cause overvoltage or overcurrent, and hence a failure in the system. The influence of multiple crossovers on the control of cascaded 3L-NPC converters need to be explored.

1.2.4 Reliable Operation Considering the Thermal Conditions

Reliability have become an important criterion of performance and posed a great challenge to the design and control of power converters. Fifty-five percentage of power device failures is caused by abnormal thermal conditions [18]. High mean temperatures and temperature fluctuations can cause fatigue of package materials of semiconductors, thus leading to damages such as bond wire lift-off and solder crack. For the cascaded MVDC converters, thermal stresses among SMs are practically non-identical due to the mismatched component parameters and individual cooling system conditions of each SM, even though the SMs work at even loading or voltage sharing control. The lifetime of converter systems is determined by the first failed SM. As the temperature imbalance may cause premature damages to certain SMs, the system lifetime will then decrease [19].

1.3 Objectives and Contributions of the Thesis

The objectives and contributions of this work are outlined as:

- Demonstrate the operation of a cascaded 3L-NPC converter-based MVDC link fitted with suitable control schemes. System operation is verified, step-by-step, following a hierarchical approach going from switching level to application level. For completeness, the communication and hardware protection schemes are discussed as well. A 30-kW laboratory scaled MVDC testbed is used to experimentally validate simulation results obtained using MATLAB/Simulink. This testbed has been down-scaled from the ANGLE-DC project, with similar per unit values as those employed in the real system. Using the experimental testbed, a number of simulation scenarios are experimentally verified including the start-up/shut-down procedure of the converter system, steady-state and dynamic performance of DC voltage and power control loops, and transitions between different control modes.
- Analyse the cause of DC voltage imbalance across SMs within a cascaded 3L-NPC converter and present voltage balancing control methods to address this issue, with and without communication. It is revealed that the DC voltage imbalance may occur due to the inversely proportional relationship between the incremental DC voltage and duty cycle within an SM when under power control. This cause is further confirmed by analysing the system model, where each SM is represented as an equivalent impedance as viewed from the DC input terminal. Under DC voltage imbalance, there is an unstable system pole located at the right-half of the s-plane. Two balancing control methods are presented to shift the location of system poles and, hence, to mitigate the DC voltage imbalance: 1) a PI-based control method that requires communication with a central controller and 2) a communication-less inverse-droop-based control method. The communication-dependent PI-based method can achieve a precise balancing control of DC voltages and decoupling from the power controller. Upon loss of communication, the PI-based method is replaced by the inverse-droop-based method to prevent an interruption in system operation.
- Investigate the multiple crossovers due to the interaction between constant I_{dc} and P$-V_{dc}$ droop control in the cascaded 3L-NPC converter based three-terminal MVDC system. The mechanism of the power and voltage drifts caused by the multiple crossovers are first analysed. It is found that the normal operating point is unstable in the condition of multiple crossovers. Then, the droop gain is suitably selected considering both the situation of multiple crossovers and DC voltage balancing performance, with another secondary power compensator being employed to guarantee

the power flow accuracy. Therefore, the multiple crossovers are avoided, and meanwhile, the DC voltage balancing, and power control accuracy are ensured. The presented solution has been experimental validated through a three-terminal MVDC testbed based.

- Present the thermal sharing control of the cascaded 3L-NPC converter to balance the thermal stresses among SMs. A thermal sharing control loop was superposed on the typical current controller within each SM to regulate the active and reactive power according to individual SMs' junction temperatures, with the high-level main controller used to control the total power and calculate the temperature reference. The thermal control capability of this topology was discussed. Considering the thermal control capability, the main controller is used to manage the thermal conditions of the system by monitoring the temperature of each SM. On the one hand, the main controller modifies the temperature references once the outputs of SM's thermal PI regulators reach the upper or lower boundary. On the other hand, even though thermal sharing control is implemented, power semiconductors still have risks of exceeding the maximum allowable temperature in the event of extreme heating conditions. In this case, the converter would be blocked for protection. System modelling and controller parameter design were then presented in detail. The effectiveness of the presented method has been experimentally validated in the cascaded 3L-NPC converters.

1.4 Thesis Outline

The rest of this thesis is organized as follows:

Chapter Two provides a literature review of state-of-art research on MVDC converters. Different converter topologies of the cascaded DC/DC and DC/AC converters are studied. In particular, the performance of MMCs and cascaded 3l-NPC converter are compared regarding the cost, efficiency and reliability. Finally, the control of cascaded converters is briefly reviewed. Two unique issues resulting from using such a type of converter, DC voltage thermal imbalance are pointed out. The corresponding control methods in previous works have also been reviewed.

Chapter Three presents hierarchical control strategy for the basic operation of the cascaded 3L-NPC converters. A high-level main controller with communication is used to send references and commands to converter SMs. The application control loops are included in the

main controller, while the switching-level and converter-level control loops are embedded in the SMs. With the use of a developed MVDC testbed, a series of scenarios were adopted to experimentally verify simulation studies conducted in MATLAB/Simulink.

Chapter Four presents the analysis and mitigation methods for DC voltage imbalance across cascaded 3L-NPC converter SMs. The mechanism of the voltage imbalance is given, followed by an in-depth small-signal model-based analysis. Then, two DC voltage balancing methods are presented, with communication and without communication. For completeness, the hybrid control structure considering partial SMs fitted with communication and others with without communication is discussed. The transition between these two control methods is also given. The effective of the presented method is experimentally validated.

Chapter Five presents the control scheme to eliminate multiple crossovers due to interactions between different converter stations, and meanwhile, to ensure the DC voltage balancing within cascaded 3L-NPC converters. This is achieved by suitable controller parameter design. In addition, a secondary power compensator is presented to ensure the power control accuracy. The effectiveness of the method has been validated through a three-terminal MVDC testbed.

Chapter Six presents an active thermal sharing control to improve the reliable operation of the cascaded converter. The structure of the thermal sharing control loop is presented, with a main controller used to send references. Based on the intrinsic characteristic of the cascaded topology, the thermal control capability is investigated. With a detailed system model, the gain of the thermal controller is suitable selected. The decoupling between the thermal sharing control and the output power control is also theoretically derived. The analyses and the control methods are verified in both PLECS simulation and experimental tests.

Chapter Seven presents the conclusions drawn, main findings and recommendations for future work.

1.5 List of Publications

Journal Paper

[1] J. Chen, W. Ming, C. E. Ugalde Loo, S. Wang and N. Jenkins, "Analysis and Mitigation of DC Voltage Imbalance for Medium-Voltage Cascaded Three-level Neutral-Point-Clamped Converters," *IEEE Trans. Power Electron*, vol. 37, no. 4, pp. 4320-4336, Apr 2022.

[2] J. Chen, S. Wang, J. Liang, R. Navaratne and W.Ming, "Decentralized Control for Multi-terminal Cascaded Medium-Voltage Converters Considering Multiple Crossovers," *IEEE Trans. Power Delivery*, early access.

[3] J. Chen et *al.*, "Demonstration of Converter Control Interactions in MMC-HVDC Systems", *Electron.,* vol. 11, no. 2, 2022.

[4] J. Chen, S. Wang, C. E. Ugalde Loo and, J. Liang, I. Lüdtke, W. Ming, "Active Thermal Sharing Control of a Cascaded Three-Level Neutral-Point-Clamped Converter", *IEEE Trans. Power Electron*, under review.

Conference Paper

[1] J. Chen, W. Ming, C. E. Ugalde Loo and S. Wang, "Laboratory Demonstration of a Cascaded Three-Level Neutral-Point-Clamped Converter for Medium-Voltage DC Transmission," in *CIGRE Session*, Paris, Aug. 2022.

[2] J. Chen, W. Ming, J. Liang, I. Ludtke and S. Wang, "Power Control Strategy for C3L-NPC converters considering thermal conditions," in *IEEE Conf. IECES 2023*, accepted.

[3] W. Ming, J. Chen, J. Wu and J. Yu, "D-suite Technologies for Low-voltage Distribution Networks," in *Int. Conf. CIRED 2023*, accepted.

Chapter 2

Literature Review

This chapter presents a literature review on the technologies of the MVDC converters, including the topologies and control strategies for the cascaded medium-voltage DC/DC and DC/AC converters.

2.1 Topologies of MVDC Converters

2.1.1 Cascaded DC/AC Converters

The cascaded DC/AC converters used in the MVDC applications mainly include MMCs and cascaded 3L-NPC converters. To accommodate the MVDC operation, MMCs have been adapted from the HV level to the MV level and adopted in the previous projects. Apart from the MMCs, cascaded 3L-NPC have been recently used in the MVDC applications such as the ANGLE-DC project launched by Scottish Power Energy Networks (SPEN). Although both the types of converters were considered during the planning stage, the cascaded 3L-NPC converter was finally selected due to its low cost and since its performance meets all industry standards and requirement of UK's distribution system such as harmonic distortion, operating losses, reliability and availability[12], [13] and [20]. In [20], the cascaded 3L-NPC system was compared with an MMC-based configuration in terms of total cost of the ownership (TCO), return on investment (ROI), reliability (reflected as a B10 value which represents the time after which 10% of the components in a population of identical products or systems are expected to fail due to a specific type of failure mechanism. The larger B10 is, the longer the lifetime is expected) and efficiency. The main advantage using the 3L-NPC system is its significantly lower cost, although MMCs have slightly higher reliability and efficiency (e.g., for the ±27 kV DC voltage in Table 2.1, the efficiency and B10 of cascaded 3L-NPC converter are 98.26% and 1.04, compared to those of an MMC which are 5.91 and 99.13%, respectively). As such, the selection of the 3L-NPC converter topology can be seen a compromise among several measures. The detailed comparison provided in [20] is summarized in the Table 2.1.

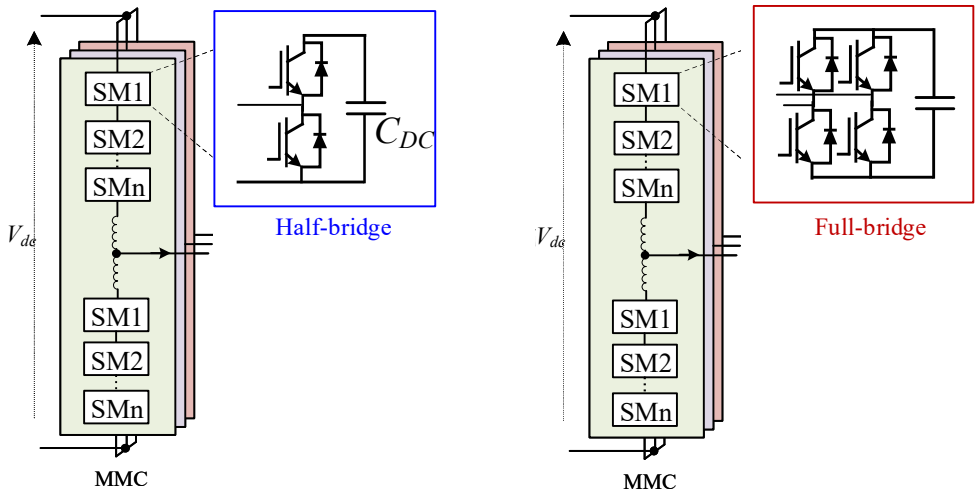
According to Table 2.1, the TCO of a cascaded 3L-NPC converter is lower than the TCO of an MMC at any DC voltage level. For instance, for a ±27 kV cascaded 3L-NPC the TCO is $867,535, which is 17% lower than the cost of a ±27 kV MMC ($1045,470). This is mainly due to larger number of power devices (power semiconductors and passive devices) required in an MMC. Although the ROI of the cascaded 3L-NPC ($ROI_{_C3L\text{-}NPC}$=0.51) is slightly lower than that of the MMC ($ROI_{_MMC}$=0.64), this is due to the higher redundancy level in cascaded 3L-NPC converter. The $ROI_{\_C3L\text{-}NPC}$ will be higher than $ROI_{\_MMC}$ if the two types of converters are at the same redundancy level [20]. This economic benefit makes the cascaded 3L-NPC converter an attractive option in the industry, where most applications are price driven and very cost sensitive.

The cascaded 3L-NPC converter has a slightly lower efficiency and a reduced B_{10} life. For instance, at the ±27 kV DC voltage level, the efficiency and B_{10} life of the cascaded 3L-NPC converter are 98.26% and 1.04 years, compared with 99.13% and 5.91 years of MMC. Hence, for less cost sensitive applications requiring very high efficiency and B_{10} life, adoption of MMCs would be preferable.

TABLE 2.1. CHARACTERISTICS COMPARISON OF MULTI-LEVEL VSCS AT DIFFERENT DC VOLTAGE LEVELS.

Voltage	Topologies	Efficiency (%)	ROI	Redundancy (%)	TCO	B_{10} life (years)
±10 kV	Cascaded 3L-NPC converter	98.06	0.47	100	422,370	1.12
	MMC	98.81	0.49	50	603,769	10.65
±27 kV	Cascaded 3L-NPC converter	98.26	0.51	83	867,535	1.04
	MMC	99.13	0.64	22	1,045,470	5.91
±50 kV	Cascaded 3L-NPC converter	98.48	0.98	80	1,417,603	1.03
	MMC	99.31	1.09	18	1,699,364	5.64

The topologies of the MMCs are shown in Figure 2.1, including the half-bridge (HB) and full-bridge (FB) structures.



(a) (b)

Figure 2.1. MMC topologies: (a) half-bridge; (b) full-bridge.

For the HB structure, each SM is a modularized HB two-level converter. The SMs switch on and off in turn during a fundamental period. This means that some SM capacitors are connected and meanwhile, the rest bypassed. The AC voltage waveforms of the upper and lower arms and the phase-to-neutral voltage are shown in Figure 2.2. As can be seen, the voltages at both arms are superposed with a DC offset, while phase angles of the AC components are complementary (see Figure 2.2(a)). The phase-to-neutral voltage is the difference between the upper and lower bridge arm voltages (see Figure 2.2(b)).

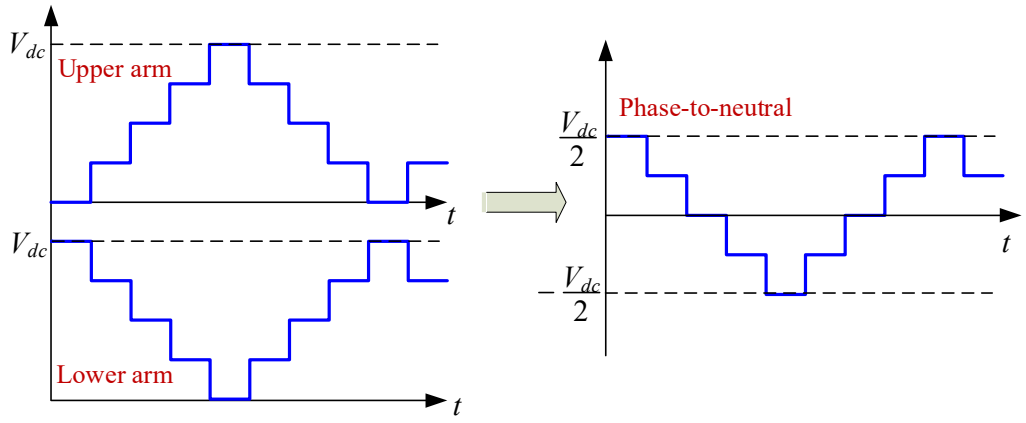
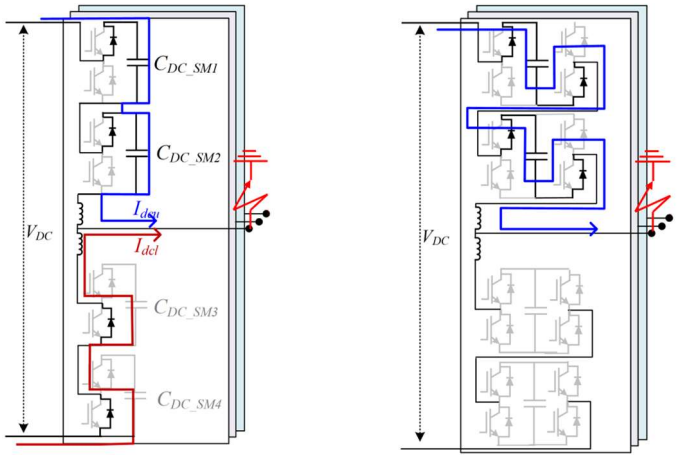


Figure 2.2. AC voltage waveforms of the MMC.

Compared with the FB option, the HB-MMC has lower power losses and capital cost due to the less used power semiconductors. However, the fault blocking capability of the HB-MMCs is inferior to the FB-MMCs. The HB-MMC does not have DC fault blocking capability, thus relies on AC or DC circuit breakers to isolate DC faults. Thyristors connected in anti-parallel to the SM terminals can be employed to bypass the short-circuit current and protect the freewheel diodes. However, this method does not isolate a DC fault and additional devices are required for fast fault isolation. To address the issues of DC faults, the FB-MMCs can be used for isolating the DC fault [22]. Also, considering the compromise between the DC fault blocking capability, power losses and cost, a hybrid structure comprising the HB and FB SMs were presented [23], [24].

Another fault issue is the single-phase-to-ground (SPG) short-circuit, which is also significant although the probability of occurrence is low [25]−[27]. The valve-side SPG faults in bipolar HB-MMCs will lead to grid-side nonzero-crossing currents and overvoltage of the SM capacitors in upper arms of converters. The grid-side AC circuit breaker (ACCB) may have difficulty in interrupting such nonzero-crossing fault currents. The upper arm overvoltage may

damage the SM capacitors and threaten the insulation of the converter. In Figure 2.3(a), when the SPG fault occurs, all IGBTs will be blocked. However, SM capacitors in the upper arms of the two non-faulted phases will be charged through the anti-parallel diodes during every negative half-cycle of the valve-side post-fault AC voltages. Also, due to the free-wheeling effect of diodes and the small resistance in the current paths, the currents flow through the lower arms in the two non-faulted phases are always positive. However, the nonzero-crossing fault currents can be avoided if the FB-MMCs are used. Figure 2.3(b) shows the current flowing path of a FB-MMC in case of the SPG fault. It can be seen that the upper bridge arms still encounter the overvoltage due to the charging of the upper DC capacitors. However, the current does not flow through the lower arms in the two non-faulted phases since all the diodes in the lower arms will be reversed-biased. Thus, there is no DC offset of the fault current and ACCB can be used to interrupt the connection between the converter and grid sides. Therefore, FB-MMCs are more suitable to be used in the situation where isolation of AC and DC faults are required.



(a) (b)

Figure 2.3. Current flow paths under SPG faults: (a) half-bridge; (b) full-bridge.

The cascaded 3L-NPC converters are another promising option for the MVDC application. The MVDC link in ANGLE-DC is based on two controllable VSC stations, as shown in Figure 2.4. For each converter station at the end of the DC circuit of the MVDC link, twelve DC series-connected 3L-NPC SMs are installed to build up the DC voltage to ±27 kV. Sets of six SMs are connected with six-winding isolation transformers (see Tr.ij in Figure 2.4). The isolation transformer is with a vector group connection of Yd11, where the high-voltage (primary) winding is star-connected, and the low-voltage (secondary) winding is delta-connected with a 30-degree lead. A grounding resistor is connected in shunt at the midpoint of the cascaded SMs

to achieve a bipolar operation. Similar to the MMCs, in the case of SPG faults in the AC side of a SM, the SM's DC capacitor will be charged, which causes the overvoltage of this SM. The fault will be more severe when it occurs at the SM closest to the DC link as the capacitor will be charged to the DC link voltage [6]. A measure to address this is adding a thyristor branch in parallel with the DC terminal of each SM to discharge the capacitor, and meanwhile, the AC circuit breakers of both side converter stations are cut off to eliminate the fault current [6].

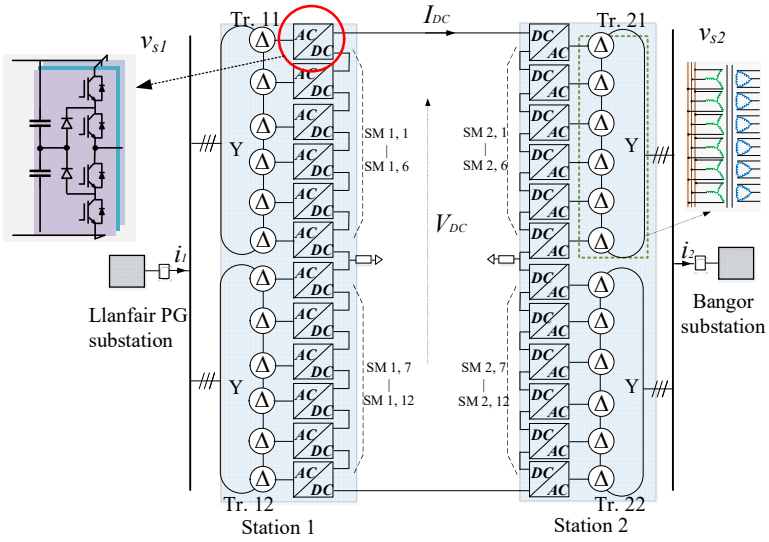


Figure 2.4. Cascaded 3L-NPC converters [12].

2.1.2 Cascaded DC/DC Converters

The cascaded DC/DC converters are mainly categorized as the modular configuration based and MMC based types [28]−[31]. The basic constituent submodule of the modular configuration-based type is a full-bridge dual active bridge (DAB) converter or an LLC resonant converter which consists of two inductances and a capacitor [32]. As shown in Figure 2.5, both types of converters comprise two full-bridge converters, two DC capacitors, a series-connected inductor (and an additional series-connected capacitor for the LLC resonant converter), and a high-frequency (HF) transformer. The HF transformer provides the required galvanic isolation and voltage matching between two voltage levels. The HF transformer is used to deliver the HF square waves of AC voltage with tens of kilohertz from one side to another. Compared with the conventional transformer designed for the sinusoidal waves, the HF transformer has the advantage of low volume, light weight, low cost, and can also avoid voltage and current waveform distortion caused by the core saturation of LF transformers. Also, the soft-switching operation can be achieved in both types to reduce the power losses.

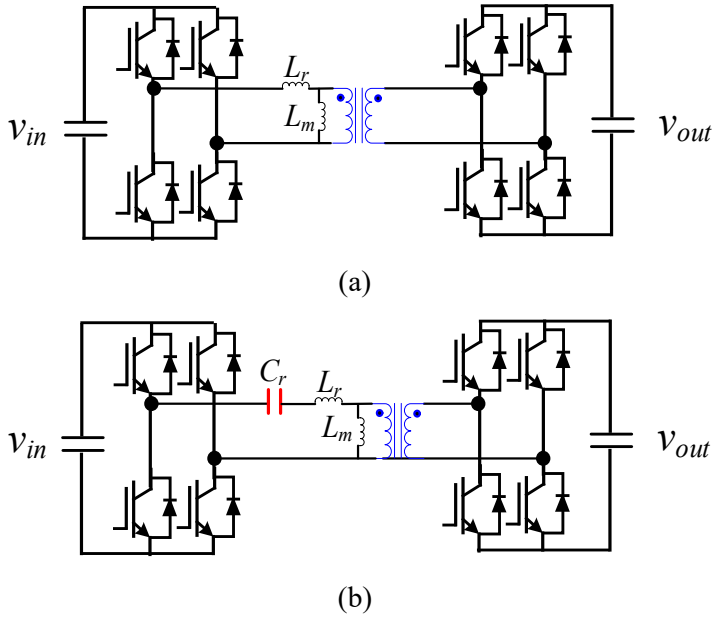


Figure 2.5. Single DC/DC converters: (a) DAB converter; (b) LLC resonant converter.

Individual DAB or LLC converters can be combined at will, to obtain different configurations of cascaded inverters. This is achieved by connecting individual SMs in parallel and series as needed. As shown in Figure 2.6, the general cascaded configurations include input-series-output-parallel (ISOP) and input-series-output-series (ISOS) [33]. The series connection is used for supporting a high DC link voltage while the parallel connection for withstanding a large current stress.

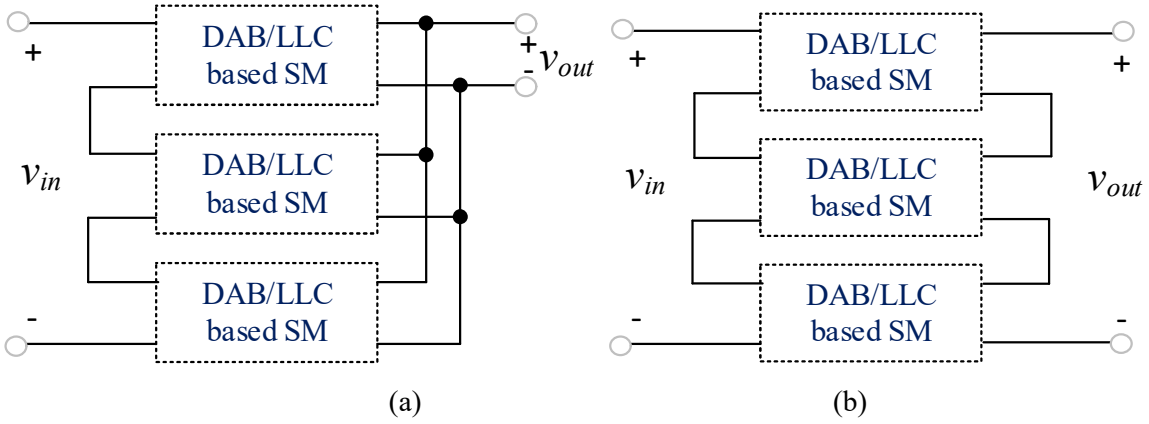


Figure 2.6. Modular configuration of the DC/DC converters: (a) ISOP connection; (b) ISOS connection [33]**.**

Similar to the cascaded DC/AC converters, the SMs also need to be bypassed in fault conditions to ensure continuous operation. To achieve this, a thyristor-based protection circuit can be also paralleled with the DC capacitor to facilitate the bypassing operation upon failures of any SMs

[34]. [35] proposed a protection method and theoretically analysed the influence of bypassing operation on the dynamics of the fault and healthy SMs.

Although the DAB and LLC based modular configuration can achieve the high-power density, set against the advantage is the large potential differences between the primary and secondary sides, which places large stress on the insulation of the transformer windings and other components [36].

Another popular choice is using the MMC based front-to-front DC/DC converter (see Figure 2.7). Two half-bridge or full-bridge MMCs are combined to constitute the DC/DC converter. A medium-frequency transformer with several hundred hertz to several kilohertz can be used to reduce the transformer size, reactors and capacitors [37]. The soft switching can also be achieved for this type of converter. Another advantage is that the DC fault can be prevented from propagating from one side to the other side through suitable control. As traditional HF square modulation could raise high dv/dt in the transformer, the insulation will be affected. To this end, quasi-square-wave (QSW) and quasi-two-level (Q2L) operation were proposed to alleviate the high dv/dt [38]. However, due to the use of two sets of MMCs, the converter system becomes bucky and the volume is increased, thus reducing the power density.

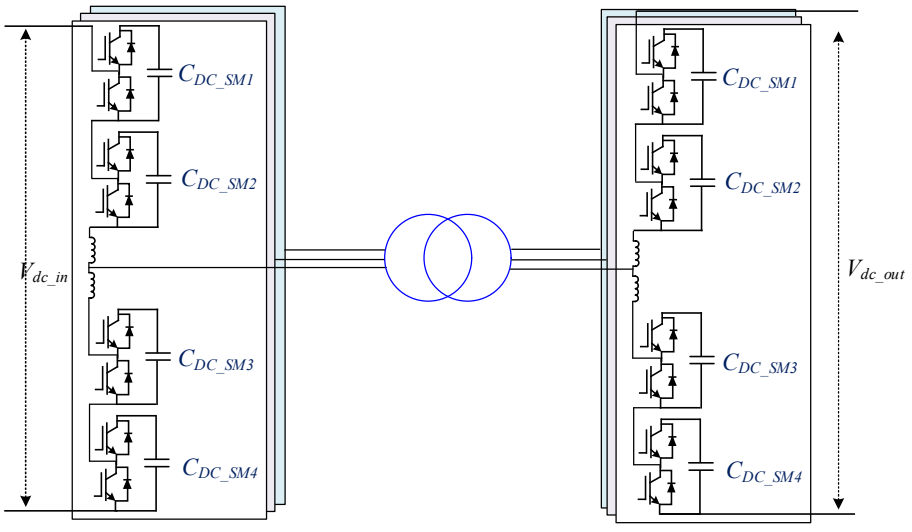


Figure 2.7. MMC based DC/DC converters [37].

Additionally, the MMC based topology can be combined with the LLC resonant topology to form the resonant modular multilevel DC–DC converters (RMMCs) [39]− [41]. RMMCs inherit the advantages of both types of converters and are suitable for the high step-ratio and low step-ratio conversions. The high step-ratio conversion is usually adopted in the connection

between the MVDC and LVDC netwotks, while the low step-ratio conversion is applied in the connection between two MVDC networks with similar voltage levels. The basic RMMCs with high and low step-ratio are given in Figure 2.8 and Figure 2.9, respectively. The reader of interest to the evolution of the high step-ratio converter to the low step-ratio counterpart is refered to [41].

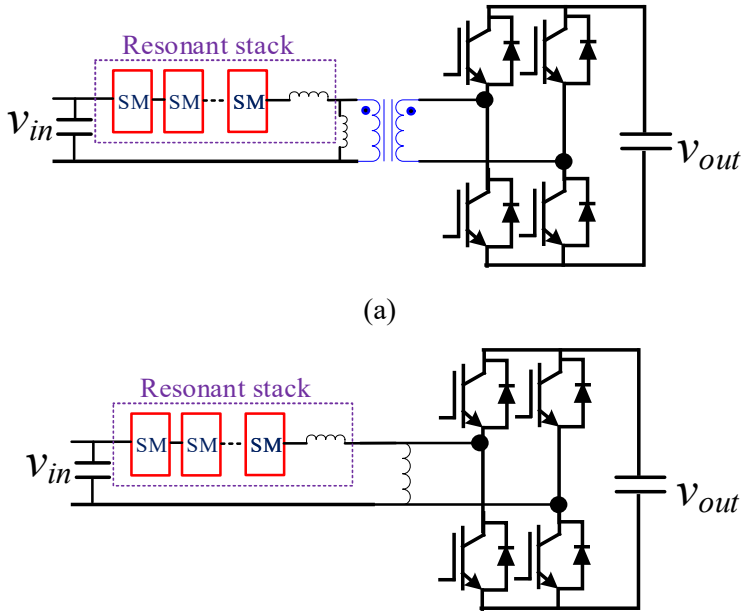


Figure 2.8. High step-ratio RMMC: (a) transformer-coupled RMMC; (b) transformer-less RMMC [41].

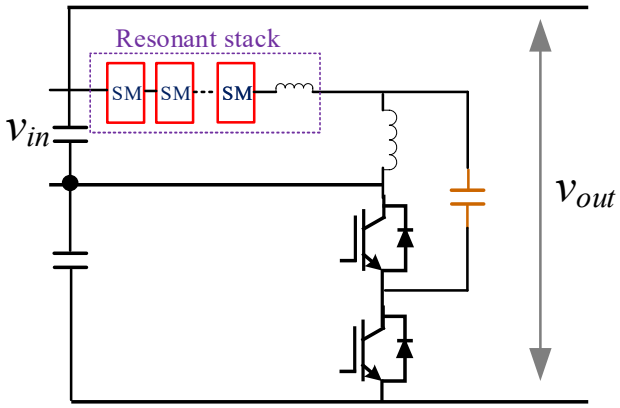


Figure 2.9. Low step-ratio RMMC [41].

2.2 Control of Cascaded MVDC Converters

2.2.1 Voltage and Power Balancing Control

Similar to the general power electronic converters, the MVDC converters can control the active power and reactive power, and also are able to support voltage and frequency of the grid. The

MVDC converters can operate under grid following, grid forming and grid supporting control modes according to different applications[42], [43]. Among the control strategies, the technical challenges introduced by the cascaded topologies should be particularly focused. A common challenge for the cascaded converters such as the MMCs and cascaded DC/DC converters is the voltage imbalance across different SMs' capacitors. Without suitable control in place, the stability issue may arise.

For MMCs, the PWM and nearest level modulation are commonly used. Capacitor voltage balancing control are different regarding the two modulation methods. The PWM methods include the phase disposition methods [44], [45] and phase shifts methods [46], [47]. The turn-on and turn-off of each SM are determined by the comparison between the PWM carriers and the modulation wave. A PI based voltage balancing controller is superposed to the control variables generated by the current controllers to balance the voltage. The schematic is shown in Figure 2.10. In this scheme, the average voltage of each phase ($\bar{v}_{cu}$) is compared with the voltage of the m^{th} SM, the error goes to a PI controller and then generates a compensating control variable and the corresponding duty cycle D_i. Through this closed loop control, the DC voltage of each SM can trace the average value.

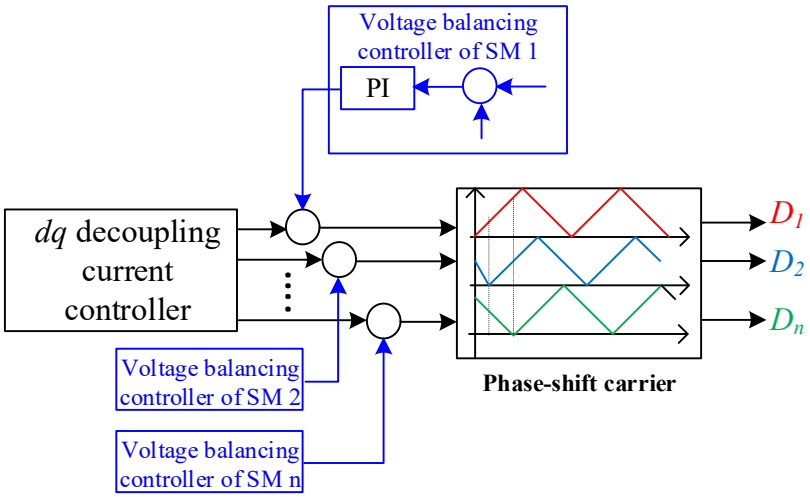


Figure 2.10. PWM based voltage balancing control.

However, the PWM methods need a high switching frequency, and thus would lead to large power losses when the number of SMs increases. Hence, this method is not suitable for the high voltage applications where a great number of SMs are required. To address this challenge, the nearest level modulation was presented, and the sorting method was used to balance the

SMs' voltages [48]−[50]. For nearest level modulation, the arm voltage reference is divided by the value of the capacitor voltage to calculate the desired voltage level. The voltage level decides how many SMs will be inserted as each SM generates one voltage level. As the calculated number may not be an integer, a rounding function is used to find the closest integer of the inserted number. A sorting method is then used to balance the capacitors' voltages. The principle of the sorting method is [48]:

- When the arm current charges the capacitors, the submodules with the lowest storage capacitor voltages will be switched on.
- When the arm current discharges the capacitors, the submodules with the highest storage capacitor voltages will be switched on.

The overall process is shown in Figure 2.11.

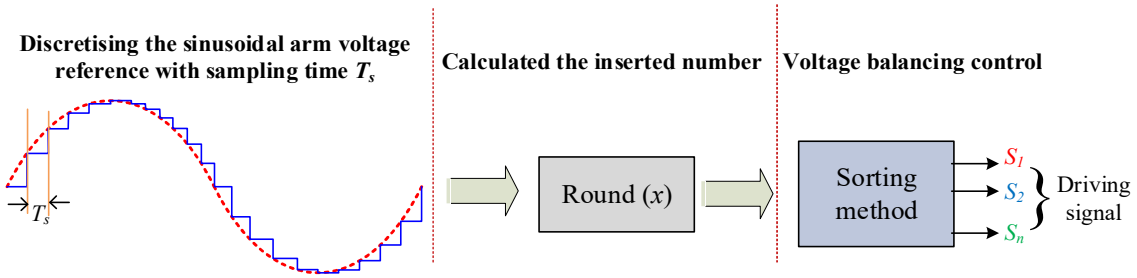


Figure 2.11. Nearest level modulation with sorting method for voltage balancing.

For the modular configuration based DC/DC converters, a three-loop control strategy using a dedicated input-voltage controller for ISOP connection was proposed in [51]. A simpler method which uses common-duty-ratio control was proposed in [52], where the duty ratio to all the converter modules connected in ISOP configuration is identical (see Figure 2.12). Thus, only a single closed control loop is enough. The voltage balance can be automatically achieved due to the common-duty-ratio control. However, the mismatched parameters among SMs may have adverse impact on the balancing performance. The voltage balancing performance is analysed by using both a small-signal averaged model and a steady-state DC model of the ISOP converter. It is hown that the sharing of input voltage is related to the mismatches in various parameters such as the leakage inductance, input capacitors and turn ratio of transformer.

In order to improve the voltage balancing performance, the input voltage sharing (IVS) and output current sharing (OCS) loops are added [31], [53]. For the IVS method, the voltage sharing loop is embedded in each SM with a common output voltage controller, as shown in

Figure 2.13. Although the modularization has been greatly achieved, an external controller is still needed to coordinate the sharing control functions of the SMs, thus greatly compromising the flexibility of the system. In [15], a fully modularized method was proposed to make each SM able to operate in stand-alone mode. To achieve this, each SM has an own output voltage regulating loop. As there are mismatches in the voltage references and output voltage sampling coefficients of the modules, signal diodes should be used to ensure that only one output voltage regulating loop is active and regulates all the outputs of all modules. The proposed architecture is shown in Figure 2.14.

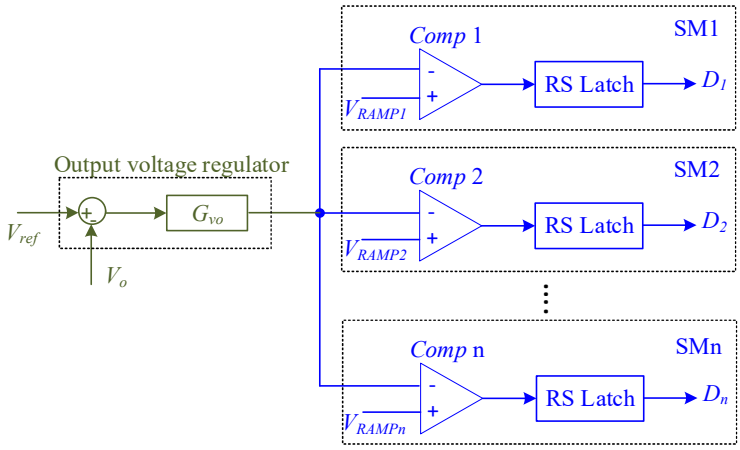


Figure 2.12. Common-duty control for DC/DC converters [52].

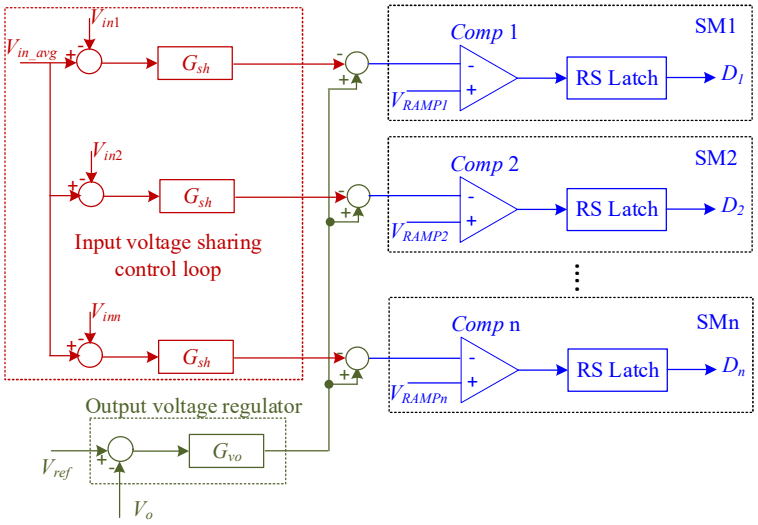


Figure 2.13. Input voltage sharing control for DC/DC converters [31].

The other sharing method named as the OCS is shown in Figure 2.15 [53]. With the control strategy, the duty cycles of modules with larger output currents will increase and the duty cycles of modules with smaller output currents will decrease, and finally to achieve OCS. As the output currents are equal, the input voltage balance is also achieved. Hence, altough the control

object is different with the IVS control, the final control effect of the two methods is the same. Another control alternative is the cross-feedback OCS-controlled method [54]. In this method, a voltage outer loop provides a common reference for the current loops of all SMs. The current feedback for a SM is not its own but the sum of currents of all other remaining SMs. However, with increase of the number of SMs, the control strategy will become complex due to the large amount of signal cables.

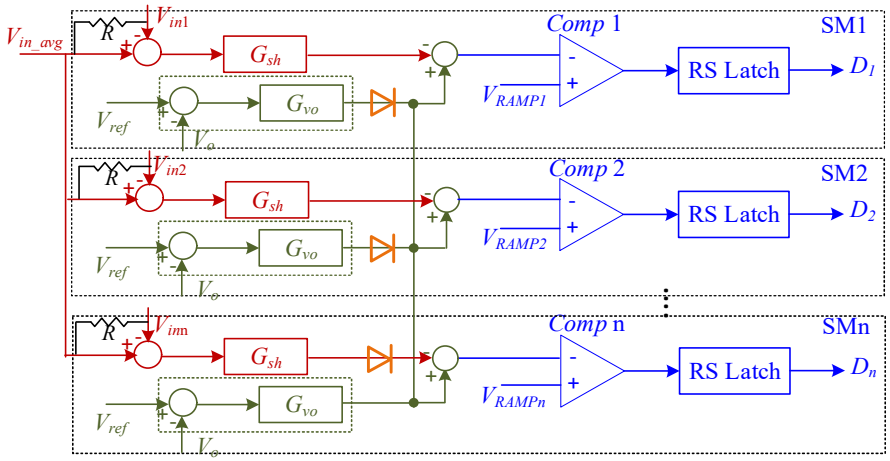


Figure 2.14. Fully modularized control method for DC/DC converters [15].

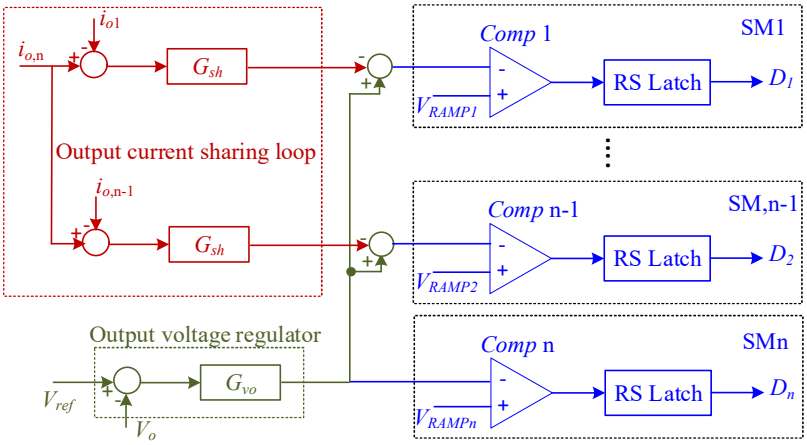


Figure 2.15. Current sharing control for DC/DC converters [53].

A common feature of the aforementioned methods is that a central controller is required to send the input voltage reference to the SMs. The system may malfunction upon the loss of the communication between the central controller and the SM controllers. To this end, the decentralized voltage balancing control methods were presented [55], [56]. The decentralized scheme is shown in Figure 2.16, where a $V_o - V_{in}$ inverse droop control is employed. Due to the droop characteristic, the operating point will move back to the original point during a perturbation in DC voltage. It can be seen that the larger the droop gain, the better the input

voltage sharing accuracy. However, a larger droop gain leads to the deterioration of the system output voltage regulation performance. This trade-off between the input voltage sharing and the output voltage regulation performance was addressed in [57] by using another voltage shifting loop.

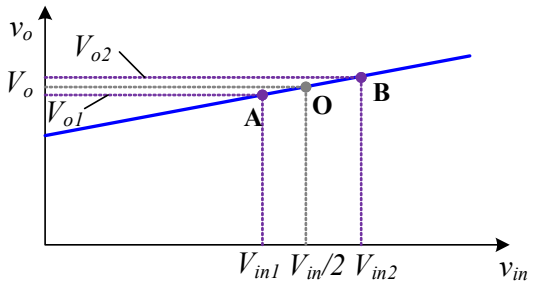
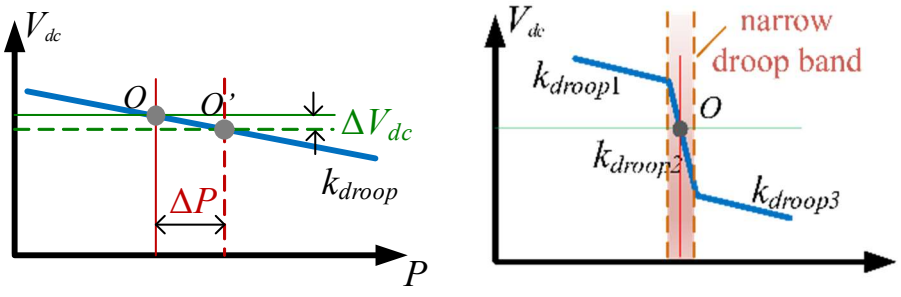


Figure 2.16. Decentalized voltage sharing control.

2.2.2 Decentralized Control with Multiple Droop Characteristics

The decentralized control strategies are promising to be widely used in the MVDC systems [58]-[60]. The power feeding and voltage support can be automatically shared by power converters thus improving the voltage and power regulation, and meanwhile, decreasing the risk of system failures compared with the centralized control. Traditional decentralized control such as the power versus voltage droop method usually adopts a single droop slope [61]. Such control typically has a shallow droop (e.g. 5%) and thus acts like a voltage source more than a current source. In this case, the accuracy of power control is significantly impacted by any DC voltage disturbance. A slight DC voltage offset ΔV_{dc} (e.g. caused by measurement errors of sensors) will cause a huge mismatch of power flow ΔP as shown in Figure 2.17(a). Further increasing the slope of the droop will mitigate the inaccuracy but could lead to voltage instability in dynamic events (e.g. change of loads), which actually imposes greater threats to the MVDC systems.



(a) **(b)**

Figure 2.17. Control characteristics in power versus voltage ($P-V_{dc}$) droop. (a) Conventional droop cure with a single droop slope. (b) Improved droop curve with multiple droop slopes.

A popular solution to overcome this problem is to adopt multiple droop characteristics with one converter thus to precisely control the power while well stabilize the system in dynamic events. The control with multiple droop characteristics is shown in Figure 2.17(b). It features a narrow droop range (with a steep droop k_{droop}) around the desired operating point [62]. Hence, the characteristic of the droop curve within this range is close to a current source. The power flow accuracy at dynamics is improved due to the less sensitivity of the high droop slope k_{droop2} to the voltage disturbance. If there is a large voltage or power change which exceeds the narrow band, the droop slope is changed to a smaller one (k_{droo} and k_{droop3}), in order to support DC voltage.

Although the advantages of the multiple-slope based decentralized control have been reported in [63]-[65], the concerns of consequent adverse effects also arise. One of the adverse effects is the risk of multiple crossovers caused by the interactions between different converter stations and has been reported in limited resources such as [66], [69]. This may result in the shift of DC voltage and unintended power imbalances at converter stations. In [66], the multiple crossovers caused by the control characteristics was first discovered in a high-voltage direct-current (HVDC) link, where one converter station operated with constant power control and the other station with current versus voltage droop ($I_{dc}- V_{dc}$) control. In [69], the multiple crossovers resulted from another typical control strategy— constant current and power versus voltage droop ($P- V_{dc}$) control was studied. This type of control strategy has been widely used in the DC distribution networks where parts of converter stations are with droop control to regulate the DC voltage and the converters connected to renewable energies are with current control [70], [71]. The effects of multiple crossovers have been experimentally assessed through a MMC based HVDC link. Also, a guideline on how to select a suitable droop slope to avoid the multiple crossovers were given. However, the mechanism of the power and voltage drifts caused by the multiple crossovers remains unexplored. On the other hand, although multiple crossovers can be avoided by reducing the droop slope following the guideline in [69], this is in sacrifice of the narrow droop range — the power control accuracy at dynamics is decreased when the system is subjected to a perturbation in either DC voltage or current.

When the cascaded 3L-NPC converters adopt the multiple-slope based droop control, DC volatge balancing control should be properly designed in consideration together with the

multiple crossovers and power control accuracy. In Figure 2.17, the smaller the slope is, the better the DC voltage balancing would be, but the power control accuracy will be affected.

Therefore, to achieve better suppressions of DC voltage imbalance and multiple crossovers, the droop gain should be decreased. However, this is contradictory to the power control accuracy. Thus, how to find a control solution that takes into account these three factors is a challenge.

2.2.3 Active Thermal Control

Apart from high efficiency, high power quality, and fault-ride-through capabilities offered by the power electronic converters, reliability is an important performance criterion affecting their design and control [72], [73]. Around 55% of the failures in power electronic converters are caused by temperature-related issues [18]. High mean temperatures and temperature fluctuations can cause fatigue and damage in the packaging of the semiconductor materials—leading to bond wire lift-off and solder crack.

Power converters are normally connected in parallel or in series to achieve high current or high voltage ratings. Even when all submodules (SMs) within a converter may operate at even loading or under voltage sharing control, the thermal stress may be different for each SM. This may be due to a mismatch in component parameters and different individual cooling system conditions [74]. Given that the lifetime of converter systems is determined by the first failed SM, temperature imbalance may lead to premature damage of certain SMs—decreasing the overall lifetime of the system [75].

Active thermal control addresses the reliability issues just discussed [76]. An often-adopted approach is to modify the switching modulation of a single SM by using discontinuous pulse-width modulation (D-PWM) [76] and zero-sequence current injection [77]. By altering the flow path of the current, the semiconductor device that exhibits the highest temperature is prevented from conducting and being switched on. As a result, the burden of thermal stress is distributed to other switching components in the same SM. However, by incorporating D-PWM, the harmonic performance of the output current/voltage may be affected [77].

For the thermally oriented converter control, the switching frequency and controller limits are modified to avoid exceeding the maximum temperature [78], [79]. The schemetic is shown in Figure 2.18. As can be seen, both the mean teperature and the temperature cycling can be taken as the control targets. The junction temerature was first estimated, and then two PI regulators were used to reduce the switching frequency and current to prevent the device from overtemperature (see Figure 2.18). Another control method is the minimum DC voltage control [80]. On the basis of meeting the requirements of the grid codes, the DC voltage is ajusted to its minimum value to reduce the thermal stresses. Compared with the switching modulation based methods, the disadvantage of the converter control is that the thermal stresses in specific devices can not be dedicatedly controlled. To address this, [81] proposed a thermal based finite control set model predictive control (MPC) method. A cost function, which includes the current control error, junction temperature of specific devices and power losses, were employed. The suitable switching vectors which minimise the cost function were selected. Sets against the advantage are the complex computation and harmonics due a varying switching frequency.

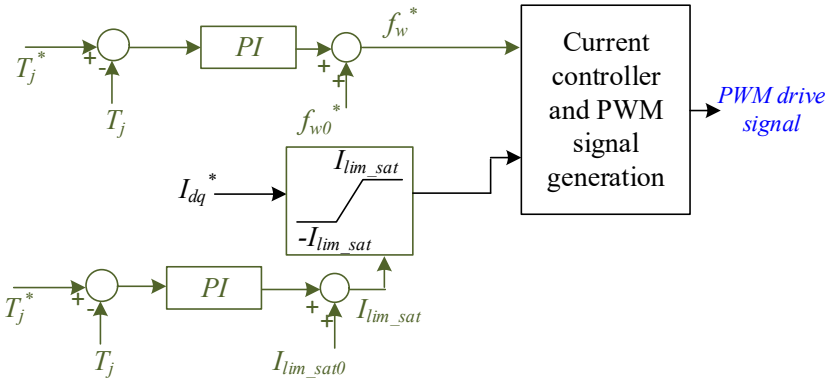


Figure 2.18. Thermal control by regulating the switching frequency and sturation of current controller [78]**.**

Another method, named power routing, redistributes the power among different SMs according to their thermal conditions [82]. The SM with the highest temperature is allocated with the least power and vice versa, enabling thermal stress to be shared equally among SMs. The SM with the highest temperature is allocated the least power and vice versa, enabling thermal stress to be shared equally. The junction temperature a device is estimated based on its power losses and thermal impedance [83]. The conduction loss is mainly related to the current and voltage drop across the device, whereas the switching loss is related to the switching frequency and DC voltage [84]. This concept has been adopted in the cascaded H-bridge converter-based smart transformers and interleaved DC-DC converters [82], [85]. The power references sent to

the input-parallel-output parallel converters are proportional to the SM individual accumulated damage which represents the life consumption. Firstly, the accumulated damage is estimated through rainflow counting and Miner's rule. The accumulated damage is updated after a fixed time period. Then, the virtual resistor, which is the function of the accumulated damage, is used to distribute the power references to the SM controller. The schematic is shown in Figure 2.19. In [86], the juntion temperature of the SM was stabilized by regulating its reactive power (see Figure 2.20). The injection of the reactive power modifies the magnitudes and phase angles of both the output voltage and current, thus changing the thermal conditions of specific power devices. For example, the temperature cycling of neutal-point clamped diodes is mitigated with underexcited reactive power injection, although the temperature of other power devices are slightly increased [86]. The reactive power is made circulating inside the parallel converters and not output to the grid.

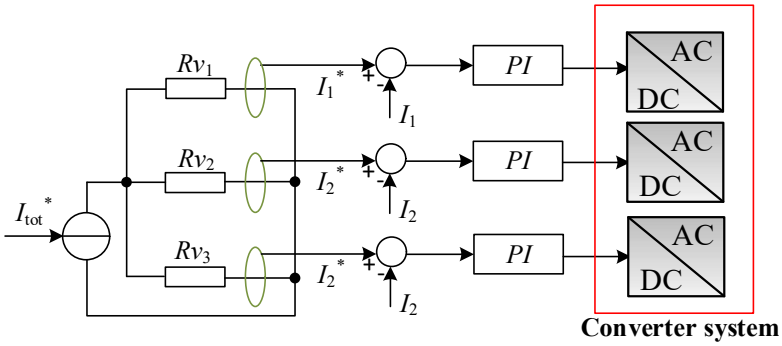


Figure 2.19. Power routing control stategy [85].

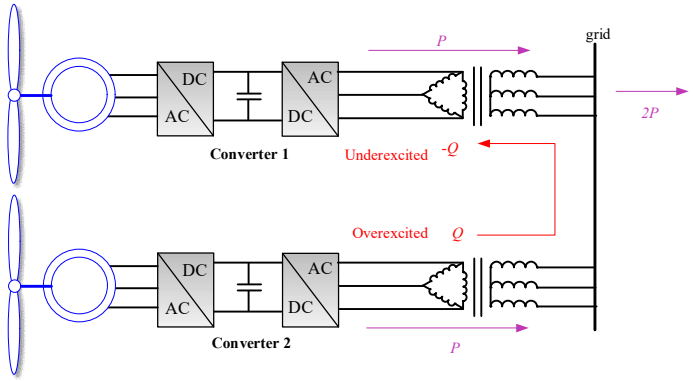


Figure 2.20. Thermal control by injecting circulating reactive power [86].

In [87], the discontinuous modulation combined with the power routing was proposed considering a more complex configuration in a smart transformer – each buliding block comprises both cascaded H-bridge (CHB) and DAB converters, as shown in Figure 2.21. The power routing can only address the first case in Figure 2.21(a), where the weak CHB cell and

DAB cell are in the same building block, but cannot address the second case in Figure 2.21(b), where the cells with weak reliability (highlighted in yellow) are not in the same block. To this end, the D-PWM is adopted. The weak CHB cell is thermally compensated by adjusting the clamped phase angle of the D-PWM to reducing the switching losses, while the DAB cell is compensated by reducing the power.

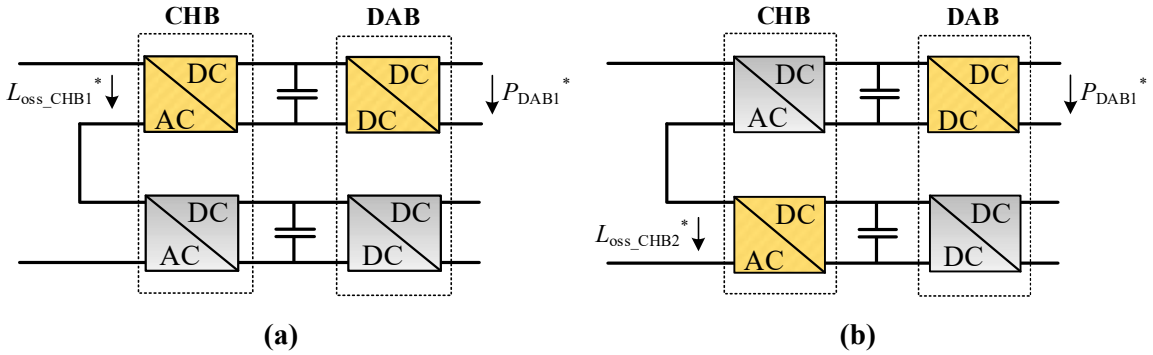


Figure 2.21. Thermal stresses in cascaded CHB-DAB converters [87].

For the MVDC converters, thermal imbalance among SMs could be more than 20% in MMCs [72]. Thermal balancing control strategies have been presented in [74], [88]. However, this topic regarding the cascaded 3L-NPC converters has not been investigated so far and only DC voltage and power balancing control have been presented in recent studies [89], [90]. For MMCs, the sorting method presented in [74] optimizes thermal balancing by considering a weighting trade-off between the capacitor voltage and thermal balancing control loops. By using this thermal control method, the lifetime of the first failed power semiconductor device may be increased by 50%. In [88], a PI controller is used to balance the junction temperature of SMs in an MMC. This control loop is superposed on the capacitor voltage controller to adjust the DC voltage of the SMs and, hence, adjusting the power losses. However, the conduction losses in MMCs are dictated by the arm current magnitude and are nearly equal in all SMs, so only the switching losses can be adjusted by regulating the DC voltage. Conversely, as each SM in a cascaded 3L-NPC converter is an individual converter, both conduction and switching losses may be adjusted by controlling the active/reactive power and DC voltage of each SM. On the other hand, unlike the MMCs where the DC voltage of the SMs can be reduced to zero, there is a minimum limit for the DC voltage of each 3L-NPC SM as the DC/AC converter is a boost-type circuit from the AC side to DC side.

Apart from the cascaded converters, in microgrids where converters are parallel-connected, the temperature dependent droop control strategies were proposed in [91], [92] to achieve equal

thermal distributions. In [91], a lifetime oriented droop controller was developed based on the relationship between the temperature and power relationship. In [92], the droop coefficient of the converter was adjusted through online monitoring of the line frequency thermal stresses. Thus the reliability is enhanced compared with the conventional decentralized power sharing strategies.

2.3 Summary

In this chapter, the topologies and control of modular DC/DC and DC/AC converters in MVDC applications are reviewed. For DC/DC converters, the input-series topologies based on DAB and LLC converters are popular choices due to their high modularity and mature control technologies. For the DC/AC converters, MMCs dominated in the HVDC and MVDC transmissions. In addition, a novel cascaded 3L-NPC converter is also a promising candidate for the MVDC application due to its lower cost compared to MMCs.

Although the control methods for the modular DC/DC converters and MMCs have been well developed, the suitable control methods for the cascaded 3L-NPC converters are yet to be explored. Therefore, a hierarchical control schematic suitable for this type of converter are presented in this study (see Chapter 3), where a communication-based control structure is developed to control the SMs through a high-level main controller.
A common challenge faced by MVDC converters may be stability and reliability issues caused by cascaded topologies in which multiple SMs are connected in series. The stability issue arises due to the imbalance power and voltage sharing in each SM. Different control methods to address the power and voltage imbalance are reviewed. This type of approach is moving towards high modularity (not relying on communication) through decentralized control. However, the controller design is based on the converter topology. Directly transferring the methods to the cascaded 3L-NPC converters should be done with care. In this study, the voltage and power sharing control are particularly designed for the cascaded 3L-NPC converters, for being with and without communications (see Chapter 4).

The performance of power and voltage balancing control is coupled with other factors (e.g. power flow accuracy and multiple crossovers between different converter stations) when the system is extended to a multi-terminal system. Traditional balancing control methods only focused on SMs in a single cascaded converter while the coupling of other factors in converter

systems were not considered. In this study, the voltage balancing control is considered together with the multiple crossovers and power control accuracy. An improved control method is presented to make a good trade-off between the voltage balancing, multiple crossovers and power control accuracy (see Chapter 5).

The active thermal control can mitigate the thermal stresses of semiconductors, thus extending the converter lifetime. The PWM modulation and current controller can be optimized to mitigate the conduction and switching losses. Thanks to the cascaded topology, the power routing concept was presented, where the load of an over-heated SM is redistributed to other SMs to achieve equal thermal sharing. As a consequence, the overall lifetime of the converter system is extended. The previous control methods are always topology-dependent and most thermal control methods were performed by only adjusting the active power. In this study, the suitable thermal sharing control methods for the cascaded 3L-NPC converters are presented, the thermal stresses are equally shared by concurrently adjusting the active and reactive power.

Chapter 3

Laboratory Demonstration of Cascaded 3L-NPC Converters

This chapter presents the hierarchical control methods and hardware design for the cascaded 3L-NPC converters. The laboratory demonstration is performed through a MVDC testbed down scaled from the ANGLE-DC project.

3.1 Introduction

The control and operation of cascaded 3L-NPC converters in MVDC applications is still an under-researched topic, which has only been presented in selected references, and often through desktop simulation exercises [89], [93]. Comprehensive studies dedicated to system control and operational issues remain to be assessed and experimentally validated.

This chapter demonstrates the operation of a cascaded 3L-NPC converter-based MVDC link fitted with suitable control schemes. System operation is verified, step-by-step, following a hierarchical approach going from switching level to application level. A 30-kW laboratory scaled MVDC testbed is used to experimentally validate simulation results obtained using MATLAB/Simulink. This testbed has been down-scaled from the ANGLE-DC project, with similar per unit values as those employed in the real system. Using the experimental testbed, a number of simulation scenarios are experimentally verified including the start-up/shut-down procedure of the converter system, steady-state and dynamic performance of DC voltage and power control loops, and transitions between different control modes.

3.2 Hierarchical Control Design of the System

The switching, converter and application control layers of the cascaded 3L-NPC converters are presented in this section. The switching-level control layer includes the Carrier Disposition-based Sinusoidal PWM (CD-SPWM) method. A closed-loop current controller is implemented in the converter-level control layer. For the application-level control, different control modes are available and can be selectively used according to the practical requirements of the system. The complete control schematic is shown in Figure 3.1.

3.2.1 Switching-level Control

The most used modulation methods are the Sinusoidal PWM (SPWM) and Space-Vector PWM (SVPWM) methods. Although SVPWM provides a better harmonic performance and a higher DC voltage utilization, CD-SPWM is adopted due to its ease of implementation. In orange block of Figure 3.1, it can be observed that the phase voltage v_{xo} switches between $\frac{U_{dc}}{2}$ and 0 when the modulation wave is positive, and between 0 and $-\frac{U_{dc}}{2}$ when modulation wave is negative. It should be noted that a neutral-point voltage balancing controller is embedded within each SM as a 3L-NPC converter exhibits neutral-point voltage imbalance. To address

this problem, a common-mode signal is calculated by a PI controller, and this is added on the three-phase sinusoidal modulation signals, as seen in the red rectangle in Figure 3.1.

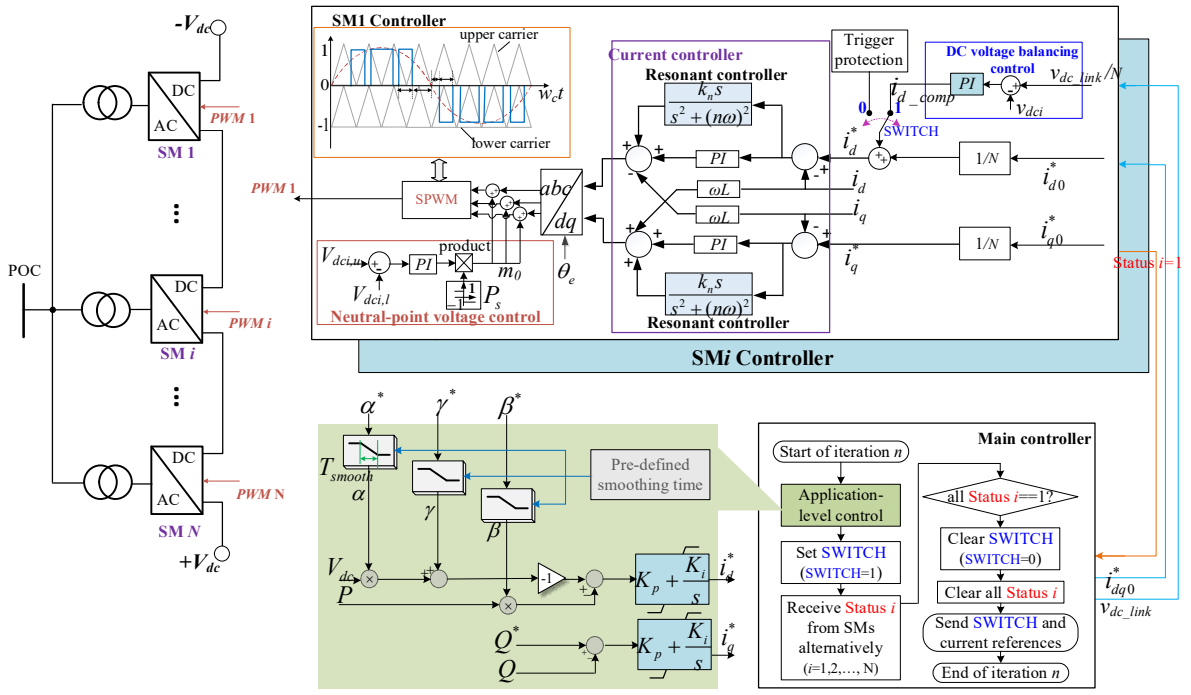


Figure 3.1. Control schematic of the cascaded 3L-NPC converters.

3.2.2 Converter-level Control

The current controller operates in a *d*-*q* synchronous reference frame following a coordinates transformation. This enables the active and reactive power to be decoupled and thus controlled independently. To this end, PI controllers are used. The parameters of the PI regulators can be designed based on a second-order transfer function for a linear system. The decoupling terms $-\omega L i_q$ and $\omega L i_d$ can be added to decouple the current components at *d*-axis and *q*-axis. Voltage feedforward e_{dq} can be also used to improve the dynamic performance of the current controller.

The traditional current controller regulates positive-sequence current and works effectively if the voltage of connected grid is balanced. However, if the voltage imbalance occurs, both positive-sequence and negative-sequence currents will exist. Dual current controller regulating both positive-sequence and negative-sequence currents will be needed as shown in Figure 3.2 [94].

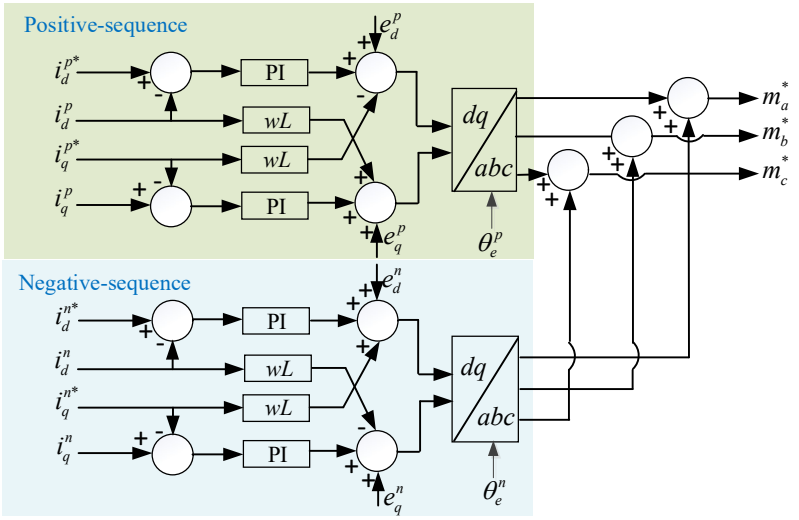


Figure 3.2. Dual current controller for positive and negative sequence control.

To control the negative-sequence current to zero, the current references are set as $\mathbf{i}_{\alpha\beta}^{n} = 0$. In this control scheme, the positive-sequence components $\mathbf{F}_{\alpha\beta}^{p} = \left[\mathbf{v}_{\alpha\beta}^{p} \quad \mathbf{i}_{\alpha\beta}^{p}\right]$ and the negative-sequence components $\mathbf{F}_{\alpha\beta}^{n} = \left[\mathbf{v}_{\alpha\beta}^{n} \quad \mathbf{i}_{\alpha\beta}^{n}\right]$ need to be extracted from $\mathbf{F}_{\alpha\beta} = [\mathbf{v}_{\alpha\beta} \quad \mathbf{i}_{\alpha\beta}]$. $\mathbf{F}_{\alpha\beta}^{p}$ and $\mathbf{F}_{\alpha\beta}^{n}$ can be obtained by misplaced subtraction as

$$\mathbf{F}_{\alpha\beta}^{p}(t) = \frac{1}{2}\left[\mathbf{F}_{\alpha\beta}(t) + j\mathbf{F}_{\alpha\beta}(t - T/4)\right]$$

$$\mathbf{F}_{\alpha\beta}^{n}(t) = \frac{1}{2}\left[\mathbf{F}_{\alpha\beta}(t) - j\mathbf{F}_{\alpha\beta}(t - T/4)\right] \tag{3-1}$$

Thus, the phase angles θ_e^{p} and θ_e^{n} in Figure 3.2 can be obtained by locking the phases of the $\mathbf{v}_{\alpha\beta}^{\mathrm{p}}$ and $\mathbf{v}_{\alpha\beta}^{\mathrm{n}}$ separately.

As the structure of the dual current controller is complex, a resonant controller with a transfer function of $ks/(s^2 + (2\omega)^2)$ can be superposed on the PI controller, since the negative-sequence components present second-order harmonics at the *d-q* frame (the negative-sequence h^{th} harmonics at stationary reference frame present $(h+1)^{th}$ harmonics at the synchronous rotating reference frame [67]). The gain parameter k is tuned through trial and error until the controller achieves desired dynamic response and steady performance. In addition, considering that the bandwidth of the current controller does not eliminate potential harmonics introduced by the non-linear characteristics of the converters or distortions in the grid voltage, including resonant controllers in parallel to each PI controller can also improve the harmonic performance (see the purple rectangle in Figure 3.1). For example, to mitigate the intrinsic 5$^{\text{th}}$

and 7^{th} harmonics of converters, a resonant controller with a transfer function $ks/(s^2 + (6\omega)^2)$ is added to the PI controller in the *d-q* frame.

3.2.3 Application-level Control

For MVDC operation, the control modes include constant DC voltage control (V_{dc}/Q), constant power control (P/Q) and droop control (V_{dc} -P/Q). The droop control is adopted to improve the regulation of the DC voltage and to guarantee system operation upon failures at the converter stations. A control structure combining the three control modes is employed [95], which is shown in Figure 3.1 (enclosed by the green rectangle). By setting suitable values to α, β and γ, control mode transitions can be achieved, as shown in Figure 3.3, where $k = \beta/\alpha$ is the slope of the droop curve and $\gamma = -\alpha V_{dc,0} - \beta P_0$, where $V_{dc,0}$ and P_0 are the normal operating points.

It should be noted that there is a risk of communication failure in the SMs of the MVDC system when the hierarchical control structure discussed in this section is adopted. If not properly addressed, communication failures may lead to instability. To this end, the algorithm shown at the bottom right of Figure 3.1 is implemented. The control modes are selected with the 'SWITCH' command. The SM controller is enabled when 'SWITCH = 1'. To achieve this, the flag 'Status i' is returned from the SM's controller to the main controller. If all 'Status i = 1', the communication is assumed as normal, and 'SWITCH' is set to 1 by the main controller. Otherwise, there is a communication failure in the SMs. In this case, 'SWITCH' will be set as zero to trigger the SM protection. The SMs that lose communication will automatically trigger their protection.

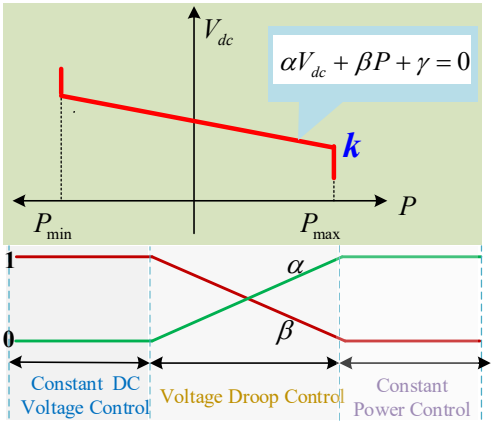


Figure 3.3. Control schematic of the cascaded 3L-NPC converters.

3.3 Configuration of the MVDC Testbed

3.3.1 Laboratory-scale Testbed with Cascaded 3L-NPC Converters

The operation of ANGLE-DC is demonstrated by a scaled-down MVDC testbed. The experimental platform is shown in Figure 3.4(a), which aimed to resemble the real practical configuration as much as possible. There are two converter cabinets, labelled Stations 1 and 2, which constitute the back-to-back converter system. The power of each cabinet is supplied by a power amplifier (PA-3*3000-AB/260/2G) which emulates the AC grid, shown in Figure 3.4(b). Figure 3.5 shows the internal structure of the cabinet as well as the hardware board within each SM. Figure 3.5(a) shows the twelve 3L-NPC cascaded SMs, a high-level main controller and the isolation transformers. The main controller is used to coordinate and monitor the operation of the SMs. Figure 3.5(b) shows the top layer components of a single SM, which includes three-phase IGBT power modules, SM controllers based on DSP 28335 and the power supply to the microcontroller. Other components such as the inductor, relay and cooling fans are under the bottom layer.

(a) **(b)**

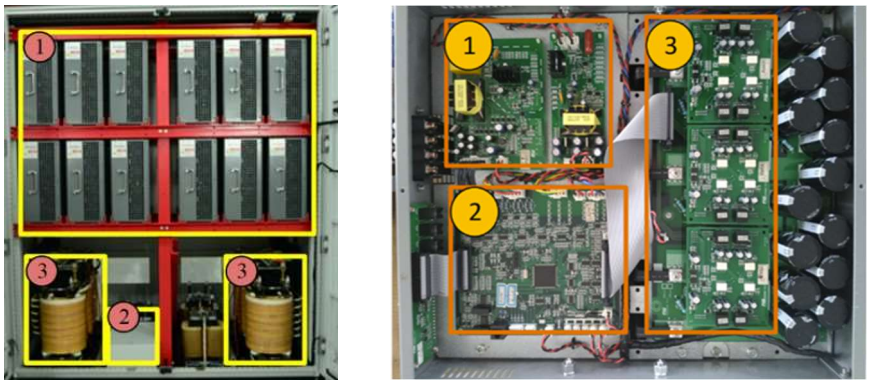
Figure 3.4. Laboratory scaled MVDC platform: (a) back-to-back cascaded 3L-NPC converter; (b) connection between the converter and a power amplifier.

The leakage inductance of the transformer in real system can provide filtering of the harmonics. Since the leakage inductance of the transformer for the testbed is significantly smaller than that of the real system, an additional L-type grid-connected inductor is used. The values of the L-filter and DC capacitors are calculated as:

$$L_{p.u.} = \frac{L_s {N_{Tr.}}^2/12}{L_{base}} = \frac{\omega_{base} L_s {N_{Tr.}}^2/12}{Z_{ac\_base}} = 0.22 \text{ p. u.} \tag{3-2}$$

$$C_{p.u.} = \frac{C_{dc}/12}{C_{base}} = \frac{C_{dc}/12}{\frac{1}{\omega_{base} Z_{dc\_base}}} = 5.5 \text{ p. u.} \tag{3-3}$$

where $Z_{ac\_base} = \frac{V_{AC\_base}^2}{S_{base}}$ ($S_{base} = S,\ V_{AC\_base} = V$), $\omega_{base} = \omega$, and N_{Tr} is the turns ratio of the isolation transformer.



(a) (b)

Figure 3.5. Internal structure of the MVDC station and each SM. (a) MVDC station: 1) twelve 3L-NPC SMs, 2) high-level main controller, and 3) isolation transformers. (b) Each SM: 1) power supply to the microcontroller, 2) DSP28335 controller board, and 3) three-phase IGBT power modules.

A parameter comparison between the experimental testbed and the real ANGLE-DC system is provided in Table 3.1. As illustrated, except for the DC capacitance, the selected parameters of the testbed in per unit values are similar to those of the real system.

TABLE 3.1. PARAMETER COMPARISON BETWEEN THE ANGLE-DC CONFIGURATION AND THE EXPERIMENTAL TESTBED [96].

Parameters	ANGLE-DC station	Per unit value	MVDC testbed
Power rating S	33 MVA (2.75 MVA*12)	1 p.u.	30 kVA (2.5 kVA*12)
AC voltage V (rms of $v_{1,2}$)	33 kV	1 p.u.	415 V
DC link voltage V_{DC}	±27 kV	1 p.u.	±540 V
Transformer rating	2×17 MVA (Y-33 kV/Δ-2.1 kV)	1 p.u.	2×15 kVA (Y-415 V/Δ-41.5 V)
Transformer impedance	0.2 p.u.	0.2 p.u.	—
Filter inductance (per VSC)	—	0.22 p.u.	0.5 mH
DC capacitance (per VSC)	2300 mF	5.32 p.u./ 5.5 p.u.	5400 mF
Switching frequency	750 Hz	—	10 kHz

3.3.2 Signal Measurement and Hardware Protection

Representative block diagrams summarising signal measurement and hardware protection are provided in Figure 3.6. The current and voltage of each SM are detected by the SM controller. Once the maximum value limit is reached, the SM protection is triggered. At the same time, the PWM driving signals are blocked immediately and the relay at the AC side is opened. As the sampling of the Analogue-to-Digital Converter (ADC) is not quick enough (the signal is sampled once per PWM period, which is 100 μs), an edge detection method is used. At the comparator, if the measured signal is greater than the reference voltage, the output voltage changes from low to high. This method can detect the fault signal within 10 μs, thereby improving the speed of response of the protection scheme.

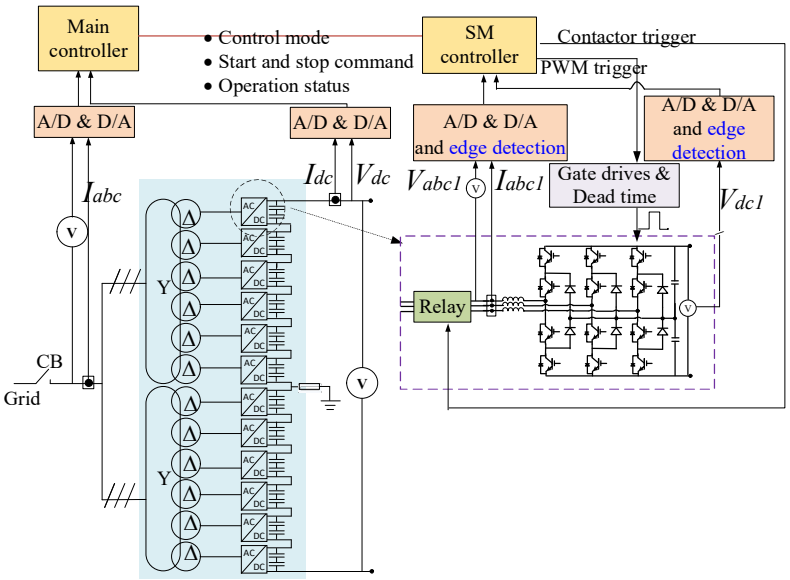


Figure 3.6. Signal measurement and hardware protection diagram.

3.3.3 Communication

The communication diagram for the MVDC experimental testbed is shown in Figure 3.7. The main controller dispatches control commands and sends suitable references to each SM. Data communication is achieved using an RS485 cable and the Modbus protocol. Also, a digital signal is sent to the SMs for PWM carrier synchronisation. The main controller additionally communicates with a PC in real time to monitor the status of the system operation. To facilitate implementation, the control system (including the ADC sampling, phase-locked loop, Proportional-Integral (PI) controller and protection) was built in MATLAB/Simulink. Then, executable Code Composer Studio (CCS) codes were translated from this MATLAB/Simulink model and downloaded to the DSP 28335 based microcontrollers.

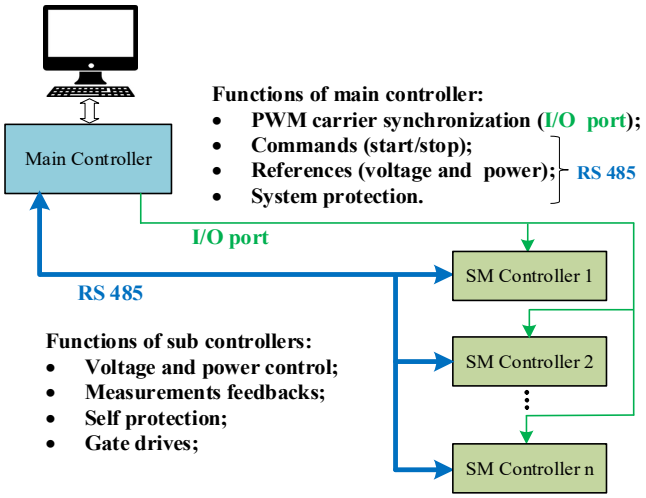


Figure 3.7. Communication diagram.

3.4 Simulation and Experimental Validation

3.4.1 Simulation Results

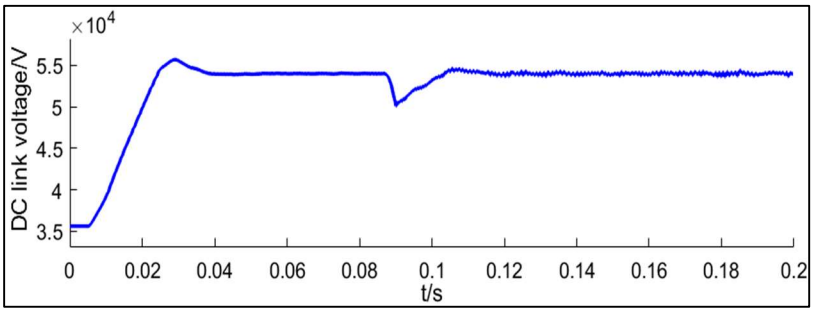
The simulation results are shown in Figure 3.8 to Figure 3.11. The references of DC voltage active and reactive power are set as the rated value of the real ANGLE-DC project. Figure 3.8 shows the results of the step change of active power. The DC voltage is first increased to 5400 V after 0.03 s (see Figure 3.8(a)). At time 0.1 s, the reference of active power is changed from zero to 30 MW (i.e., 1 p.u.). The total current at the primary side of the transformer is shown in Figure 3.8(b). Figure 3.8(c) and Figure 3.8(d) show the individual AC current and DC voltage of each SM. It can be seen that the power and DC voltage of SMs can be shared equally.

Figure 3.9 shows the condition when power factor is set as zero (i.e., the system is operated with only reactive power). It is seen that the system can work well under reactive power control mode.

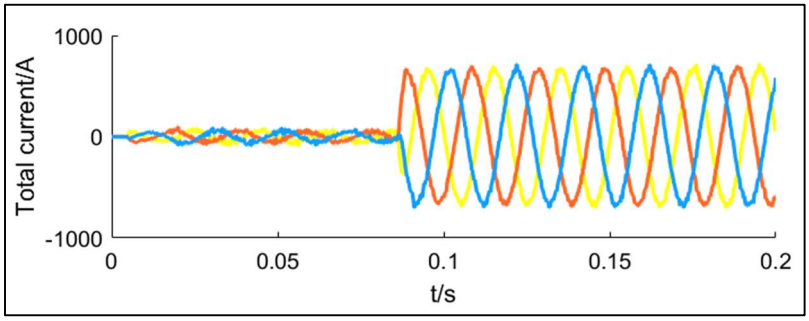
Figure 3.10 shows the results under unbalanced grid voltage. A 0.1 p.u. negative-sequence component is added in the grid voltage (see Figure 3.11). To control the current as balanced sinusoidal waveform, the dual current controller in Figure 3.2 is used. As seen in Figure 3.10(b), the output current has been balanced. Due to the interactions between the positive-sequence current and the negative grid voltage, there is a slight 2^{nd} order ripple in the DC voltage (see Figure 3.10(c)).

Figure 3.11 shows the results when droop control is adopted in the two-terminal converter stations. At time 0 s to 0.07 s, the system is operated at the desired operating points. At 0.07 s, one converter station is blocked due to a contingency. The DC voltage is increased to another

steady-state point according to the droop curve. Thus, the droop control can ensure the regulation of DC voltage when a converter station encounters fault condition.



(a)



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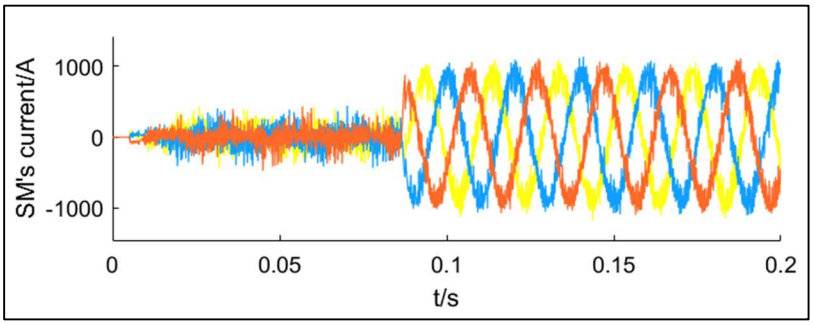
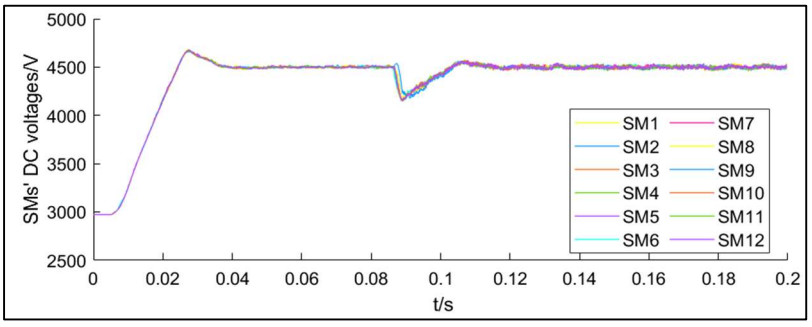
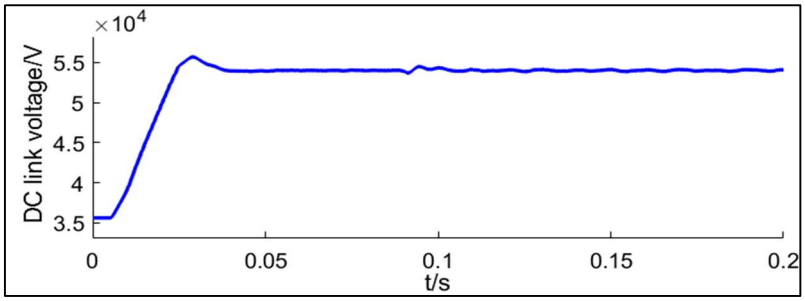


(c)

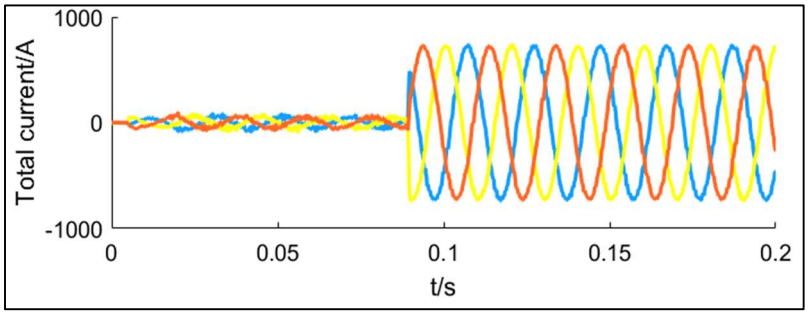


(d)

Figure 3.8. Step reference change of the active power under unit power factor: (a) DC link voltage; (b) Total AC current; (c) Current of SM 1; (d) SMs' DC voltages.



(a)



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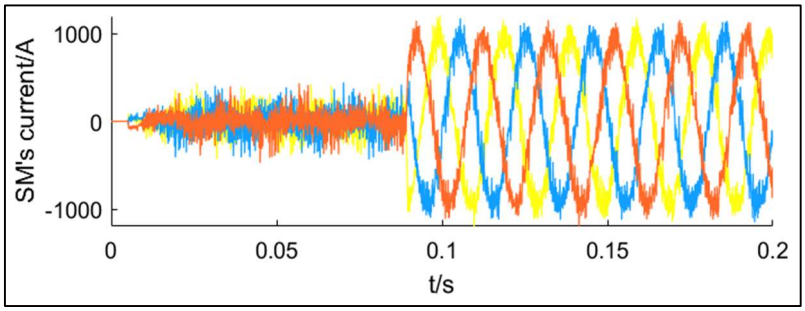
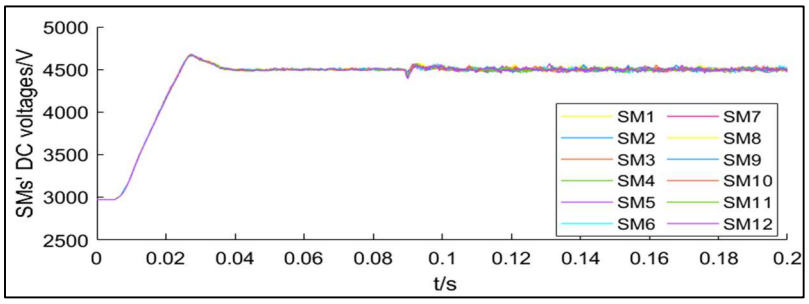


(c)



(d)

Figure 3.9. Step reference change of the reactive power under zero power factor: (a) DC link voltage; (b) Total AC current; (c) Current of SM 1; (d) SMs' DC voltages.

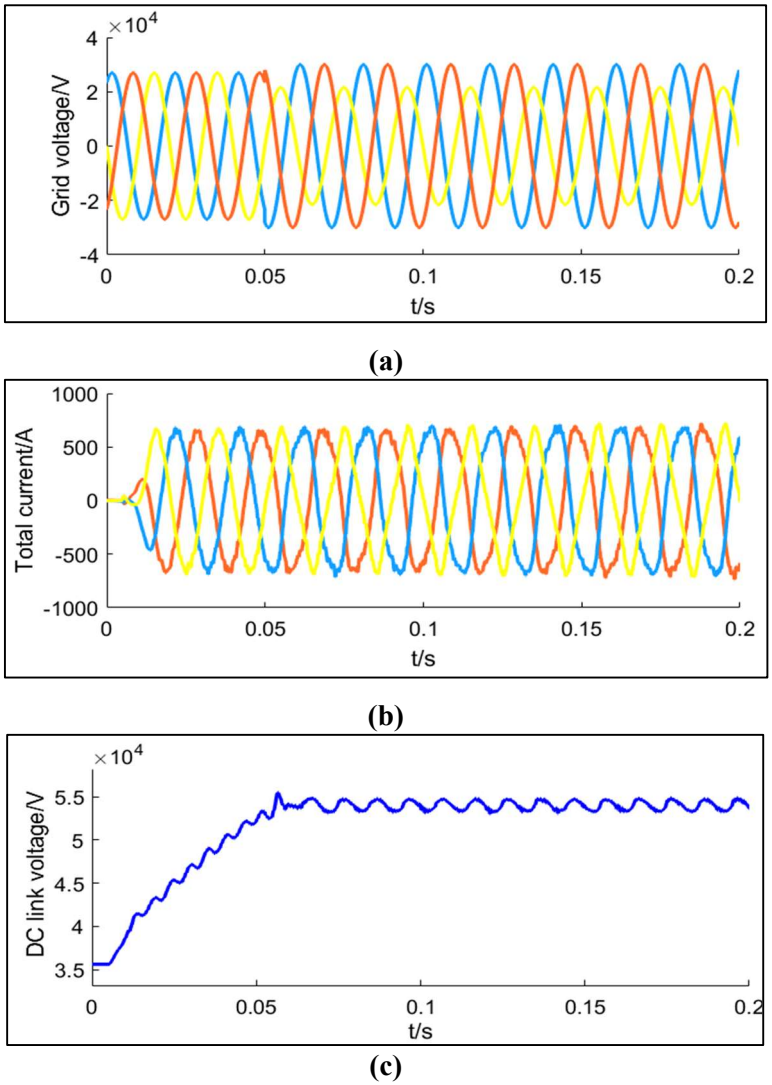
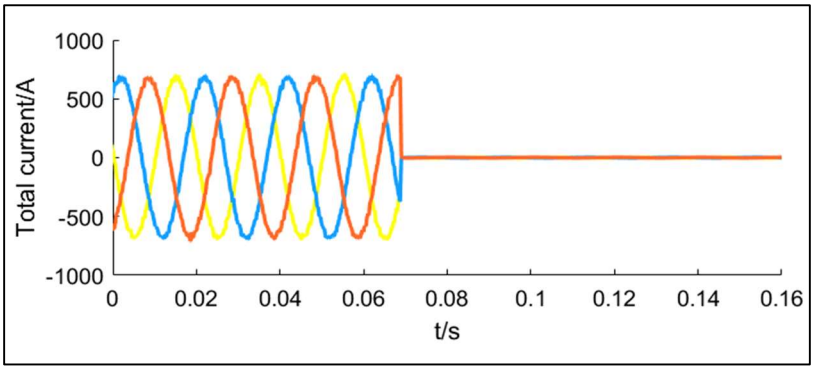


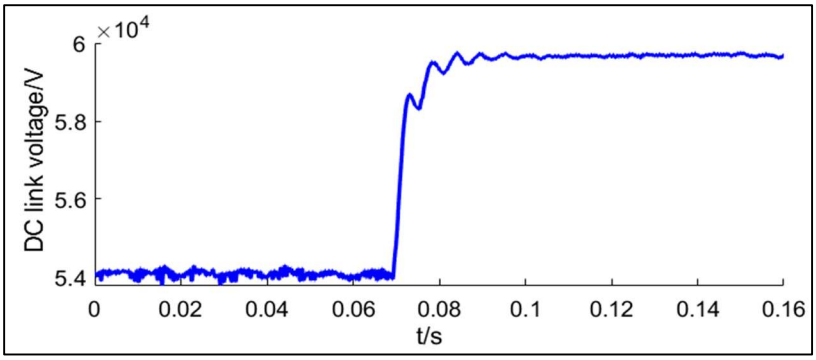
Figure 3.10. Performance under unbalanced grid voltage with 20% negative-sequence voltage. (a) Grid voltage; (b) Total AC current; (c) DC link voltage.

3.4.2 Experimental Results

The MATLAB/Simulink simulation model of the cascaded 3L-NPC converter system presented in the previous sections was experimentally validated using the MVDC testbed. For the experimental tests, as the power provided by the power amplifier was limited to 9 kVA, eight SMs were cascaded to build a 720 V DC link voltage (±360 V) instead of twelve (see Table 3.1). Four SMs were connected to the upper transformer (Tr.i1) and the other four to the lower transformer (Tr.i2), with a grounding resistor at the midpoint of the SMs. The controller parameters in per-unit values for both the simulation model and the experimental testbed are given in Table 3.2. Even when a reduced number of SMs was used, the control methods can still be validated using the experimental testbed.



(a)



(b)

Figure 3.11. Droop control under fault conditions. (a) Total AC current; (b) DC link voltage.

TABLE 3.2. PER UNIT VALUES OF CONTROL PARAMETERS.

Proportional gain of the PI-based d-axis current controller (k_{pid})	4.29	Proportional gain of the PI-based neutral-point voltage controller ($k_{p,NP}$)	1
Integral gain of the PI-based d-axis current controller (k_{iid})	10	Integral gain of the PI-based neutral-point voltage controller ($k_{i,NP}$)	0.5
Proportional gain of the PI-based q-axis current controller (k_{piq})	4.29	Proportional gain of the PI-based DC voltage balancing controller (k_{pudc})	6
Integral gain of the PI-based q-axis current controller (k_{iiq})	10	Integral gain of the PI-based DC voltage balancing controller (k_{iudc})	120

The energization process of the hardware is shown in Figure 3.12. Firstly, the relay of the control circuit is closed, and the DC capacitance used for supplying the power of control circuit is charged to 300 V. Then the 300 V is divided into 5 V, 8V and 15V for different uses such as power supplies for DSP board and gate driver. After the energization process of the control circuit is finished, the main AC circuit breaker is closed so that the converters are connected to

the AC grid. DC link capacitance is then charged through the anti-parallel diodes of the three-phase converter. When DC link capacitance is fully charged, the controller in the converter allows to be enabled.

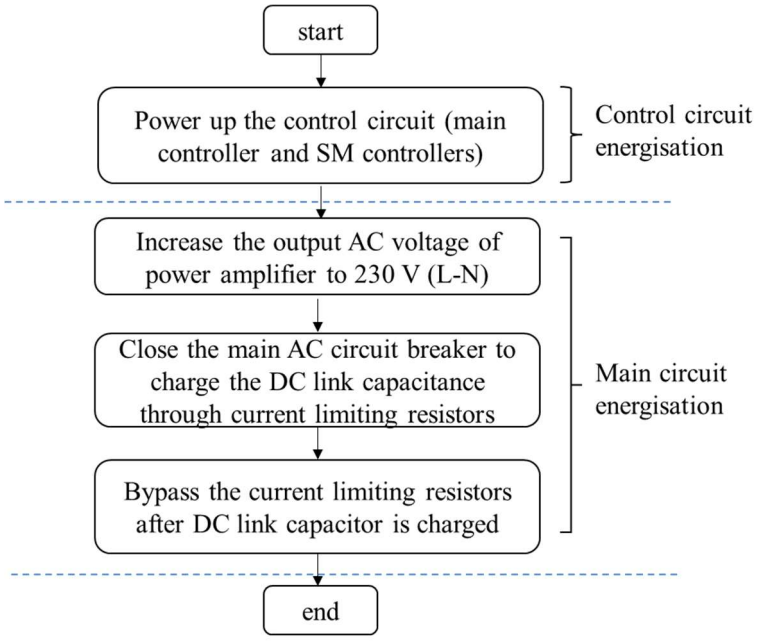


Figure 3.12. Energisation process of the equipment.

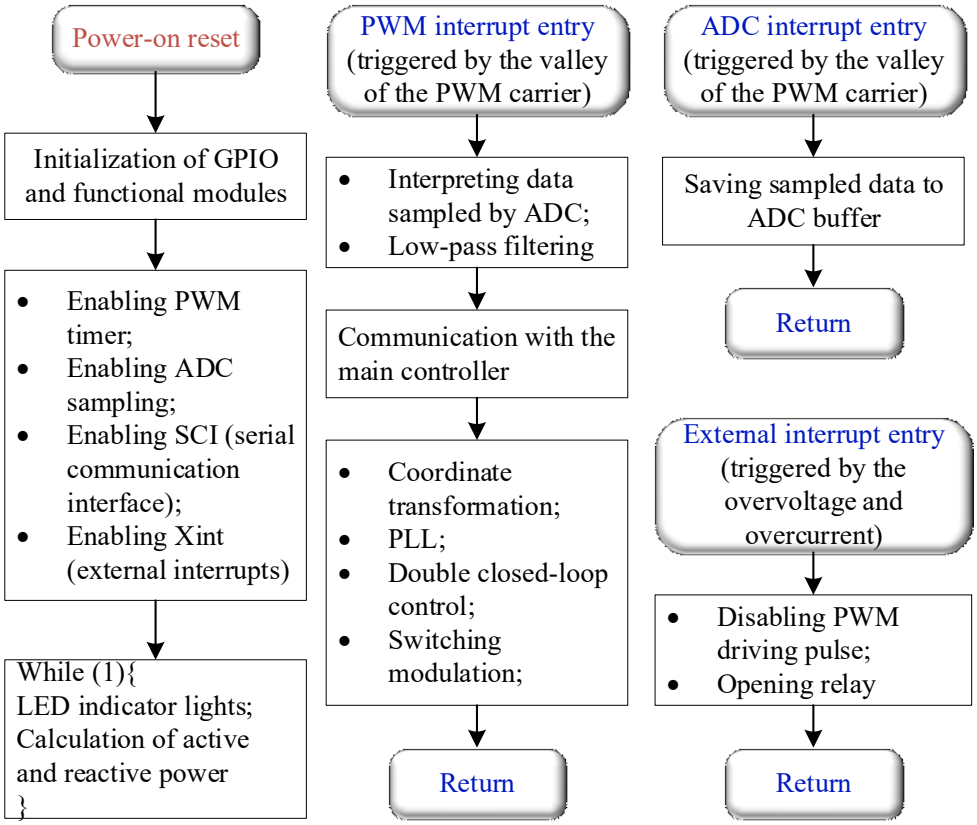
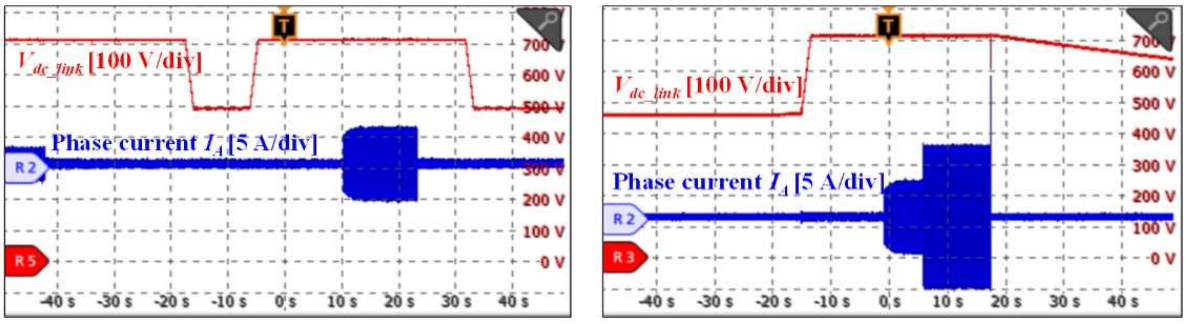


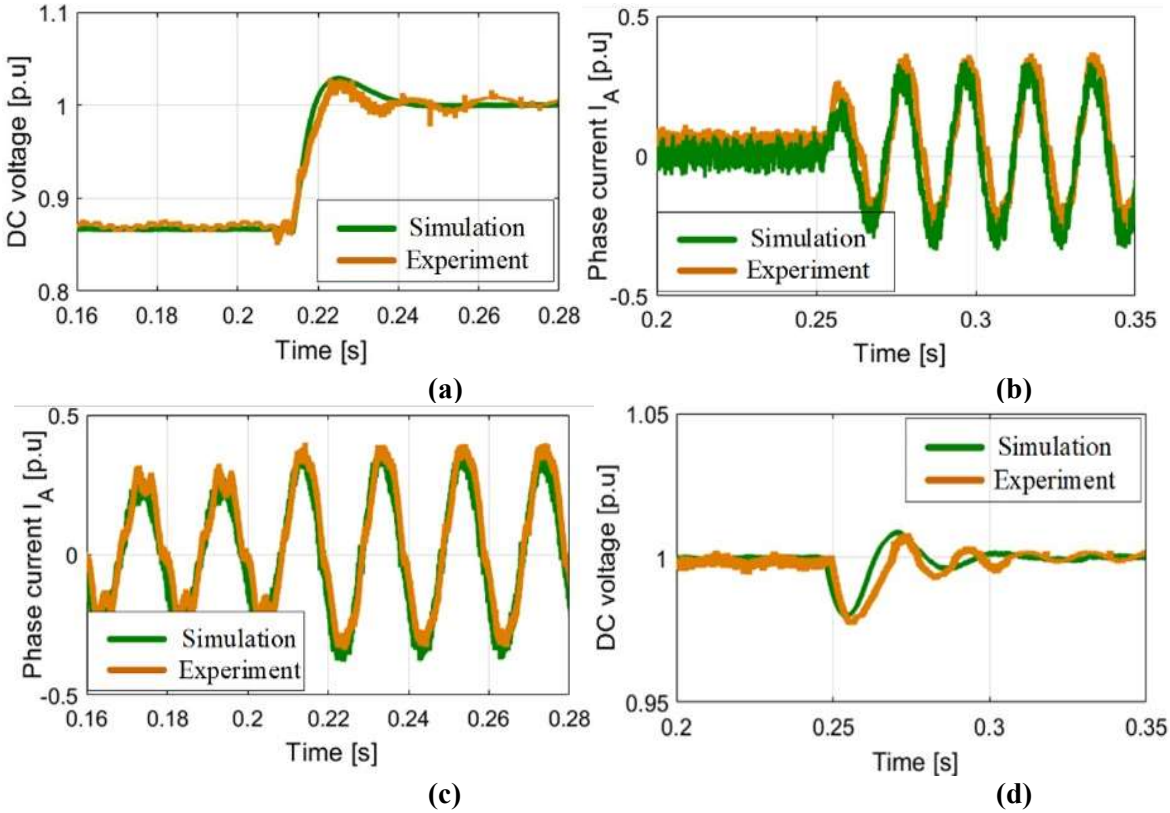
Figure 3.13. Flow chart of the DSP28335 code.

Figure 3.13 shows the flow chart of the programming code. The ADC sampling, calculation of the controllers and PWM run in the PWM Interrupt program due to their rigorous requirements of refresh cycle. In addition, the protection program is put in the External Interrupt to achieve fast fault detection and clearance.



(a) **(b)**

Figure 3.14. Start-up and shutdown procedures: (a) normal condition; (b) overcurrent condition.



(a) **(b)**

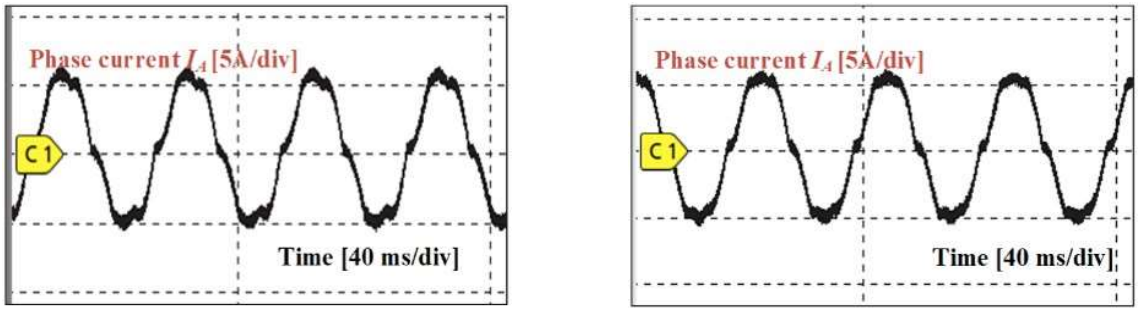
(c) **(d)**

Figure 3.15. Comparison of simulation and experimental results of reference step-changes: (a) DC voltage reference change; (b) power reference change; (c) load current upon reference changes in DC voltage; (d) DC voltage upon reference change in power.

Figure 3.14 shows the start-up and shut-down procedures of the testbed, where Figure 3.14(a) shows the start-up and shut-down procedures under normal operating conditions and Figure 3.14(b) shows the shut down procedure under fault conditions. The power or voltage can

increase or decrease following a ramp function to avoid large overshoot. However, if a fault occurs, the system should be shut down as soon as possible to protect power electronic devices. Thus, the shut-down operations for the normal and fault conditions are different. In normal conditions (see Figure 3.14(a)), the voltage control acts before the power control, and the voltage reference follows a ramp function for both the start and shutdown stages. For contingencies such as an overcurrent condition (see Figure 3.14(b)), the system protection is triggered, during which the PWM driving signals are blocked and the AC coil relays in the three-phase AC circuits are opened. Then, the electric charge stored in the DC capacitors is discharged through a discharging resistor.

Figure 3.15(c) shows the variations in AC current following the reference change in DC voltage shown in Figure 3.15(a). Conversely, Figure 3.15(d) shows the variations of DC voltage under the power reference change shown in Figure 3.15(b). It is seen that the DC voltage and power are controlled well during both transient and steady-state regimes. In addition, the responses obtained from the simulation and the experimental testbed agree on well.



(a) **(b)**

Figure 3.16. Phase-A current waveforms: (a) without resonant controllers in place; (b) including resonant controllers to mitigate 5th and 7th order harmonics.

The harmonic performance is explored in Figure 3.16. To this end, results without resonant controllers to eliminate 5th and 7th harmonics are compared with results when the resonant controllers are in place. As can be seen in Figure 3.16(a), there are waveform distortions when the resonant controllers are not used. The improved waveform with the resonant controller in place is shown in Figure 3.16(b), which, as it can be seen, is closer to a sinusoidal.

A final test considers a control mode transition (see Figure 3.17). The two converter stations are under constant DC voltage and constant power control before time T1. Station 1 changes from DC voltage control to droop control at time T1 while the Station 2 is kept at the constant

power control between T1 and T2. To achieve a smooth transition, coefficient α slowly decreases from 1 to a predetermined value α_0 ($\alpha_0 \in (0,1)$) during a smoothing time T_{smooth} = 10 ms, while β slowly increases from 0 to β_0 ($\beta_0 \in (0,1)$). At time T2, Station 2 changes from constant power control to droop control. Thus, the control modes have been completely switched from the constant power/voltage control to the droop control after T2. It is seen that there are no obvious fluctuations of power and DC link voltage during the control mode transitions.

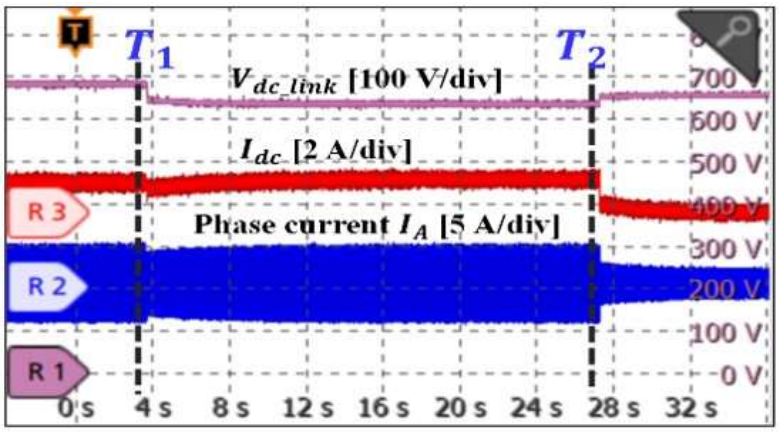


Figure 3.17. Control mode transitions.

From the experimental scenarios, it can be seen that the system is well operated with the given controller parameters. However, the real system features a point-to-point configuration while in this paper, the demonstration system is simply modelled as a back-to-back configuration due to the lack of knowledge of the transmission line impedance. The effect of DC impedance is initially considered in [68], where the results of the simulation indicate that the primary sources of contribution are the odd order harmonics, with the 13th to 19th harmonics being particularly dominant. The line impedance may have an impact on the control which is performed using the controller parameters given in this paper. Thus, the line impedance should be included in the analysis when its value is known, to achieve a better controller design.

3.5 Summary

In this chapter, a simulation model of a cascaded 3L-NPC converter-based MVDC link was verified through an experimental testbed. A hierarchical controller design, from the switching-level to an application-level, was presented. A unique feature of the cascaded 3L-NPC

converter is that each SM is also a standard individual 3L-NPC converter. To coordinate all the SMs, a high-level main controller with communication is thus required. The switching-level control and the converter-level control are implemented in the SM controller, and the application-level control is performed in the main controller. An MVDC testbed with similar per-unit values as the real converter system of ANGLE-DC was developed. With the developed experimental facilities, typical operating scenarios have been verified, including system start-up/shut-down procedures, voltage and power control performance, transition between control modes, and system protection. The results obtained from the experimental testbed and the simulation model based on the real system are in good agreement.

Chapter 4

Active DC Voltage Balancing Control for Submodules of a Cascaded 3L-NPC Converter

This chapter presents the analysis and mitigation methods on the potential voltage imbalance across SMs. The design of the voltage balancing control and the system stability is performed based on the small-signal system model.

4.1 Introduction

For the cascaded 3L-NPC converters, a special technical issue exhibited by the cascaded topology is DC voltage imbalance, which should be considered in particular during the design of controllers. Given that the DC terminals of SMs are connected in series, their shared DC voltages may be different. This may cause SM overvoltage and, potentially, an unstable system operation. Further to the generic control design in Chapter 3, in this Chapter, the cause of DC voltage imbalance was analysed, and DC voltage balancing control was presented in detail. It is revealed that the DC voltage imbalance may occur due to the inversely proportional relationship between the incremental DC voltage and duty cycle within a SM when under power control. This cause is further confirmed by analysing the system model, where each SM is represented as an equivalent impedance as viewed from the DC input terminal. Under DC voltage imbalance, there is an unstable system pole located at the right-half of the *s*-plane. Two balancing control methods are presented to shift the location of system poles and hence, to mitigate the DC voltage imbalance: a PI-based control method that requires communication with a central controller and a communication-less inverse-droop based control method. It is shown that the communication-dependent PI-based method achieves a precise balancing control of DC voltages and decoupling from the power controller. Upon loss of communication, the PI-based method is replaced by the inverse-droop based method to prevent an interruption in system operation. In the presented methods, only an additional PI/inverse-droop controller is required in each SM, and no other hardware is required except for a DC voltage sensor. Thus, the extra cost to the entire system will be limited.

The presented DC voltage balancing control methods are verified through simulations conducted with MATLAB/ Simulink based on the system parameters of the ANGLE-DC project. The effectiveness of the control methods is also experimentally validated using a laboratory-scale MVDC testbed, which is down scaled from the ANGLE-DC project.

4.2 Analysis of DC Voltage Imbalance

4.2.1 Physical Mechanism of DC Voltage Imbalance

A cascaded 3L-NPC converter topology consisting of two SMs is used as an example to analyse the DC voltage imbalance.

For simplicity of analysis, AC voltages in secondary transformers and power factors for SM1 and SM2 are assumed to be equal. If AC power is equally shared by both SMs, then $i_{s1} = i_{s2}$. For each SM, the AC output power is equal to the DC input power. Thus, at steady-state, $V_{dc1} = V_{dc2}$, and no current flows through the DC capacitors of the SMs, as shown in Figure 4.1(a).

However, in practice a slight voltage difference between SM1 and SM2 may appear under transients due to the asynchronous update of control variables, sampling and mismatched component parameters. For example, if $C_{dc1u,l}$ is smaller than $C_{dc2u,l}$ due to the manufacturing tolerance or component degradation, v_{dc1} will be slightly higher than v_{dc2} during a perturbation in the DC link voltage, as shown in Figure 4.1(b).

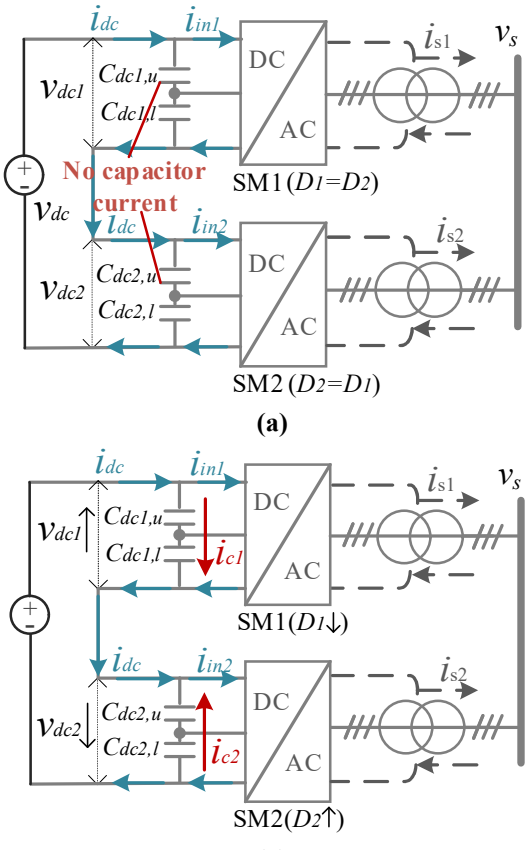


Figure 4.1. Cascaded 3L-NPC converter circuit. (a) Voltage balance at steady-state. (b) Voltage imbalance under a perturbation.

However, the voltage imbalance will not occur if the power flows from the AC side to the DC side. Although the duty cycle is still inversely proportional to the DC voltage, the higher the DC voltage of a SM is, the smaller the duty cycle is and, the less time required for charging time by the AC current. Thus, the DC voltage will be automatically decreased.

This voltage difference between SMs may lead to a further DC voltage imbalance. As the AC power of each SM is regulated by a current controller, equal power sharing can still be achieved under DC voltage perturbations due to the high bandwidth of the current controller. If power flows from the DC side to the AC side, the duty cycle of SM1 (D_1) with a higher voltage (V_{dc1}) will be reduced by the current controller, whereas the duty cycle of SM2 (D_2) with a lower voltage (V_{dc}) will increase. The inverse relationship between duty cycle and DC voltage will inevitably cause V_{dc} to continue increasing and conversely, V_{dc2} to continue reducing.

For MMCs, the uneven charging and discharging processes are caused by the SMs being turned on and off during a fundamental period. This means that only a certain amount of SM capacitors is connected at any time while other capacitors are bypassed [97]. As the instantaneous arm currents flowing through the SMs will be different at different phase angles of a sinusoidal cycle, the charging to the SM capacitors is also different, which leads to the voltage imbalance of the MMC.

4.2.2 Analysis based on the Small-signal Model

The input-to-SM-output transfer matrix for the i^{th} SM at the inverter station is obtained from a state-space representation following linearization of the nonlinear system model [98]. The current controller and the converter plant in a *dq* reference frame are included in the state-space model. It is assumed that the grid voltage v_s is constant and the phase-locked loop (PLL) is ideal; thus, the PLL dynamics that describe the response of system to changes in the input signal or other external factors in order to maintain synchronization are not taken into account.

In this chapter, the neutral-point voltage is controlled by a common-mode modulation signal m_0 [99]. This signal is generated by the voltage difference between the upper and lower capacitors through a PI controller, and then superimposed on the three-phase modulation wave generated by the current controller. The average neutral-point current can be regulated to zero using this method, so the DC offset of the neutral-point voltage can be eliminated. As m_0 only influences the common-mode voltage, the dynamics of the neutral-point voltage are decoupled from those of the terminal voltages [100]. Thus, the DC voltage controller can be designed independently from the neutral-point voltage controller. As only the DC voltage imbalance resulting in the cascaded topology is the main scope of this thesis, the dynamics of the neutral-point voltage are not considered in the system model.

The voltage equations of the AC side at *dq* frames are:

$$v_d = \frac{v_{dc}\delta_d}{2} = Ri_d + L\frac{di_d}{dt} - \omega Li_q + v_s \tag{4-1}$$

$$v_q = \frac{v_{dc}\delta_q}{2} = Ri_q + L\frac{di_q}{dt} + \omega Li_d \tag{4-2}$$

where δ_d and δ_q are the duty cycles calculated by the current PI controllers:

$$\delta_d = \frac{2}{V_{dc}}\left[k_{pid}(i_d^* - i_d) + k_{iid}\int_0^t (i_d^* - i_d)dt - \omega Li_q + v_s\right] \tag{4-3}$$

$$\delta_q = \frac{2}{V_{dc}}\left[k_{piq}(i_q^* - i_q) + k_{iiq}\int_0^t (i_q^* - i_q)dt + \omega Li_d\right] \tag{4-4}$$

where $i_d^* = \frac{2P^*}{3V_s}$ and $i_q^* = \frac{2Q^*}{3V_s}$ are the current references.

The DC side equations are:

$$v_{dc}i_{dc\_conv} = \frac{3}{2}(v_d i_d + v_q i_q) \tag{4-5}$$

$$C_{dc}\frac{dv_{dc}}{dt} = i_{dc} - i_{dc_{conv}} \tag{4-6}$$

Based on the equations of (4-1)−(4-6), the state-space representation for the i^{th} SM is given by

$$\frac{d}{dt}\begin{bmatrix}\Delta x_{id\_I}\\ \Delta x_{iq\_I}\\ \Delta i_{di}\\ \Delta i_{qi}\\ \Delta v_{dci}\end{bmatrix} = \mathbf{A}\underbrace{\begin{bmatrix}\Delta x_{id\_I}\\ \Delta x_{iq\_I}\\ \Delta i_{di}\\ \Delta i_{qi}\\ \Delta v_{dci}\end{bmatrix}}_{\mathbf{x}} + \mathbf{B}\underbrace{\begin{bmatrix}\Delta P_i^*\\ \Delta Q_i^*\\ \Delta i_{dc}\end{bmatrix}}_{\mathbf{u}} \tag{4-7}$$

$$\mathbf{y} = \mathbf{Cx} \tag{4-8}$$

where

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & -k_{iid} & 0 & 0 \\ 0 & 0 & 0 & -k_{iiq} & 0 \\ \frac{1}{L_s} & 0 & -\frac{R}{L_s} - \frac{k_{pid}}{L_s} & 0 & \frac{V_s + RI_d - \omega LI_q}{L_s V_{dc}} \\ 0 & \frac{1}{L_s} & 0 & -\frac{R}{L_s} - \frac{k_{piq}}{L_s} & \frac{RI_q + \omega LI_d}{L_s V_{dc}} \\ \frac{-3I_d}{2C_{dc}V_{dc}} & \frac{-3I_q}{2C_{dc}V_{dc}} & -\frac{3V_s + 3(R - k_{pid})I_d}{2C_{dc}V_{dc}} & -\frac{3(R - k_{piq})I_q}{2C_{dc}V_{dc}} & 0 \end{bmatrix},$$

$$\mathbf{B}=\begin{bmatrix} \frac{2k_{iid}}{3V_s} & 0 & 0 \\ 0 & \frac{2k_{iiq}}{3V_s} & 0 \\ \frac{2k_{pid}}{3L_sV_s} & 0 & 0 \\ 0 & \frac{2k_{piq}}{3L_sV_s} & 0 \\ -\frac{k_{pid}I_d}{C_{dc}V_{dc}V_s} & -\frac{k_{piq}I_q}{C_{dc}V_{dc}V_s} & \frac{1}{C_{dc}} \end{bmatrix}, \mathbf{C}=[0 \quad 0 \quad 0 \quad 0 \quad 1].$$

In the state-space representation, $\mathbf{u}=[\Delta P_i^* \quad \Delta Q_i^* \quad \Delta i_{dc}]^T$ is the input vector, Δv_{dci} is a scalar output, and $\mathbf{x}=\left[\Delta x_{id\_I} \ \Delta x_{iq\_I} \ \Delta i_{di} \ \Delta i_{qi} \ \Delta v_{dci}\right]^T$ is the state vector. In the adopted notation, uppercase variables represent RMS values (or average values) and 'Δ' stands for perturbed variables. P_i^* is the reference of active power, Q_i^* is the reference of reactive power, i_{dc} is the DC link current, i_{di} is the *d*-axis current, i_{qi} is the *q*-axis current, and v_{dci} is the DC voltage. L_s, R and C_{dc} are the transformer leakage inductance, AC circuit resistance and DC capacitance of each SM, ω is the grid frequency, $k_{pid,q}$ and $k_{iid,q}$ are the proportional and integral gains of the PI controller, and Δx_{id_I} and Δx_{iq_I} are the outputs of the integral action of the PI controller.

Based on (4-7) and (4-8), the transfer matrix representation in the Laplace domain is given as

$$\mathbf{Y}(s)=[\mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\mathbf{B}]\mathbf{U}(s)=\mathbf{C}\frac{\text{adj}(s\mathbf{I}-\mathbf{A})}{\det(s\mathbf{I}-\mathbf{A})}\mathbf{B}\mathbf{U}(s)=\mathbf{G}(s)\mathbf{U}(s) \tag{4-9}$$

where *s* is the Laplace variable, 'adj' stands for the adjoint matrix of $(s\mathbf{I}-\mathbf{A})$, 'det' for its determinant, $\mathbf{G}(s)=\mathbf{C}\frac{\text{adj}(s\mathbf{I}-\mathbf{A})}{\det(s\mathbf{I}-\mathbf{A})}\mathbf{B}$ is the transfer matrix, and $\det(s\mathbf{I}-\mathbf{A})$ is the characteristic polynomial. From (4-7)–(4-9), Δv_{dci} can be expressed as

$$\Delta v_{dci}=G_P(s)\Delta P_i^*+G_Q(s)\Delta Q_i^*+G_{idc}(s)\Delta i_{dc} \tag{4-10}$$

where

$G_p(s)=\mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\left[\frac{2k_{iid}}{3V_s} \quad 0 \quad \frac{2k_{pid}}{3L_sV_s} \quad 0 \quad -\frac{k_{pid}I_d}{C_{dc}V_{dc}V_s}\right]^T$, $G_Q(s)=\mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\left[0 \quad \frac{2k_{iiq}}{3V_s} \quad 0 \quad \frac{2k_{piq}}{3L_sV_s} \quad -\frac{k_{piq}I_q}{C_{dc}V_{dc}V_s}\right]^T$, and $G_{idc}(s)=\mathbf{C}(s\mathbf{I}-\mathbf{A})^{-1}\left[0 \quad 0 \quad 0 \quad 0 \quad \frac{1}{C_{dc}}\right]^T$.

As a single SM is modelled, the relationship between different SMs is obtained by analysing the equivalent DC circuit consisting of cascaded SMs. Assuming the parameters for each SM are identical, the voltage equations for an *N* SM-cascaded converter are represented as:

$$\begin{cases} \Delta v_{dc1} = G_P(s)\Delta P_1^* + G_Q(s)\Delta Q_1^* + G_{idc}(s)\Delta i_{dc} \\ \Delta v_{dc2} = G_P(s)\Delta P_2^* + G_Q(s)\Delta Q_2^* + G_{idc}(s)\Delta i_{dc} \\ \vdots \\ \Delta v_{dcN} = G_P(s)\Delta P_N^* + G_Q(s)\Delta Q_N^* + G_{idc}(s)\Delta i_{dc} \\ \sum_{i=1}^{N} \Delta v_{dci} = \Delta v_{dc\_link} \end{cases} \tag{4-11}$$

For an equal current sharing in each SM, $\Delta P_1^* = \Delta P_2^* = \cdots = \Delta P_N^* = \frac{\Delta P^*}{N}$ and $\Delta Q_1^* = \Delta Q_2^* = \cdots = \Delta Q_N^* = \frac{\Delta Q^*}{N}$. An equivalent DC circuit for such conditions is shown in Figure 4.2.

In Figure 4.2, $Z_{dc}^P(s) = G_{idc}(s)$, $D_d(s) = G_P(s)/G_{idc}(s)$, $D_q(s) = G_Q(s)/G_{idc}(s)$. A relationship between the neighbouring SMs is obtained from the equivalent DC circuit as follows:

$$\frac{\Delta v_{dc,i}}{Z_{dc}^P(s)} = \frac{\Delta v_{dc,i+1}}{Z_{dc}^P(s)} = \Delta i_{dc} - \frac{D_d(s)\Delta P^* + D_q(s)\Delta Q^*}{N} \tag{4-12}$$

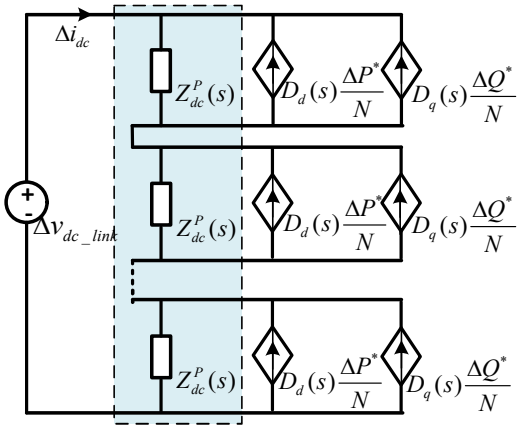


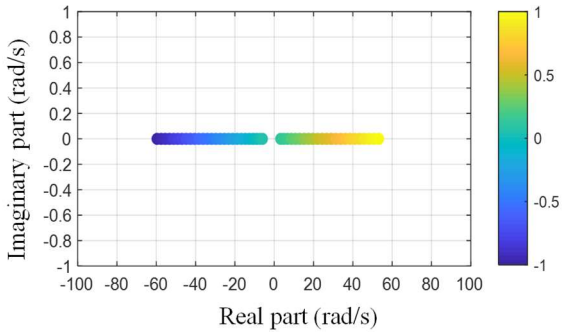
Figure 4.2. Equivalent DC circuit for equal current sharing in each SM.

Based on (4-9) and (4-12),

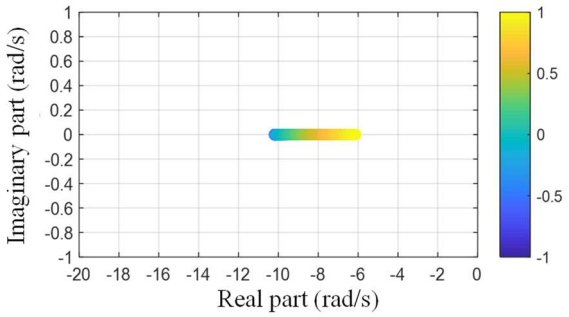
$$\det(s\mathbf{I} - \mathbf{A})\left(\Delta v_{dc,i} - \Delta v_{dc,i+1}\right) = (a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0)\left(\Delta v_{dc,i} - \Delta v_{dc,i+1}\right) = 0 \tag{4-13}$$

where a_0, a_1, a_2, a_3, a_4 and a_5 are given in the Appendix A. From (4-13), ensuring an equal voltage sharing between SMs and the speed to achieve this are dictated by the eigenvalues of system matrix **A** (i.e., the poles of the $Z_{dc}^P(s)$). The root locus of $Z_{dc}^P(s)$ with varying operating points is shown in Figure 4.3. System parameters in Table 3.1 are used to plot the root locus. As the system has five poles, only the dominant poles are displayed for clarity. Figure 4.3(a)

shows the trajectory of the dominant poles when P changes from -1 p.u. to 1 p.u. with Q equal to zero. As it can be seen, a right-half-plane pole is introduced when the active power is changed from a negative value (rectifier mode) to a positive value (inverter mode), which is the cause of the DC voltage imbalance. The dominant pole moves from the coordinate (-60, j0) to around (60, j0) on the s plane with the increase of active power. Thus, as the power increases, the dominant pole moves further away from the original point and hence DC voltage diverges faster. Figure 4.3(b) shows instead the trajectories when Q changes from -1 p.u. to 1 p.u. and P is set to zero. It is observed that the DC voltage balance is not affected by Q as the pole is always located at the left-half of the s-plane, although the response time for voltage balancing would slow down as the pole moves closer to the imaginary axis.



(a)



(b)

Figure 4.3. Root locus of dominant poles (obtained by solving equation (4-13)) for different power operating conditions. (a) P changes and $Q = 0$. (b) Q changes and $P = 0$.

4.3 Voltage Balancing Control Methods

Two control methods to achieve a balanced DC voltage are presented in this section. Firstly, a PI-based method relying on communications is presented. Then, a droop-based control method, suitable upon loss of communication, is discussed.

4.3.1 PI based Control with Communication

A block diagram for this control method is shown in Figure 4.4.

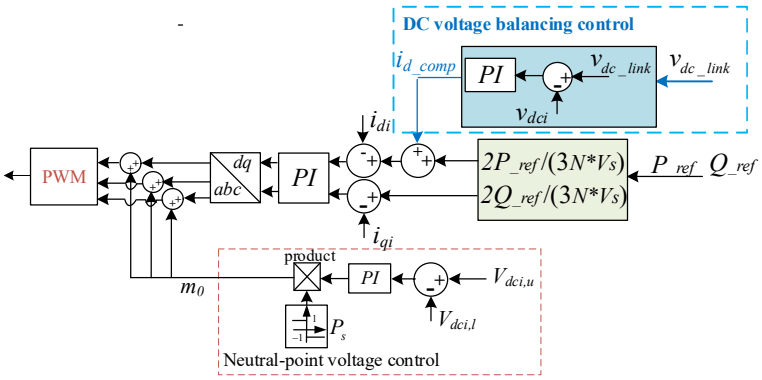


Figure 4.4. PI-based voltage balancing controller with communication.

The PI-based DC voltage balancing controller is added to each *P/Q* controller at the inverter station. A high-level central controller measures the DC link voltage and sends the instantaneous DC voltage (v_{dc_link}) and power references ($P_{\_ref}$ and $Q_{\_ref}$) to the low-level controller at each SM through the RS485 communication interface, as shown in Figure 4.4. The low-level controller uses the average DC voltage and compares it with the DC voltage of each SM. A PI controller is used to generate a compensating current reference to adjust the DC voltage. Through this feedback structure, the DC voltage of each SM can converge to the average value. As reactive power has a negligible effect on the voltage imbalance, the PI-based structure is added to the *d*-axis control loop only (i.e., superimposed with the active power controller). In addition, a PI-based neutral-point voltage control method is used to balance the neutral-point voltage of each SM. The output of its PI controller acts as the zero-sequence variable which is added on the three-phase sinusoidal modulation waveforms.

Due to the integral action of the PI controller, the steady-state error of DC voltage difference is driven to zero. In addition, as the central controller sends the instantaneous DC link voltage value to each SM, the sum of the compensation currents supplied by the PI controllers is zero (i.e. $\sum_{i=1}^{N} i_{d\_compi} = G_{PI}(s) \sum_{i=1}^{N} \left(\frac{v_{dc\_link}}{N} - v_{dci}\right) = 0$ and $G_{PI}(s)$ is the transfer function of the DC voltage balancing PI controller). Therefore, the voltage balancing control method does not affect the output power, which means it is decoupled from the power control.

To verify the decoupling between the DC voltage balancing control and the neutral-point voltage balancing control, a set of comparative simulations was conducted. Figure 4.5(a) shows the neutral-voltage when a single 3L-NPC SM is used (without cascading other SMs), while Figure 4.5(b) shows the neutral-point voltage of one SM in the case of four cascaded SMs. The

neutral-point voltage in both cases shows similar values with regards to the DC offsets and the 3rd order voltage ripples.

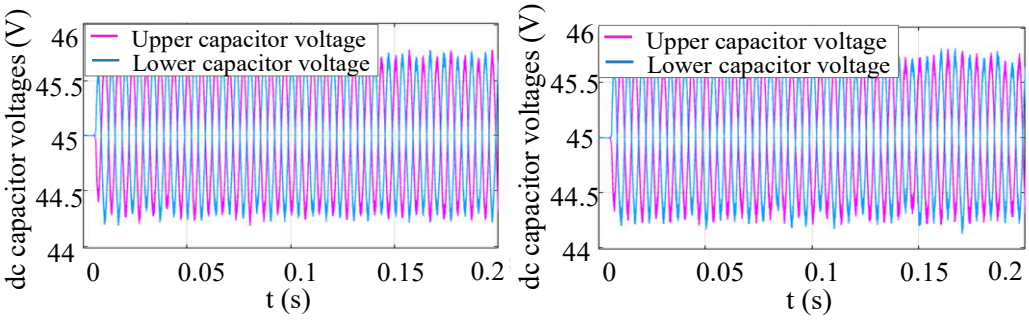


Figure 4.5. Neutral-point voltage waveforms: (a) waveforms without DC voltage balancing control; (b) waveforms with DC voltage balancing control.

Controller parameters should be properly selected for the presented voltage balancing controllers. The selection can be performed through small-signal analysis and pole placement. The system poles should be placed in the left-half plane to guarantee system stability.

With the use of DC voltage balancing control, the voltage equation (4-10) is rewritten as

$$\Delta v_{dci} = G_P(s)\frac{\Delta P^*}{N} + G'_P(s)G_{PI}(s)\left(\frac{\Delta v_{dc_{link}}}{N} - \Delta v_{dci}\right) + G_{idc}(s)\Delta i_{dc} \tag{4-14}$$

where the current source generated from reactive power has been omitted due to its negligible influence. In (4-14), $G'_P(s) = \frac{3V_s}{2}G_P(s)$ and $G_{PI}(s) = -\frac{k_{pudc}s + k_{iudc}}{s}$. Based on [101], $k_{iudc} = 200k_{pudc}$ is adopted. Letting $Z^C_{dc}(s) = \frac{G_{idc}(s)}{G_P(s)G_{PI}(s)}$, the equivalent DC circuit of the cascaded topology is shown in Figure 4.6.

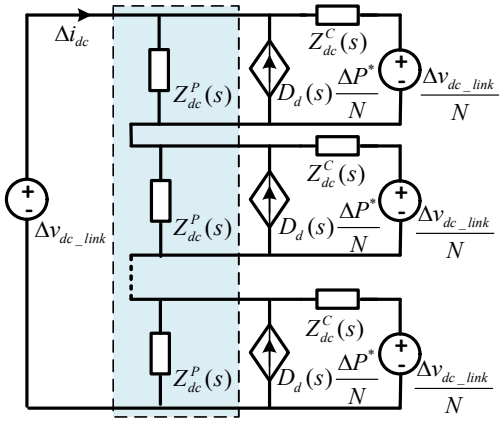


Figure 4.6. Equivalent DC circuit with PI controller.

From Figure 4.6, as each SM works with communication and all SMs have the same parameters, the equivalent DC circuit of each SM is identical. The input DC impedance $Z_{dc}^{U}(s)$ of each SM is obtained by setting the output of the voltage and current sources to zero, resulting in

$$Z_{dc}^{U}(s) = Z_{dc}^{C}(s)//Z_{dc}^{P}(s) = \frac{G_{idc}(s)}{1+G_{P}^{I}(s)G_{PI}(s)} \tag{4-15}$$

where symbol '//' stands for a parallel connection. The relationship between the neighbouring SMs in Figure 4.6 is given by

$$\underbrace{\left(\det(s\mathbf{I}-\mathbf{A})\,s-\mathbf{C}\mathrm{adj}(s\mathbf{I}-\mathbf{A})\begin{bmatrix}\frac{2k_{iid}}{3V_s}\\0\\\frac{2k_{pid}}{3LV_s}\\0\\-\frac{3k_{pid}I_d}{2C_{dc}V_{dc}}\end{bmatrix}\left(k_{pudc}s+k_{iudc}\right)\right)}_{G_{u,1}(s)}\times\left(\Delta v_{dc,i}-\Delta v_{dc,i+1}\right)=$$

$$(a_6's^6+a_5's^5+a_4's^4+a_3's^3+a_2's^2+a_1's+a_0')\left(\Delta v_{dc,i}\Delta v_{dc,i+1}\right)=0 \tag{4-16}$$

where a_0', a_1', a_2', a_3', a_4', a_5', a_6' are given in the Appendix A. $G_{u,1}(s)$ is the denominator term of $Z_{dc}^{U}(s)$ following suitable algebraic expansion. Thus, the eigenvalues of $G_{u,1}(s)$ are the poles of $Z_{dc}^{U}(s)$. The root locus of the dominant poles of $Z_{dc}^{U}(s)$ is shown in Figure 4.7 for both positive and negative power flows. The eigenvalue trajectories are plotted for rated power (i.e., P =1 p.u.) as proportional gain k_{pudc} increases from 0 to 50 p.u., with a base value $Z_{dc\_base} = \frac{V_{DC\_base}^2}{S_{base}}$ ($S_{base} = S$, $V_{DC\_base} = V_{DC}$).

For an inverter mode, shown in Figure 4.7(a), the poles move to the left-half of the s-plane as k_{pudc} increases, thus demonstrating the effectiveness of the voltage balancing method. However, the value of k_{pudc} should not be too large; otherwise, the poles may become unstable when power flow is reversed, as shown in Figure 4.7(b).

To ensure an acceptable damping ratio of complex conjugate dominant poles (≥ 0.5), these poles should lie inside a specific region of the complex plane within a radial line drawn from the origin and its reflection across the real axis. The radial line is at an angle of 60° with reference to the negative real axis [102]. This condition is achieved if the proportional gain of the PI controller is selected as $k_{pudc} = 25$.

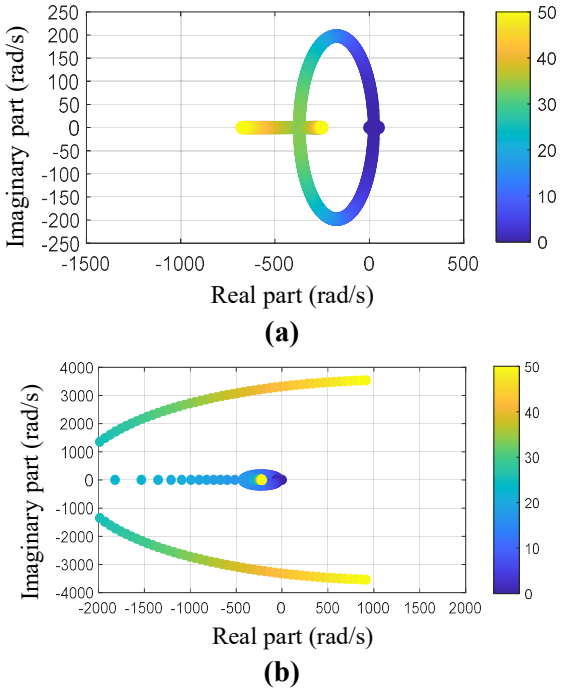


Figure 4.7. Root locus of dominant poles (obtained by solving equation (4-16)) with increasing k_{pudc} under PI controller. (a) Positive power flow. (b) Negative power flow.

4.3.2 Inverse-droop based Control without Communication

Communication may be lost during operation. Under such conditions, the high-level central controller would not be able to send DC link voltage information to the SMs—thus making the system vulnerable to instability. To prevent this, a self-balancing control method without the need for communication is presented. The method is inspired by the droop control strategies employed in DC/DC converters [103] and adapted to control the cascaded 3L-NPC converter.

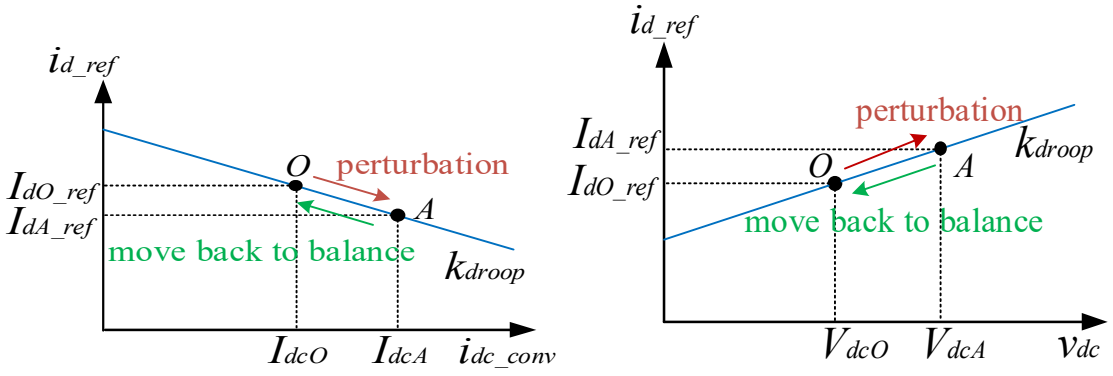


Figure 4.8. Droop curves for voltage balancing control. (a) $i_{dc\_conv} - i_d^*$ curve. (b) $v_{dc} - i_d^*$ curve.

Two potential control implementations are discussed. In the first one, shown in Figure 4.8(a), the current reference i_d^* is adjusted by i_{dc_conv}, which is the DC current entering the converter after passing through the DC capacitor (see Figure 4.1). Current i_{dc_conv} could move from the equilibrium point I_{dcO} to I_{dcA} following a perturbation, which discharges the DC capacitor. According to the droop curve, i_d^* will decrease to prevent the DC capacitor from discharging so that the operating condition moves back to the equilibrium point. The advantage of using this method is that it does not require DC voltage sensors. However, the reconstruction of i_{dc_conv} through AC currents may introduce noise interference, which is not desirable.

The second method, called the inverse-droop controller, is shown in Figure 4.8(b). When v_{dc} changes from the equilibrium point V_{dcO} to V_{dcA} following a perturbation, i_d^* increases according to the curve shown. Thus, the discharge of the DC capacitor will be accelerated to move the DC voltage down to the equilibrium point.

Since the noise introduced by the reconstruction of current in the first method may deteriorate the control performance, the inverse-droop controller is adopted instead. Its schematic is shown in Figure 4.9. It should be noted that due to the fixed reference point V_{dcO}, the sum of i_{d_compi} is not guaranteed to be zero (i.e., $\sum_{i=1}^{N} i_{d\_compi} = K_{droop} \sum_{i=1}^{N} (v_{dci} - V_{dcO}) \neq 0$). This means the DC voltage balancing control is coupled to the power control loop. Due to this, it is recommended that the inverse-droop controller is adopted as a replacement of the PI-based controller only upon communication failure.

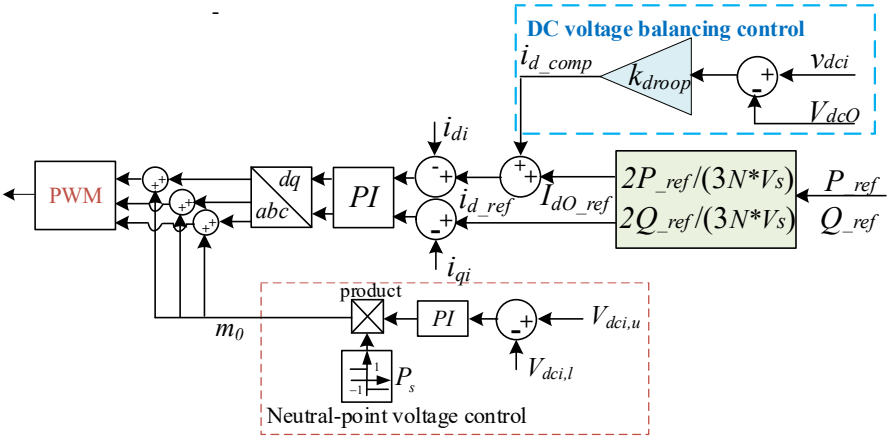


Figure 4.9. Inverse-droop based voltage balancing controller.

The gain of the droop-based voltage balancing controller is tuned based on the small-signal analysis. The voltage equation for SMs without communication is given by

$$\Delta v_{dci} = G_P(s)\frac{\Delta P^*}{N} + G'_P(s)k_{droop}\Delta v_{dci} + G_{idc}(s)\Delta i_{dc} \tag{4-17}$$

where $Z_{dc}^{C1}(s) = \frac{G_{idc}(s)}{k_{droop}G'_P(s)}$. Figure 4.10 shows the equivalent circuit for this condition, from where the DC equivalent impedance with inverse-droop controller is obtained as

$$Z_{dc}^{U1}(s) = Z_{dc}^{C1}(s)//Z_{dc}^{P}(s) = \frac{G_{idc}(s)}{1+k_{droop}G'_P(s)} \tag{4-18}$$

The voltage equation of neighbouring SMs is given by

$$\underbrace{\left(\det(s\mathbf{I}-\mathbf{A}) - \mathbf{C}\text{adj}(s\mathbf{I}-\mathbf{A})\begin{bmatrix}\frac{2k_{iid}}{3V_s}\\0\\\frac{2k_{pid}}{3LV_s}\\0\\-\frac{3k_{pid}I_d}{2C_{dc}V_{dc}}\end{bmatrix}k_{droop}\right)}_{G_{u,2}(s)} \times \left(\Delta v_{dc,i} - \Delta v_{dc,i+1}\right) =$$

$$(a_5''s^5 + a_4''s^4 + a_3''s^3 + a_2''s^2 + a_1''s + a_0'')\left(\Delta v_{dc,i} - \Delta v_{dc,i+1}\right) = 0 \tag{4-19}$$

where a_0'', a_1'', a_2'', a_3'', a_4'', a_5'' are given in the Appendix A. $G_{u,2}(s)$ is the denominator term of $Z_{dc}^{U1}(s)$. The root locus of the dominant poles as the droop coefficient k_{droop} is increased from 0 to 50 p.u., for P = 1 p.u., is plotted for both positive and negative power flows.

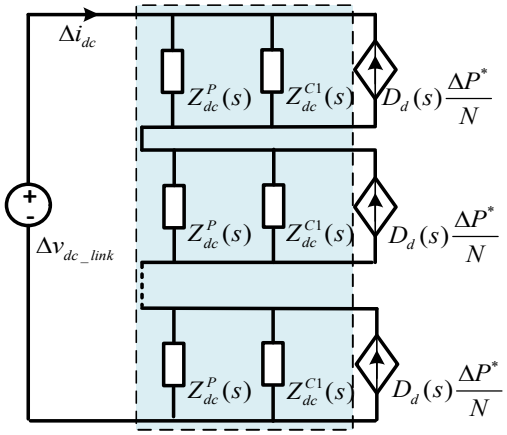


Figure 4.10. Equivalent DC circuit with inverse-droop controller.

As shown in Figure 4.11, increasing the value of k_{droop} will guarantee the system is stable for an inverter operation. However, k_{droop} should not be larger than 40 to preserve stability for rectifier operation according to Figure 4.11(b). Although a larger k_{droop} ensures a better voltage balance characteristic, it may affect the accuracy of the output power [55]. Thus, an appropriate value should be carefully selected considering both the performance of voltage balancing and the impact on the power control. The value of the droop coefficient k_{droop} is set

as 10 to maximize the voltage balancing performance and to restrict the influence on the power control.

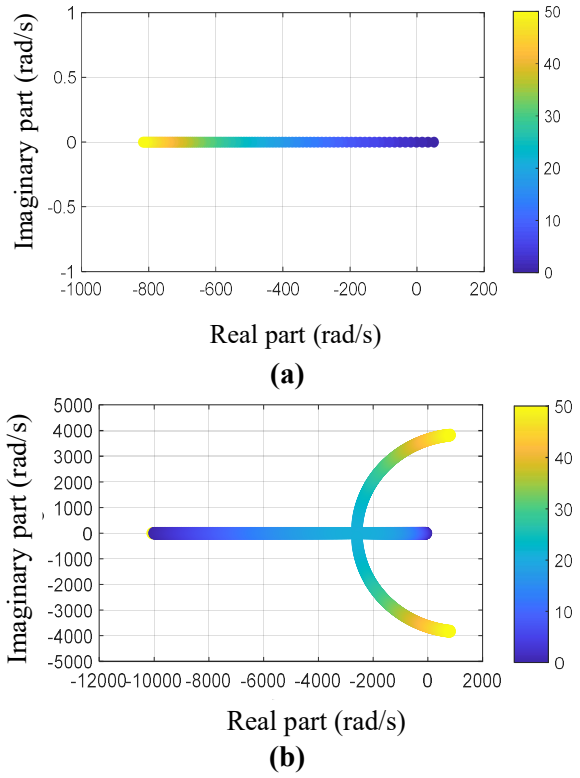


Figure 4.11. Root locus of dominant poles (obtained by solving equation (4-19)) with increasing k_{droop} under inverse-droop controller. (a) Positive power flow. (b) Negative power flow.

4.3.3 Hybrid Control combining PI and Inverse-droop based Control Methods

If the number of SMs with communication is m and the number of SMs without communication is l (with $l = N - m$), then

$$m\Delta v_{dc,i} + l\Delta v_{dc,j} = \Delta v_{dc\_link} \tag{4-20}$$

where Δv_{dci} and Δv_{dcj} denote the DC voltage of the i^{th} SM with communication and the DC voltage of the j^{th} SM without communication, respectively. Combining equations (4-16), (4-19) and (4-20), a relationship between $\Delta v_{dc,i}$ and $\Delta v_{dc,j}$ is obtained as

$$\mathbf{C}\text{adj}(s\mathbf{I} - \mathbf{A})\begin{bmatrix}0 & 0 & 0 & 0 & \frac{1}{C_{dc}}\end{bmatrix}^{T}\left((N-m)G_{u,1}(s) + mG_{u,2}(s)s\right)\left(\Delta v_{dc,i} - \Delta v_{dc,j}\right) = 0 \tag{4-21}$$

where $G_{u,1}(s)$ and $G_{u,2}(s)$ are the same as in (4-16) and (4-19). Figure 4.12 shows the root locus of the dominant poles p_i (i =1, 2) as m varies from 1 to 11, with the active power being

kept at 1 p.u. The controller parameters are selected according to the analyses in Sections III-B-1 and III-B-2, where $k_{pudc} = 25$ and $k_{droop} = 10$. As it can be seen, one of the poles moves close to the imaginary axis as m is increased, which means that the difference of DC voltage between SMs converges to zero at a decreased rate. The worst case happens when m = 11.

To have a comprehensive understanding of the hybrid control structure, the Bode diagram of a transfer function $G_d(s) = \frac{\Delta v_{dci}(s) - \Delta v_{dcj}(s)}{\Delta v_{dc_{link}}(s)}$ is used to analyze the disturbance rejection ability of the cascaded converters. $G_d(s)$ reflects the impact of the DC link voltage perturbation on the voltage difference between SMs. The smaller the amplitude of $G_d(s)$ is, the better the disturbance rejection.

Both cases for m=1 and m=11 are studied, and the Bode diagram is shown in Figure 4.13. The voltage balancing performance for both cases is influenced by the perturbation of the DC link voltage. However, the magnitude in the Bode diagram for the case when m=1 (i.e., 1 PI controller and 11 inverse-droop controllers) is lower than that for the case when m=11 (i.e., 11 PI controllers and 1 inverse-droop controller) at frequencies below 400 rad/s, which implies that a larger DC voltage error may appear resulting from the perturbation as m increases. This illustrates that the disturbance rejection ability is decreased as more PI-based controllers are used in the hybrid structure.

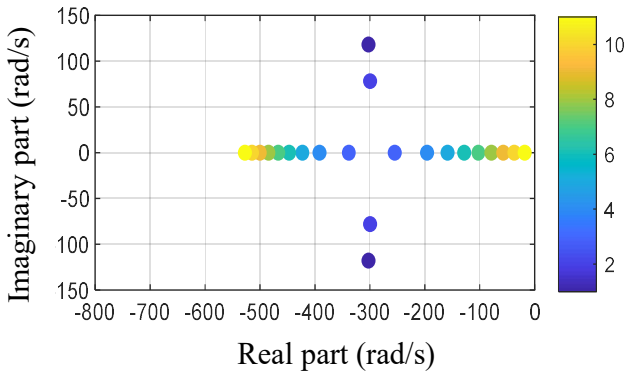


Figure 4.12. Root locus of dominant poles (obtained by solving equation (4-21)) with increasing values of m, with $k_{pudc} = 25$ and $k_{droop} = 10$.

On the contrary, if all the SMs work under the same control strategy (either PI-based control or inverse-droop based control), they will exhibit a similar dynamic performance regardless of the number of cascaded SMs. Thus, it is recommended that all the SMs should automatically switch to communication-less control if communication with any SM is lost.

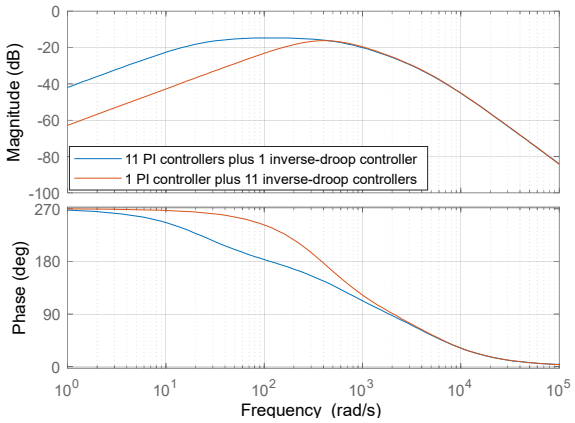


Figure 4.13. Bode diagram of $G_d(s) = \frac{\Delta v_{dci}(s) - \Delta v_{dcj}(s)}{\Delta v_{dc_{link}}(s)}$.

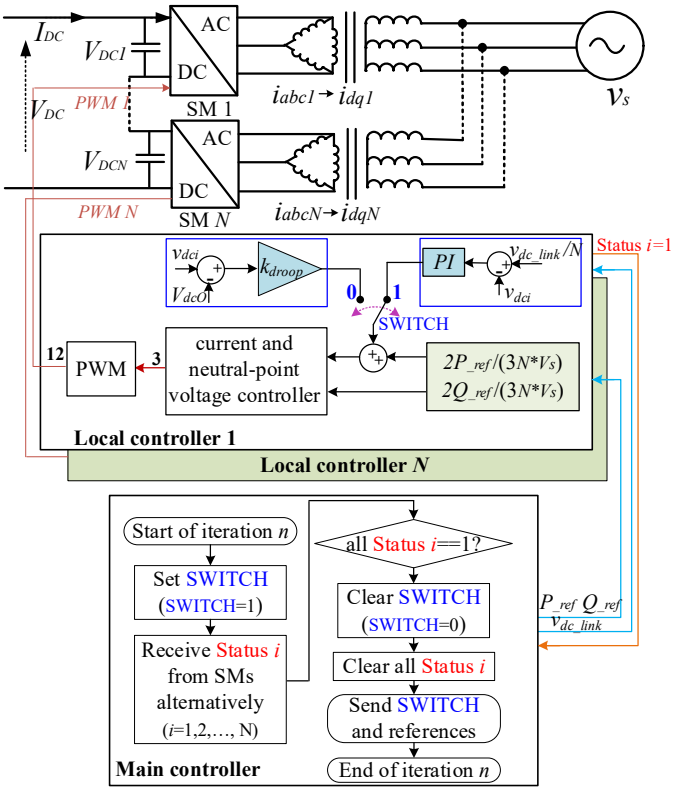


Figure 4.14. Overall control structure combing both control loops.

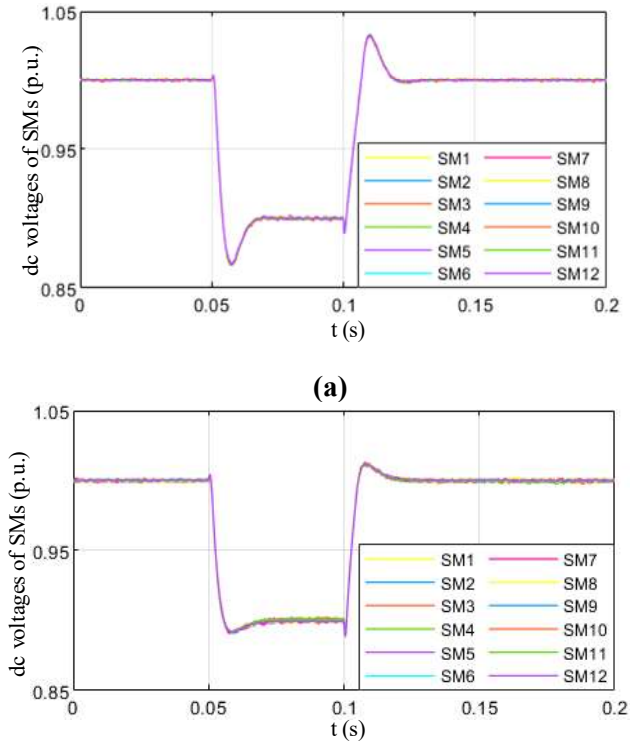
Both DC voltage balancing control methods combing their mode switching are integrated into Figure 4.14. To switch from the PI-based control scheme to an inverse-droop scheme, the Modbus protocol between the central and SM controllers is used. The control modes are selected by the SWITCH command. The PI-based voltage balancing control is used when SWITCH = 1 and switches to the droop-based control with SWITCH = 0. To achieve this, the Status i is returned from the SM's controller to the main controller. If all Status i equal 1, the

communication is assumed as normal, and SWITCH is set as 1 by the main controller. Otherwise, there are communication failures of SMs. SWITCH will be set as zero to switch the SMs to the droop-based control mode. The SMs which lost communication will automatically switch their control mode.

4.4 Simulation and Experimental Validation

4.4.1 Simulation Results

The control methods presented in Section 4.3 were verified by conducting simulations in MATLAB/Simulink, with results shown in Figure 4.15 and Figure 4.16. Operation for twelve cascaded SMs is simulated, and the simulation parameters are provided in Table I. The performance of the voltage balancing control methods is assessed for step changes in the DC link voltage, with results presented in Figure 4.15(a) when communication is available (PI-based control) and in Figure 4.15(b) when communication is lost (inverse-droop based control).



(a)

(b)

Figure 4.15. DC voltages of SMs 1 to 12. (a) with PI-based control. (b) with inverse-droop based control.

From the results, it can be seen that both control methods successfully achieve DC voltage balancing upon step changes in the DC link voltage (see how the traces for all SMs exhibit a similar behaviour). This is consistent with the eigenvalue analysis presented in Section 4.3.

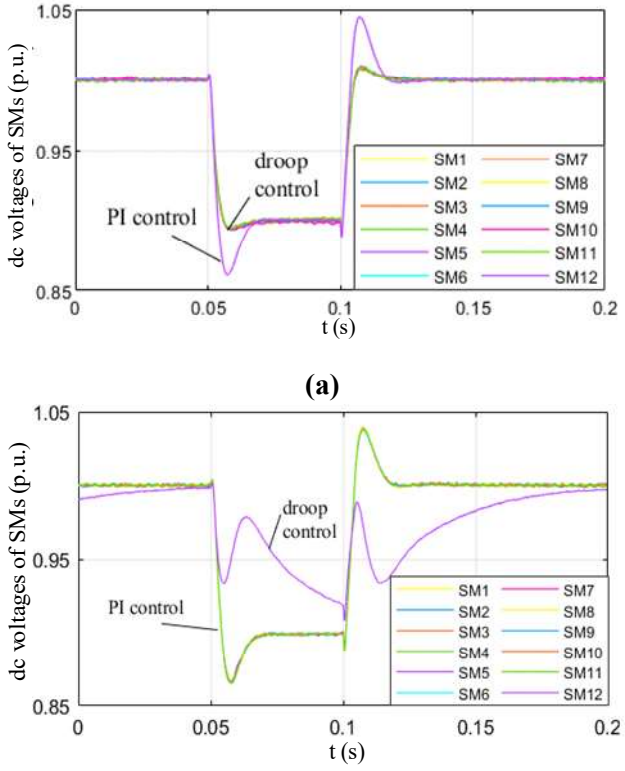


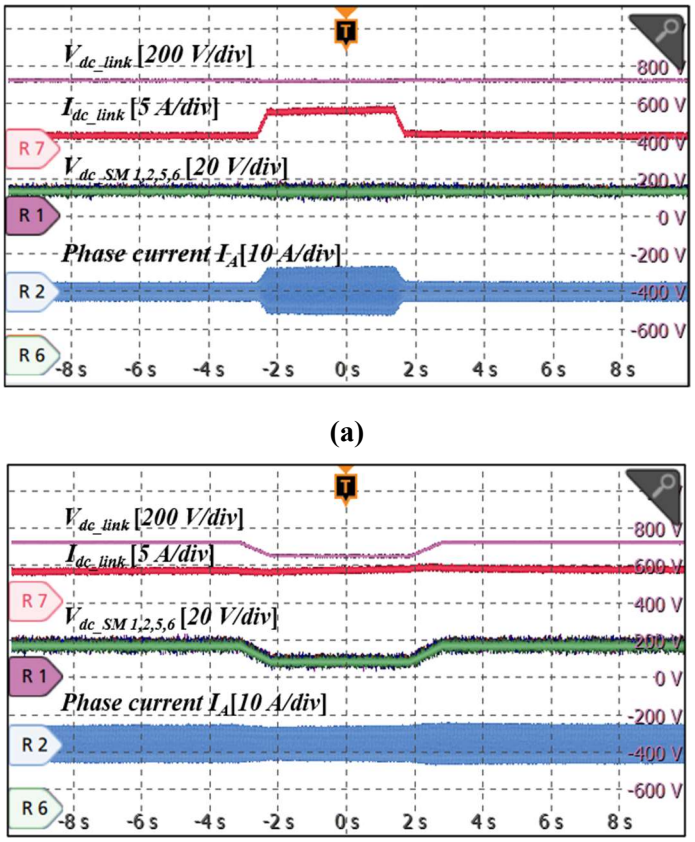
Figure 4.16. DC voltages of SMs 1 to 12 for a hybrid control structure. (a) 1 PI controller plus 11 inverse-droop controllers. (b) 1 inverse-droop controller plus 11 PI controllers.

For completeness, system performance is also verified for a hybrid control structure considering some SMs with communication and the rest without it, as described in Section 4.3.3. For simplicity, only the extreme cases are provided: the results shown in Figure 4.16(a) correspond to the case when m = 1 (i.e., a single SM has communication and 11 SMs feature the communication-less inverse-droop controllers), whereas results in Figure 4.16(b) show the case for m = 11 (i.e., 11 SMs have communication and 1 SM features the communication-less inverse-droop controller). As it can be observed from these results, an increase in the number of SMs with PI-based control in the hybrid structure will aggravate the DC voltage imbalance under dynamic conditions.

4.4.2 Experimental Results

The system configuration used for experimental test is same as that in Chapter 3, where eight SMs are cascaded. For the experiments, the performance of the voltage balancing methods is assessed for reference changes in the set points of active power and DC voltage. Figure 24 shows representative experimental results for the PI-based control scheme. The top purple trace shows the DC link voltage, the red trace (second layer from the top) shows the DC link current,

and the green, orange, pink and dark blue traces (third layer) show the DC voltages of four SMs. The bottom blue trace shows the current of phase a. At the start of the experiment, the DC link voltage is increased by the rectifier station to the rated value (i.e., 720 V). After the rated DC link voltage is reached, the inverter station begins to regulate power according to the active power references (at around 4.2 kW) sent by the high-level central controller. At this point, the PI-based voltage balancing controller is enabled. Figure 4.17(a) shows results for a reference change in power, whereas Figure 4.17(b) shows results for a reference change in DC voltage. The references are modified using ramp functions with slopes of 750 W/s and 10 V/s, respectively, to achieve a smooth dynamic behaviour, as opposed to step changes. For simplicity, DC voltage traces for 4 SMs (SM1, SM2, SM5 and SM6) are shown only. It can be observed that all SMs exhibit a balanced DC voltage performance for both types of reference change.



(a)

(b)

Figure 4.17. Operation with PI-based DC voltage balancing controllers. Results for: (a) active power reference change; (b) DC link voltage reference change.

Figure 4.18 shows the system performance when communication is lost. Under such conditions, the DC voltage balancing control is disabled altogether. The DC voltages of the SMs diverge

afterwards, although the total DC link voltage is kept constant. To avoid overvoltage at some SMs, the system protection is triggered, during which the PWM driving signals are blocked and the AC coil relays in the three-phase AC circuits are opened.

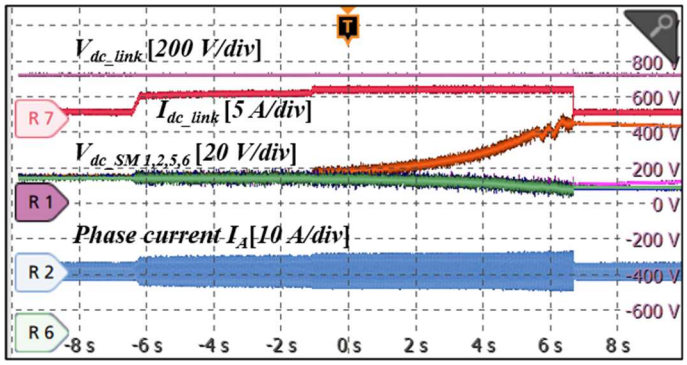
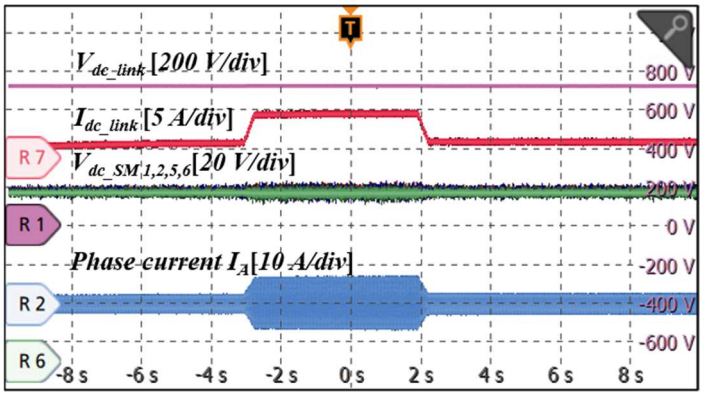
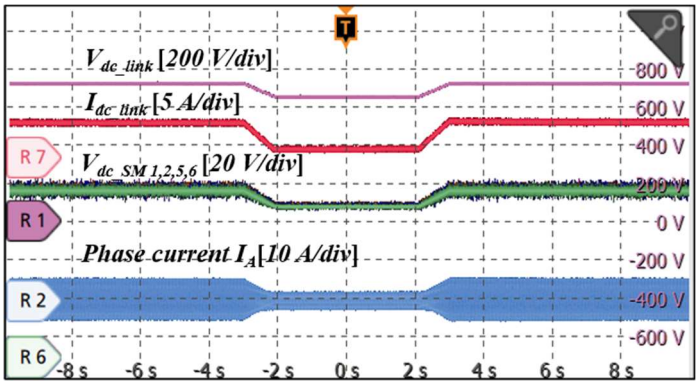


Figure 4.18. Operation when communication is lost.



(a)



(b)

Figure 4.19. Operation with droop-based DC voltage balancing controllers. Results for: (a) active power reference change; (b) DC link voltage reference.

A final experiment is conducted for the case of invalid communication. In this case, communication-less inverse-droop based control will be activated in place of the PI-based

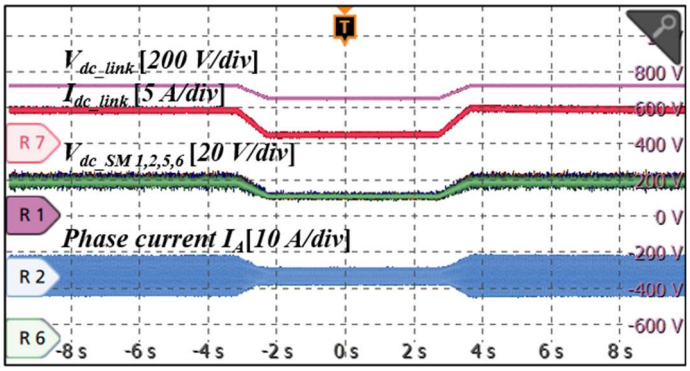
control requiring communication. Figure 4.19 shows the experimental results when all SMs operate with the inverse-droop controllers. Similar experimental conditions as for the PI-based control method are used, with the results presented in Figure 4.19 showing the system performance upon ramp reference changes in active power and DC link voltage as previously discussed. As it can be seen, the inverse-droop based method ensures system stability when communication is not available.

However, as the given voltage reference employed is the historic value just before communication is lost, the inverse-droop controller will influence the output power accuracy during the reference change of DC link voltage, regulated by the rectifier station, as shown in Figure 4.19(b). This demonstrates the coupling between the voltage balancing controller and the power controller, as discussed in Section III. Given that the main focus of this chapter is to address DC voltage imbalance, compensation for power accuracy falls out of the scope of the work. The interested reader is referred to [57], where a suitable control method to mitigate this disadvantage can be found.

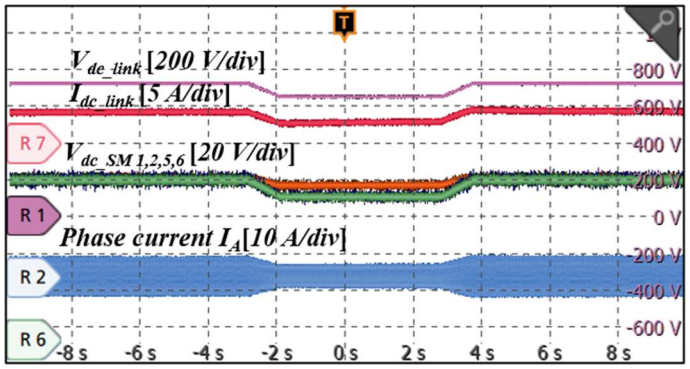
The experimental performance of a hybrid control structure combining both DC voltage balancing methods is shown in Figure 4.20. Two extreme cases are studied: one PI-based controller and seven inverse-droop based controllers (with results shown in Figure 4.20(a)) and seven PI-based controllers and one inverse-droop based controller (with results shown Figure 4.20(b)). It can be seen that the DC voltage balancing performance worsens as the number of PI-based controllers in a hybrid structure increases. Since the hybrid control method influences the DC voltage balancing performance, it is recommended that all SMs change from PI-based to the inverse-droop based control once communication fails at any SM. For completeness, Figure 4.21 shows the transition between the control modes.

Tests are also conducted to explore the influence of the DC voltage balance control on the neutral-point voltage control. The neutral-point voltages (upper and lower DC capacitors' voltages) of the SM1, 2, 5 and 6 are shown in Figure 4.22. It can be seen that the neutral-point voltage of any SM is still balanced under the presented DC voltage balancing control. To further validate the decoupling between the DC voltage balancing control and neutral-point voltage balancing control, an experimental test has been conducted with results shown in Figure 4.23 (the performance of 4 SMs is shown only). At the beginning of the test, the SMs are equipped with both neutral-point voltage balancing control and DC voltage balancing

control. At time 0.8 s, the DC voltage balancing control is disabled. As it can be seen, a divergent DC voltage imbalance occurs afterwards. However, neutral-point voltage balance is still maintained although the DC voltage is unbalanced.



(a)



(b)

Figure 4.20. Operation with hybrid DC voltage balancing control methods. (a) one PI-based controller and seven inverse-droop based controllers. (b) seven PI-based controllers and one inverse-droop based controller.

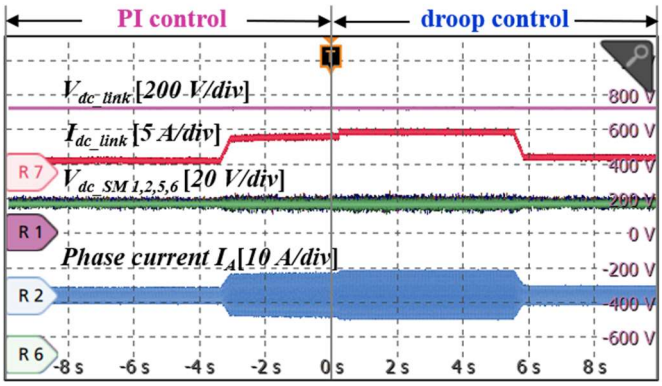


Figure 4.21. Waveforms under mode transition.

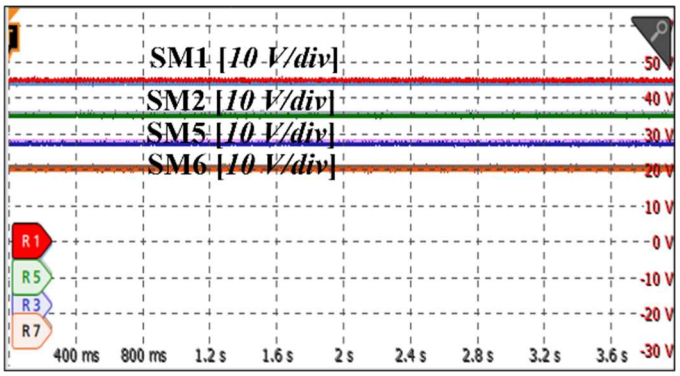


Figure 4.22. Upper and lower DC voltage waveforms of SM1,2,5,6 under DC voltage balancing control.

It should be emphasized that the controller parameters in the experimental tests are smaller than the ones used in the simulations. The reason is that the voltage imbalance is not too severe due to the restricted power condition used in the experiments. Thus, the controller parameters have been selected smaller than the set of parameters used for rated power.

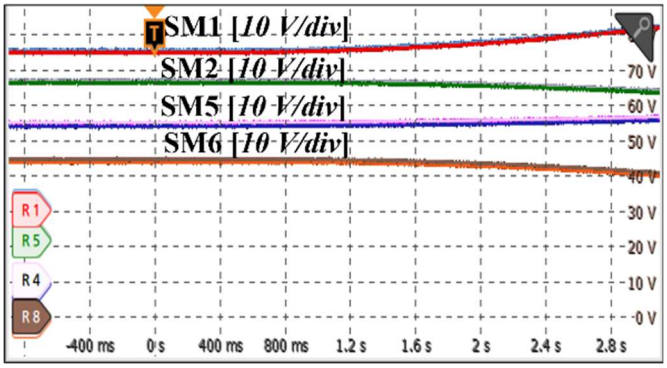


Figure 4.23. Upper and lower DC voltage waveforms of SM1,2,5,6 under DC voltage balance and imbalance.

4.5 Summary

For the cascaded 3L-NPCconverters, DC voltage imbalance across SMs is a special issue which may pose challenge to the system operation. This should be focused when designing the control system. This chapter reveals the cause of imbalance and presents two control methods to balance the voltages among SMs. Through detailed modelling of the 3L-NPC converter, it is found that DC voltage imbalance is exhibited due to a right half-plane pole in the system. A conventional PI-based method is effective to counteract it. This relies on communications

through a central controller, and real-time DC link voltage data is sent to each SM. As the sum of control variables from all P0I controllers within SMs is zero, the DC voltage balancing control is decoupled from the power control. Due to this advantage, the PI-based method is adopted as the default controller for voltage balancing. However, there is always the risk to lose communication and, thereby, to exhibit stability issues.

Upon loss of communication, it is shown that an inverse-droop based method may take over the voltage balancing control, offering a good performance. Here, DC voltages are automatically balanced according to the droop characteristics of SMs. This alternative method ensures the continuous operation of the system at the expense of accuracy of output power. Although hybrid configurations featuring PI and inverse-droop based controllers in the same converter station can be adopted, all SMs should be switched to the droop control mode concurrently upon loss of communication at any SM to ensure good transient performance of the system.

The DC voltage balancing control schemes presented in this chapter have been verified with simulation results in MATLAB/ Simulink. The effectiveness of the presented control schemes has also been demonstrated using an MVDC experimental testbed with similar per unit values as those of the ANGLE-DC project.

Chapter 5

Decentralized Control for Multi-terminal Cascaded 3L-NPC Converter Systems Considering Multiple Crossovers

This chapter investigates the multiple crossovers due to interactions between different converters in a three-terminal MVDC system. Suitable control methods are presented to eliminate multiple crossovers and meanwhile, to ensure the power flow accuracy and DC voltage balancing of each cascaded 3L-NPC converter.

5.1 Introduction

Applying cascaded 3L-NPC converters in a multi-terminal MVDC system requires consideration of both the DC voltage balance within individual converters and the interactions between different converter stations. Decentralized control using multiple droop characteristics is a promising approach for coordinated operation, but interactions between the stations may result in multiple crossovers that cause the system to deviate from the set-point and lead to power and voltage drifts. However, the mechanism behind these drifts caused by multiple crossovers in cascaded converters with multiple slopes based decentralized control has not been studied, and simultaneous consideration of DC voltage balance, multiple crossovers, and power control accuracy requires appropriate control strategies.

This chapter firstly revealed the mechanism behind the power and DC voltage drifts. It is found that the normal operating point is unstable in the condition of multiple crossovers. Secondly, a control scheme that seeks to guarantee the power control accuracy and DC voltage balancing and, concurrently to avoid the multiple crossovers, was presented. To achieve this, the droop gain is suitably selected considering both the DC voltage balancing performance and occurrence of multiple crossovers, with another secondary power compensator being used to guarantee the power flow accuracy. The presented control scheme has been verified in MATLAB/Simulink simulation and also experimentally validated in a three-terminal MVDC testbed integrated with cascaded 3L-NPC converters.

5.2 Decentralized Control with Multiple-slope Characteristics in Cascaded 3L-NPC Converters

5.2.1 Configuration of a Three-terminal MVDC System

In Figure 5.1, the renewable energies or electrical loads of the third terminal can be connected to the point-to-point MVDC link through a DC/DC or a DC/AC converter station (Station 3), which may work under DC current control mode. For example, a three-terminal simulation model was presented, where energy storage system (ESS) is incorporated in the system to improve the power quality, efficiency and reliability of the transmission system [104]. The ESS is installed at the VSC station on the mainland of North Wales. It provides a feasible solution to mitigate the intermittency and unpredictability of wind power. The other two cascaded 3L-

NPC converter stations work under droop control to regulate the DC link voltage. However, there are potential adverse interaction effects due to the coupling of different converter stations.

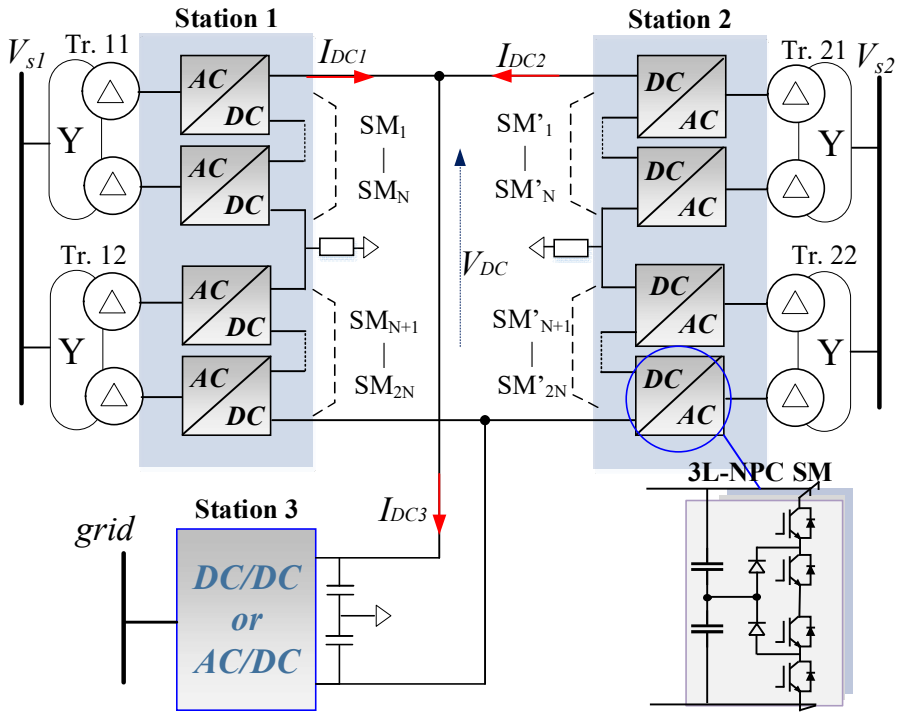


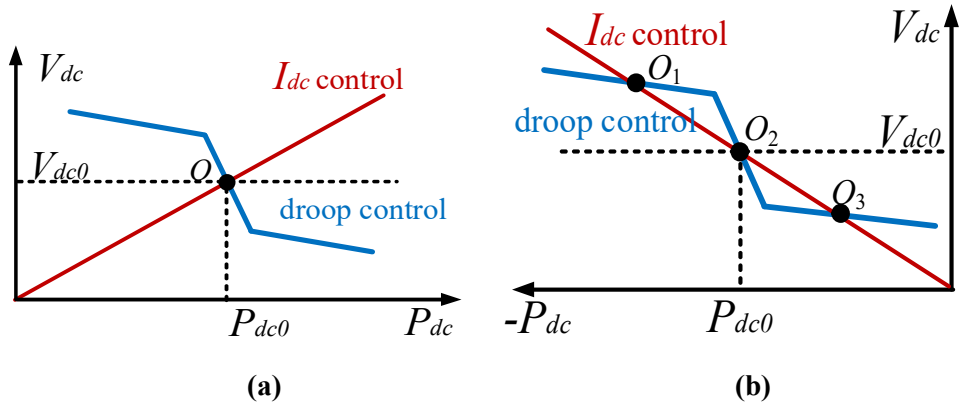
Figure 5.1. Cascaded 3L-NPC converter based three-terminal MVDC link.

5.2.2 Multiple crossovers due to interactions between Different Control Characteristics

The multiple crossovers may exist if the Station 3 adopts the constant I_{dc} control while the cascaded 3L-NPC converter stations (Station 1 and 2) adopt the $P-V_{dc}$ control. This control scheme is one of typical options in the multi-terminal conditions, where a part of converters adopt droop control to concurrently participate in the DC voltage regulation and the remaining converters that are connected to the renewable energies are operated at the current source mode [69]. The interactions have been displayed in Figure 5.2, where Station 1,2 and 3 are illustrated. The blue solid line represents the droop curve of Station 1 and 2, while the red solid line represents the curve of Station 3. It can be seen in Figure 5.2(a) that there is no interaction between I_{dc} and $P-V_{dc}$ control in the positive power flow (the positive power and current of the three converter stations are defined by the red arrow directions in Figure 5.1).

However, multiple crossovers may exist in the reverse direction of power flow, which indicates the occurrence of the multiple crossovers. As seen in Figure 5.2(b), there are three intersection

points of the two curves, denoted as O_1, O_2 and O_3. The adverse impacts caused by the multiple crossovers can be the deviations of the voltage and power from the desired operating points, thus deteriorating the performance of system or even making the system unstable due to the large deviations of voltage and power.



(a) **(b)**

Figure 5.2. Multiple crossovers caused by different control characteristics. (a) Positive power flow condition. (b) Negative power flow condition.

As seen in Figure 5.2, the larger the droop gain is, the more accurate the power control can be achieved. However, it is also shown that the droop gain should be decreased to avoid multiple crossovers. In addition, as discussed in Chapter 4, the droop slope is also associated with the and DC voltage imbalance. In Figure 5.2, the smaller the droop gain is, the closer to the voltage source characteristics the converter is, and thus the better DC voltage performance. Therefore, only by optimizing the droop gain cannot balance the three aspects (i.e., DC voltage balancing, power flow accuracy and multiple crossovers), and suitable control methods are required.

5.2.3 Analysis of Power and Voltage drifts in Multiple Crossovers

The mechanism of the power and voltage drifts due to the multiple crossovers is given in this Section. As can be seen in Figure 5.2, multiple crossovers are caused by the interaction between I_{dc} and $P-V_{dc}$ droop control. There are three intersection points (O_1, O_2 and O_3), so the operating point is likely to oscillate between the intersections. However, through the simulation and experimental studies in the previous work [69], the operating points will be located at one point (e.g., either O_1 or O_3) at steady-state. This means that O_2 is an unstable point. The mechanism behind this phenomenon has not been given so far.

To study this phenomenon, two cases are discussed, regarding the changes of the DC current and DC voltage, respectively. These changes are caused by either changes of given references

or disturbances due to the environmental factors, circuit components, or external factors. Figure 5.3(a) shows the shift of the operating point when the system is subjected to a DC current change, while Figure 5.3(b) shows the case under a DC voltage change. Assume the original operating points of Station 1, 2 and 3 are O_2 in Figure 5.3.

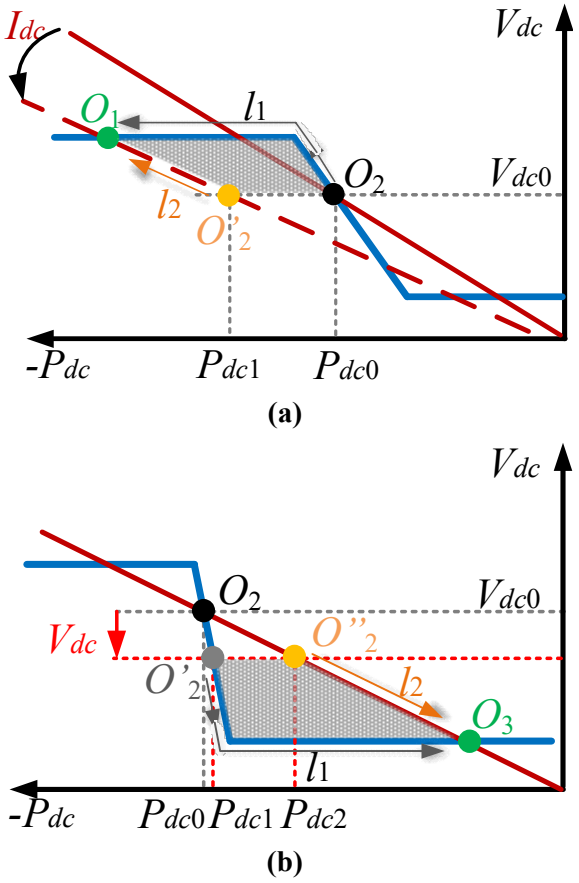


Figure 5.3. Power and voltage drifts under a disturbance. (a) The case under a DC current disturbance. (b) The case under a DC voltage disturbance.

In Figure 5.3(a), the DC current is slightly increased in Station 3 (the DC current curve is changed from the red solid line to the red dashed line). Following the DC current change, the operating point of the Station 3 fitted with constant current control jumps from the original point O_2 to a new point O_2'. The operating point of Station 1 with $P{-}V_{dc}$ control is maintained at O_2 in this case. As it can be seen, the power at O_2' is P_{dc1}, which has a greater absolute value than the power P_{dc0} at O_2. This means that the AC power absorbed by the Station 3 is larger than the power output from DC to AC side in Station 1. According to the power balance relationship in (5-1), it is obtained that the DC link capacitor is charged in this case. Then, the DC voltage is increased. The operating point of Station 3 moves in the direction of the line arrow $\overrightarrow{l_2}$, while the operating points of Station 1 in the direction of the line arrow $\overrightarrow{l_1}$. The

absorbed power remains lager than the output power until operating points reaching at O_1. Hence, a new stable operating condition is achieved at O_1.

$$C_{dc} v_{dc} \frac{dv_{dc}}{dt} = \left|P_{drp,1}\right| - \left|P_{i_{dc},3}\right| \quad (5\text{-}1)$$

where C_{dc} is the equivalent DC link capacitance, $P_{drp,1}$ is the power of Station 1 and $P_{i_{dc},3}$ is the power of Station 3.

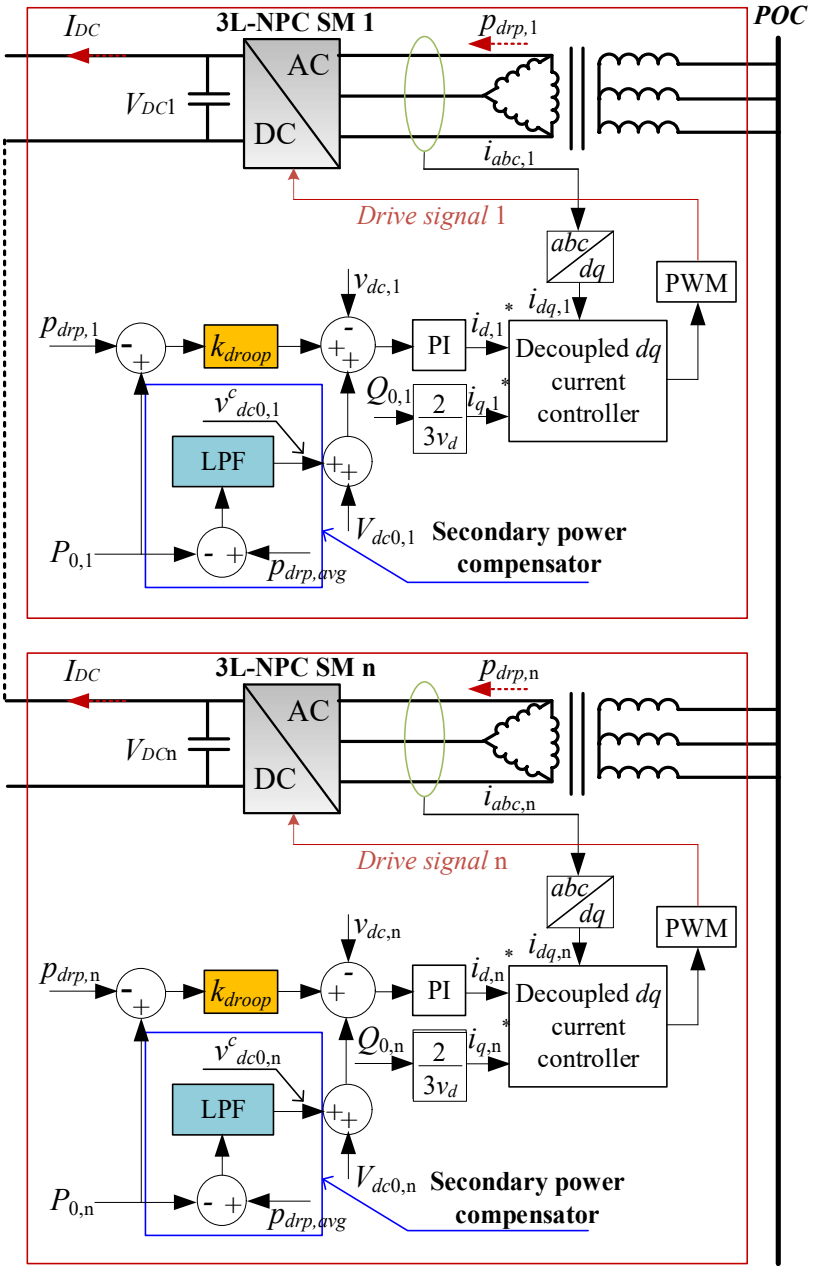
In Figure 5.3(b), the DC voltage slightly changes from the original point (the DC voltage drops from the grey dashed horizontal line to the red dashed horizontal line). Following the DC voltage change, the operating point of Station 1 jumps from the O_2 to a new point O_2', while the operating point of Station 3 jumps to O_2''. As $\left|P_{drp,1}\right| < \left|P_{i_{dc},3}\right|$, the DC link capacitor is discharged based on (5-1) and the DC voltage will be decreased. Then, the operating point of Station 3 moves in the direction of $\overrightarrow{l_2}$, while the operating points of Station 1 in the direction of $\overrightarrow{l_1}$. The absorbed power remains lower than the output power until operating points reaching at O_3. Thus, the new stable point will be located at the position of O_3. Through the analysis in Figure 5.3, it is obtained that the operating point O_2 is unstable when the multiple crossing occurs. It may shift to the O_1 or O_3 depending on the disturbance. The adverse effects are the voltage and power drifts which need to be addressed.

5.3 Presented Decentralized Control Scheme

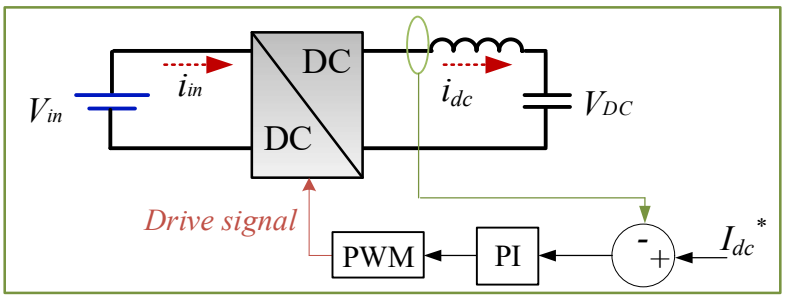
5.3.1 Decentralized Control Schematic

To improve the performance of DC voltage balancing and power control accuracy, and concurrently to mitigate the adverse interactions, an improved control method is presented, as seen in Figure 5.4.

For the cascaded 3L-NPC converter station in Figure 5.4(a), predetermined given references are dispatched by a high-level controller which is not shown in the Figure. Each SM controller works at the $P_i - V_{dci}$ droop control mode, so the external characteristic of the converter station is also exhibited as the droop control. A droop gain k_{droop} is used in the $P_i - V_{dci}$ droop controller. The normal operating points of each SM are $P_{0,i}$ and $V_{dc\ ,i}$. Output signals from the droop controller are the current references which are forwarded to the current controller performed at the *dq* frame. A PLL is used for grid frequency synchronization.



(a)



(b)

Figure 5.4. The decentralized control schematic of the system. (a) Droop control for C3L-NPC converters. (b) DC current control for DC/DC converters.

The constant current control for the current-controlled converter in Station 3 is depicted in Figure 5.4(b). As can be seen, a closed-loop current controller is used to control the inductor current to trace the given reference. As the kdroop2 in the narrow band is the cause behind the multiple crossovers, the optimal design for kdroop2 is particularly presented in this section. The kdroop1 and kdroop3 adopt a normal droop setting with a 5% slope [105]. It is noted that droop parameter in Figure 5.4 only stands for kdroop2 while kdroop1 and kdroop3 are omitted for simplicity.

5.3.2 Droop Gain Selection

1) Droop gain selection considering the multiple crossovers: As can be seen in Figure 5.3, the slope of droop curve in the narrow band should be less than the DC current to avoid the intersections.

The conclusion can be extended to multi-terminal conditions, assuming that there are *m* stations with droop control and *h* stations with DC current control. According to the power balance, there is:

$$\sum_{i=1}^{m} P_{drp,i} = \sum_{j=1}^{h} P_{i_{dc},j} \tag{5-2}$$

where $P_{drp,i}$ and $P_{i_{dc},j}$ are the power processed by the converter stations with droop control and DC current control, respectively. $P_{drp,i}$ and $P_{i_{dc},j}$ are represented as:

$$P_{drp,i} = \frac{-1}{k_{droop}}\left(v_{dc,i} - v_{dc,i0}\right) + P_{i0} \tag{5-3}$$

$$P_{i_{dc},j} = v_{dc,j} i_{dc,j} \tag{5-4}$$

Substitute (5-3) and (5-4) into (5-2) and then take the derivative of (5-2) with respect to v_{dc}, we can obtain:

$$\sum_{i=1}^{m} \frac{-1}{k_{droop}} = \sum_{j=1}^{l} i_{dc,j} \tag{5-5}$$

Thus, to avoid the multiple crossovers, k_{droop} should be selected as $k_{droop} < \frac{m}{\left|\sum_{j=1}^{l} i_{dc,j}\right|}$.

2) Droop gain selection considering the DC voltage balancing: The selection of k_{droop} should also consider the voltage balancing performance, otherwise the system may become unstable. To select a suitable k_{droop}, the system model including the main circuits and control parts is developed. It is assumed that all SMs have identical component parameters and that slight differences due to manufacturing tolerances are omitted. The total power/voltage and the

individual DC voltage can be independently controlled for an input-series-output-parallel converter. Thus, a single SM is chosen for tuning the droop gain. The state-space representation of the i^{th} SM considering the inner current control loop is:

$$\frac{d}{dt}\begin{bmatrix}\Delta x_{id\_I}\\ \Delta x_{iq\_I}\\ \Delta i_{di}\\ \Delta i_{qi}\\ \Delta v_{dci}\end{bmatrix} = \mathbf{A}\begin{bmatrix}\Delta x_{id\_I}\\ \Delta x_{iq\_I}\\ \Delta i_{di}\\ \Delta i_{qi}\\ \Delta v_{dci}\end{bmatrix} + \mathbf{B}\boldsymbol{\lambda}\begin{bmatrix}\Delta i_{di}^{*}\\ \Delta i_{qi}^{*}\\ \Delta i_{dc}\end{bmatrix} \tag{5-6}$$

The detailed information of matrices A and B is given in [12]. $\boldsymbol{\lambda} = \mathrm{diag}\left(\frac{3V_s}{2} \quad \frac{3V_s}{2} \quad 1\right)$ is a diagonal matrix, where V_s is the RMS value of grid voltage.

The transfer function of Δi_{di}^{*} to Δv_{dci} is given as

$$\Delta v_{dci} = \underbrace{[\mathbf{C_1}(\boldsymbol{s}\mathbf{I}-\mathbf{A})^{-1}\mathbf{B}']}_{\boldsymbol{G_1(s)}}\Delta i_{di}^{*} = G_1(s)\Delta i_{di}^{*} \tag{5-7}$$

where $\mathbf{C_1} = [0 \quad 0 \quad 0 \quad 0 \quad 1]$. $\mathbf{B}'$ has a dimension of 5×1, representing the first column vector of $\mathbf{B\lambda}$. With use of the droop controller, we can obtain

$$\begin{aligned}\Delta i_{di}^{*} &= G_{PI}(s)\left(\Delta v_{dc,i}^{*} - \Delta v_{dc,i}\right)\\ &= G_{PI}(s)\left(-k_{droop}\left(\Delta p_{drp,i} - \Delta p_{i0}\right) + \Delta v_{dc,i0} - \Delta v_{dc,i}\right)\end{aligned} \tag{5-8}$$

$$\Delta p_{drp,i} = \frac{3V_s}{2}\Delta i_{di} \tag{5-9}$$

$$\Delta i_{di} = \underbrace{[\mathbf{C_2}(\boldsymbol{s}\mathbf{I}-\mathbf{A})^{-1}\mathbf{B}']}_{\boldsymbol{G_2(s)}}\Delta i_{di}^{*} = G_2(s)\Delta i_{di}^{*} \tag{5-10}$$

where $\mathbf{C_2} = [0 \quad 0 \quad 1 \quad 0 \quad 0]$. $\Delta v_{dc,i0} = \frac{\Delta v_{dc0}}{2N}$ and $\Delta p_{i0} = \frac{\Delta p_0}{2N}$ are selected to achieve the DC voltage and power balancing. $G_{PI}(s) = \frac{K_{pvb}s + K_{ivb}}{s}$ is the outer loop PI controller. Combining (5-7)−(5-10), the closed-loop transfer function of $\Delta v_{dc,i0}$ to Δv_{dci} for the i^{th} SM is obtained as

$$G_{vb}(s) = \frac{\Delta v_{dci}}{\Delta v_{dc,i0}} = \frac{G_{PI}(s)G_1(s)}{1+1.5k_{droop}V_sG_{PI}(s)G_2(s)+G_{PI}(s)G_1(s)} \tag{5-11}$$

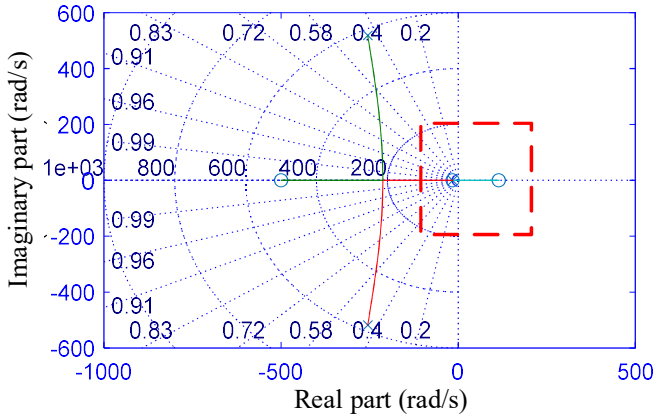
The open-loop transfer function corresponding to (5-11) is

$$G_{vb\_open}(s) = \frac{G_{PI}(s)G_1(s)}{1+1.5k_{droop}V_sG_{PI}(s)G_2(s)} \tag{5-12}$$

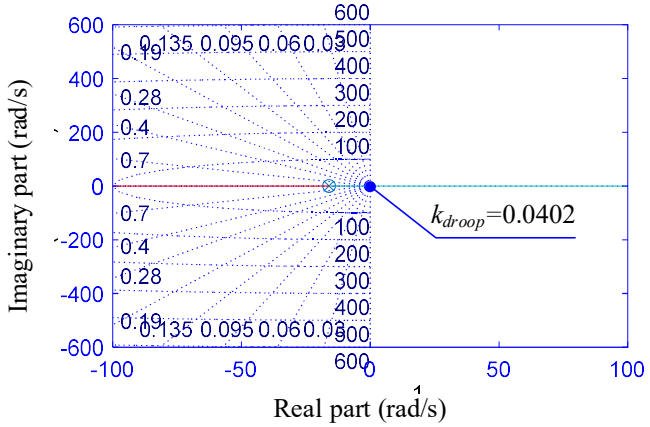
When k_{droop} is increased, the closed-loop poles' trajectories of $G_{vb}(s)$ is shown in Figure 5.5. The main circuit and controller parameters excluding the droop gain are same to Chapter 4. Figure 5.5(a) shows the closed-loop pole trajectories under positive power flow while Figure 5.5(b) shows the zoom-in view where the threshold of the k_{droop} that makes system stable is displayed. From Figure 5.5, it can be seen that one dominant pole will move to the right half s-plane (unstable area) when the k_{droop} increases. The threshold value of k_{droop} that makes the system stable is 0.0402. Therefore, considering both the multiple crossovers and DC voltage balancing performance, the k_{droop} should be selected as

$$k_{droop} = Min\left(\frac{m}{\left|\sum_{j=1}^{l} i_{dc,j}\right|}, \quad K_{vb,opt}\right) \tag{5-13}$$

Figure 5.6 shows the open-loop Bode diagram of (5-13) under k_{droop} =0.023. The obtained bandwidth and phase margin of the open-loop system are 200 rad/s and 55° which are acceptable.



(a)



(b)

Figure 5.5. Closed-loop poles' trajectories in equation (5-10) as k_{droop} increases. (a) Dominant poles' trajectories. (b) Zoom-in view of dominant poles' trajectories.

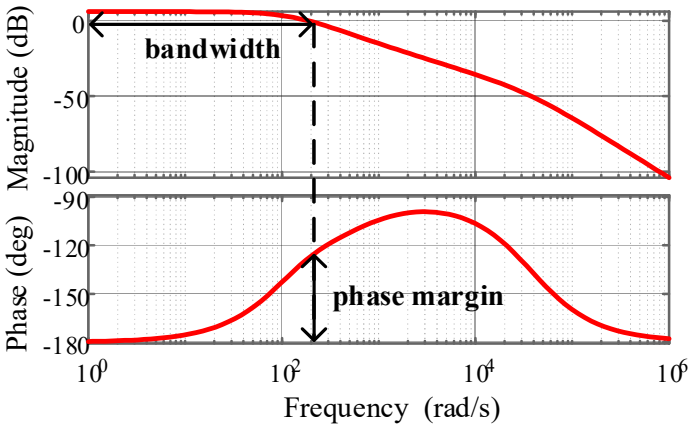


Figure 5.6. Open-loop Bode diagram of equation (5-10) when k_{droop} =0.023.

5.3.3 Design of Secondary Power Compensator

Since a smaller droop gain is used to avoid multiple crossovers, a potential large power offset may occur under the dynamic change of DC current. This reduces the accuracy of power control and sacrifices the advantages of using the narrow band in the piecewise droop control. A secondary power compensator is used to compensate the potential large power offset due to the smooth droop curve. The power reference is superposed with a compensation variable which aims to eliminate the power flow offset (see the blue rectangular in Figure 5.4). This compensation variable is obtained from a low-pass filter (LPF) and given as

$$\Delta v_{dc0,i}^{c} = K_{comp} \underbrace{\frac{1}{\tau s+1}}_{\text{LPF}} \left(\Delta p_{drp_{avg}} - \Delta p_{i0}\right) \tag{5-14}$$

$$\Delta p_{drp\_avg} = \frac{\sum_{i=1}^{n} \Delta p_{drp,i}}{n} \tag{5-15}$$

where K_{comp} is the proportional gain of the compensator, τ is the time constant of the LPF, $\Delta v_{dc0,i}^{c}$ is the compensating voltage reference, and p_{drp_avg} is the average power of all SMs. After adding the compensator, the Δi_{di}^{*} in (5-8) is expressed as

$$\Delta i_{di}^{*} = G_{PI}(s)\left(\Delta v_{dc,i}^{*} - \Delta v_{dc,i}\right) = G_{PI}(s)\left(-k_{droop}\left(\Delta p_{drp,i} - \Delta p_{i0}\right) + \Delta v_{dc,i0} + \frac{K_{comp}}{\tau s+1}\left(\Delta p_{dr\ \ avg} - \Delta p_{i0}\right) - \Delta v_{dc,i}\right) \tag{5-16}$$

Combining (5-7), (5-9), (5-10) and (5-16), we can obtain the sensitivity of $\Delta p_{drp,i}$ to $\Delta v_{dc,i}$ by setting Δp_{i0} and $\Delta v_{dc,i0}$ to zero. The sensitivity of $\Delta p_{drp,i}$ to $\Delta v_{dc,i}$ in each SM is shown in (5-17). Adding all equations in (5-17) yields the sensitivity of the total output power (Δp_{drp}) to the DC link voltage (Δv_{dc}) which is shown in (5-18).

$$\begin{cases} \Delta v_{dc,1} = \frac{-G_1(s)G_{PI}(s)}{1+G_1(s)G_{PI}(s)}\left(k_{droop}\Delta p_{drp,1} - \frac{K_{comp}}{\tau s+1}\Delta p_{drp\_avg}\right) \\ \Delta v_{dc,2} = \frac{-G_1(s)G_{PI}(s)}{1+G_1(s)G_{PI}(s)}\left(k_{droop}\Delta p_{drp,2} - \frac{K_{comp}}{\tau s+1}\Delta p_{drp\_avg}\right) \\ \Delta v_{dc,n} = \frac{-G_1(s)G_{PI}(s)}{1+G_1(s)G_{PI}(s)}\left(k_{droop}\Delta p_{drp,n} - \frac{K_{comp}}{\tau s+1}\Delta p_{drp\_avg}\right) \end{cases} \quad (5\text{-}17)$$

$$\Delta v_{dc} = \frac{-G_1(s)G_{PI}(s)}{1+G_1(s)G_{PI}(s)}\sum_{i=1}^{n}\left(k_{droop}\Delta p_{drp,1} - \frac{K_{comp}}{\tau s+1}\Delta p_{drp\_avg}\right)$$

$$= \frac{-G_1(s)G_{PI}(s)}{1+G_1(s)G_{PI}(s)}\left(k_{droop} - \frac{K_{comp}}{\tau s+1}\right)\Delta p_{drp} \quad (5\text{-}18)$$

In (5-18), due to the low-pass filtering effect of $\frac{K_{comp}}{\tau s+1}$, the power compensator has little impact on the sensitivity of the power to DC voltage and hence, the droop characteristic is still determined by k_{droop}. To decouple the dynamics between the secondary power compensating loop and the droop control loop, the LPF should be properly designed to ensure that the response speed of the secondary power compensating loop should be 5−10 times slower than that of the droop control loop. The K_{comp} can be selected by studying the transfer function of the secondary power compensating loop. Based on (5-7), (5-9), (5-10) and (5-16), the relationship between Δp_{i0} and $\Delta p_{drp,i}$ is given in (5-19). Adding all equations in (5-19) yields (5-20).

$$\begin{cases} \Delta p_{drp,1} = \frac{3V_sG_{PI}(s)G_2(s)}{2\left(1+G_1(s)G_{PI}(s)\right)+3k_{droop}V_sG_{PI}(s)G_2(s)}\left(\Delta p_{10}\left(k_{droop}+\frac{K_{comp}}{\tau s+1}\right)+\frac{K_{comp}}{\tau s+1}\Delta p_{drp\_avg}\right) \\ \Delta p_{drp,2} = \frac{3V_sG_{PI}(s)G_2(s)}{2\left(1+G_1(s)G_{PI}(s)\right)+3k_{droop}V_sG_{PI}(s)G_2(s)}\left(\Delta p_{20}\left(k_{droop}+\frac{K_{comp}}{\tau s+1}\right)+\frac{K_{comp}}{\tau s+1}\Delta p_{drp\_avg}\right) \\ \Delta p_{drp,n} = \frac{3V_sG_{PI}(s)G_2(s)}{2\left(1+G_1(s)G_{PI}(s)\right)+3k_{droop}V_sG_{PI}(s)G_2(s)}\left(\Delta p_{n0}\left(k_{droop}+\frac{K_{comp}}{\tau s+1}\right)+\frac{K_{comp}}{\tau s+1}\Delta p_{drp\_avg}\right) \end{cases} \quad (5\text{-}19)$$

$$\sum_{i=1}^{n}\Delta p_{drp,i} = \frac{3V_sG_{PI}(s)G_2(s)}{2\left(1+G_1(s)G_{PI}(s)\right)+3k_{droop}V_sG_{PI}(s)G_2(s)}\left(\sum_{i=1}^{n}\Delta p_{i0}\left(k_{droop}+\frac{K_{comp}}{\tau s+1}\right)+ n\frac{K_{comp}}{\tau s+1}\Delta p_{drp\_avg}\right) \quad (5\text{-}20)$$

By rearranging (5-20), the closed-loop transfer function of Δp_0 to Δp_{drp} is obtained as

$$G_P(s) = \frac{\Delta p_{drp}}{\Delta p_0} = \frac{3V_sG_{PI}(s)G_2(s)\left(k_{droop}-\frac{K_{comp}}{\tau s+1}\right)}{2\left(1+G_1(s)G_{PI}(s)\right)+3V_sG_{PI}(s)G_2(s)\left(k_{droop}-\frac{K_{comp}}{\tau s+1}\right)} \quad (5\text{-}21)$$

The open-loop transfer function corresponding to (5-21) is

$$G_{vb\_open}(s) = \frac{3V_sG_{PI}(s)G_2(s)\left(k_{droop}-\frac{K_{comp}}{\tau s+1}\right)}{2\left(1+G_1(s)G_{PI}(s)\right)} \quad (5\text{-}22)$$

To decouple the dynamics between the secondary power compensating loop and the droop control loop, the response time of the secondary power compensating loop can be 5−10 times larger than that of the droop control loop. The closed-loop pole trajectory is shown in Figure 5.7.

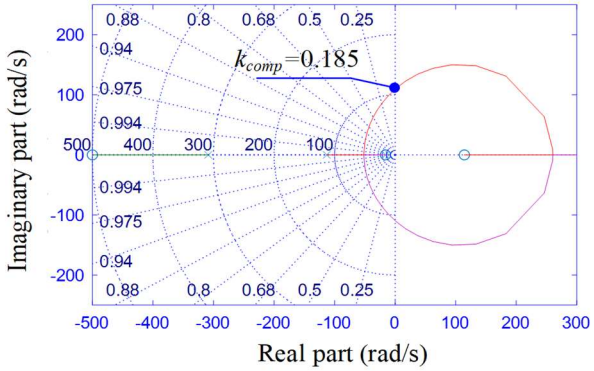
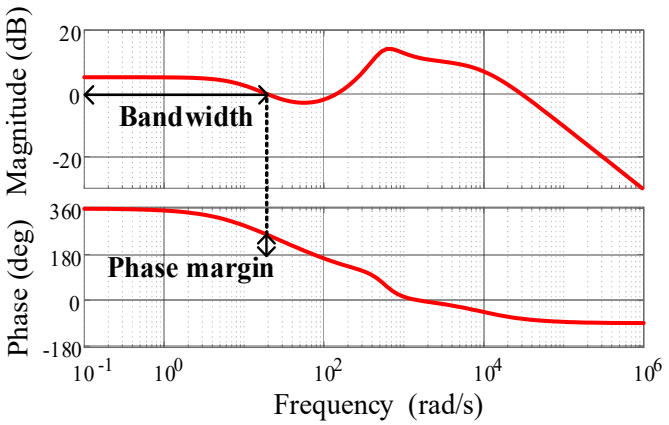
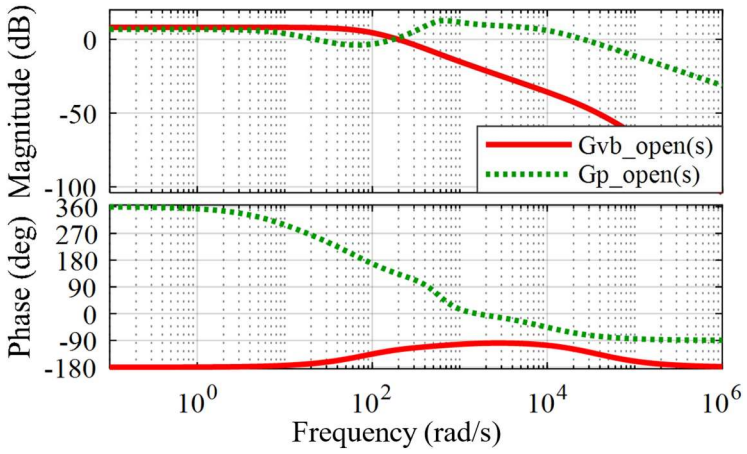


Figure 5.7. Closed-loop poles' trajectories in equation (5-18) as k_{comp} increases.



(a)



(b)

Figure 5.8. Open-loop Bode diagram. (a) Bode diagram of equation (5-18) with k_{comp} =0.085 and $\tau = 0.1$. (b) Comparison between $G_{vb\_open}(s)$ and $G_{P\_open}(s)$.

As can be seen in Figure 5.7, a pair of conjugate poles will move to the right half s-plane when k_{comp} is greater than 0.185. Thus the k_{comp} should be selected less than the upper bound.

To decouple the dynamics between the secondary power compensating loop and the droop control loop, the response speed of the secondary power compensating loop should be 5−10 times slower than that of the droop control loop. The open loop Bode diagram of the secondary power compensator ($G_{P\_open}(s)$) with k_{comp} =0.085 is shown in Figure 5.8. The cut-off frequency of $G_{P\_open}(s)$ is 20 rad/s, which has 1/10 times the bandwidth of the droop control loop (by comparing the red solid line and green dashed line in Figure 5.8(b)). Thus, the dynamics of the two control loops can be decoupled.

5.4 Simulation and Experimental Validation

5.4.1 Simulation Results

The simulation is conducted in MATLAB/Simulink for a three-terminal system, where two stations are based on the cascaded 3L-NPC converters, and the third terminal is a converter operated as a controllable current source (the configuration is same as the Figure 5.1). Both cascaded 3L-NPC converter stations work under $P - V_{dc}$ droop control while the converter in station 3 under DC current control. The parameters of the main circuits and voltage and current PI controllers are the same as [90]. The power and voltage references of the droop controller for all the four case studies (Figures 5.9 to 5.12) are $P_0 = 10$ kW and V_{dc0}=360 V, respectively. The DC current reference for the DC/AC converter is set as I_{dc0}=55 A.

Figures 5.9−5.12 show the DC current output from the converter station 3 and the DC voltage and power of one of the cascaded 3L-NPC converters. Figure 5.9 shows the case when k_{droop} is 0.06 which is greater than the threshold. In Figure 5.9(a), the DC current can track the reference. However, due to the multiple crossovers, the operating points will deviate from the desired operating points. This phenomenon is reflected in the Figure 5.9(b) and (c). The DC voltage will decrease to the minimum voltage according to the droop curve (the minimum voltage is set as 280 V).

Figure 5.10 shows the case when k_{droop} is properly selected as k_{droop}=0.023. As seen in Figure 5.10(b) and (c), by contrast to Figure 5.9, the operating points are nearly same to the

references. Thus, the adverse multiple crossings have been eliminated. Also, the DC voltage across SMs is balanced well, as shown in Figure 5.10(d).

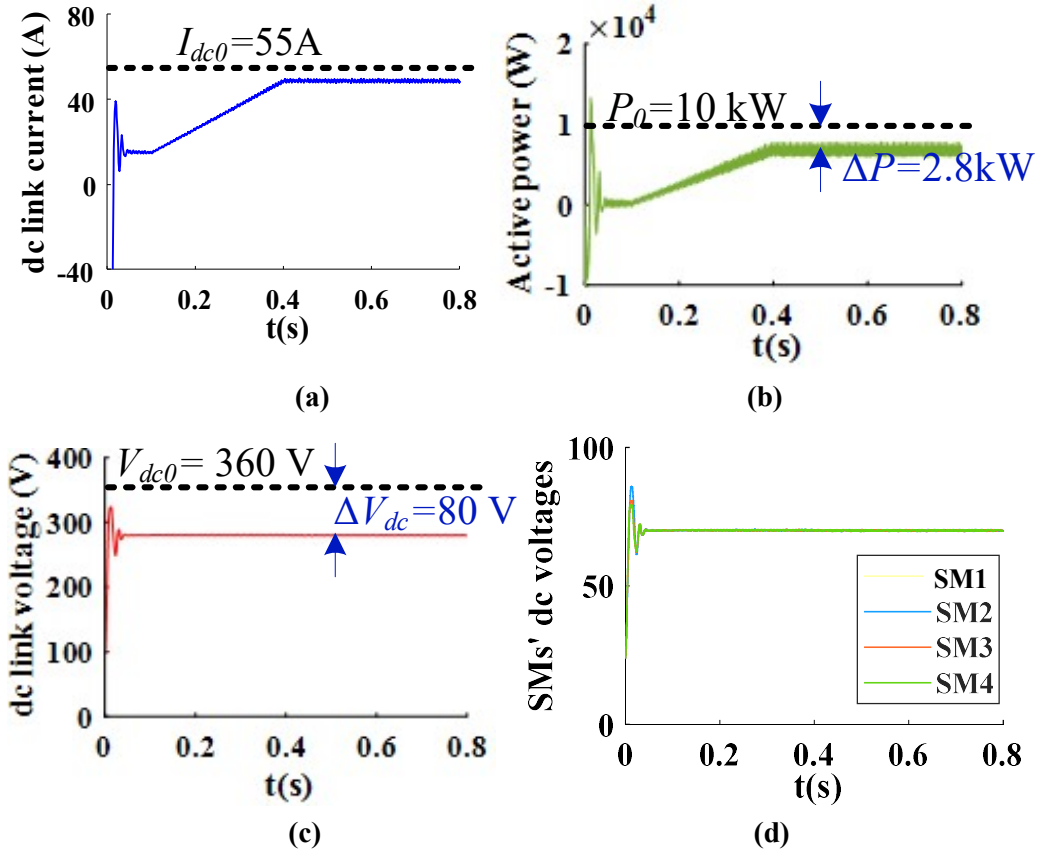


Figure 5.9. Multiple crossovers when k_{droop} is 0.06. (a) DC current. (b) total power. (c) DC link voltage. (d) SMs' DC voltages.

Figure 5.11 shows the impact of the change of the DC current on the voltage and power drift when the secondary compensating controller is not used. In Figure 5.11(a), the current reference of the converter station 3 has a slight change from 55 A to 40 A after 0.7s. Since a smaller k_{droop} is used, the cascaded 3L-NPC converter station is more sensitive to such a change of DC current due to the flat characteristic of the droop curve. As a consequence, a relatively large drift of power arises and the voltage decreases, as shown in Figure 5.11(b) and (c).

Figure 5.12 shows the improved performance after implementing the secondary compensating loop. As can be seen, although the DC current drops down, the power can be restored to the desired value by increasing the DC voltage (see Figure 5.12(c) and (d)). Thus, the secondary compensating loop is useful for the application where an accurate power control is required.

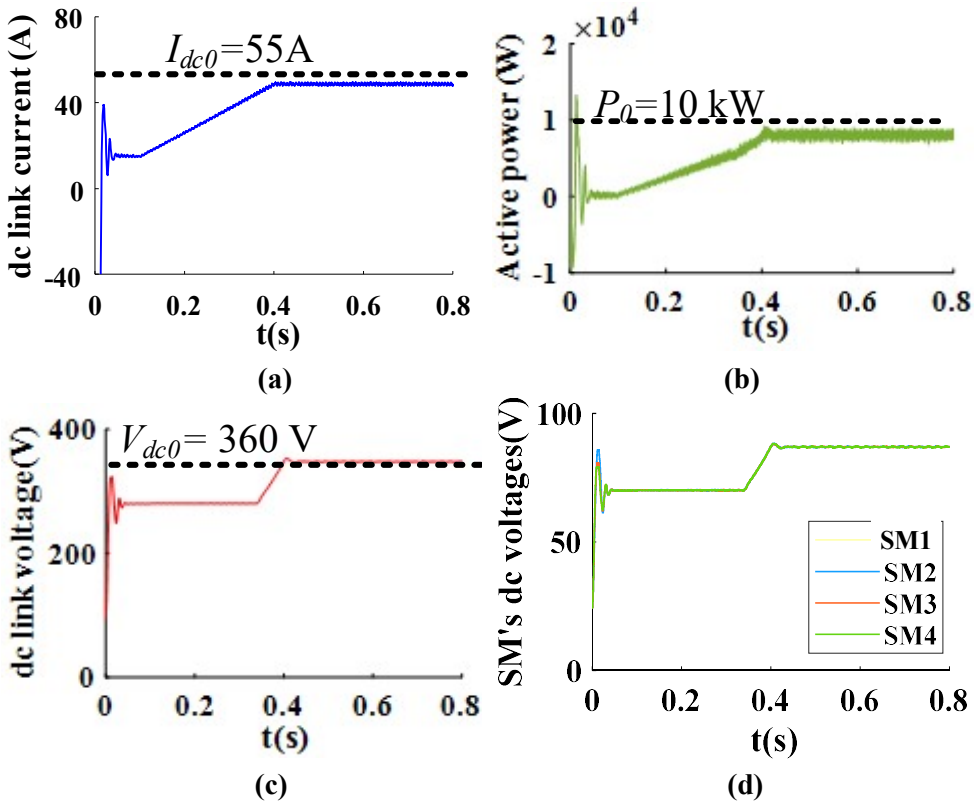


Figure 5.10. No multiple crossovers when k_{droop} is 0.023. (a) DC current. (b) total power. (c) DC link voltage. (d) SMs' DC voltages.

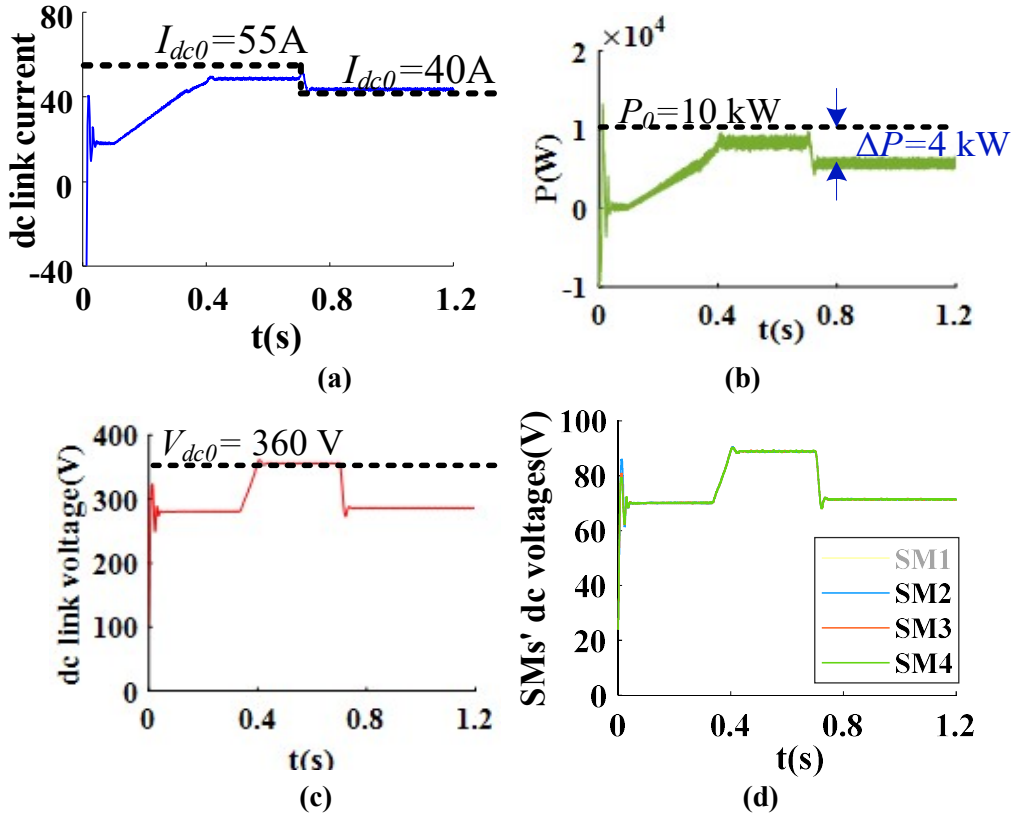


Figure 5.11. Power drift without using secondary power compensating controller. (a) DC current. (b) total power. (c) DC link voltage. (d) SMs' DC voltages.

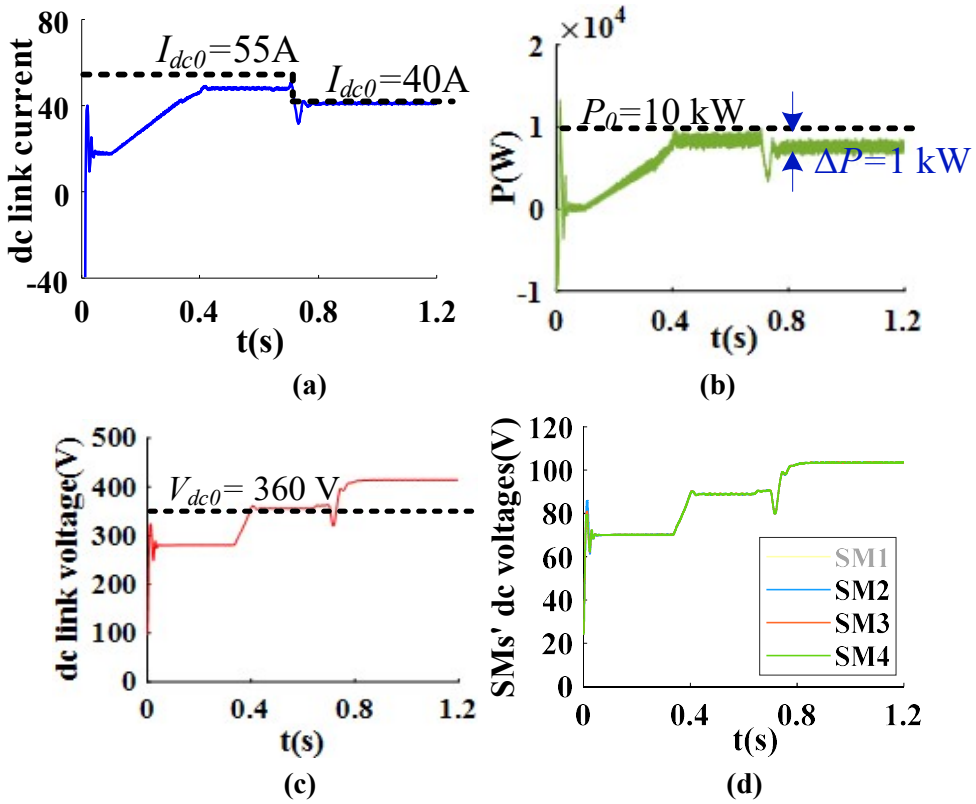


Figure 5.12. Improved power control accuracy with using secondary power compensating controller. (a) DC current. (b) total power. (c) DC link voltage. (d) SMs' DC voltages.

5.4.2 Experimental Results

The presented control schemes were experimentally validated using a three-terminal MVDC testbed consisting of two cascaded 3L-NPC converter stations and a DC power supply. The DC power supply is EA-PS 9200-25, which can provide 1.5 kW power.

For each cascaded 3L-NPC converter station, two 3L-NPC SMs were cascaded to build a 180 V DC link voltage, with each SM is operated at 90 V. The DC power supply is operated under current source mode to provide desired DC current. The hardware configuration of the system is shown in Figure 5.13. Since the operation conditions of the two cascaded 3L-NPC converters are identical, only one cascaded 3L-NPC converter is observed. Given that the power provided by the DC power supply is limited, the chosen k_{droop} is not strictly consistent with that in the simulation. According to (5-13) and [90], it is obtained that the higher the power is, the more likely the multiple crossovers and voltage imbalance are to arise. Therefore, the previous sub-chapters considered the selection of k_{droop} in the worst case (i.e., at maximum power) while in this experiment, the selection range of k_{droop} can be increased. Although the experiments are carried out at relatively low power, the presented scheme can still be verified.

Figure 5.13. Three-terminal MVDC configuration consisting of two cascaded 3L-NPC converter stations and a DC power supply.

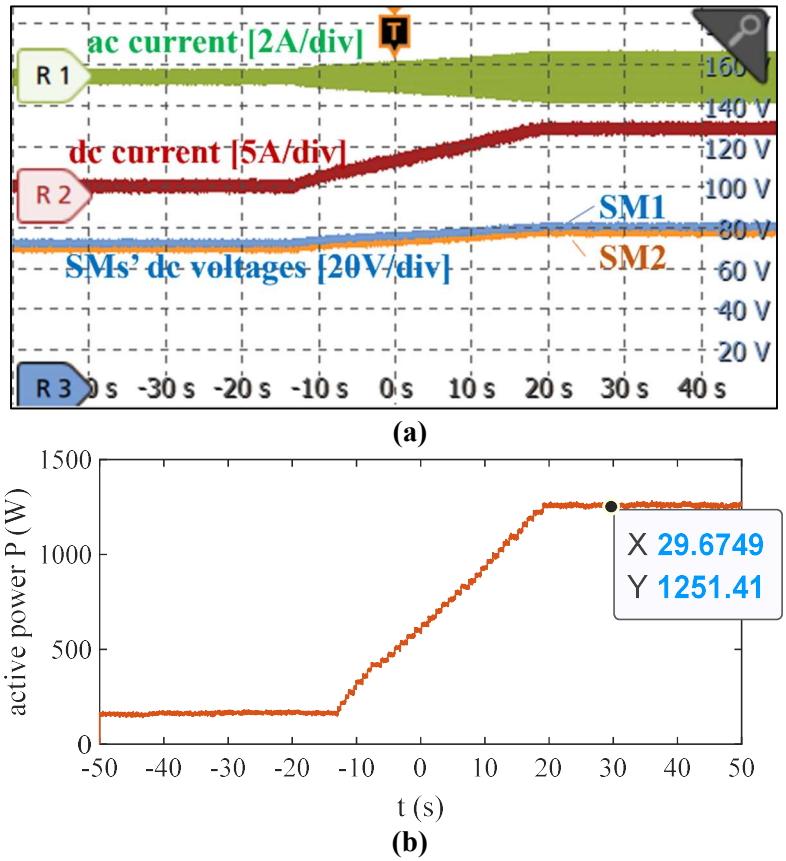
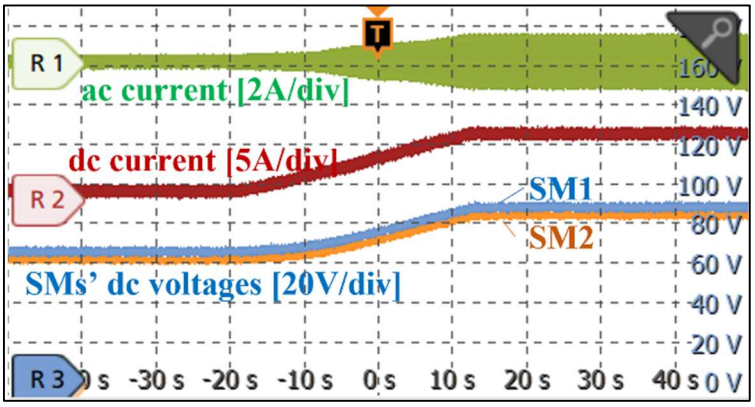


Figure 5.14. Waveforms when k_{droop} is set to 0. 36. (a) Currents and DC voltages. (b) Output power from DC power supply.

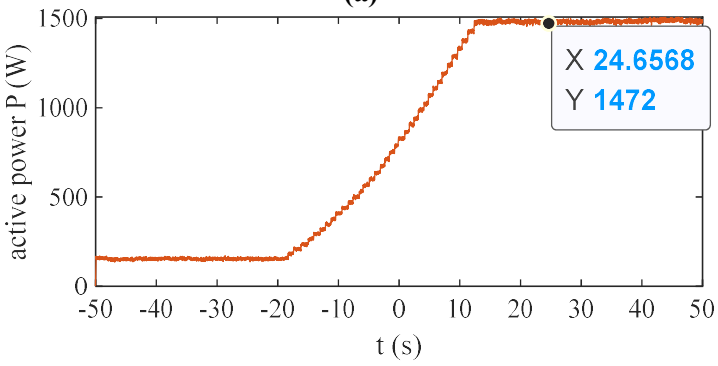
In Figure 5.14, the references of each cascaded 3L-NPC converter station are set as $P_0 =$ 750 W and V_{dc} =180 V, and the current of DC power supply is adjusted from 0 to around 8 A. As can be seen, multiple crossings arise when k_{droop} is 0.36 which is larger than the threshold

$\frac{2}{|i_{dc}|} = 0.25$. As shown in Figure 5.14(a), the DC voltage of each SM at steady-state is 80 V, which is 10 V less than the given voltage. In Figure 5.14(b), the steady-state power is around 1.25 kW, which is 0.25 kW less than the given value (the high-frequency ripples of the power have been filtered without influencing the steady-state performance).

The multiple crossings are avoided in Figure 5.15 when k_{droop} decreases to 0.072. As seen in Figure 5.15(a) and (b), the drifts of DC voltage and power are effectively mitigated and thus the desired operating point is achieved. Also, the SMs' DC voltages are well balanced.



(a)



(b)

Figure 5.15. Waveforms when k_{droop} is set to 0.072. (a) Currents and DC voltages. (b) Output power from DC power supply.

In Figure 5.16(a), the DC current changes from around 8 A to 7.2 A after time -20 s. Consequently, there is a 200 W power drift (see Figure 5.16(b)) due to such a change of DC current. To pursue an accurate power control performance, the secondary power compensating controller is implemented after time 16 s. The power quicky restores to the similar level of the original operating power. Thus, power accuracy is improved by about 13%. This is achieved by increasing the DC voltage. The A voltage limitation can be added to avoid the overvoltage according to the requirements of the real applications. From the perspective of power output

accuracy, the presented methods are qualified.

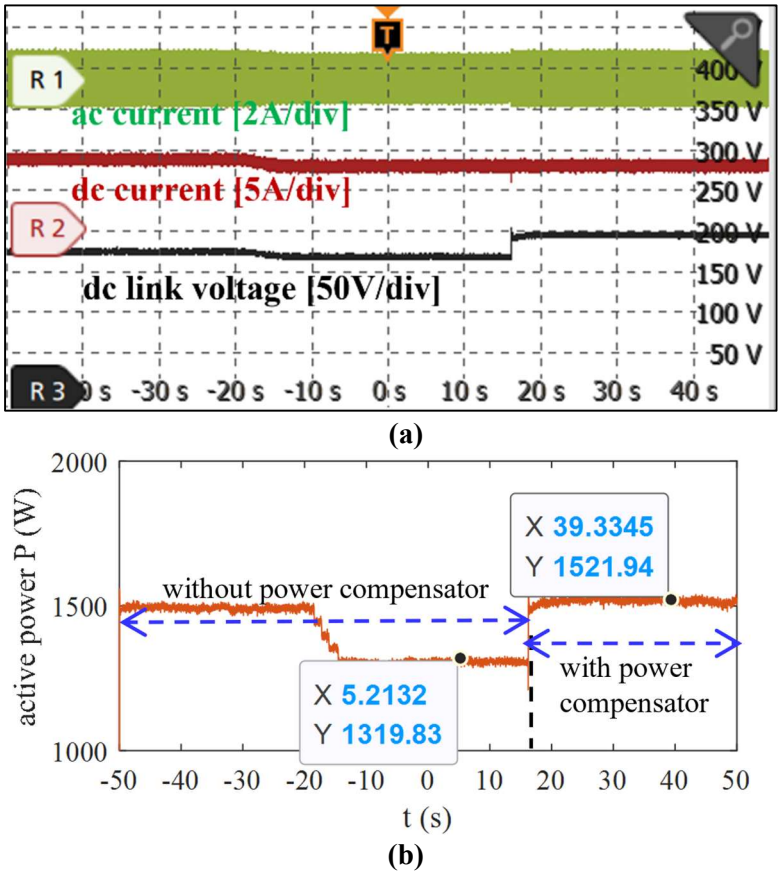


Figure 5.16. Waveforms under DC current change, with and without secondary power compensator. (a) Currents and DC voltage. (b) Output power from DC power supply.

5.5 Summary

This chapter focused on the multiple crossovers of multiple-slope based decentralized control in a cascaded 3L-NPC converter based three-terminal MVDC system. The voltage and power drifts caused by the multiple crossovers were first analysed. Then, a trade-off between the multiple crossovers, DC voltage balancing across SMs and the power control accuracy was well addressed by modifying the droop controller.

When cascaded 3L-NPC converter stations adopt the voltage−power droop control while another station the constant DC current control, the multiple crossovers may appear. Through analysis on the physical mechanism, the normal operating point is unstable, and may move away due to a disturbance. This leads to a large power and voltage drifts, which are not desired in practical applications.

Decreasing the droop gain is helpful for eliminating multiple crossovers. Also, the DC voltage balancing performance can be improved as well with using a smaller droop gain, since the converter is more like a voltage source so that DC voltage difference between SMs can be decreased. Thus, the droop gain should be properly selected to concurrently satisfy the performance of these two aspects. The small-signal analysis is used to design the droop gain. With the designed gain value, the system presented satisfactory performance regarding bandwidth and stable margin which are shown in the Bode diagram.

Although a small droop gain is helpful for the aforementioned two aspects, this is at the cost of decreasing the power control accuracy. This trade-off cannot be balanced by adjusting the droop gain only. To address this, a secondary power compensator is used to restore the power to the given reference. The response time of the secondary power compensator is 1/10 time of that of the droop controller. Thus, their dynamics are decoupled.

The theoretical analyses and presented control methods have been verified by both MATLAB simulation and experimental tests based on a 1.5 kW three-terminal laboratory-scale MVDC testbed.

Chapter 6

Active Thermal Sharing Control for Submodules of a Cascaded 3L-NPC Converter

This chapter presents the active thermal sharing control of the cascaded 3L-NPC converter to enhance the system reliability. This way, active and reactive power regulation is conducted according to the individual junction temperature of each SM.

6.1 Introduction

Although equal sharing of current and voltage stresses among SMs can be achieved by the DC voltage balancing control in previous chapters, the thermal stresses can be unequally shared due to the mismatched parameters of components (e.g. IGBTs) and partial cooling system failures. This may lead to different degradation of SMs and hence reduction of the system reliability. To address this challenge, in this chapter, an active thermal sharing controller is superposed on the voltage balancing controller as an outer control loop to adjust the DC voltage and power of each SM. By means of this method, the equal thermal sharing is achieved.

In this method, a PI-based thermal controller is embedded in each SM to adjust the active and reactive power. A high-level main controller is used to send the mean temperature of SMs as the reference to SM controllers and manage the thermal conditions of the system. Constrained by the minimum DC voltage of each SM, the thermal regulation range is limited. Hence, the thermal control capability which is dependent of the minimum DC voltage is discussed. Upon the thermal control capability of any SM reaching the limit, the temperature reference is changed to be the mean temperature of the rest SMs by the main controller. To facilitate the controller parameter design, a system model is presented in detail, followed by a gain tuning of the thermal PI controller based on the Bode plot. The presented control strategy is validated using a laboratory-scale MVDC testbed. It is shown that the junction temperature of SMs can be effectively balanced when cooling system failures occurring in a SM.

6.2 Active Thermal Sharing Control Method

6.2.1 Thermal Sharing Control Loop

The active thermal sharing control loop is enclosed by the green dashed block in Figure 6.1. The junction temperature reference T_j^* is calculated by the main controller and sent to each SM's thermal sharing control loop. T_j^* is the average junction temperature of all SMs. T_{ji} traces T_j^* through a closed loop, where T_{ji} is the junction temperature of the i^{th} SM. The error between T_j^* and T_{ji} is eliminated by two PI controllers, which generate compensating active and reactive power references. As the active power of each SM is proportional to its DC voltage, the d-axis variable $v_{dci,comp}^*$ is added as a compensation term to the DC voltage controller and, thus, to regulate active power. On the other hand, the q-axis variable $i_{qi,comp}^*$ is added as a

compensation term to the q-axis current control loop to regulate reactive power. Through this configuration, thermal stress is equally distributed for all SMs. Additionally, since the sum of outputs from the thermal PI controllers of all SMs equals zero, the thermal control loop is decoupled with the power control loop. This implies that even though the thermal controllers regulate power changes in individual SMs, the total change across all SMs remains zero. The detailed analysis is given in Section 6.4.

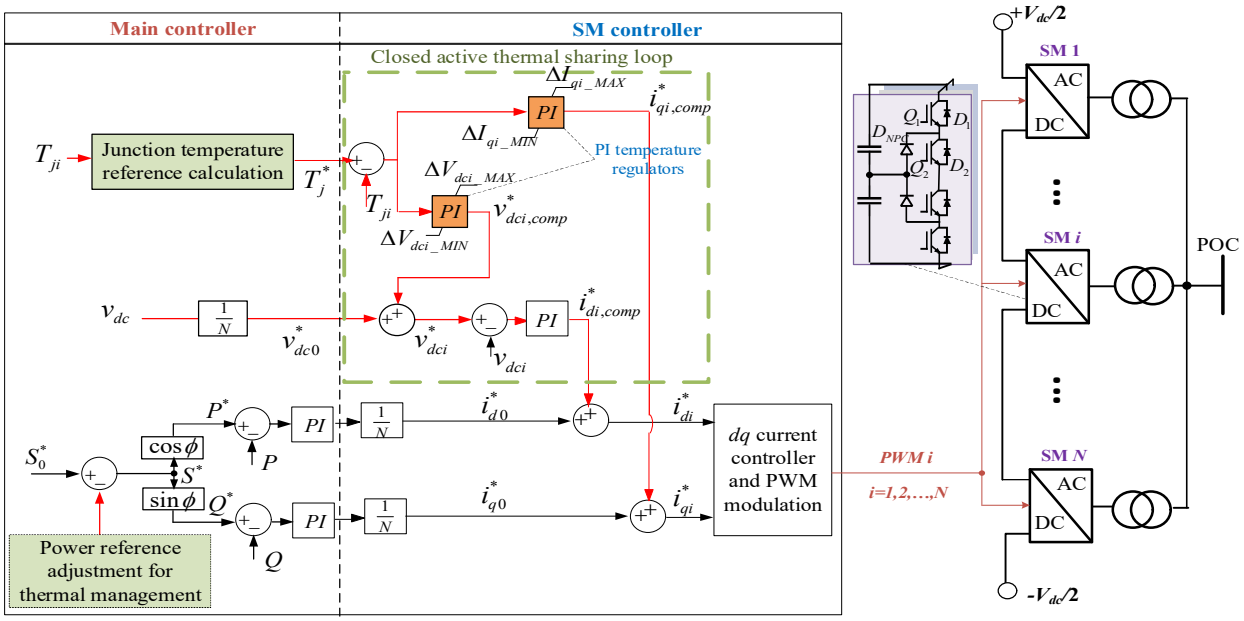


Figure 6.1. Thermal sharing control schematic of the MVDC system with *N* cascaded SMs.

Juncture temperature is determined by the power losses. The power losses at different power factors are shown in Figure 6.2, which is obtained through the simulation conducted in PLECS using the IGBT module F3L75R07W2E3_B11. The parameters of this IGBT module at 25℃ are given in Table 6.1. It can be seen that the T_1 and T_2 are the devices with high power losses at the unit power factor with positive active power flow (the power flows from the DC to AC side), while the D_1 and D_2 become the dominant devices at unit power factor with negative active power flow (the power flows from the AC to DC side). When power factor is zero, the D_{npc} and T_2 have the highest losses.

The lifetime of a converter is restricted by the most severely heated components. Thus, T_{ji} may be selected as the junction temperature of the most heated component of the i^{th} SM. However, as each SM is formed by 30 individual devices (4 IGBTs and 6 diodes per phase), it would take significant time to calculate all junction temperatures to identify the device exhibiting the

highest temperature. For simplicity, a three-phase balanced condition and no drift in the neutral-point voltage are assumed. In this case, the devices of one bridge arm only (Q_1, Q_2, D_1, D_2 and D_{NPC} in Figure 6.1) are sufficient to represent the thermal condition of a SM due to the symmetrical structure of the converter. Thus, T_{ji} should be selected as the highest temperature:

$$T_{ji}=\max\{T_{Q_1 i}, T_{Q_2 i}, T_{D_1 i}, T_{D_2 i}, T_{D_{NPC} i}\} \tag{5-1}$$

where $T_{Q_1 i}$, $T_{Q_2 i}$, $T_{D_1 i}$, $T_{D_2 i}$and $T_{D_{NPC} i}$ are the junction temperatures of the five devices.

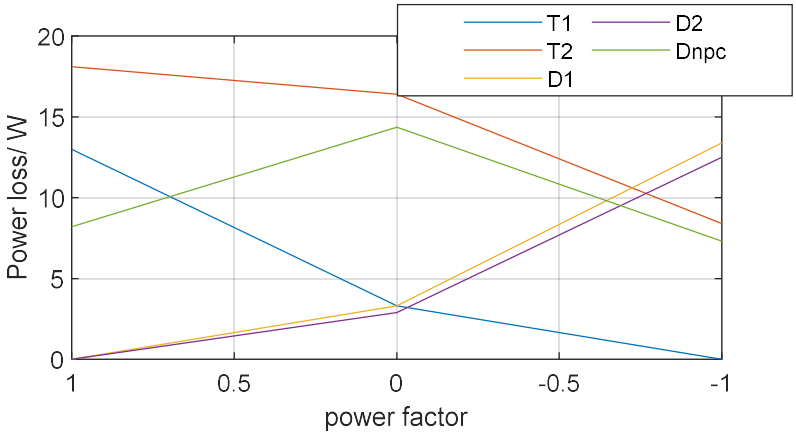


Figure 6.2. Power loss distribution at different power factors.

TABLE 6.1. PARAMETER OF IGBT MODULE F3L75R07W2E3_B11.

IGBT	Value	Diode	Value
V_{ce0}	0.772 V	V_{f0}	0.83 V
R_{ce}	3.29 mΩ	R_f	2.22 mΩ
$E_{on}+E_{off}$	3.5 mJ	E_{rec}	5.9 mJ
$R_{th,1,Q}$	0.051 K/W	$R_{th,1,D}$	0.097 K/W
$\tau_{th,1,Q}$	5×10^{-4} s	$\tau_{th,1,D}$	5×10^{-4} s
$R_{th,2,Q}$	0.117 K/W	$R_{th,2,D}$	0.219 K/W
$\tau_{th,2,Q}$	5×10^{-3} s	$\tau_{th,2,D}$	5×10^{-3} s
$R_{th,3,Q}$	0.426 K/W	$R_{th,3,D}$	0.576 K/W
$\tau_{th,3,Q}$	0.05 s	$\tau_{th,3,D}$	0.05 s
$R_{th,4,Q}$	0.506 K/W	$R_{th,4,D}$	0.508 K/W
$\tau_{th,4,Q}$	0.2 s	$\tau_{th,4,D}$	0.2 s

6.2.2 Power Losses of Semiconductors

The T_{ji} is determined by the device's power losses which include both the conduction and switching loss. The real-time power loss calculation of a device x ($x = Q_1, Q_2, D_1, D_2$ and D_{NPC}) over a fundamental period is given as

$$P_{con} = \frac{1}{T_0}\int_{\varphi_2}^{\varphi_1} v_{drop}(t)i(t)\delta(t)dt \tag{6-2}$$

$$P_{sw} = \frac{f_{sw}}{T_0}\int_{\varphi_2}^{\varphi_1} E_{sw}\big(v_{dc}(t), i(t)\big)dt \tag{6-3}$$

$$P_{loss} = P_{con} + P_{sw} \tag{6-4}$$

where δ(t) is a switching function, denoted as δ(t) = 1 when device is on and δ(t) = 0 when device is off. $\boldsymbol{v_{drop}}$ is the conduction voltage drop on the resistance of a device and $\boldsymbol{E_{sw}}$ is the switching energy. For IGBT devices, $\boldsymbol{E_{sw} = E_{on} + E_{off}}$, while for anti-parallel diodes, $\boldsymbol{E_{sw} = E_{rec}}$. $\boldsymbol{\varphi_1}$ and $\boldsymbol{\varphi_2}$ are the phase angles. $\boldsymbol{T_0}$ is the fundamental period.

Based on the instantaneous power loss calculation, the average models of the five power devices in one arm has been listed in Table 6.2 according to [84].

Table 6.2. Average power loess of devices in a fundamental period [84].

	Conduction losses	Switching losses
T_1	$\frac{M\hat{I}}{12\pi}\{3V_{ce0}[(\pi-\varphi)cos(\varphi)+sin(\varphi)] + 2R_{ce}\hat{I}[1+cos(\varphi)]^2\}$	$f_{sw}E_{sw}\left(\frac{\hat{I}}{I_{ref}}\right)^{K_I}\left(\frac{V_{ce0}}{V_{ref}}\right)^{K_V}\frac{1+cos(\varphi)}{2\pi}G_I$
T_2	$\frac{\hat{I}}{12\pi}\{V_{ce0}[12+3M(\varphi cos(\varphi)-sin(\varphi))] + R_{ce}\hat{I}[3\pi-2M(1-cos(\varphi))^2]\}$	$f_{sw}E_{sw}\left(\frac{\hat{I}}{I_{ref}}\right)^{K_I}\left(\frac{V_{ce0}}{V_{ref}}\right)^{K_V}\frac{1-cos(\varphi)}{2\pi}G_I$
D_1	$\frac{M\hat{I}}{12\pi}\{V_{f0}[-\varphi cos(\varphi)+sin(\varphi)] + 2R_{ce}\hat{I}[1-cos(\varphi)]^2\}$	$f_{sw}E_{sw}\left(\frac{\hat{I}}{I_{ref}}\right)^{K_I}\left(\frac{V_{ce0}}{V_{ref}}\right)^{K_V}\frac{1-cos(\varphi)}{2\pi}G_I$
D_2	$\frac{M\hat{I}}{12\pi}\{V_{f0}[-\varphi cos(\varphi)+sin(\varphi)] + 2R_{ce}\hat{I}[1-cos(\varphi)]^2\}$	0
D_{npc}	$\frac{\hat{I}}{12\pi}\{V_{f0}[12+3M((2\varphi-\pi)cos(\varphi)-2sin(\varphi))] + R_f\hat{I}[3\pi-4M(1+cos^2(\varphi))]\}$	$f_{sw}E_{sw}\left(\frac{\hat{I}}{I_{ref}}\right)^{K_I}\left(\frac{V_{ce0}}{V_{ref}}\right)^{K_V}\frac{1+cos(\varphi)}{2\pi}G_I$
$\hat{I}$: Peak value of current; M: modulation index;		
I_{ref}: Reference current value of the switching loss measurement		
V_{ref}: Reference voltage value of the switching loss measurement		
K_I: Exponent for the current dependency of switching losses;		
K_V: Exponent for the voltage dependency of switching losses;		
G_I:Adaptation factor for the non-linear semiconductor characteristics;		

The analytical expression of the power losses in Table 6.2 is complicated and not suitably incorporated into the system modelling. $P_{loss,x}$ is represented by a 2nd order polynomial of active and reactive power, given as:

$$P_{loss,x} = a_{1,x}P_i + a_{2,x}P_i^2 + a_{3,x}P_iQ_i + a_{4,x}Q_i + a_{5,x}Q_i^2 = f_{loss,x}(P_i, Q_i) \quad (6\text{-}5)$$

where $\mathbf{a}_x = [a_{1,x}, a_{2,x}, a_{3,x}, a_{4,x}, a_{5,x}]$ is the coefficient vector obtained by the polynomial fitting. Take device T_1 as an example. The comparison between the polynomial fitting and the theoretical analysis is shown in Figure 6.3. As can be seen, the fitting results are satisfactory, although there is a slight mismatch.

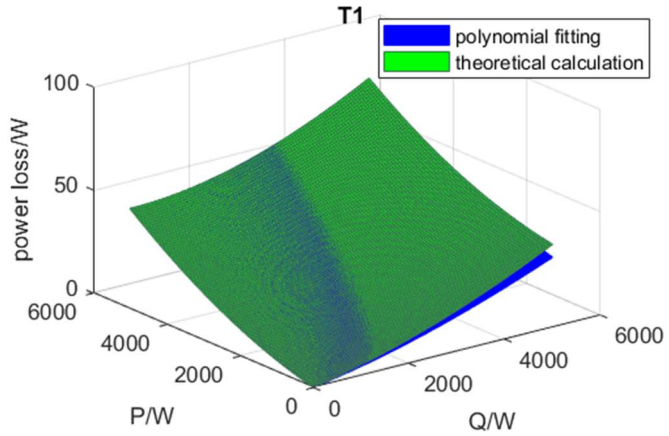


Figure 6.3. Comparison of power losses between theoretical analysis and polynomial fitting.

6.2.3 Junction Temperature Estimation

The junction temperature is estimated based on the thermal impedance network. There are types of the RC thermal impedance model – Cauer and Foster thermal models [106]. The model is adopted and shown in Figure 6.4. There are four layers of impedance with different time constants. The temperature at the top is the junction temperature, which has the highest value. The aging of the IGBT module is related to the junction temperature.

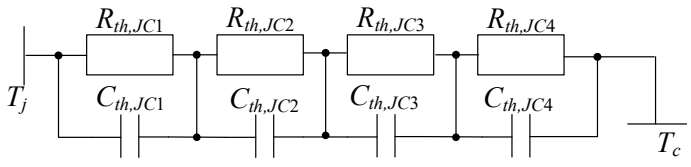


Figure 6.4. Thermal impedance network.

The junction temperature of power devices at steady-state can be calculated based on the 1-D lumped thermal network in Figure 6.4:

$$T_{j,x} = P_{loss,x}\left(R_{th,JH,x} + R_{th,HA}\right) + T_{jA} \quad (6\text{-}6)$$

where $R_{th,JH,x} = \left(R_{th,1,x} + R_{th,2,x} + R_{th,3,x} + R_{th,4,x}\right)$ is the thermal impedance of junction to heat sink. $R_{th,HA}$ is the thermal impedance of the heat sink to the ambient air. T_{jA} is the ambient temperature.

6.3 Thermal Control Capability Analysis

6.3.1 Thermal Control Limitation

Thermal regulation is limited to the adjustable range of active and reactive power among SMs. Assuming some SMs are overheated by ΔT_j, their junction temperature ($T_{j,oh}$) will be equal to that of normal SMs ($T_{j,nom}$) after applying the thermal sharing control method. Based on (3),

$$P_{loss,nom}R_{th,nom} = P_{loss,oh}R_{th,oh} + \Delta T_j \quad (6\text{-}7)$$

where $P_{loss,nom}$ and $P_{loss,oh}$ are the power losses of the most heated components in the normal and overheated SMs, respectively. $R_{th,nom} = R_{th,JH,nom} + R_{th,HA}$ and $R_{th,oh} = R_{th,JH,oh} + R_{th,HA}$ are the thermal impedances of junction to the ambient air of the corresponding components. $P_{loss,oh}$ has a lower boundary $P_{loss,min}$ which is determined by the minimum allowable power of a SM, $P_{i,min}$ and $Q_{i,min}$. As the remaining power is redistributed equally to the normal SMs, their active and reactive power are $\frac{P-mP_{i,min}}{N-m}$ and $\frac{Q-mQ_{i,min}}{N-m}$, where m is the number of overheated SMs, and $P = \frac{3}{2}V_d I_d$ and $Q = \frac{3}{2}V_d I_q$ are the active power and reactive power of the converter. As the reactive power of each SM can be reduced to zero, the minimum reactive power and current, $Q_{i,min}$ and $I_{qi,min}$, are then zero. The minimum active power $P_{i,min}$ is proportional to the minimum DC voltage $V_{dci,min}$ of the SM, and this is given as:

$$P_{i,min} = V_{dci,min}I_{dc} = V_{dci,min}\frac{P}{V_{dc}} \quad (6\text{-}8)$$

where $V_{dci} = \frac{V_{dc}}{N}$ is the DC voltage of the i^{th} SM and V_{dc} is the total DC link voltage. $V_{dc,min}$ should be no less than the peak AC voltage, but it should provide sufficient margin for the required power. The voltage synthesized by the converter is given as

$$v_d + jv_q = (R + j\omega L)\left(i_d + ji_q\right) + v_s \quad (6\text{-}9)$$

The phasor diagram of the converter voltage is shown in Figure 6.5. As the resistance is normally much lower than the inductive impedance, the voltage drop on the resistor can be omitted. Thus, it can be seen in Figure that the 90° lagging power factor would lead to the

largest converter voltage. The largest converter voltage and the required minimum DC voltage to provide such a voltage are given as

$$V_{dq,l} \approx \omega L I_s + V_s \tag{6-10}$$

$$V_{dc,min} = 2V_{dq,l} \tag{6-11}$$

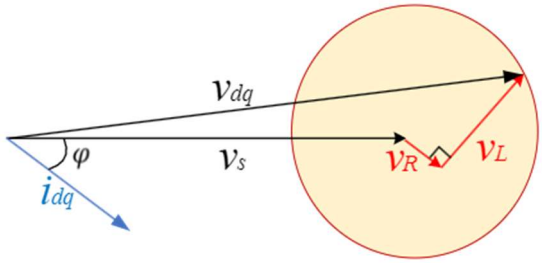


Figure 6.5. Phasor diagram of the converter voltage.

Considering10% of the grid overvoltage, $V_{dc,min}$ is expected to provide at least 1.2 p.u. V_s to supply the desired output power [107], [80]. The maximum value of ΔT_j to meet the condition for temperature equal sharing is obtained by combining (5-5)−(5-8) as:

$$\Delta T_{j,max} = f_{loss,nom}\left(\frac{\left(N - m\frac{V_{dc,min}}{V_{dc}}\right)P}{(N-m)N}, \frac{Q}{N-m}\right)R_{th,nom} - f_{loss,oh}\left(\frac{V_{dc,min}P}{NV_{dc}}, 0\right)R_{th,oh} \tag{6-12}$$

where $V_{dc,min} = 1.2 \times 2 \times \sqrt{2}NV_s^{sec}$ and V_s^{sec} is the AC voltage at the secondary side of the isolation transformer at the converter side (i.e., low voltage rating). In (6-12), $f_{loss,nom}$ and $f_{loss,oh}$ are the polynomial functions used for fitting the power losses of the normal and overheated SMs. The equation indicates that if the increased temperature of the overheated SMs exceeds $\Delta T_{j,max}$, the thermal sharing control limitation has been reached. Thus, temperature equal sharing cannot be achieved. This unequal sharing should be considered in the reference calculation of junction temperature.

6.3.2 Junction Temperature Reference Calculation

If $\Delta T_j \leq \Delta T_{j,max}$, the saturation of the temperature PI controller of a SM is not reached and the controller output is proportional to the error between the junction temperature and its reference. In this condition, T_j^* is selected as the mean value of T_{ji} $(i = 1,2,\dots,N)$ to avoid interfering

with the DC voltage and power. Assuming identical proportional and integral gains for all PI controllers, the sums of the compensation terms are:

$$\mathbf{X}_{comp,sum} = \mathbf{G}_{th,sum}(s)\left(T_j^* - T_{ji}\right) = \mathbf{0}_{1\times 2} \tag{6-13}$$

where $\mathbf{X}_{comp,sum} = \left[\sum_{i=1}^{N} v_{dci,comp}^* \quad i_{qi,comp}^*\right]$ is a vector with the sums of the compensation terms. $\mathbf{G}_{PI,th,dq}(s) = \left[\sum_{i=1}^{N} G_{PI,th,d}(s) \quad \sum_{i=1}^{N} G_{PI,th,q}(s)\right]$ is a vector with the sums of transfer functions of the PI controllers as entries. $\mathbf{0}_{1\times 2} = [0 \quad 0]$ is a vector with zero entries. From (6-13), it can be seen that the sums of $v_{dci,comp}^*$ and $i_{qi,comp}^*$ are zero, which implies that the thermal control does not influence the DC link voltage or total power.

As discussed previously, when ΔT_j is greater than $\Delta T_{j,max}$, the thermal control limit is reached. Under this condition, the output of the temperature PI controller of the overheated SMs will decrease to its lower limit. Thus, if T_j^* were still set as the mean value of T_{ji}, the sums of $v_{dci,comp}^*$ and $i_{qi,comp}^*$ in (6-13) would be non-zero and the thermal control would interfere with the DC voltage and total power regulation. To prevent this, T_j^* is selected as the mean temperature of the remaining (*N*-*m*) SMs instead of the mean temperature of all SMs. The temperature reference is thus modified as:

$$T_j^* = \frac{\sum_1^{N'} T_{jm}}{N'} \tag{6-14}$$

where T_{jm} is the temperature of the m^{th} SM that meets either $v_{dci,comp}^* \geq \Delta V_{dci,MIN}$ or $i_{qi,comp}^* \geq \Delta I_{qi,MIN}$, and N' is the number of SMs that meet such a constraint. Here, $\Delta V_{dci,MIN}$ and $\Delta I_{qi,MIN}$ are the limit values of the temperature PI controllers as shown in Fig. 3. In turn, $\Delta V_{dci,MIN} = V_{dci,min} - V_{dc0}^*$ and $\Delta I_{qi,MIN} = I_{qi,min} - I_{q0}^* = -I_{q0}^*$, and are selected according to the allowable minimum active and reactive power. To ensure $v_{dci,comp}^*$ and $i_{qi,comp}^*$ reach their minimum values at the same time, the ratio of the gain of the *d*-axis and *q*-axis PI controllers is selected as $\frac{G_{PI,th,d}(s)}{G_{PI,th,q}(s)} = \frac{|\Delta V_{dci,MIN}|}{|\Delta I_{qi,MIN}|}$.

6.3.3 Thermal Management by Power Adjustment

In the event of severe overheating, the highest temperature among SMs $T_{ji,max}$ may exceed the maximum allowable junction temperature $T_{j,MAX}^*$ even if a thermal control scheme is implemented. Thus, the power output of the cascaded converter must be reduced to avoid damaging the SMs. This is achieved by decreasing the apparent power setpoint S^*. To do this,

T_{ji} of all SMs is firstly sent from SM controllers to the main controller to identify the SM with the highest temperature. Then, an appropriate power reduction ΔS^* is calculated based on (6-5) and (6-6). Details for this process are given in the flowchart in Figure 6.6.

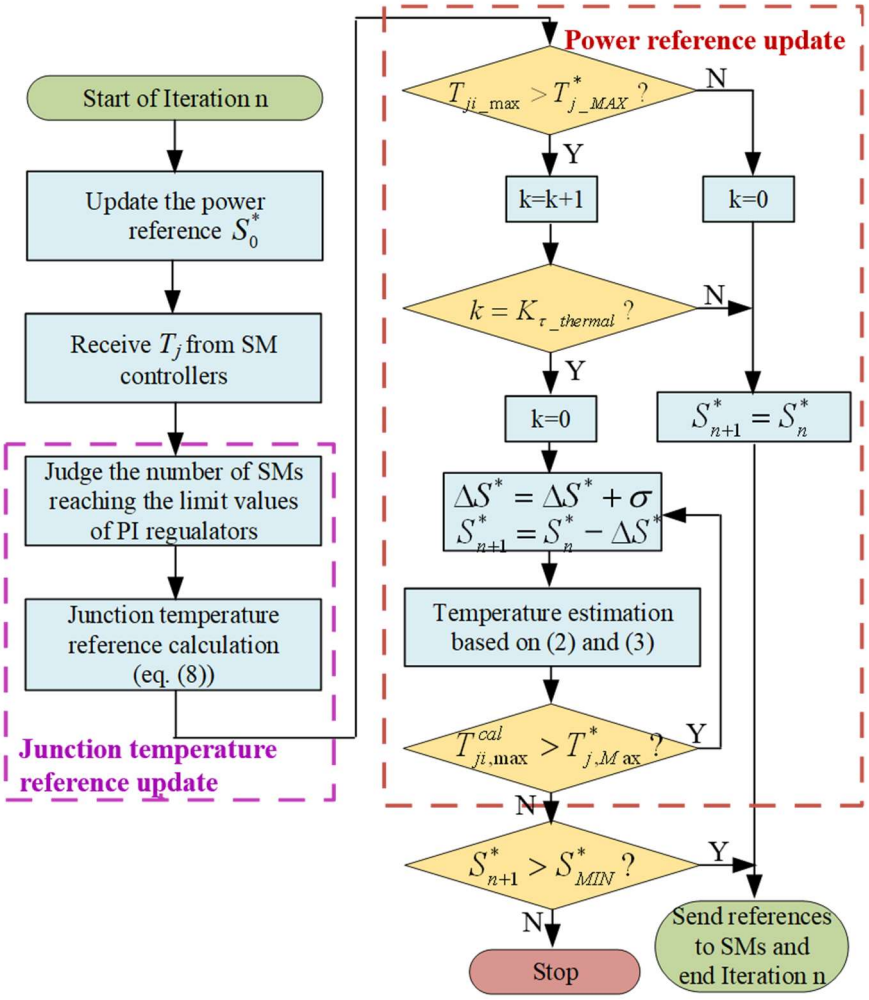


Figure 6.6. Thermal management inside the main controller.

The process starts by initializing setpoint S_0^*. The main controller receives T_{ji} from the SMs and uses (6-14) to calculate reference T_j^*. Meanwhile, the maximum temperature $T_{ji,max}$ is found. In the next step, $T_{ji,\max}$ is compared with a predetermined threshold value $T^*_{j,MAX}$. Considering a thermal time constant, a time delay $T_{delay} = K_{\tau,thermal} T_{PWM}$ is considered, which is the time interval for calculating ΔS^*, where T_{PWM} is the switching period ($T_{PWM} = \frac{1}{10\ kHz} = 100\mu s$). T_{delay} was selected as 200 ms in this paper by considering the time constant of the thermal impedance in Table 6.1. $K_{\tau,therm}$ is the counter value, which is equal to

$K_{\tau,therm} = \frac{T_{delay}}{T_{PWM}} = 2000$. If $T_{ji,\max} > T^*_{j,MAX}$ after T_{delay}, $S^*_{n+1} = S^*_n - \Delta S^*$ is updated for the next iteration. ΔS^* is iteratively obtained using (6-5) and (6-6) until condition $T^{cal}_{ji,\max} < T^*_{j,MAX}$ is met, where $T^{cal}_{ji,\max}$ is a theoretically calculated value of the maximum junction temperature which dictates whether S^*_n should be further decreased. If $T_{ji,\max}$ has been limited below $T^*_{j,MAX}$, S^*_n remains unchanged (i.e., $S^*_{n+1} = S^*_n$) and the algorithm proceeds to the next iteration. An allowable minimum power S^*_{MIN} could be set according to practical requirements. If $S^* < S^*_{MIN}$, the operation of system should be shut down.

6.4 Modelling and Controller Parameter Design

6.4.1 Small-signal Model of the System

1) *Small-signal model of a single SM:* The dynamic equations of the dq current loop in the SM controller are:

$$\dot{\hat{\boldsymbol{\imath}}}_{dqi} = \frac{1}{L}\left[\left(\hat{\boldsymbol{\imath}}^*_{dq0} + \hat{\boldsymbol{\imath}}^*_{dqi,comp} - \hat{\boldsymbol{\imath}}_{dqi}\right) + K_{i,I}\hat{\boldsymbol{x}}_{I_{dqi}}\right] - \frac{R\hat{\boldsymbol{\imath}}_{dqi}}{L} \tag{6-15}$$

$$\dot{\hat{\boldsymbol{\imath}}}_{I_{dqi}} = \hat{\boldsymbol{\imath}}^*_{dq0} + \hat{\boldsymbol{\imath}}^*_{dqi,comp} - \hat{\boldsymbol{\imath}}_{dqi} \tag{6-16}$$

where $\mathbf{i}_{dqi} = [i_{di} \quad i_{qi}]$ is the dq current, and $\mathbf{i}^*_{dq0} = [i^*_{d0} \quad i^*_{q0}]$ and $\mathbf{i}^*_{dqi,comp} = [i^*_{di,comp} \quad i^*_{qi,comp}]$ are the references produced by the power and thermal controllers, respectively. $\mathbf{x}_{I_{dqi}} = [x_{I_{di}} \quad x_{I_{qi}}]$ is the output of the integral action of the current PI controller, $K_{p,I}$ and $K_{i,I}$ are the proportional and integral gains of the controller, and L and R are the transformer leakage inductance and AC circuit resistance. In this notation, '$\hat{x}$' stands for the perturbed value of variable x and an uppercase notation is used to denote RMS values of AC variables (or average values of DC variables).

The equations of the DC voltage PI controller are:

$$\hat{\imath}^*_{di,comp} = K_{p,u_{dc}}\dot{\hat{x}}_{V_{dci}} + K_{i,u_{dc}}\hat{x}_{V_{dci}} \tag{6-17}$$

$$\dot{\hat{x}}_{V_{dci}} = -\hat{v}_{dci} + \frac{\hat{v}_{dc}}{N} + \hat{v}^*_{dci,comp} \tag{6-18}$$

where $v^*_{dci,comp}$ is the DC voltage reference generated by the thermal controller, $K_{p,u_{dc}}$ and $K_{i,u_{dc}}$ are the proportional and integral gains of the controller and $x_{V_{dci}}$ is the output of the integral action. The dynamic equation of the DC voltage of the SM is obtained from the power relationship between the AC and DC sides of a converter as

$$\dot{\hat{v}}_{dci} = \frac{I_{dc}\hat{v}_{dci}}{C_{dci}V_{dci}} + \frac{\hat{\imath}_{dc}}{C_{dci}} - \frac{3V_{di}\hat{\imath}_{di}}{2C_{dci}V_{dci}} \tag{6-19}$$

where i_{dc} is the DC link current and C_{dci} is the DC capacitance. Assuming v_{dc} is fully regulated by the DC voltage control station, $\hat{v}_{dc}$ is considered as zero for simplicity.

For modeling the dynamics of the thermal network, a four-layer thermal impedance with different time constants is normally considered ($\tau_{th,i}$). The time constants are shown in Table 6.1. However, to facilitate the analysis, a first-order transfer function $\left(\frac{R_{th,JH}}{\tau_{th}s+1}\right)$ was used instead to represent its dynamics, where τ_{th} is the equivalent time constant defined as the time when the output of the system is approximately equal to 0.63 times the steady value under a step input. A simulation was performed in the time-domain to analyze temperature variations caused by unit power losses, using both actual impedance and equivalent impedance. Figure 6.7 displays the comparison, which indicates a minor discrepancy. Thus, the equivalent impedance is acceptable to represent the dynamics of thermal behaviors.

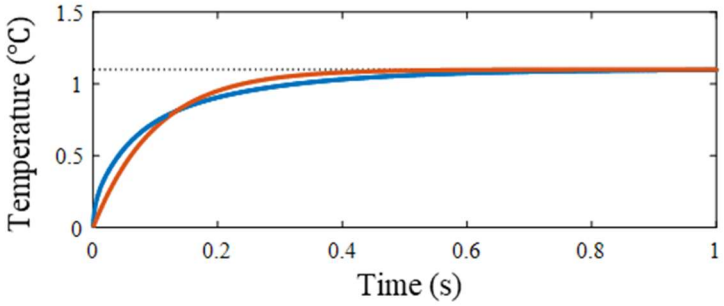


Figure 6.7. Change of temperature under unit power loss (the orange line represents equivalent impedance, and the blue line represents real impedance).

By linearizing (6-5), the dynamic equation of the thermal network is then

$$\dot{\hat{T}}_{ji} = \frac{-\hat{T}_{ji} + \hat{\mathbf{W}}_i \mathbf{F}_{loss}}{\tau_{th}} \tag{6-20}$$

where $\mathbf{F}_{loss} = [a_1 + 2a_2P_{0i} + a_3Q_{0i} \quad a_3P_{0i} + a_4 + 2a_5Q_{0i}]^T$ and $\mathbf{W}_i = [P_i \quad Q_i]$. It is noted that only the dynamics of the impedance of junction to heat sink are considered. The dynamics of the impedance of heat sink to the ambient air are not modeled due to the very large time constant (of around tens of seconds [74]). Hence, the temperature variation of the heat sink during an updating period of the thermal control loop is considered unchanged. Combining (6-15)−(6-20), the state-space representation of a single SM without controllers is:

$$\dot{\hat{\mathbf{x}}}_{SMi} = \mathbf{A}_{SMi}\hat{\mathbf{x}}_{SMi} + \mathbf{B}_{SMi}\hat{\mathbf{u}}_{SMi} \tag{6-21}$$

$$\hat{\mathbf{y}}_{SMi} = \mathbf{C}_{SMi}\hat{\mathbf{x}}_{SMi} \tag{6-22}$$

where $\mathbf{x}_{SMi} = \left[\mathbf{i}_{dqi} \quad \mathbf{x}_{I_{dqi}} \quad T_{ji} \quad v_{dc} \quad x_{V_{dci}}\right]^T$ is the state vector, $\mathbf{u}_{SMi} = [v^*_{dci,comp} \quad i^*_{qi,comp} \quad \mathbf{i}^*_{dq0}]^T$ is the input vector and $\mathbf{y}_{SMi} = [T_{ji} \quad \mathbf{W}_i]^T$ is the output vector. $\mathbf{A}_{SMi}$, $\mathbf{B}_{SMi}$ and $\mathbf{C}_{SMi}$ are provided in the Appendix B. The transfer matrix representation of (6-21)-(6-22) is obtained as

$$\widehat{\mathbf{Y}}_{SMi}(s) = [\mathbf{C}_{SMi}(s\mathbf{I} - \mathbf{A}_{SMi})^{-1}\mathbf{B}_{SMi}]\widehat{\mathbf{U}}_{SMi}(s) = \begin{bmatrix} G_{1,th}(s) & G_{2,th}(s) & G_{3,th}(s) & G_{4,th}(s) \\ G_{1,P}(s) & G_{2,P}(s) & G_{3,P}(s) & 0 \\ G_{1,Q}(s) & G_{2,Q}(s) & 0 & G_{3,Q}(s) \end{bmatrix} \widehat{\mathbf{U}}_{SMi}(s) \tag{6-23}$$

The outputs of the temperature and power PI controllers are given, respectively, by

$$\hat{v}^*_{dci,comp} = G_{PI,th,d}(s)\left(\hat{\delta}^*_i - \hat{\delta}_i\right) \tag{6-24}$$

$$\hat{\imath}^*_{qi,comp} = G_{PI,th,q}(s)\left(\hat{\delta}^*_i - \hat{\delta}_i\right) \tag{6-25}$$

$$\hat{\imath}^*_{dq0} = \frac{1}{N} G_{PI,W}(s)\left(\widehat{\mathbf{W}}^* - \widehat{\mathbf{W}}\right) \tag{6-26}$$

where $G_{PI,th,d}(s) = \frac{K_{P,th}s + K_{i,th}}{s}$, $G_{PI,th,q}(s) = \frac{0.2V_{dc}}{I_q} G_{PI,th,d}(s)$ and $G_{PI,W}(s) = \frac{K_{P,W}s + K_{i,W}}{K_{i,W}s}$ are the transfer functions of the thermal and power PI controllers (see Figure 6.1). In (6-26), $\mathbf{W}^*$ is the power reference and $\mathbf{W}$ is the output power ($\mathbf{W} = \sum_{i=1}^{N} \mathbf{W}_i$), whereas in (6-24) and (6-25), δ_i is the difference between T_{ji} and the mean value (i.e., $\delta_i = T_{ji} - \frac{\sum_{i=1}^{N} T_{ji}}{N}$), and δ_i^* is the reference of δ_i. To achieve equal thermal sharing, δ_i^* is set to zero.

2) *Small-signal model of the cascaded 3L-NPC converters*: Assuming the parameters for each SM are identical, the temperature equations for an *N* SM-cascaded system are:

$$\begin{cases} \hat{T}_{j1} = G_{\delta,th}(s)\left(\hat{\delta}^*_1 - \hat{\delta}_1\right) + \boldsymbol{G}_{W,th}(s)\left(\widehat{\boldsymbol{W}}^* - \widehat{\boldsymbol{W}}\right)^T \\ \hat{T}_{j2} = G_{\delta,th}(s)\left(\hat{\delta}^*_2 - \hat{\delta}_2\right) + \boldsymbol{G}_{W,th}(s)\left(\widehat{\boldsymbol{W}}^* - \widehat{\boldsymbol{W}}\right)^T \\ \vdots \\ \hat{T}_{jN} = G_{\delta,th}(s)\left(\hat{\delta}^*_N - \hat{\delta}_N\right) + \boldsymbol{G}_{W,th}(s)\left(\widehat{\boldsymbol{W}}^* - \widehat{\boldsymbol{W}}\right)^T \end{cases} \tag{6-27}$$

where $G_{\delta,th}(s) = \left(G_{1,th}(s) + \frac{0.2V_{dc}}{I_q} G_{2,th}(s)\right) G_{PI,th,d}(s)$, and $\mathbf{G}_{W,th}(s) = [\mathbf{G}_{P,th}(s) \quad \mathbf{G}_{Q,th}(s)] = \left[\frac{1}{N} G_{PI,W}(s)G_{3,th}(s) \quad \frac{1}{N} G_{PI,W}(s)G_{4,th}(s)\right]$. From (6-27), the following expressions are obtained:

$$\begin{cases} \hat{T}_{ji} - \hat{T}_{j1} = G_{\delta,th}(s)\left[\left(\hat{\delta}_i^* - \hat{\delta}_i\right) - \left(\hat{\delta}_1^* - \hat{\delta}_1\right)\right] \\ \hat{T}_{ji} - \hat{T}_{j2} = G_{\delta,th}(s)\left[\left(\hat{\delta}_i^* - \hat{\delta}_i\right) - \left(\hat{\delta}_2^* - \hat{\delta}_2\right)\right] \\ \vdots \\ \hat{T}_{ji} - \hat{T}_{jN} = G_{\delta,th}(s)\left[\left(\hat{\delta}_i^* - \hat{\delta}_i\right) - \left(\hat{\delta}_N^* - \hat{\delta}_N\right)\right] \end{cases} \tag{6-28}$$

Letting $\delta_N^* = -\sum_{i=1}^{N-1} \delta_i^*$ and adding all equations in (5-28) yields

$$\hat{\delta}_i = G_{\delta,th}(s)\left[\hat{\delta}_i^* - \hat{\delta}_i\right] \tag{6-29}$$

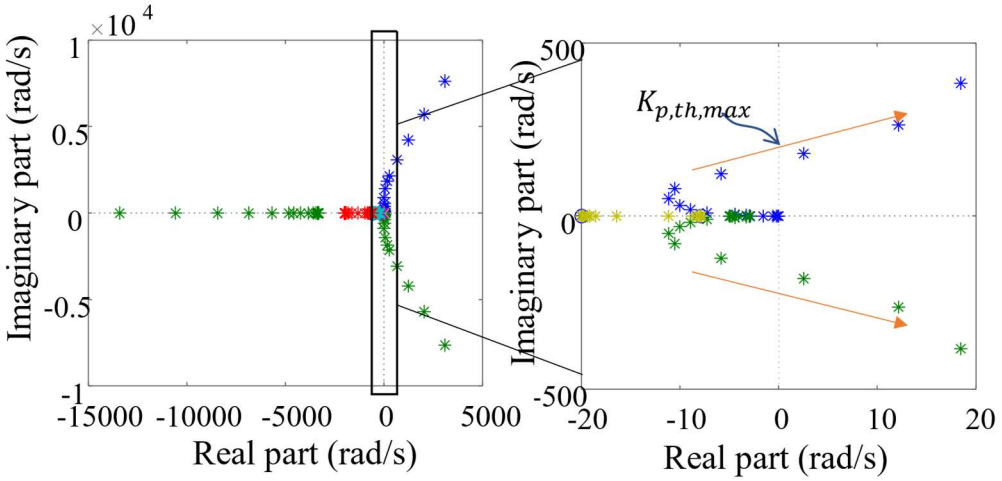
Solving for $\hat{\delta}_i$ results in

$$\hat{\delta}_i = \frac{G_{\delta,th}(s)}{1+G_{\delta,th}(s)}\hat{\delta}_i^* \tag{6-30}$$

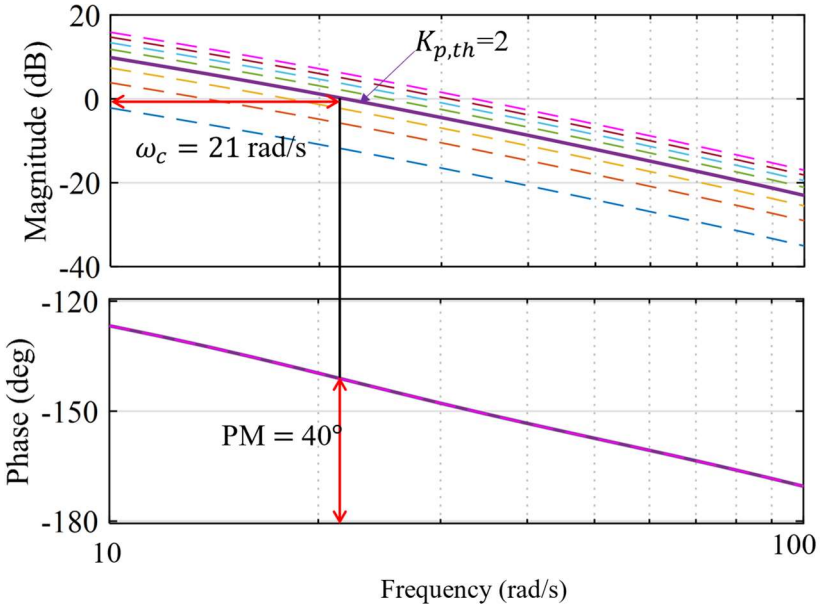
Equation (6-30) shows that when the constraint $\delta_N^* = -\sum_{i=1}^{N-1} \delta_i^*$ is met, the difference between the temperature of each SM and the mean temperature can be independently controlled. In fact, the control system has N control degrees of freedom: one for the control of total power and the remaining $N-1$ for temperature control between N modules. The thermal balancing control (i.e., $\hat{\delta}_i^* = 0$) is a special case as $\hat{\delta}_i^*$ can be selected arbitrarily to regulate the temperature difference between any neighboring SMs. As the thermal control loops are decoupled from each other and from the power controller, $G_{PI,W}(s)$, $G_{PI,th.d}(s)$ and $G_{PI,th.q}(s)$ can be tuned separately.

6.4.2 Controller Parameter Tuning

The tuning of $G_{PI,W}(s)$ is referred to [101], and only tuning of $G_{PI,th}(s)$ was discussed in this thesis. The zero of $G_{PI,th,d}(s)$ is selected to cancel the pole of the equivalent thermal impedance transfer function $\frac{R_{th,JH}}{\tau_{th}s+1}$ which has the largest time constant in the control system. Thus, $K_{i,th}$ is selected as $K_{i,th} = K_{P,th}/\tau_{th}$. The parameters of the controllers and relevant circuit used for tuning the thermal PI controller are same as Chapter 3. Figure 6.8(a) shows that the closed-loop poles locate in the left-half s plane when $K_{p,th}$ is less than the threshold gain value $K_{p,th,max}$, which indicates that the system is stable. If $K_{p,th}$ is larger, the system may become unstable since the dominant poles move to the right-half s plane. To further select a suitable gain, the Bode diagram of $G_{\delta,th}(s)$ is analyzed in Figure 6.8 (b). As seen, the bandwidth of the thermal control loop increases as the value of $K_{P,th}$ increases, whereas the phase margin is reduced. To obtain a suitable dynamic performance, $K_{P,th}$=2, where the cut-off frequency is 20 rad/s and the phase margin is 40º.



(a)



(b)

Figure 6.8. Frequency-domain analysis. (a) Closed-loop poles' trajectories with increase of $K_{p,th}$. (b) Bode plot of $G_{\delta,th}(s)$ with different $K_{P,th}$ from 0.5 to 4.

6.5 Simulation and Experimental Validation

6.5.1 Simulation Results

The simulation is conducted based on the PLECS with four SMs are cascaded together. The $R_{th,JH}$ of SM1 is larger than that of other three SMs to create the mismatch in parameters of components. In Figure 6.9, the $R_{th,JH}$ of SM1 is increased to twice the normal value and the system is operated without thermal sharing control. As it can be seen in Figure 6.9(a) and (b),

the junction temperature swing of SM1 is 1.7 ℃ higher, and meanwhile, the mean temperature is 10 ℃ higher than that of the others.

Figure 6.10 shows the case when thermal sharing control is implemented. As shown in Figure 6.10(a) and (b), the junction temperature of the four SMs have been equally shared. To achieve this, the DC voltage of the SM1 decreases to around 80 V while the others increase to 95 V (see Figure 6.9(c)). However, the total power is not influenced since the power control is decoupled with the thermal sharing control (see Figure 6.10(d)).

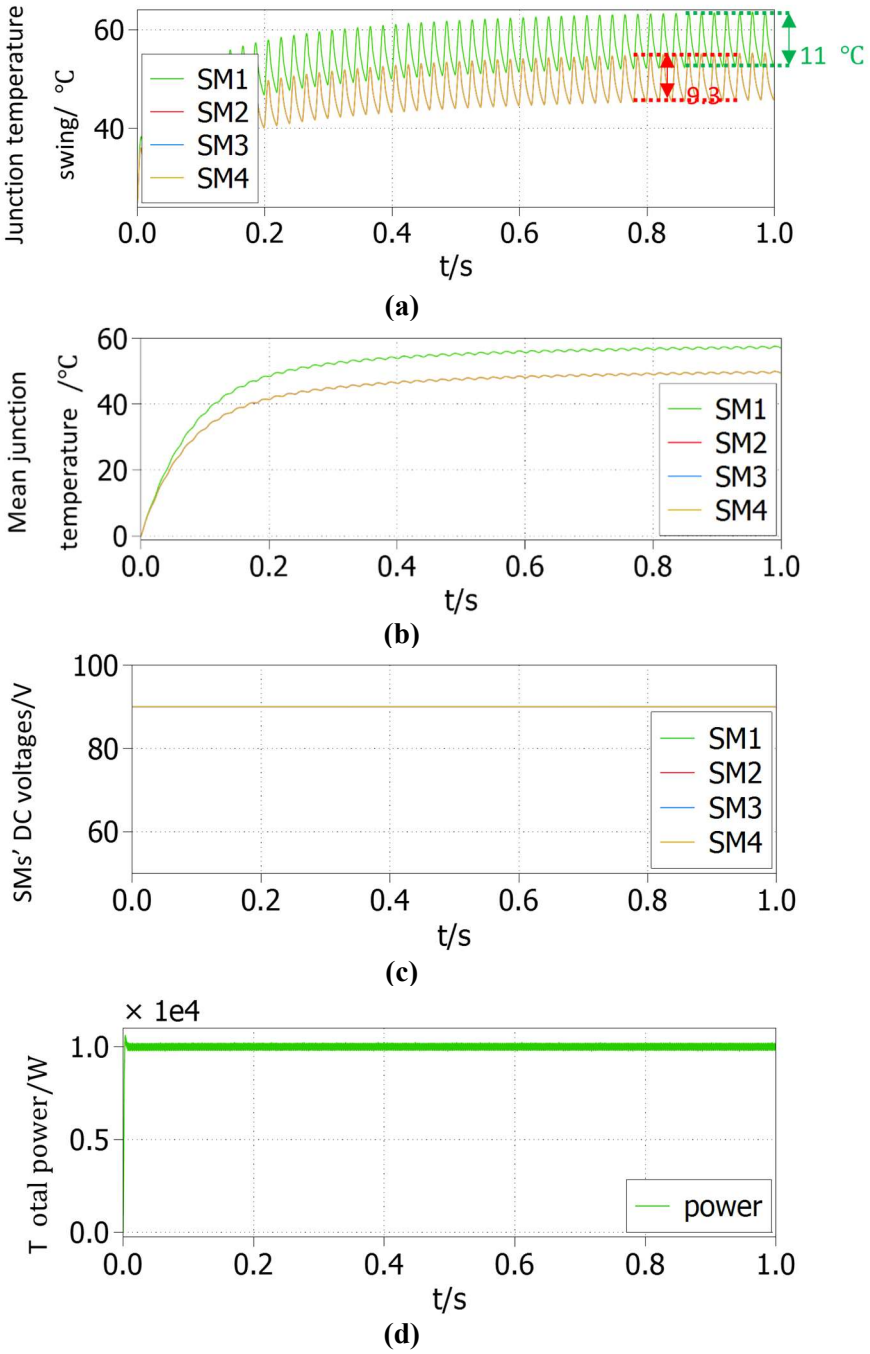


Figure 6.9. Results without using thermal sharing control.

Figure 6.11 and Figure 6.12 show the case when $\boldsymbol{R_{th,JH}}$ of SM1 is changed to be four times larger than that of other SMs to mimic a more severe overheating condition. In Figure 6.11, the temperature reference is the mean value of the junction temperature of the four SMs. When the thermal control capability reached the limitation after 0.3 s (see Figure 6.11(c)). The thermal PI regulator of SM1 is saturated, and consequently, the thermal sharing control is no longer decoupled with the power control. Thus, the power control is affected, and the power has a large drop in Figure 6.11(d).

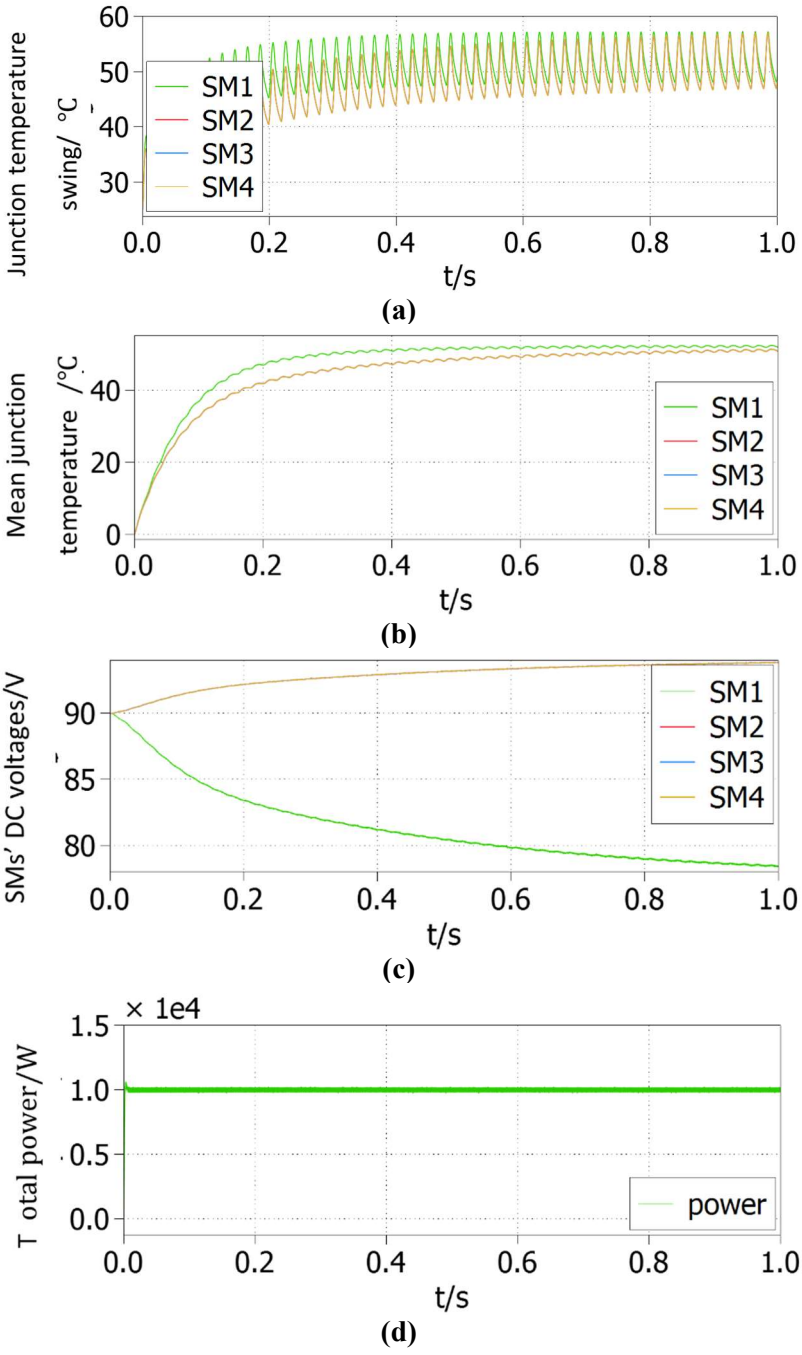
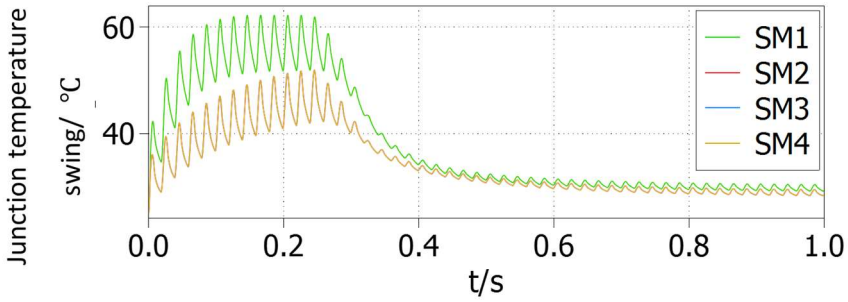
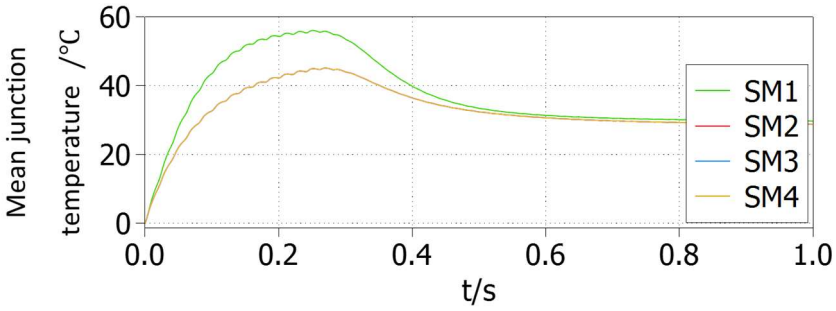


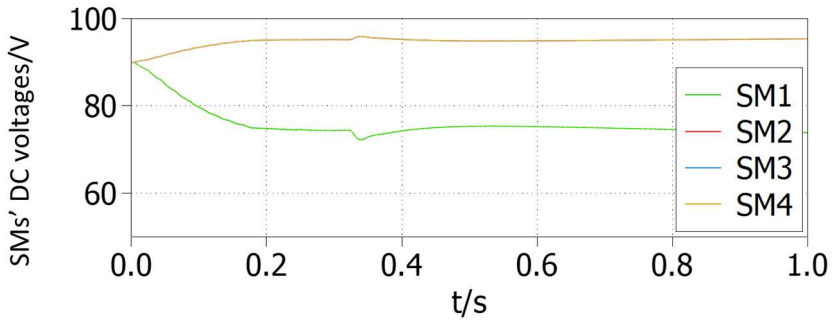
Figure 6.10. Results with using thermal sharing control.



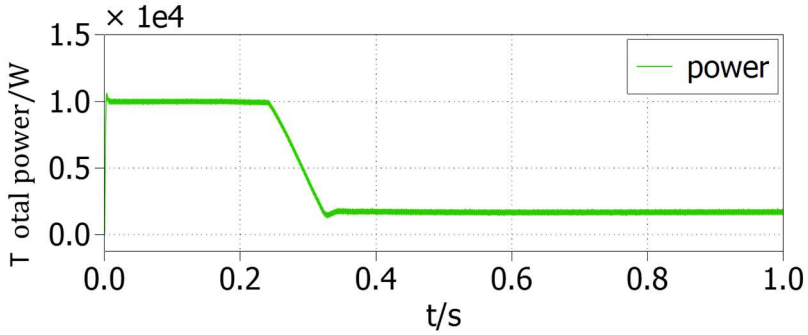
(a)



(b)

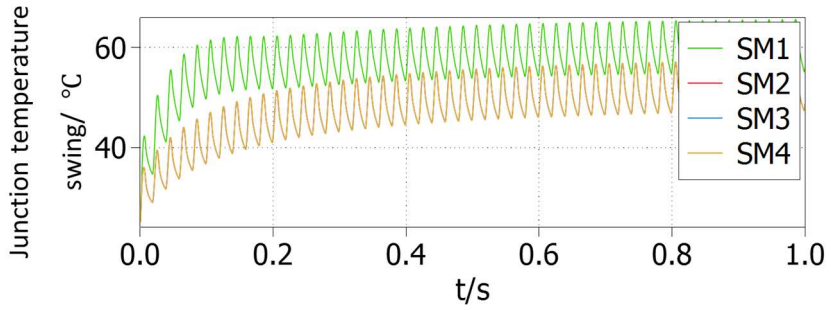


(c)

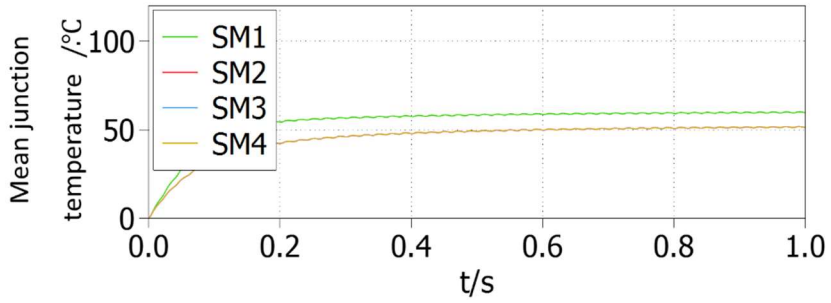


(d)

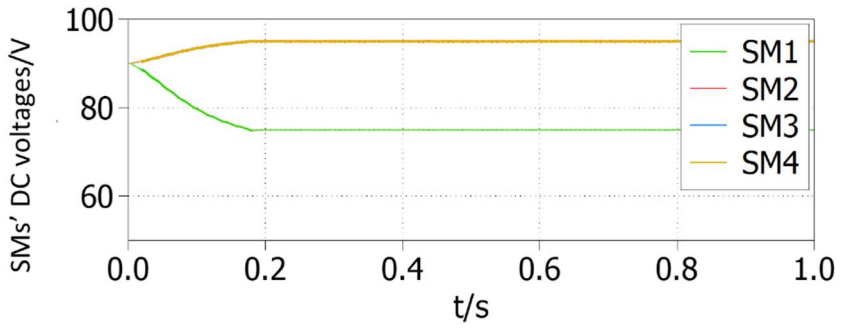
Figure 6.11. Results under maximum thermal control capbility (temperature reference is the mean value of the four SMs).



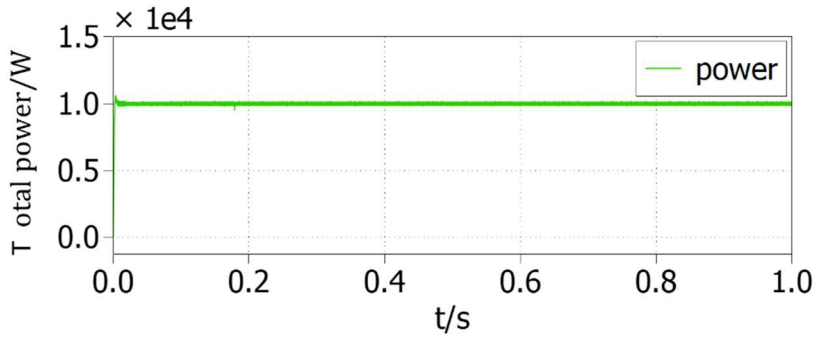
(a)



(b)



(c)



(d)

Figure 6.12. Results under maximum thermal control capbility (temperature reference is the mean value of the remaining SMs except for SM1).

In Figure 6.12, the temperature reference is changed to the mean value of the junction temperature of the remaining three SMs after the thermal control limitation of SM1 is reached.

Thus, the decoupling between the power control and thermal sharing control still holds. This is reflected in Figure 6.12(d). As the maximum thermal control capability has been reached, the temperature of SM1 is not completely equal to that of the others. There is a difference of about 8 ℃ in temperature between SMs, as shown in Figure 6.12(a) and (b).

6.5.2 Experimental Results

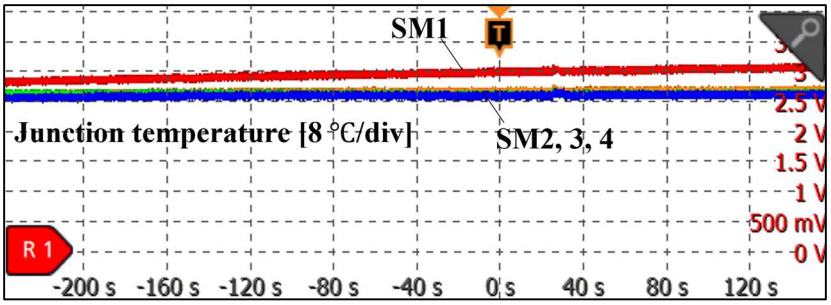
The effectiveness of the proposed thermal balancing approach is validated through the laboratory-scale MVDC testbed, which is same as the configuration in Chapter 3. The negative-temperature-coefficient (NTC) thermistor inside the power module package was used to measure the heat sink temperatures of SMs. Each SM is installed with a cooling fan to dissipate the heat of power devices. The estimated junction temperature is obtained using a digital-to-analogue converter, which has a sensitivity of 16 ℃/V.

In practice, the air-cooling system may encounter failures due to issues caused by electronic parts, such as the power supply and power drives, and mechanical parts, such as the bearings, lubricant, shaft and fan blades [108]. These may lead to a reduction of air flow rate and even complete failure of the cooling system. In the experimental tests, the fan speed is regulated from zero to the rated speed (3000 rpm) to mimic cooling conditions.

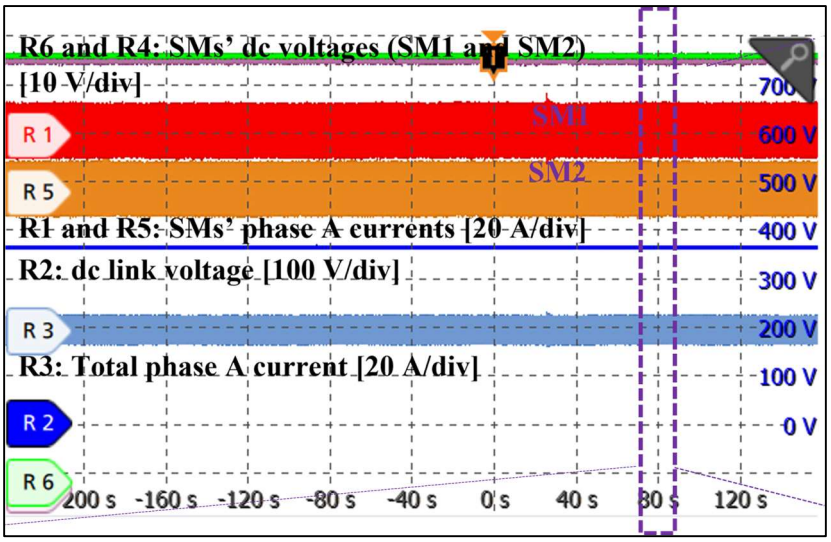
Figure 6.13 shows the typical voltage balancing control while the fan of SM1 is operated at 60% rated speed to mimic partial failure conditions (with the remaining three SM fans operating at 100% rated speed. It is seen that there is a temperature difference of around 8 ℃ between SM1 and remaining SMs (i.e. SM2, 3 and 4) in Figure 6.13(a). The DC voltages of the SMs and currents of phase A of SM1 and SM2 and the total DC voltage and current of the four SMs are given in Figure 6.13(b). As seen from traces R4, R6, R1 and R5 within the yellow dashed rectangle, the SMs' currents and DC voltages are equally shared.

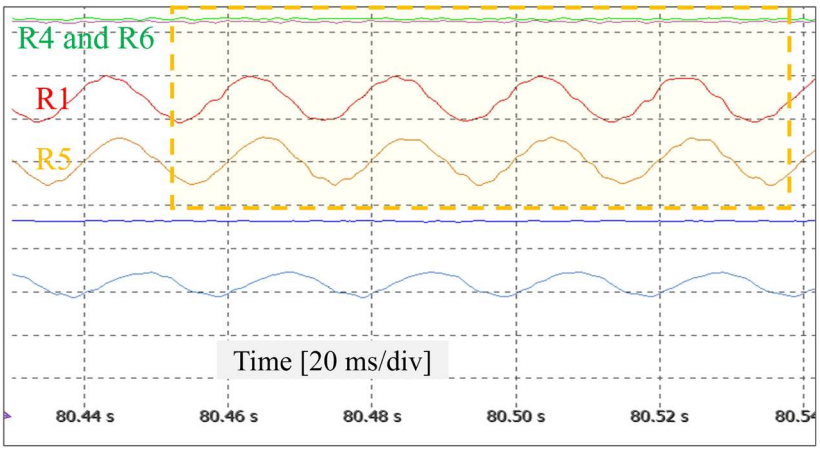
Figure 6.14 shows the waveforms when the thermal sharing control is implemented for the same cooling system failure conditions as in Figure 6.13. The temperature difference between SM1 and other SMs is effectively reduced (see Figure 6.14(a)). The balance of junction temperature is achieved by the closed-loop regulation afforded by the thermal controller in Figure 6.1. The DC voltage and current of SM1 are decreased to eliminate the overheating, and conversely, the DC voltage and AC current of SM2 are increased. As seen from the zoomed-

in view in Figure 6.14(b), the DC voltage difference between traces R6 (SM1) and R4 (SM2) is around 8 V and the difference of peak-to-peak AC current between traces R1 (SM1) and R5 (SM2) is around 5.5 A (obtained by the value of R5 minus R1).



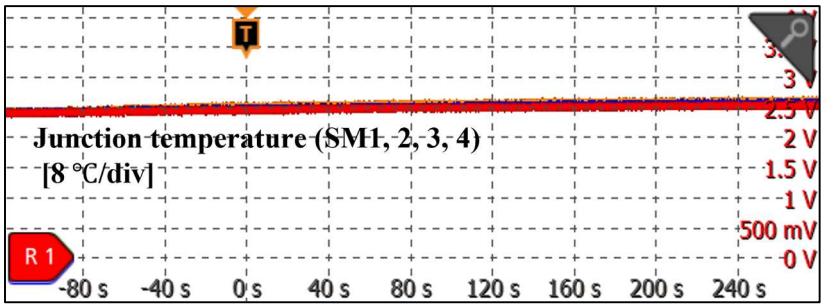
(a)



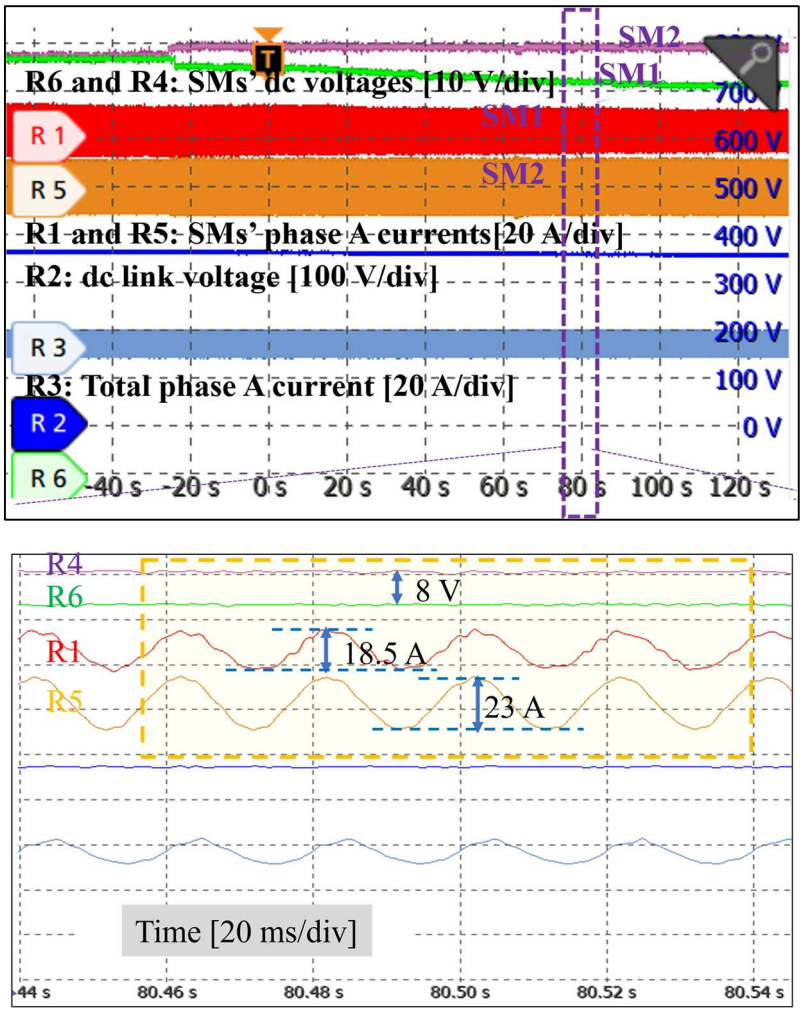


(b)

Figure 6.13. Junction temperatures of SMs without thermal sharing control (the fan of SM1 is at 60% rated speed and the others at 100% rated speed): (a) junction temperatures of SMs; (b) SM and total AC current and DC voltage (the bottom plot shows a zoomed-in view).

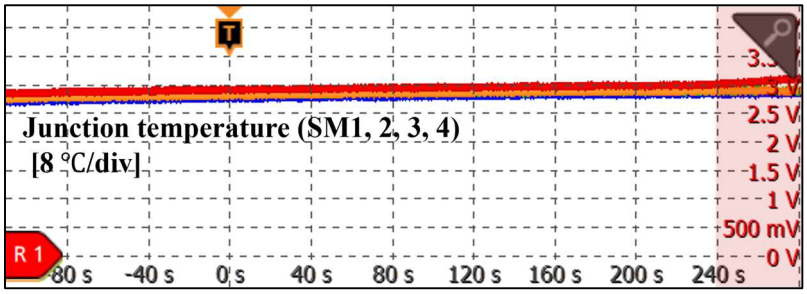


(a)

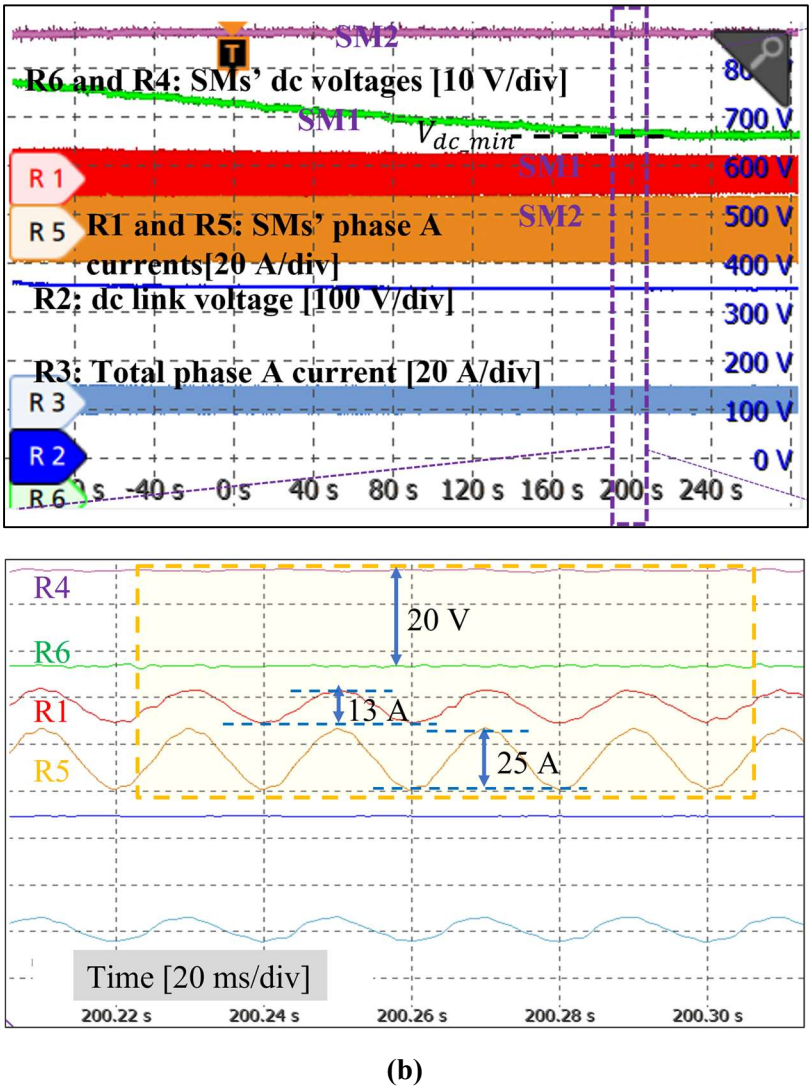


(b)

Figure 6.14. Junction temperatures of SMs with thermal sharing control (same thermal conditions as in Figure 6.12): (a) junction temperatures of SMs; (b) SM and total AC current and DC voltage (the bottom plot shows a zoomed-in view).



(a)



(b)

Figure 6.15. Junction temperatures of SMs with thermal sharing control (the fan of SM1 is at zero speed and the others at 100% rated speed): (a) junction temperatures of SMs; (b) SM and total AC current and DC voltage (the bottom plot shows a zoomed-in view).

Figure 6.15 shows that the dc voltage further decreases to the minimum limit value when the fan speed is zero to mimic the full cooling system failures of SM1. At a time of 220 s, the dc voltage of SM1 has reached its minimum value set as 75 V (see Figure 6.15(b)). With the

thermal balancing control, the differences in dc voltages and AC currents of SMs at this severe condition are increased to 20 V and 12 A (obtained by subtracting the values of R5 minus R1), which are larger than those in Figure 6.14(b). Meanwhile, the temperature reference is changed automatically to the average temperature of SMs 2, 3, and 4. Since the thermal control capability has been reached, a slight temperature imbalance appears after 240 s (see the pink rectangle in Figure 6.15(a)). It is seen that the total output power in Figure 6.14(b) and Figure 6.15(b) is not influenced by implementing the thermal controller, which verifies that the thermal control scheme is decoupled from the power control. It is noted that the dynamics of temperatures in experimental tests have slow response time than those in simulation results. This is because the heat sink temperature in simulation is set as constant, thus the dynamics due to the time constant of the cooling system is omitted.

As SMs work at different operating points, there is a risk of deteriorating the harmonic performance of the total current [74]. To investigate this point, the fast Fourier transform (FFT) for the system under a conventional power balancing control is compared with that under the presented thermal sharing control. The spectra of the currents of phase-A under both control strategies are shown in Figure 6.16(a). Figure 6.16(b) shows the zoomed-in total phase-A currents displayed in Figure 6.13(b) and Figure 6.15(b), respectively. The harmonics for both control methods within the range of 0 to 50 kHz present similar characteristics. Hence, the presented control strategy has little impact on the current distortion.

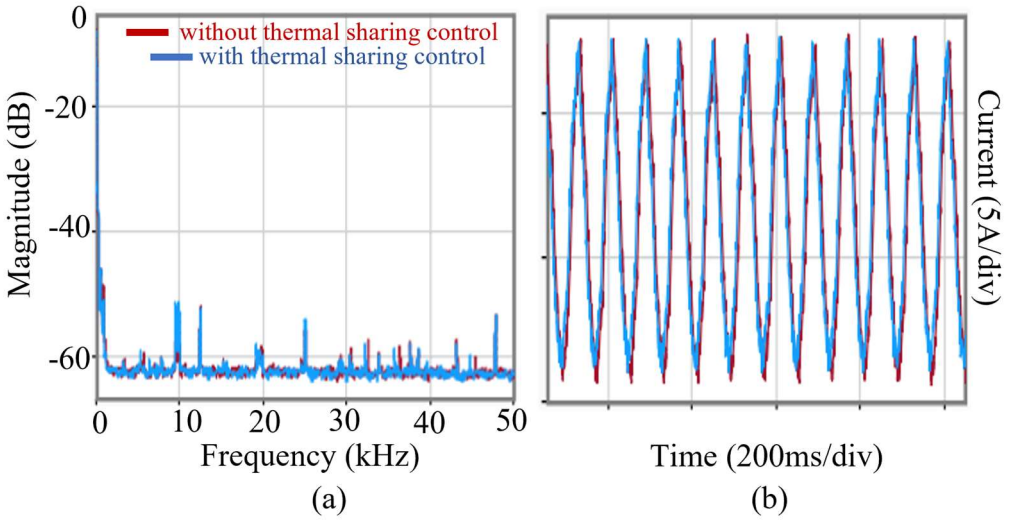


Figure 6.16. FFT analysis of AC harmonics with and without thermal sharing control.

6.6 Summary

For the cascaded 3L-NPC converters, the thermal stresses may be distributed unequally among SMs even with and thus influence the system reliability and increase maintenance cost. The proposed active thermal sharing control method is able to balance the thermal stresses by concurrently regulating the active and reactive power. Based on a temperature PI regulator in each SM, the junction temperature difference between SMs can be effectively balanced.

A unique issue exhibited by the cascaded 3L-NPC converter topology is the limitation of the thermal regulation which is constrained by the minimum DC voltage of the SM. In the event of severe temperature imbalance, the thermal control limit can be reached. In this case, the temperature reference is modified by the main controller to maintain the system operation. To facilitate the controller design, a small-signal system model is presented. Based on the system model, it is found that the power and thermal control loops are decoupled so that the thermal and power controller can be independently designed.

The presented thermal sharing control scheme was experimentally validated through the laboratory-scale MVDC testbed. The cooling system failures may occur due to the faults of electronic and mechanical parts. Converters consisting of four cascaded SMs at 360 Vdc/ 2 kVA were tested at different temperature conditions to mimic cooling system failures, which were achieved by adjusting the cooling system. By implementing the presented thermal control, the junction temperature has been effectively balanced under cooling system failures.

Chapter 7

Conclusions and Future Work

This chapter concludes the contributions in the thesis and presents the potential challenges to be solved in future work and related technical solutions.

7.1 Conclusions

High integration of renewable energies into distribution networks poses great challenges to the existing grid. MVDC technology can offer good controllability of power flows, enhanced power transfer capability and a better control of grid voltages. In the ANGLE-DC project in UK, cascaded 3L-NPC converters were adopted due to its lower cost compared with its counterparts−MMCs. As the cascaded 3L-NPC converters are first used in the MVDC power transmission system, the suitable control methods are still under-researched. This thesis contributed to the active control of such a type of converter in distributed networks, with a laboratory-scale MVDC testbed being used to demonstrate the presented control methods.

A hierarchical control structure was presented for this cascaded converter. The switching control and converter control are implemented in each SM and the application control is implemented in the main controller. The main controller can provide flexible control and management for all the cascaded SMs. The suitable hardware communications were explored as well. Converter-level and system-level measures are coordinated to enable fast blocking and isolation of converter under fault conditions. To provide confidence in the control methods, a MVDC testbed was developed based on the real ANGLE-DC project. This testbed features the same characteristics as the real converter station under per-unit scales. With the developed experimental facilities, typical operating scenarios have been verified, including system start-up/shut-down procedures, voltage and power control performance, transition between control modes, and system protection.

A unique challenge exhibited by the cascaded 3L-NPC converters is that the DC voltage imbalance may occur between SMs. The DC voltage imbalance may result in system stability if suitable measures are not taken. The mechanism behind the voltage imbalance is first analysed. Then, the voltage balancing control methods were presented, including the PI-based method with communication and inverse-droop based method without communication. The PI controller with communication is used to precisely regulate SMs' voltages without influencing output power, while the inverse-droop based control takes over the DC voltage regulation upon loss of communication, thus ensuring that the system can continue to operate. The hybrid control structure that combines both PI-based and droop-based methods were also analysed. It is found that all the SMs should switch to the droop-based methods concurrently if communication in any of SMs is failed. The effectiveness of presented methods has been

validated through MATLAB simulation and experimental tests.

With development of MVDC technologies, more renewable energies will be integrated into the MVDC link of through the power electronic converters. The multi-terminal MVDC link will become the future trend. DC voltage balancing control in each converter should be designed in consideration together with the interactions of different converters in a complex multi-terminal system. The multiple crossovers due to interactions between different converter will inevitably happen, which may cause adverse impacts such as the power and voltage drifts due to the multiple crossovers. The interactions between constant current and voltage vs. power droop control was analysed in this thesis. Firstly, the mechanism of power and voltage drifts was analysed. It is shown that that the normal operating point is unstable in the condition of multiple crossovers. Secondly, a control scheme was presented to ensure DC voltage balancing performance and power control accuracy and concurrently, to avoid the multiple crossovers. This is achieved by suitable droop gain design and a secondary power compensator. The presented solution has been verified through MATLAB simulation and experimental validated based on a three-terminal MVDC testbed. The accuracy of power at steady-state has been improved by 15% since the multiple crossovers are eliminated. Besides, the power accuracy has been further improved by 13% with a secondary power compensator at dynamic changes of DC current.

Beyond the electric characteristics, thermal characteristics of converter is also of great concern. Although DC voltage balancing control can ensure the equal voltage and power sharing in SMs, the thermal stress may not be equally shared in abnormal conditions such as the mismatched components and partial cooling system failures in SMs. This may cause premature failure of certain SMs, thereby reducing the system lifetime. To improve the system reliability, an active thermal sharing control was presented on the basis of the voltage balancing control. An additional thermal control loop was added in each SM. The references of DC voltage and reactive current in SMs are regulated according to their individual temperature. The thermal control capability that is limited to the minimum DC voltages of SMs were also analysed. Controller parameters were tuned based on the detailed electrical and thermal models. The cases for mismatched components in IGBT devices and different cooling conditions in SMs were studied through PLECS simulation and experimental tests. It is shown that the junction temperature of SMs was effectively balanced using the presented methods.

7.2 Future Work

7.2.1 Bypass Operation under Fault Conditions

The cascaded 3L-NPC converter was designed without the capability to achieve bypass operation when any of SMs is failed. This means that if one SM is damaged, the whole system must be shut down. This will increase the maintenance cost and reduce the control flexibility of the system. Bypassing the fault SMs in real-time can ensure the safe and continuous operation of the system.

Thus, in the next step of study, how to achieve online bypass operation of system will be focused. DC circuit breakers are supposed to be parallelly connected to the DC terminal of each SM. If a SM encounter faults, the DC circuit breaker should be closed to discharge the DC capacitor, thus bypassing the DC side of the fault SM. An IGBT based circuit breaker is expected to use as the discharging rate can be controlled to avoid fast discharging of the DC capacitor. An additional mechanical circuit breaker can be paralleled to the DC terminal as well and is closed when the DC voltage of the fault SMs is decreased to zero. The conventional AC circuit breaker can be used to isolate the fault SMs with the grid at AC side. The impact of the bypassing process on other SMs should be also analyzed. Finally, suitable control should be investigated to make the SM that has been bypassed reconnect to the grid after the fault is cleaned.

7.2.2 Disturbance-observer based Adaptive Control

The internal and external disturbances would affect the system performance. The internal disturbance can be the mismatches of components in SMs and the external disturbance can be the fluctuation of grid voltage or the fluctuation of the voltage at the secondary transformer.

To improve the robustness of the system, one potential solution is to use the disturbance observer based adaptive control methods. The disturbance terms should be included in the system model, and then model predictive control can be used to achieve the maximization of a given objective function. Efficiency, harmonics and tracing performance can be included in the objective function.

Appendix A

For the state-space representation in (4-7), let $k_1 = -k_{iid}$, $k_2 = -k_{iiq}$, $k_3 = \frac{1}{L_s}$, $k_4 = -\frac{R}{L_s} - \frac{k_{pid}}{L_s}$, $k_5 = \frac{V_s + RI_d - \omega LI_q}{L_s V_{dc}}$, $k_6 = \frac{1}{L_s}$, $k_7 = -\frac{R}{L_s} - \frac{k_{piq}}{L_s}$, $k_8 = \frac{RI_q + \omega LI_d}{L_s V_{dc}}$, $k_9 = \frac{-3I_d}{2C_{dc}V_{dc}}$, $k_{10} = \frac{-3I_q}{2C_{dc}V_{dc}}$, $k_{11} = -\frac{3V_s + 3(R - k_{pid})I_d}{2C_{dc}V_{dc}}$, $k_{12} = -\frac{3(R - k_{piq})I_q}{2C_{dc}V_{dc}}$, $k_{13} = k_{iid}$, $k_{14} = \frac{k_{pid}}{L_s}$, $k_{15} = \frac{3k_{pid}I_d}{2C_{dc}V_{dc}}$.

The coefficients in equation (4-13) are:

$a_5 = 1$, $a_4 = -(k_4 + k_7)$, $a_3 = k_4k_7 - k_3k_1 - k_6k_2 - k_5k_{11} - k_8k_{12}$, $a_2 = k_6k_2k_4 + k_7k_3k_1 + k_5k_7k_{11} + k_4k_{12}k_8 - k_5k_9k_1 - k_8k_{10}k_2$, $a_1 = k_6k_2k_3k_1 + k_5k_7k_9k_1 + k_8k_2k_4k_{10} - k_6k_5k_2k_{11} - k_8k_{12}k_3k_1$, $a_0 = k_6k_2k_9k_{11}k_5 + k_3k_1k_2k_{10}k_8$.

The coefficients in equation (4-16) are:

$a'_6 = a_5$, $a'_5 = a_4 + k_{pudc}\lambda_4$, $a'_4 = a_3 + k_{pudc}\lambda_3 + k_{iudc}\lambda_4$, $a'_3 = a_2 + k_{pudc}\lambda_2 + k_{iudc}\lambda_3$, $a'_2 = a_1 + k_{pudc}\lambda_1 + k_{iudc}\lambda_2$, $a'_1 = a_0 + k_{pudc}\lambda_0 + k_{iudc}\lambda_1$, $a'_0 = k_{iudc}\lambda_0$, where $\lambda_4 = k_{15}$, $\lambda_3 = k_9k_{13} + k_{11}k_{14} - k_{15}(k_4 + k_7)$, $\lambda_2 = k_{15}(k_4k_7 - k_1k_3 - k_6k_2) + k_{13}(k_{11}k_3 - k_9k_7 - k_9k_4) + k_{14}(k_1k_9 - k_{11}k_7)$, $\lambda_1 = k_{15}(k_6k_2k_4 + k_7k_3k_1) + k_{13}(k_4k_7k_9 - k_3k_{11}k_7 - k_6k_2k_9) - k_{14}k_1k_7k_9$, $\lambda_0 = k_{15}k_6k_2k_3k_1 + k_{13}(k_6k_2k_4k_9 + k_6k_2k_3k_{11}) + k_{14}k_6k_2k_9k_1$.

The coefficients in equation (4-19) are:

$a''_5 = a_5$, $a''_4 = a_4 + k_{droop}\lambda_4$, $a''_3 = a_3 + k_{droop}\lambda_3$, $a''_2 = a_2 + k_{droop}\lambda_2$, $a''_1 = a_1 + k_{droop}\lambda_1$, $a''_0 = a_0 + k_{droop}\lambda_0$.

Appendix B

Matrices of the small-signal model of equations (5-21) and (5-22) are given as:

$$\boldsymbol{A}_{SMi} = \begin{bmatrix} k_1 & 0 & k_2 & 0 & 0 & k_3 & k_4 \\ 0 & k_5 & 0 & k_6 & 0 & 0 & 0 \\ k_7 & 0 & 0 & 0 & 0 & k_8 & k_9 \\ 0 & k_{10} & 0 & 0 & 0 & 0 & 0 \\ k_{11} & k_{12} & 0 & 0 & k_{13} & 0 & 0 \\ k_{14} & 0 & 0 & 0 & 0 & k_{15} & 0 \\ 0 & 0 & 0 & 0 & 0 & k_{16} & 0 \end{bmatrix}$$

$$\mathbf{B}_{SMi} = \begin{bmatrix} \frac{K_{p,I}K_{p,u_{dc}}}{L} & 0 & \frac{K_{p,I}}{L} & 0 \\ 0 & \frac{K_{p,I}}{L} & 0 & \frac{K_{p,I}}{L} \\ K_{p,u_{dc}} & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}$$

$$\mathbf{C}_{SMi} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ \frac{3V_{di}}{2} & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & \frac{3V_{di}}{2} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

where $k_1 = k_5 = -\frac{K_{p,I}+R}{L}$, $k_2 = k_6 = \frac{K_{p,I}K_{i,I}}{L}$, $k_3 = \frac{-K_{p,I}K_{p,u_{dc}}}{L}$, $k_4 = \frac{K_{p,I}K_{i,u_{dc}}}{L}$, $k_7 = k_{10} = -1$, $k_8 = -K_{p,u_{dc}}$, $k_9 = -K_{i,u_{dc}}$, $k_{11} = \frac{3V_{di}(a_1+2a_2P_{0i}+a_3Q_{0i})}{2\tau_{th}}$, $k_{12} = \frac{3V_{di}(a_3P_{0i}+a_4+2a_5Q_{0i})}{2\tau_{th}}$, $k_{13} = \frac{-1}{\tau_{th}}$, $k_{14} = -\frac{3V_{di}}{2C_{dci}V_{dci}}$, $k_{15} = \frac{I_{dc}}{C_{dci}V_{dci}}$, $k_{16} = -1$.

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