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GaN-based cryogenic temperature power electronics for superconducting motors in cryo-electric aircraft

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Abstract

Climate change has spurred a shift to electric transportation, but aviation faces challenges with electric energy storage and propulsion. Cryogenically cooled superconducting motors, along with cryogenically cooled power electronics, offer a solution to increase the efficiency and power density of electric aircraft. This paper evaluates the feasibility of cryogenic power electronics by characterising new technologies (GaN, nanocrystalline) using new experimental techniques. It is found that the on resistance reductions of GaN E-high electron mobility transistors at cryogenic temperatures depend on the maximum blocking voltage of the device, and the size of the gate resistor for ohmic p-GaN devices. Different types of nanocrystalline cores are shown to vary greatly in their behaviour at cryogenic temperatures, which is measured using a modified core loss measurement circuit. Further analysis shows that the losses of a GaN based cryogenic inverter could potentially halve that of an equivalent Si based inverter.

Keywords: power electronics, gallium nitride, nanocrystalline, motor drives, cryogenic electronics

(Some figures may appear in colour only in the online journal)

1. Introduction

The widespread adoption of electric vehicles is steadily progressing, but ambiguity still surrounds the technology needed for large electric transportation, such as aircraft. This presents an issue for the aviation industry, since the anticipated growth in air traffic between now and 2050 will further increase CO_2 emissions [1]. This has been recognised by companies like Airbus, who are studying hydrogen, H_2, fuel cell powered aircraft alongside Air New Zealand [2]. It is possible that superconducting motors will be the enabling technology for commercial electric aircraft due to their excellent power densities [3–6]. However, these motors, which employ high temperature superconductors (HTS), require cryogenic cooling below a critical temperature to achieve these high power densities.

In an HTS motor driven aircraft if H_2 is used with a fuel cell it would be stored as liquid hydrogen, LH_2, for greater energy

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density. The LH_2, which would be stored below −253 °C, can cool a HTS motor below its critical temperature, so it can serve as both a coolant and fuel. Similar architectures have been proposed in [7–10], where the Airbus 'ASCEND' [7] program is creating a demonstrator for this dual purpose of LH_2. In these powertrains, LH_2 cools the HTS motor and HTS cables, and H_2 boiled off from losses is used to cool the power electronics. After use as a coolant, the H_2 can be used to generate electricity via a fuel cell. It is beneficial for the power electronics to transfer as much heat to the H_2 as possible, since fuel cells benefit from a high operating temperature [11].

In such a powertrain the temperature of the power electronics would be cryogenic (<−150 °C). At these temperatures silicon-carbide (SiC) FETs [12–14] and IGBTs [15, 16] tend to have an increase in conduction losses due to a higher $R_{DS(ON)}$ while silicon (Si) FETs [17, 18] and gallium nitride (GaN) high electron mobility transistors (HEMTs), [19–24] have reduced conduction losses. However, carrier freezeout limits the $R_{DS(ON)}$ reductions of Si devices in comparison to GaN devices. Although unaffected by carrier freezeout, the $R_{DS(ON)}$ reductions of GaN HEMTs at cryogenic temperature are strongly dependent on the technology used to achieve enhancement mode, E-HEMT, behaviour [22–24]. The reasons for these changes due to gate behaviour have not yet been explained in commercial power devices which is critical to understand in order to design converters to operate at cryogenic temperature.

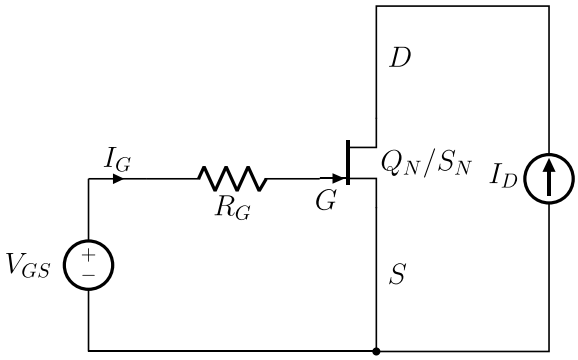
Another important point in the literature on cryogenic power electronics is the characterisation of inductor cores. In some work it was shown that ferrite [25, 26] and nanocrystalline cores [25, 27] have higher losses in liquid nitrogen (LN_2) (i.e. 77 K or −196 °C). In contrast, in other work the core losses of some nanocrystalline materials have been shown to remain unchanged when cooled from RT to −196 °C [28]. This suggests that there is variability in the core loss of these materials depending on the manufacturer, or the experimental setup. The method used to characterise these cores to date has also relied on the classical two winding method. However, nanocrystalline and ferrite cores can have a low permeability, especially at cryogenic temperatures, which can increase phase errors between measured currents and voltages. To reduce this error cancellation methods can be used [29–31], but these methods have yet to be applied to nanocrystalline cores, or cryogenic core loss characterisations.

In contrast to inductors, the behaviour of capacitors at cryogenic temperatures is generally well understood [32, 33]. Film and ceramic capacitors are the most stable with temperature, and the change in equivalent series resistance (ESR) is minimal. The capacitor characterisations to date are in agreement between different publications, which confirm that with proper selection changes in capacitor behaviour will be minimal in comparison to other components [32, 33].

Several power converters, which are designed to be operated at cryogenic temperatures have already been reported in the literature [18, 34]. In [18] Si switches were used to develop a 40 kW three level ANPC inverter, where the authors demonstrated a 30% reduction in losses at −196 °C in comparison to room temperature. However, the losses that would arise from a filter inductor are not considered, and the driver I.C.s are not in the same enclosure as the power modules. In [34] a 1 kW three level flying capacitor inverter was presented, where a ferrite core is used for its filter inductor. It was shown that although the conduction losses when operated down to −60 °C are reduced with GaN E-HEMTs, the inductor core losses become dominant with decreasing temperature. The temperature range was also limited by the driver I.C. used. A cryogenic GaN based, two level current source inverter operating at 77 K has also been proposed [35]. In this design an efficiency improvement of 0.7% was measured between RT and CT, but the reported experimental results are limited to 300 W and the total efficiency of the converter is not given. In addition, a loss distribution is not presented and the impact of using a CT inductor is not explored. Although, recently there has been an increasing number of publications in this field, these designs usually either use RT inductors, or the efficiency is low [36], or the output power is less than 1 kW [37].

A number of system level studies have also been proposed, where the operating conditions of the power electronics in a cryo-electric aircraft have been discussed [38–42]. In [38] the architecture of a cryo-electric aircraft is discussed, where the power electronics driving the HTS motor are assumed to be operating between 20 K to 120 K, and IGBTs are suggested for use as switches as they are relatively easy to drive. In [39, 40] the DC/AC inverter is assumed to operate between 40 K and 120 K over the course of a flight, and based on the Airbus ASCEND architecture [42] the power electronics efficiency, including filtering, is expected to be $\geqslant$99.41% before 2030 with a power density $\geqslant$31.35 kW kg^{-1}. In the NASA backed CHEETA programme [41] similar operating temperatures are expected for the power electronics, being cooled at 30 K to 50 K using LH_2.

Although there are many existing publications on the selection of power electronics components for cryogenic temperatures, the findings have not been translated into the efficiency benefits which are expected in a cryogenic power converter. The goal of this paper is to verify existing experimental results reported in the literature, as well as to identify and develop new methods of characterising devices at cryogenic temperatures to allow for better cryogenic power converter designs. This paper focuses on experimentally characterising the conduction loss of GaN and Si switches at cryogenic temperatures, and the core losses of nanocrystalline and ferrite cores at cryogenic temperatures. In section 2 the conduction losses are characterised using a standard circuit for static measurements of GaN and Si devices. In section 3 new characterisation methods are introduced to help explain and model the $R_{DS(ON)}$ reductions observed in the GaN E-HEMTs under test. In section 4 a core loss characterisation method called partial cancellation is modified to characterise the core losses of two different nanocrystalline cores and one ferrite core at cryogenic temperatures. In section 5 there is a brief discussion of the results in the context of a three phase motor drive, which is followed by a conclusion in section 6.



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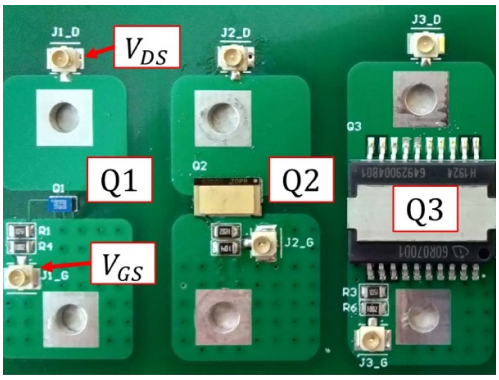

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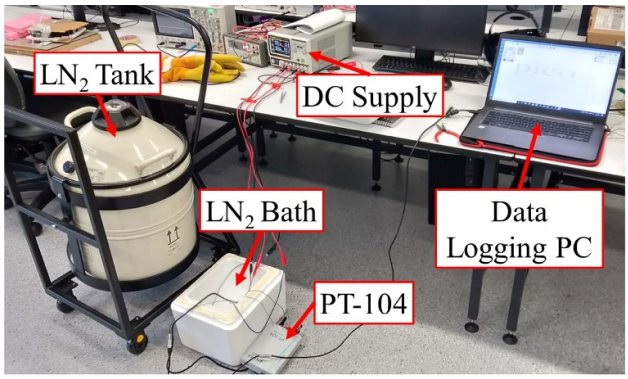

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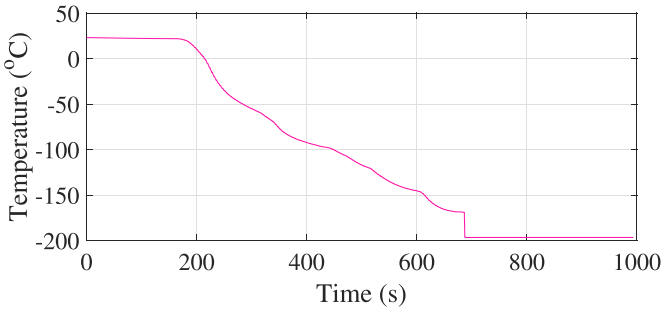
Figure 1. (a) Test circuit for measuring $R_{DS(ON)}$. (b) Example characterisation PCB showing a selection of GaN E-HEMTs. (c) Experimental setup.

2. Conduction loss of switches

The equivalent on resistance, $R_{DS(ON)}$, is used as a measure of conduction loss in a switch. To measure $R_{DS(ON)}$ at cryogenic temperatures LN_2 was used to cool each component down to −196 °C. A printed circuit board (PCB) was developed for each type of component tested and both the current through and voltage across each device was measured using Kelvin connections to evaluate $R_{DS(ON)}$. The test circuit and experimental setup are shown in figure 1. A drain current, I_D, of



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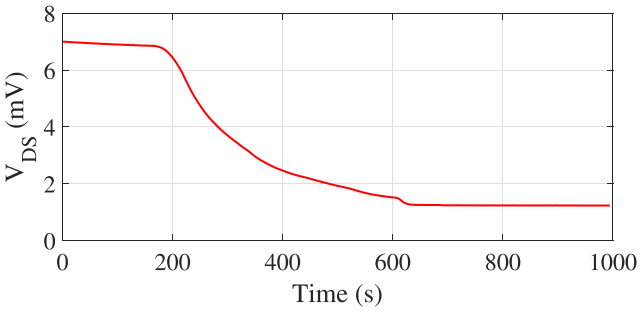

(b)

Figure 2. Example of data logging for Q2 (a) temperature and (b) drain to source voltage.

1A DC was used in each experiment, where the voltage across the device and its temperature were measured using a PT-104 data logger, which has a measurement accuracy of 15 μV and 0.015 °C respectively. I_D was selected as 1 A to ensure minimal self heating of the device under test, while simultaneously establishing a measurably large voltage drop across the device channel. Since the self heating of the devices were low during testing it meant that pulsed measurements were not necessary. *VI* curves of each device were also taken up to 20 A to ensure the $R_{DS(ON)}$ would not vary significantly with current when submerged in LN_2. Each device was cooled through LN_2 vapour over 15 min to avoid any damage that may occur due to thermal shock, which was achieved by suspending the devices above the LN_2 bath. As the devices were suspended above the LN_2 bath, their temperature as well as drain to source voltage, V_{DS}, were logged using the PT-104 data logger. A P0K1.202.3FW.B.007 temperature sensor was placed on, or as close as possible, to the thermal pad of each device to measure temperature. The data logged for temperature and V_{DS} for Q2 is shown in figures 2(a) and (b) respectively. Since the temperature of the devices decrease very slowly due to the LN_2 vapours, there is little variability in the temperature between measurements. The sampling rate of the PT-104 data logger is 10 samples per second for both temperature and V_{DS}, which allows their changes to be tracked quickly given the slow temperature decrease. There is a sudden decrease in temperature between approximately −150°C and −196°C in figure 2(a) when the sample is submerged in LN_2, but at this point the

Table 1. GaN E-HEMTs tested in LN_2.

Name	Part number	Gate technology	$R_{DS(ON)}$ (mΩ)	Maximum V_{DS}, I_D
Q1	EPC2045	Recessed Gate	7	100 V, 16 A
Q2	GS61008T	Schottky p-GaN	7	100 V, 90 A
Q3	IGOT60R070D1	Ohmic p-GaN	55	600 V, 31 A
Q4	PGA26E19BA	Ohmic p-GaN	140	600 V, 19 A
Q5	TP65H070LDG	Cascode	72	650 V, 25 A
Q6	GS66508	Schottky p-GaN	50	650 V, 30 A
Q7	GS66516	Schottky p-GaN	25	650 V, 60 A

Table 2. Si based devices tested in LN_2.

Name	Part number	Gate technology	$R_{DS(ON)}$ (mΩ)	Maximum V_{DS}, I_D
S1	IPP110N20N3	Si MOSFET	11	200 V, 88 A
S2	IPW65R115CFD7AXKSA1	Si-SJ MOSFET	115	650 V, 24 A
S3	C2M0080120D	SiC MOSFET	55	600 V, 31 A
S4	IGW25N120H3FKSA1	IGBT	800	1.2 kV, 50 A

$R_{DS(ON)}$ has already flattened out, so there is minimal change in the measurements of V_{DS} as shown in figure 2(b). A summary of each GaN E-HEMT tested is given in table 1, and Si based switches are given in table 2. Each device listed in tables 1 and 2 was thermally cycled approximately three to five times per device and it was found the $R_{DS(ON)}$ reductions remained the same across all tests.

2.1. GaN E-HEMTs

GaN HEMTs are normally on devices that conduct through a two dimension electron gas (2-DEG). This 2-DEG is formed by the piezoelectric effect due to strain between the AlGaN/GaN layers. Modifications to the gate are required to ensure the device is normally off (i.e. enhancement mode operation).

The simplified structures of commonly used gate technologies are given in figure 3, where the 2DEG is on the GaN side for all devices tested. The device Q1 uses the recessed gate structure in figure 3(a) to create a normally off behaviour by thinning the AlGaN/GaN layer beneath the gate. This reduces the piezoelectric effect and hence the 2DEG, which creates an open circuit beneath the gate until a sufficient V_{GS} is applied.

The structure of a generic p-doped GaN (p-GaN) gate is shown in figure 3(b). These devices create normally off behaviour by placing a layer of p-GaN at the gate which depletes the 2-DEG beneath the gate. If an ohmic contact is used as in Q3 and Q4, the device is turned on when the gate current (I_G) is high enough to deplete the p-GaN layer. If a Schottky contact is used as in Q2, Q6 and Q7, the turn on process is controlled by voltage rather than current.

Q5 uses cascode configuration, where an Si FET is in series with a normally on GaN HEMT as shown in figure 3(c). This means the threshold voltage is set by the Si FET making the device normally off.

To confirm the gate structure of each device given in table 1, the threshold voltage, V_{TH}, change at cryogenic temperature

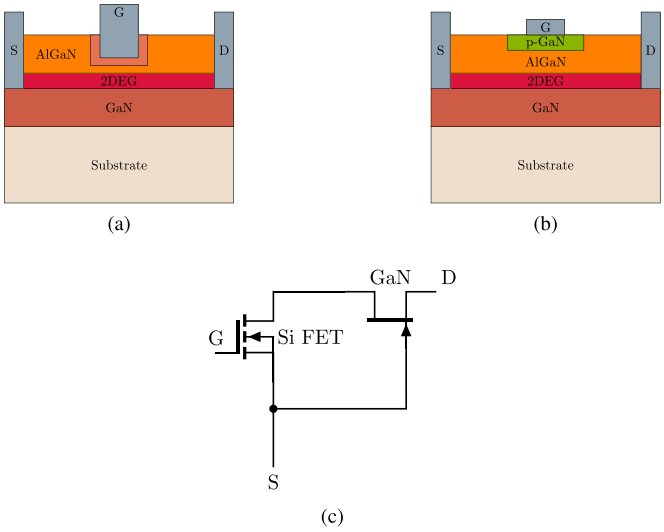

Figure 3. (a) Recessed gate lateral structure, (b) ohmic p-GaN and Schottky p-GaN lateral structure, (c) cascode device internal circuit.

was measured and compared to those from [22] for devices from the same manufacturer with similar max V_{DS}, I_D ratings. A selection of V_{TH} measurements are shown in figure 4, and the change in V_{TH} compared to the results of [22] are shown in table 3. It can be seen that trends in gate behaviour are very similar, with cascode devices, Q5, and ohmic p-GaN devices, Q3, showing an increase in V_{TH} at −196 °C, and the Schottky p-GaN devices, Q6 and Q7, showing a decrease in V_{TH} at −196 °C. The ohmic p-GaN and cascode devices can be differentiated based on the size of V_{TH}, where a cascode device has a large value of V_{TH} due to the series Si MOSFET controlling the device turn on.

For each GaN E-HEMT in table 1 its normalised $R_{DS(ON)}$ change with temperature is shown in figure 5. The impact of gate technology on cryogenic performance is clear. Devices using an ohmic p-GaN gate had a parabolic shaped change in

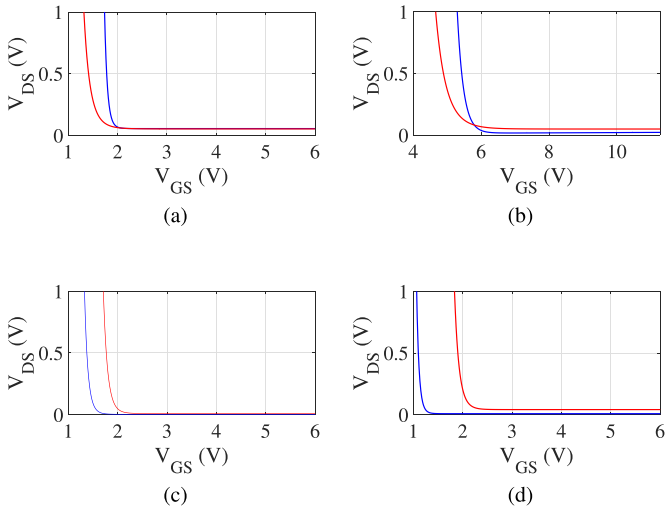

Figure 4. Threshold voltages of GaNs under test (a) Q3, (b) Q5, (c) Q6, (d) Q7.

Table 3. GaN threshold voltage change in LN_2.

Device	V_{TH} (25 °C)	V_{TH} (−196 °C)	ΔV_{TH}	ΔV_{TH}in [22]
Q3	1.6	1.9	0.3	0.1
Q5	5.5	5.9	0.4	1.1
Q6	2	1.6	−0.4	−0.9
Q7	2	1.1	−0.9	−0.9

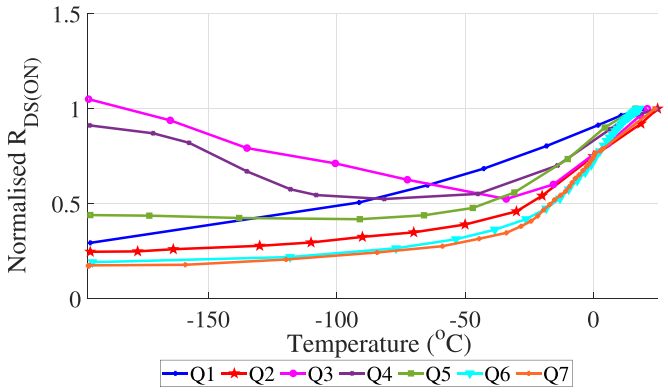

Figure 5. GaN E-HEMT normalised $R_{DS(ON)}$ change with temperature.

$R_{DS(ON)}$ with decreasing temperature, showing minimal or no reduction in $R_{DS(ON)}$ at −196 °C. This is likely due to changes in the p-GaN layer with decreasing temperature, since in other work the threshold voltage of Schottky p-GaN gates has been noted to increase [22]. The cascode E-HEMT followed a similar trend, although there is still a net $R_{DS(ON)}$ reduction of approximately 50%. The initial decrease in $R_{DS(ON)}$ is due to the GaN HEMT, but carrier freezeout in the series Si FET begins to negate these reductions as temperature decreases further. It is clear the most promising devices for applications in cryogenic environments use recessed gate and Schottky p-GaN gates.

The normalised $R_{DS(ON)}$ of the Schottky p-GaN device tested in [22] (GS1) is 0.42 at 200 K. In figure 5 at 200 K the normalised $R_{DS(ON)}$ of Q2 reaches 0.35, Q6 reaches 0.27, and Q7 reaches 0.25. Comparing all of these results shows that the $R_{DS(ON)}$ of Schottky p-GaN devices depends greatly upon the specifications of the device under test, as all of these devices are from the same manufacturer and use the same gate type. The current and voltage ratings of these devices have an influence on the rate of $R_{DS(ON)}$ reductions, as they change the area and length of the 2DEG. This will be discussed further in section 3.

Considering the ohmic p-GaN devices in [22], both devices tested have a normalised $R_{DS(ON)}$ of ≈0.5 at 77 K, whereas in this paper the normalised $R_{DS(ON)}$ is ≈1 at 77 K. This difference is attributed to an increase in the internal resistance of the ohmic gate, R_P, which causes the sizing of the gate resistor, R_G, as shown in figure 1(a), to have a greater influence on the device turn on process. This point is discussed further in section 3, where the ohmic p-GaN devices are tested with varying gate sizes, and it is found that the smallest value of R_G achieves the greatest $R_{DS(ON)}$ reduction in LN_2.

Three samples of devices with the most promising gate technologies, Q1 and Q7, were tested to gauge the variability in $R_{DS(ON)}$ reductions at cryogenic temperatures, as shown in figure 6. For Q1 the spread of $R_{DS(ON)}$ in LN_2 is lower than at RT, while for Q7 the spread of $R_{DS(ON)}$ in LN_2 is slightly larger than at RT. In both cases the variation of $R_{DS(ON)}$ and its reductions with temperature are minimal. This suggests that variations between GaN devices will likely not overshadow

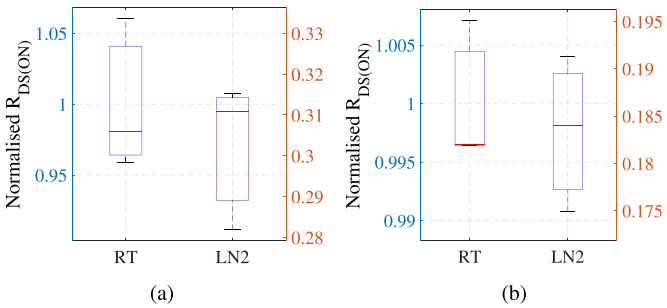

Figure 6. Variability of Q1 and Q7 $R_{DS(ON)}$ reduction. (a) Q1. (b) Q7.

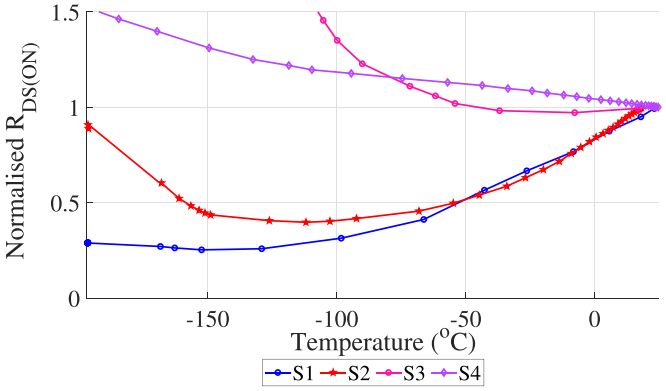

Figure 7. Normalised $R_{DS(ON)}$ change with temperature for Si based switches.

the trends in gate behaviour shown in figure 5, and the maximum possible $R_{DS(ON)}$ reduction with temperature will not significantly vary from device to device.

2.2. IGBT, Si, and SiC devices

The normalised $R_{DS(ON)}$ change with temperature for the Si devices listed in table 2 is shown in figure 7. The Si MOSFET, S1, is the best performing device, as its LN_2 $R_{DS(ON)}$ is only approximately 30% of its RT value. The minimum $R_{DS(ON)}$ of S1 is reached at approximately −150 °C, where it is 25% of its RT value after this point it increases, which is possibly due to carrier freezeout. Although the Si-superjunction (SJ) MOSFET, S2, has good performance at higher temperatures, there is a significant increase in $R_{DS(ON)}$ below approximately 150 °C. The SiC device, S3, is clearly not optimal for cryogenic environments either, since it has far higher conduction losses when compared to its RT $R_{DS(ON)}$. Although the IGBT device, S4, has increased conduction losses, it is not to the same extent shown with S3.

For the Si MOSFET that was tested it was found that its $R_{DS(ON)}$ did not increase appreciably once it reached −196 °C, which is in agreement with the existing literature [17, 43]. Considering the Si SJ device, S2, its $R_{DS(ON)}$ increases significantly below −150 °C, which has not been observed in existing literature [18]. A possibility for this behaviour is that S2 is unable to fully turn on due to an increase in V_{TH} with reducing temperatures, since the $R_{DS(ON)}$ increase observed in this

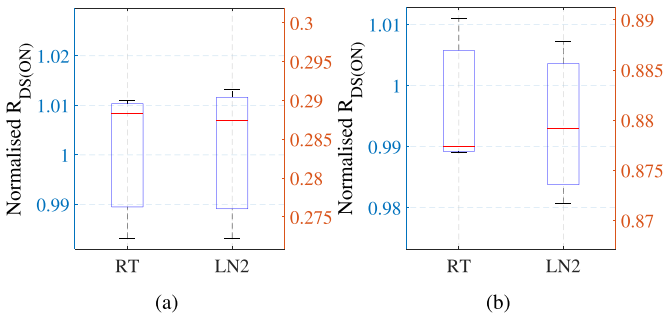

Figure 8. Variability of S1 and S2 $R_{DS(ON)}$ reduction. (a) S1. (b) S2.

device is well above other Si SJ devices that have been characterised in the literature [18, 43].

Since S1 and S2 were the best of the devices in figure 7, their variations in $R_{DS(ON)}$ reductions are shown in figure 8 as was done with the GaN E-HEMTs. In comparison to the GaN devices in figures 6, S1 and S2 have even lower variability. The maximum deviation from the median in either case is only ≈ 1%, where as this was as high as 6% with Q1. All of the devices in both figures 6 and 8 shows that the spread of variability of $R_{DS(ON)}$ between RT and LN_2 remains roughly the same.

3. GaN E-HEMT gate behaviour

The results in figure 5 show that with certain GaN E-HEMTs significant $R_{DS(ON)}$ reductions are possible in LN_2, but the reason for why this varies so much between different gates requires further investigation. A breakdown of the measured $R_{DS(ON)}$ for a generic p-GaN E-HEMT is shown in figure 9. The total resistance can be expressed as,

$$R_{DS(ON)} = R_{CT} + R_{2DEG} + R_{CH} \tag{1}$$

where R_{CT} is the total contact resistance, R_{2DEG} is the combined resistance of the 2-DEG from the gate to the drain and gate to the source, and R_{CH} is the resistance directly beneath the gate. R_{CT} can be expressed as the sum of source contact resistance, R_{CS} and the drain contact resistance, R_{CD},

$$R_{CT} = R_{CS} + R_{CD} \tag{2}$$

while R_{2DEG} can be expressed as the sum of source to gate 2-DEG resistance, R_{2DEGS}, and the drain to gate 2-DEG resistance, R_{2DEGD},

$$R_{2DEG} = R_{2DEGD} + R_{2DEGS}. \tag{3}$$

As defined in [44], R_{CH} is given by,

$$R_{CH} = \frac{L_G}{\mu_i n_i q W} \tag{4}$$

where L_G is the gate length, μ_i is the electron mobility, n_i is the 2DEG density and W is the width of the channel, while q is the electron charge. The subscript i denotes the temperature at

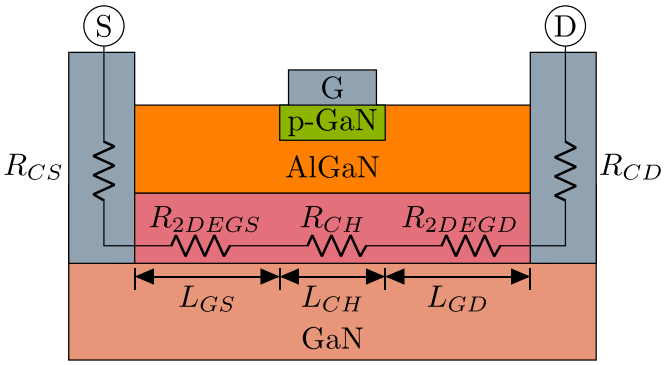

Figure 9. Equivalent circuit for total on resistance measurements.

which R_{CH} is evaluated. In this equation $\mu_i n_i$ is also a function of the gate–source voltage, V_{GS}, and therefore,

$$\frac{L_G}{\mu_i n_i q W} = k_i \Delta V \tag{5}$$

where k_i is a fitting parameter, and $\Delta V = V_{GS} - V_{GS(th)}$. This means that if V_{GS} is varied in small increments beyond the gate-source threshold voltage, $V_{GS(th)}$, then R_{CH} can be found, since it can be assumed that R_{2DEG} and R_{CT} are mostly unaffected by V_{GS}. Linear regression can be used to find k_i by fitting a model to measurements of $R_{DS(ON)}$ against $1/\Delta V$ when the device under test is fully turned on. The gradient of the fitted linear regression would be the inverse of k_i for the device under test at a specific temperature. The ratio of k_i at two different temperatures, will then be,

$$\frac{k_1}{k_2} = \frac{\mu_1 n_1}{\mu_2 n_2} = \kappa_m \tag{6}$$

If it is assumed that when fully turned on μ_i and n_i are uniform between R_{CH} and R_{2DEG} then,

$$R_{2DEG} = \frac{L_{GS} + L_{GD}}{\mu_i n_i q W}. \tag{7}$$

Here L_{GS} and L_{GD} are as shown in figure 9. Under these assumptions κ_m should also represent the change in R_{2DEG} with temperature. The y-axis intercept of a $R_{DS(ON)}$ vs $1/\Delta V$ curve, $R_{DS(intercept)_i}$, represents $R_{CT} + R_{2DEG}$ and therefore,

$$\frac{R_{CT_1} + R_{2DEG_1}}{R_{CT_2} + R_{2DEG_2}} = \frac{R_{DS(intercept)_1}}{R_{DS(intercept)_2}} = \kappa_r. \tag{8}$$

By comparing κ_r to κ_m it is now possible to further investigate the total $R_{DS(ON)}$ change. If $\kappa_r \approx \kappa_m$ then it can be inferred that R_{CT} is small. In contrast, if $\kappa_r < \kappa_m$ then it follows that R_{CT} is a noticeable part of the total $R_{DS(ON)}$. This method cannot predict the exact change in n_i and μ_i, but it is useful for understanding device trends and behaviour between room and cryogenic temperatures, which will assist in device selection.

The experimentally measured $R_{DS(ON)}$ of Q7 and Q2 at both RT and −196 °C are shown in figures 10(a) and (b), respectively. Based on the linear regression fits shown, for Q7 the

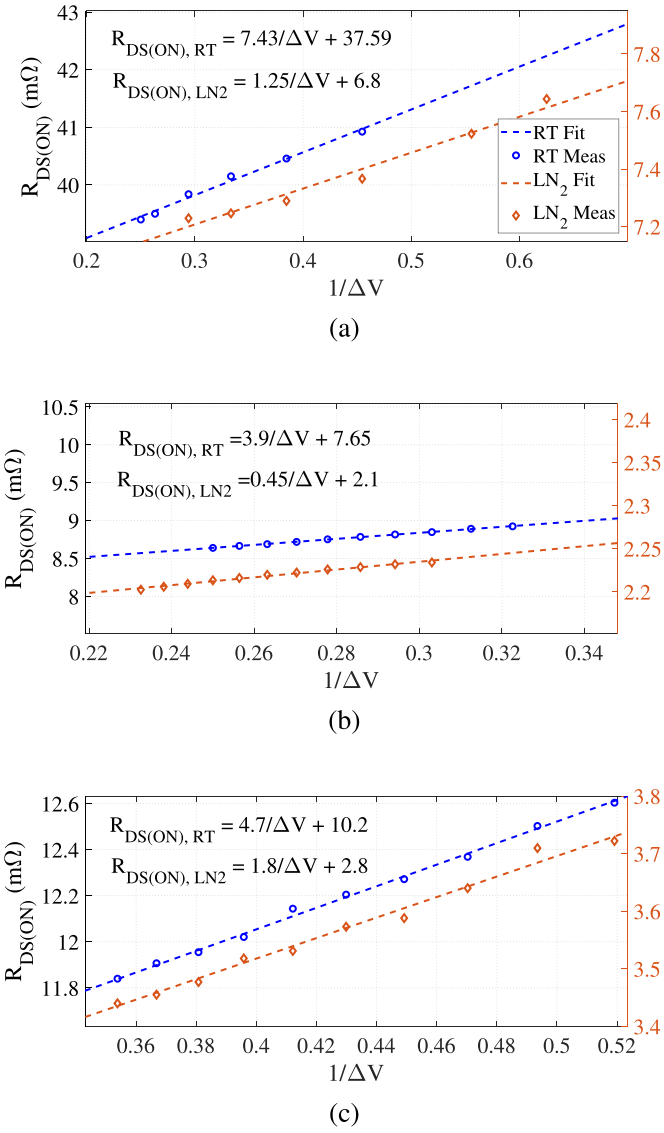

Figure 10. Model fit to $R_{DS(ON)}$ measurements of different GaN E-HEMTs. (a) Q7. (b) Q2. (c) Q1.

condition is $\kappa_r \approx \kappa_m$, while for Q2 the condition is $\kappa_r < \kappa_m$. These devices are both from the same manufacturer and use a Schottky p-GaN gate. So this difference is hypothesised to occur due to differences in maximum drain-source blocking voltage, $V_{(BL)DSS}$, between the two devices. Commercially available GaN E-HEMTs use a lateral structure, where high $V_{(BL)DSS}$ ratings are achieved by lengthening the 2-DEG to separate the drain and source pins. For a device with higher $V_{(BL)DSS}$, R_{CH} will then be large relative to R_{CT}. This means that a larger $R_{DS(ON)}$ reduction can achieved using a single HV GaN E-HEMT, rather than multiple LV devices connected in series. This matches the trends shown in figure 5.

Applying this method to Q1 also provides insight into the behaviour of the recessed gate device. The linear regression fit to experimental $R_{DS(ON)}$ measurements of Q1 is shown in figure 10(c). In contrast to Q2 and Q7, the condition is

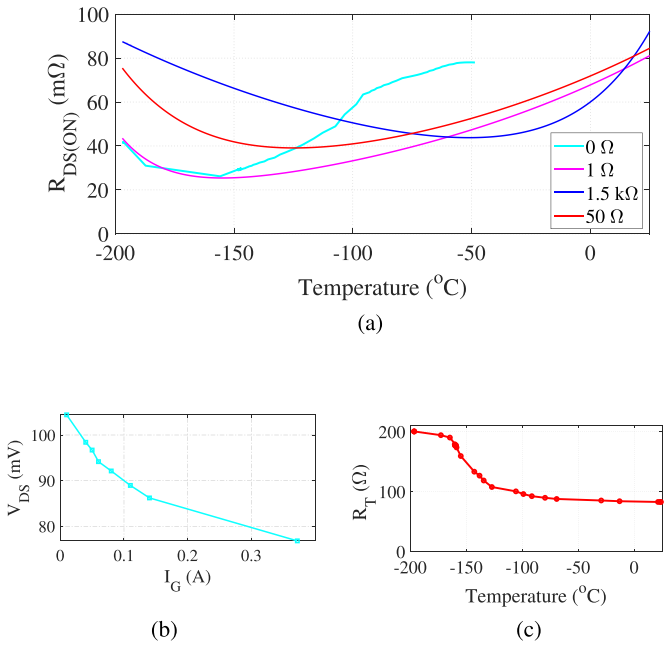

Figure 11. (a) Change in $R_{DS(ON)}$ with T_c & R_G. (b) Change in V_{DS} with I_G at $R_G = 0\Omega$, $T_c = -196^{\circ}$C. (c) Increase of R_T with T_c at $R_G = 50\Omega$.

$\kappa_r > \kappa_m$. Since the region of 2-DEG is thinned beneath the gate of Q1 this means the resistance of this region is high relative to the rest of the 2-DEG. This explains why Q1 has a lower $R_{DS(ON)}$ reduction than Q2 even though they have similar $V_{(BL)DSS}$ ratings.

The above method cannot be applied to Q3 and Q4 due to the change in turn on process observed with ohmic p-GaN gates in figure 5. The unique behaviour of Q3 and Q4 can instead be supported by investigating the $R_{DS(ON)}$ breakdown of figure 9 in relation to the total gate resistance (R_{GT}). R_{GT} can be thought of as a resistance formed by an external gate resistor R_G and the resistance presented by the ohmic p-GaN layer, R_P,

$$R_{GT} = R_G + R_P(T_c) \tag{9}$$

R_P is dependent on temperature, and the turn on of the device is dependent on the current through R_P. If R_P increases then a higher V_{GS} is needed to generate the desired I_G. This makes it difficult to reach the threshold current, $I_{G(th)}$, which in turn prevents the device from turning on and causes $R_{DS(ON)}$ to increase. Although Schottky p-GaN devices would suffer from similar low temperature effects, they are voltage controlled rather than current controlled. This means that the effects of an increased R_P manifest in the form of an increased $V_{GS(th)}$ in Schottky p-GaN gates, while the I_G requirements are negligible.

Results supporting this theory are shown in figure 11(a). The curves illustrate the change in $R_{DS(ON)}$ with temperature for Q3 at different values of R_G. When the device is cooled, if R_G is large then I_G is not high enough to overcome $I_{G(th)}$. A net $R_{DS(ON)}$ reduction of $\approx 50\%$ can be achieved at about -160 °C if R_G is lowered to 1Ω. Setting $R_G = 0\Omega$ demonstrates similar reductions, although the relationship with temperature is difficult to measure due to self heating from the high gate current. Importantly these effects are not observed in the Schottky p-GaN devices of figure 5, where since the value of V_{GS} is much higher than $V_{GS(th)}$ in the first place it means the increase in $V_{GS(th)}$ cannot be observed in the change in $R_{DS(ON)}$. In figure 11(b) the increase in I_G for Q3 at -196 °C and its relationship to $V_{DS(ON)}$ is shown. The increase of R_P against temperature is measured directly in figure 11(c) when $V_{GS} = 6V$ and $R_G = 50\Omega$. This shows that R_P is effectively doubled at -196 °C, and a sharp increase in R_P occurs at ≈ -125 °C. These increases in R_P and the increased $I_{G(th)}$ shown in figure 11(b) are hypothesised to occur due to carrier freezeout in the p-GaN layer, however further investigation is required to pinpoint the root cause of failure.

These results make it clear that ohmic p-GaN gates are not viable for use at cryogenic temperatures. Currently only minimal reductions in $R_{DS(ON)}$ are possible, and to do this a high I_G is required, which will cause significant losses at the gate.

Comparing all of the devices shows the optimal GaN E-HEMT technology to use at cryogenic temperatures are Schottky p-GaNs. This is because they are available in with higher $V_{(BL)DSS}$ ratings and not limited by R_{CH}, which is why they had the most significant $R_{DS(ON)}$ reduction of all GaN E-HEMTs tested.

4. Inductors

The conventional two winding method is typically used to characterise core loss in magnetic cores [27]. In this method, the magnetic field strength (H) in a core under investigation is calculated by exciting a winding that has N_1 number of turns with a current $i_1(t)$ since,

$$H = \frac{N_1 i_1(t)}{l_m}. \tag{10}$$

Here l_m is the magnetic path length of the core under investigation. Magnetic flux density (B) in this core is found by measuring the voltage $v_2(t)$ induced across a second winding that has N_2 number of turns over a single time period T_p since,

$$B = \frac{1}{N_2 A_e} \int_0^{T_p} v_2(t)\,\mathrm{d}t. \tag{11}$$

Here A_e is the effective cross-sectional area of the core. The energy lost in the core can then be found by integrating the area within the BH curve,

$$E = \oint H\,\mathrm{d}B. \tag{12}$$

This assumes the current and voltage measurements will have no phase error in them. In a practical setup this is impossible to avoid, since component interconnections, probes, and the shunt resistor used to measure $i_1(t)$ will all have parasitic inductances. The error in power measurement that results from this phase error is given as [30],

$$\Delta = \tan(\phi_i)\Delta\phi_p \tag{13}$$

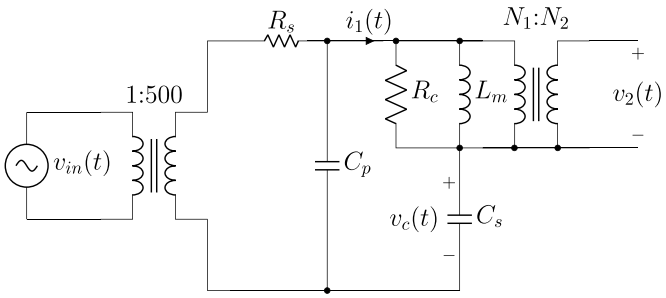

Figure 12. Equivalent circuit of partial capacitive cancellation method.

where $\Delta\phi_p$ is the phase discrepancy caused by the parasitic inductance of the measurement setup, and ϕ_i is the phase difference between $v_2(t)$ and $i_1(t)$. Inspection of (13) shows that when the quality factor of the core under test is high, then $\Delta\phi_p$ will be amplified.

To account for this error, the partial cancellation method proposed in [30] can be used. However, this method was developed for ferrite cores and is difficult to apply to nanocrystalline cores due to their significantly high relative permeabilities, μ_r. The μ_r values of nanocrystalline are in the range of 10 000–100 000, leading to a very high inductance, L_m, which needs to be partially cancelled using C_s. The resulting reactance of the partially cancelled winding is very high, and cannot be easily driven through a power amplifier to generate the required $i_1(t)$. Therefore, this paper proposes a modification, where by the partially cancelled winding is parallel compensated using the capacitor C_p as shown in figure 12. C_p is chosen such that,

$$C_p \approx \frac{C_s}{1+\omega^2 L_m C_s}. \tag{14}$$

As shown by $v_{\text{in}}(t)$ in figure 12, a power amplifier is used to excite a transformer which then steps up the voltage to generate the required excitation current $i_1(t)$ through L_m. The purpose of the shunt resistor, R_s, is to increase the power factor seen by $v_{\text{in}}(t)$ The core under test was placed inside an LN_2 container as shown by figure 13 to evaluate core losses at −196 °C. The cores under test are listed in table 4. The voltage across the sense winding, $v_2(t)$, and the cancellation capacitor, $v_c(t)$, is measured using Keysight N2790A differential probes. The current through the core, $i_1(t)$, is measured using a Keysight N2780A current probe. The core loss calculation still follows the partial cancellation method [30], where the total core loss measured is given by,

$$P_{\text{core}} + \Delta P_{\text{core}} = P_{\text{core}} + V_2 \sin(\phi_i) I_1 \Delta\phi_p \tag{15}$$

where P_{core} is the actual core loss, and ΔP_{core} is the error in core loss measurement. The power dissipated in C_s is given by,

$$P_{C_s} = -V_C I_1 \Delta\phi_p \tag{16}$$

where the measured P_{C_s} represents the error in power measurement across C_s. By comparing (15) to (16), it can be seen that

Table 4. Inductor cores tested in LN_2.

Name	Core type	Rated $B_{\max}$
L1	Nanocrystalline	1.25
L2	Nanocrystalline	0.85
L3	Ferrite	0.3

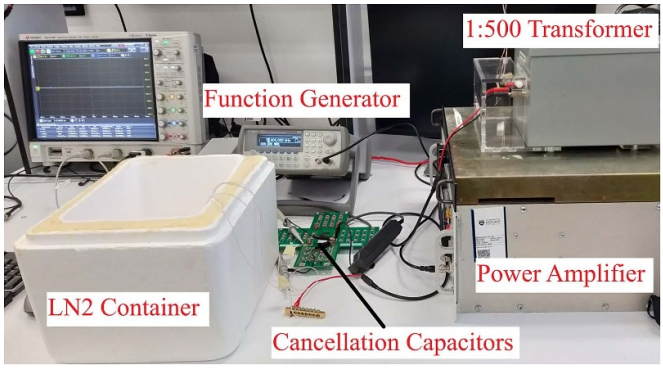

Figure 13. Experimental setup for core loss characterisation.

ΔP_{core} is proportional to P_{C_s}. The constant of proportionality between the two terms, k, is given as

$$k = \frac{V_C}{V_2 \sin(\phi_i)}. \tag{17}$$

Since ϕ_i cannot be measured, a small phase shift, ϕ_p', is introduced to the measurements of current $i_1(t)$, which results in $i_1(t)'$, to calculate k using,

$$k = \frac{\int_0^T v_C i_1(t)'\,\mathrm{d}t - \int_0^T v_C i_1(t)\,\mathrm{d}t}{\int_0^T v_S i_1(t)'\,\mathrm{d}t - \int_0^T v_S i_1(t)\,\mathrm{d}t}. \tag{18}$$

The phase shift of ϕ_p' is introduced to the current waveform using a MATLAB program, which is also used to compute the core losses measured using partial cancellation. For further information a detailed derivation of k can be found in a prior paper which covers the partial cancellation method [30].

The permeability changes measured for three cores, referred to as L1, L2 and L3, are shown in figure 14 over a range of frequencies. At lower frequencies the nanocrystalline cores, L1 and L2, have a similar change μ_r, however at high frequencies the difference in μ_r is much lower for L2. Both of the nanocrystalline cores maintain their μ_r better than the ferrite core, L3, when submerged in LN_2. The *BH* curves at 25 °C and −196 °C are shown in figure 15. For all of the cores the saturation flux density (B_{sat}) is increased which means they can operate at higher currents. It can also be observed that the area of the *BH* curve for L2 and L3 is noticeably larger at −196 °C compared to 25 °C, which suggests that these cores will have higher losses at cryogenic temperatures. The difference in core loss power density (P_v) is shown in figure 16 at 10 kHz. Clearly L1 has the least change in P_v compared to L2 and L3. In all cases the P_v at −196 °C stays close to the 25 °C results at high values of B_{peak}. This is because of the increase in B_{sat},

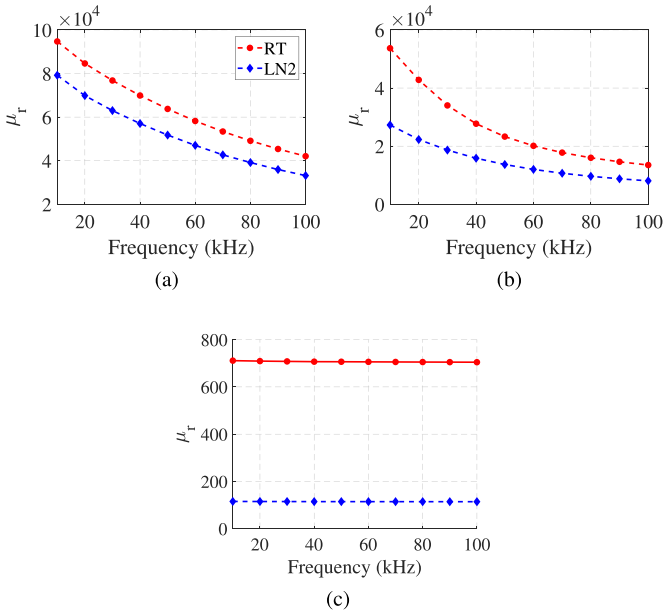

Figure 14. μ_r change of (a) L1 (b) L2 (c) L3 between RT and LN_2.

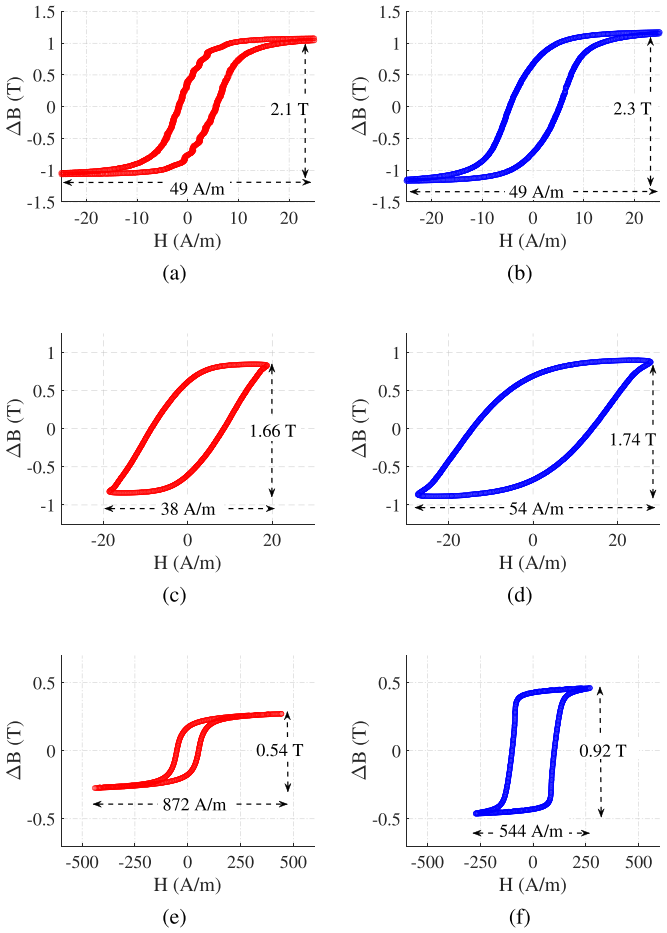

Figure 15. *BH* curves. (a) L1 RT. (b) L1 LN_2. (c) L2 RT. (d) L2 LN_2. (e) L3 RT. (d) L3 LN_2.

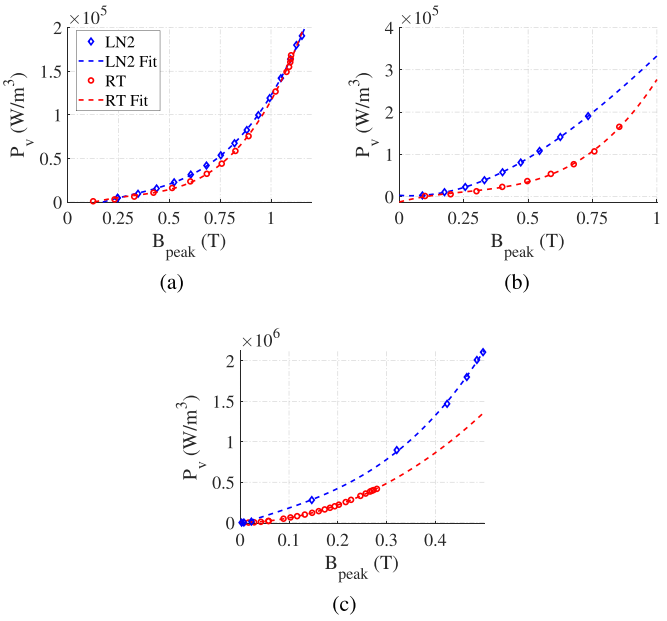

Figure 16. Core loss comparison between RT and LN_2. (a) L1. (b) L2. (c) L3.

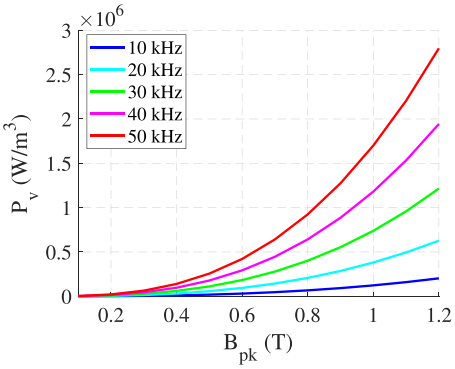

Figure 17. Steinmetz fit of L1 at different frequencies.

Table 5. Steinmetz parameters of nanocrystalline cores.

Parameter	L1 (25 °C)	L2 (25 °C)	L1 (−196 °C)	L2 (−196 °C)
k	0.035 11	0.095 34	0.036 45	0.093 94
α	1.63	1.605	1.632	1.638
β	3.01	2.294	2.732	2.153

which means operating inductors under cryogenic conditions is possible at higher flux densities compared to at 25 °C.

Since L1 was the best performing core, measurements of its core losses up to 50 kHz were fit to the Steinmetz equation, which is of the form,

$$P_v = kf^{\alpha}B^{\beta}. \tag{19}$$

The plot shown in figure 17 summarises how P_v of L1 changes with B and f. This shows that as frequency increases the core losses will begin to increase significantly. The 25 °C and −196 °C Steinmetz parameters for both L1 and L2 are shown in table 5. At −196 °C the α for L1 remains the same while for L2 it increases, from which it can be inferred that L2 will have more severe core losses at high frequencies at −196 °C.

5. Theoretical motor drive case study

Using the experimental component characterisations presented in the preceding sections, the switch losses of a power converter at cryogenic temperatures can be theoretically assessed. For this purpose, a 500 kW three-phase inverter in an HTS motor powertrain is used as case study, which is illustrated in figure 18. The goal of this analysis is to compare the benefit of using GaN switches in a cryogenically cooled inverter, to a Si based room temperature inverter. As given in table 6, a

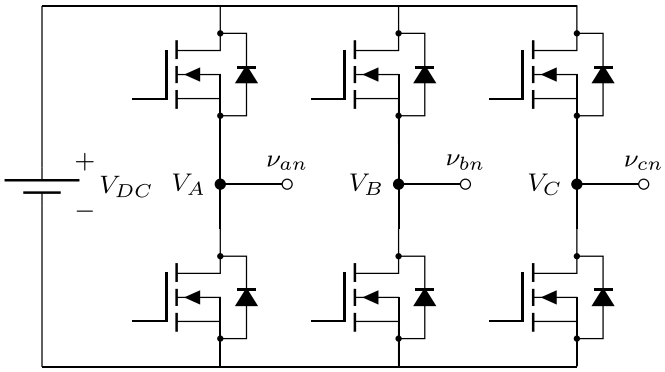

Figure 18. Three phase inverter considered in loss analysis.

Table 6. Cryogenic three phase inverter specifications.

Specification	Case 1	Case 2
Switch	S1	Q7
N_{series}	6	2
N_{parallel}	8	8

GaN and an Si inverter converter are compared as 'Case 1' and 'Case 2', respectively, since IGBTs and SiC devices do not work well under cryogenic conditions. The components selected for the case study are listed in table 5. The switching losses are estimated using datasheet values and changes in V_{TH} measured in section 3.

The inverter is assumed to be operating with a DC bus voltage, V_{DC}, of 1 kV, at a switching frequency, f_s, of 50 kHz to generate a 1 kHz fundamental frequency, f_o. To reach the desired blocking voltage, V_{DC}, the $R_{\text{DS(ON)}}$ of the switches are scaled based on their maximum V_{DS} as per,

$$N_{\text{series}} > \frac{V_{\text{DC}}}{V_{\text{DS(MAX)}}} \tag{20}$$

where N_{series} is the number of switches needed in series to reach the desired V_{DC}. Similarly, to meet the output current requirement, I_o, of the inverter, $R_{\text{DS(ON)}}$ is scaled based on each switches maximum I_{DS} as per,

$$N_{\text{parallel}} > \frac{I_{\text{DS}}}{I_{\text{DS(MAX)}}} \tag{21}$$

where N_{parallel} is the number of parallel switches needed. The scaled resistance for an effective switch is calculated using,

$$R_{\text{DS(Total)}} = \frac{N_{\text{series}}}{N_{\text{parallel}}} \cdot R_{\text{DS(ON)}}. \tag{22}$$

The conduction losses are then given by,

$$P_{\text{cond}} = R_T \cdot I^2_{o,\text{RMS}}. \tag{23}$$

Using the approach taken in [34], the switching losses are also estimated.

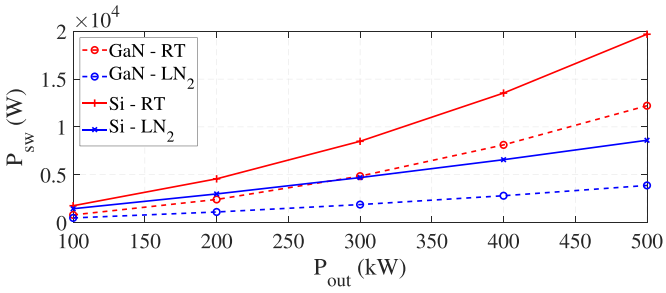

Figure 19. Switch losses in GaN and Si based converter at different temperatures.

Based on (20)–(23), estimates of the total switch loss, P_{sw}, are shown in figure 19 for Cases 1 and 2 respectively, considering the inverter shown in figure 18. Clearly the GaN based inverter has far less losses compared to the Silicon MOSFET inverter, which is due to lower switching and conduction losses in the GaN inverter at both RT and LN_2. However, in practice connecting the GaN devices in series and parallel will present significant challenges, which is one of the main factors complicating their immediate use within an HTS motor drive. In addition to reduced switch losses, the reduced losses from a nanocrystalline core would also be a significant improvement upon existing attempts at cryogenic filter inductors [28]. However, further work needs to be done to identify the filtering requirements for an HTS motor, as well as requirements for scaling the filter inductors to a high power level.

6. Conclusion

In this article, a selection of switches, and magnetic cores were evaluated in a cryogenic environment. It was shown that GaN E-HEMTs using Schottky p-GaN gates, and Si FETs have the lowest conduction losses in LN_2. Furthermore, new experimental techniques were introduced which allowed for a more in depth understanding of the gate behaviour of GaN E-HEMTs in LN_2, showing that $R_{\text{DS(ON)}}$ reductions with temperature depend on the $V_{\text{(BL)DSS}}$ of the switch. The behaviour of ohmic p-GaN devices were also studied further than done before in previous work, where it was shown the $R_{\text{DS(ON)}}$ in LN_2 can be reduced by using a smaller value of R_G, although this leads to too large of an I_{G} to be feasible in practice. An improved measurement circuit was also introduced for core loss characterisation, which allowed for magnetic materials to be characterised in LN_2 without phase errors that would have impacted the accuracy of previous cryogenic core loss measurements. The methods presented in this paper provide new and useful insights into the selection of components for cryogenic power electronics. This was illustrated through a theoretical case study of switch losses in a three phase inverter, where the losses of GaN based cryogenic inverter were half that of an equivalent cryogenic Si MOSFET based inverter.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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