# Low-Loss Bidirectional Solid-State Circuit Breakers with Reliable Breaking Capability for Protecting DC Microgrids

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***Abstract*—Silicon-controlled rectifier-based dc solid-state circuit breakers (SCR-SSCBs) have received an increased attention for their ease of control and high efficiency, but their considerable conduction losses remain a major disadvantage. This paper presents a new bidirectional SCR-SSCB topology which reduces the conduction losses by ~50%, with the loss reduction attributed to an inductor being eliminated from the main circuit during normal operation. This is achieved by conducting current through one semiconductor switch instead of two as in conventional devices. In addition, the presented topology enhances the reliability of protection by enabling a controlled interruption of short-circuit faults, in which fault interruption is not affected by the parameters of external systems to which the circuit breaker is connected to. A second topology which reduces the size of the capacitors in the commutating circuit is also introduced. A detailed analysis of the operating principle of the two novel topologies is presented. Recommendations supported by mathematical modeling are provided for selecting the relevant components of the devices. The performance of the two topologies was verified through simulation and experimental tests.**

***Index Terms*—Bidirectional circuit breaker, dc circuit breaker, dc protection, SCR-based circuit breaker, dc fault isolation**.

## I. INTRODUCTION

DC microgrids have become attractive alternatives for future power system architectures. However, their protection against faults is challenging due to the lack of natural zero-crossing currents and this has been identified as a major barrier preventing the widescale deployment of dc power systems. The development of emerging dc circuit breakers (DCCBs) for the fast interruption of dc faults is thus a major requirement for the protection of dc microgrids [1].

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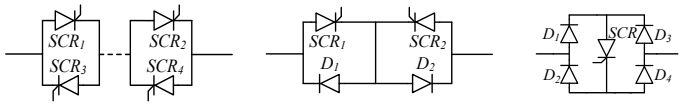
DCCBs are typically categorized as mechanical CBs, hybrid CBs, and solid-state CBs (SSCBs). SSCBs with power electronic components have attracted more attention than mechanical and hybrid CBs due to their faster response, lighter weight and volume, and an arc-free interruption of the fault current. SSCBs are being increasingly used in low-voltage and medium-voltage distribution systems such as dc data centers [2], marine power systems [3], aircraft power systems [4], photovoltaic systems [5], and railway systems [6]. SSCBs deploy power semiconductor switches in series, such as insulated-gate bipolar transistors (IGBTs), metal-oxide-semiconductor field-effect transistors (MOSFETs), and silicon-controlled rectifiers (SCRs). This enables the interruption and isolation of short-circuit fault currents. However, the on-state losses, particularly for bidirectional devices where the number of power semiconductor elements doubles, are still very high. It is of great interest to reduce the losses caused by power electronic components under regular operating conditions.

Generally, SCRs have lower on-state losses than MOSFETs when the values of current are high. SCRs can also withstand higher voltages and higher pulse currents. SCRs are forced turn-off components where the turn off is generally achieved by using LC resonant circuits; this simplifies the configuration and control circuitry of SCR-based dc SSCBs (SCR-SSCB). Among these devices, Z-source SSCBs (Z-SSCBs) have gained significant attention due to their structural simplicity, quick response time, and ability to interrupt and isolate short-circuit faults automatically without the use of additional detection circuits [7].

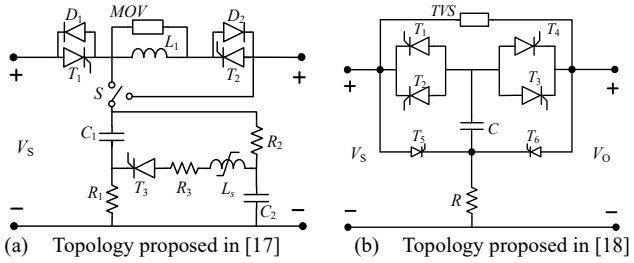
The Z-SSCB was first presented in [8]. This device creates a zero-crossing current at the SCR by using an LC resonant circuit, allowing the SCR to be turned off for blocking the fault. Since then, several unidirectional Z-SSCB topologies have been proposed [9]-[12], all of which share a similar working principle. A focus has been placed in optimizing the structure and function of the device to have a common ground, smaller reflected currents to the source, lighter weight, and smaller volume. Bidirectional Z-SSCBs were also introduced to protect dc distribution systems where power flows bidirectionally [13]-[16]. The majority of the bidirectional devices incorporate reverse parallel SCRs and diodes onto unidirectional Z-SSCBs to achieve bidirectionality, as shown in Fig. 1.

Despite their advantages, Z-SSCBs have several drawbacks. Firstly, they can only automatically turn off in the event of a fast fault current rise due to a small fault impedance. The turn

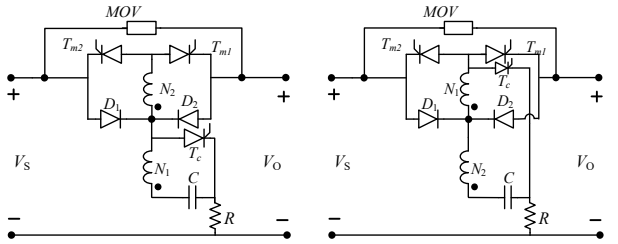



(a) Anti-parallel 1 (b) Anti-parallel 2 (c) Bridge

**Fig. 1.** Connection of power electronic devices for bidirectional Z-SSCBs.




(a) Topology proposed in [17] (b) Topology proposed in [18]




(c) Topology proposed in [19] (d) Topology proposed in [20]

**Fig. 2.** Active SCR-SSCB topologies proposed in [17]-[20].

off process could fail when faults with a large impedance occur. Hence, their performance is easily influenced by parameters of the external system that is protected by the Z-SSCBs, such as line inductance and load impedance [7]. This further reduces the reliability of the protection. Secondly, bidirectional Z-SSCBs have high on-state losses resulting from the use of two semiconductor power electronic components in the circuit where current flows under non-faulted operating conditions.

To improve the reliability and controllability of Z-SSCBs, two bidirectional SCR-SSCB topologies with active turn-off functions were presented in [17], [18]. These are shown in Figs. 2(a)-(b). Their active turn-off is achieved by comparing the detected currents with a preset threshold via either analogue or digital protection units. This allows the devices to protect against faults with a wider range of impedance and, hence, reduces the impact of external system parameters.

Two bidirectional SCR-SSCB topologies based on coupled inductors and diode bridges with a safe start function were introduced in [19], [20] and are shown in Figs. 2(c)-(d). The current commutating circuits of both devices are isolated from the loads. In addition, their capacitors are continuously charged by the power supply through a diode. Under no-fault conditions, however, the four topologies in Fig. 2 have two semiconductor devices in the current path, resulting in large on-state losses.

Other bidirectional SCR-SSCB configurations were introduced in [21], [22], where a single semiconductor device is used in the main circuit in either forward or reverse operation. This leads to low on-state losses. However, the increased (doubled) number of semiconductor devices required results in higher costs and a more complex control logic.

In [23]-[24], two topologies based on a mixture of different power electronics devices (SCR and IGBT in series) were presented. These topologies commutate the fault current to the LC branch by turning off the IGBT during fault interruption, which also leads to turning off the thyristor. The presence of IGBTs, however, affects the efficiency and increases the complexity of the control scheme. Two capacitive commutation-based SSCBs were proposed in [25]-[26]. These topologies benefit from a simple structure, good controllability, and a low conduction loss. Notwithstanding, as with the devices presented in [23]-[24], there is a significant surge current to the source during fault interruption.

To overcome the shortcomings of existing SCR-SSCB devices, a novel topology, termed SCR-based bidirectional CB (SCR-BCB1), is investigated in this paper. The device exhibits low on-state losses and a reduced use of semiconductors. A single semiconductor device is used in the main circuit under no-fault conditions, which helps decreasing the power losses by about 50%. At the same time, the topology deploys an analogue control circuit to achieve the active turn-off function.

A second topology, termed SCR-BCB2, is also introduced in this paper. This device decreases the volume and cost of the capacitor and increases the power density of the CB [27]. Both topologies exhibit a performance unaffected by external system parameters and, hence, are extremely reliable.

The remainder of the paper is organized as follows. Section II explains the operation principle of the introduced topologies. The considerations when selecting their main components are discussed in Section III. Experiments were carried out to verify the performance of the proposed topologies, with results discussed in Section IV. Section V presents a comparative study of the proposed topologies with other configurations found in the literature. Section VI presents the concluding remarks and closes the paper.

## II. Operation of the Presented Topologies

### *A. First Topology (SCR-BCB1)*

The first topology, SCR-BCB1, is schematically shown in Fig. 3. It consists of four thyristors ($SCR_1$, $SCR_2$, $SCR_3$, $SCR_4$), a coupled inductor, two diodes ($D_1$, $D_2$), two capacitors ($C_1$, $C_2$), a charging resistor ($R$), and a metal oxide varistor ($MOV$). $SCR_1$ and $SCR_2$ form a bidirectional current flow path (in a reverse parallel arrangement), while $L_{w1}$ and $L_{w2}$ are respectively the primary and secondary coils of the coupled inductor. $D_1$ and $D_2$ are used to rectify the charging current of $C_1$ and $C_2$ to prepare for the interruption of short-circuit faults. $R$ is used to limit the surge current when the capacitors are being charged.

$C_1$ charges through the path $D_1 \rightarrow C_1 \rightarrow R$, whereas $C_2$ charges through the path $D_2 \rightarrow C_2 \rightarrow L_{w2} \rightarrow R$. Although the charging current for $C_2$ goes through $L_{w2}$, there is no current induced at $L_{w1}$ since the thyristor in the main circuit is not turned on. $SCR_3$, $C_1$, $R$, and $L_{w2}$ form a current commutating circuit for the forward flow of current, whereas $SCR_4$, $C_2$, $R$, and $L_{w2}$ form a current commutating circuit for the reverse direction. $MOV$ is used to absorb energy during fault current interruption irrespective of the direction of current flow.

As SCR-BCB1 operates in a similar manner to block fault currents in forward and reverse directions, the blocking of a forward fault current is considered as an example to explain

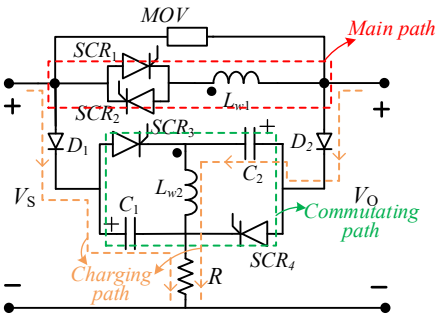



**Fig. 3.** Schematic of topology SCR-BCB1.

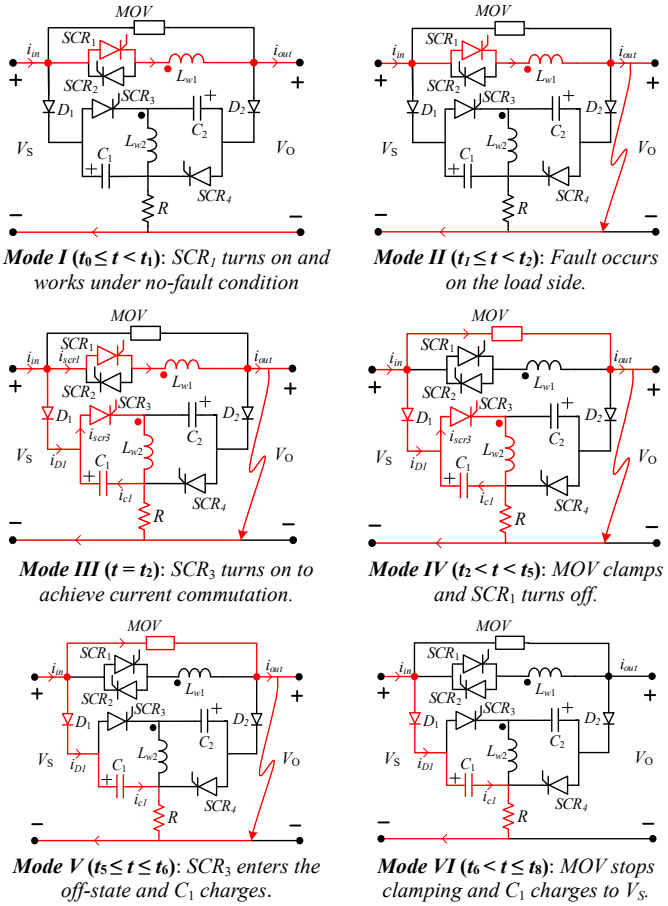



**Fig. 4.** Operation modes of SCR-BCB1 during short-circuit fault clearance.

the operation principle. Fig. 4 shows the different operation modes, while Fig. 5 shows the corresponding waveforms of SCR-BCB1 (see blue traces) during the short-circuit fault clearance. In the figure, $v_{GS,scr1}$, $v_{GS,scr3}$, and $v_{GS,scr5}$ are trigger signals. Signal $v_{GS,scr1}$ is used to turn on the CB, $v_{GS,scr3}$ is used to turn on $SCR_3$ when the fault current reaches the set threshold current, and $v_{GS,scr5}$ is used to charge $C_1$ before turning on SCR-BCB2.

A description of the operation modes is provided next.

*1) Mode I* ($t_0 \le t < t_1$): Under no-fault conditions, a pulse trigger signal is applied to the gate of $SCR_1$ to turn it on, allowing the voltage source to supply the load through the path $V_S \rightarrow SCR_1 \rightarrow L_{w1} \rightarrow V_O$. $C_1$ is fully pre-charged before $SCR_1$ is triggered.

*2) Mode II* ($t_1 \le t < t_2$): A short-circuit fault occurs at $t = t_1$ and the output current ($i_{out}$) and the current in $SCR_1$ ($i_{scr1}$)

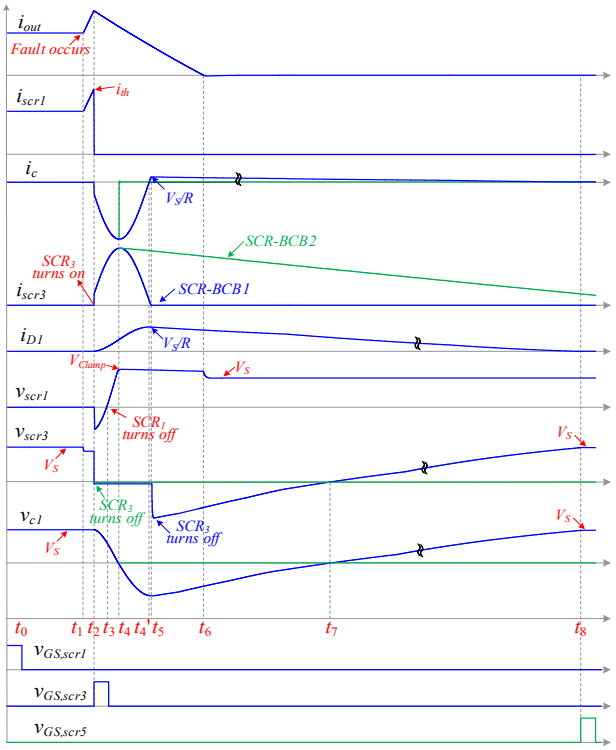



**Fig. 5.** Current and voltage waveforms of SCR-BCB1 (blue), and SCR-BCB2 (green) during fault interruption.

increase rapidly, as shown in Fig. 5.

*3) Mode III* ($t = t_2$): When the fault current reaches the preset threshold $i_{th}$, a trigger signal is applied to the gate of $SCR_3$ to turn it on. Then, an LC resonant circuit will be formed by $L_{w2}$ and $C_1$. An instantaneous voltage will be induced at $L_{w1}$ due to the mutual inductance of the coupled inductor. Because the voltage across *MOV* equals the sum of the voltage across $SCR_1$ and $L_{w1}$, when its value reaches the clamping voltage of *MOV*, *MOV* conducts. Simultaneously, the current begins to flow through the path $D_1 \rightarrow SCR_3 \rightarrow L_{w2} \rightarrow R$ once $SCR_3$ is triggered.

*4) Mode IV* ($t_2 < t < t_5$): Current continues flowing through the paths $C_1 \rightarrow SCR_3 \rightarrow L_{w2}$ and $D_1 \rightarrow SCR_3 \rightarrow L_{w2} \rightarrow R$ and *MOV* clamps the voltage across $SCR_1$ and $L_{w1}$. As a result, no current flows through $SCR_1$, which allows it to be turned off at $t = t_3$. The voltage of $C_1$ becomes negative at $t = t_4$ due to the resonance, and $C_1$ then begins to be charged naturally at $t = t_4$'.

*5) Mode V* ($t_5 \le t \le t_6$): At $t = t_5$, the current through $SCR_3$ decreases to zero and the current of $C_1$ ($i_{c1}$) equals $V_S/R$. The output current ($i_{out}$) decreases to zero at $t = t_6$.

*6) Mode VI* ($t_6 < t \le t_8$): During this period, *MOV* stops clamping and $C_1$ continues charging until its voltage increases to the magnitude of the source voltage $V_S$. When $SCR_1$ is triggered and a short-circuit fault remains on the load side, $C_1$ ensures that SCR-BCB1 quickly interrupts the short-circuit current for the next fault.

### *B. Modified Topology with DC Capacitor (SCR-BCB2)*

The capacitors in the commutating circuit of SCR-BCB1 must withstand a negative voltage during the commutation process, so an ac capacitor is required. However, ac capacitors

generally have a smaller capacitance and a bigger volume than dc capacitors, which leads to a decreased power density of the CB [27]. To benefit from the use of dc capacitors, a second topology, termed SCR-BCB2, incorporates diodes to SCR-BCB1 across $C_1$ and $C_2$. The schematic of SCR-BCB2 is shown in Fig. 6.

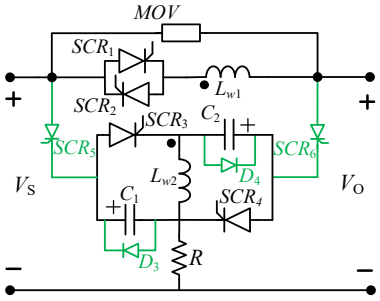
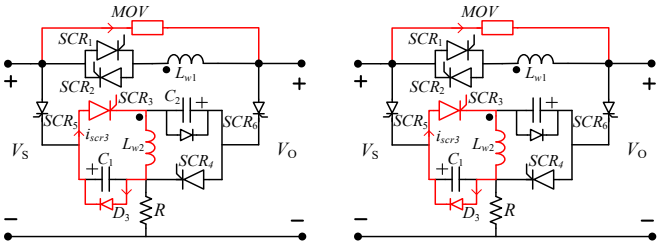



**Fig. 6.** Schematic of topology SCR-BCB2.

With relation to Fig. 3 and Fig. 6, assuming that $D_1$ and $D_2$ in SCR-BCB2 are not replaced by $SCR_5$ and $SCR_6$, the current would flow through the path $D_1 \rightarrow SCR_3 \rightarrow L_{w2} \rightarrow R$ or $D_2 \rightarrow SCR_4 \rightarrow R$ continuously during the fault interruption process ($t_0 \le t \le t_5$) as $SCR_3$ and $SCR_4$ do not withstand a reverse voltage to turn off due to the presence of $D_3$ and $D_4$. Thus, compared to SCR-BCB1 in Fig. 3, $SCR_5$ and $SCR_6$ replace $D_1$ and $D_2$ to control the capacitor charging, which can also reduce the voltage stress on $SCR_1$ by avoiding a voltage rise in $L_{w1}$ when current flows through it during the conduction of $SCR_3$.

Characteristic waveforms of voltages and currents of SCR-BCB2 are shown in Fig. 5 using green traces alongside those from the first topology. It is to be noted that the working principle of SCR-BCB2 is the same as for SCR-BCB1 until $t_4$. The remaining instances of the operating sequence are shown in Fig. 7 and summarized next.




***Mode IV* ($t = t_4$)**: *$C_1$ voltage becomes zero and current flows via $D_1$.*

***Mode V* ($t_4 < t \le t_8$)**: *$SCR_3$ current decreases to zero.*

**Fig. 7.** Two working subintervals of SCR-BCB2 during short-circuit fault clearance.

*1) Mode IV* ($t = t_4$): At $t = t_4$, the voltage across $C_1$ decreases to zero and tries to become negative. Due to the presence of $D_3$, the current initially flowing through $C_1$ begins to flow through $D_3$ instead. The voltage of $C_1$ becomes zero due to the forward-biased voltage of $D_3$.

*2) Mode V* ($t_4 < t \le t_8$): During this subinterval, the fault current is cleared completely at $t = t_6$, and the current of $SCR_3$ decreases until it eventually reaches a value of zero.

## III. Circuit Modeling and Design Considerations

The mathematical modeling of the fault interruption process for the investigated topologies is here presented alongside some design considerations. The mathematical model is used to guide the selection of components. The current threshold for triggering both SCR-BCBs is set to $i_{th}$ so that they stay closed until a detected current reaches the threshold. Once $i_{th}$ is reached, the current commutating circuit will be activated to interrupt current following the process described in Section II.

Table I shows the parameters of the devices used in the analysis. As SCR-BCB1 and SCR-BCB2 have the same operating principle before $t_4$, the modeling process for both configurations is jointly discussed in this section.

TABLE I
Parameters of the Components

| Parameters | Values | Details |
|---|---|---|
| Voltage source $v_S$ | 50 V | EA-PS 9200-25 |
| Primary coil $L_{w1}$ | 630 µH | |
| Secondary coil $L_{w2}$ | 70 µH | |
| Mutual inductance coefficient $k$ | 0.97 | |
| Capacitor $C_1$, $C_2$ | 100 µF | |
| Load resistance $R_L$ | 25 Ω | |
| Fault resistance $R_f$ | 1 Ω | |
| Charging resistor $R$ | 47 Ω | |
| $D_1$, $D_2$ | $I_{F(AV)}$ = 3 A | SR3100 |
| $D_3$, $D_4$ | $I_{F(AV)}$ = 25 A | VS-HFA25TB60-M3 |
| $SCR_1$-$SCR_6$ | 200 V/10 A<br>$t_q$ = 15 µs @ 25℃<br>$t_q$ = 35 µs @ 125℃ | 2N6402 |
| MOV | $v_{clamping}$ = 74.8 V @ 1 mA | V68ZA2P |
| Current sensor | Accuracy: ±0.5% | LA25-NP |
| Voltage comparator | | LM393M |
| Optocoupler | Response Time: 1.3 µs | PC817 |

### A. Circuit modeling for fault current interruption

The equivalent circuits for Modes II and III during fault current interruption are shown in Fig. 8.

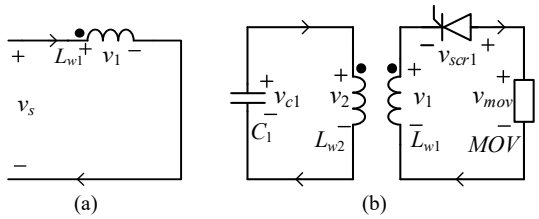



**Fig. 8.** Equivalent circuits of the presented topologies for (a) Mode II ($t_1 \le t < t_2$), (b) Mode III ($t = t_2$).

When either of the presented SCR-BCB topologies is under no-fault conditions, the voltage across the terminals of $C_1$ equals the voltage of the power supply $v_s$, and the current flows through $SCR_1$ and $L_{w1}$ only. Since the resistance of $L_{w1}$ is negligible, the power losses are then caused by $SCR_1$. As the dc network has a very low impedance, the current flowing through $SCR_1$ increases rapidly after a short-circuit fault on the load side. The equivalent circuit before the magnitude of the fault current reaches $i_{th}$ is shown in Fig. 8(a). According to Kirchhoff's voltage law (KVL), it is deduced that

$$\begin{cases} -v_s + v_1 = 0 \\ v_1 = L_{w1}\dfrac{di_{out}}{dt} \end{cases} \tag{1}$$

where $v_1$ is the voltage across $L_{w1}$. Before $t_1$, the initial value

of current $i_{out}$ is $i_0$. Therefore, the solution to (1) is

$$i_{out} = i_0 + \frac{v_s}{L_{w1}} t \tag{2}$$

According to (2), the output current $i_{out}$ increases linearly with time before $SCR_1$ turns off, and the rate of change of the fault current is inversely proportional to the value of $L_{w1}$. If the line impedance $L_{line}$ is considered, the rate of change of the fault current is inversely proportional to the sum of $L_{w1}$ and $L_{line}$.

When the fault current reaches $i_{th}$, the voltage comparator generates a high-level signal which is forwarded to the gate driver chip to create a trigger signal, activating thyristor $SCR_3$. $C_1$ discharges immediately following this. An LC resonant circuit is then formed by $C_1$ and $L_{w2}$, resulting in the equivalent circuit shown in Fig. 8(b). Applying KVL yields

$$\begin{cases} v_{scr1} + v_1 = v_{mov} \\ -v_{c1} + v_2 = 0 \\ v_1 = nkv_2 \end{cases} \tag{3}$$

where $v_{scr1}$ is the voltage across $SCR_1$, $v_{c1}$ is the capacitor voltage, $v_2$ is the voltage across the secondary coil $L_{w2}$, $n$ is the turns ratio, and $k$ is the mutual inductance coefficient of the coupled inductor. In Mode III, the voltage across the varistor $v_{mov}$ should be less than the clamping voltage of the varistor $v_{clamp}$, namely

$$\begin{cases} v_{scr1} + v_1 < v_{clamp} \\ v_{clamp} = av_s \end{cases} \tag{4}$$

where $a$ is the ratio between $v_s$ and $v_{clamp}$. Equation (4) is rewritten as

$$v_{scr1} < (a - nk) v_s \tag{5}$$

To turn off the thyristor under the reverse voltage, the thyristor voltage $v_{scr1}$ should be less than 0; then,

$$a < nk \tag{6}$$

$C_1$ continues to discharge after $SCR_1$ is turned off. Neglecting the voltage drop and losses in $SCR_3$, $C_1$ and the secondary coil of the coupled inductor still form an LC resonant circuit, which is described by

$$L_{w2}C_1 \frac{d^2 v_{c1}}{dt^2} + v_{c1} = 0 \tag{7}$$

The initial values of $v_{c1}$(t) and $i_{c1}$(t) are $v_s$ and $-i_{th} \cdot nk$ respectively, and the solution of (7) is obtained as

$$\begin{cases} v_{c1}(t) = v_s \cos \dfrac{t}{\sqrt{L_{w2}C_1}} - nki_{th}\sqrt{L_{w2}/C_1} \sin \dfrac{t}{\sqrt{L_{w2}C_1}} \\ i_{c1}(t) = v_s \sqrt{L_{w2}/C_1} \sin \dfrac{t}{\sqrt{L_{w2}C_1}} + nki_{th} \cos \dfrac{t}{\sqrt{L_{w2}C_1}} \end{cases} \tag{8}$$

By differentiating (8) twice and substituting the result into (3), yields

$$v_{scr1} = \frac{nkv_s}{2L_{w2}C_1} t^2 + \frac{n^2k^2i_{th}}{C_1} t + v_{mov} - nkv_s \tag{9}$$

At this moment, $v_{mov}$ has reached the value of $v_{clamp}$, which means $v_{mov} = v_{clamp} = av_s$. This condition will be valid only at this instance, although normally the value of $v_{mov}$ changes with the current. To ensure that $SCR_1$ is turned off, $v_{scr1}$ should remain negative during the turning off period ($t_q$) of the thyristor. Using such a consideration results in

$$\frac{nkv_s}{2L_{w2}C_1} t_q^2 + \frac{n^2k^2i_{th}}{C_1} t_q + (a - nk) v_s \le 0 \tag{10}$$

Since from (6) $a–nk < 0$, one can conclude that

$$C_1 \ge \frac{n^2k^2i_{th}}{(nk - a)v_s} t_q + \frac{nk}{2L_{w2}(nk - a)} t_q^2 \tag{11}$$

Equation (11) shows the capacitance value with relation to $i_{th}$, $n$, $k$, $t_q$, $L_{w2}$ and $a$. Before the value of $C_1$ is obtained, it is generally necessary to determine the parameters of the coupled inductor, varistor, and thyristor. This process is described in the following section.

### *B. Design Considerations*

According to the analysis in the previous section and considering Figs. 3-7, the main components in SCR-BCB1 and SCR-BCB2 include thyristors ($SCR_1$, $SCR_2$) in the main path, thyristors ($SCR_3$, $SCR_4$) and capacitors ($C_1$, $C_2$) in the commutating circuit, the coupled inductor, and the diodes ($D_1$, $D_2$) and thyristors ($SCR_5$, $SCR_6$) to charge the capacitors ($C_1$, $C_2$). These parameters must be carefully selected to ensure the successful fault interruption of by the CBs.

*1) Selection of $D_1$, $D_2$, $D_3$, and $D_4$*

$D_1$ and $D_2$ are used to respectively charge $C_1$ and $C_2$. The maximum charging current ($i_{Dmax}$) complies with

$$i_{D\max} = v_s / R \tag{12}$$

From (12), the maximum current that $D_1$ and $D_2$ can carry must be greater than $i_{Dmax}$.

$D_3$ and $D_4$ are used as the circulation path in the LC resonant circuit when the direction of current is negative. This implies their maximum allowable instantaneous current should be higher than the maximum value of $i_{c1}(t)$ in (8).

*2) Selection of thyristors*

The maximum current and voltage magnitudes that a thyristor can withstand during the interruption of a short-circuit fault are among the most important considerations to prevent damage. In the main path, the maximum current flowing through $SCR_1$ and $SCR_2$ should be greater than the set threshold $i_{th}$. Additionally, the voltage to be withstood should be greater than the clamping voltage of the varistor $v_{clamp}$. The maximum voltage and maximum current that $SCR_3$ and $SCR_4$ can withstand should be greater than $v_s$ and $i_{c1}(t)$. The selection of $SCR_5$ and $SCR_6$ is similar as the selection of $D_1$ and $D_2$ (considering the maximum current defined in (12)).

*3) Selection of MOV*

The MOV absorbs energy during the transient period of a short-circuit fault. In addition, its maximum continuous operating voltage should be higher than the supply voltage. Generally, the varistor's clamping voltage $v_{clamp}$ is typically 1.2 to 2 times the value of $v_s$ [28], which implies that the value of $a$ should also be between 1.2 and 2. In addition, $a$ should be smaller than $nk$ according to (6).

*4) Selection of the coupled inductor and capacitors*

The maximum current and the inductance of the coils should be considered when designing coupled inductors. According to (2), the inductance of the primary coil limits the ramp rate of the fault current. The larger the inductance is, the

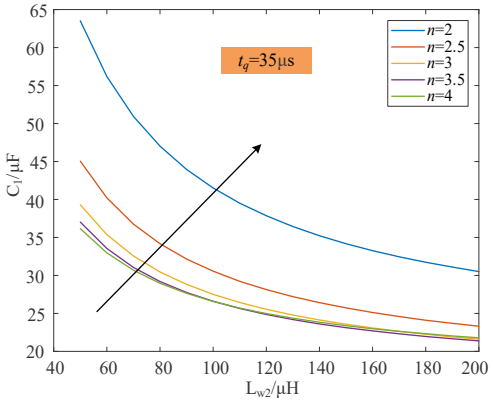



**Fig. 9.** Relationship between $C_1$ and $L_{w2}$ subjected to variations in $n$ (with $t_q$ = 35 μs).

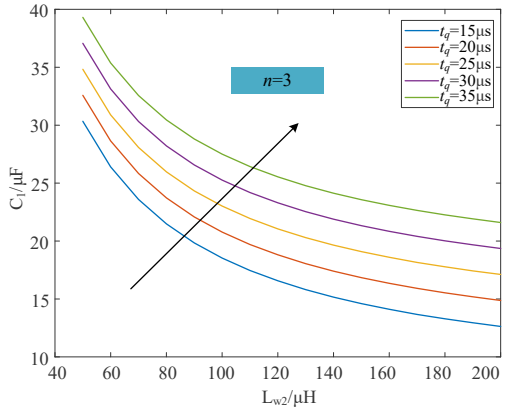



**Fig. 10.** Relationship between $C_1$ and $L_{w2}$ subjected to variations in $t_q$ (with $n$ = 3).

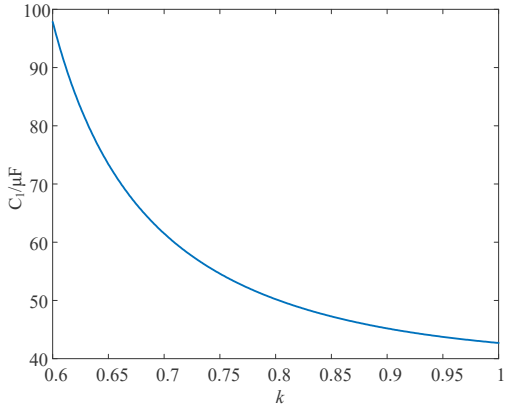



**Fig. 11.** Relationship between $C_1$ and $k$.

slower the ramp rate of the fault current and the greater the weight and volume of the coupled inductor would be. According to (6), the turns ratio of the coupled inductor $n$ should be greater than $a/k$. The relationship between $C_1$, $L_{w2}$ and $n$ is given in (11). Figs. 9 and 10 show the relationship between $C_1$ and $L_{w2}$. According to Table I, $t_q$ is selected as 35 μs and $n$ as 3. When $t_q$ = 35 μs, $L_{w2}$ decreases with an increase of $C_1$ and the relationship between $C_1$ and $L_{w2}$ does not change much if $n \geq 3$. When $n$ = 3, a smaller turn-off time $t_q$ leads to smaller values of $C_1$ and $L_{w2}$.

As the voltage and current ratings increase, so does the size and cost of the coupled inductor, while the value of $k$ decreases. According to (6), as $k$ decreases, $n$ must increase to ensure that the varistor operates properly. A variation in the value of $k$, according to (11), would impact the value of $C_1$. This relationship is shown in Fig. 11.

As shown in Fig. 11, the required value of $C_1$ gradually increases as $k$ decreases. As a result, at higher voltage and current levels, a larger value of $C_1$ can be adopted to compensate for the decrease in $k$ after establishing that the saturation current of the coupled inductor can ensure a successful triggering of the CB.

*5) Selection of charging resistor R*

Resistor $R$ is used to limit the charging current of the capacitors to $v_s/R$. The power rating of $R$ needs to be considered to ensure the normal operation of the charging path. The greater the resistance value, the slower $C_1$ charges and the lower the maximum charging current of the capacitor. However, the value of $R$ should be chosen so that $C_2$ attains an overdamped transient behavior when charging. This enables $C_2$ to charge without exhibiting resonance throughout the charging duration.

## IV. Experimental Validation and Practical Considerations

The experimental platform shown in Fig. 12 was developed to verify the performance of SCR-BCB1 and SCR-BCB2. The test parameters and components used are given in Table I. Thyristors 2N6402 were selected as they have a turn-off time of 15 μs at 25°C and 35 μs at 125°C. A coupled inductor with a coupling coefficient of 0.97 was chosen, which has values of inductance of the primary and the secondary coils of 630 μH and 70 μH. The capacitance of $C_1$ was selected as 100 μF. A 1 mH inductor ($L_{line}$) was used to limit the rate of rise of the fault current. Current sensor LA25-NP was incorporated to detect the current, and the threshold current was set to 4 A. Comparator LM393M and optocoupler PC817 form an analogue protection unit which triggers the commutating circuits when an overcurrent is detected (i.e. for values greater than 6 A). EA-PS 9200-25 is used as the main power source ($V_S$) and HM7042-5 is used to power the control circuits.

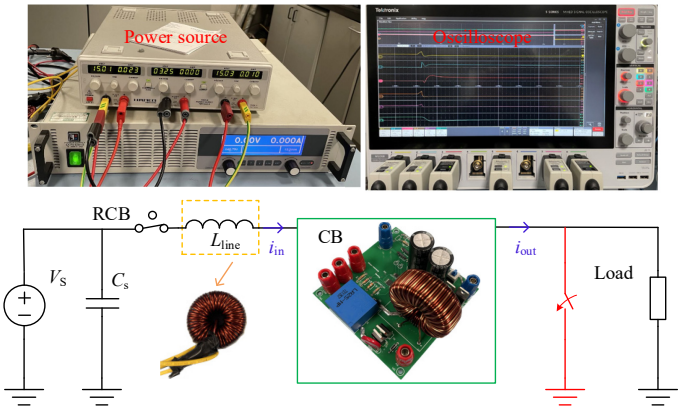



**Fig. 12.** Experimental setup and circuits diagram for dc tests.

### A. Verification of SCR-BCB1

The performance of this topology was assessed when interrupting a short-circuit fault. Experimental results are shown in Fig. 13. These are described next.

A current of 2 A flows through SCR-BCB1 initially. When the short-circuit fault occurs, the fault current increases

linearly. This behavior lasts until the current flowing through $SCR_1$ reaches 6.2 A. At this point, $SCR_3$ in the commutating circuit is triggered, resulting in the discharging of $C_1$ to draw the fault current to zero. $SCR_1$ begins to withstand the reverse voltage at this point, and this continues for approximately 35 μs, which corresponds to the theoretical turn-off time of the circuit. The thyristor current $i_{scr1}$ is reduced to zero from its peak value and the maximum voltage stress on $SCR_1$ is about 1.6 $v_s$ (83.7 V). Because of the presence of $D_1$, when $SCR_3$ is turned on, current begins to flow through the path $D_1 \rightarrow SCR_3 \rightarrow L_{w2} \rightarrow R$. When $SCR_3$ is turned off, the current flowing through $D_1$ begins to charge $C_1$. In this case, the peak value of the fault current is 0.2 A higher than the set threshold value of 6 A, which is caused by the delay in the trigger signal of $SCR_3$ [29], the error of the current sensor measurement, and the voltage divider resistors of the voltage comparator. The total delay in the trigger signal was estimated to be about 2 μs without considering the error caused by the resistors used for the current sensor and the voltage comparator.

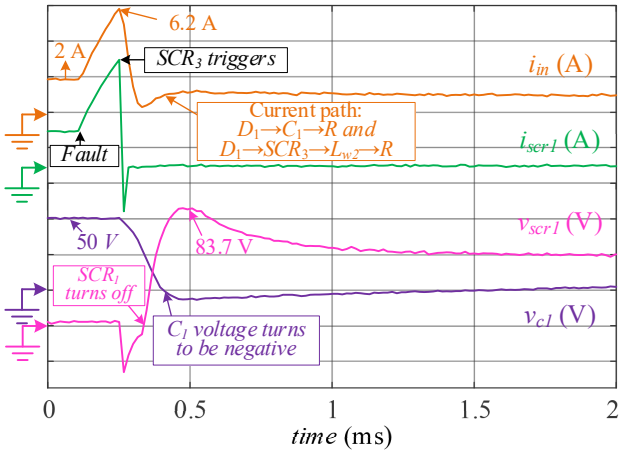



**Fig. 13.** SCR-BCB1: Fault current interruption.

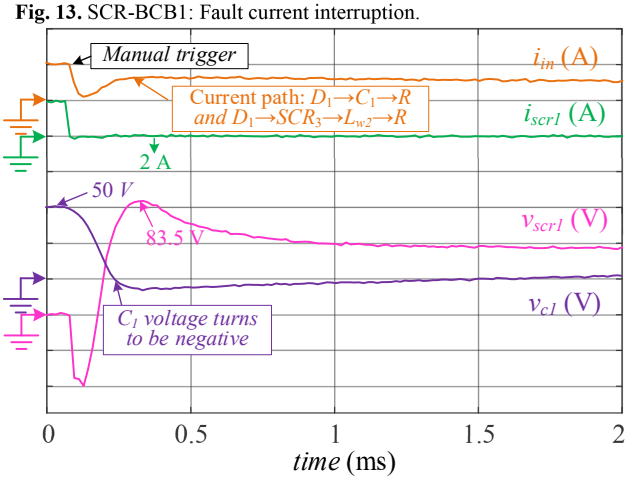



**Fig. 14.** SCR-BCB1: Manual triggering.

SCR-BCB1 can be manually activated to act as a switch, which enhances its controllability and reliability. This feature was assessed in another experimental test, with waveforms of the main devices during manual triggering shown in Fig. 14. Under no-fault conditions, a trigger signal is sent directly to $SCR_3$ in the current commutating circuit to discharge $C_1$, which turns off $SCR_1$. Following conduction of $SCR_3$, the operating process is similar to that of the device when interrupting the short-circuit fault current.

### *B. Verification of SCR-BCB2*

For SCR-BCB1, the capacitor voltage $v_{c1}$ changes polarity during the fault interruption process (see Fig. 13). This requires the use of ac capacitors which are typically larger and more expensive than dc capacitors. To prevent a change in voltage polarity, as shown in Fig. 6, in SCR-BCB2 a diode is used across $C_1$ and $C_2$ to clamp the capacitor voltage. To assess the performance of SCR-BCB2 for fault interruption, a similar short-circuit fault as in Section IV-A was experimentally tested, with results shown in Figs. 15 and 16.

As observed in Fig. 15, when the fault current reaches 6.2 A, $SCR_3$ is activated. This causes the discharging of $C_1$, and starts its turn-off process. As $SCR_5$ is used instead of $D_1$ in SCR-BCB1, the previous current path $V_S \rightarrow SCR_5 \rightarrow SCR_3 \rightarrow L_{w1} \rightarrow R$ is no longer formed. The magnitude of $v_{c1}$ is also reduced to zero and remains unchanged.

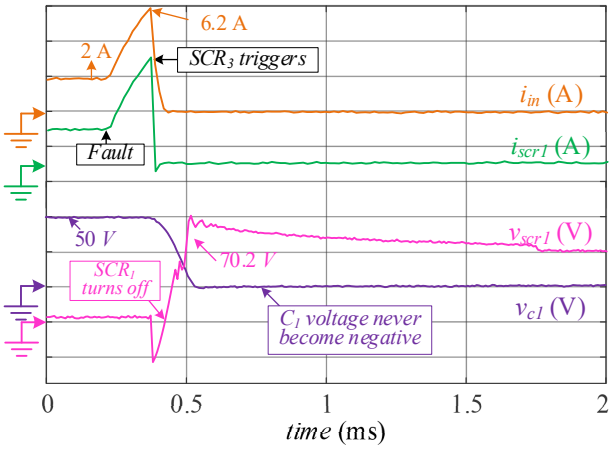



**Fig. 15.** SCR-BCB2: Fault current interruption.

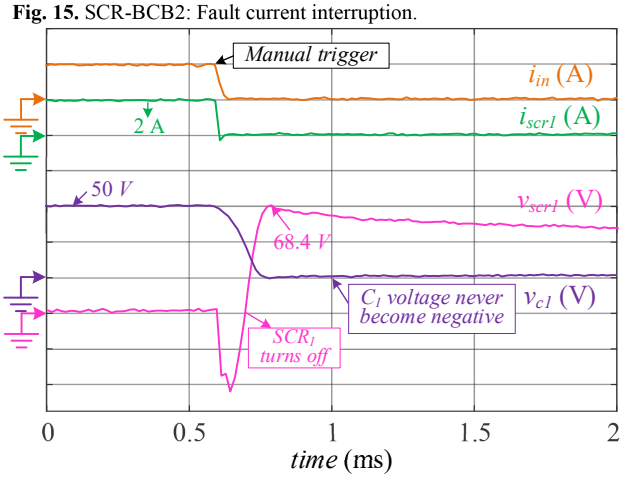



**Fig. 16.** SCR-BCB2: Manual triggering.

Fig. 16 shows the experimental results when SCR-BCB2 is manually triggered. During the turn-off process, $v_{c1}$ never becomes negative, enabling the use of a dc capacitor.

When comparing the two presented topologies, the voltage stress on $SCR_1$ in SCR-BCB2 is less than that in SCR-BCB1, both for short-circuit fault turn-off and a manual triggering, as shown in Fig. 17. This is due to the presence of $D_1$ in SCR-BCB1, which causes a voltage rise in $L_{w1}$ when current flows through it at the time of $SCR_3$ conducting.

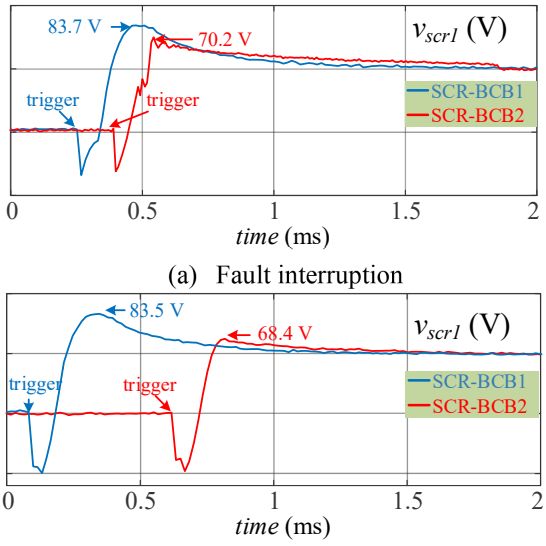



**Fig. 17.** Comparison of the voltage stress on $SCR_1$ for the presented topologies.

### *C. Topology design for a higher voltage level*

The voltage level for small ships [30], metros, and light rail transit [31] is usually around 1 kV. Thus, SCR-based SSCBs are suitable for use in the power systems of these applications. In this section, the design of a 1 kV/2 kA CB is presented and simulation results are included to further demonstrate the use of the presented topologies in applications with higher voltage ranges. The fault current threshold was set to 3 kA.

According to the design principle in Section III, thyristors T3800N18TOFVTXPSA1 (1800 V/4000 A, $t_q$ = 250 µs) were selected for $SCR_1$-$SCR_4$, while thyristors VS-111RKI120PBF (1.2 kV/110 A) were used for $SCR_5$ and $SCR_6$. These components ensure a maximum charging current of the capacitor to be 100 A, with a discharging resistor $R$ = 100 Ω. Similarly, diodes APT100S20BG (120 A) were adopted for $D_1$ and $D_2$ and RA201248XX (4800 A) for $D_3$ and $D_4$. The *MOV* B72260B0102K001 with a clamping voltage of 1620 V was adopted. $C_1$ and $C_2$ were designed to be 6.6 mF for this voltage rating, so capacitors B32373A5307J030 (2 ac capacitors in series as one group and 44 groups of capacitors in parallel for a total of 88 capacitors) and C44UQGT7220M33K (3 dc capacitors in parallel) were selected. A MATLAB/Simulink simulation was conducted using the parameters for the previous components with results shown in Fig. 18.

As shown in Figs. 18(a)-(c), the two proposed CBs are capable of interrupting and isolating short-circuit faults in a medium-voltage application. The waveforms of $i_{out}$ for both topologies are essentially the same, as are the waveforms of $i_{scr}$. The difference in simulation results between SCR-BCB1 and SCR-BCB2 is that $v_{c1}$ in SCR-BCB2 is no longer subjected to negative voltages during fault interruption. Fig. 18(d) shows the waveforms of the output current $i_{out}$ of SCR-BCB1 for various values of line inductance. This shows that the line inductance affects the rate of rise and fall of the fault current but has no effect on the performance of the CB.

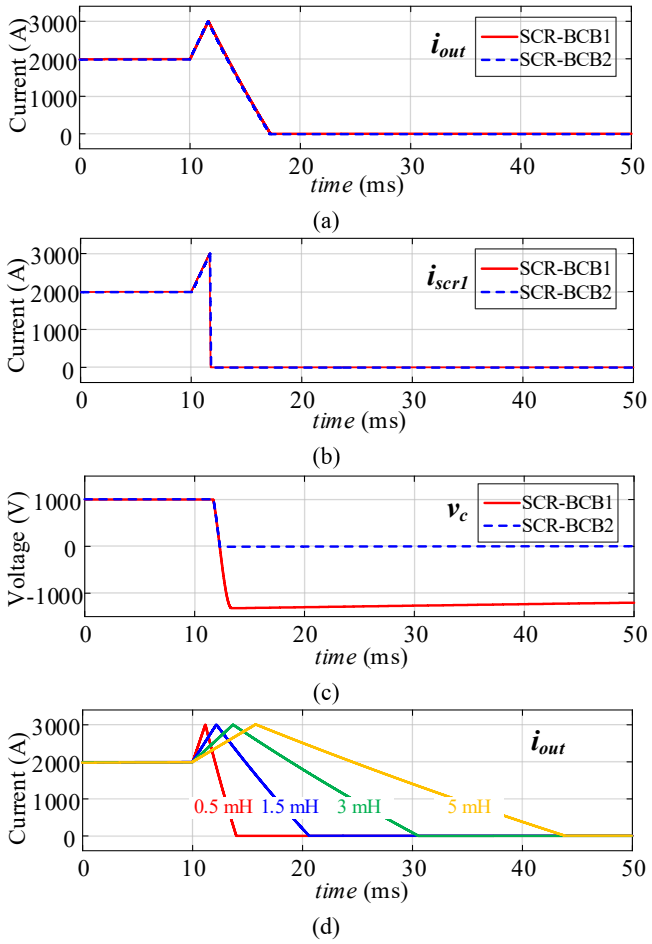



**Fig. 18.** Simulation results of the 1 kV/2 kA SCR-BCB: (a) output current, (b) $SCR_1$ current, (c) $C_1$ voltage, (d) sensitivity test of the line inductance.

TABLE II
COST COMPARISON BETWEEN SCR-BCB1 AND SCR-BCB2 IN LOW VOLTAGE

| Topology | SCR-BCB1 | SCR-BCB2 |
|---|---|---|
| $D_1$, $D_2$ | SR3100 (£0.0742) | / |
| $D_3$, $D_4$ | / | VS-HFA25TB60-M3 (£1.52) |
| $SCR_5$, $SCR_6$ | / | 2N6402 (£0.27421) |
| $C_1$, $C_2$ | R60EW61005000K (£15.85) | 100ZLJ100M10X20 (£0.72) |
| **Total Cost** | £31.8484 | £5.02842 |

Note: All the cost information is from Digikey [32].

TABLE III
COST COMPARISON BETWEEN SCR-BCB1 AND SCR-BCB2 IN HIGHER VOLTAGE

| Topology | SCR-BCB1 | SCR-BCB2 |
|---|---|---|
| $D_1$, $D_2$ | APT100S20BG (£4.61) | / |
| $D_3$, $D_4$ | / | RA201248XX (£257.157) |
| $SCR_5$, $SCR_6$ | / | VS-111RKI120PBF (£39.84) |
| $C_1$, $C_2$ | B32373A5307J030 (88×2 in total / £100.34×88×2) | C44UQGT7220M33K (3×2 in total / £145.13×6) |
| **Total Cost** | £17669.06 | £1464.774 |

Note: All the cost information is from Digikey [32].

### *D. Cost comparison between SCR-BCB1 and SCR-BCB2*

To further compare the cost between SCR-BCB1 and SCR-BCB2 due to the differences in their components, the scaled-down design used for the experimental results presented in Sections IV-A and IV-B and the higher voltage design in Section IV-C were used as examples. For a meaningful exercise, the components that differ between the two topologies have been primarily compared, with results from this comparison shown in Tables II and III. As observed, SCR-BCB2 leads to a lower investment cost than SCR-BCB1. In addition, the greater the voltage rating is, the greater the cost of the SCR-BCB1 becomes.

## V. A Comparative Study

In Table IV, the two presented topologies in this paper (SCR-BCB1 and SCR-BCB2) are compared with typical bidirectional topologies available in the literature. The comparison is made with regards to the number of components and characteristics like conduction loss, isolation of the source, among others. An analysis is presented next.

To achieve fault current interruption, the topology presented in [17] employs inductors, while the one in [19] uses coupled inductors. These topologies where the commutation is inductor-based lead to a moderate conduction loss. SCR-BCB1 and SCR-BCB2 address such a drawback by reducing the number of semiconductors in the main circuit.

Z-SSCBs can automatically interrupt a short-circuit fault current without the need for additional control circuits, but their automatic turn-off is strictly limited by parameter setting and is highly susceptible to external system parameters, resulting in controllability and reliability issues. Instead, SCR-BCB1 and SCR-BCB2 are independent from external parameters and have better controllability than the Z-SSCBs reported in [13]-[15].

The topologies in [23], [24] employ a mixture of devices to compensate for the lack of controllability of Z-SSCBs. Their performance is not affected by external parameters, and a high reliability can be achieved. However, the presence of four semiconductor components in the main circuit during normal operation significantly increases the conduction loss. In contrast, SCR-BCB1 and SCR-BCB2 have a single thyristor in the main circuit, resulting in a much lower conduction loss.

The topologies in [18], [25]-[26] use a single capacitor which discharges to interrupt a short-circuit fault. They are simple in structure and exhibit a quick response to current interruptions. The shortcoming is the large transient surge current reflected to the source incurred during the short-circuit fault interruption. In contrast, SCR-BCB1 and SCR-BCB2 avoid such a surge current on the source side by using an embedded current-commutation circuit. In addition, in the presence of a short-circuit on the load side, the topologies in [25]-[26] cannot provide a safe start. To overcome this issue, the design in [17] includes additional thyristors to detect faults on the load side, while SCR-BCB1 and SCR-BCB2 use capacitor pre-charging to guarantee a safe start. Regarding on-state loss, SCR-BCB1 and SCR-BCB2 exhibit slightly greater loss than the topologies investigated in [25] and [26]. This is due to the presence of the primary coil of the coupled inductor on the main circuit despite having the same number of thyristors on the main circuit.

Overall, although SCR-BCB1 and SCR-BCB2 do not have the lowest component count, they offer the simultaneous advantages of significantly reducing the conduction loss of bidirectional CBs, preventing a surge current to the source during fault interruption, and ensuring a safe start in the presence of a fault at the load side. Furthermore, SCR-BCB2 allows the use of dc capacitors, which even further reduces the cost and size of the CB.

TABLE IV
Comparison of SCR-BCB1 and SCR-BCB2 with different SSCBs in the Literature

| SCR-SSCB | Inductor-based commutation | | | | Z-source | | | Mixed devices | | Capacitive commutation | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **SCR-BCB1** | **SCR-BCB2** | [17] | [19] | [13] | [14] | [15] | [23] | [24] | [18] | [25] | [26] |
| Number of thyristors | **4** | **6** | 3 | 3 | 8 | 2 | 1 | 2 | 2 | 6 | 4 | 4 |
| Number of diodes | **2** | **2** | 2 | 2 | 4 | 2 | 4 | 4 | 2 | 0 | 0 | 5 |
| Number of IGBTs | **0** | **0** | 0 | 0 | 0 | 0 | 0 | 2 | 2 | 0 | 0 | 0 |
| Number of semiconductors in the main circuit | **1** | **1** | 2 | 2 | 4 | 2 | 3 | 4 | 4 | 2 | 1 | 1 |
| Number of capacitors | **2** | **2** | 2 | 1 | 4 | 3 | 1 | 4 | 1 | 1 | 2 | 2 |
| Number of inductors | **2** | **2** | 2 | 2 | 2 | 2 | 2 | 0 | 0 | 0 | 0 | 0 |
| Number of resistors | **1** | **1** | 2 | 1 | 4 | 0 | 0 | 0 | 1 | 2 | 2 | 3 |
| Conduction loss | **L**(1) | **L** | M(2) | M | H(3) | M | H | H | H | M | L | L |
| Isolated source from load | **Yes** | **Yes** | Yes | Yes | Yes | No | Yes | No | No | No | No | No |
| Manual trigger capability | **Yes** | **Yes** | Yes | Yes | No | No | No | Yes | Yes | Yes | Yes | Yes |
| Controllability | **Yes** | **Yes** | Yes | Yes | No | No | No | Yes | Yes | Yes | Yes | Yes |
| Automatic trigger | **No** | **No** | No | No | Yes | Yes | Yes | No | No | No | No | No |
| Influenced by outer parameters | **No** | **No** | No | No | Yes | Yes | Yes | No | No | No | No | No |
| Safe start | **Yes** | **Yes** | No | Yes | No | No | No | No | No | Yes | No | No |
| DC capacitor | **No** | **Yes** | No | No | No | No | No | No | No | No | No | No |

(1) There is only one semiconductor in the main circuit, leading to a low conduction loss. (2) There are two semiconductors in the main circuit, leading to a moderate conduction loss. (3) There are more than two semiconductors in the main circuit, leading to a high conduction loss.

## VI. Conclusion

Two novel SCR-SSCBs topologies (termed SCR-BCB1 and SCR-BCB2) which significantly reduce the on-state losses of semiconductor devices by ~50% when compared to existing bidirectional configurations were presented in this paper. This reduction in loss is attributed to the elimination of an inductor from the main circuit during normal operation. Such an improvement exhibited by the topologies is facilitated by having a single thyristor in their main circuit under no-fault conditions. Compared to conventional Z-SSCBs, both SCR-BCB devices have reliable breaking capability which is independent of the external parameters of the system to be protected. This enables them to block faults without being limited by the range of the fault impedance and the fault current ramp rate. With SCR-BCB2 specifically, the use of diodes ensures that the capacitor voltage in the communicating circuit is always greater than or equal to zero, allowing the use of dc capacitors. This further reduces the cost and size of the device. SCR-BCB2 also reduces the voltage stress on the thyristor.

The detailed design process for the presented topologies as well as the selection criteria of key components are provided. The parameters can be suitably selected for various application scenarios using the provided formulas and criteria to achieve a successful interruption of fault currents.

Experimental tests with the investigated topologies were conducted to verify their performance when interrupting short-circuit faults and for a manual triggering. The results show that both topologies enable a quick interruption of the main circuit current after receiving the trigger signal. In particular, SCR-BCB2 ensures that the capacitors in the commutating branch are not exposed to negative voltages during fault interruption.

The two novel topologies presented in this paper significantly reduce the high on-state losses of bidirectional SCR-SSCBs while ensuring a reliable isolation of short-circuit faults. These attributes make them attractive for the protection of dc microgrids.

## Acknowledgement

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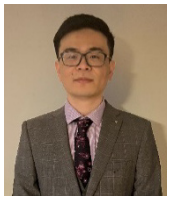

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