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# Highly Efficient GaN Doherty Power Amplifier for N78 Sub-6 GHz Band 5G Applications

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**Abstract:** In this paper, a high-efficiency GaN Doherty power amplifier (DPA) for 5G applications in the N78 sub-6 GHz band is introduced. The theoretical analysis of the matching networks for the peak and carrier transistors is presented, with a focus on the impact of unequal power splitting for both transistors and the recommendation of a post-harmonic suppression network. The proposed design features an unequal Wilkinson power divider at the input and a post-harmonic suppression network at the output, both of which are crucial for achieving high efficiency. The Doherty power amplifier comprises two GaN 10 W HEMTs, measured across the 3.3 GHz to 3.8 GHz band (the N78 band), and the results reveal significant improvements in gain, output power, drain efficiency, and power-added efficiency. Specifically, the proposed design achieved a power gain of over 12 dB and 42 dBm saturated output power. It also achieved a drain efficiency of 80% at saturation and a power-added efficiency of 75.2%. Furthermore, the proposed harmonic suppression network effectively attenuated the harmonics at the output of the amplifier from the second to the fourth order to more than −50 dB, thus enhancing the device's linearity.

**Keywords:** Doherty power amplifier (DPA); GaN HEMT sub-6 GHz for 5G; power divider/combiner; high efficiency; power combiners; harmonic suppression; unequal Wilkinson power divider

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## 1. Introduction

The demand for high-performance RF power amplifiers (PAs) has surged with the advent of 5G wireless communication networks. These PAs play a pivotal role in ensuring seamless signal transmission, making them critical components in bridging the gap between transmitters and receivers. Many applications depend mainly on PAs as detection systems [1], hyperthermia therapy system [2,3], and wireless communications networks [4]. Some of the most important wireless communication networks are the 5G networks. As 5G networks continue to expand, particularly with the deployment of small cell networks, the management of power consumption and heat dissipation in wireless base stations poses significant challenges for system designers. The exponential growth in data rates and the increasing complexity of modulation schemes, such as 4096 Quadrature Amplitude Modulation, mandate PAs that are not only highly efficient but also capable of handling high peak-to-average power ratios (PAPR). The integration of multiple-input multiple-output

(MIMO) transmissions further complicates transmitter design, underscoring the need for wideband, high-efficiency PAs with compact footprints [5].

Gallium nitride (GaN) PAs have emerged as promising candidates, particularly for the 5G sub-6 GHz band. GaN offers advantages such as high power density, efficiency, and wideband performance. Moreover, GaN technology exhibits low thermal resistance and can operate at high frequencies, aligning well with the demands of 5G networks. PAs operating in the FR1 range must efficiently handle complex modulations with high PAPR, making high-efficiency PAs a necessity [6,7].

Various methods and architectures have been proposed to enhance PA efficiency, especially at output power back-off (OPBO) levels. These include the Doherty power amplifier (DPA) [7–9], Chireix-outphasing PAs [10–12], Envelope Elimination and Restoration (EER) [13,14], Envelope Tracking (ET) methods [15,16], and Power Combining methods [17,18].

Among these, DPA stands out due to its simplicity, reliability, and excellent linearity. Recent advancements have expanded its bandwidth through innovative strategies. While improving DPA bandwidth is critical, it often leads to increased circuit complexity. Strategies like output compensation stages and subsequent matching networks [7,19], an unusual inverted impedance network [20], and digital approaches [10,12] have been employed. This paper addresses the challenge of maintaining a DPA's basic structure while achieving broad bandwidth and exceptional efficiency.

DPAs are designed to split and combine power at the amplifier's input and output, respectively. The power divider circuit, which plays a crucial role in optimizing linearity, offers an optimal power split ratio based on input power. Various power divider methods, such as quadrature hybrid couplers [21,22], equal-split Wilkinson's [23,24], and the dual-input Doherty technique that utilizes digital input processing for optimal splitting [25,26], have been explored. In our study, we employed the unequal-split Wilkinson's method and included a harmonic suppression circuit at the DPA network's output to ensure both linearity and maximum efficiency. In this paper, we present the design and simulation of a PA based on the CG2H40010F GaN HEMT from Wolfspeed, operating in the 3 GHz to 4 GHz frequency range, covering the 5G N78 band (3.3 GHz–3.8 GHz). The Advanced Design System (ADS) software version 2022, provided by Keysight Technologies, was utilized for RF circuit design.

This research contributes significantly to the field of RF power amplifiers for 5G applications. The main contributions include the following:

- Proposed a design for a high-efficiency GaN Doherty power amplifier tailored to the N78 sub-6 GHz band, the most widely used band in active 5G NR networks.
- Significantly improved PAE by 27% through the incorporation of a 2.5:1 unequal Wilkinson power divider at the amplifier's input, in contrast to using an equal Wilkinson divider.
- Introduced a seventh-order post-harmonic suppression network that effectively suppressed harmonics from the second to the fourth order to more than −50 dB, enhancing linearity and PAE.
- Achieved a gain of 12 dB, an output power of 42 dBm, a drain efficiency of 80%, and a power-added efficiency of 75.2% in the proposed DPA design.
- Validated the simulation results by fabricating and measuring both the power divider and the harmonic suppression network, showing good agreement.
- The paper serves as a valuable reference for future studies in the field and paves the way for further enhancements and optimizations in RF PA designs for 5G applications.

Overall, the paper offers a comprehensive and innovative approach to achieving high efficiency in GaN DPAs, addressing the specific requirements of 5G applications in the N78 band. Its findings contribute to the ongoing development of advanced RF technologies for enhanced connectivity and performance in the 5G era.

The paper is structured as follows: In Section 2, a revision of the Doherty technique to improve efficiency was performed. The basic structure and advantages of the Doherty technique and how to calculate the output power, gain, linearity, and efficiency of that

technique are discussed. In Section 3, all parts of the proposed DPA design are presented, including the design of the unequal Wilkinson power divider and the harmonic suppression network. The expected performance of DPA as a function of both frequency and input power is presented and discussed in detail in Section 4, in addition to the review and discussion of simulation results and comparison of this work with the literature. Finally, Section 5 summarizes the conclusions drawn from this research.

## 2. Doherty Power Amplifier

The Doherty power amplifier (DPA), conceived by W.H. Doherty in 1936 [27], is designed for highly efficient linear power amplification. In Figure 1, we present the schematic of our proposed DPA, emphasizing its key components. This configuration includes two amplifiers, the main class AB amplifier (carrier) and the auxiliary class C amplifier (peak). Two $\lambda/4$ transmission lines are integrated for phase correction and impedance translation, along with active load impedance modulation.

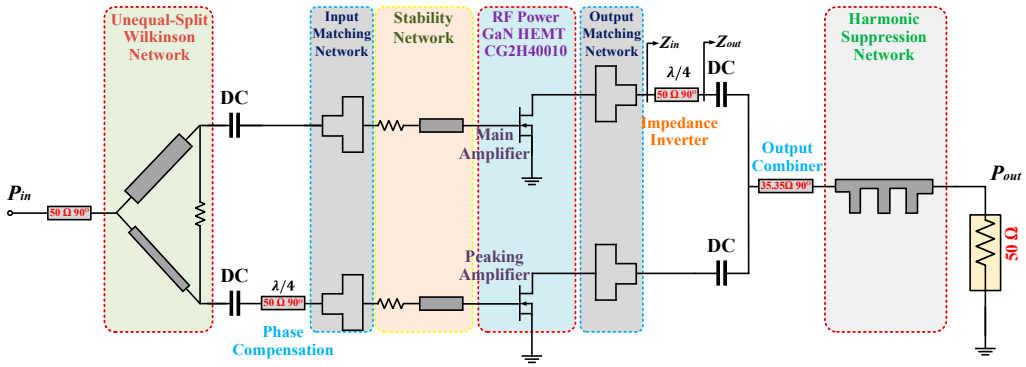



**Figure 1.** An illustration of the planned Doherty power amplifier.

In practical terms, the main amplifier efficiently handles low input power, achieving peak efficiency and voltage levels. However, when it reaches the breakpoint threshold, as depicted in Figure 2, the auxiliary amplifier dynamically adjusts the load and amplifies output power while maintaining high voltage levels and efficiency. According to theoretical considerations [10], the DE at the breakpoint is expected to be equivalent to the efficiency at saturation and remain consistently high across the entire Doherty region. However, the presence of parasitic components within the transistors and the knee voltage effect, which leads to a gradual and smoother activation of the auxiliary transistor, results in a decrease in the efficiency profile within the Doherty region. Consequently, the efficiency achievable in practical applications at the breakpoint is typically lower than the efficiency observed under the saturation point, as demonstrated in Figure 2.

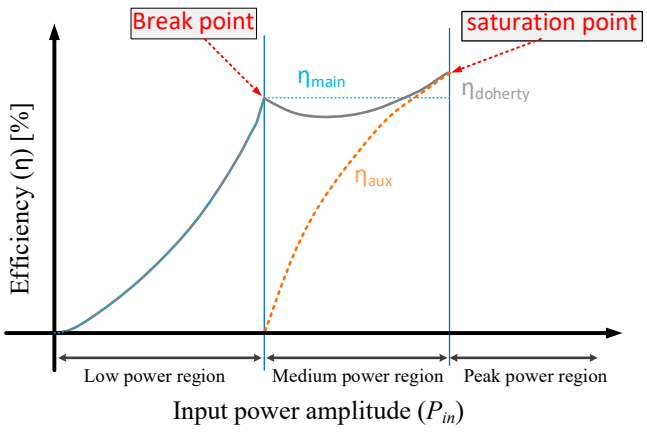



**Figure 2.** Efficiency plot for the Doherty amplifier against input power [9].

The DPA's performance factors include output power, gain, linearity, and efficiency. Drain efficiency (*DE* or $\eta$) is defined as:

$$DE = \eta(\%) = \frac{P_{out}}{P_{DC}} \times 100 = \frac{0.5V_{out} * I_{out}}{(V_{dc,main} * I_{dc,main}) + \left(V_{dc,peak} * I_{dc,peak}\right)} * 100, \quad (1)$$

where $P_{out}$ and $P_{DC}$ are output DC power provided by the PA, $V_{out}$ and $I_{out}$ are output voltage and current at the fundamental frequency, and $V_{dc,main}I_{dc,main}$ and $V_{dc,peak}I_{dc,peak}$ are the DC power of the main and peak PA, respectively.

Power-added efficiency (*PAE*) is another efficiency indicator defined as:

$$PAE(\%) = \frac{P_{out} - P_{in}}{P_{DC}} \times 100, \quad (2)$$

Gain (*G*) is calculated as:

$$G(dB) = 10\log\left(\frac{P_{out}}{P_{in}}\right) \text{ [dB]}, \quad (3)$$

## 3. Circuit Design of RF DPA

### *3.1. Design of Wilkinson Power Divider*

Reference [23] indicates that the small-signal gain decreases by 3 dB when the auxiliary amplifier splits an input signal into two equal-phase output signals using a Wilkinson power divider (Figure 3). This power divider equally splits the input power (port 1) into two equal-phase output signals (port 2 and port 3), maintaining matched states and offering isolation between the output ports. The formulas below demonstrate how to calculate the Wilkinson power divider parameters [27–41]:

$$Z_1 = Z_0\left[\left(\frac{P_{main}}{P_{peak}}\right)^{-1.5} + \left(\frac{P_{main}}{P_{peak}}\right)^{0.5}\right]^{0.5}, \quad (4)$$

$$Z_2 = Z_0\left(1 + \frac{P_{main}}{P_{peak}}\right)^{0.5}\left(\frac{P_{main}}{P_{peak}}\right)^{0.25}, \quad (5)$$

$$Z_3 = Z_0\left(\frac{P_{main}}{P_{peak}}\right)^{-0.25}, \quad (6)$$

$$Z_4 = Z_0\left(\frac{P_{main}}{P_{peak}}\right)^{0.25}, \quad (7)$$

$$R_w = Z_0\left[\left(\frac{P_{main}}{P_{peak}}\right)^{0.5} + \left(\frac{P_{main}}{P_{peak}}\right)^{-0.5}\right], \quad (8)$$

where $Z_0$ represents the normalized impedance (typically 50 Ω), $R_w$ is the isolation resistance, and $P_{main}$ and $P_{peak}$ represent the output power of the main branch (port 2) and the auxiliary branch (port 3), respectively.

In our design, we implemented Wilkinson's power divider with an unequal split to send more power to the main amplifier, resulting in a significant gain increase while reducing the auxiliary amplifier's power demand, allowing it to operate at a less deep class-C level. By adjusting the division factor (*Q*) value, defined as $Q = P_{main}/P_{peak}$, the power distribution between ports 2 and 3 can be altered.

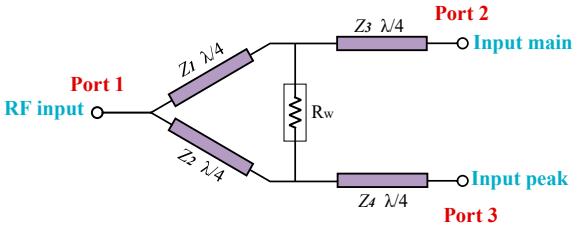



**Figure 3.** Wilkinson power divider's basic layout.

Table 1 displays branch impedances ($Z_1$, $Z_2$, $Z_3$, and $Z_4$) and isolation resistance ($R_w$) with varying division factor ($Q$) values. The values were obtained through simulations with ADS software, adjusting the division factor to achieve the desired power division ratio. It is important to note that these values depend on the specific design and substrate properties, and may vary based on the actual power divider design. The optimal division factor ($Q$) for our proposed circuit was determined as 2.5 after considering critical factors, gain, and PAE, as shown in Figure 4.

**Table 1.** Branch Impedances and Isolation Resistance with Sweep of Division Factor ($Q$).

| $Q$ | $Z_1$ (Ω) | $Z_2$ (Ω) | $Z_3$ (Ω) | $Z_4$ (Ω) | $R_W$ (Ω) |
|---|---|---|---|---|---|
| 0.5 | 102.988 | 51.494 | 59.46 | 42.045 | 106.066 |
| 1 | 70.711 | 70.711 | 50 | 50 | 100 |
| 1.5 | 58.327 | 87.491 | 45.18 | 55.334 | 102.062 |
| 2 | 51.494 | 102.988 | 42.045 | 59.46 | 106.066 |
| 2.5 | 47.049 | 117.622 | 39.764 | 62.872 | 110.68 |
| 3 | 43.869 | 131.607 | 37.992 | 65.804 | 115.47 |
| 3.5 | 41.45 | 145.075 | 36.556 | 68.389 | 120.268 |
| 4 | 39.528 | 158.114 | 35.355 | 70.711 | 125 |
| 4.5 | 37.953 | 170.787 | 34.329 | 72.824 | 129.636 |
| 5 | 36.628 | 183.142 | 33.437 | 74.767 | 134.164 |

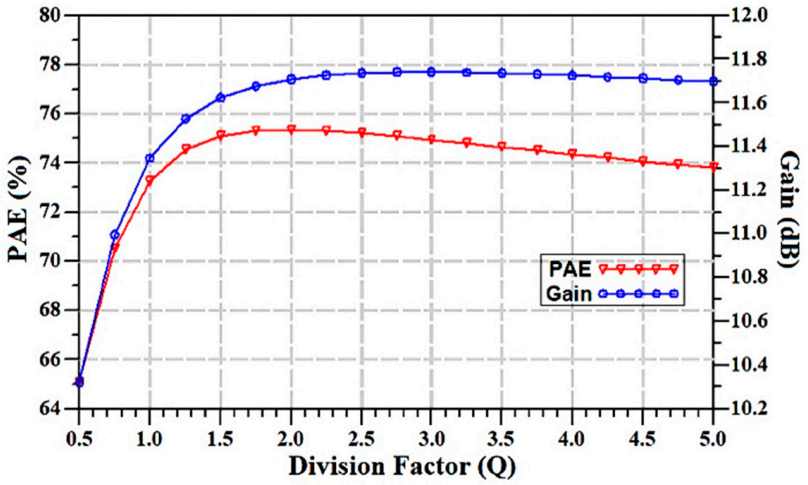



**Figure 4.** The gain and PAE of the proposed circuit with a sweep of division factor ($Q$).

The diagram in Figure 5 illustrates the layout and the simulated performance of the unequal Wilkinson power divider. Return loss was below −17 dB over the entire band (3.3–3.8 GHz). The isolated port was connected to allow for the insertion of an external resistor.

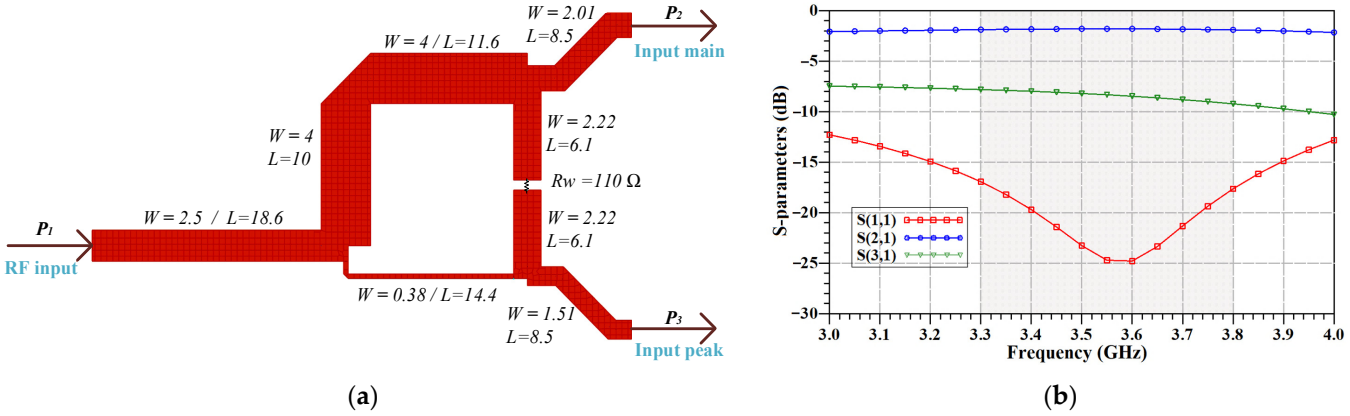



**Figure 5.** Unequal Wilkinson power divider. (**a**) The layout (dimension in mm). (**b**) EM simulation result versus frequency.

### *3.2. Load Modulation in DPAs*

Load modulation in DPAs enhances efficiency and linearity by adjusting the carrier amplifier's load impedance, optimizing its efficiency and reducing heat generation. It also aligns the carrier amplifier's load with the peaking amplifier's output power, reducing distortion and enhancing signal quality. When combined with techniques like bias modulation and envelope tracking, it further improves DPA performance. Both amplifiers employ an output combiner with quarter-wavelength transmission lines, providing a 90-degree phase shift and contributing to load modulation. This modulation adjusts the impedance presented to the PA's output, varying with the current from the other device, as seen in Figure 6 [29].

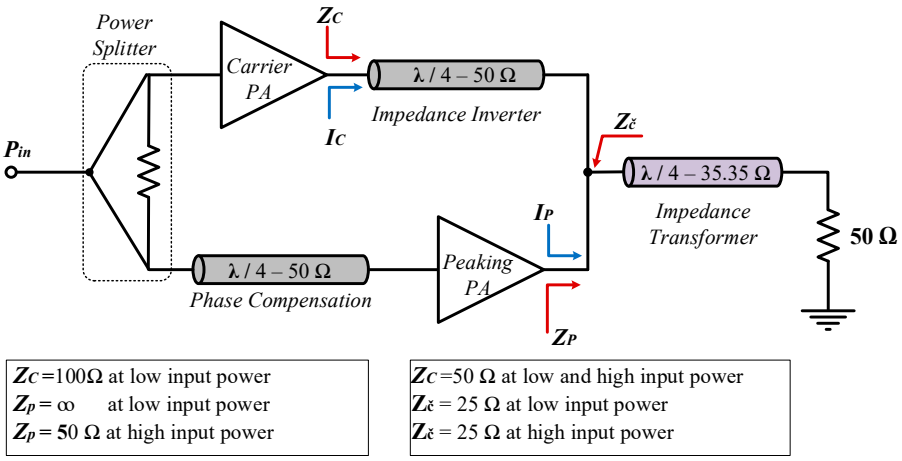



**Figure 6.** The schematic diagram of a DPA with the principle of load modulation for adjustment output impedance of the amplifier.

When the input power is low (in back-off conditions), only the carrier PA is active and the impedance presented to the peaking PA ($Z_P$) will be ∞. The impedance at the combination point $(Z_{\acute{C}})$ is first transformed to 25 ohms using the 35.35-ohm impedance transformer as per Equation (9), and the impedance presented to the carrier PA $(Z_C)$ is 100 ohms as per Equation (10). When the input power increases, the peaking PA becomes active. At this time, the output impedance presented to the carrier PA and the peaking PA are both 50 ohms as per Equation (10). In both conditions, considering the 35.35-ohm impedance transformer performance, the load impedances of the main and peaking amplifiers change based on given information and the value of impedance at the combination

point $(Z_{\acute{C}})$ lead to 25 Ω. This impedance would be transformed to the output impedance ($R_L$= 50 Ω) using a 35.35 Ω impedance transformer as depicted in Figure 6.

$$Z_{\acute{C}} = (Z_T)^2/R_L, \tag{9}$$

$$Z_C = (Z_I)^2/[R_L(1 + (I_P/I_C))], \tag{10}$$

### *3.3. Design of Input- and Output-Matching Networks*

The broadband DPA operating from 3.3 GHz to 3.8 GHz, utilizing two 10 W GaN transistors (CG2H40010F from Cree), was designed to validate our proposed approach. We performed load-pull simulations on the selected high-power-density device using a drain bias of 28 V at 3.5 GHz to determine the desired output power and gain, and by using the source and load impedance values of the device from its datasheet, as displayed in Figure 7.

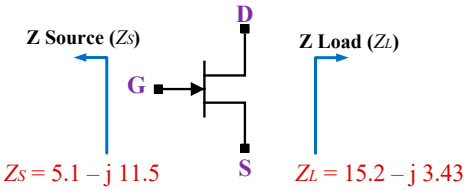
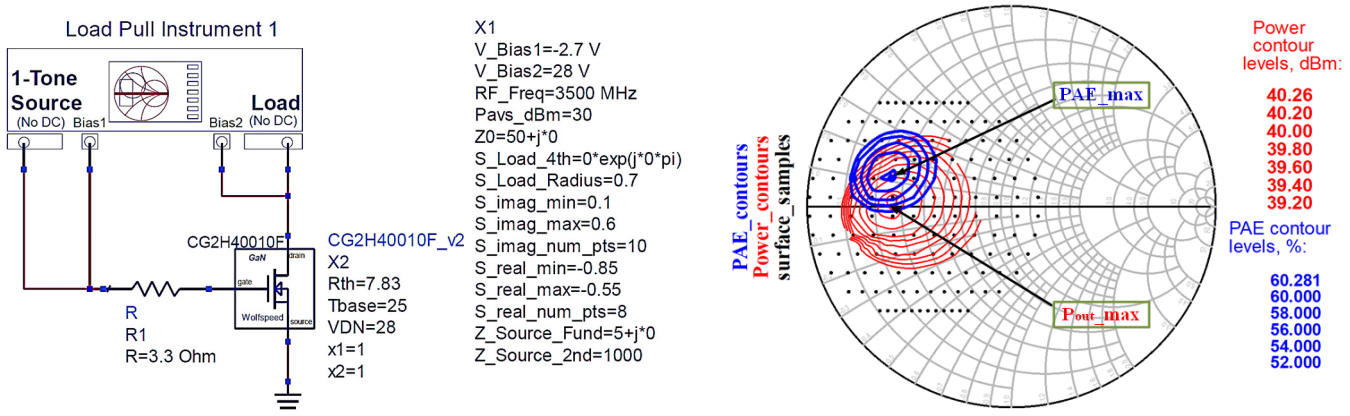



**Figure 7.** Source and load impedance of the transistor at 3.5 GHz, VDD = 28 V, and IDQ = 100 mA.

Designing DPA matching networks, including an input-matching network (IMN) and an output-matching network (OMN), is vital for optimizing performance. An IMN ensures efficient power transfer by matching DPA input impedance to the source, while an OMN matches the DPA load impedance. Keeping the PA's output reflection co-efficient below −10 dB is crucial, and ADS aids in determining actual input and output impedances. Load-pull simulations reveal power and PAE contours, e.g., CG2H40010F GaN HEMT's 3.5 GHz performance with 40.26 dBm output power and 60.28% PAE (Figure 8).




(**a**) (**b**)

**Figure 8.** (**a**) Setup simulations of load-pull analysis. (**b**) Load-pull results of PAE and output power contours.

The load-pull simulation revealed input and output impedances of 6.617 + j10.23 Ω and 13.28 + j1.518 Ω. The design employs distributed elements to match the power amplifier's input and output sections, fine-tuned across the bandwidth using the Smith chart utility tool in ADS. Optimized input and output networks were connected to the CG2H40010F, utilizing TLIN elements converted to MLIN. The final layouts with the optimized input- and output-matching networks for the main transistor are shown in Figure 9 and include the gate and drain biasing network. The procedure for designing input- and output-matching

networks for the auxiliary transistor mirrors the main transistor's approach. Figure 10 presents the final designs, detailing microstrip line dimensions and gate/drain bias values for the auxiliary transistor.

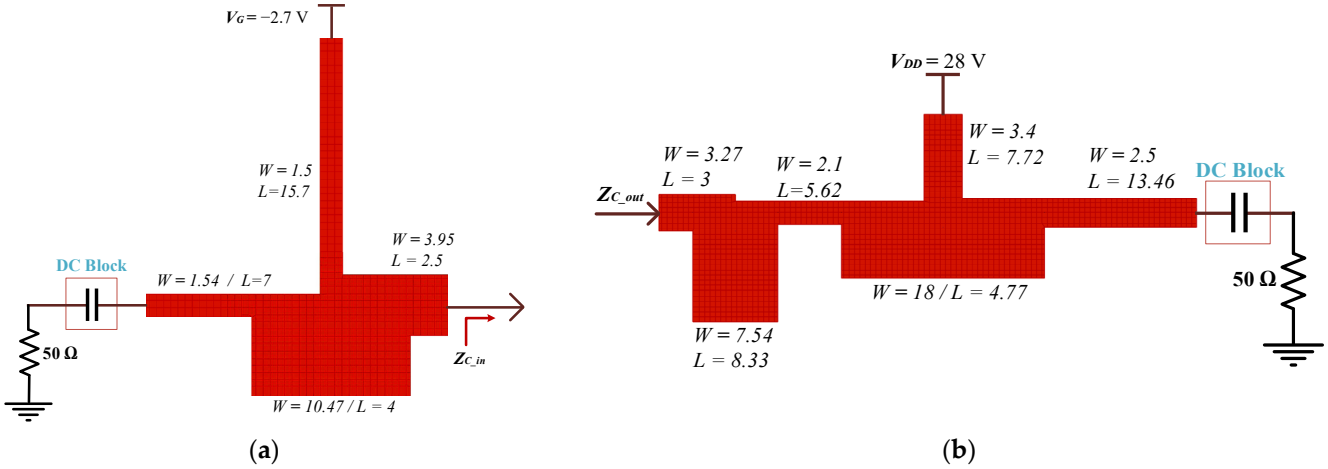



**Figure 9.** The layout of the (**a**) IMN of the main and (**b**) OMN of the main (dimensions in mm).

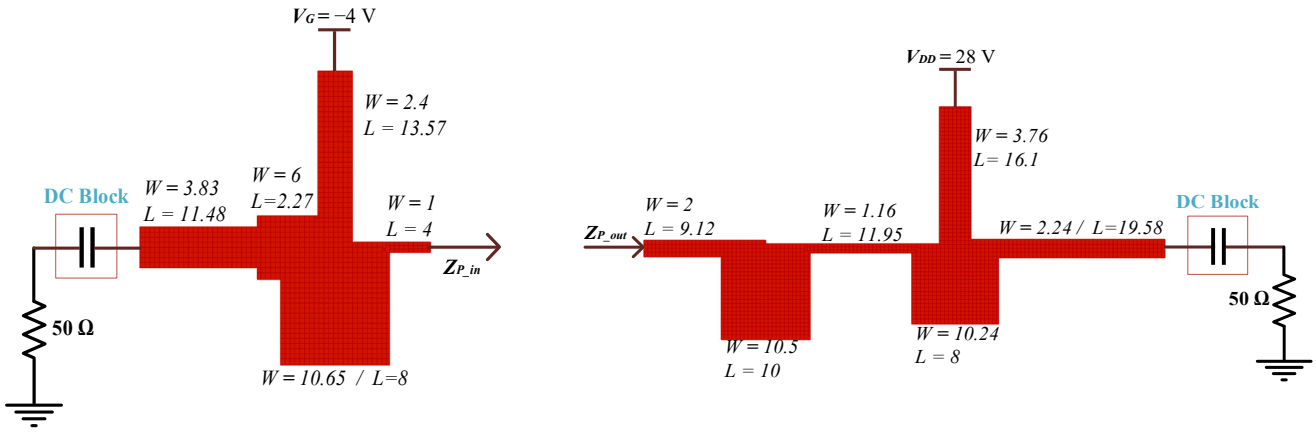



**Figure 10.** The layout of the (**a**) IMN of the peak and (**b**) OMN of the peak (dimensions in mm).

### *3.4. Stability Analysis*

Stability analysis plays a crucial role in DPA design, ensuring the amplifier's reliability under various conditions. The stability of a DPA is influenced by several factors, including impedance matching, load and source impedance, bias settings, and the characteristics of the power combiner. To function effectively as an RF power amplifier instead of an oscillator, a DPA must possess a stability factor (K) greater than 1 [30]. One commonly used method for assessing unconditional stability, where K > 1, is Rollet's condition, which relies on the value of K. However, while the K-Δ test provides a mathematical evaluation of unconditional stability, it does not enable straightforward comparisons between different devices due to its reliance on two separate parameters. A newer criterion, utilizing a single parameter μ [31], has been introduced to gauge stability. When μ surpasses 1, the device is considered unconditionally stable, and higher μ values indicate greater stability.

According to the stability plot in Figure 11, the device is unconditionally stable through both the K-Δ Test and the μ-Test by adding a 3.3-ohm resistance in the gate pin of both transistors in the frequency range of 3 to 4 GHz. This finding makes the device appropriate for the DPA design proposed in the paper.

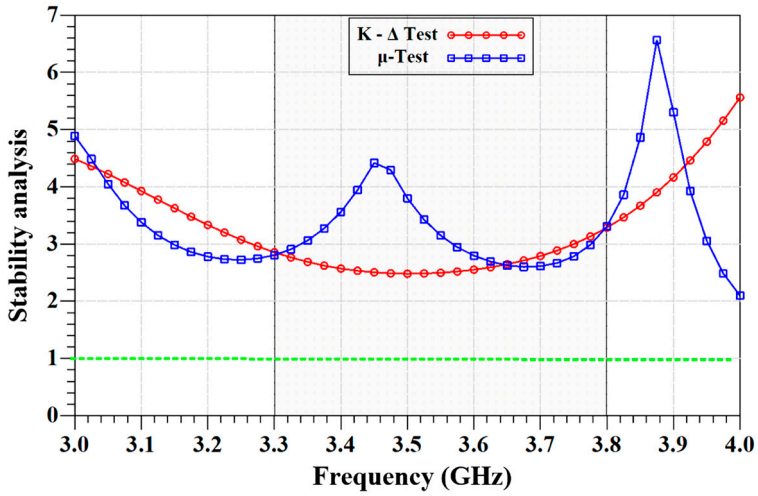



**Figure 11.** Stability analyses based on K-Δ test and μ-test.

### *3.5. Design of Harmonic Suppression Network*

DPA's post-harmonic suppression network aims to reduce the high-order harmonic content generated by the amplifier and thus increase the efficiency of our amplifier. This is achieved by designing the circuit such that the two active devices in the Doherty configuration, the main amplifier and the peaking amplifier, operate out of phase with each other. The design of a maximally flat (Binomial) low-pass filter, to be fabricated using microstrip lines, has a cutoff frequency of 4.5 GHz. By following the proposed filter specifications, it was determined that an order of 7 (N = 7) would suffice. Referencing [32], the prototype element values can be determined. The next step is to calculate the new filter component values from capacitors ($C'_k$) and inductors ($L'_k$) by means of Equations (11) and (12).

$$L'_k = \frac{R_0 L_k}{\omega_c}, \tag{11}$$

$$C'_k = \frac{C_k}{R_0 \omega_c}, \tag{12}$$

where $\omega_c$ is the cutoff frequency; $L_k$ and $C_k$ are the component values for the original prototype; and $R_0$ is the nominal characteristic impedance equal to 50 Ω. To increase its reliability for use in high-frequency RF circuits, the lumped-element filter can be transformed into a system of distributed elements, such as open- or short-circuited transmission line stubs. This conversion can be achieved through the use of Richards' transformation, which transforms lumped elements into transmission line sections. The filter elements are then physically separated by applying Kuroda's identities to the transmission line sections [32].

Figure 12a presents the electrical transmission line schematic design of the harmonic suppression network, which has been carefully developed based on the previously discussed steps. The final layout of the network, shown in Figure 12b, displays the physical width and length of the design, including the integration of 35.35-ohm impedance transformers at the beginning of the network. To enhance the performance of the network, an additional series microstrip line has been added to ensure a 50-ohm connection to the output combiner, ensuring an appropriate width for welding the output port with the load. To ensure a smooth transition from the electrical microstrip lines shown in Figure 12a to the physical lines in Figure 12b, and prevent any junction discontinuity, a T-junction model has been added. To ensure that the performance of the network was not impacted by the additions made to it, an improvement was made to the network values using the Optimization Cockpit tool in ADS. The result of this optimization can be seen in the frequency response of the electromagnetic simulation results for the proposed network, which is displayed in Figure 13.

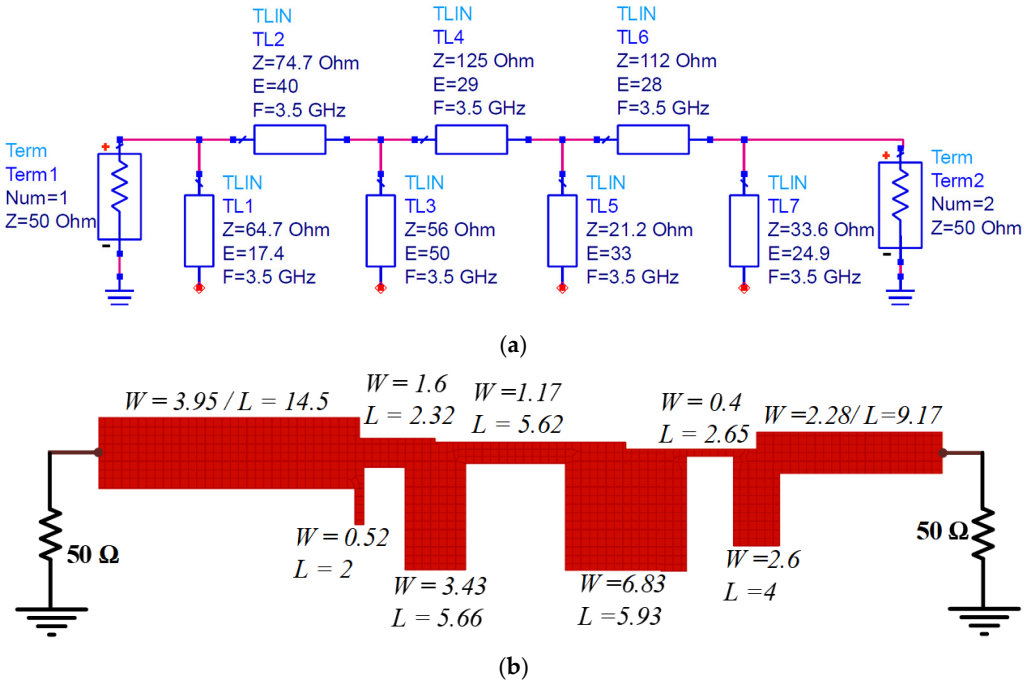



**Figure 12.** Harmonic suppression network design. (**a**) Ideal transmission line schematic. (**b**) Layout design with dimensions in mm.

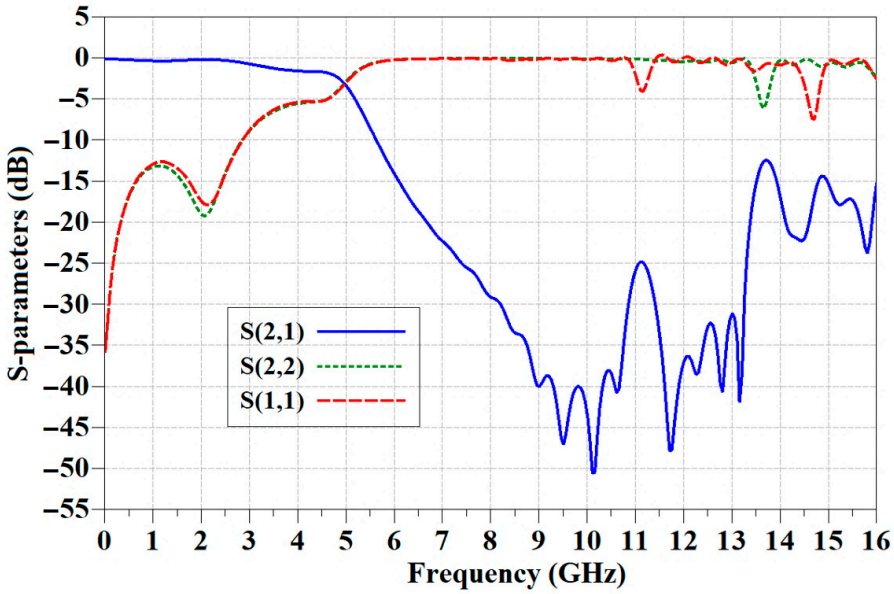



**Figure 13.** Results of the electromagnetic simulation of S-parameters for the proposed harmonic suppression network.

## 4. Implementation and Simulation Results of the N78 Band Sub-6 GHz DPA

The final circuit design of the DPA is shown in Figure 14 and is composed of several parts: an unequal Wilkinson power divider to split the input signal, a phase compensation network to correct the phase difference between the carrier and peaking branches, and input-matching networks, consisting of two identical CG2H40010F devices. Additionally, the design features output-matching networks, an impedance inverter network, and a harmonic suppression network with a 35.35-ohm impedance transformer. To enhance performance, bypass capacitors with a high Q factor of 500 were added to the DC biasing line for amplifiers $C_1$, $C_2$, $C_3$, and $C_4$, with capacitance values of 1 pF. The DC coupler

comprises surface mount device (SMD) capacitors $C_5$, $C_6$, $C_7$, and $C_8$ with capacitance values of 15 pF. The DPA was fabricated on a Rogers RT/duroid 5880 substrate, which has a relative dielectric constant (εr) of 2.2, a substrate thickness (H) of 31 mil, a loss tangent (Tan δ) of 0.0009, and copper conductors with conductivity (σ) of $5.8 \times 10^3$ and a thickness (T) of 0.035 mm. The main and auxiliary amplifiers are powered by the same drain bias voltage ($V_{DS}$) of 28 V, with the main gate bias voltage being set at −2.7 V and the auxiliary gate bias voltage set at −4 V. The scatter parameters of the designed DPA are displayed in Figure 15. The simulation results indicate that despite a slight shift towards lower frequencies, the DPA maintained a small-signal gain of approximately 14 dB within a 600 MHz bandwidth ranging from 3.20 GHz to 3.80 GHz, providing full coverage of the N78 frequency band. Additionally, input matching was achieved with better than 13 dB across the operating range from 3.20 GHz to 3.90 GHz. The output matching was approximately 13 dB in the higher portion of the operating band, ranging from 3.2 to 3.9 GHz, but slightly decreased towards the lower end of the band.

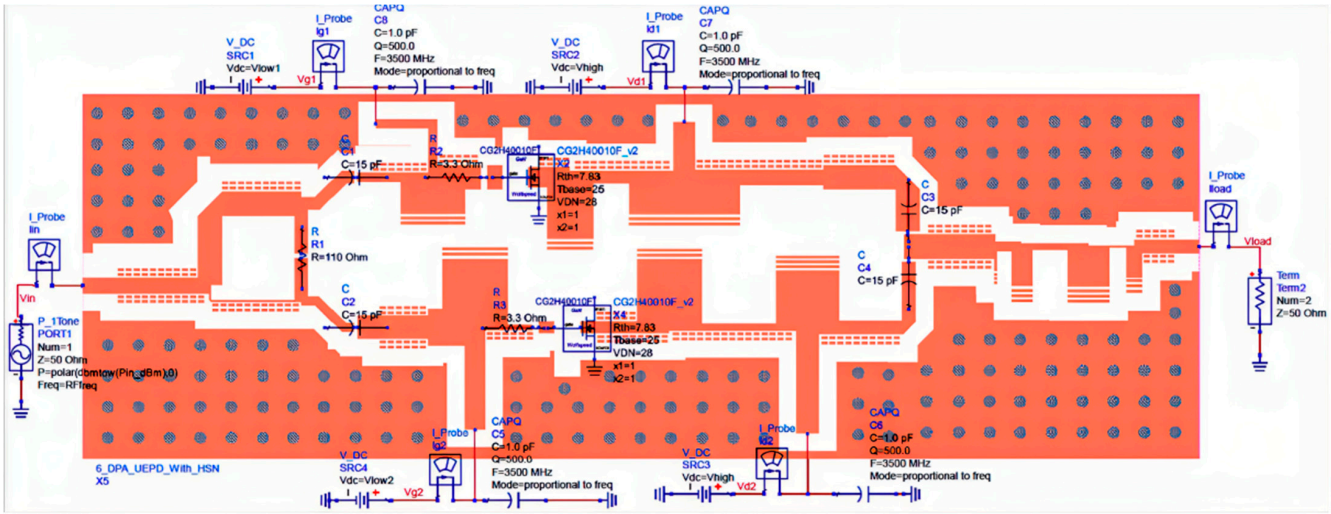



**Figure 14.** Completely layout design of the proposed Doherty power amplifier.

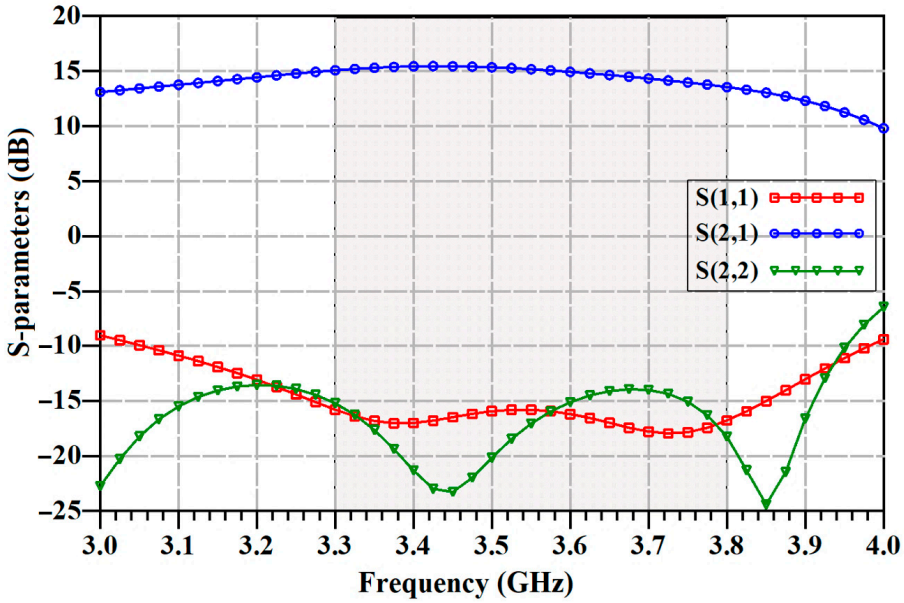



**Figure 15.** The scattering parameters of the proposed DPA.

### *4.1. Simulated DPA Performance*

This section presents the results of the designed Doherty power amplifier, including curves of output power, power gain, and power-added efficiency (PAE). Figure 16 illustrates the simulated values of output power (Pout), amplifier gain, drain efficiency (DE), and power-added efficiency (PAE) plotted against the input power (Pin), which is scaled from 0 to 40 dBm. In Figure 16a, it can be observed that the large-signal gain during nominal operation is approximately 15.7 dB when the input power is at 10 dBm. To achieve a 3 dB compression point value (P3dB) for our design, the Pin value needs to be set at 29.2 dBm. Consequently, the output power is approximately 41.8 dBm at P3db when the Pin value is at 29.2 dBm. The simulated plot of both the drain efficiency and the power-added efficiency of the proposed DPA design is presented in Figure 16b, when getting 78.4% and 74.3% of the P3dB, respectively. Compared with the efficiency characteristics of a non-Doherty power amplifier (class AB) bias conditions, we obtain a PAE at the P3db point of 55% and 58% for DE, as shown in Figure 17. The corresponding intrinsic drain voltage and current waveforms of the designed DPA are depicted in Figure 18.

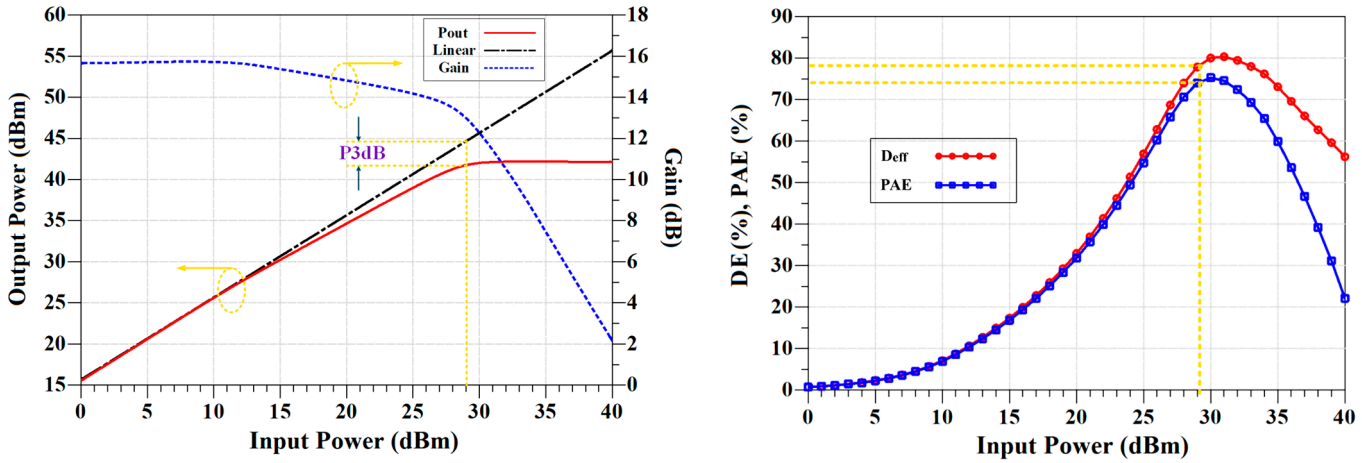



**Figure 16.** The results of the designed DPA. (**a**) Large-signal gain and output power. (**b**) PAE and DE, in terms of input power.

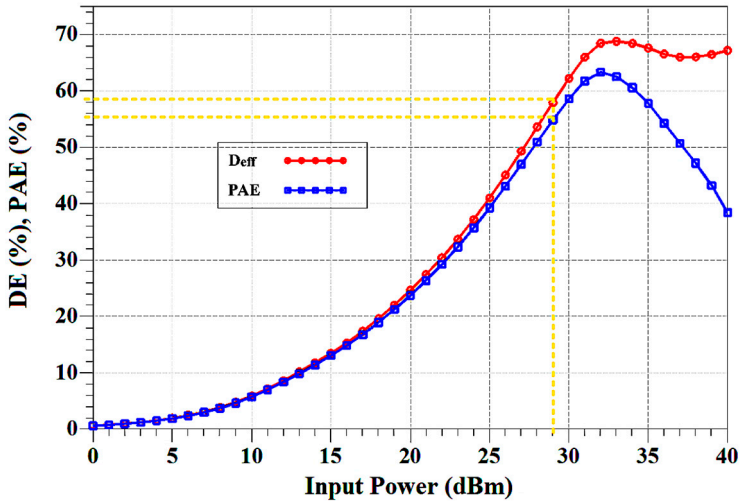



**Figure 17.** Drain efficiency and PAE versus input power for non-Doherty (class AB) bias conditions.

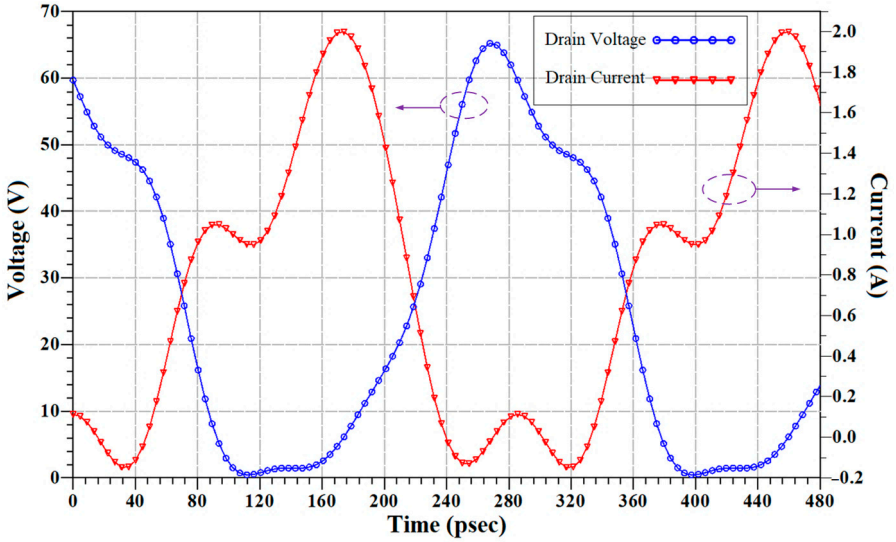



**Figure 18.** Simulated time-domain curve of intrinsic drain voltage and current of the designed DPA.

### *4.2. Performance Comparison of Three DPA Designs*

In this section, we present and analyze results for three DPA designs in Figure 19, all of whose design parts have been discussed previously. The first design, labeled as (EPD without HS), utilizes an equal Wilkinson power divider but lacks a harmonic suppression network. The results of this design can be seen in Figure 19 as the solid blue line with a square symbol. The second design, labeled as (UPD without HS), is another DPA that employs an unequal Wilkinson power divider and does not include a harmonic suppression network. In Figure 19, the results of this design are represented by the solid green line with a triangle symbol. Lastly, the third design, identified by the labeled (UPD with HS), features an unequal Wilkinson power divider along with a harmonic suppression network. The results of this design can be seen in Figure 19 as the solid red line with a circle symbol.

This paper proposes adopting the third design of the DPA, which incorporates a post-harmonic suppression network on the output in addition to an unequal Wilkinson power divider on the input. The performance of the proposed amplifier in the third design was compared to the previous two designs, and the results are summarized in Table 2. The large-signal gain of the amplifier in the proposed design reaches 12 dB, representing a 15% improvement over the first design and a 4% improvement over the second design, as shown in Figure 19a. There is also an improvement in the output power of the amplifier, which reaches 41.85 dBm, an increase of 4.6% over the first design and 1.6% over the second design, as shown in Figure 19b. Although the improvement in gain and output power values is not substantial due to the harmonic suppression network being considered a load on the output of the amplifier, its impact is evident in the improved drain efficiency and power-added efficiency, which reached 75.4% and 70.6%, respectively, representing a 64.6% and 69.5% improvement over the first design, and a 33.2% and 34.2% improvement over the second design, as shown in Figure 19c,d.

**Table 2.** Summary of the performance of the three DPA designs.

| Parameter / Design | Gain (dB) | | Pout (dBm) | | DE (%) | | PAE (%) | |
|---|---|---|---|---|---|---|---|---|
| | Value | Improvement | Value | Improvement | Value | Improvement | Value | Improvement |
| EPD without HS | 10.43 | - | 40 | - | 45.8 | - | 41.7 | - |
| UPD without HS | 11.54 | 10% | 41.2 | 3% | 56.57 | 23.5% | 52.6 | 27% |
| UPD with HS | 12 | 15% | 41.85 | 4.6% | 75.4 | 64.6% | 70.6 | 69.5% |

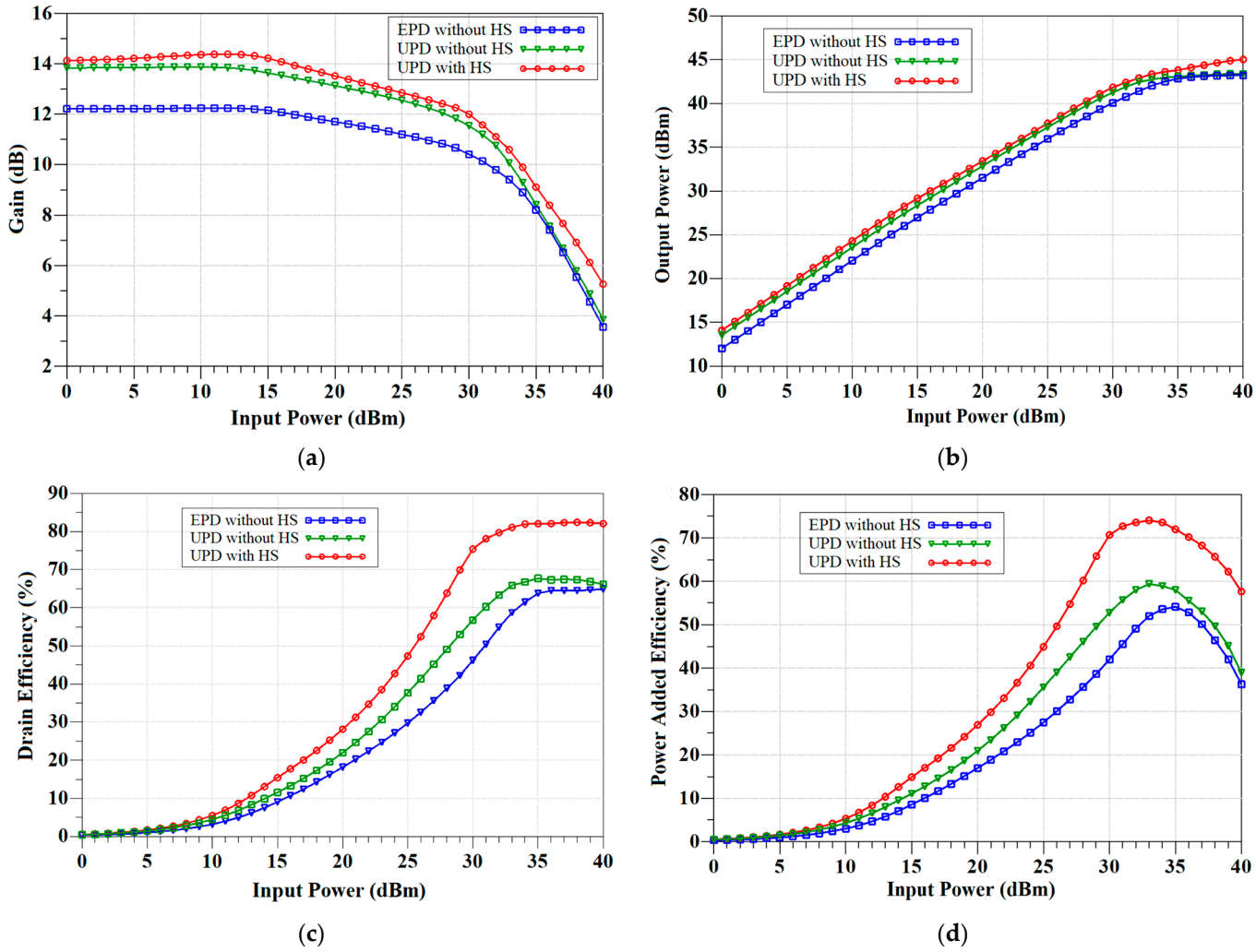



**Figure 19.** Performance comparison of the three DPA designs versus input power: (**a**) large-signal gain, (**b**) output power, (**c**) drain efficiency, and (**d**) power-added efficiency at saturation.

### *4.3. The Performance of the Unequal Wilkinson Power Divider*

Figure 20 displays a photograph of a 2.5:1 Wilkinson power divider that underwent fabrication and subsequent connection to a vector network analyzer device. This connection allowed for the measurement of its circuit S-parameters, focusing on a central frequency of 3.5 GHz. Figure 21 presents a comparison between the measurement and simulation results, utilizing CST Studio Suite software version 2021, for the proposed unequal divider. The measurements revealed insertion loss values of approximately 2 dB for S21 and 7.2 dB for S31, both at 3.5 GHz. Additionally, the output port isolation (S23) exhibited performance better than 12 dB, indicating effective isolation between the two output ports. The measured return loss (S11) also surpassed 20.6 dB at 3.4 GHz. However, some inconsistencies between the simulation and measurement outcomes were observed in Figure 21. These disparities could be attributed to unforeseen variations that occurred during the fabrication and assembly processes. Furthermore, the decision to employ two 220 Ω resistors in parallel, necessitated by the unavailability of a single 110 Ω resistor in the Egyptian market, may have played a role in these observed discrepancies.

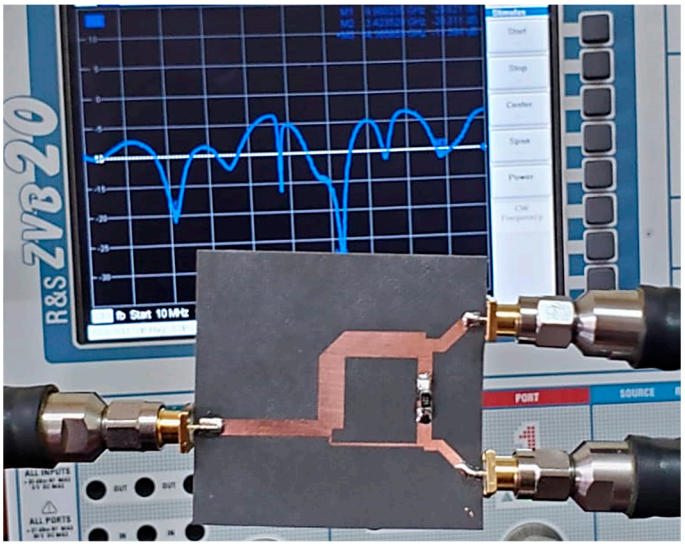



**Figure 20.** Photograph of the fabricated 2.5:1 unequal Wilkinson power divider.

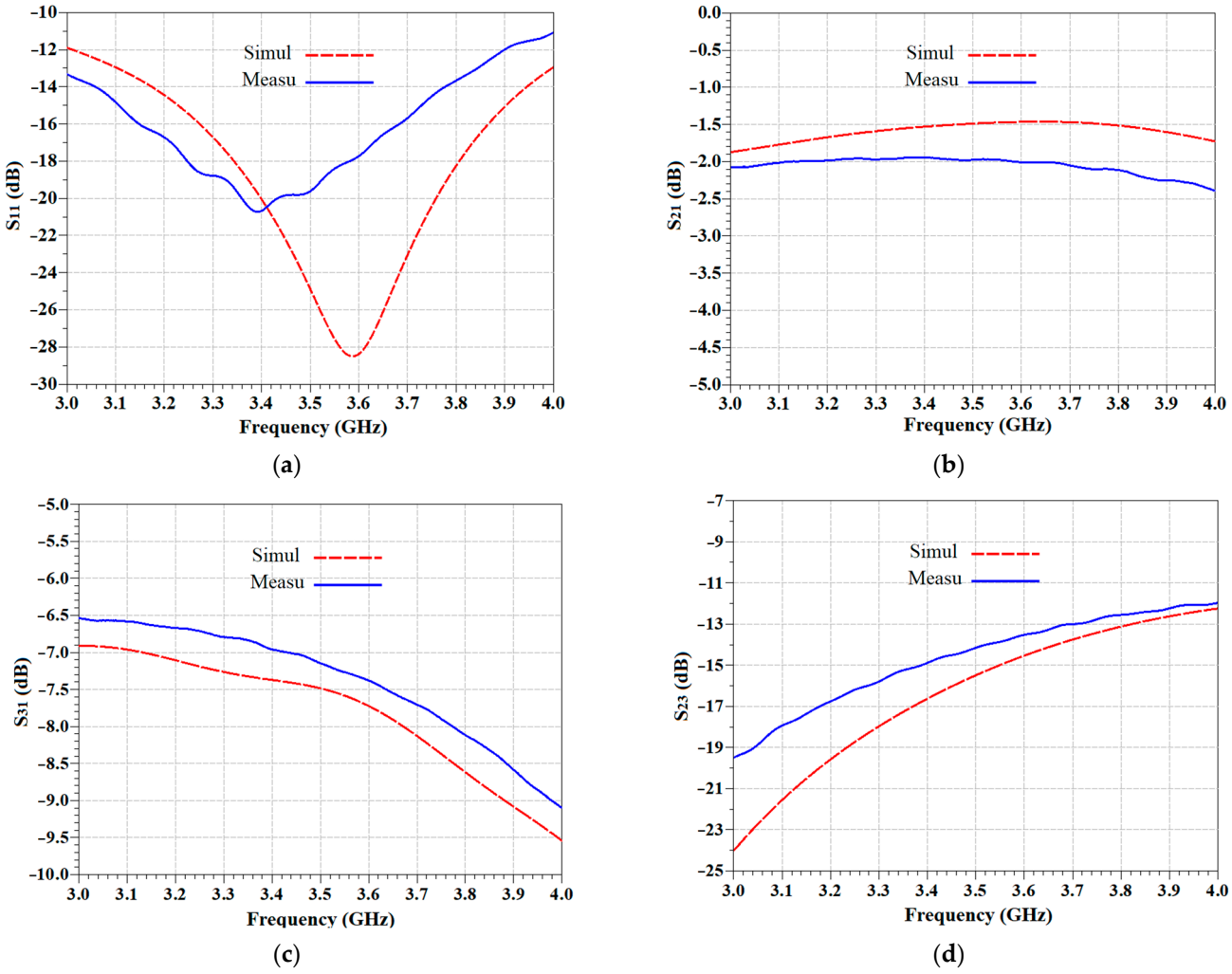



**Figure 21.** Simulated (dashed) and measured (solid) scattering parameters of the 2.5:1 Wilkinson power divider. (**a**) S11, (**b**) S21, (**c**) S31, and (**d**) S23.

### *4.4. The Performance of the Harmonic Suppression Network*

Figure 22 displays a photograph of the post-harmonic suppression network that was fabricated and combined with a 35.35-ohm impedance transformers microstrip line at the input port and a 50-ohm microstrip line at the network end to allow sufficient soldering space for the SMA coaxial connectors. The response of the proposed filter was measured using an R&S® ZVB vector network analyzer from 0 to 16 GHz, and the results are shown in Figure 23. To make the measurement easy, the source/load impedances of the filter were set at 50 Ω, and the filter exhibited a seventh-order general Binomial low-pass response that was visible. The measured response (blue solid line) of the filter had a low-pass characteristic with a 3 dB cutoff frequency of 4.9 GHz. The insertion loss reached 10 dB at 5.5 GHz and 26.3 dB at 7 GHz. These measurements were in good agreement with the simulated results.

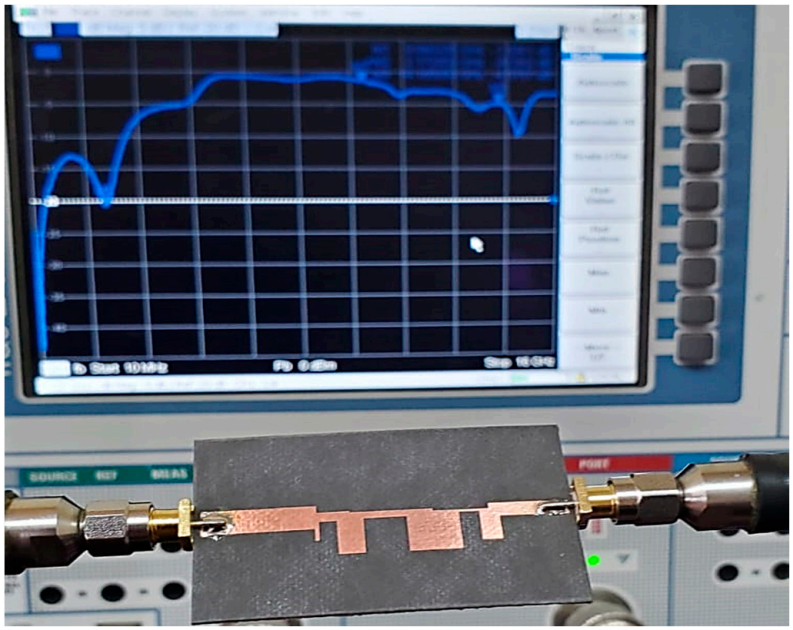


**Figure 22.** Photograph of the fabricated post-harmonic suppression network.

Figure 24 illustrates the effect of our proposed design (DPA with HS) on the attenuation output power of harmonics from the second to the fourth order in comparison to the harmonic content of a conventional DPA (DPA without HS) in terms of input power. The results demonstrate that the suggested topology provides excellent harmonic suppression with high efficiency versus input power. Although the Doherty amplifier is a balanced amplifier, our design considered the fundamental frequency. We incorporated a suggested harmonic suppression network at the output to prevent the occurrence of harmonics, which is clearly demonstrated in the harmonic balance simulation results shown in Figure 25. The impact of the post-harmonic suppression network is illustrated by comparing the harmonic spectra at the output of the RF amplifier. Figure 25 displays the spectra of four harmonics for power, voltage, and current obtained from the harmonic balance (HB) simulation. Each spectrum figure includes DC (0 Hz), fundamental (3.5 GHz), second (7 GHz), third (10.5 GHz), and fourth (14 GHz) harmonic components. Notably, the values of the second to fourth harmonics are all below −50 dBm, providing evidence of the effective suppression achieved by the proposed harmonic suppression network. This successful suppression contributes to increased amplifier efficiency and improved linearity of the output signal. These findings are further supported by the simulated time-domain output voltage and current waveforms for the proposed DPA, as illustrated in Figure 26.

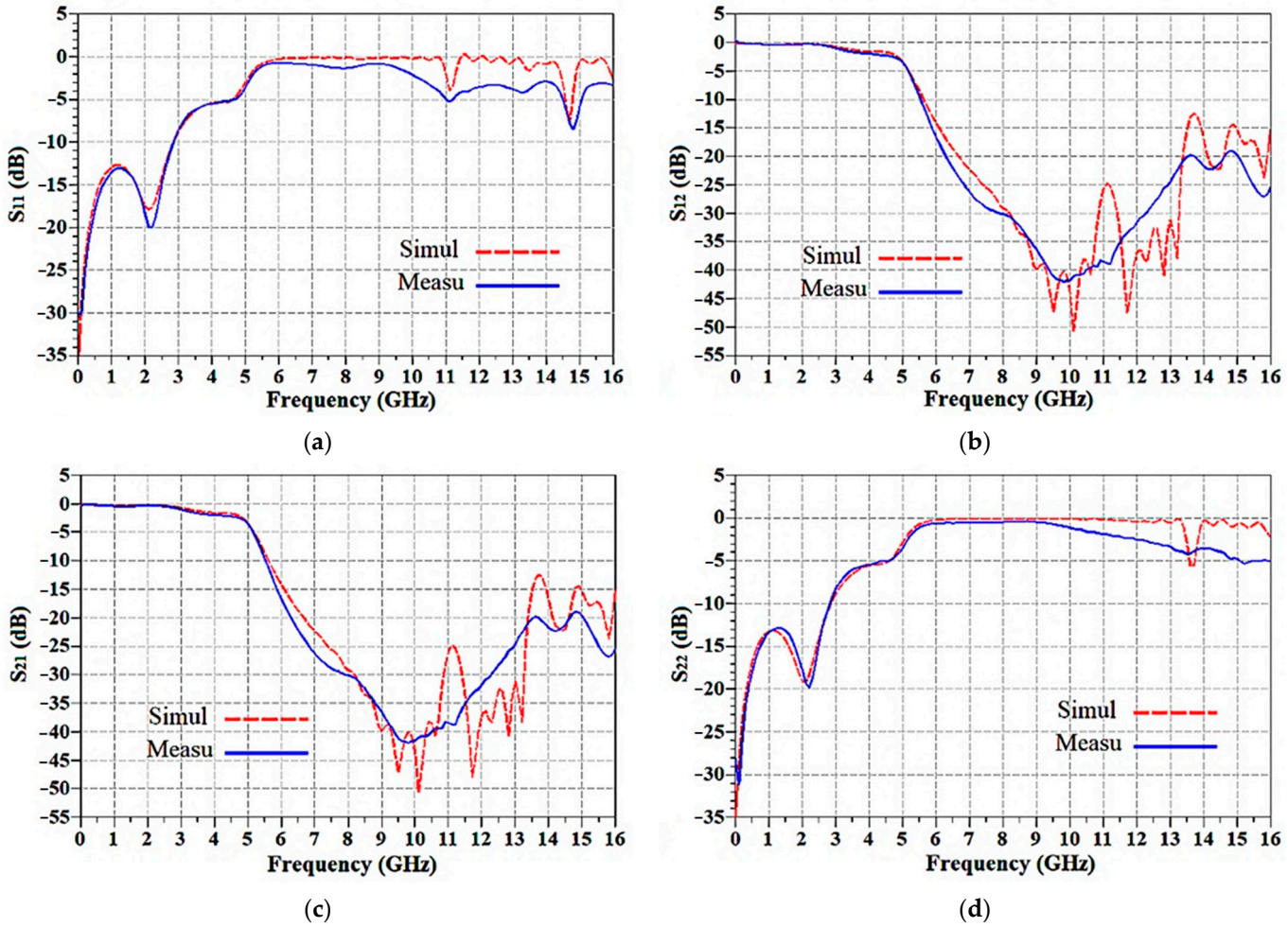



**Figure 23.** Results of the electromagnetic simulation (dashed) and measured (solid) S-parameters for the proposed harmonic suppression network. (**a**) S11, (**b**) S12, (**c**) S21, and (**d**) S22.

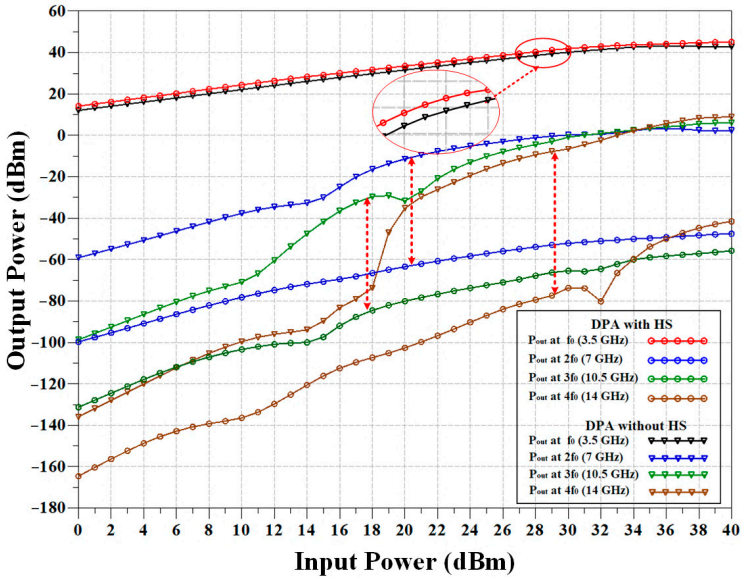
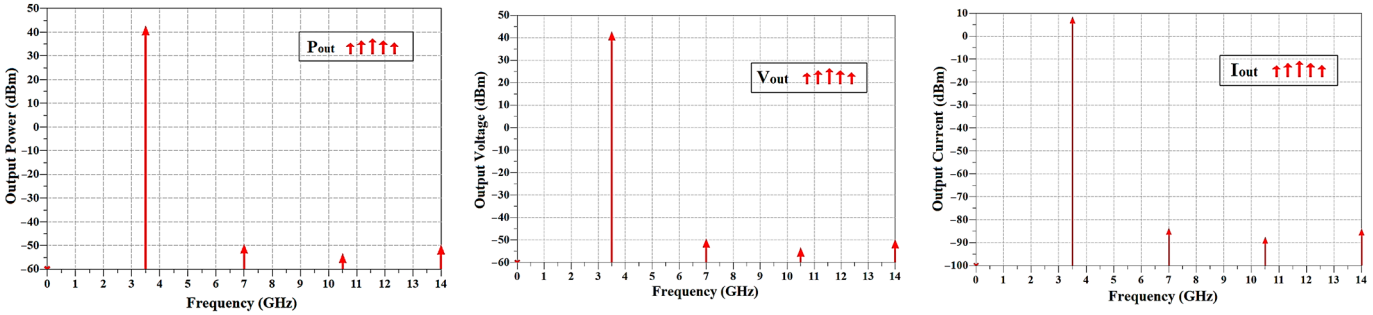



**Figure 24.** Comparison of power reduction at harmonic frequencies between the proposed design (DPA with HS) and the conventional design (DPA without HS).




(**a**) (**b**) (**c**)

**Figure 25.** Spectrum in dBm for four harmonics for (**a**) output power, (**b**) output voltage, and (**c**) output current.

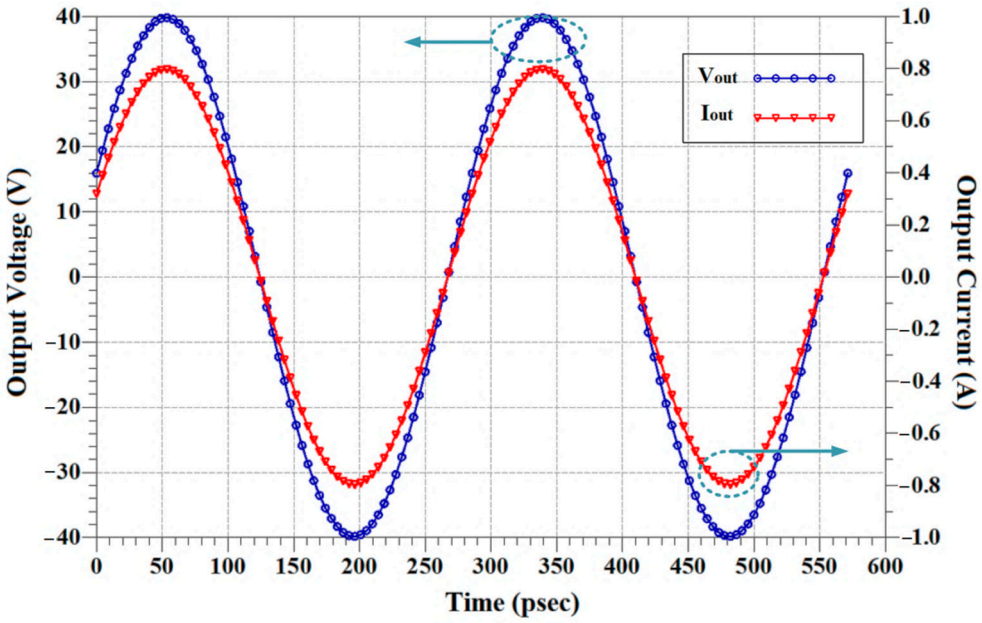



**Figure 26.** Steady-state time-domain output voltage and current waveform for proposed DPA.

The proposed DPA components were assembled with the addition of two transmission lines for 50-ohm impedance at the input and output ports. Optimizing these transmission lines, converted from electrical lengths to physical dimensions, yielded the highest results via EM simulation (Figure 27). This simulation confirms the DPA's proper operation within the 3.3–3.8 GHz frequency range, as seen in Figure 27. The parameters of gain, output power, DE, and PAE at the center frequency of 3.5 GHz are presented. Notably, maximum PAE and DE values reach around 75.2% and 80%, respectively, while the amplifier achieves a large-signal gain exceeding 12 dB and an output power of approximately 42 dBm. As previously discussed, the proposed DPA structure significantly enhances PAE, DE, and gain. These improvements were investigated by implementing an unequal Wilkinson power divider at the amplifier's input and introducing a harmonic suppression network at the output.

Table 3 offers a performance summary of the DPA designed in this study, comparing it with other studies focusing on Doherty amplifier design within the 6 GHz frequency band for 5G applications. Wherever feasible, we have used the same device for comparison, with the assessments relying on simulation results. Our proposed DPA, as discussed earlier, achieved notable PAE levels and demonstrated a broad bandwidth. This performance aligns with existing technologies in this frequency range, affirming the suitability of our straightforward and efficient broadband approach for 5G applications in the N78 band.

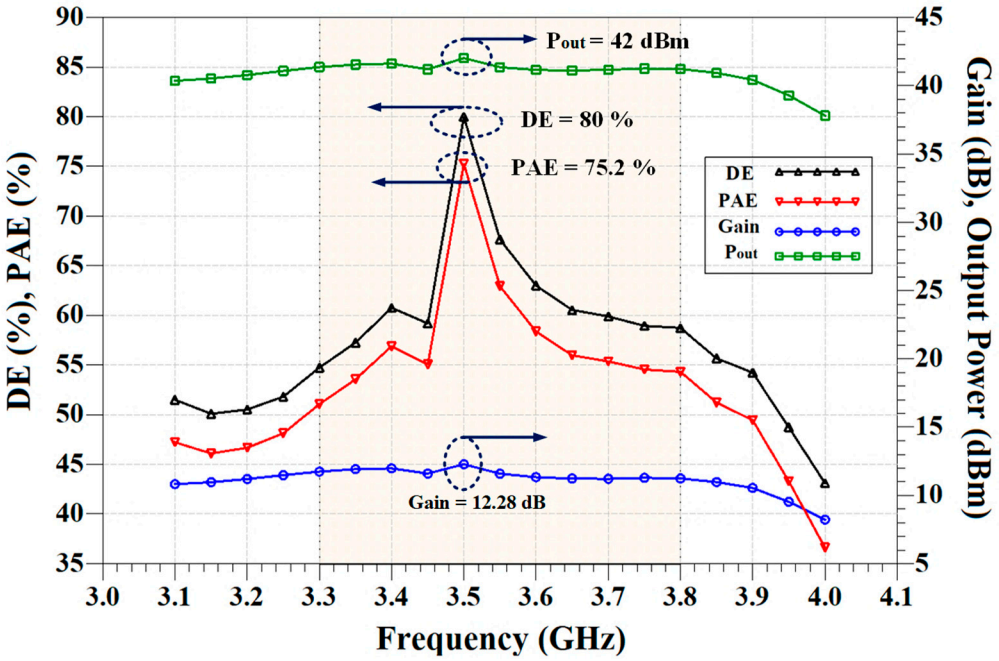



**Figure 27.** The gain, output power, DE, and PAE for the proposed DPA from 3.1 GHz to 4 GHz.

**Table 3.** Performance comparison of this work with similar works based on simulation.

| Ref. | Frequency (GHz) | Pout (dBm) | PAE (%) | Gain (dB) | Transistor |
|---|---|---|---|---|---|
| [6] | 2.8–3.3 | 43–44.2 | 62–76.5 (DE) | 8–13.5 | CGH40010F |
| [7] | 2.9–3.3 | 43.9–44.7 | 70.8–73.3 (DE) | 6–11 | CGH40010F |
| [33] | 4.5–5.3 | 39.5 | 44–54 | 11 | HIWAFER 0.25 µm GaN |
| [34] | 1.7–2.2 | 42.5 | 58–72 | 8.2–10.2 | 10 W Cree GaN HEMT |
| [35] | 1.2–1.6 | 33 | 60 | 19 | GaAs pHEMT |
| [36] | 1.4–2.1 | 34 | 35.7 | 12.7 | CGH40010F |
| [37] | 3.4–3.8 | 43 | 70 | 8 | CG2H40010F |
| [38] | 3.5–4 | 41.7 | 49.6 | 11.1 | CGH40006S |
| [39] | 4.1–5.6 | 38.4–39.5 | 41.2–49 | 8.3–11.2 | GaN MMIC |
| [40] | 3–3.6 | 43–44 | 55–66 (DE) | 12 | CGH40010F |
| This Work | 3.3–3.8 | 42 | 75.2 | 12.2 | CG2H40010F |

## 5. Conclusions

In conclusion, this paper proposed a design for a high-efficiency GaN Doherty power amplifier for 5G applications within the band of 3.3 to 3.8 GHz and compared its results to those of the traditional DPA design. This paper implemented an unequal Wilkinson power divider, which significantly boosted PAE from 41.7% to 52.6% compared to the traditional DPA design. Additionally, we introduced a seventh-order post-harmonic suppression network at the amplifier's output, effectively attenuating second- to fourth-order harmonics to levels exceeding −50 dB. This enhancement not only improved linearity but also contributed to an overall increase in PAE, reaching 70.6% compared to the traditional DPA design. Consequently, our DPA design, incorporating both the unequal power divider and the post-harmonic suppression circuit, comprehensively enhances power amplifier performance in terms of gain, output power, and efficiency. To verify the simulation results, both the power divider and the harmonic suppression network were fabricated and measured. The simulation and measurement results are compared and showed good agreement, with some discrepancies due to unexpected variations during fabrication and assembly. The proposed DPA design achieved a gain of 12 dB, an output power of 42 dBm, a drain efficiency of 80%, and a power-added efficiency of 75.2%. These results demonstrate the suitability of the proposed power amplifier design for 5G applications in the sub-6 GHz

N78 band, which is the most widely used band in active 5G NR networks. Additionally, this research represents a noteworthy contribution to the field of RF power amplifiers for 5G applications and offers potential avenues for further studies in this domain.

**Author Contributions:** Conceptualization, M.A.E.E. and T.G.A.; Methodology, M.A.E.E., T.G.A. and H.A.I.; Software, M.A.E.E. and T.G.A.; Validation, T.G.A. and H.A.I.; Formal analysis, T.G.A., E.K.I.H. and M.A.; Investigation, H.A.I.; Data curation, A.J.A.A.-G. and M.A.; Writing—original draft, M.A.E.E. and T.G.A.; Writing—review & editing, M.A.E.E., E.K.I.H., A.J.A.A.-G., T.A.H.A. and M.A.; Visualization, T.A.H.A. and M.A.; Supervision, T.G.A., H.A.I., E.K.I.H. and M.A.; Project administration, A.J.A.A.-G. and M.A. All authors have read and agreed to the published version of the manuscript.

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**Data Availability Statement:** The data presented in this study are available on request from the corresponding authors.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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