An X-type Boost Multilevel Inverter Based on Switched Capacitor Cells with Low Voltage Stress and High Frequency Applications

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***Abstract*—A novel X-type boost switched capacitor multilevel inverter utilizing a single power supply is proposed. It has a great application potential in the field of new energy power generation and high frequency scenarios. The proposed topology mainly has the following advantages. Firstly, the proposed topology avoids the use of H-bridge to output bipolar level, so that the maximum inverse voltage stress of the switch does not exceed $4V_{dc}$. Secondly, the maximum switching frequency of the proposed topology is 3 times the fundamental frequency, which provides an opportunity for the application of the inverter in high frequency engineering. Thirdly, the charging of the bridge arm capacitors is synchronous, which simplifies the modulation strategy of the extended topology. Moreover, the operating principle of the topology was analyzed in detail, and the feasibility of the inverter and the correctness of the modulation strategy were verified.**

***Index Terms*—Multilevel, bipolar inverter, switched-capacitor, low voltage stress, self-balancing, boost.**

I. Introduction

Recently, the proportion of clean energy in the energy supply system has been increased. As a DC-AC energy conversion interface, multilevel inverters play an important role in photovoltaic power generation systems [1]. In addition, with the vigorous development of the multilevel inverter technology, multilevel inverters are also widely used in power distribution systems, electric vehicles, etc. [2]-[3]. Compared with the traditional two-level inverter, multilevel inverter has the advantages of low total harmonic distortion (THD), low electromagnetic interference (EI), low total standing voltage (TSV), and better matching of sinusoidal waveform. Therefore, the multilevel inverter is suitable for achieving efficient conversion in DC-AC links [4], [5]. The typical multilevel inverters include neutral point clamped (NPC) multilevel inverter, flying capacitor (FC) multilevel inverter and cascaded H-bridge (CHB) multilevel inverter [6], [7], [8]. NPC and FC inverters need to use a large number of diodes or capacitors for neutral point clamping when outputting multilevel, leading to complicated inverter structures. Moreover, these two inverters require additional capacitor voltage balance, which further increases the complexity of the system and the manufacturing cost [9], [10]. The CHB inverter utilizes numerous isolated sources to output multiple levels, which limits its application in actual engineering [11]. In addition, traditional multilevel inverters are mostly step-down inverters. When the input voltage does not meet the output conditions, the step-up link is necessary. The bulky iron core and multiple coils of the transformer cause the system to become complicated and increase the inverter volume [12], [13].

To simplify the structure, reduce power devices and isolation sources, and increase the output gain of the inverter, researchers have proposed many different topologies [14], [15], [16], [17]. The capacitor strings of the topology proposed in [14] and [15] are charged in parallel with the power supply. The voltage divider capacitor reduces the TSV of the inverter. The capacitor of the topology proposed in [16] is charged by the power pack, and the output gain is improved. The topology in [17] uses inverter cascade to increase the number of output levels.

It is a suitable idea to use the capacitor as a virtual power supply instead of the isolation source in the inverter. In switched capacitors (SCs), the capacitor is charged in parallel with the power supply. The high voltage gain is obtained by superposing the capacitor and the power supply in series, which avoids the use of bulky inductance components. Therefore, many SC boost converters and SC multilevel inverters have been proposed [18], [19], [20], [21].

In [22], [23], [24], a series of multilevel inverters based on SC structure have been proposed. Through a suitable switching control strategy, the capacitor is charged in parallel with the power supply. The stored charge is released in the discharge circuit to transfer the electrical energy. In the charging circuit of the inverter, the capacitor is periodically charged to the rated voltage, which ensures the self-balance of the capacitor voltage. However, these structures are solidified and cannot be expanded, which limits the number of output levels.

Extended topologies have been proposed in [25] and [26], which use dual power inputs and have symmetrical and asymmetrical operating modes. The output voltage of the inverter is the superposition of the dual power supply voltage and the capacitor voltage, which increases the output voltage level and the number of output levels. However, at least two

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isolated power supplies are required in the above two topologies, which would reduce the scope of the inverter applications. In addition, when the inverter is working in the asymmetrical mode, the voltage ratio of the isolated power supply needs to be set according to the structure of the inverter. Compared with single-input inverters, the application scenarios of multi-input inverters have many limitations.

The extended multilevel topologies in [27], [28], [29] utilize a single power supply. Although these topologies are simple and have a considerable number of output levels, an H-bridge is used at the end of these topologies to complete the polarity conversion of the output levels. The switches of the H-bridge should withstand the accumulated voltage of the previous circuit, which limits the application scopes, especially in high-voltage and high-power applications. For the topology proposed in [30], the charging and discharging states of the symmetrical sub-circuits are complementary, which helps to reduce the voltage ripple and total harmonic distortion of the inverter output voltage. However, many semiconductors and H-bridge are required.

Two circuits of full-cell and half-cell were proposed in [32]. This circuit configuration realizes the superposition charging of multi-stage capacitors, and the number of output voltage levels is improved. A similar circuit configuration was introduced in [33]. This topology avoids the use of H-bridge and reduces the voltage stress of semiconductors.

In order to further reduce the voltage stress of the device and increase output gain, in this paper, a novel X-type switched capacitor multilevel inverter utilizing a single power supply is proposed. The proposed topology can be used in photovoltaic power generation systems, electric vehicles, flexible power distribution and other fields. It has the following salient features:

- The proposed topology avoids the requirement of the terminal H bridge, ensuring that the maximum voltage stress of each switch does not exceed $4V_{dc}$.
- The maximum switching frequency of the proposed topology is 3 times of the fundamental frequency under the selective harmonic elimination pulse width modulation strategy.
- The upper and lower bridge arm capacitors are charged synchronously, which simplifies the modulation strategy for the multi-level extension of the topology.
- The capacitor voltage of the proposed topology has the ability of self-balancing, and the single-input characteristic facilitates its industrial applications.

In Section II, the general structure of the proposed topology is introduced, and the 7-L inverter is used as a tutorial to explain its operation principle and modulation strategy. In Section III, the principle of determining the capacitance value is given and the loss analyses of the 7-level inverter are carried out. Next, In Section IV, a comparative study of the proposed topology and well-known topologies is given. In Section V, the performance of the proposed 7-level inverter is extensively verified by simulations and experiments. Finally, the conclusion is given in Section VI.

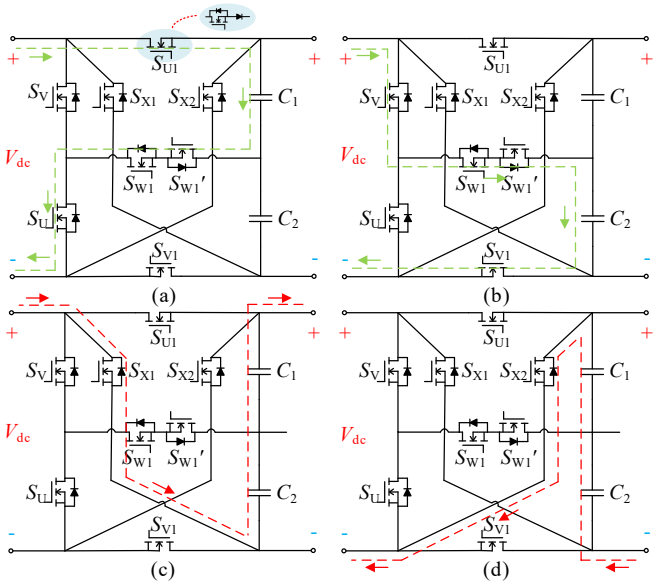

Fig. 1. X-type Bipolar Circuit. (a) Capacitor C_1 charging path, (b) Capacitor C_2 Charging path, (c) Positive discharge path, (d) Negative discharge path.

II. Circuit Description

A. X-type Bipolar Circuit

X-type bipolar switched capacitor circuit is shown in Fig. 1. The operating principle of the unidirectional switches S_{U1}, S_{V1} is equivalent to a bidirectional switch in series with a diode in hardware. Fig. 1(a) and 1(b) are the charging paths of capacitor C_1 and capacitor C_2, respectively. Capacitors C_1 and C_2 are charged in parallel with the power supply. Fig. 1(c) and 1(d) are the positive discharge path and the negative discharge path of the capacitor, respectively. It can be seen that the X-type circuit can output a bipolar level. Because of the bipolar voltage output characteristics of the module, the inverter avoids the use of the H-bridge. Therefore, the peak invert voltage (PIV) of the switches is reduced.

B. Proposed General switched capacitor multilevel inverter

Fig. 2 shows the proposed general switched capacitor multilevel inverter (SCMLI), which is composed of left half bridge (LHB) module, X-type module and right half bridge (RHB) module. The switches of the group U, V, and W are used to complete the charging operation of the upper and lower bridge arm capacitors. The upper bridge arm capacitors are simultaneously charged under the switching action of group U. the lower bridge arm capacitors are simultaneously charged under the switching action of group V. The working mode of synchronous charging effectively simplifies the modulation strategy of the multi-stage extended topology.

Assuming that the number of the extended X-type module is i, the number of switches (N_{Switch}), capacitors ($N_{Capacitor}$), the number of output levels (N_{Level}) and the output voltage gain G can be obtained by

$$N_{Switch} = 6i + 8, \tag{1}$$

$$N_{Capacitor} = 2i, \tag{2}$$

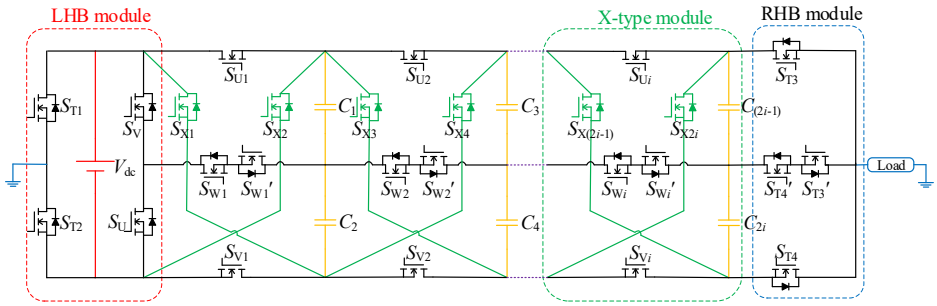

Fig. 2. Generalized topology of the proposed switched capacitor multilevel inverter.

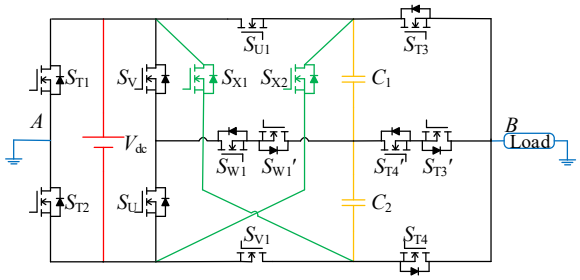

Fig. 3. Topology of the proposed 7-level inverter.

$$N_{Level} = 4i + 3\,, \tag{3}$$

$$G = \frac{V_{out}}{V_{dc}} = 2i + 1\,. \tag{4}$$

C. Seven-Level Inverter

Fig. 3 shows the circuit configuration of the proposed 7-level inverter (i =1), which consists of 14 switches, 2 capacitors and a DC voltage source (can be fuel cell, PV or battery). When the switches S_{U1}, S_U and S_{W1}' are turned on, capacitor C_1 is charged to V_{dc} in parallel with the voltage source. When the switches S_{V1}, S_V and S_{W1} are turned on, capacitor C_2 is charged to V_{dc} in parallel with the voltage source. Different from the inverters that adopt H-bridge output bipolar level, the X-type module of the proposed inverter has the inherent polarity reversal ability. Therefore, the proposed inverter effectively reduces the PIV of the switches, which is beneficial to the extension of the inverter.

D. States of Seven-Level Inverter

Fig. 4 shows the operating principle of the proposed inverter, which is explained through seven operating modes with different output voltage levels. Table I shows the working status of switches and capacitors in these modes. In Fig. 4, the red dotted line represents the discharge circuit of the inverter. The purple dotted line represents the reverse current circuit of the inverter, which proves that the inverter has the ability to carry an inductive load. The charging circuit of the capacitors is represented by a green dotted line. In order to clearly explain the operating principle of the inverter, it is assumed that all the components of the inverter are ideal, and there is no internal resistance and positive voltage drop in the inverter. The capacitance of the circuit is large enough, and the inverter works in a stable state.

State A (0 level): As shown in Fig. 4(a), when the switches S_V, S_{V1}, S_{W1}, S_{T2}, and S_{T4} in the current circuit are turned on, the capacitor C_2 is charged to V_{dc} by the voltage source, and the capacitor C_1 remains unchanged. The output bus voltage V_{bus} is

$$V_{bus} = V_B - V_A = 0\,. \tag{5}$$

State B ($+V_{dc}$): As shown in Fig. 4(b), when the switches S_U, S_{U1}, S_{W1}', S_{T2} and S_{T3} in the current circuit are turned on, the capacitor C_1 is charged to V_{dc} by the voltage source, and the capacitor C_2 remains unchanged. The output bus voltage V_{bus} is

$$V_{bus} = V_B - V_A = V_{dc}\,. \tag{6}$$

State C ($+2V_{dc}$): As shown in Fig. 4(c), when the switches S_{X1}, S_{T2} and S_{T4}' in the current circuit are turned on, the capacitor C_2 and the voltage source are connected in series to output voltage. The output bus voltage V_{bus} is

$$V_{bus} = V_B - V_A = V_{dc} + V_{C2} = 2V_{dc}\,. \tag{7}$$

State D ($+3V_{dc}$): As shown in Fig. 4(d), when the switches S_{X1}, S_{T2}, and S_{T3} in the current circuit are turned on, the capacitors C_1 and C_2 participate in the output of the inverter. At this time, the inverter output bus voltage V_{bus} is

$$V_{bus} = V_B - V_A = V_{dc} + V_{C1} + V_{C2} = 3V_{dc}\,. \tag{8}$$

State E ($-V_{dc}$): As shown in Fig. 4(e), when the switches S_V, S_{V1}, S_{W1}, S_{T1} and S_{T4} in the current circuit are turned on, the capacitor C_2 is charged to V_{dc} by the voltage source, and the capacitor C_1 remains unchanged. The output bus voltage V_{bus} in the state shown in Fig. 4(e) is

$$V_{bus} = V_B - V_A = -V_{dc}\,. \tag{9}$$

State F ($-2V_{dc}$): As shown in Fig. 4(f), when the switches S_{X2}, S_{T1}, S_{T3}', and S_{T4}' in the current circuit are turned on, the capacitor C_1 and voltage source are connected in series to output voltage, and the capacitor C_2 remains unchanged. The output bus voltage V_{bus} is

$$V_{bus} = V_B - V_A = -V_{C1} - V_{dc} = -2V_{dc}\,. \tag{10}$$

State G ($-3V_{dc}$): As shown in Fig. 4(g), when the switches S_{X2}, S_{T1} and S_{T4} in the current circuit are turned on, the capacitors C_1

TABLE I
SWITCHING STATES AND CAPACITANCE STATES OF THE PROPOSED INVERTER

States	On-State Switches	Output Voltage V_{bus}	Capacitor states C_1	Capacitor states C_2
A	S_V, S_{V1}, S_{W1}, S_{T2}, S_{T3}', S_{T4}	0	–	▲
B	S_U, S_{U1}, S_{W1}', S_{T2}, S_{T3}, S_{T4}'	$+V_{dc}$	▲	–
C	S_U, S_{U1}, S_{X1}, S_{W1}, S_{T2}, S_{T3}', S_{T4}'	$+2V_{dc}$	–	▼
D	S_U, S_{U1}, S_{X1}, S_{W1}, S_{T2}, S_{T3}, S_{T4}'	$+3V_{dc}$	▼	▼
E	S_V, S_{V1}, S_{W1}, S_{T1}, S_{T3}', S_{T4}	$-V_{dc}$	–	▲
F	S_V, S_{V1}, S_{X2}, S_{W1}', S_{T1}, S_{T3}', S_{T4}'	$-2V_{dc}$	▼	–
G	S_V, S_{V1}, S_{X2}, S_{W1}', S_{T1}, S_{T3}', S_{T4}	$-3V_{dc}$	▼	▼

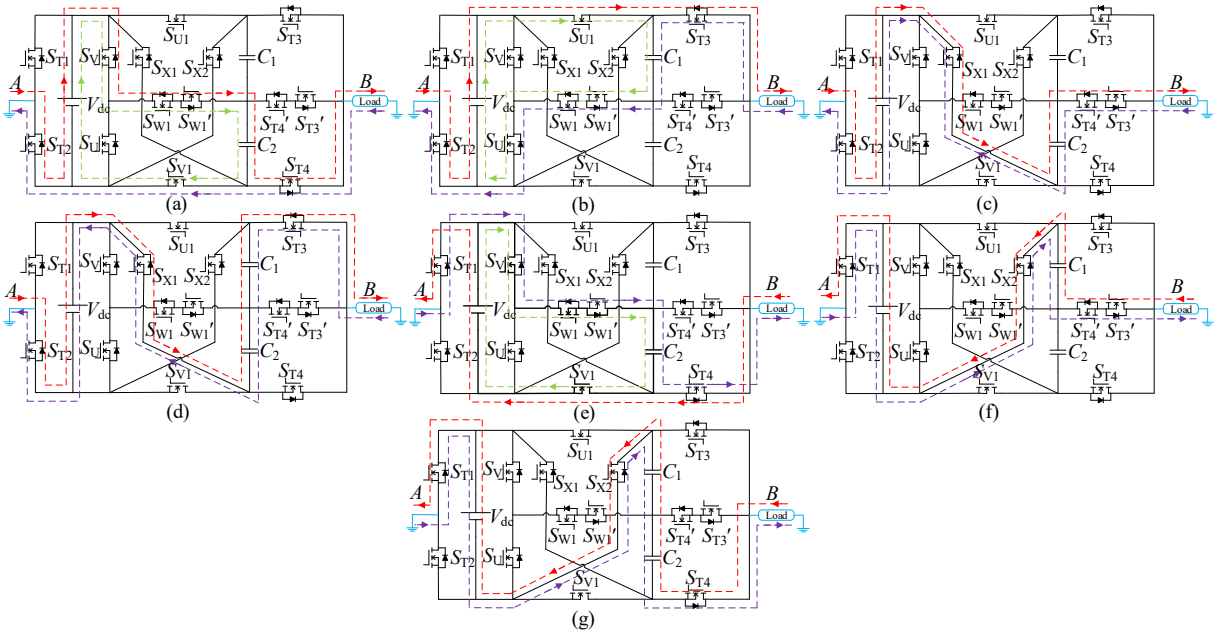

Fig. 4. Current flows in the proposed 7-level inverter. (a) State A, (b) State B, (c) State C, (d) State D, (e) State E, (f) State F, (g) State G.

and C_2 participate in the output of the inverter. At this time, the inverter output bus voltage V_{bus} is

$$V_{bus} = V_B - V_A = -V_{C1} - V_{C2} - V_{dc} = -3V_{dc}. \quad (11)$$

For a multilevel inverter, the output voltage is the superposition of the power supply voltage and the capacitor voltage. The continuous discharge of the capacitor will cause the deterioration of the output voltage quality. Therefore, it is necessary to ensure that each capacitor is charged to the rated voltage after discharge. According to the operating principle of the 7-level inverter, the capacitors are charged in parallel with the power supply after the discharge cycle ends. The periodic charging and discharging process ensures that there is no continuous voltage deviation, and realizes the self-balance of the capacitor voltage.

E. Modulation strategy of seven-level inverter

For a multilevel inverter, there are many modulation strategies can be referred. Commonly used modulation strategies include sinusoidal pulse width modulation (SPWM), space vector pulse width modulation (SVPWM) and selective harmonic elimination pulse width modulation (SHEPWM), etc. The SPWM strategy is simple and easy to implement, but the switching frequency is high. SVPWM is suitable for low-level output scenarios (usually 3-5 levels), and it would make the modulation too complicated in inverters with higher than 5 levels. Compared with the above two modulation strategies, SHEPWM has the advantages of low switching frequency, high voltage utilization, low harmonic distortion rate and low losses. Therefore, SHEPWM is referred for the proposed 7-level inverter.

The modulation principle diagram of 7-level inverter is shown in Fig. 5. The main principle of SHEPWM is to select a suitable conduction angle, and make the Fourier expansion of the eliminated harmonics equal to 0. For the z-level staircase waveform, the Fourier expansion is

$$v(\omega t) = \frac{4V_{dc}}{m\pi} \sum_{m=1,3,5...}^{\infty} \left[\cos(m\theta_1) + \cos(m\theta_2) + \cdots + \cos(m\theta_z)\right] \times \sin(m\omega t), \quad (12)$$

where 1, 2 ... z are the conduction angles of each step level.

When all conduction angles are 0, the maximum fundamental wave amplitude V_{1p} is

$$\begin{cases} v_1(\omega t) = \dfrac{4V_{dc}}{\pi} \times \left[\cos(\theta_1) + \cos(\theta_2) + \cdots + \cos(\theta_z)\right] \times \sin(\omega t) \\ V_{1p} = \dfrac{4z}{\pi} V_{dc} \end{cases}. \quad (13)$$

If m is the number of harmonics to be eliminated, the conduction angle of each level can be obtained by the equation

$$\cos(m\theta_1) + \cos(m\theta_2) + \cdots + \cos(m\theta_z) = 0. \quad (14)$$

Here, the ratio of the desired output voltage V_1 to the fundamental wave amplitude V_{1p} is defined as the modulation index M_a. To eliminate the 5th and 7th harmonics in the proposed 7-level inverter, the conduction angle can be obtained by the following equations

$$\begin{cases} \cos\theta_1 + \cos\theta_2 + \cos\theta_3 = 3M_a \\ \cos 5\theta_1 + \cos 5\theta_2 + \cos 5\theta_3 = 0 \\ \cos 7\theta_1 + \cos 7\theta_2 + \cos 7\theta_3 = 0 \end{cases}. \quad (15)$$

The conduction angle should satisfy the following equation

$$0 < \theta_1 < \theta_2 < \theta_3 < \frac{\pi}{2}. \quad (16)$$

According to (15), for a given modulation index $M_a = 0.8$, we can obtain that θ_1=11.5°, θ_1=28.7°, θ_3=57.1°. For the SHEPWM method shown in Fig.5, six constant signals $\pm e_1$, $\pm e_2$

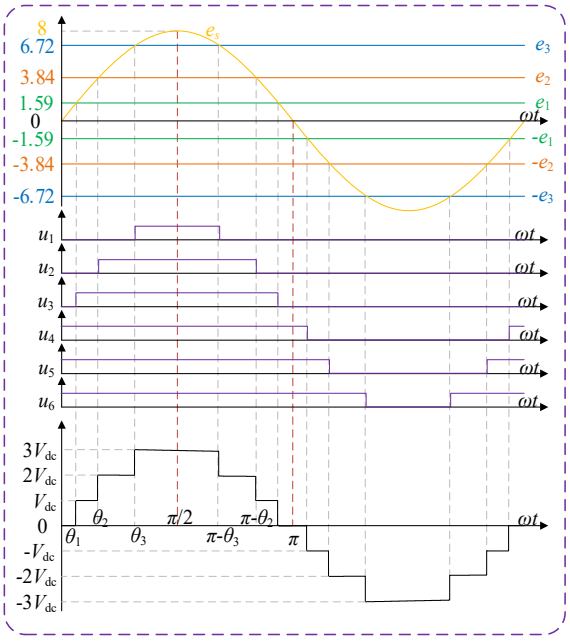

Fig. 5. Modulation principle diagram of 7-level inverter.

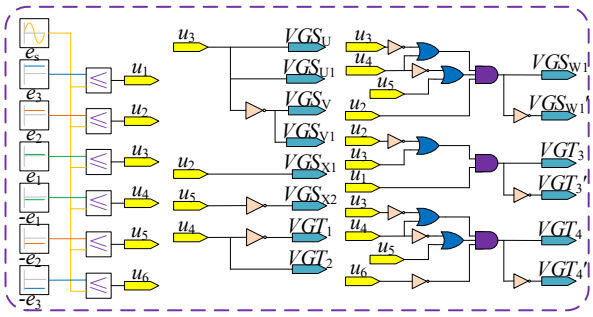

Fig. 6. Modulation logic of 7-level inverter.

and $\pm e_3$ are used to compare with the modulation wave e_s respectively. The amplitude of constant signal $\pm e_i$ is determined by the modulation wave amplitude and the conduction angle. The amplitude of $\pm e_i$ can be obtained by the equation

$$\pm e_i = \pm A \sin\theta_i, \tag{17}$$

where A is the amplitude of the modulation wave, i=1, 2, 3.

When the modulated wave is larger than the constant signal, the output is high level; otherwise, the output is low level. Thus, six groups of basic PWM signals u_1~u_6 are obtained, and the driving signal of each switch is obtained through logical combination. The logic is shown in Fig. 6.

III. Capacitance Determination and Losses Calculation

A. Determination of Capacitance

When the capacitor is discharged in series with the voltage source, the charge stored in the capacitor is released, which causes ripples in the voltage of the capacitor. A large ripple voltage may cause deteriorations of the inverter efficiency and THD, which seriously affect the quality of the output voltage waveform. The magnitude of the ripple voltage is related to the capacitor for the proposed inverter. Generally, the limit value

TABLE II
Operating Parameters of Each Switch

Parameters	S_U S_V	S_{U1} S_{V1}	S_{W1} S_{W1}'	S_{X1} S_{X2}	S_{T1} S_{T2}	S_{T3} S_{T4}	S_{T3}' S_{T4}'
f_S	f_o	f_o	$3f_o$	f_o	f_o	$3f_o$	$3f_o$
V_S	V_{dc}	$2V_{dc}$	V_{dc}	$2V_{dc}$	V_{dc}	$2V_{dc}$	$0.5V_{dc}$

TABLE III
Operating Parameters of the Inverter

Parameters (i)	$V_{C,i}$ (V_{dc})	$V_{D,i}$ (V_{dc})	ωt (θ_i)	$r_{eq,i}$
4	2	0	$\pi/2$	$3r_S+2r_{ESR}$
3	1	1	θ_3	$3r_S+ r_{ESR}$
2	0	0	θ_2	$3r_S$
1	-1	1	θ_1	$4r_S+ r_{ESR}$

of the ripple voltage should not exceed 10% of the rated capacitor voltage. The working state of the capacitor in one cycle of the 7-level inverter is shown in Table I. It can be seen that the capacitor C_1 and the capacitor C_2 have the same discharge time. therefore, they have the same parameter design principle.

Capacitor C_2 is taken as an example. The maximum discharge interval of capacitor C_2 is $[\theta_2, \pi-\theta_2]$. During $[\theta_2, \theta_3]$ and $[\pi-\theta_3, \pi-\theta_2]$, the output level of the inverter is $2V_{dc}$. During $[\theta_3, \pi-\theta_3]$, the inverter output level is $3V_{dc}$. The inverter load impedance is Z_L. Then the maximum discharge charge Q_{C2} of capacitor C_2 can be obtained by the following equation

$$\Delta Q_{C2} = \frac{1}{2\pi f_o}\left[\int_{\theta_2}^{\theta_3}\frac{2V_{dc}}{Z_L}d\omega t + \int_{\theta_3}^{\pi-\theta_3}\frac{3V_{dc}}{Z_L}d\omega t + \int_{\pi-\theta_3}^{\pi-\theta_2}\frac{2V_{dc}}{Z_L}d\omega t\right], \tag{18}$$

where ω is the angular frequency corresponding to the inverter, and f_o is the inverter output frequency. The above equation can be further calculated

$$\Delta Q_{C2} = \frac{V_{dc}}{2\pi f_o Z_L}\left[3\pi - 4\theta_2 - 2\theta_3\right]. \tag{19}$$

When the capacitance value C is given, the ripple voltage of the capacitor C_2 can be calculated as

$$\Delta V_{C2} = \frac{V_{dc}}{2\pi f_o Z_L C}\left[3\pi - 4\theta_2 - 2\theta_3\right]. \tag{20}$$

When the ripple voltage limit value U_{rip} is given ($U_{rip}\leq 0.1V_C$, V_C is the rated voltage of the capacitor), the minimum value of the capacitors C_1 and C_2 can be obtained as

$$C_{1,\min} = C_{2,\min} = \frac{V_{dc}}{2\pi f_o Z_L U_{rip}}\left[3\pi - 4\theta_2 - 2\theta_3\right]. \tag{21}$$

B. Calculation of Losses

(i) Ripple loss: Ripple loss is caused by the ripple voltage of the capacitor. For the proposed inverter, the amount of charge V_{C2}' released by the capacitor C_2 in another small discharge period is consistent with the amount of charge V_{C1}' released by the capacitor C_1 in the interval $[\theta_3, \pi-\theta_3]$, there is

$$\Delta V_{C2}' = \Delta V_{C1}' = \frac{\Delta Q_{C1}}{C} = \frac{V_{dc}}{\pi f_o Z_L C}\left[\pi - 2\theta_3\right]. \tag{22}$$

The ripple loss of capacitor C_2 can be obtained by

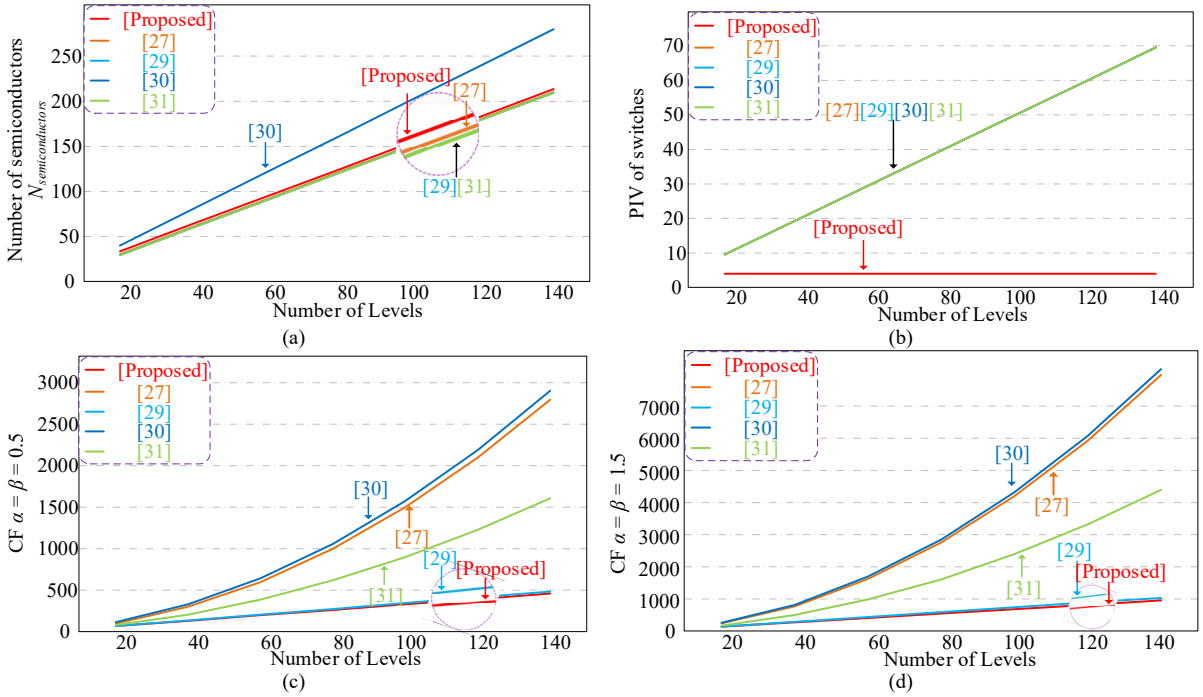

Fig. 8. Comparison of the proposed topology with other well-known topologies.

$$P_{rip2} = f_o C\left(\Delta V_{C2}{}^2 + \Delta V_{C2}{}'^2\right). \quad (23)$$

Capacitor C_1 has the same working state as capacitor C_2, so the ripple loss P_{rip1} of capacitor C_1 is consistent with the ripple loss P_{rip2} of capacitor C_2. The total ripple loss P_{rip} of the proposed inverter is

$$P_{rip} = P_{rip1} + P_{rip2} = 2P_{rip2}. \quad (24)$$

(ii) Switching loss: Switching loss is caused by the superposition of voltage and current when the switch changes its state. When the output capacitance is C_{OSS}, the maximum reverse voltage to withstand is V_S, and the loss of the switch in one switching cycle can be estimated as

$$P_E = C_{OSS} V_S{}^2. \quad (25)$$

Table II shows the operating frequency f_S and the maximum reverse voltage V_S of each switch. When the 7-level inverter works under SHEPWM strategy, it can be seen that the maximum operating frequency of the switch is 3 times the output frequency, and the PIV of the switch is $2V_{dc}$. Therefore, the proposed 7-level inverter is suitable for high-voltage and high-frequency environments. In the proposed inverter, the switching loss can be calculated as

$$P_{sw} = f_S C_{OSS} V_S{}^2 = \frac{103 f_o C_{OSS} V_{dc}{}^2}{2}. \quad (26)$$

(iii) Conduction loss: The conduction loss is caused by the parasitic impedance of semiconductor devices. In the discharge circuit of the inverter, the main parasitic impedances include the conduction resistance r_D and the voltage drop V_D of the anti-parallel diode, the conduction resistance r_S of the switch and the equivalent series resistance r_{ESR} of the capacitor.

According to the operating principle in section II, in the positive half cycle and the negative half cycle, the proposed inverter has the same working state, and thus has the same loss. The various impedances of the working circuit during the positive quarter cycle are shown in Table III.

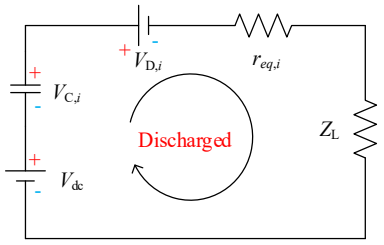

Fig. 7. Discharge equivalent circuit diagram of the inverter.

Fig. 7 shows the equivalent diagram of the inverter discharge circuit. Where V_{dc}, $V_{C,i}$ and $V_{D,i}$ are the output voltage, the discharge capacitor voltage and anti-parallel diode voltage drop, respectively. Z_L is the load impedance. For the SHEPWM, the average conduction loss of the inverter can be obtained as

$$P_{con} = f_o \frac{2}{\pi} \sum_{i=1}^{4} \left[(\theta_i - \theta_{i-1}) \left(\frac{V_{dc} + V_{C,i} - V_{D,i}}{r_{eq,i} + Z_L} \right)^2 \times r_{eq,i} \right], \quad (27)$$

where $\theta_0 = 0$. Finally, the total loss P_{Looses} can be obtained as

$$P_{Looses} = P_{rip} + P_{sw} + P_{con}. \quad (28)$$

The above losses are different under different parameters. When the input voltage is 30V and the load is 100 Ω. It is worth noting that r_S, r_{ESR}, r_D, C_{OOS}, C and f_o are 0.19 Ω, 0.06 Ω, 0.8 V, 780 pF, 2200 μF and 50 Hz, respectively. According to the above loss analysis, the total loss P_{Losses} is 2.01 W and the efficiency is 95.27%. Under the same experimental parameters, the actual loss measured is 2.24 W and the efficiency is 94.7%. Affected by the measurement accuracy, it can be known that the actual loss is slightly higher than the theoretical loss.

IV. Comparative Study of the Proposed Topology and Other Well-Known Topologies

In order to demonstrate the performance of the proposed multilevel inverter, the proposed topology and the well-known topologies in [27], [29], [30], [31] are compared.

The number of semiconductors $N_{semiconductors}$ (including N_{switch} and N_{diode}) at different levels of output is shown in Fig. 8(a). The proposed topology uses less semiconductors than the topology in [30], and this advantage increases with the extension of output voltage level. The proposed topology uses 3 more semiconductor devices than the topology in [27] and 4 more semiconductor devices than the topologies in [29] and [31]. Nevertheless, the gap will not increase with the extension of the inverter.

As shown in Fig. 8(b), the PIVs of existing topologies increase with the number of levels. Because of the inherent level polarity conversion capability of the X-type bipolar module, the PIV of the proposed topology is $4V_{dc}$ and much less than those of existing topologies. Because of the low voltage stress, the proposed topology can be used in medium-high voltage applications.

In actual engineering, the choice of topology should make a compromise between several factors. In order to better explain this situation, a cost function (CF) is introduced

$$\mathrm{CF} = N_{semiconductors} + \alpha \mathrm{PIV} + \beta \mathrm{TSV}, \qquad (29)$$

where α and β are the specific gravity coefficients to present the significance of PIV and TSV, respectively. If the significance of PIV and TSV is greater than the number of semiconductors, then both α and β should be greater than 1. If the significance of PIV and TSV is less than the number of semiconductors, then α and β should be less than 1. Fig. 8(c) and Fig. 8(d) are comparisons of different topologies when the specific gravity coefficient is 0.5 and 1.5, respectively. It can be seen that the proposed topology has optimal selectivity in both cases, which shows the excellent performance of the proposed topology.

V. Simulation and Experimental Results

A. Simulation results of seven-level inverter

In order to verify the feasibility of the proposed multilevel inverter, a 7-level inverter model was built in the MATLAB/Simulink environment. Simulation parameters are shown in Table IV.

Fig. 9 shows the output voltage and load current of the 7-level inverter. When the input voltage is 30 V and the load is set to 50 Ω and 90 mH, the inverter output voltage is a 7-step square wave. It can be seen that the peak output voltage is 90 V and the output gain is 3. The load current is sinusoidal and lags behind the voltage, which verifies the inverter's ability to carry an inductive load.

The synthesis principle of the output voltage is shown in Fig. 10. Terminal A outputs a peak voltage of 90 V and a valley voltage of -60 V. The output peak voltage of terminal B is 30V, and the valley voltage is 0 V. Under the SHEPWM strategy, the inverter output voltage is the superposition of the A terminal and the B terminal, which is consistent with the theoretical analysis of the inverter output voltage.

TABLE IV

Simulation Parameters

Items	Specification
Input voltage V_{dc}	30 V
Capacitor C_1, C_2	2200 μF
Load resistor R	50 Ω
Load inductor L	90 mH
Out frequency f_o	50 Hz
Conduction angle	11.5°, 28.7° and 57.1°

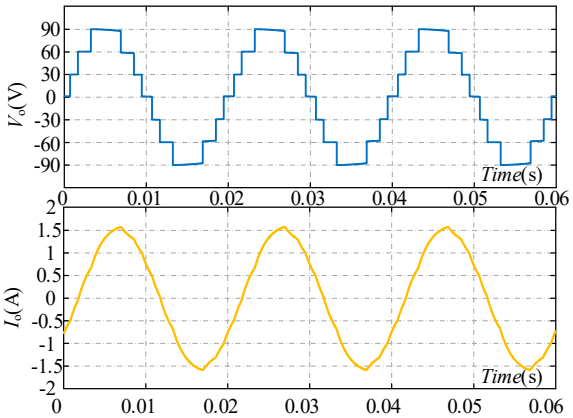

Fig. 9. Simulation waveforms of output voltage and load current.

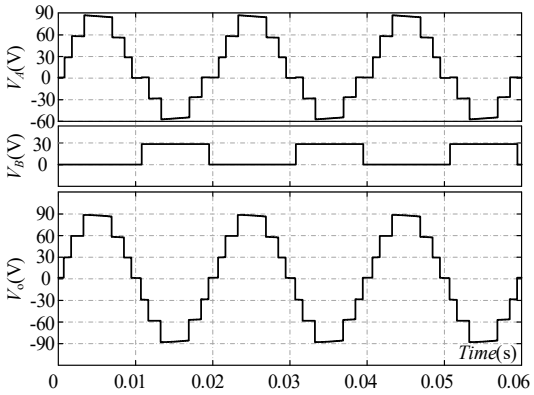

Fig. 10. Simulation waveforms of the voltage output from the inverter half-bridge.

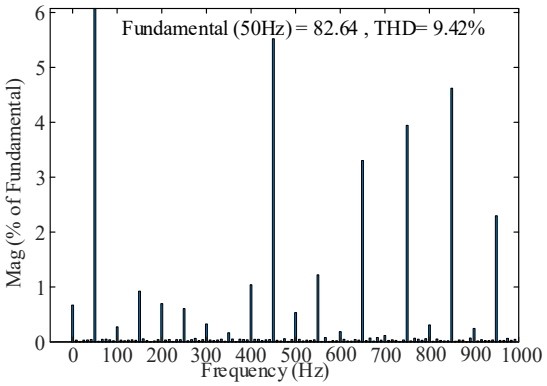

Fig. 11. Fourier analysis of output voltage.

Fig. 11 shows the Fourier analysis of the output voltage. Under the designed conduction angle, the 5th and 7th harmonics of the output voltage are obviously eliminated. The characteristics of SHEPWM to eliminate specific harmonics are verified, and the harmonic distortion rate is reduced.

B. Experimental Results of seven-level inverter

In order to further verify the feasibility of the proposed topology, extensive experimental analysis was carried out on the 7-level inverter laboratory prototype. The selection of experimental parameters takes into account the existing equipment in the laboratory, the detailed parameters are given in Table V and the experimental prototype is shown in Fig. 12. In the steady-state experiment, the output voltage, load current and capacitor ripple voltage of the 7-level inverter are studied. In this experiment, the input voltage is fixed at 30 V and the output frequency is set at 50 Hz.

TABLE V
EXPERIMENTAL PARAMETERS

Items	Specification
Input voltage V_{dc}	20 V or 30 V
Capacitor C_1, C_2	2200 μF
Load resistor R	70 Ω or 120 Ω
Load inductor L	30 mH
Out frequency f_o	25 Hz, 50 Hz or 100 Hz
Conduction angle	11.5°, 28.7° and 57.1°
Power switches	SPP20N60C3
Optocoupler drivers	TLP250

Fig. 13 (a) and (b) respectively show the input voltage and load current waveforms of the inverter under pure resistive and inductive loads. It can be seen that the peak value of the inverter output voltage is close to 90 V, and the inverter achieves a voltage gain of 3 times. When the pure resistive load Z_L=70 Ω, the load current waveform is a stepped waveform, and when the inductive load Z_L=70Ω+30mH, the load current shows sinusoidal and the current lags the voltage by a certain angle. The voltage waveforms of the capacitor are described in Fig. 14. It can be seen that the ripple voltage of each capacitor is within the design range, and the capacitor voltage is self-balanced.

Fig. 15 shows the output voltage and load current waveforms at different loads. It can be seen that when the load changes, the output voltage of the inverter remains unchanged, and the load current can follow the change of the load category to make corresponding changes. These results show that the inverter can work stably under different working conditions and has strong applicability.

When the input voltage changes, the output voltage and load current waveforms are shown in Fig. 16. It can be seen that the inverter output level number and boost gain remain unchanged during the input voltage change, and the load current changes accordingly with the change of the output voltage amplitude. The change process is stable and reliable.

Fig. 17 shows the output voltage and load current waveforms when the output frequency changes. The experimental results show that the inverter can adapt to complex frequency conditions. In addition, the highest switching frequency of the proposed inverter is 3 times the fundamental frequency, so the proposed topology can be applied in higher frequency projects.

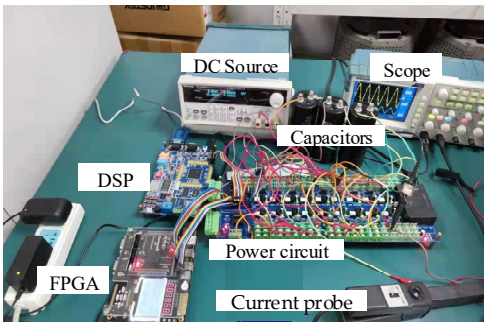

Fig. 12. Experimental platform.

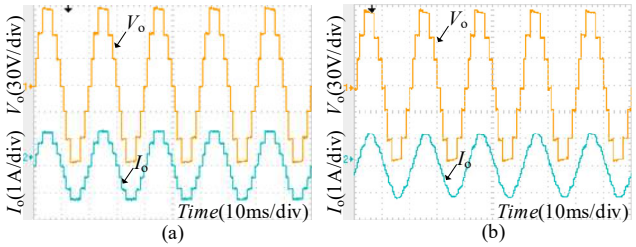

Fig. 13. Experimental waveforms. (a) pure resistive load, (b) inductive load.

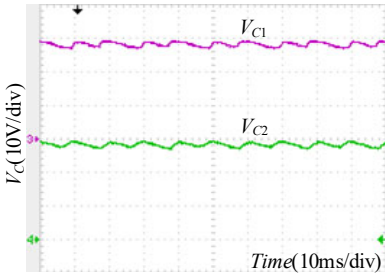

Fig. 14. Experimental waveforms of capacitor voltage.

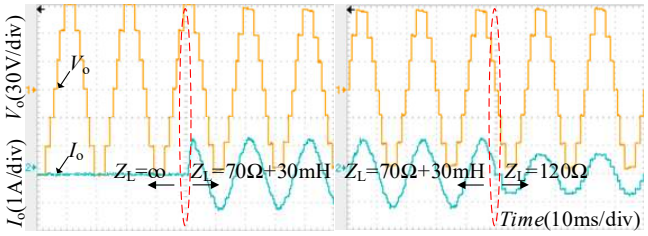

Fig. 15. Experimental waveforms of voltage and current under different loads.

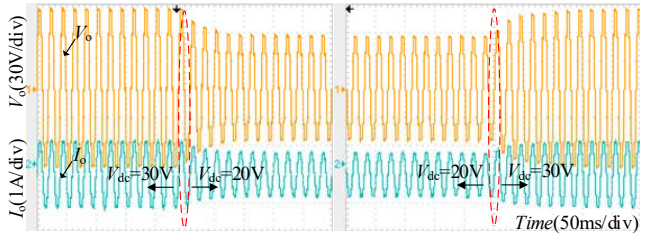

Fig. 16. Experimental waveforms of voltage and current under input voltage changes.

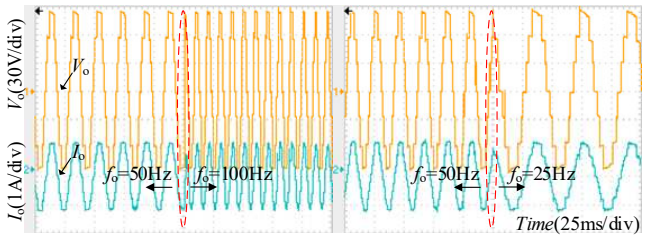

Fig. 17. Experimental waveforms of voltage and current under frequency changes.

V. Conclusions

In order to reduce the peak inverse voltage of the switches and increase the output voltage gain of the inverter, an X-type switched capacitor multilevel inverter utilizing a single power supply is proposed. The X-type circuit of the proposed topology reduces the voltage stress of the semiconductor and the proposed topology has a low switching frequency under the SHEPWM strategy. The output level number and voltage gain of the proposed topology can be further improved by the extension of the X-type module. The characteristic of the synchronous charging of the capacitor simplifies the modulation of the multi-level extension structure.

The comparative study between the proposed topology and other well-known topologies shows that the proposed topology has advantages in reducing voltage stress and manufacturing cost. Finally, the feasibility of the proposed multilevel inverter is verified through the simulation and experimental results.

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