Applied Physics Letters

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Citation: Appl. Phys. Lett. **95**, 232502 (2009); doi: 10.1063/1.3271683
View online: http://dx.doi.org/10.1063/1.3271683
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v95/i23
Published by the American Institute of Physics.

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Bidirectional magnetic nanowire shift register

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(Received 16 September 2009; accepted 21 October 2009; published online 7 December 2009)

We experimentally demonstrate a shift register based on an open-ended chain of ferromagnetic NOT gates which can support bidirectional data flow. Up to eight data bits are electrically input to the device, stored for extended periods without power, and then output either in a first in first out or last in first out scheme. Comparing to traditional transistor-based logic, this bidirectionality offers a range of devices that are reversible and not limited to only one mode of operation. © *2009 American Institute of Physics*. [doi:10.1063/1.3271683]

In ferromagnetic nanowires, the magnetization is confined to one of two possible directions, resulting in an intrinsically digital system ideal for encoding information. Currently there is considerable research into domain wall (DW) (the region separating two magnetic domains) motion[1–5] and pinning[6,7] within these nanowires and their potential uses for future technologies.[8,9] One type of device receiving great attention is a shift register for data storage applications.[10,11] This typically can operate in one of two ways. Data is either always moved in one direction along the conduit, i.e., the first data in is always the first out (FIFO), or it is stored and subsequently sent back through the register to the original input point; the last data into the device is the first data out (LIFO).

In this letter, we present a demonstration of a bidirectional magnetic nanowire based shift register. We show how an open-ended chain of ferromagnetic NOT gates can operate as either a FIFO or LIFO buffer, storing data for extended periods without power. In contrast to traditional transistor-based logic where source and drain introduces inherent asymmetry, bidirectional magnetic nanowires have the potential to form a range of devices that are logically reversible and not limited to only one mode of operation: a property appealing for complex logic and data storage schemes.

For this work, data are encoded using the direction of magnetization of the nanowire [see Fig. 1(a)]. The minimum field required to reverse the magnetization of a section of nanowire is termed the nucleation field, H_{Nuc}. A DW present in a nanowire can overcome the inherent pinning due to wire roughness and propagate when an applied magnetic field, H_{Global}, exceeds the characteristic propagation field, H_{Prop}. Thus if $H_{\mathrm{Nuc}} > H_{\mathrm{Global}} > H_{\mathrm{Prop}}$, a DW can move without a new domain being nucleated. However, under a globally applied field head to head (HH) and tail to tail (TT) DWs [see Fig. 1(a)] will move in opposite directions. Previously, magnetic NOT gates[11] [Fig. 1(b)] have been used to separate DWs. The gate performs a logical NOT operation by transforming HH DWs into TT DWs and vice versa. This allows an arbitrarily chosen data sequence to be propagated in one direction using only a rotating H_{Global} to operate the gate. A counterclockwise rotating field moves HH (TT) DWs from left to right through the gate in the half cycle $+(-)x$ to $-(+)x$ (see Ref. 11 for a detailed description).

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Figure 1(b) shows a scanning electron microscope (SEM) image of the shift register. The device is constructed from a Permalloy ($Ni_{80}Fe_{20}$) nanowire (110 nm wide, 10 nm thick) with eight magnetic DW NOT gates, patterned using electron beam lithography. For these nanowires $H_{\mathrm{Nuc}} \sim 210$ Oe and $H_{\mathrm{Prop}} \sim 10$ Oe. The NOT gates are operated using an elliptically rotating H_{Global}, of magnitude 60 Oe in x, 110 Oe in y, and frequency f. The gates implemented in this register have an areal footprint of 0.30 μm^2, a 12-fold reduction from previously quoted dimensions.[11]

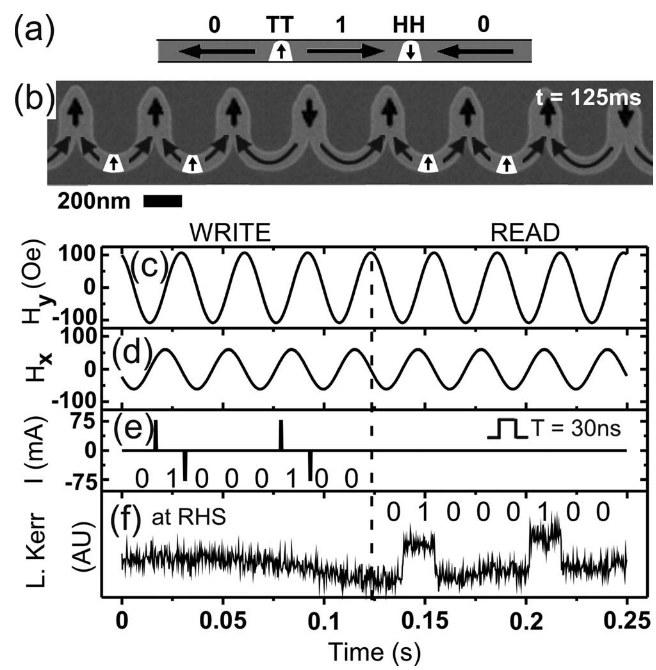

FIG. 1. (a) Schematic of a nanowire with only two possible single domain states. Magnetization direction is represented by arrows and encoded data state is shown as 0 or 1. White region indicates a DW. (b) SEM image of data storage area with schematic of magnetic state at $t = 125$ ms, i.e., after data input (see text). [(c)–(f)] Operating the buffer at 32 Hz for FIFO read. [(c) and (d)] A rotating magnetic field operates the NOT gates passing DWs left to right. The first half of the sequence moves data into the register. The second half reads out data. (e) A sequence of short current pulses (duration $T = 30$ ns) synchronized with H_{Global} creates DWs. H_{Global} then propagates them toward the gates. Sequence shown is applied to a Au stripe patterned over the left hand end of the wire, writing 01000100. (f) 100 averages of MOKE signal at RHS. During the write stage no change in signal is measured. After $t = 125$ ms, readout begins and the wire switches to show the data sequence originally input.

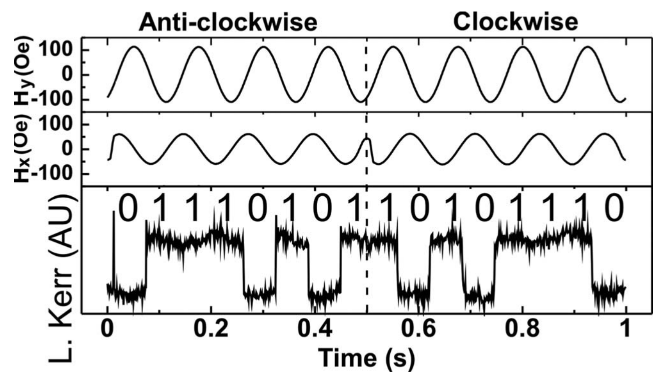

FIG. 2. Rotating the magnetic field four cycles clockwise, then four cycles counter-clockwise demonstrates LIFO use of the register with only one input/output arm. Upper plots: H_{Global}, applied at $f=8$ Hz. Lower plot: 100 averages of the MOKE signal at LHS. Sequence 01110101 (50 μs pulses) is written into the register during $0\ \text{s}<t<0.5\ \text{s}$. Once the field is reversed ($t>0.5$ s) the data sequence is output along the original input arm in reverse order.

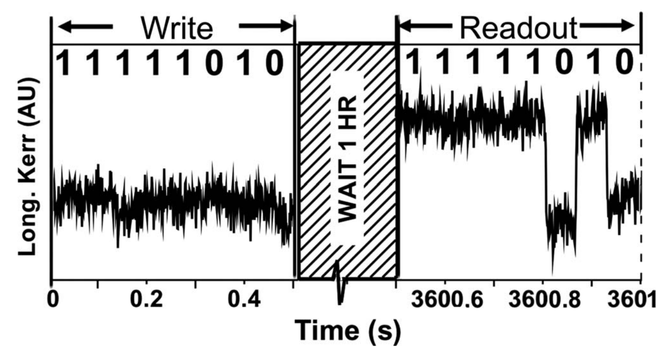

FIG. 3. 100 averages, MOKE signal at RHS for two 0.5 s long acquisitions separated by a delay of 1 h. During the first 0.5 s the sequence 11111010 (50 μs pulses) is written to the register. For $0.5\ \text{s}<t<3600.5\ \text{s}$, H_{Global} is reduced to 0 Oe and the data are held in the register. For $t>3600.5$ s, four further rotations of the operating field read out the sequence 11111010.

Data are input into the left hand side (LHS) of the nanowire by nucleating a new domain using a local Oersted field, H_{Local}. This field is generated by a current-carrying Au stripe (2 μm wide, 150 nm thick) patterned over the LHS end of the nanowire. A current pulse $+(-)I$ [see Fig. 1(e)] such that $|H_{Local}|>|H_{Nuc}|$, synchronized with H_{Global}, locally reverses the end of the nanowire and so creates a HH (TT)DW. The pulse is applied when $|H_{x,Global}|>|H_{Prop}|$, so the DW moves toward the shift register and avoids annihilation at the LHS.

High sensitivity, spatially resolved magneto-optical Kerr effect (MOKE) microscopy is used to probe the magnetization state at any chosen position along the register. The experimental setup is sensitive to magnetic moment changes of only $\sim 10^{-16}$ A/m, but only at low bandwidth. Consequently, the device demonstrated in this paper is limited to a clocking frequency of around 32 Hz. Faraday rotation in the lenses due to stray field from the electromagnet used causes an additional contribution to the Kerr signal. This is in phase and proportional to the y component of H_{Global} and is subtracted from the displayed data.

The data input to the register are measured by placing the MOKE laser spot on the LHS on Fig. 1(b); ouput from the register is measured at either the LHS or RHS depending on device operation. The two possible magnetization directions of the nanowire section [see Fig. 1(a)], used to encode the bits 0 and 1, are measured as low and high states, respectively, in the MOKE signal.

Figures 1(c)–1(f) demonstrates the operation of the register as a FIFO buffer over one input, output cycle. A series of 30 ns current pulses of amplitude ~ 75 mA, synchronized with H_{Global} [$f=32$ Hz, see Figs. 1(c) and 1(d)], create a sequence of HH(TT) DWs; the current pulses are applied when $H_{x,Global}=+(-)20$ Oe and $H_{y,Global}=-(+)100$ Oe. An eight-bit sequence is written into the device from the LHS over four cycles of H_{Global} ($8\times\frac{1}{2}$ field cycles), and a further four cycles are required to move the sequence out of the register at the RHS. The pulse sequence shown in Fig. 1(e) writes the sequence 01000100. The magnetic state of the wire after the data has been written ($t=125$ ms) is shown schematically in Fig. 1(b). Figure 1(f) shows 100 averages of the MOKE signal measured at the RHS. No magnetic switching is seen for the first 125 ms, during which the data are input; the data are read out in the interval $125\ \text{ms}<t<250$ ms.

The converse of the previous operation is the LIFO type buffer. For the register to function in this way, H_{Global} must rotate counterclockwise for read-in, and clockwise for output. This is possible as the left-right symmetry of the NOT gate makes transmission through a gate reversible under field rotation reversal. Figure 2 demonstrates this experimentally. At $t=500$ ms, all data has been written into the register (as in the first half of FIFO sequence) at which point H_{Global} begins to rotate clockwise. This causes the DWs to move from right to left until the data is output on the LHS. The lower trace in Fig. 2 shows the MOKE signal measured at the wire LHS. Over the first 500 ms the sequence 01110101 is input and switching is seen corresponding to input sequence. As the field reverses rotation direction the sequence is read out in reverse order (i.e., LIFO) for $t>500$ ms.

The previous experiments demonstrate storage of data sequences for short periods of time. Data are read out immediately after writing, so storage takes place only over time scales on the order of 10 ms. It is possible to demonstrate longer, non-volatile, storage, by adding a delay to H_{Global} ($f=8$ Hz). For FIFO operation, after the first four field rotations all data are written into the register. H_{Global} is then reduced to 0 Oe for a set wait period and the device is left unpowered. After the wait period a further four field rotations are applied to move the data out of the register. Figure 3 shows the data for a wait period of 1 h. The input sequence 11111010 is fully reproduced over 100 sequence repetitions.

In conclusion, we have experimentally demonstrated that a shift register based on ferromagnetic nanowires and NOT gates can support bidirectional operation. Eight-bit data storage is demonstrated in the device for more than one hour without power. Data is electrically input to the device and can be output either in a FIFO or LIFO scheme. This flexibility is useful for reducing future device size or generating more complex logic schemes.

This work was supported by the Corrigan Scholarship and the European Community under the Sixth Framework Programmes MAGLOG (Contract No. 510993) and SPINSWITCH (Grant No. MRTN-CT-2006-035327).

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