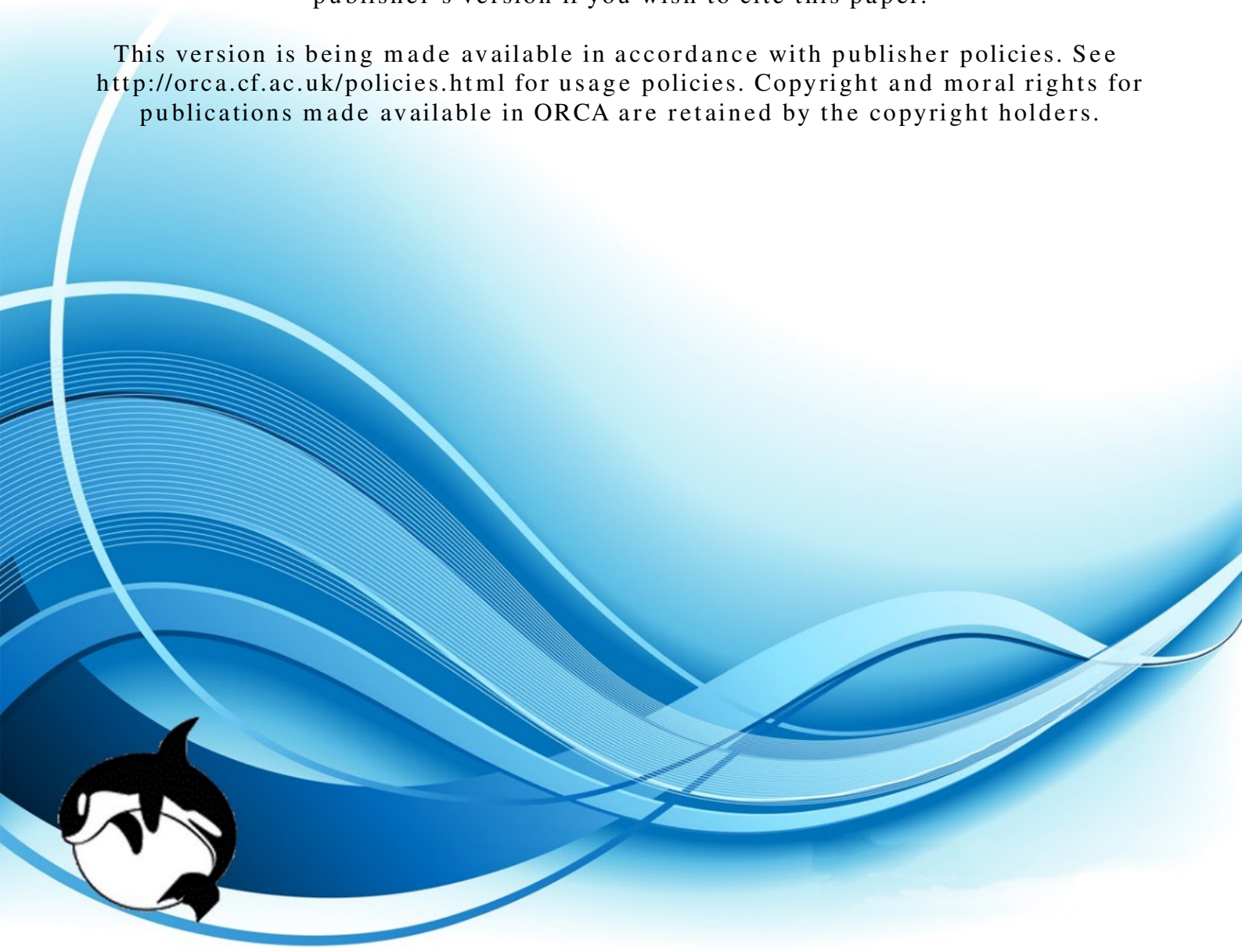

SiC-Based EV Charger for DC Bus Second-Order Ripple Reduction

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***Abstract*- An attractive dc/ac inverter for electric vehicle (EV) chargers is the three-phase four-wire inverter as it is able to handle unbalanced loads, supply neutral current, and provide balanced voltages. However, generation of second-order ripple on the dc bus is inevitable under the presence of unbalanced loads. To mitigate the magnitude of this ripple, conventional four-wire inverters require large and expensive capacitors in the neutral leg. To alleviate these issues, this paper presents a novel three-phase four-wire inverter based on silicon carbide MOSFETs. The topology is configured as a dc/dc buck converter for each phase leg and the neutral leg. Moreover, the capacitance of the neutral leg has been reduced by around eight times compared to that of the conventional neutral leg topology, in turn increasing the power density and reducing overall cost. By adopting a suitably designed control strategy, the proposed topology decreases the second-order ripple on the dc bus and provides neutral current when operating under unbalanced conditions.**

Index Terms—Electric vehicle, neutral leg, second-order ripple, silicon carbide, three-phase four-wire inverter.

NOMENCLATURE

v_{CN}	Neutral capacitor voltage.
V_{dc}	Voltage of the dc terminal.
$V_{2\omega}$	Amplitude of second-order voltage ripple.
p_{ac}	Instantaneous ac side output power.
V_{rms}	Phase-to-ground rms voltage of the ac side.
P_o	Output power of the dc bus.
$P_{2\omega}$	Amplitude of the second-order power ripple.
δ	Imbalance factor at the ac side.
V_{max}	Maximum voltage at the dc bus.
$I_{2\omega}$	Decoupling current.

I. INTRODUCTION

THE dependence on fossil fuels for electricity generation and the need for transport for the development of the economy, technology, and society have increased concerns on the negative environmental impact in the coming years [1]. In response to these issues, the use of electric vehicles (EV) for private transportation has increased in the last decade to replace vehicles based on internal combustion engines [2]. However, EVs still face challenges preventing them from becoming the favored transport option, such as the price of each vehicle, battery autonomy, and fast charging for long journeys [3].

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Although the battery is a component with room for enhancement in an EV, battery chargers are prime candidates to improve in terms of efficiency, cost, and charging time. EV chargers have also attracted attention due to their capabilities to supply electrical energy and create a standalone network by using power electronics converters [4]. This idea is shown in Fig. 1, where the most common converters adopted to form a three-phase system are the three-phase inverters. These can either supply three-phase or single-phase loads for domestic use, where the EV battery is considered as the dc source. This serves as a backup to a traditional grid when subjected to high demand, voltage variations, or blackouts [5].

In general, a three-phase distribution network operates under unbalanced conditions where the loads may have different magnitudes per phase. This may cause power quality problems [6], [7]. For instance, load imbalance may produce zero-sequence currents, so an extra wire is required. Conventional three-phase inverters cannot alleviate such phase imbalance [8]. However, this issue may be relieved by incorporating three-phase four-wire inverters—which could be adapted for on-board or off-board EV charger applications.

The basic four-wire inverter topology comprising a split dc-link capacitor was presented in [9]. This is a simple topology consisting of six switches only. Also in [9], a size reduction of the neutral inductor was achieved by suppressing the third-order harmonic in the neutral current. A nonlinear control method was presented in [10] to ensure power quality and electromagnetic compatibility by reducing the inverter leakage current. However, in both cases, bulky capacitors are required to limit the voltage ripple on the dc bus whenever imbalance arises at the ac side of the inverter. Despite the simplicity of the four-wire topology, the voltage balance control of the split capacitors is complex and sensitive to disturbances [11].

More complex four-wire topologies with eight switches have been investigated since. In addition to provide a circulation path for neutral current, these topologies exhibit a high power density as split dc link capacitors are not required. Some references have proposed enhancements to the topology. For instance, in [12] the neutral current was reduced by using a control strategy to balance the output voltage. In [13], the output voltage was regulated for unbalanced conditions. In [14], an adaptive frequency control scheme was implemented to handle grid frequency variations and provide low total harmonic distortion (THD) in voltage and current. Despite its advantages over simpler topologies, the main drawback of a four-wire configuration with eight switches is the propagation of electromagnetic interference (EMI) resulting from the neutral line being directly linked to the dc busbars. Moreover, its control strategy is complex, as the phase and neutral legs cannot be independently controlled [15].

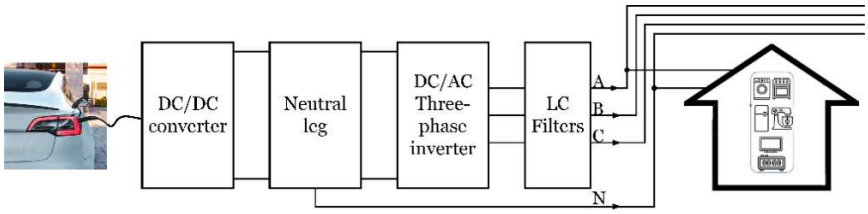


Fig. 1. Three-phase four-wire inverter with neutral leg for an EV charger in vehicle-to-grid mode.

Another topology reported in the literature is the three-phase inverter with an independently controlled neutral leg, which combines the split dc link inverter and the four-leg topology. In [16] a balanced neutral point voltage was achieved for this topology by means of a control scheme, allowing the capacitance of the dc link capacitors to be reduced. This was also achieved in [17]. An increase in dc voltage utilization of around 15% was accomplished by injecting third harmonics into the neutral point [18]. The main advantage of having an independently controlled neutral leg is the reduction in complexity of the control scheme, as the control of the phase legs and the neutral legs is independent. This also prevents EMI in the dc and ac terminals [19]. The use of a four-wire inverter for automotive applications was presented in [20], where the independently controlled neutral leg enabled relieving the imbalance issues on the split capacitors.

A further negative consequence of the imbalance between phases at the ac side is the generation of second-order ripple on the dc bus of the inverter [21]. If care is not exercised, the useful life of batteries can be reduced, which is a concern when they are employed as a dc source for EV chargers [22]. To mitigate the effect of low-order harmonic components, compensation techniques have been developed [23], [24]. However, these schemes require additional passive and active elements—increasing the volume and cost of the inverter. In [25] a four-wire inverter with an improved neutral leg was presented, where the power density was increased by eliminating one split capacitor from the conventional neutral leg topology in [15]. Moreover, the improved neutral leg enables reducing the second-order ripple with no need for additional components. Nonetheless, for higher power demand in an isolated grid, the inverter output power and capacitance requirements of the neutral leg increase. This, in turn, leads to an increment in volume and cost of the inverter.

The adoption of compound semiconductor devices based on silicon carbide (SiC) and gallium nitride for onboard battery chargers [26] and fast EV charging stations [27] have enabled an increase in the power density of EV chargers. This improved power density over Si-based configurations is facilitated by the size reduction of passive components due to an increased switching frequency [28]. For instance, the use of SiC MOSFETs enables increasing the switching frequency to 250 kHz in the ac/dc converter studied in [29] which, in turn, reduces the required inductance of the grid-side filter. However, in four-wire topologies such as the one studied in [20], the capacitance of the split capacitors cannot be reduced by simply increasing the switching frequency as this would also increase the second-order ripple in the dc bus.

This paper presents two main contributions to help bridge the previously discussed research gaps. The first one is the introduction of a novel SiC-based three-phase four-wire inverter suitable to supply electricity to an isolated grid. The topology was primarily designed for EV chargers but could be extended to battery-based energy storage systems. The second contribution is the associated control strategy for the inverter, which enables a simultaneous provision of neutral current and the reduction of second-order ripple on the dc bus under unbalanced conditions. This is possible because the control loops of the phase legs and the neutral leg are independent. The analysis and simulation and experimental results presented in the paper demonstrate that the capacitance requirements of the neutral leg in the presented topology are reduced compared to the topologies introduced in [15] and [25], leading to an increased power density and lower production costs.

II. Operation of a Four-Leg Buck Inverter

The topology under investigation consists of a three-phase inverter with an independently controlled neutral leg. Each half bridge forms an equivalent dc/dc buck converter per phase to supply the loads. The neutral leg is connected to the common neutral point of the three-phase load. This way, the four-leg buck inverter consists of 8 switches as shown in Fig. 2: S_1-S_6 for phases *A*, *B*, and *C* and S_{N1}-S_{N2} for the neutral leg.

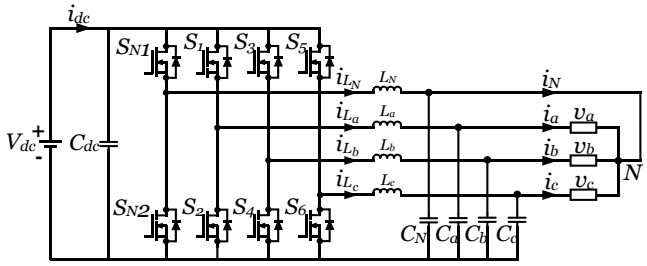


Fig. 2. Three-phase four-leg buck inverter.

As the neutral leg is controlled to produce half of the dc voltage V_{dc} only, the voltage of the neutral capacitor v_{CN} is

$$v_{CN} = \frac{1}{2}V_{dc} \tag{1}$$

The voltages in the filter capacitors of the phase legs v_{Ca}, v_{Cb}, v_{Cc} are given by

$$\begin{aligned} v_{Ca} &= V_o \sin(\omega t) + \frac{1}{2}V_{dc} \\ v_{Cb} &= V_o \sin\left(\omega t - \frac{2}{3}\pi\right) + \frac{1}{2}V_{dc} \\ v_{Cc} &= V_o \sin\left(\omega t + \frac{2}{3}\pi\right) + \frac{1}{2}V_{dc} \end{aligned} \tag{2}$$

where V_o is the output voltage and half of the dc input voltage has been compensated. Since the inverter consists of dc/dc buck converters, the voltages in (2) are always positive.

The phase-to-neutral voltages v_a, v_b, v_c are the difference between the voltage of the filter capacitors in (2) and v_{CN} in (1), namely

$$\begin{aligned} v_a &= v_{Ca} - v_{CN} = V_o \sin(\omega t) \\ v_b &= v_{Cb} - v_{CN} = V_o \sin\left(\omega t - \frac{2}{3}\pi\right) \\ v_c &= v_{Cc} - v_{CN} = V_o \sin\left(\omega t + \frac{2}{3}\pi\right) \end{aligned} \tag{3}$$

To reduce the second-order ripple on the dc bus of the inverter, the second-order compensation voltage

$$v_{2\omega} = V_{2\omega} \sin(2\omega t + \theta_{2\omega}) \tag{4}$$

is added to the expressions in (2), leading to

$$\begin{aligned} v_{Ca} &= V_o \sin(\omega t) + \frac{1}{2}V_{dc} + v_{2\omega} \\ v_{Cb} &= V_o \sin\left(\omega t - \frac{2}{3}\pi\right) + \frac{1}{2}V_{dc} + v_{2\omega} \\ v_{Cc} &= V_o \sin\left(\omega t + \frac{2}{3}\pi\right) + \frac{1}{2}V_{dc} + v_{2\omega} \end{aligned} \tag{5}$$

Similarly, $v_{2\omega}$ is added to the neutral capacitor and, thus,

$$v_{CN} = \frac{1}{2}V_{dc} + v_{2\omega} \tag{6}$$

Despite the additional second-order voltage in the phase and neutral capacitors, the output phase voltages will remain balanced. This can be verified by subtracting (6) from the equations in (5), resulting in the same expressions as in (3).

The capacitance of the filter capacitors C_a, C_b, C_c is assigned the same value as that for the neutral leg capacitor C_N, which implies $C_N = C_a = C_b = C_c$. The rationale behind this consideration is to ensure that the decoupling current flowing through all capacitors is the same so none of the four legs is overstressed. Thus, the currents i_{Ca}, i_{Cb}, i_{Cc} through the filter capacitors and neutral leg capacitor i_{CN} are given as:

$$\begin{aligned} i_{Ca} &= \omega C_a V_o \cos(\omega t) + i_{2\omega} \\ i_{Cb} &= \omega C_b V_o \cos\left(\omega t - \frac{2}{3}\pi\right) + i_{2\omega} \\ i_{Cc} &= \omega C_c V_o \cos\left(\omega t + \frac{2}{3}\pi\right) + i_{2\omega} \\ i_{CN} &= i_{2\omega} \end{aligned} \tag{7}$$

where $i_{2\omega}$ is a second-order current, defined as

$$i_{2\omega} = 2\omega C_n V_{2\omega} \cos(2\omega t + \theta_{2\omega}) \tag{8}$$

From (5) and (7), expressions for power of the phase capacitors p_{Ca}, p_{Cb}, p_{Cc} and neutral capacitors p_{CN} are

$$\begin{aligned} p_{Ca} &= v_{Ca} i_{Ca}, \quad p_{Cb} = v_{Cb} i_{Cb} \\ p_{Cc} &= v_{Cc} i_{Cc}, \quad p_{CN} = v_{CN} i_{CN} \end{aligned} \tag{9}$$

The total instantaneous power of the capacitor legs p_{Ct} is calculated by adding the expressions in (9) and conducting algebraic simplification:

$$\begin{aligned} p_{Ct} &= p_{Ca} + p_{Cb} + p_{Cc} + p_{CN} \\ &= 4\omega C_n V_{2\omega} V_{dc} \cos(2\omega t + \theta_{2\omega}) \end{aligned} \tag{10}$$

For the suppression of second-order ripple on the dc bus, the following condition must be fulfilled

$$p_{Ct} = P_{2\omega} \tag{11}$$

Thereby, if $P_{2\omega}$ is offset by the total neutral and filter capacitor power, the magnitude of the second-order voltage ripple $V_{2\omega}$ in (4) is defined as:

$$V_{2\omega} = \frac{P_{2\omega}}{4\omega C_n V_{dc}} \tag{12}$$

The ratio of the ac output power to the magnitude of the second-order power ripple is determined as:

$$p_{ac} = P_o + P_{2\omega} \cos(2\omega t) \tag{13}$$

III. Control Structure

The control strategy for the three-phase four-leg buck inverter consists of two cascaded loops as shown in Fig. 3: one for the neutral leg and another for the three-phase legs. The inverter legs are independently controlled as they are decoupled at the fundamental frequency. This structure allows for the reduction of second-order harmonics on the dc bus.

It must be highlighted that a control strategy for interfacing the presented inverter with a traditional ac distribution grid falls out of the scope of this paper. The reader is referred to [30] for further information on how to achieve this.

A. Three-phase closed-loop controller

The four-leg buck inverter is designed to operate in an off-grid system. This requires the voltage to remain balanced when different loads per phase are connected to it. Proportional-resonant (PR) controllers are used for the phase legs due to their suitability to track sinusoidal references.

The outer ac voltage loop regulates the output voltage of the inverter at the fundamental frequency, while the inner current loop regulates the output current. This cascaded control structure provides the pulse width modulation (PWM) signal for switches S_1-S_6. The PR controllers are

$$G_{PR\_v}(s) = k_{P\_v} + \frac{2\omega_c k_{r\_v} s}{s^2 + 2\omega_c s + \omega^2} \tag{14}$$

$$G_{PR\_i}(s) = k_{P\_i} + \frac{2\omega_c k_{r\_i} s}{s^2 + 2\omega_c s + \omega^2} \tag{15}$$

where k_{P_v} and k_{r_v} are the proportional and resonant gains for the outer voltage loop in (14). Similarly, k_{P_i} and k_{r_i} are the proportional and resonant gains for the inner current controller loop in (15), while ω_c is the cut-off frequency and ω the resonant frequency for which the PR controllers act. The fundamental frequency is 50 Hz (314 rad/s).

Fig. 4 shows the Bode diagram of the inner current control loop. A phase margin of 88° is exhibited for gains $k_{P\_i} = 20.2$ and $k_{r\_i} = 795$. These gains were obtained heuristically using the frequency response plot.

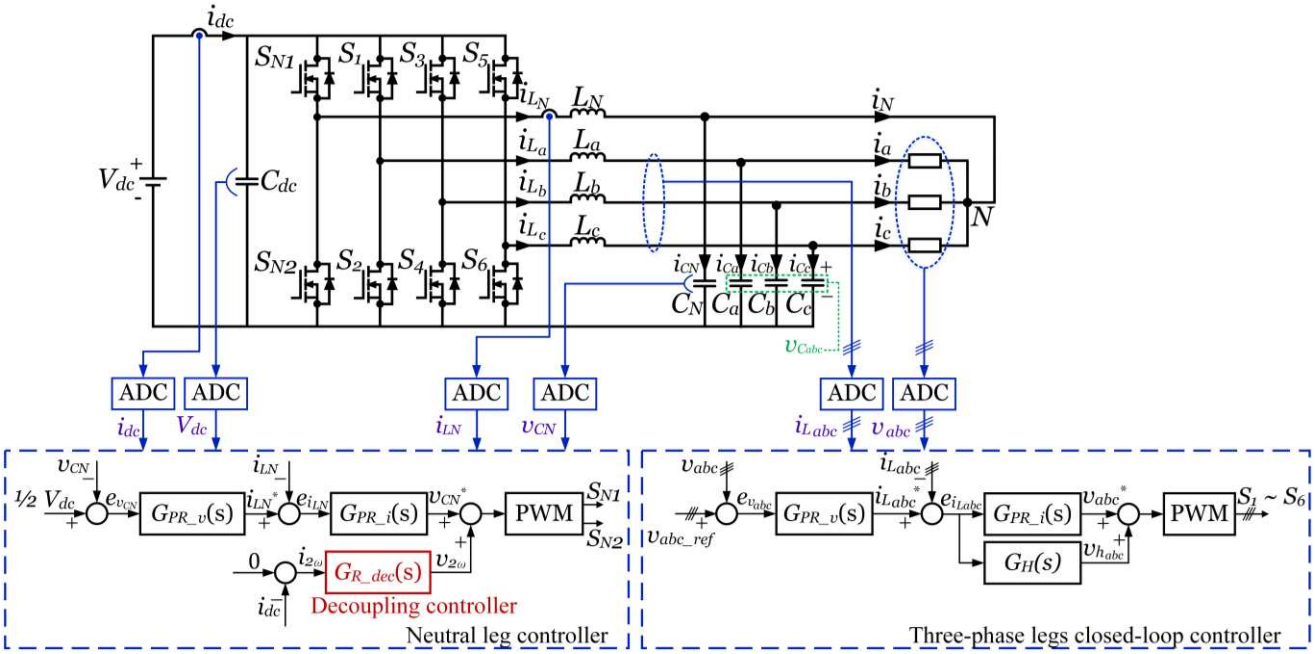


Fig. 3. Control scheme for the four-leg buck inverter.

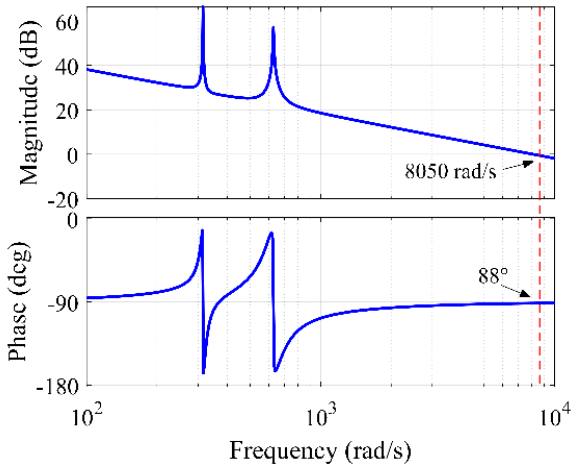


Fig. 4. Bode plot of the inner current control loop with a harmonic compensator for the four-leg buck inverter.

In addition to controller $G_{PR\_i}(s)$ operating at the grid frequency, a harmonic compensator $G_H(s)$ was implemented in parallel within the current loop controller. This was done to compensate the second-order harmonics by introducing a decoupling element for the reduction of the second-order ripple on the dc side. $G_H(s)$ has a resonant behavior at the desired frequency to be compensated and is defined as

$$G_H(s) = \frac{2\omega_c k_{r\_h} s}{s^2 + 2\omega_c s + (h\omega)^2} \tag{16}$$

where k_{r_h} is the resonant term and h is the harmonic number. The resonance frequency for $G_H(s)$ occurs at twice the grid frequency (100 Hz) and $k_{r\_h} = 415$.

B. Neutral leg controller

The neutral leg is regulated to provide a neutral current path. This is achieved by adopting similar voltage and current control loops as for the three-phase control. All parameters in $G_{PR\_i}(s)$ and $G_{PR\_v}(s)$ remain the same. To maintain a constant neutral point voltage, the reference signal is defined as half the dc input voltage V_{dc} and the feedback signal is the neutral capacitor voltage v_{CN}. The neutral inductor current i_{LN} is the feedback signal for the inner current loop (see Fig. 3).

To reduce the second-order ripple on the dc bus and achieve active power decoupling, a second-order resonant controller $G_{R\_dec}(s)$ is used. The decoupling current $i_{2\omega}$ is derived from the dc bus current signal i_{dc}, from which its second-order components are filtered out. The controller receives $i_{2\omega}$ as a reference, as defined in (8), to produce the second-order compensation voltage $v_{2\omega}$ as defined by (4), which is in turn injected to the phase and neutral capacitors as described by (5) and (6). $G_{R\_dec}(s)$ is defined by

$$G_{R\_dec}(s) = \frac{2\omega_c k_{r\_dec}(2\omega)s}{s^2 + 2\omega_c(2\omega)s + (2\omega)^2} \tag{17}$$

where k_{r_dec} is the resonant gain with a value of 972.

IV. Comparison of Four-Wire Topologies

The most commonly used topology for four-wire systems is shown in Fig. 5, where larger split capacitors are required to restrict the amplitude of the second-order ripple on the dc bus.

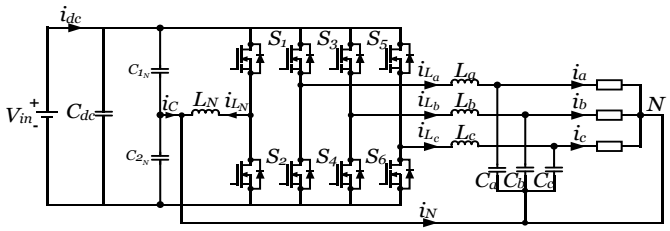


Fig. 5. Three-phase four-wire inverter with conventional neutral leg.

A. Neutral leg capacitance requirements

The minimum dc voltage requirement for unbalanced conditions is given by twice the grid voltage and twice the second-order voltage ripple magnitude, that is

$$V_{dc} = 2\sqrt{2}V_{rms} + 2V_{2\omega} \tag{18}$$

where V_{rms} is the phase-to-ground rms voltage.

The amplitude of the second-order power ripple $P_{2\omega}$ depends on the imbalance ratio δ and the output power P_o:

$$P_{2\omega} = P_o\delta \tag{19}$$

where δ is obtained by relating the positive sequence current I_+ and the negative sequence current I_- as

$$\delta = \frac{I_-}{I_+} \tag{20}$$

The sizing of the capacitance C_{conv} in a conventional neutral leg requires two bulky capacitors clamped with the leg to limit the magnitude of $P_{2\omega}$ on the dc bus. This is determined as [25]

$$C_{conv} = \frac{8\gamma P_o}{\omega(V_{max}^2 - 8V_{rms}^2)} \tag{21}$$

where the peak voltage V_{max} in the dc bus is estimated as

$$V_{max} = V_{dc} + \Delta V \tag{22}$$

where ΔV is the voltage variation of V_{dc}, which can be of around 0.5 to 1% [23], [24].

As in (1), the capacitor voltage v_{CN} needs to fulfil the following condition with respect to the ac voltage:

$$v_{CN} = \sqrt{2}V_{rms} \tag{23}$$

Therefore, from (12) and (23) the required neutral leg capacitance C_{n-buck_inv} in the three-phase four-leg buck inverter is defined as:

$$C_{n-buck\_inv} = \frac{\delta P_o}{2\omega V_{max}^2 - 4\omega\sqrt{2}V_{rms}V_{max}} \tag{24}$$

As discussed before, the capacitance requirement of each phase leg is similar as that of the neutral leg. Therefore,

$$C_a = C_b = C_c = C_{n-buck\_inv} = \frac{\delta P_o}{2\omega V_{max}^2 - 4\omega\sqrt{2}V_{rms}V_{max}} \tag{25}$$

Fig. 6 shows that the neutral capacitance requirements as a function of the output power P_o for the four-leg buck inverter can be up to four times lower than for the improved neutral leg and up to eight times lower than for a conventional neutral leg.

Fig. 7 shows the capacitance requirements for the leg of phase *A* of the four-leg buck inverter. Unlike the conventional topology [15] or improved neutral leg topology [25], the capacitance value, obtained with (25), is identical for all three phases and equal to the capacitance of the neutral leg for an output power ranging from 1 to 10 kW (plotted in Fig. 6 with a dashed red font) as described by (24).

As a way of an example, let $P_o = 2$ kW and $V_{max} = 750$ V. Using (24), a capacitance $C_{n-buck\_inv} = 19.32$ µF is required for the neutral leg in a 50 Hz system. A simulation of the four-leg buck inverter was conducted in MATLAB/Simulink to verify the capacitance requirements to mitigate the second-order ripple on the dc bus. Results are shown in Figs. 8 and 9.

As shown in Fig. 8, the amplitude of the voltage ripple of the neutral capacitor $V_{2\omega}$, calculated from (12), reaches the boundary $\sqrt{2}\,V_{rms}$ defined in (23). To prevent inverter malfunction, the second-order voltage ripple must not overlap with the phase voltages, as shown by the figure, as otherwise the ac voltages can be deformed.

Fig. 9 shows the voltages of the phase filter capacitors. As observed, these are clearly deformed by the injection of the decoupling current to the neutral and filter capacitors. (**Note**: Section V shows in more detail the second-order components present in the filter and neutral capacitors.)

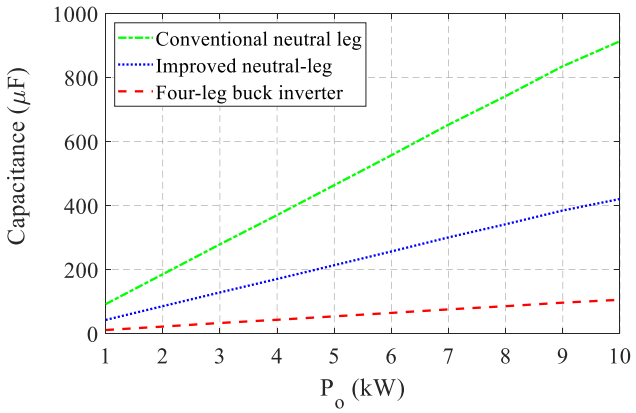


Fig. 6. Total neutral leg capacitance comparison (V_{dc} = 750 V; imbalance ratio δ = 0.5)

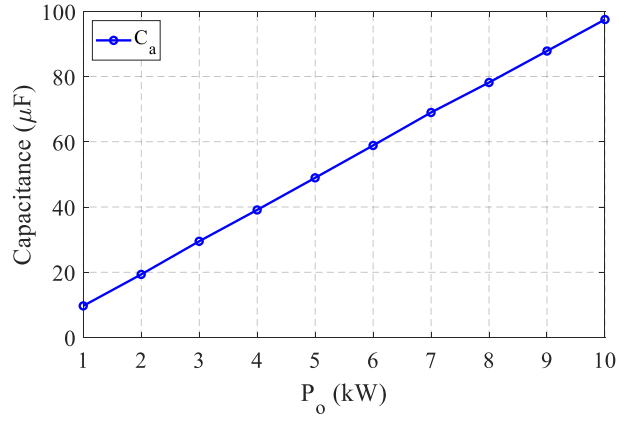


Fig. 7. Capacitance requirements for the leg of phase *A* (V_{dc} = 750 V; imbalance ratio δ = 0.5). These are similar as for the legs of phases *B* and *C* and the neutral leg.

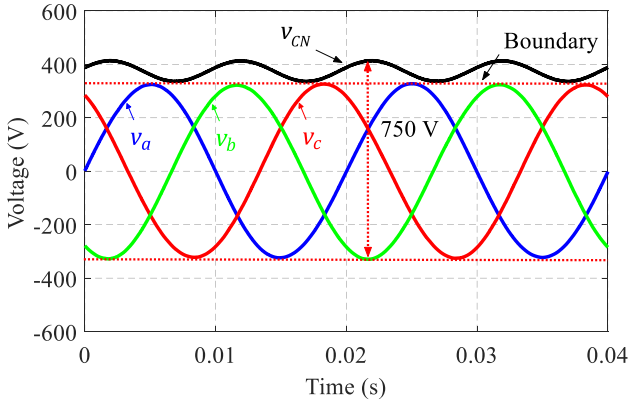


Fig. 8. Simulation results. Verification of the capacitance requirement of the four-leg buck inverter.

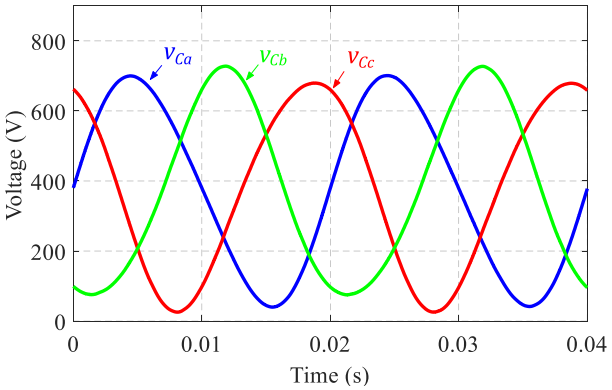


Fig. 9. Simulation results. Verification of the capacitance requirement of the four-leg buck inverter. The filter capacitor voltages exhibit a second-order component.

B. LC filter selection

The capacitance C_f and inductance L_f of the LC filter for the conventional and improved neutral leg topologies in [31] and [32] are obtained with:

$$C_f = \frac{0.05}{\omega Z_b} \tag{26}$$

$$\Delta I_{Lf\_max} = \frac{V_{dc}}{6 f_{sw} L_f} \tag{27}$$

where Z_b is the base impedance of the inverter, ΔI_{Lf_max} is the maximum output current, and f_{sw} is the switching frequency. C_f in (26) is obtained by limiting the power factor drop to less than 5%. In contrast, L_f in (27) is selected so as to limit the ripple of the output current to 10% of ΔI_{Lf_max}.

For the four-leg buck inverter, the capacitance of the LC filter depends of the requirements established by (25).

The inductance L_n of the neutral leg inductor is calculated from the current ripple arising from the additional stress brought by the decoupling current using

$$\Delta I_N = \frac{V_{dc} - V_{CN}}{L_n} \cdot \frac{D}{f_{sw}} \tag{28}$$

where D is the duty ratio.

The dc link capacitor for filtering f_{sw} is determined as [33]:

$$C_{dc} = \frac{I_{rms}}{\Delta V_{dc} f_{sw}} \tag{29}$$

Table I gives the details of the passive components for the three 2 kW four-wire inverters investigated in this paper, which were calculated from (21), (24)-(29).

As evidenced by (27) and (28), the value of L_f and L_n depends directly on the switching frequency. Moreover, these inductances are expected to be large due to the additional current stress caused by the imbalance on the system and the elimination of the second-order ripple on the dc bus. The current stress impacts the neutral and phase leg inductors and switches since they are connected in series.

C. Size and costs

A volume comparison of the inductors and film capacitors used in the four-wire inverters is given in Fig. 10 for a rated output power $P_o = 2$ kW. The conventional and improved neutral leg have higher volumes of ~40% and ~19% with respect to the four-leg buck inverter.

Fig. 11 shows a cost comparison of the passive components of the topologies. The four-leg buck-inverter affords a decrease in cost of ~42% and ~25% over the conventional and improved neutral leg topologies. (Further details of the passive components can be found in [34]-[38].)

Fig. 12 shows an additional volume comparison for the inverter topologies for different output power, while Fig. 13 shows a comparison for cost. The volume of the four-leg buck inverter at 10 kW can decrease by ~1.8 times compared to the conventional neutral leg inverter and by ~1.2 times compared to the improved neutral leg inverter. In terms of cost, the four-leg buck inverter reduces the construction costs by nearly 2.5 times compared to the conventional topology and by ~1.74 times with respect to the improved neutral leg topology.

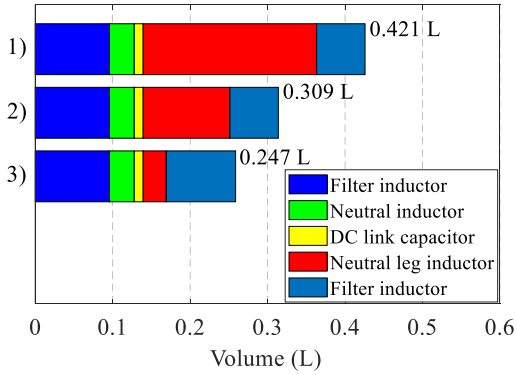


Fig. 10. Comparison of the volume of passive components for 2 kW four-wire topologies: 1) Conventional neutral leg. 2) Improved neutral leg. 3) Four-leg buck inverter.

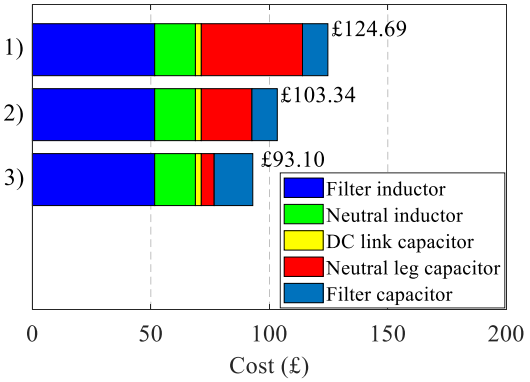


Fig. 11. Cost comparison of the passive components of 2 kW four-wire topologies: 1) Conventional neutral leg. 2) Improved neutral leg. 3) Four-leg buck inverter.

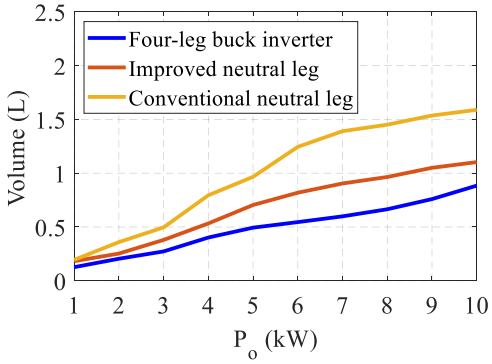


Fig. 12. Volume comparison of the passive components of four-wire topologies for different output power.

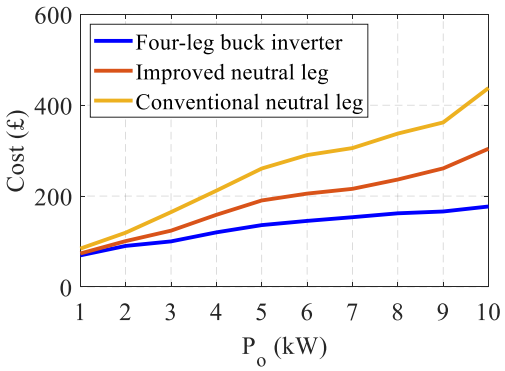


Fig. 13. Cost comparison of the passive components of four-wire topologies for different output power.

Table I provides the total volume and cost of the three topologies under comparison. As evidenced by Figs. 10 and 11, the difference in volume (and thus cost) is mainly driven by the neutral leg capacitor (see the red shading in the bar charts). This is because the capacitor of the neutral leg of the four-leg buck inverter is smaller by 8 times when compared to the conventional topology and by 4 times with respect to the improved neutral leg topology. This has a corresponding implication in cost. As it can be observed, the dc link capacitor, phase filter, and neutral leg inductors have a similar volume and cost regardless of the topology (see the dark blue, green, and yellow shadings in the bar charts).

TABLE I.
MAIN COMPONENTS FOR 2 kW THREE-PHASE FOUR-WIRE TOPOLOGIES

		Conv. neutral-leg [15]	Improved neutral leg [25]	Four-leg buck inverter
MOSFETs		**8 units**	**8 units**	**8 units**
INDUCTOR	**Filter**	**3 units** 1 mH; 5 A 0.031 L ea. £17.20 ea.	**3 units** 1 mH; 5 A 0.031 L ea. £17.20 ea.	**3 units** 1 mH; 5 A 0.031 L ea. £17.20 ea.
	Neutral leg	**1 unit** 1 mH; 5 A 0.031 L ea. £17.20 ea.	**1 unit** 1 mH; 5 A 0.031 L ea. £17.20 ea.	**1 unit** 1 mH; 5 A 0.031 L ea. £17.20 ea.
FILM CAPACITOR	**dc link**	**1 unit** 3 µF; 900V 0.011 L ea. £2.48 ea.	**1 unit** 3 µF; 900V 0.011 L ea. £2.48 ea.	**1 unit** 3 µF; 900V 0.011 L ea. £2.48 ea.
	Filter	**3 units** 5 µF; 350 V 0.208 L ea. £3.57 ea.	**3 units** 5 µF; 350 V 0.208 L ea. £3.57 ea.	**3 units** 20 µF; 500 V 0.055 L ea. £7.24 ea.
	Neutral leg	**2 units** 100 µF; 500 V 0.112 L ea. £21.35 ea.	**1 unit** 100 µF; 500 V 0.112 L ea. £21.35 ea.	**1 unit** 20 µF; 500V 0.028 L ea. £5.43 ea.
Total units		**18 units**	**17 units**	**17 units**
Total size (L)		**0.421**	**0.309**	**0.247**
Total cost (£)		**124.69**	**103.34**	**93.10**

D. Impact of decoupling current

1) Neutral leg

The injection of decoupling current $i_{2\omega}$ to capacitor C_N as shown in (7) causes current stress on both the switches and the inductor. The neutral inductor current is

$$i_{LN} = i_n + i_{CN} \tag{30}$$

From the expressions for current of the neutral leg capacitor in (7) and the second-order voltage ripple in (12), the magnitude of the compensation current $I_{2\omega}$ is:

$$I_{2\omega} = i_{CN} = \frac{P_{2\omega}}{2V_{dc}} \tag{31}$$

Current stress is not present in the neutral leg of the conventional topology as there is no flow of decoupling current. In the four-leg buck inverter and the improved neutral leg inverter, the decoupling current leads to current stress.

2) Three-phase legs

Since the filter capacitors store second-order components, the decoupling current flows through the three-phase inductor legs. Thus, current stress occurs in these inductors as well. Using Kirchhoff's current law, the currents of the phase inductors are

$$\begin{aligned} i_{La} &= i_a + i_{Ca} \\ i_{Lb} &= i_b + i_{Cb} \\ i_{Lc} &= i_c + i_{Cc} \end{aligned} \tag{32}$$

From (7), the total phase inductor currents are:

$$\begin{aligned} i_{La} &= i_a + \omega C_a V_o \cos(\omega t) + I_{2\omega} \\ i_{Lb} &= i_b + \omega C_b V_o \cos(\omega t - 120°) + I_{2\omega} \\ i_{Lc} &= i_c + \omega C_c V_o \cos(\omega t + 120°) + I_{2\omega} \end{aligned} \tag{33}$$

In (33), an additional decoupling current $I_{2\omega}$ is observed in each phase inductor of the four-leg buck inverter. The current magnitude of the filter inductor depends on the imbalance factor present in the three-phase system.

Fig. 14 shows the impact of the decoupling current in the neutral and phase leg inductors when the inverter operates at different output power and under an imbalance factor $\delta = 0.5$. The current stress on the neutral and phase leg inductors resulting from the inclusion of decoupling current is ~1.2 times higher for an output power ranging from 0 to 10 kW compared to when the decoupling controller is not active.

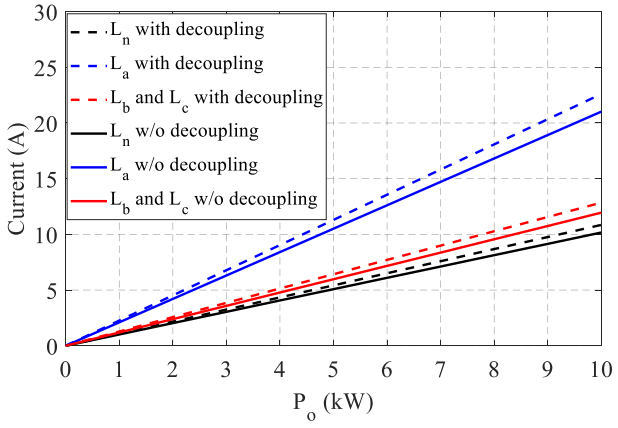


Fig. 14. Current stress on the neutral and phase leg inductors of the four-leg buck inverter with an imbalance factor $\delta = 0.5$. The impact in phases *B* and *C* is the same as the load imbalance occurs in phase *A*.

V. Simulation and Experimental Results

A. Simulation results

1) *Step change in load with no decoupling controller*

To verify the performance of the four-leg buck inverter, a co-simulation was done via MATLAB/Simulink and PLECS (which considered the SiC MOSFET C2M0080120D model from Wolfspeed [39]). Table II shows the simulation parameters. An imbalance ratio $\delta = 0.5$ was used. For balanced load conditions $R_a = R_b = R_c = 105\ \Omega$. Imbalance arises 100 ms into the simulation when the load in phase A reduces to $R_{a,imb} = 52\ \Omega$. Fig. 15 shows the simulation results.

TABLE II.
Simulation and Experimental Validation Parameters

Parameter	Value
DC input voltage	750 V
AC output voltage (rms)	230 V
Grid filter inductance	1 mH
Neutral inductance	1 mH
Grid filter capacitance	20 µF
Neutral capacitance	20 µF
Grid frequency	50 Hz
Switching frequency	20 kHz

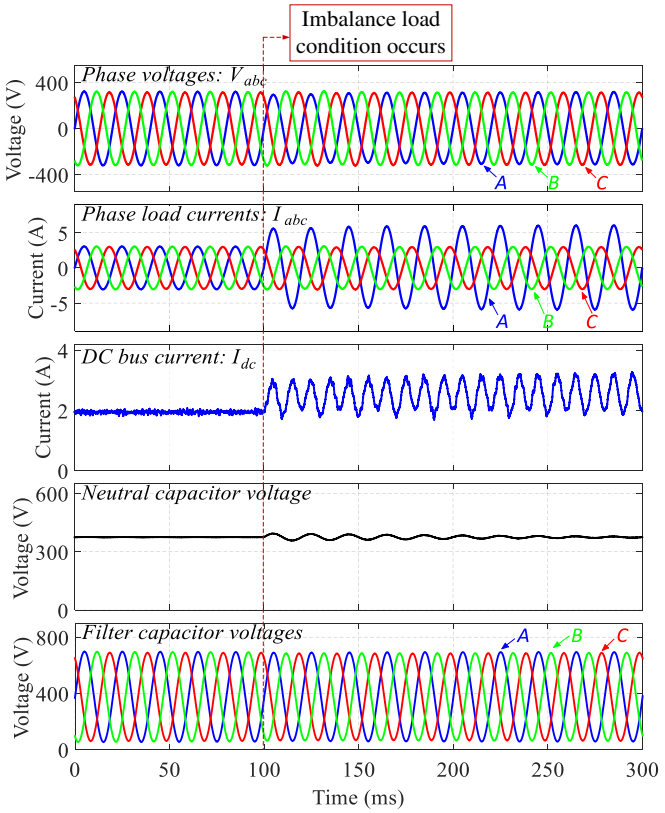


Fig. 15. Simulation results of the four-leg buck inverter without decoupling controller.

Following the imbalance, the rms current of phase A increases from 2.3 A to 4.6 A. However, the phase voltages remain unaffected. As a result, a second-order ripple with an amplitude of ~1.4 A appears on the dc bus current. The voltage on the neutral leg capacitor remains constant at 375 V after the load change as the decoupling control is not active.

2) *Step change in load with decoupling controller*

The co-simulation was repeated for the same load conditions as before. A step change in the load of phase A occurs at 100 ms and results are shown in Fig 16. A similar behavior is observed in the phase voltages and phase currents as when the decoupling controller is inactive. However, the second-order current ripple on the dc bus reduces following a transient behavior when such controller is in operation. This ripple is transferred to the phase filter and neutral leg capacitors filters, whose waveforms are deformed by second-order components. The voltage amplitude of the second-order voltage ripple in the neutral leg capacitor is 48.7 V, which is consistent following calculation with (12).

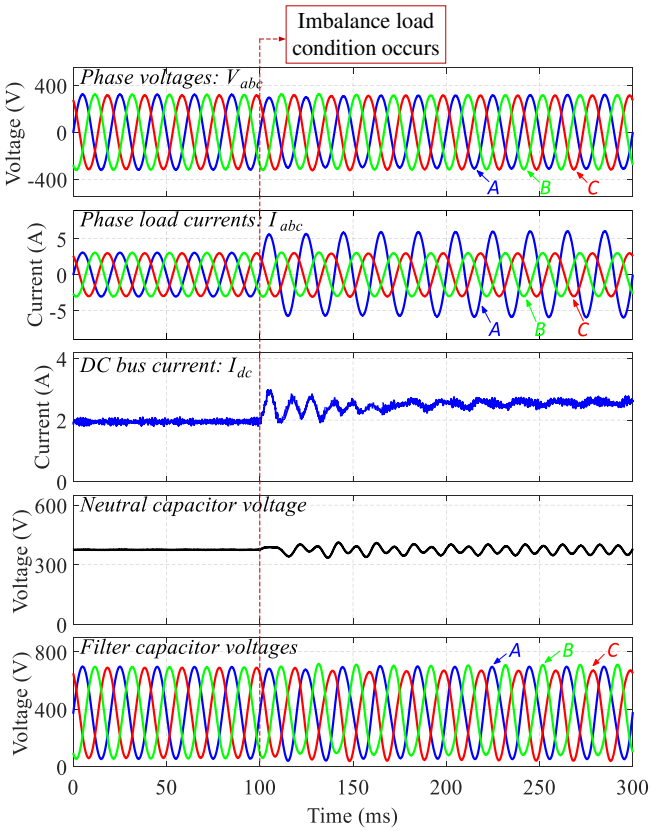


Fig. 16. Simulation results of the four-leg buck inverter with decoupling controller implemented.

3) *Losses*

These were obtained via simulation in PLECS of the SiC MOSFET C2M0080120D model [39]. Similar parameters as for the efficiency measurements were used. Simulation results are shown in Fig. 17.

Fig. 17 shows that the losses in the conventional neutral leg topology are lower compared to the other two. The conduction and switching losses in the phase legs of the four-leg buck-inverter are greater by ~4.2% compared to the improved neutral leg inverter. This is due to the increment in current stress in the phase legs resulting from the flow of decoupling current to the filter capacitors. However, the four-leg buck inverter exhibits lower neutral conduction and switching losses of ~17% compared to the improved neutral leg inverter. This is because the decoupling current is distributed across all legs—whereas for the improved neutral leg topology the neutral leg fully receives the decoupling current impact.

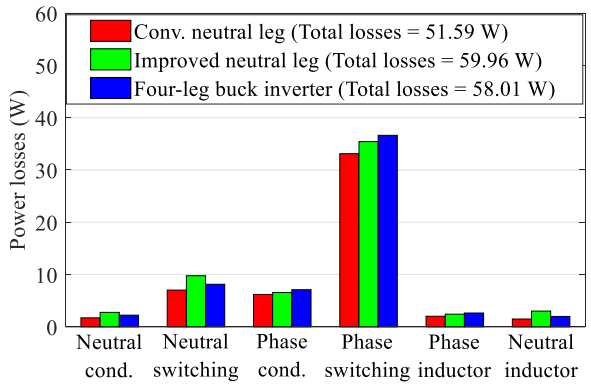


Fig. 17. Comparison of power losses in the neutral and phase legs of the topologies at 2 kW.

Additional simulations were conducted to compare the power losses in the three topologies under a maximum load current (at 11 kW). Although the total losses for the topologies naturally increase for a greater output power (see Fig. 18), the improved neutral leg inverter still exhibits the highest amount of losses. The presented four-leg buck inverter shows an improvement, but still exhibits higher losses than the topology with the conventional neutral leg. More specifically, the conduction and switching losses in the phase legs of the four-leg buck-inverter are greater by ~3.8% compared to the improved neutral leg inverter, while the neutral conduction and switching losses are lower by ~16% compared to the same inverter.

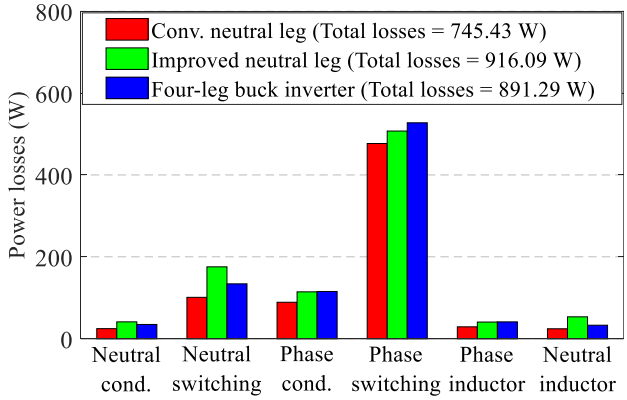


Fig. 18. Comparison of power losses in the neutral and phase legs of the four-wire topologies at 11 kW.

Simulations of the four-leg buck inverter have been also conducted to quantify the power losses for different power ranges when adopting SiC-MOSFETs and Si-based semiconductors. For this exercise, switches Si-IGBT IKW25N120H3 [40] and SiC-MOSFET C2M0080120D [39] were adopted due to their similar power ratings, as shown in Table III.

Table III. Switching devices for power losses simulation.

Device	Maximum voltage	Maximum current ($T_c = 100°C$)
SiC-MOSFET (C2M0080120D)	1200 V	24 A
Si-IGBT (IKW25N120H3)	1200 V	25 A

Results from the comparison are provided in Fig. 19. Implementation of the decoupling controller inevitably increases the power losses when either semiconductor device is adopted. However, an inverter based on Si-IGBTs exhibits higher losses of ~30% for output powers ranging from 0 to 11 kW when compared to a device based on SiC-MOSFETs. The reduced power losses make of the SiC-based inverter a more suitable topology compared to a Si-based counterpart.

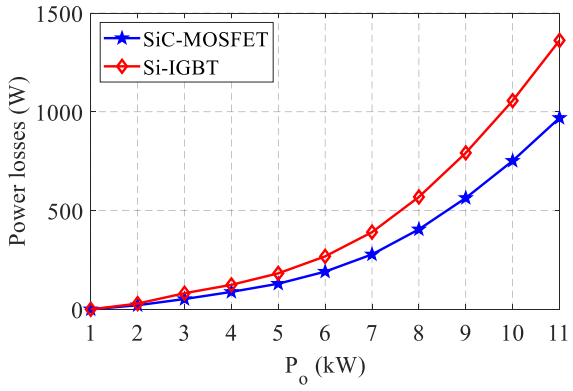


Fig. 19. Comparison of power losses of the four-leg buck inverter based on Si-IGBTs and SiC-MOSFETs.

Note: To mitigate the temperature increase resulting from the additional stress in the switches, implementation of a cooling system would be crucial. Reference [25] presents the selection of a heat sink with cooler fan [41] applicable to 11-kW conventional and improved neutral leg topologies. A similar cooling system may be adopted for the four-leg buck inverter. Although this would invariably increase the volume of the topology, assessing the impact of cooling systems and thermal management falls out of the scope of this work.

B. Experimental results

The setup for the experimental validation of the four-leg buck inverter is shown in Fig. 20. The main hardware consists of an Imperix platform with SiC MOSFETs (C2M0080120D) power modules [42]. The control algorithm for the phase legs and the neutral leg was achieved by an Imperix B-Box 3.0 [43]. A switching frequency of 20 kHz was used.

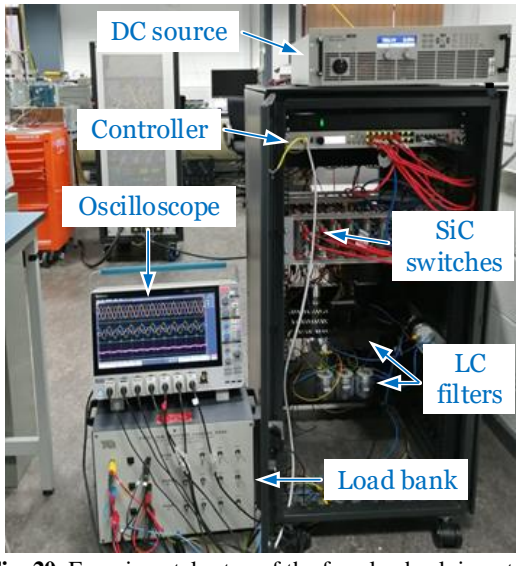


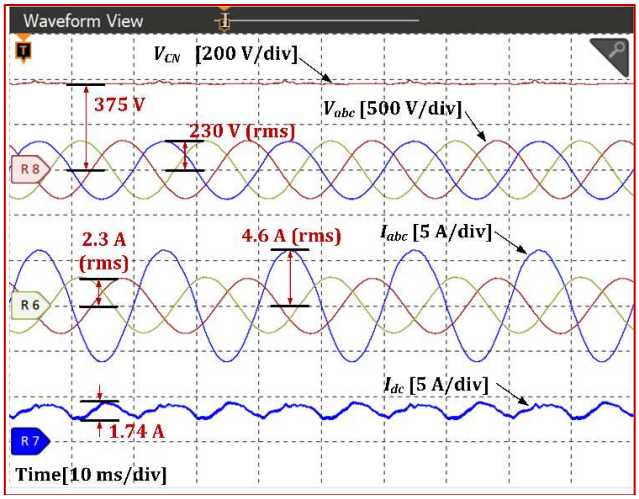
Fig. 20. Experimental setup of the four-leg buck inverter.

To provide the feedback signals for the outer voltage control loops in Fig. 3, the DIN 800V voltage sensor was employed [44]. For the phase and neutral inductor currents, the sensors embedded in the SiC power modules were used for the inner current loops. However, the dc bus current was measured with a DIN 50 A current sensor [45]. To display the voltage and current measurements the Tektronix MSO58 oscilloscope was used. Table II summarizes the corresponding parameters of the four-leg buck inverter built in the laboratory.

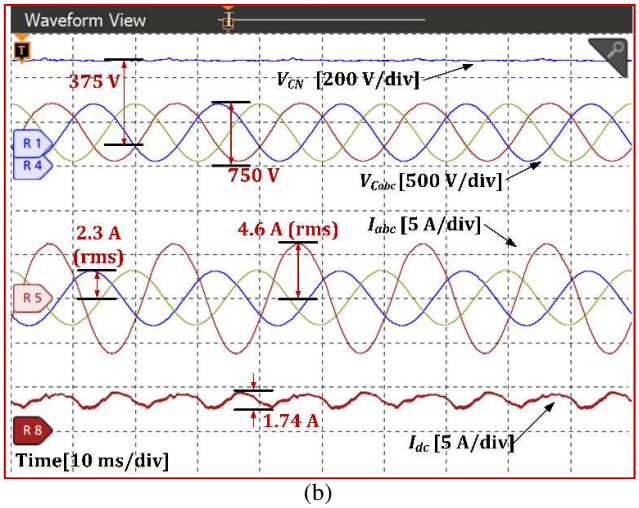
1) Steady-state performance without decoupling controller.

To verify the inverter performance in steady-state under unbalanced conditions, the loads were set as $R_{a,imb} = 52\ \Omega$ and $R_b = R_c = 105\ \Omega$. An imbalance ratio $\delta = 0.5$ was adopted. Experimental results are shown in Fig. 21.

Fig. 21(a) shows a balanced three-phase rms output voltage of 230 V facilitated by the closed loop control scheme. The output load currents exhibit imbalance due to difference in loading for phase A compared to phases B and C. Since the decoupling controller is not in operation, a second-order ripple occurs on the dc bus. This has a magnitude of 1.74 A. As shown in Fig. 21(b), there is no second-order component being stored in the filter and neutral leg capacitors.



(a)



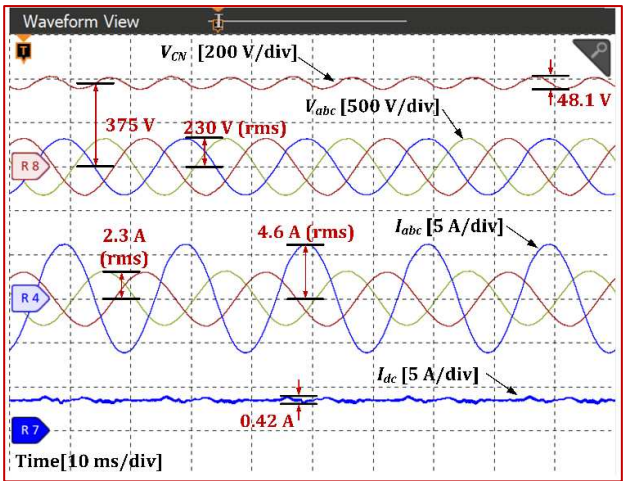
(b)

Fig. 21. Experimental steady-state performance of the four-leg buck inverter under unbalanced conditions without decoupling controller. (a) Three-phase output voltages. (b) Filter capacitor voltages.

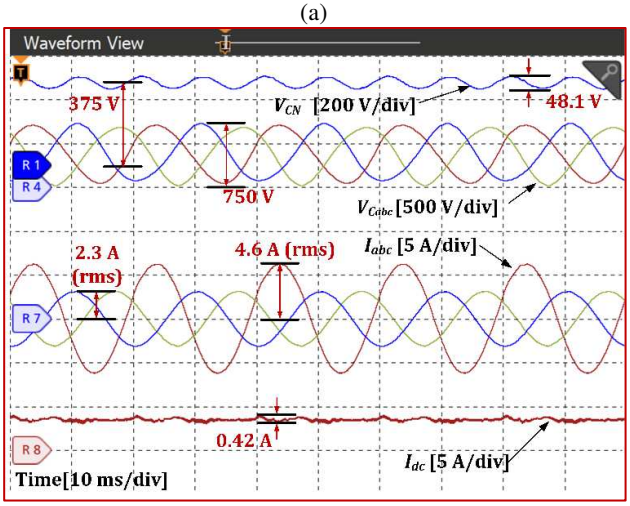
2) Steady-state performance with decoupling controller.

The same experiment was repeated with the decoupling controller being activated, with results shown in Fig. 22. In this case, the three-phase voltages remain balanced despite the unbalanced load conditions in phase A. The dc bus current i_{dc} reflects the effect of the decoupling controller, showing a significant reduction in the magnitude of the second-order ripple by ~75%, decreasing from 1.74 A to 0.42 A. However, the dc bus current still exhibits residual ripple. This could be attributed to the presence of non-ideal components of the experimental platform, which may incorporate noise into the dc current trace [46]. (Although the residual ripple could be further reduced by fine-tuning parameters of the control scheme, such a design exercise falls outside the scope of this work.) The phase filters and neutral leg capacitor voltages also show the effect of the decoupling controller as they contain second-order components, which is consistent with (5) and (6). The magnitude of the second-order voltage ripple in the neutral leg capacitor is 48 V—consistent when using (12).

The second-order ripple reduction allows both the dc bus current i_{dc} and voltage V_{dc} to be free from second-order ripple. This in turn prevents any adverse effects on the dc voltage source (e.g. an EV battery).



(a)



(b)

Fig. 22. Experimental steady-state performance of the four-leg buck inverter under unbalanced conditions with decoupling controller. (a) Three-phase output voltages. (b) Filter capacitor voltages.

Fig. 23 shows the fast Fourier transform (FFT) for the current on the dc bus to compare the harmonic components with and without a decoupling controller. The second-order harmonics are substantially reduced by around 95% when the decoupling controller is in operation.

While the decoupling controller is operating, the second-order harmonics are reduced by the harmonic compensator cascaded with the current loop control for each phase leg. Fig. 24 shows the FFT of the measured current of phase A. A THD of 1.21% is observed when the decoupling controller is active and 0.78% without it. The increase in magnitude of the second-order harmonic on the ac side when the decoupling controller is used occurs as a decoupling current is present in the phase legs to reduce the second-order ripple on the dc side.

Fig. 25 shows the harmonic spectrum of the neutral capacitor. A second-order component of ~25V is exhibited when the decoupling controller is active. Similarly in Fig. 26, a second-order component of around 25 V is stored in the filter capacitor of phase A.

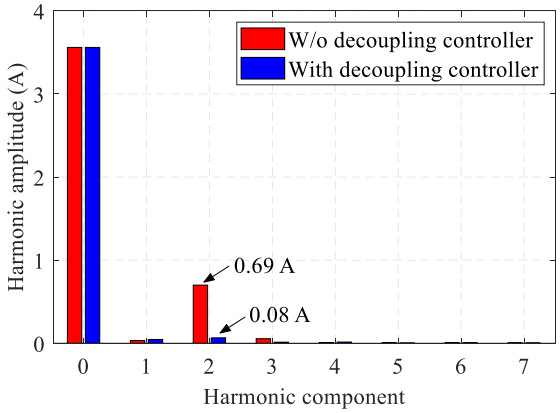


Fig. 23. FFT of the dc bus current.

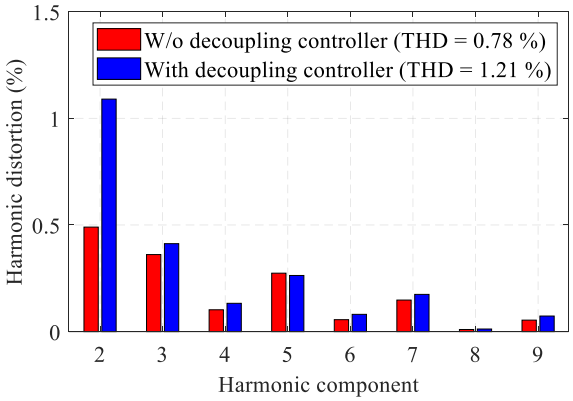


Fig. 24. FFT of the load voltage for phase A.

3) Step change in load with no decoupling controller

For this experiment, the phases are initially under balanced load conditions ($R_a = R_b = R_c = 105\ \Omega$) and the decoupling controller is inactive. A step in the load of phase A leads to $R_{a,imb} = 52\ \Omega$, while the loads in phases B and C remain the same. Results are provided in Fig. 27, which shows the balanced output voltages before and after the step load occurs. At this point, the rms current of phase A increases from 2.3 A to 4.6 A. The current on the dc bus of the inverter exhibits a second-order current ripple with an amplitude of ~1.7 A. This behavior is similar to that obtained in simulation (see Fig. 15).

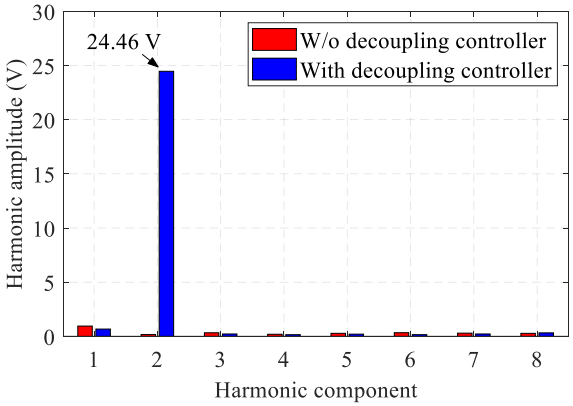


Fig. 25. FFT of the neutral capacitor voltage.

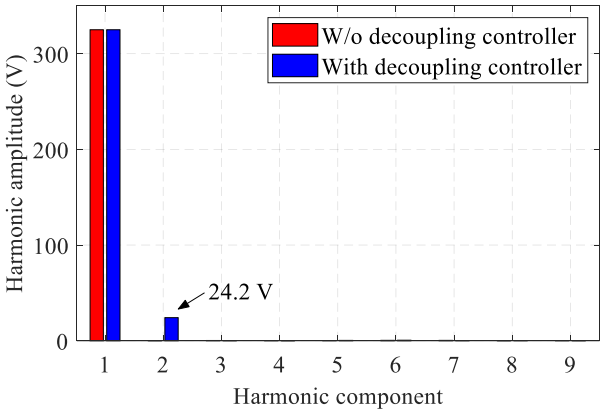


Fig. 26. FFT of the filter capacitor voltage of phase A.

3) Step change in load with no decoupling controller

For this experiment, the phases are initially under balanced load conditions ($R_a = R_b = R_c = 105\ \Omega$) and the decoupling controller is inactive. A step in the load of phase A leads to $R_{a,imb} = 52\ \Omega$, while the loads in phases B and C remain the same. Results are provided in Fig. 27, which shows the balanced output voltages before and after the step load occurs. At this point, the rms current of phase A increases from 2.3 A to 4.6 A. The current on the dc bus of the inverter exhibits a second-order current ripple with an amplitude of ~1.7 A. This behavior is similar to that obtained in simulation (see Fig. 15).

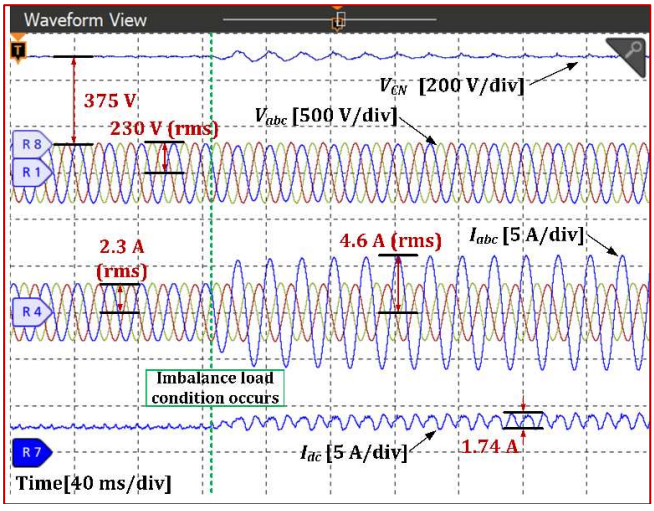


Fig. 27. Experimental transient performance of the four-leg buck inverter without decoupling controller.

4) Step change in load with decoupling controller

The previous experiment was repeated with the decoupling controller under operation, with results shown in Fig. 28. As observed, the output voltages are balanced when the step load occurs. There is an increment though in the rms current from 2.3 A to 4.6 A in phase *A*. However, a reduction in the second-order ripple current is observed. Moreover, a second-order voltage ripple is exhibited in the capacitor of the neutral leg capacitor with a magnitude of ~48 V. The behavior is similar as that exhibited in simulation (see Fig. 16).

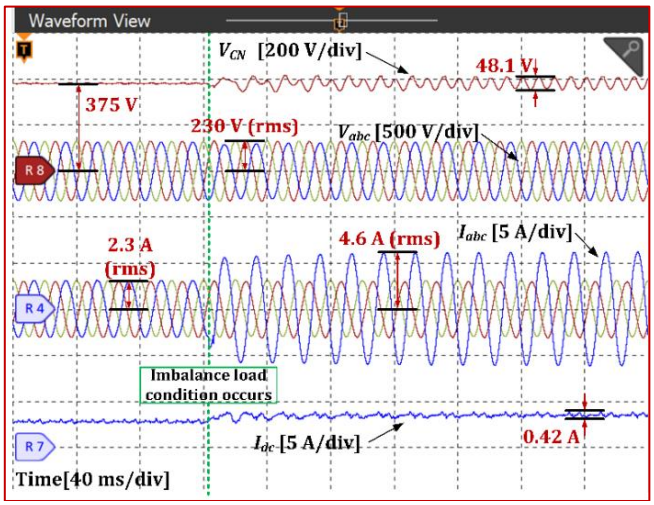


Fig. 28. Experimental transient performance of the four-leg buck inverter with decoupling controller.

5) Efficiency

The efficiency of the four-leg buck inverter is here compared with the conventional and the improved neutral leg topologies. To this end, experimental measurements were carried out using a Yokogawa WE1806 power analyzer. The inverter parameters are as in Table II.

Fig. 29 shows results under balanced conditions for different values of P_o. A similar efficiency is seen for all topologies due to the absence of second-order ripple on the dc bus.

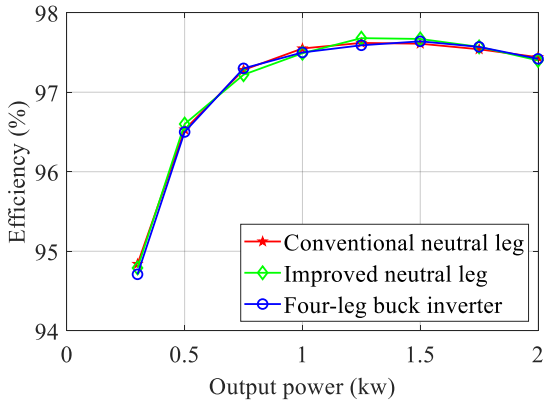


Fig. 29. Efficiency comparison under balanced conditions.

Fig. 30 shows the efficiency afforded by the topologies upon an imbalance ratio $\delta = 0.5$. Compared to balanced conditions (see Fig. 29), efficiency drops for all power outputs. A similar efficiency is exhibited by the four-leg buck inverter and the topology with an improved neutral leg. The reduced efficiency with respect to the conventional neutral leg topology arises from the injection of decoupling current, which causes current stress and power losses in the neutral legs, inductors, and switches. However, the four-leg buck inverter has an increase in efficiency of 0.2% over the improved neutral leg at 2 kW.

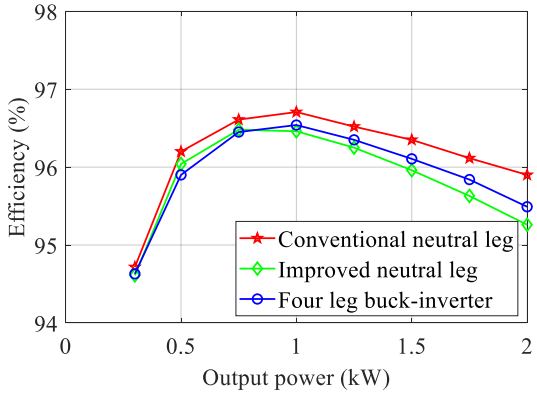


Fig. 30. Efficiency comparison under unbalanced conditions.

VI. Conclusions

A novel four-wire inverter configuration was presented in this paper. The topology has the potential to be employed for EV chargers and battery-based energy storage systems to supply energy to an isolated grid for domestic use. The inverter has advantages over existing configurations as the phase and neutral legs can be independently controlled to provide a neutral current. It is also possible to mitigate the second-order ripple on the dc bus of the inverter when operating under unbalanced conditions by means of a suitable control strategy. This also avoids a negative impact on the dc source such as an EV battery.

The presented topology reduces the capacitance requirement on the neutral leg by around eight and four times compared to the conventional and improved neutral leg four-wire topologies. This attribute reflects in an increased power density and thus cost reduction for output powers above 5 kW as the topology does not require the incorporation of additional active and passive components.

The topology was co-simulated using MATLAB/Simulink and PLECS. Simulation results were experimentally verified using a 2 kW prototype enabled by an Imperix platform. Experimental and simulation results exhibit a good agreement, where it is evident that the decoupling control loop ensures balanced three-phase voltages under the presence of load imbalance.

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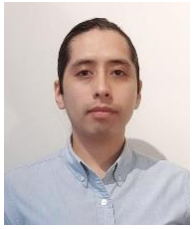

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