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The design of a hybrid DC/DC converter for LED lighting system using a single switch

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ABSTRACT

A novel hybrid Luo-Cuk converter designed for LED lighting systems combines elements from both Luo and Cuk topologies. By integrating the input branch of both topologies, the converter, employing a single switch, can generate two distinct types of outputs simultaneously. One output follows a Luo-type, while the other adopts a Cuk-type . Through a series connection of the outputs from Luo and Cuk topologies, the voltage gain of the converter has been notably enhanced. The converter's output can be effectively regulated using a single controller. To validate the consistency between the topology's performance and theoretical analysis, simulation and prototype results have been provided.

1. Introduction

Light-emitting diodes (LEDs) are rapidly replacing traditional light sources across various applications due to their exceptional longevity, compact size, high light efficiency per watt, eco-friendliness, and accurate colour rendering (Patakamoori et al., 2022). Numerous academic inquiries have focused on enhancing LED lamp performance, extending their lifespan, and refining controllability to boost overall efficiency. A significant area of interest within power electronics research is LED driving power generation, which plays a vital role in propelling advancements in LED applications (Fathabadi, 2016; Aganza-Torres et al., 2014; Araújo et al., 2010; Ismail et al., 2008). This has become a central focus for research endeavours. Presently, individual LED lights have limitations in providing high power outputs and significant brightness levels, posing challenges in meeting specific application requirements (Krames et al., 2007). To address this challenge, multiple LEDs are configured and grouped together to attain a wider range, enhanced luminosity, dynamic visual effects, and adaptable colour shifting as required for various applications. LED drivers can operate in either parallel or series modes, with the series mode demanding higher voltage generation and the parallel mode necessitating increased current delivery. The diverse LED connection configurations can lead to a mismatch between the load and the power supplied due to these different connection types. Leveraging its high conversion efficiency, swift dynamic response, array of topologies, and versatile feedback control methods, switching converter structures find extensive utility in powering LEDs, ensuring high efficiency, excellent performance, and reliability.

Boost converters, often utilized to elevate output voltage in response to a given input, employ a straightforward step-up mechanism with a heightened duty cycle (Haroun et al., 2014; Al-Saffar and Ismail, 2015; El Aroudi et al., 2013; Wijeratne and Moschopoulos, 2012). Nevertheless, these boost converters are hindered by parasitic elements within inductors and power semiconductors, constraining their ability to achieve substantial voltage gains. Additionally, power semiconductors contend with high voltage stress, potentially impacting the functionality of MOSFETs and IGBTs. Diodes also contribute to switching losses due to their relatively high reverse recovery current, especially under elevated current and voltage conditions. To mitigate this challenge, a flyback converter can be employed as a solution, incorporating a set-up transformer to address the issue (Fathabadi, 2016; Aganza-Torres et al., 2014; Cruz Martins and Demonti, 2002). However, the utilization of step-up transformers presents several challenges, including low operating frequencies, issues related to leakage energy, and switching transients. In response to these challenges, the adoption of high-voltage converters with significant voltage amplification has been advocated (Chen et al., 2018; Hsieh et al., 2013). Pioneering topologies employing multiple stages of multiplication have been put forth to augment voltage gain and alleviate voltage stress on power semiconductors (Araújo et al., 2010; Ismail et al., 2008; Haroun et al., 2014; Prudente et al., 2008). Within the domain of DC-to-DC power converters, several investigations (Bharatiraja et al., 2017; Banaei et al., 2014; Buck and Dc, 2017; Lin and

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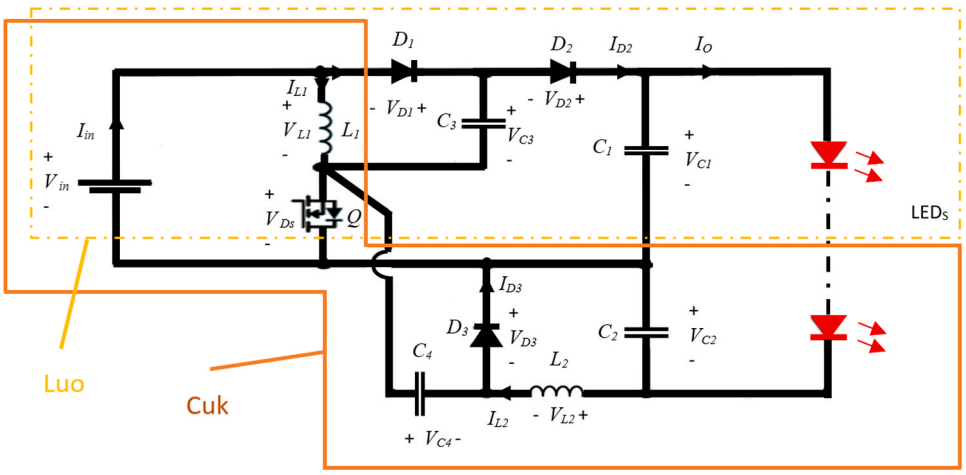

Fig. 1. Topology of the proposed combined-type converter.

Nian, 2014a; Zhang et al., 2018; Maroti et al., 2018) have explored the utilization of single switches to attain elevated voltage gain without requiring a high-duty cycle. Additionally, quadratic converters have been developed to enable substantial voltage gains. These converters, as detailed in (Khooban et al., 2020; Farsizadeh et al., 2020), aim to minimize instability effects within a microgrid. The controller coefficients for these systems were optimized using a specific optimization algorithm (Farsizadeh et al., 2020). Comparatively, quadratic converters like the quadratic DC–DC buck–boost converter are less efficient than traditional options like the boost converter. Additionally, the main semiconductor in these converters experiences relatively high voltage stress (Al-Saffar and Ismail, 2015). In addressing the need for versatile voltage conversions, a single-switch topology has been employed to design a quadratic DC–DC buck–boost converter, as discussed in (Zhang et al., 2018).

In the context of PV-based grid systems, the recommendation is to employ a high step-up single switch converter (Saravanan and Babu, 2017). Another viable option is the utilization of Z-source converters, providing buck-boost capabilities (El Aroudi et al., 2013). However, it's important to note that Z-source converters necessitate several passive elements such as two inductors and two capacitors, along with semiconductors possessing relatively high voltage ratings and susceptibility to switching transients. These converters aim to enhance voltage gain and reduce voltage stress across power semiconductors (de and Baptista, 2013). Additionally, an integrated buck-boost SRC with high gain has been introduced to control multi-LED loads (Kolla et al., 2022). In the domain of power factor correction (PFC) converters, an enhanced buck-boost PFC converter with a single-stage dual-output configuration has been suggested (Liu et al., 2015). On a similar note, certain topologies outlined in (Shen et al., 2011),and (Wu et al., 2019)have showcased notable step-down conversion gains through the use of interconnected inductors. However, these topologies face a notable drawback, encountering considerable switching spikes across the switch due to leakage energy present in the interconnected inductor. Authors in (D. L. E. D. Driver, 2017), have proposed an effective method to recycle this leakage energy, mitigating the switching spikes. An alternate strategy entails utilizing a soft-switched full-bridge converter in conjunction with a parallel inductor, as outlined in (Tang et al.,2019). Utilizing a secondary side transformer in this setup offers various advantages, including reduced duty cycle loss and improved efficiency under light loads. However, it does increase the number of components per lamp, leading to higher system cost and size. Cascading two converters in series without redundant switches or controllers can yield multiple topologies with distinct advantages (Wijeratne and Moschopoulos, 2012; Kadri et al., 2010). For example, a single-switch converter with low voltage drops was introduced in (Lin and Nian, 2014b). However, a drawback is that the primary power switch experiences voltage stress equal to the converter output voltage, leading to elevated conduction losses (Lin and Nian, 2014b). In (Maroti et al., 2018), and (Oluwafemi et al., 2017) a single switch Cuk topology was employed to generate additional voltage using an extra capacitor and inductor. Nonetheless, this converter faces increased switching losses when diodes operate with higher voltages and currents. In comparison, the cascade boost converter distinguishes itself by providing higher gain across a broader range of voltage gain. Nevertheless, the main switch in this topology is subject to higher voltage drops (Chen, . et al., 2011). In various research works, different topologies for single-switch boost converters have been extensively investigated, emphasizing the importance of minimizing magnetic components, reducing weight and size, lowering conduction losses, and optimizing the cost-effectiveness of inductors. The objective is to ensure that the voltage stress on the switches remains nearly proportional to the voltage of their respective outputs. While some approaches involve integrating a classic DC-to-DC converter directly, others advocate for cascading classical converters to enhance boosting capabilities, ultimately reducing the size and cost of the converter circuit. In this context, the proposed topology, leveraging both Luo and Cuk converters, stands out by requiring only a single semiconductor power switch. Notably, it offers increased voltage static gain and minimized voltage stress across power switches and diodes compared to traditional boost topologies. Moreover, this converter can efficiently handle multiple output types and series outputs. Achieving adjustable output branches for driving varying numbers and types of LEDs can be realistically implemented using just one controller. Additionally, this work places a significant emphasis on the power converter's design aspects, which have been substantiated through rigorous simulation and experimental work.

The paper's organization is as following: Section 2 delves into the structure of the innovative combined Cuk- Luo topology. A detailed Explanation of the operational principle is outlined in Section 3. Equations in State-Space Representation are provided in Section 4, followed by analysis of Steady-State Performance in Section 5. Sections 6 and 7 encompass simulations, experimental results, and comparative analyses with related topologies. The final section, Section 8, delivers the concluding remarks.

2. The structure of the innovative combined Cuk-Luo topology

The schematic of the topology is displayed in Fig. 1, showcasing the integration of both the Cuk and Luo converters. Common elements include the input inductor, power switches, and input source. Every element is linked in parallel, except for the switch Q and inductor L_1 at the input. Significantly, it's important to highlight that the polarity of

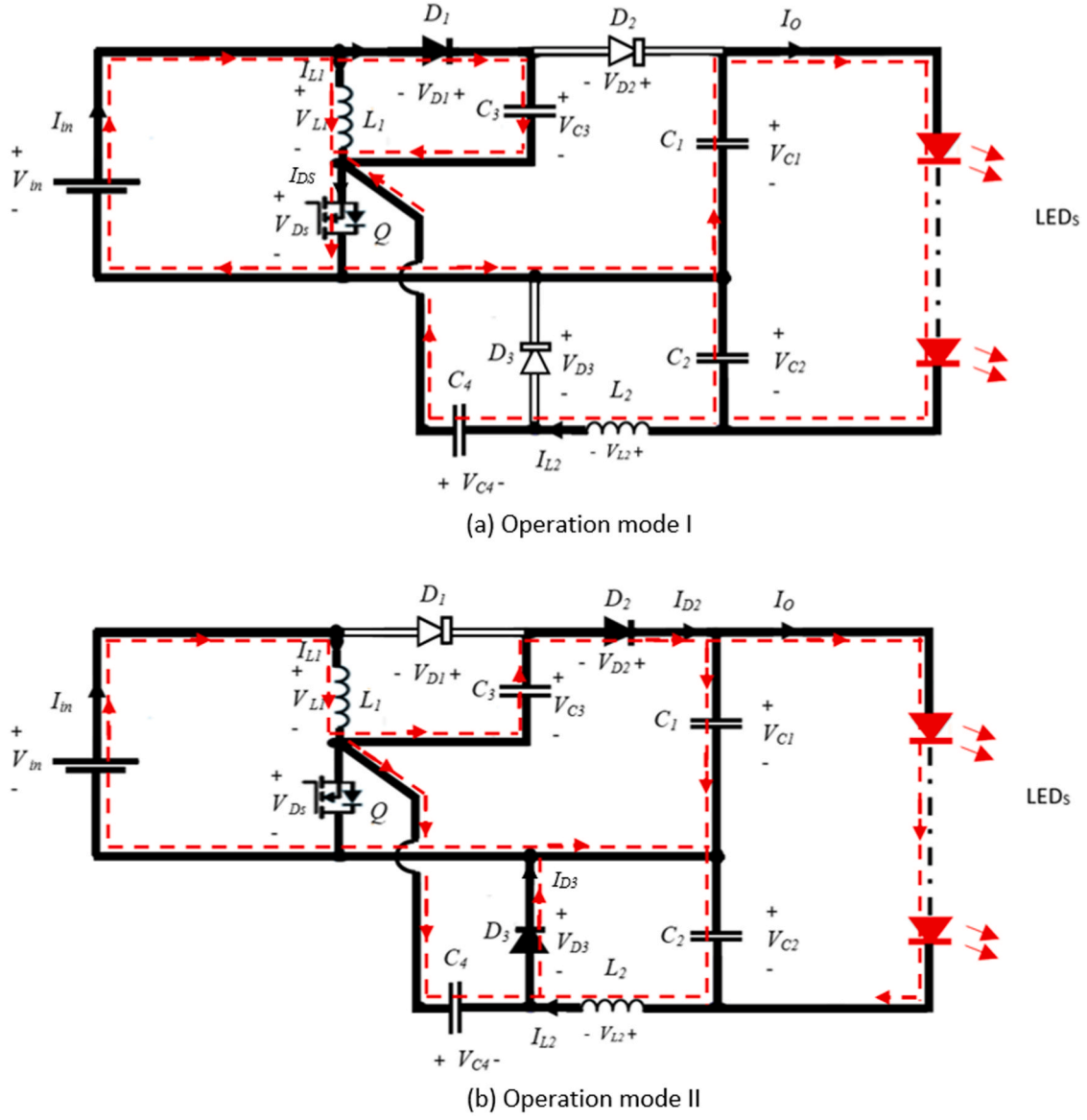

Fig. 2. Equivalent-circuits of the switching-modes (a) Operation mode I. (b) Operation mode II.

the voltage at the Cuk converter's output is opposite to that at its input. The output is coupled to a dual-output termination connected to LED combinations LED1s and LED2s. Through a fusion of the advantageous features of both Luo and Cuk converters, this design achieves a reduction in the count of switches and inductors while amplifying the voltage gain. Moreover, it alleviates the voltage stress on the switch and diminishes input ripple current.

3. Explanation of the operational principle

The novel combined Luo-Cuk converter offers the flexibility to generate two distinct types of outputs and a serial output comprising both. To understand its operation, let's consider the scenario of a serial output with the assumption of ideal components and continuous inductor current. During one switching cycle, the combined Luo-Cuk converter undergoes two distinct operating modes, which correspond to the circuit depicted in Fig. 2(a) and (b). Fig. 3 illustrates the key waveforms during steady-state operation. The converter operating modes is elucidated as follows:

During operating mode [I]: when the switch Q and D_1 are activated (as illustrated in Fig. 2(a), inductors L_1 and L_2 receive energy. Concurrently, capacitor C_4 undergoes a discharge cycle. Diodes D_2 and D_3 are blocked by negative voltages applied to V_{C1} and V_{C4}, respectively. The voltage across the inductors can be described as follows:

$$V_{L_1} = L_1 \frac{di_{L1}}{dt} = V_{in} \tag{1}$$

$$V_{L_2} = L_2 \frac{di_{L2}}{dt} = -V_{C_2} + V_{C_4} \tag{2}$$

At $t = T_{on} = DT_s$, the current i_{L1} reaches its peak value, denoted as i_{L1}max. The rise in current i_{L1} during a switch's conduction period can be described as follows:

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} DT_s \tag{3}$$

Simultaneously, i_{L2} also reaches its maximum value, denoted as i_{L2} max. The increase in the maximum value Δi_{L2} is described as follows:

$$\Delta i_{L_2} = \frac{V_{C_2} + V_{C_4}}{L_2} DT_s \tag{4}$$

At present, LEDs are powered by capacitors, and the current flow through switch Q is as follows:

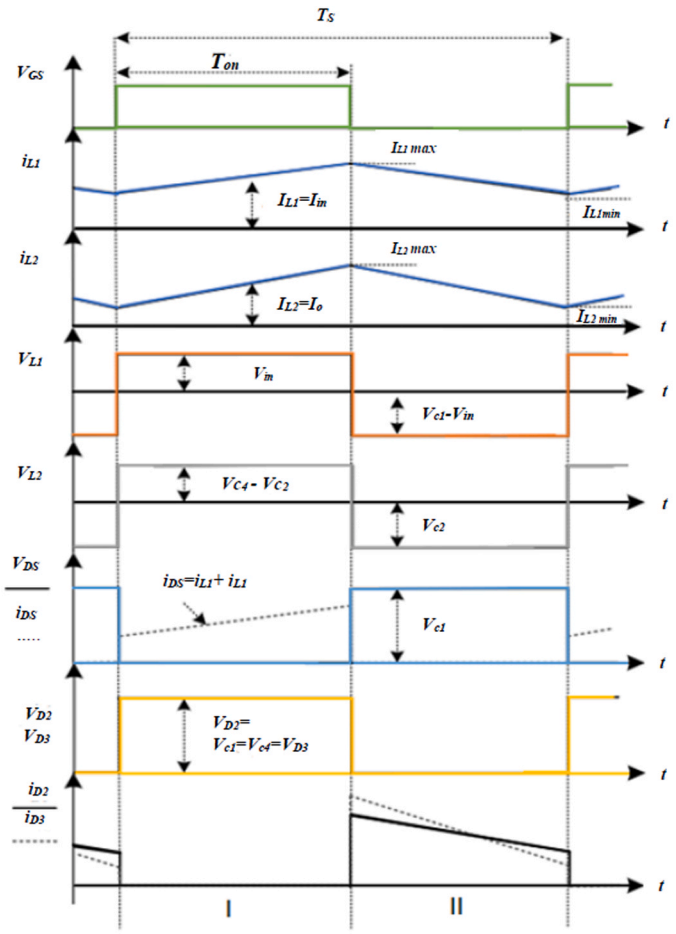

Fig. 3. Key waveforms based on complementary control.

$$iD_s = iL_1 + IL_2 \tag{5}$$

To ensure the validity of state variables, it consider the series resistance(r) of capacitor C_4. The equations describing this mode, in line with circuit theory, are illustrate in Fig. 2(a):

$$\begin{cases} L_1 \dfrac{diL_1}{dt} = V_{in} \\ L_2 \dfrac{diL_2}{dt} = -V_{C_2} + V_{C_4} \\ C_1 \dfrac{divc_1}{dt} = -\dfrac{V_{C_1} + V_{C_2}}{R} \\ C_2 \dfrac{divc_2}{dt} = iL_2 - \dfrac{V_{C_1} + V_{C_2}}{R} \\ C_3 \dfrac{divc_3}{dt} = \dfrac{V_{in}}{R} - iL_1 - \dfrac{V_{C_3}}{R} \\ C_4 \dfrac{divc_4}{dt} = iL_2 \end{cases} \tag{6}$$

During operating mode [II]: In the scenario depicted in Fig. 2(b), when switch Q is deactivated, diode D_1 undergoes reverse biasing, while diodes D_2 and D_3 transition to a forward bias state. During this period, both the power source and inductor L_1 discharge energy concurrently. Diode D_2 provides power to the LEDs and charges capacitor C_1. Meanwhile, capacitor C_4 is replenished through diode D_3, and capacitor C_2 interacts with inductor L_2. The current in inductors L_1 and L_2 experiences a linear decline, and the voltage across these inductors can be calculated using the following expressions:

$$V_{L_1} = L_1 \frac{di_{L1}}{dt} = -V_{C_1} + V_{in} + V_{C_3} = -V_{C_4} + V_{in} + V_{C_3} \tag{7}$$

$$V_{L_2} = L_2 \frac{di_{L2}}{dt} = -V_{C_2} \tag{8}$$

This implies that the current passing through diode D_3 at this moment can be expressed as follows:

$$iD_3 = iC_4 + iL_2 \tag{9}$$

The decrease in current within inductor L_1 during the switch Q's off period is as follows:

$$\Delta i_{L_1} = \frac{V_{c_4} + V_{in} + V_{C_3}}{L_1}(1 - D)T_s \tag{10}$$

The current reduction occurs due to energy release from the inductor, and the rate of current decrese during this phase is as follows:

$$\Delta i_{L_2} = \frac{V_{c_2}}{L_2}(1 - D)T_s \tag{11}$$

For D values greater than 0.5, both the Luo and Cuk topologies are in boost mode, while for D values less than 0.5, the Luo topology is in boost mode, and the Cuk topology is in step-down mode. This mode can also be described using circuit theory equations as follows:

$$\begin{cases} L_1 \dfrac{diL_1}{dt} = -V_{C_1} + V_{in} + V_{C_3} \\ L_2 \dfrac{diL_2}{dt} = -V_{C_2} \\ C_1 \dfrac{divc_1}{dt} = iL_1 - \dfrac{V_{C_1} + V_{C_2}}{R} \\ C_2 \dfrac{divc_2}{dt} = iL_2 - \dfrac{V_{C_1} + V_{C_2}}{R} \\ C_3 \dfrac{divc_3}{dt} = -iL_1 \\ C_4 \dfrac{divc_4}{dt} = iL_1 \end{cases} \tag{12}$$

4. Equations in state-space representation

A simple average model can be obtained for this open-loop step-up converter by using the average method and Eq. (6) and (12). In (13), X, U, and Y are state variable vectors, control variable vector, and output vector, respectively. A, B, C, and D are state matrix, input matrix, output matrix, and feed-forward matrix, respectively, which are given in the following Eq. (13).

$$\begin{aligned} Y &= AX + BU \\ Y &= CX + DU \end{aligned} \tag{13}$$

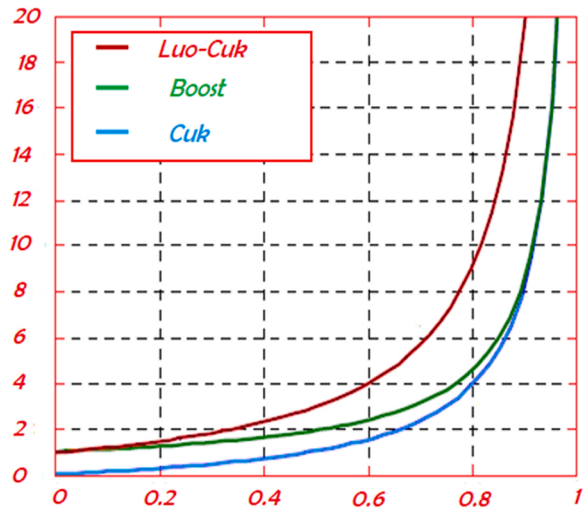

Fig. 4. The relationship-between the duty-cycle and voltage-gain of the combined Luo-Cuk, Boost and Cuk converters.

Table 1
An overview of the prototype's parameters.

Parameter	Value
V_{in}	7–10 V
V_o	48 V
L_1	300 μH
L_2	300 μH
C_1, C_2, C_3, C_4	C_1 = 400 μF, C_2 = 470 μF, C_3 = 100 μF, C_4= 100 μF
Output Power	*10 w*
f_s	25 kHz
Microcontroller	TMS320F28335

$$\begin{bmatrix} \frac{d\hat{i}L_1}{dt} \\ \frac{d\hat{i}L_2}{dt} \\ \frac{d\hat{v}c_1}{dt} \\ \frac{d\hat{v}c_2}{dt} \\ \frac{d\hat{v}c_3}{dt} \\ \frac{d\hat{v}c_4}{dt} \end{bmatrix} \begin{bmatrix} 0 & 0 & -\frac{1-D}{L_1} & 0 & -\frac{1-D}{L_1} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{D}{L_2} \\ \frac{1-D}{C_1} & 0 & \frac{1}{C_1R} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_3} & 0 & 0 & 0 & \frac{D}{C_3R} & 0 \\ \frac{1-D}{C_4} & \frac{D}{C_4} & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}L_1 \\ \hat{i}L_2 \\ \hat{v}c_1 \\ \hat{v}c_2 \\ \hat{v}c_3 \\ \hat{v}c_4 \end{bmatrix} \tag{14}$$

$$+ \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_{in} + \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_2} \\ \frac{-1}{C_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_3R} & 0 \\ \frac{-1}{C_4} & \frac{1}{C_4} & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} iL_1 \\ iL_2 \\ vc_1 \\ vc_2 \\ vc_3 \\ vc_3 \end{bmatrix}$$

$$C = [0 \quad 0 \quad 1 \quad 0 \quad 0 \quad 0]$$

$$D = 0$$

5. Analysis of steady-state performance

5.1. Voltage gain in the proposed structure

The equation below is obtained through the application of the volt-second balance principle to inductor L_1:

$$V_{in}DT_s = (V_{in} - V_{c_1})(1-D)T_s \tag{15}$$

$$V_{in}DT_s = (V_{in} - V_{c_4})(1-D)T_s \tag{16}$$

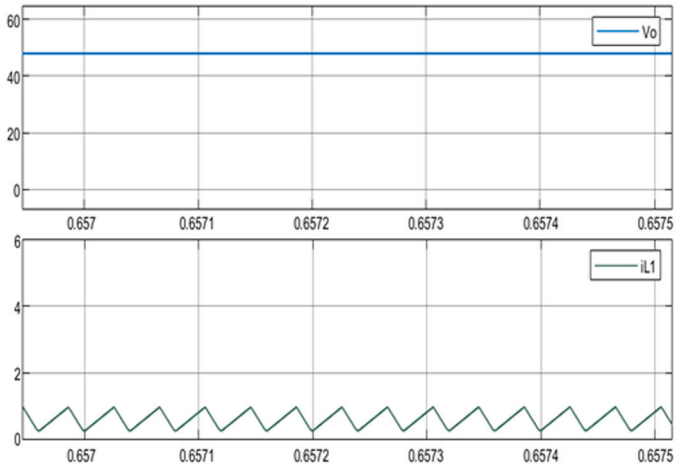

Fig. 6. Results of simulation of output voltage and the input current I_{L1}.

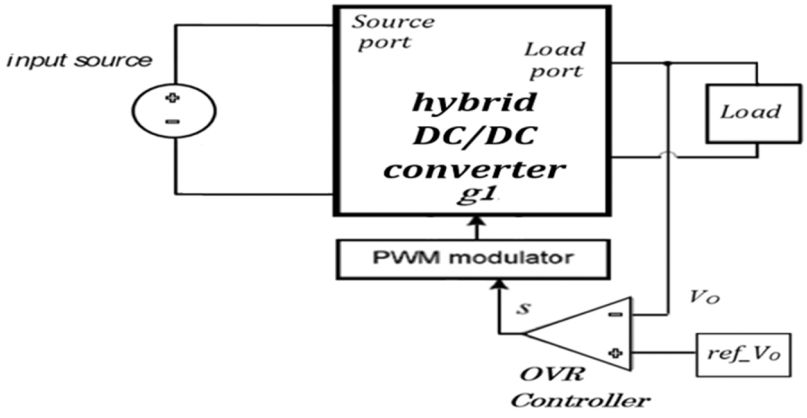

Fig. 5. Control schematic.

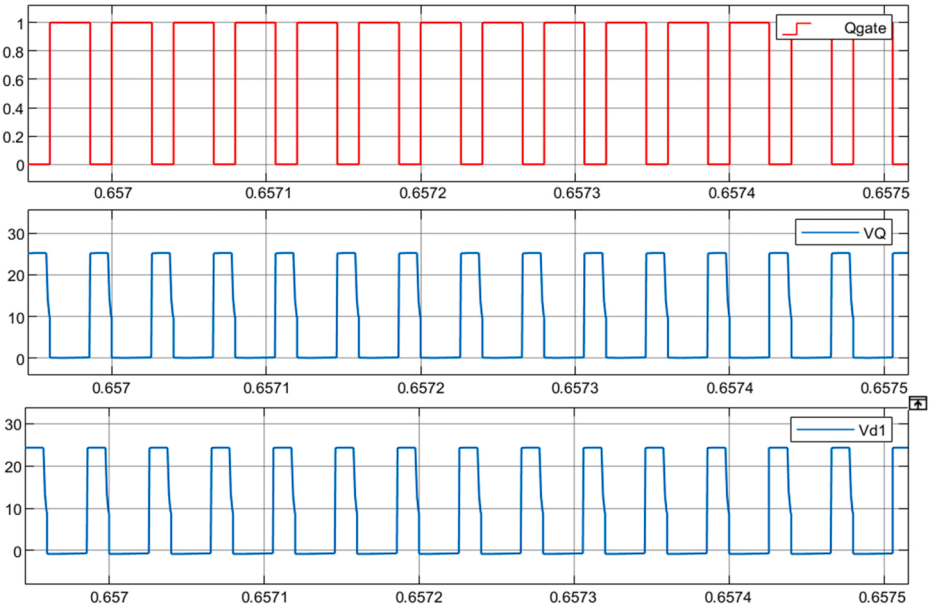

Fig. 7. The gate drive signal and voltage across the power switch Q and voltage across diode D_1.

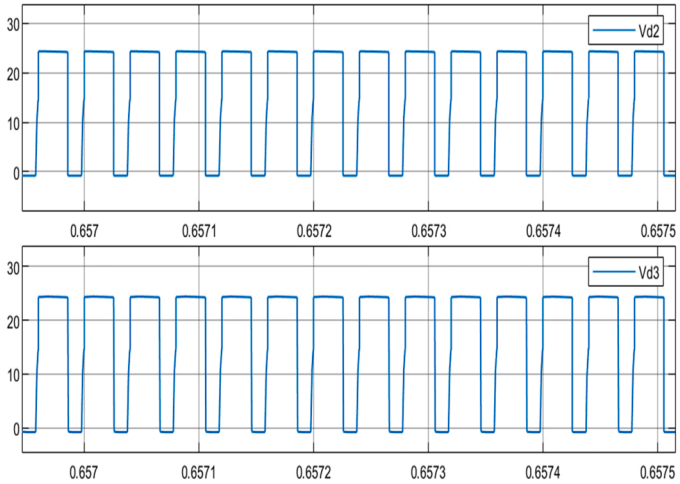

Fig. 8. Simulation results for voltage across two diodes, D_2 and D_3.

Using Eqs. (15) and (16), it can calculate the voltage across the capacitor C_1 and C_4 as follows:

$$V_{c_1} = V_{c_4} = \frac{V_{in}}{1-D} \tag{17}$$

Applying the Volt-sec-balance principle for inductor, it obtains the following equation:

$$(V_{C_4} - V_{C_2})DT_s = V_{c_2}(1-D)T_s \tag{18}$$

Eq. (18) allows for the calculation of the capacitor voltage:

$$V_{c_2} = DV_{c_4}\frac{D}{1-D}V_{in} \tag{19}$$

$$V_o = V_{c_1} + V_{c_2} \tag{20}$$

By combining Eqs. (17),(19), and (20), the steady-state voltage gain of the converetr can be calculated using the following formula:

$$M = \frac{V_o}{V_{in}} = \frac{I_o}{I_{in}} = \frac{1+D}{1-D} \tag{21}$$

The input inductor current of the converter is obtained by setting the input power equal to the output power, expressed as follows:

$$V_{in} \quad I_{in} = V_o \quad I_o \rightarrow \quad i_{L1} = \frac{1+D}{1-D} \quad I_o \tag{22}$$

The mean value of i_{L2} is determined by the following equation.

$$i_{L2} = \quad I_o \tag{23}$$

Fig. 4 presents the graphical representation depicting the relationship between duty cycle and voltage gain for the Combined Luo-Cuk, Boost, and Cuk converters. It can be observed that the Combined Luo-Cuk converter achieves a higher voltage gain compared to both Cuk and Boost converters. Moreover, this characteristic makes it well-suited for lighting applications given its substantial gain.

5.2. Stress on device voltage and current

The voltage experienced by switch Q and diodes D_2 and D_3 during their off state is:

$$V_{Ds} = \frac{V_{in}}{1-D} = \frac{V_o}{1+D} \tag{24}$$

The voltage experienced by diode D_1 when it is turned off is:

$$V_{D1} = \quad V_{in} \tag{25}$$

The current in the power switch Q and diodes D_1, D_2, and D_3 can be represented as follows:

$$I_{Ds} = \frac{2I_o}{1-D} \tag{26}$$

$$I_{D1} = I_{in} \tag{27}$$

$$I_{D2} = \frac{I_o}{1-D} \tag{28}$$

$$I_{D3} = \frac{I_o}{1-D} \tag{29}$$

5.3. Considerations for design

5.3.1. Design of inductor

The average value of the inductors and circuit under analysis is computed, ensuring a certain level of variation. This involves deter-

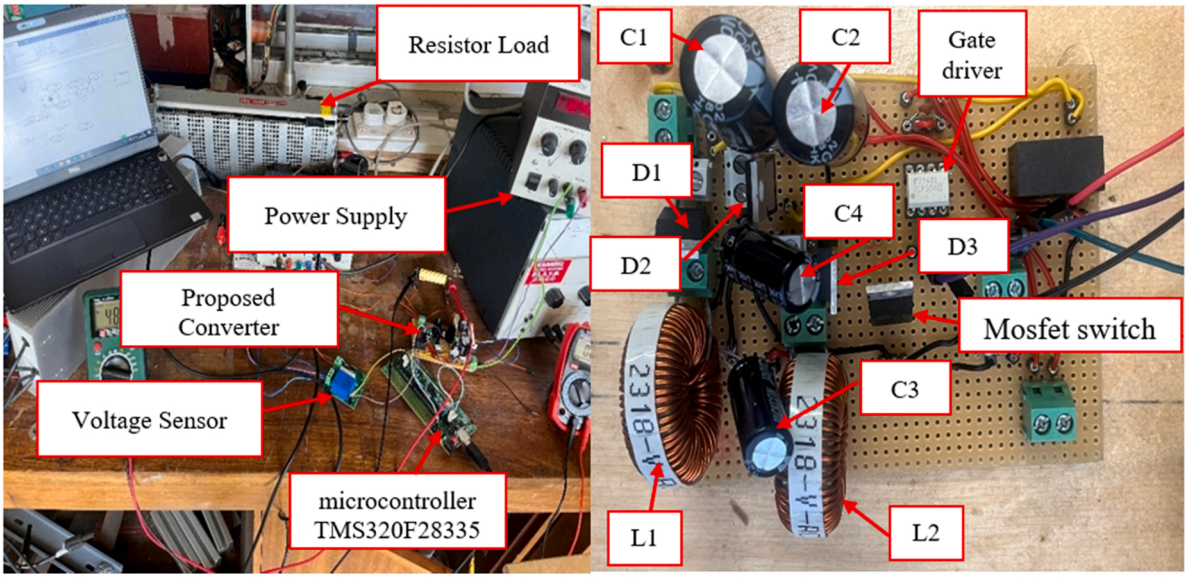

Fig. 9. DC/DC hybrid converter prototype, (a)entire setup, (b) proposed converter.

mining the inductance value based on the measured instantaneous voltage, V_L, over a defined time period Δt_L. Specifically, for inductor L_1, the voltage V_{L1} is calculated using the following approach:

$$V_{L_1} = \begin{cases} V_{in} & nT < t < nT + \delta T \\ V_{in} - Vc_1, & nT + \delta T < t < (n+1)T \end{cases} \tag{30}$$

During the initial time interval, Δt_L is equal to δT, resulting in the following:

$$L_1 = \frac{V_{in}\delta T}{\Delta i L_1} \tag{31}$$

The voltage V_{L2} for the coil L_2 can be determined using the following expression:

$$V_{L_2} = \begin{cases} Vc_1 - Vc_2 & nT < t < nT + \delta T \\ -Vc_2, & nT + \delta T < t < (n+1)T \end{cases} \tag{32}$$

Utilizing the second time interval, where $\Delta t_L = (1-\delta)T$, The voltage across coil L_2, denoted as V_{L2}, can be computed using the following approach:

$$L_2 = \frac{Vc_2(1-\delta)T}{\Delta i L_2} \tag{33}$$

5.3.2. Design of capacitors

As a part of the analysis, calculations are made for the values of capacitors C_1, C_2, and C_4 in the circuit. This is done to maintain a specific deviation ΔV_c from the average value V_C. The voltage $vc(t)$across a capacitor, in general, follows the differential Eq. (34).

$$i_c(t) = C\frac{dV_C}{dt} \tag{34}$$

The expression in Eq. (35) can be obtained using a similar approach to that employed for calculating the inductors.

$$\frac{\Delta vc}{\Delta t_c} = \frac{i_c}{C} \tag{35}$$

This approach allows for the determination of the capacitor's value by evaluating the instantaneous current in capacitor i_c over a specific time interval Δt_c. As expressed in the following equation, the current in capacitor C_1 is defined as:

$$ic_1 = \begin{cases} -I_o, & nT < t < nT + \delta T \\ I_o\dfrac{\delta}{1-\delta}, & nT + \delta T < t < (n+1)T \end{cases} \tag{36}$$

The initial time period produces the subsequent results:

$$C_1 = \frac{I_o \delta T}{\Delta vc_1} \tag{37}$$

The current flowing through capacitor C_4, denoted as I_{C4}, is determined using the following equation:

$$ic_4 = \begin{cases} -I_o, & nT < t < nT + \delta T \\ I_o\dfrac{\delta}{1-\delta}, & nT + \delta T < t < (n+1)T \end{cases} \tag{38}$$

During the initial time interval, the following results are obtained:

$$C_4 = \frac{I_o \delta T}{\Delta vc_4} \tag{39}$$

The previous approximation cannot be utilized in this case since the current in capacitor C_2 is not consistent during the switching process. When the semiconductor is conducting, the charge supplied to capacitor ΔQ is equivalent to the area of a triangle with a height of $\frac{\Delta iL_2}{2}$ and a base of T/2:

$$Q = C \quad V_c \rightarrow C = \frac{Q}{V_c} \tag{40}$$

Assuming a constant C_2:

$$C_2 = \frac{Q}{\Delta Vc_2} \tag{41}$$

Thus, the variation in the load can be described as follows:

$$Q = \int i.dt$$

$$\Delta Q = \frac{\frac{T}{2}\ \frac{\Delta i_{L_2}}{2}}{2} = \frac{T\Delta i_{L_2}}{8} \tag{42}$$

So, the capacitance value for capacitor C_2 can be determined as follows:

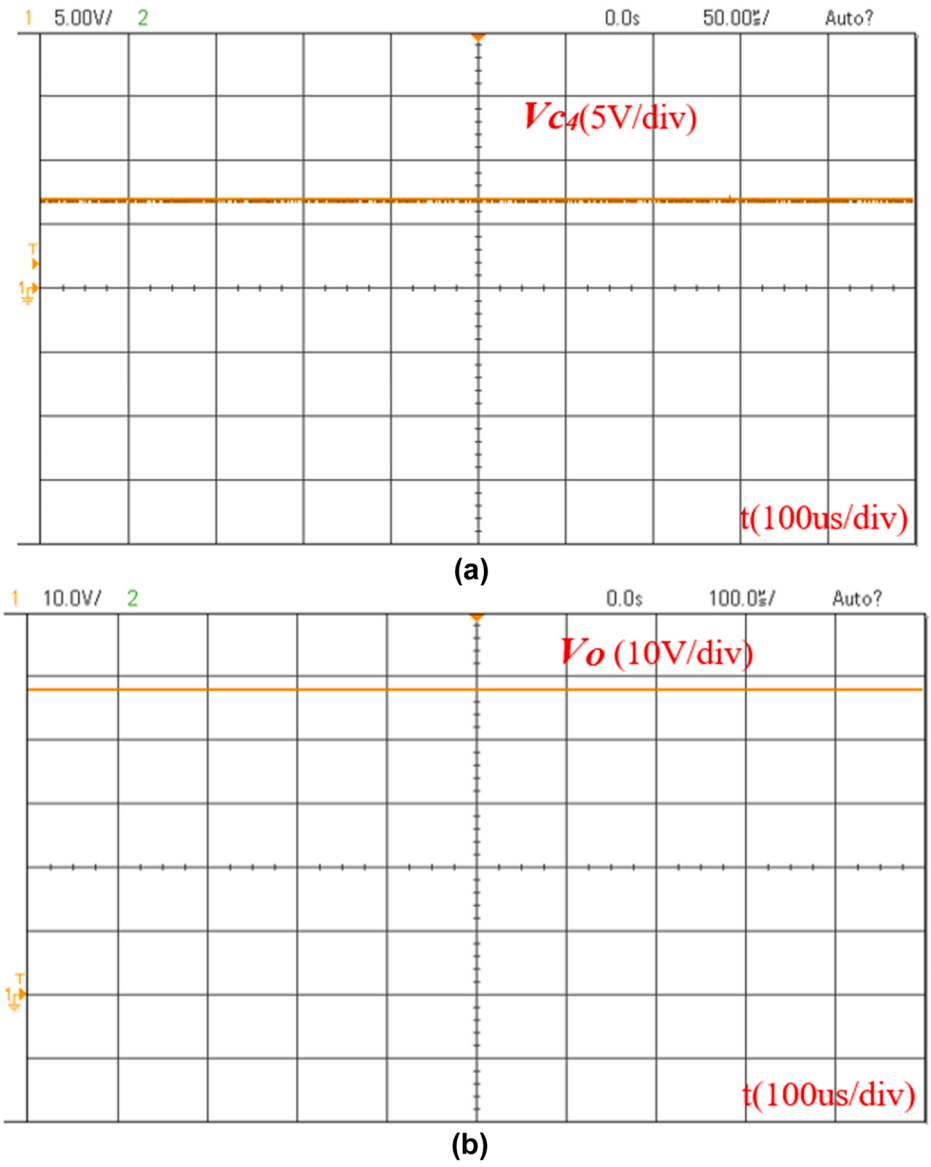

Fig. 10. (a) Voltage of Capacitor V_{C4} and (b) output voltage V_o.

$$C_2 = \frac{T\Delta iL_2}{8\Delta Vc_2} \tag{43}$$

In this study, capacitors C_1 and C_2 are analysed considering steady-state conditions. However, in practical operation, the converter may encounter dynamic changes in load resistance that need to be considered.

5.4. Analysis of losses summary

To evaluate the converter's efficiency, calculating power losses is essential and is carried out as detailed in (Kazimierczuk, 2016). Initially, determining the Root Mean Square (RMS) values for inductor currents is crucial. Disregarding ripples in the inductor currents, the RMS values are equivalent to their averages. Consequently, the following equations are formulated using (22) and (23).

Subsequently, using the specified formula, it can compute the conduction losses in the inductors.

$$P_{L1}^{Loss} = r_{L1} IL_{1rms}{}^2 = r_{L1} \left[\frac{1+D}{1-D} \quad I_o\right]^2 \tag{44}$$

$$P_{L2}^{Loss} = r_{L2} IL_{2rms}{}^2 = r_{L1} \quad [\quad I_o]^2 \tag{45}$$

Inductors L_1 and L_2 have corresponding equivalent resistances, denoted as r_{L1} and r_{L2}. Subsequently, we proceed to compute the capacitors' conduction losses using the provided equations.

$$P_{C1}^{Loss} = r_{C1} Ic_{1rms}{}^2 = r_{C1}\left[d \quad I_o{}^2 + [\frac{d}{1-d} I_o]^2 (1-d)\right] \tag{46}$$

$$P_{C2}^{Loss} = r_{C2} Ic_{2rms}{}^2 = r_{C2}\left[d \quad I_o{}^2 + [\frac{d}{1-d} I_o]^2 (1-d)\right] \tag{47}$$

$$P_{C3}^{Loss} = r_{C3} Ic_{3rms}{}^2 = r_{C3}[d \quad IL_1{}^2 + IL_1{}^2 (1-d)] \tag{48}$$

$$P_{C4}^{Loss} = r_{C4} Ic_{4rms}{}^2 \quad r_{C4}\left[dIL_2{}^2 + (1-d) IL_1{}^2\right] \tag{49}$$

The capacitors C_1, C_2, C_3, and C_4 are associated with equivalent

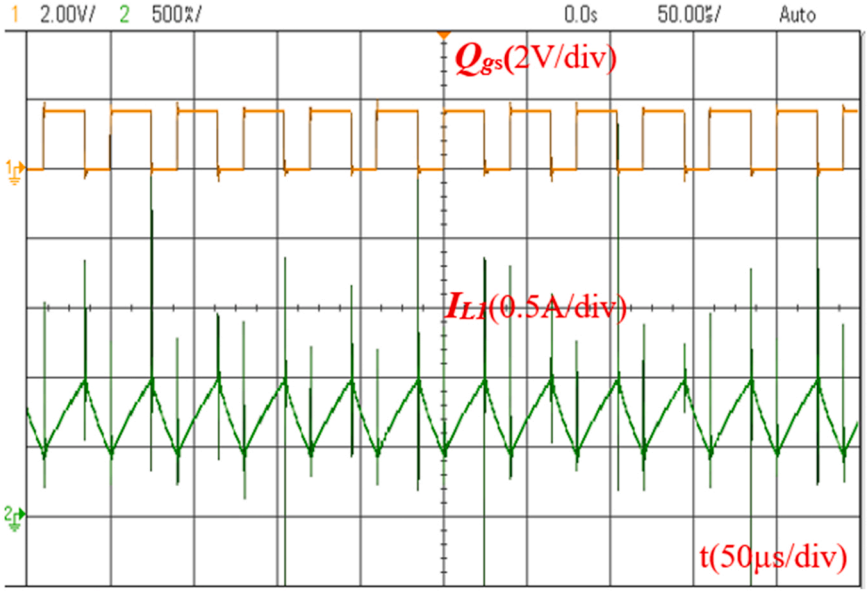

Fig. 11. The gate drive signal and Currents flows through the inductor I_{L1}.

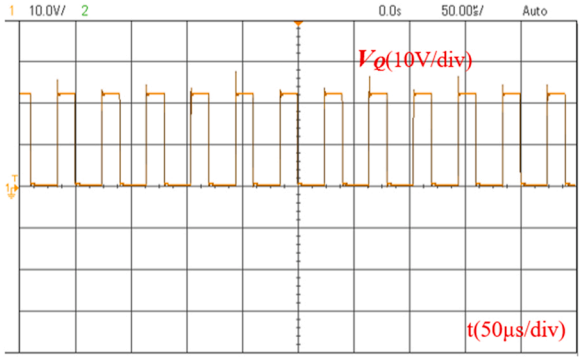

Fig. 12. Voltage-across-the switch Q.

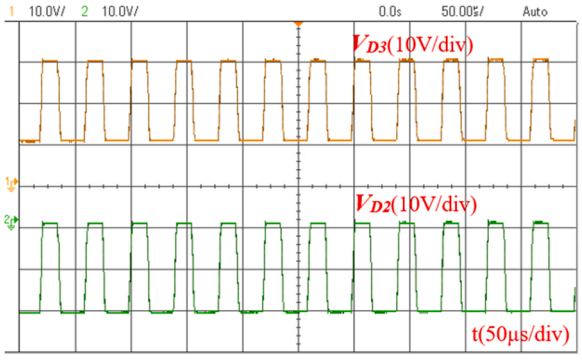

Fig. 13. Voltage across the diode D_3 and D_2.

resistances denoted as r_{C1}, r_{C2}, r_{C3}, and r_{C4}. Additionally, it is crucial to consider power losses in diodes, necessitating the determination of forward resistance and forward voltage for each diode. We can employ the given formula to compute power losses across the diodes.

$$P_{\mathrm{D1}}^{\mathrm{Loss}} = r_{D1} \quad dI_{L1rms}{}^{2} + V_{F1} \quad I_{L1} \tag{50}$$

$$P_{\mathrm{D2}}^{\mathrm{Loss}} = r_{D2} \quad dI_{D2rms}{}^{2} = \frac{r_{D2} \quad I_o{}^{2}}{1-d} + V_{F2} \quad I_o \tag{51}$$

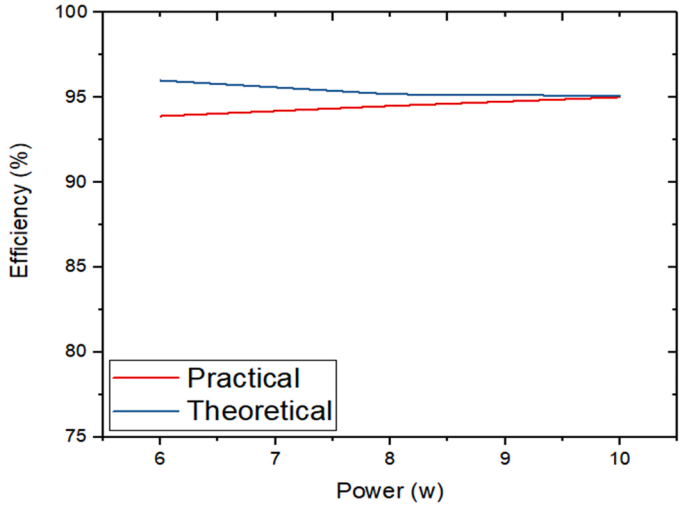

Fig. 14. Converter efficiency for various output powers.

$$P_{\mathrm{D3}}^{\mathrm{Loss}} = r_{D3} \quad dI_{D3rms}{}^{2} = \frac{r_{D3} \quad I_o{}^{2}}{1-d} + V_{F3} \quad I_o \tag{52}$$

The equivalent resistance encompassing three diodes is denoted as r_{D1-3}. Furthermore, V_{F1-3} represents the forward voltages for diodes D_1-D_3, and Io signifies the converter's output current. Lastly, we will determine power losses attributed to the power switch. Referring to (Kazimierczuk, 2016),it will analyse switching losses, accounting for both switching and conduction losses.

$$P_{\mathrm{Q}}^{\mathrm{Loss}} = r_Q d_1 (IL_{1rms} + IL_{2rms})^2 + \frac{1}{2} \quad f_s C_s V_Q{}^2 \tag{53}$$

For switch Q, the equivalent resistance is denoted by r_Q. The output capacitor is represented by the C_s value of the Mosfet. The efficiency of the presented converter can be computed using the subsequent formula:

$$\begin{aligned} P_L oss^t otal &= P_L 1^L oss + P_L 2^L oss + P_C 1^L oss + P_C 2^L oss + P_C 3^L oss \\ &+ P_C 4^L oss + P_D 1^L oss + P_D 2^L oss + P_D 3^L oss + P_Q^L oss \end{aligned} \tag{54}$$

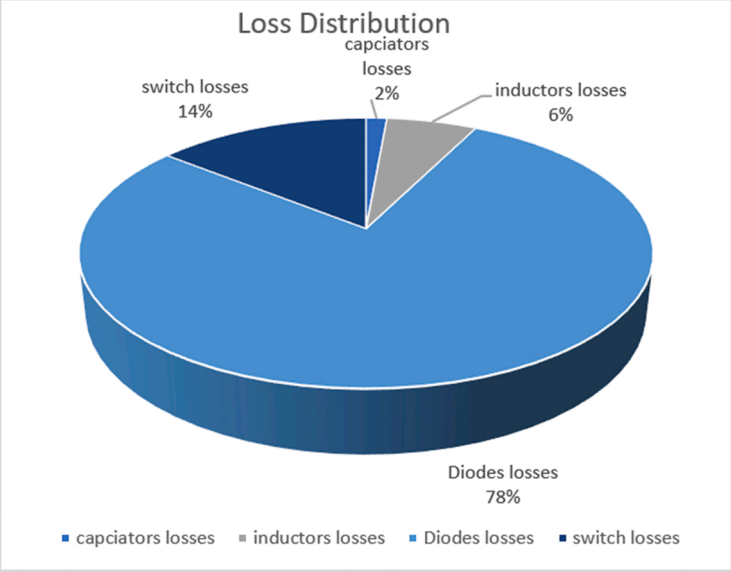

Fig. 15. Loss distribution of the presented converter.

Table 2
An analysis of the performance of similar converter topologies.

Topology resembling the proposed converter	Circuit design in (Zhang et al., 2018)	Circuit design in (Farsizadeh et al., 2020)	Circuit design in (Saravanan and Babu, 2017)	Circuit design in (Maroti et al., 2018)	Circuit design in (Banaei et al., 2014)	Proposed Circuit design
The employed switches	1	2	1	1	1	1
The employed Diodes	5	2	2	3	1	3
Number of inductors utilised	3	2	2	3	2	2
Number of capacitors utilised	3	2	3	3	3	4
Continuous input current	Y	N	Y	Y	N	N
Voltage gain, V_O	$\frac{(d)^2}{(1-d)^2}V_{in}$	$\frac{2(1+d)}{(1-d)}V_{in}$	$\frac{1}{(1-d)}V_{in}$	$\frac{d}{(1-d)^2}V_{in}$	$\frac{2d}{(1-d)}V_{in}$	$\frac{(1+d)}{(1-d)}V_{in}$
Efficiency	91 %	90 %	91 %	90 %	92 %	93.9 %
The voltage stress on the active switch	Moderate	Less	High	Less	High	Moderate

$$\eta = \frac{P_{out}}{P_{out} + P_{\text{Loss}}^{\text{total}}} \tag{55}$$

By simplifying and substituting the aforementioned equations, the efficiency of the converter can be calculated.

6. Simulation outcomes

To validate the theoretical analysis, simulations are conducted using the parameters outlined in Table 1 for the combined Luo-Cuk converter. Given its applicability in lighting systems with low-voltage inputs and LEDs, the simulation is configured to reflect such scenarios. Fig. 5 illustrates a representative control strategy for the combined Luo-Cuk converter.

A simulation waveform of the new combined Luo-Cuk converter is shown in Figs. 6–8. A waveform of inductor i_{L1} is shown in Fig. 6, which also shows the output voltage of 48 volts. Based on the figure, the ripple in current flowing through inductor L_1 appears to be relatively low. A waveform of the gate driving signal for switch Q and a voltage stress waveform for switch Q and diode D_1 is shown in Fig. 7. Further, switching voltage stress roughly equals 5/8 of the switch's output voltage. According to Fig. 8, a waveform of the voltage stress applied to the diodes D_2 and D_3 has been displayed. In accordance with the theoretical analysis, the simulation results support the results in the analysis above.

7. Results of experimental

To evaluate the practicality of the proposed concept, a low-power hardware prototype was assembled. The experimental setup featured in Table 1 adopted the same circuit parameters as the simulation. Rather than utilizing the source of solar energy, a constant voltage power supply was employed. The input was powered by a 7 V source, and the system integrated a TMS320F28335 digital signal controller for real-time control. The output voltage was configured to 48 V for testing. Fig. 9 illustrates the physical prototype and Maintaining a duty cycle below 0.7 resulted in a voltage gain of around 6.8 and helped minimize semiconductor losses, consistent with simulation outcomes. Fig. 10(a) clearly displays the 48 V output voltage, while Fig. 10(b) exhibits a voltage waveform across capacitor C_4. Fig. 11 provides waveforms for the experimental inductor currents and the gate drive signal of the switch, confirming the inductor's operation in Continuous Conduction Mode (CCM). Additionally, Fig. 12 presents the waveform of the voltage across switch Q. The waveform for voltage across diode D_2 and D_3, is provided in Fig. 13 which highlights their operation of complementary with lower voltage stress compared to the output. Lastly, practical, and theoretical efficiency curves are presented in Fig. 14.

The efficiency of the converter, when operating at 6 watts, is consistently above 93.9 % according to this figure. With a duty cycle of 0.65, the converter reaches its maximum efficiency, nearing 95 %.

Additionally, Fig. 15 demonstrates the distribution of losses in the presented converter. According to calculations based on Eqs. (44)-(55), power losses in all components can be evaluated. In this converter, approximately 78 % of power loss is attributed to the three power diodes, while the switch accounts for around 14 % of power losses after the power diodes. On the other hand, the power losses from the four capacitors and two inductors are relatively small. The figure also shows power losses calculated for the experimental conditions. For instance, at a power output of 10 watts, the diodes experience an approximate power loss of 0.4 watts.

7.1. Performance comparison highlights

As depicted in Table 2, a comparison of the proposed converter's performance with similar converters is presented. The table illustrates that the proposed converter enables superior voltage gain using a single active switch and minimizes normalized voltage stress on the switch. The analysis and discussion confirm the functionality and advantages of the proposed converter.

8. Conclusion

This paper presents an integrated Luo-Cuk converter designed for LED lighting applications, leveraging the unique features of LED drivers and lighting systems. The converter's topology, operational principles, and steady-state characteristics are comprehensively explained. The converter exhibits dual characteristics, allowing it to attain a substantial increase in voltage by combining a Luo topology and a Cuk topology within a single input branch. This setup enables the realization of two output types simultaneously using a single switch. Additionally, the converter offers an increased voltage static gain and reduces stress on diodes and switches. Experimental results from a laboratory prototype, supported by theoretical and simulation analyses, affirm the suitability of this single-switch hybrid DC/DC converter for LED-Driving (LD) and various Lighting-Systems (LS), specifically, it is well-suited for DC lighting systems (DLS) with varying level of voltage originated by the input power source.

CRediT authorship contribution statement

Conception and design of study: **E . Alhani, F. Anayi**; acquisition of data: **E . Alhani**; analysis and/or interpretation of data: **E . Alhani, F. Anayi**. Drafting the manuscript: **E . Alhani, F. Anayi**; revising the manuscript critically for important intellectual content: **E . Alhani, F. Anayi**. Approval of the version of the manuscript to be published (the names of all authors must be listed): **E . Alhani, F. Anayi**.

Declaration of Competing Interest

The authors contributed the same in producing this manuscript.

Data availability

No data was used for the research described in the article.

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