EFFICIENCY IMPROVEMENT IN BASE STATION POWER AMPLIFIERS

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by
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Abstract

Power amplifiers (PAs) are critical components in mobile base stations and are responsible for a significant portion of the overall power consumption. Due to the stringent design requirements and the high peak-to-average power ratio (PAPR) of modern communication signals, PAs are often energy inefficient, with a significant portion of the consumed power being dissipated as heat rather than being utilised for signal transmission. To address this issue, various efficiency enhancement techniques, such as Doherty, envelope-tracking, and load-modulated balanced amplifiers, have been developed. At present, Doherty PAs are the prevalent topology employed in mobile base station applications. In recent years, system level energy-saving techniques for base stations have attracted much attention. One such technique is average power tracking, which dynamically adapts the PA's supply voltage and power output based on the number of users, as opposed to maintaining a static configuration at all times. This approach effectively reduces PA consumption during low traffic periods by operating in a lower power mode and increases output during peak traffic periods by operating in a higher power mode, resulting in more efficient energy utilisation. This thesis presents the design and development of a Doherty PA for tracking average power in applications with varying supply voltages at frequencies around 3.5 GHz. This work focuses on the characterisation and modelling of the behaviour of transistors in response to changes in supply voltage, while acknowledging the challenges in fully implementing this method, such as the implementation of a supply modulator and advanced signal processing.

Load-pull measurement are widely used within the PA design community to characterise the large-signal behaviour of the transistors. In this work, load-pull measurement at different supply voltage were performed on 3 W GaN HEMT die device. The collected load-pull data

was used to develop a new DC-dependent Cardiff behavioural model which was capable to accurately interpolate the load-pull data with regard to the DC supply voltages. In addition, the model was verified against the load-pull data of 10 W and 25 W packaged GaN HEMTs which they were then used to design the multi-bias Doherty PA with a DC supply range of 30 V to 50 V.

The main challenge in utilising a behavioural model for the design of Doherty PAs is modelling the dynamic characteristics of the auxiliary stage in both ON and OFF states. To overcome this, a modified version of the Cardiff model was implemented which incorporates input drive variation. Additionally, a technique utilising a hyperbolic tangent activation function was employed to seamlessly switch between small-signal and large-signal device responses. This enabled the design of a dual-input Doherty PA, whose performance was validated through measurement and simulation results. Furthermore, a single-input version of the Doherty PA was fabricated and evaluated, displaying excellent back-off performance at 30V and 50V supply voltage, with a 100 MHz 5G test signal. The efficiency of this device exceeded 47% and it exhibited an adjacent channel leakage ratio (ACLR) of less than -45 dBc when the digital predistortion (DPD) was applied.

The thermal operating conditions and their effect on the performance of semiconductor devices are a critical consideration in the development of nonlinear models. In this thesis, a new temperature-dependent Cardiff model is developed using load-pull measurement data of two GaN HEMT dies over a temperature range of 25 °C to 100 °C. The validity of the model was verified by designing a class AB power amplifier based a 10 W packaged device. Comparison of the simulating and measurement results of the PA verified the accuracy of the model in predicting the device's behaviour under varying temperature conditions.

With the development of advanced efficiency enhancement techniques, it is now common to have multiple stages of amplification in a PA. Conventional methods for distributing the input signal to multiple stages involve the use of passive splitter components. However, providing separate inputs for each stage can offer increased flexibility for optimising PA performance. This thesis presents an unconventional application of the Cardiff model to

predict the simulated output response of a dual-input load modulated balanced amplifier (LMBA). Initially, a smaller dataset with varying input trajectories was used to extract the model coefficients, which were then tested on a much larger dataset. The device response at different input trajectories was used to identify the optimal combination of input signals, considering their magnitude and phase, to achieve optimal performance. This demonstrates the capability and flexibility of the Cardiff model in predicting the response of multi-port nonlinear devices, such as the dual-input LMBA, and its ability to be used in system-level simulations.

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I would like to express my sincere gratitude to my supervisor, Dr Roberto Quaglia, for his invaluable guidance, support and encouragement throughout my PhD journey. His expertise in measurement and design, as well as his critical feedback on my technical writing, have been instrumental in shaping my growth as a professional Microwave Engineer. He was always available to provide help and support whenever I needed it. I have learned so much from him and am deeply grateful for all that he has done for me. I am also grateful for the opportunities he has provided me to develop my professional career. His dedication and support have been invaluable and I am deeply grateful for the opportunity to have worked with him.

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List of Publications

- **E. M. Azad**, R. Quaglia, J. J. Bell, K. Chaudhry, and P. J. Tasker, "DC-Dependent Cardiff Model from Modulated Supply and Load-Pull Data," 2022 Asia-Pacific Microwave Conference (APMC), 2022, pp. 181-183, 10.23919/APMC55665.2022.9999796.

- **E. M. Azad**, R. Quaglia, K. Chaudhary, J. J. Bell, and P. J. Tasker, "Cardiff Model Utilization for Predicting the Response of Multiple-Input Power Amplifiers," in 2022 Microwave Mediterranean Symposium (MMS), 9-13 May 2022, Conference Proceedings, pp. 1–4. doi:.10.1109/MMS55062.2022.982551613.

- **E. M. Azad** et al., "Load-Pull Data Analysis of a GaN on SiC HEMT Targeting Multi Bias Doherty Design," 2022 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMiC), 7-8 April 2022, pp. 1-3, doi: 10.1109/INMMiC54248.2022.9762106.

- **E. M. Azad**, J. Bell , R. Quaglia, and P. Tasker, "Latest Cardiff Nonlinear Behavioural Model Developments," ARMMS RF and Microwave Society, Oxford, UK, 25-26 April 2022.

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- **E. M. Azad**, J. J. Bell, R. Quaglia, J. J. M. Rubio, and P. J. Tasker, "Gate Bias Incorporation into Cardiff Behavioural Modelling Formulation," 2020 IEEE/MTT-S

International Microwave Symposium (IMS), 2020, pp. 420-423, doi: 10.1109/IMS30576.2020.9223817.

Other Contributions

- M. Tian, J. Bell, **E. Azad**, R. Quaglia and P. Tasker, "A Novel Cardiff Model Coefficients Extraction Process Based on Artificial Neural Network," 2023 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications, Las Vegas, NV, USA, 2023, pp. 1-3, doi: 10.1109/PAWR56957.2023.10046221.

- A. Baddeley, **E. Azad**, R. Quaglia, J. Bell, and P. Tasker, "Gate bias voltage dependence of Cardiff admittance model in Ka-band GaAs pHEMTs," 2022 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR), 2022, pp. 8-10, doi: 10.1109/PAWR53092.2022.9719858.

- Y. Alimohammadi **et al.**, "Incorporating Gate-Lag Effects into the Cardiff Behavioural Model," 2020 50th European Microwave Conference (EuMC), 2021, pp. 684-687, doi: 10.23919/EuMC48046.2021.9338185.

Acronyms

3D	3-Dimensional
ACLR	Adjacent Channel Leakage Ratio
AM	Amplitude Modulation
APT	Average Power-Tracking
BO	Back-Off
BPA	Balanced Power Amplifier
BS	Base Station
CAD	Computer-aided Design
CSP	Control Signal Power
CW	Continuous Wave
DC	Direct Current
DPA	Doherty Power Amplifier
DPD	Digital Pre Distortion
DPS	Dynamic Power Supply
DUT	Device Under Test
DWLUT	Direct Waveform Look-up Table
ET	Envelope Tracking
EVM	Error Vector Magnitude
FEM	Finite-Element Method
GaN	Gallium Nitride
HEMT	High-Electron-Mobility Transistor

IF	Intermediate Frequency
ITU	International Telecommunication Union
IoT	Internet of Things
LDMOS	Laterally-Diffused Metal-Oxide Semiconductor
LMBA	Load-Modulated Balanaced Amplifier
LSOP	Large Signal Operating Point
MISO	Multi-input-single-output
MMIC	Monolithic Microwave Integrated Circuit
MNO	Mobile Network Operators
OBO	Output Power Back-Off
OMN	Output Matching Network
OPEX	OPerational EXpenditure
OTFS	Orthogonal Time Frequency Space
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peack-to-Average Power Ratio
PCB	Printed Circuit Board
PM	Phase Modulation
QoS	Quality of Service
RF	Radio Frequency
RFPA	Radio Frequency Power Amplifier
SCS	Signal Component Seperator
SG	Signal Generator
SM	Supply Modulator
SiC	Silicon Carbide
VNA	Vector Network Analyzer

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CHAPTER 1

Introduction

In our modern society, mobile technology (i.e. Smartphones) have become an integral aspect of daily life. They have revolutionised the way we communicate, access information, and perform everyday tasks. These devices are constantly within reach, providing us with a connection to the outside world through the internet, social media, and a variety of apps that allow us to stay organised, get directions, make purchases, learn, among other functions.

Investment in network infrastructure has greatly expanded access to mobile broadband networks for the majority of the global population, enabling them to take advantage of the numerous benefits and opportunities offered by mobile technologies. The "Coverage Gap" (which refers to those living in areas without mobile broadband coverage) has improved significantly over the last decade, decreasing from a third of the global population to only 6% [1]. The International Telecommunication Union (ITU) reports that the number of active mobile-cellular subscriptions is more than the global population in 2022, with 108 subscriptions per 100 people. In addition, there are 87 active mobile internet subscriptions per 100 people [2].

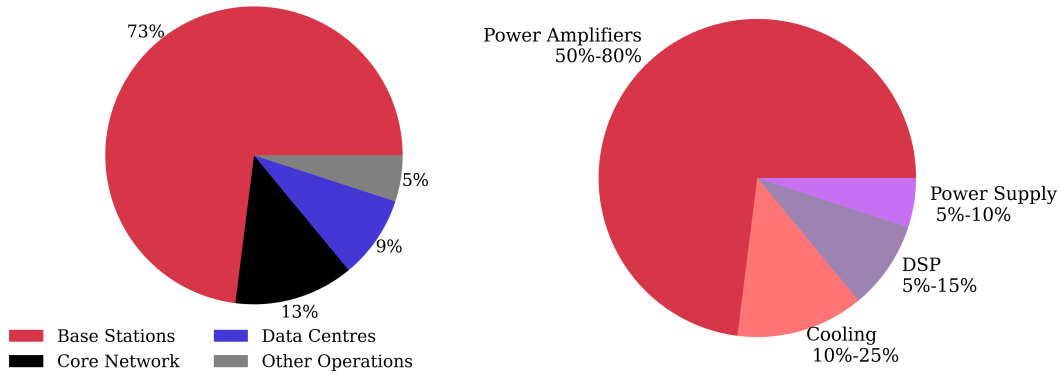
To achieve this significant progress in the mobile technology, Mobile network operators (MNOs) have been focusing on improving network capacity and quality of service (QoS) to increase the number of connected users per frequency band in a given area [3]. However, this focus on performance has led to a rise in energy consumption with each new generation of

cellular networks [4]. Currently, the 5$^{\text{th}}$ generation (5G) of mobile cellular network is being deployed in many countries globally. Operators are rolling out 5G networks using various spectrum bands, including sub-6 GHz bands and millimetre-wave (mmWave) bands [5]. Compared to previous generations of cellular networks, 5G networks have more throughput, lower latency, and support for more connected devices. The current deployment of the 5G network has been mainly based on the previous mobile infrastructure to provide additional network capacity, specially in the urban areas. The full deployment of the 5G promises to provide connectivity solution for tasks that require fast, reliable and near instantaneous network connection for applications such as healthcare, autonomous cars, and internet of things (IoT) [6].

To support the large number of connected devices, it is expected for 5G base stations to consume significantly more energy compare to the 4G [4]. This will significantly raise the operational costs (OPEX) MNOs due to higher energy bills. In other hand, MNOs are under pressure to maintain low OPEX while also meeting the growing demand for data to keep their services economically viable [7]. Therefore, energy efficiency of cellular networks is a crucial factor in reducing operational OPEX and making the network more cost-effective. Furthermore, by increasing network efficiency and reducing wasted energy, network providers can reduce their carbon footprint and environmental impact. This is an objective of the green network initiative [8, 9].

With regard to energy consumption, base stations (BSs) are the most dominant component in a cellular mobile network. In general, they are responsible for around 70% of the total energy used in the network [10]. This huge amount of energy is mostly used to operate the power amplifiers (PAs), within the transmitter modules, to boost the transmitted signal's energy level so it can travel over a longer distance to reach the users mobile devices. Figure 1.1 shows (a) the energy consumption distribution within a cellular network; and (b) the proportionate of each component in a base stations. As shown, PAs can make up to 80% [11] of the total energy consumed by a base station. However, a large amount of this

energy is wasted in the form of heat and not to transmit the signal due to the poor efficiency of the PAs.



(a) (b)

Figure 1.1: (a) Proportionate of the power consumption of a wireless cellar network [10]; (b) power consumption distribution in a base station [11]. Base stations are responsible for more than 70% of the total energy consumption of a cellular wireless network, which up to 80% of this energy consumption is dedicated to the power amplifiers.

1.1. Motivation

Designing an energy-efficient PA is a challenging task due to the trade-offs between different design requirements such as linearity, gain, efficiency, frequency bandwidth, and efficiency. For instance, the classic linear PA architectures such as class A and AB are only efficient (with textbook maximum efficiency of 50% and 78.5%, respectively) at the maximum power level where system's linearity requirement usually can not be met. Therefore, in such a scenarios the PA is used at an output back-off (OBO) level , where the efficiency reduces dramatically, to achieve a better linearity. However, the main factor contributing to the PA's low efficiency in recent cellular generations is the development of modern communication signals with a very high peak-to-average-power-ratio (PAPR). These signals require power amplifiers to operate at even lower OBO levels, resulting in overall low efficiency of PAs.

Because PAs are such a dominant components in terms of energy consumption, any improvement in their efficiency can improve the overall efficiency of the communication net-

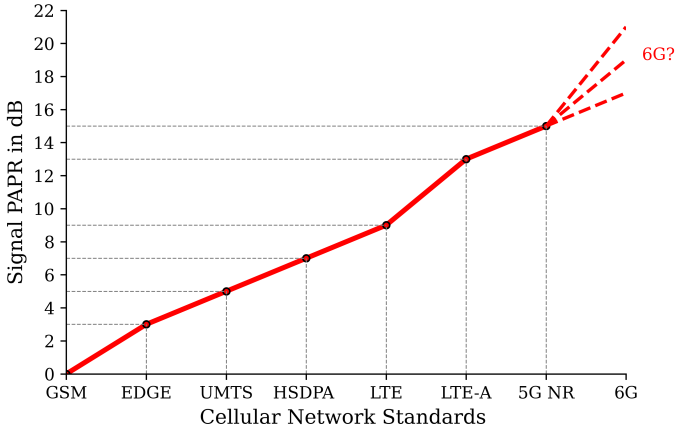


Figure 1.2: PAPR for different mobile communication standard [12, 13]. Each successive generation of cellular networks has a higher PAPR compared to the previous one.

works. That is why, despite the promises of potential waveforms for the next generation of cellular networks (6G), particularly Orthogonal Time Frequency Space (OTFS) modulation promising lower PAPR [14], an abundant amount of research and development resources have been dedicated to develop advanced efficiency enhancement techniques, such as Doherty and envelope tracking, for communication signals with high PAPR [15–18].

Doherty PA:

The Doherty PA is designed to improve efficiency at the OBO by using two amplification stages: the "Main" (biased in class AB) and the "Auxiliary" (biased in class C). At OBO, the Auxiliary PA is turned OFF and the Main PA is terminated at a higher resistive load (two times the optimum load for a classical DPA with 6 dB OBO) for improved efficiency. When the input drive exceeds the OBO threshold, the Auxiliary PA turns ON, and contributes to the overall output power, while also actively modulating the Main PA's load to a lower level (optimum load).

Envelope Tracking PA:

The **Envelope Tracking** (ET) technique improves the average efficiency of a PA by dynamically adjusting the output voltage bias point based on the input signal's amplitude. In this technique, the envelope information of the signal is used to control a modulator that adjusts the PA's supply voltage. The ET's implementation in BSs has been limited due to

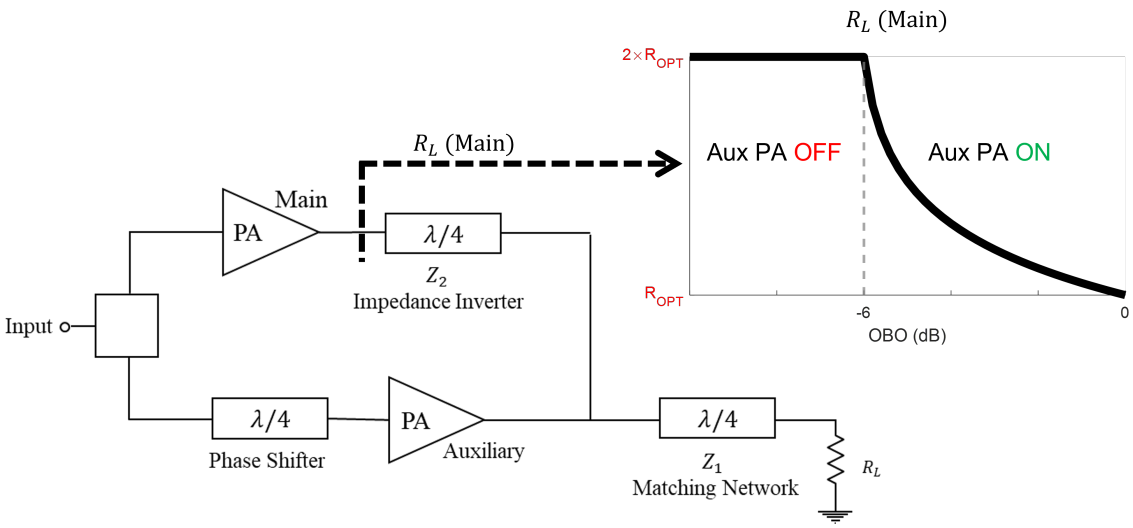


Figure 1.3: Block diagram of a **Doherty** PA and load trajectory of the Main PA with 6 dB OBO. At lower power levels (<6 dB OBO) the auxiliary PA is switched off and the main PA is terminated at a resistive load two times larger than its optimum load at the maximum power level ($2 \times R_{opt}$). For the case of higher power levels (>6 dB OBO), the Auxiliary PA turns ON and modulates the Main PA's load (through a quarter-wave transmission line). At the end, both amplifiers reach their maximum saturation condition. R_L is the load resistance.

challenges in signal processing and the low efficiency of the required fast modulators [13].

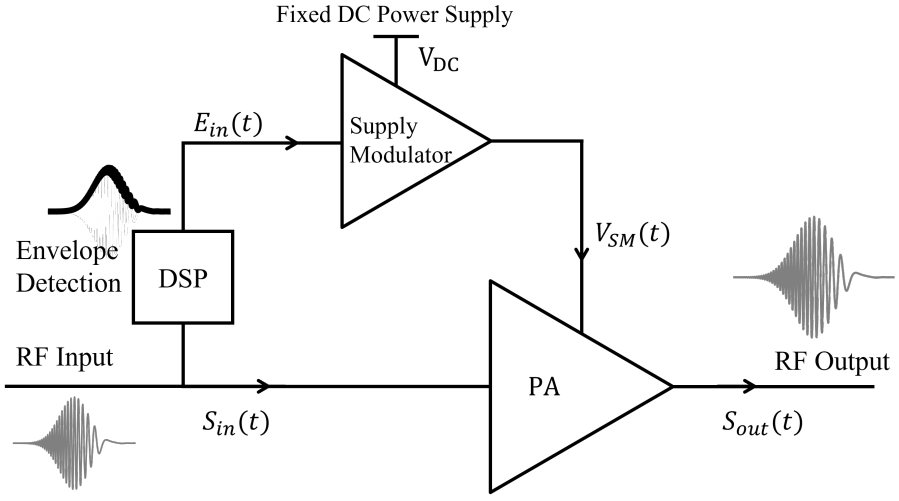


Figure 1.4: Block diagram of an **Envelope Tracking** architecture. Signal's envelopes information is fed to a modulator which adapts the supply voltage of the PA to the magnitude of input signal.

1.1.1. Load-pull measurement and Cardiff behavioural model

Load-pull measurements are commonly used in the PA design community to characterise the nonlinear behaviour of active devices. The principle of load-pull measurement is to measure the device's performance under non-50 Ohm load conditions under a large-signal excitation. The data obtained can then be used in a nonlinear CAD simulator during the PA design process. In practice, due to trade-offs between different design parameters the design of complex PA structures necessitates multidimensional characterisation data. A designer might need to vary several variables at the same time to be able to analyse the nonlinear behaviour of the active device and find the best compromise to meet all the design specifications. Therefore, to collect all the data for the design process, intensive and time-consuming measurements are inevitable.

To reduce the amount of the required load-pull data, hence reducing the measurement time, nonlinear behavioural models can be used to interpolate the load-pull data. The Cardiff university's Cardiff model [19] is one of the industry-leading nonlinear behavioural models. Its early mathematical developments were established on the accurate prediction of measurement data over a limited operation domain about the large signal operating point, LSOP. For example, at a fixed DC bias point, RF input drive level, and frequency. Further development of the Cardiff model has resulted in its improved generality, where parameters such as frequency [20] and input drive level [21] were included into its mathematical formulation.

With regards to DC bias variation, load-pull measurements at each bias point are typically required to generate a DC-dependent Cardiff behavioural model. However, during the course of this PhD, a new mathematical formulation was developed which includes the DC bias variation into the Cardiff behavioural model [22, 23]. This new formulation is able to interpolate the load-pull data with respect to DC bias variation, thus significantly reducing the amount of data required to generate a DC-dependent behavioural model. More

information about this new DC-dependent Cardiff model can be found in Chapter 4.

1.1.2. Multi-bias Doherty PA design using Cardiff behavioural model

In practice, the implementation of the envelope tracking PAs have been limited mainly because of the need for additional dynamic power supply (DPS) which is needed to rapidly adapt the PA's supply voltage to the signal's envelope. The speed required to modulate the DC supply voltage often results in the poor efficiency of the DPS which need to be taken in account when calculating the whole ET system's efficiency.

Doherty architecture has become the dominant design for base station PAs in recent years. Conventional Doherty PAs (DPAs), which use the same device size for both the main and auxiliary PAs, can achieve back-off efficiency of up to 6 dB OBO. For signals with higher PAPR (peak-to-average power ratio), an asymmetric DPA architecture can be used, in which a larger device with higher output power is employed for the auxiliary PA. This design results in a greater dynamic range (more than 6 dB OBO) compared to conventional DPAs.

By adapting the DPA's supply voltage to the average power (for example at different traffic conditions), its dynamic range can be even further improved such that efficiency is maintained at lower OBO levels [24, 25]. Note, unlike the ET PA, which requires rapid DPS, in this case a "stepped" DC supply modulation is considered. For example, a DPA with two working stages: power-saving mode and high-power mode.

Over the course of this PhD an Asymmetric-DPA capable of working at multi bias levels was designed using the new DC-dependent Cardiff behavioural model. More details on the design process of this PA will be covered in Chapter 6.

The behavioural model that is based on measurements has limitations when it comes to modelling the behaviour of a PA in class C configuration at very low input drive levels, which is required for the auxiliary stage in a DPA. When the device under test (DUT) is biased in class C and the input drive level is low, the load-pull measurement system cannot

be used as there is no output signal. This issue and its proposed solution will be discussed in more detail in Chapter 5.

1.1.3. Thermal modelling

Despite all the effort by the industry to improve the PA's performance, their poor efficiency will remain a challenge for the years to come. As a result, a large amount of energy is wasted as heat which can cause an increase in the device's temperature. It is well-known that the elevated temperature adversely affects the RF performance parameters such as gain, output power and linearity. Therefore, typically, thermal management systems are used to remove and dispose the wasted heat to keep the RFPAs temperature under control [26].

However, in certain circumstances, the use of effective thermal management system might not be feasible, and the RFPA has to operate at higher temperature levels. For example, when compactness is desired, or the ambient temperature is high and cooling the device to a suitable temperature level is either impossible or significantly costly. Needless to mention, in these situations, it is critical to select a semiconductor technology which can withstand the high-temperature operating conditions.

In recent, year gallium-nitrite (GaN) high-electron-mobility transistors (HEMTs) have attracted a lot of attention. GaN HEMTs have higher breakdown voltage and power density compare to other commercially available semiconductor technologies, such as gallium-arsenide (GaAs) and laterally-diffused metal-oxide semiconductor (LDMOS), which is an advantage in terms of output power and efficiency; hence, they have become the technology of choice for high-frequency and high-power PAs. The GaN HEMTs, in addition to power and efficiency, are also remarkably suitable for high-temperature applications [27], even though their performance declines at elevated temperatures [28], [29]. Therefore, to design a PA, it is highly beneficial to have access to nonlinear models capable of predicting the device behaviour under various temperatures in a nonlinear computer-aided design (CAD) simulator.

In Chapter 7, a new temperature-dependent Cardiff model will be discussed. This model is capable of predicting the device's behavior under various temperature conditions. The accuracy of the model is verified by comparing the simulation and measurement results of a Class AB PA, designed during this PhD project, at different temperatures.

1.1.4. Dual-input-single-output (DISO) PAs

With the development of more complex PA architectures, it is common now that to use two or more PAs to achieve the higher efficiency. In addition to the DPA, the load modulated balanced amplifier (LMBA) [17, 30], and some of its variants, like the inverted-LMBA, have demonstrated a better ability to operate on wider frequency bands. Similar to Doherty PA, in an LMBA PA multiple PA's are used to achieve high efficiency at OBO.

Independently from the architecture perspective, there are important advantages from a performance point of view if the multiple transistors can be driven by independent RF inputs, rather than derived from a single input by means of passive signal splitters. In fact, the so-called Multiple-Input, Single Output (MISO) PAs allow a "digital" signal splitting at baseband level, with the possibility of imposing non-linear relations between the several inputs which can help to optimise the RF performance [31], [32].

Increasing the number of inputs means increasing the degrees of freedom in using the PA, so the search for an optimum configuration of the input signals becomes an interesting engineering problem. For MISO PAs, the search for the optimum input configuration, either directly in measurement or with a circuit level simulation, can be time consuming. Therefore, a behavioural model derived from a smaller dataset that can predict the larger dataset through interpolation is of great interest.

In Chapter 8 of this thesis, the use of the Cardiff behavioural model to represent the response of a dual-input inverted-LMBA is proposed.

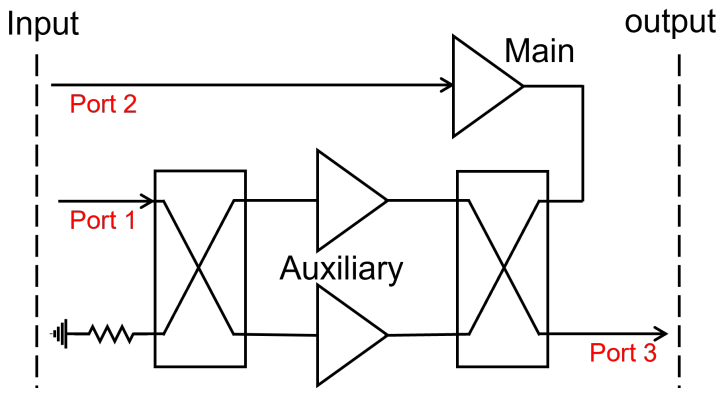


Figure 1.5: Block diagram of an inverted-LMBA MISO PA with two inputs and one output. The Cardiff model formulation can be used to predict the PA's output response (at port 3) respective to the two input stimulus signals at (port 1 and 2).

1.2. Original Contributions

Several original contributions were made as part of the research conducted and will be discussed in this thesis:

- Including Gate bias into the Cardiff model [22]
- Including Drain bias voltage into the Cardiff behavioural model [23]
- Full DC-dependent Cardiff model [23]
- Spectral analysis of Fourier transformed modulated DC and load-pull data [33].
- Load pull data analysis for multi-bias Doherty PA design [34].
- Simulation technique for multi-bias Doherty PA design [34].
- Including Temperature into the Cardiff Model
- Modelling the response of a multi-input single-output PA (MISO) [35].
- A behavioural model suitable for Doherty PA design.
- A measurement-based Doherty PA design using Cardiff model.

1.3. Overview of the Thesis

This thesis, excluding the introduction, is composed of eight chapters. The first two chapters provide an overview of relevant literature with different focuses. The next five chapters present the research conducted in detail, and the final chapter concludes the thesis.

Chapter 2, the first literature review chapter, reviews Doherty power amplifiers and other efficiency enhancement techniques such as envelope tracking, LMBA and outphasing. The recent developments in multi-bias and dual-input DPAs in the literature are also discussed. Furthermore, the importance of accurate transistor modelling and various modelling solutions to include the large signal behaviour of transistors are also explored.

Chapter 3, the second literature review chapter, focuses on load-pull measurement systems and nonlinear behaviour modelling. Various load-pull measurement systems and their advantages and limitations are reviewed. Additionally, the development of behavioural models and recent advancements in the mathematical formulation of the Cardiff model are discussed.

The first research chapter is **Chapter 4**, which is dedicated to including DC supply voltage into the Cardiff model formulation. It includes the expansion of polynomial formulation of Cardiff model to include the DC variation based on the mixing theory. The proposed model formulation is then verified using load-pull measurement data of a GaN HEMT.

Chapter 5 presents a new Cardiff model formulation and CAD implementation that is suitable for the design of class C power amplifiers, specifically the auxiliary stage in a Doherty power amplifier. The chapter examines previous work on incorporating input power into the Cardiff model, and presents a new model formulation to address its limitations. The proposed modelling solution was validated by designing and measuring a class C power amplifier.

Chapter 6 is focused on the design and measurement of a multi-bias asymmetric DPA

using the Cardiff model. The chapter includes the analysis of load-pull data to determine the optimal load modulation trajectory for optimal performance. Two variations, a single input and a dual input design, of the same DPA were fabricated, and the measurement results are compared.

Development of a temperature-dependent Cardiff model is included in **Chapter 7**. Load-pull measurements of two GaN HEMT die devices were used to develop and verify the model variation. The proposed model was then used to design a class AB power amplifier. The comparison of the measurement and simulation results of the designed PA verified the accuracy of the new temperature-dependent Cardiff model.

Chapter 8 explores the functionality of the Cardiff model in an unconventional system-level application to predict the response of a dual-input PA. Simulation data of a dual-input LMBA was used to verify the accuracy and applicability of Cardiff model.

In the final chapter **Chapter 9**, the research presented in the thesis is summarised and the results are discussed. Additionally, potential directions for future research and unresolved questions that emerged during the study are highlighted.

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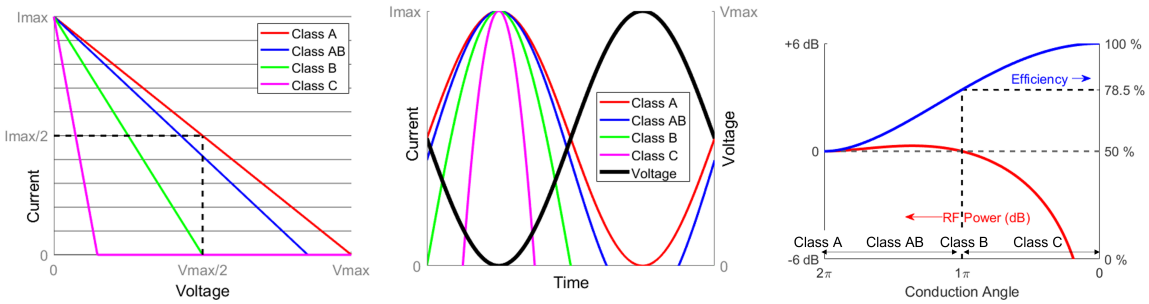
CHAPTER 2

Doherty Power Amplifiers and other Efficiency Enhancement Techniques

The conventional single-ended power amplifiers are usually identified in several classes which represent their biasing conditions. The most famous PA classes are class A, AB, B, and C. It is common in the text-books, to explain different PA classes, to start with the class A due to its intuitive biasing condition. In a class A configuration, for an ideal transistor with no knee voltage, the transistor is biased exactly at the mid-point from the maximum voltage and current, which enables full-cycle amplification of the signal (2π conduction angle) without adding any harmonic components to the signal (assuming that the amplitude of the drive signal is not exceeding given stated limits). For example, if the drive signal is a perfect sinusoidal waveform, the output current will also be sinusoidal without any added non-linearity.

However, the linearity advantage of the class A amplifiers comes at the cost of their low efficiency, with maximum theoretical peak efficiency of only 50%. Other "reduced-conduction-angle" PA classes such as class AB, B and C can be considered to achieve higher peak efficiency. For example, in a class B PA, where the transistor's gate voltage is set to pinch-off voltage (V_{gs}^{DC}=pinch-off) with zero biasing DC current (I_{ds}^{DC}=0), the PA only amplifies half of the current waveform (1π conduction angle). Figure 2.1 compares the (a) load-lines, (b) current and voltage wave-forms, and (c) power and efficiency of the traditional PA classes (class A, AB, B and C).



(a) (b) (c)

Figure 2.1: Different power amplifier classes. (a) load-lines, (b) current and voltage waveform (c) efficiency and power performance. Class B shows a better efficiency performance compare to class A while maintaining the same output power level.

As shown in Figure 2.1, a class B PA can achieve higher peak efficiency (78.5%) compared to the class A (50%) while delivering the same amount of power. Considering only efficiency and output power performance, class B is the superior configuration as it delivers higher efficiency without compromising the output power. Favourably, class B also have a good linearity performance as it is illustrated in Figure 2.2 [1].

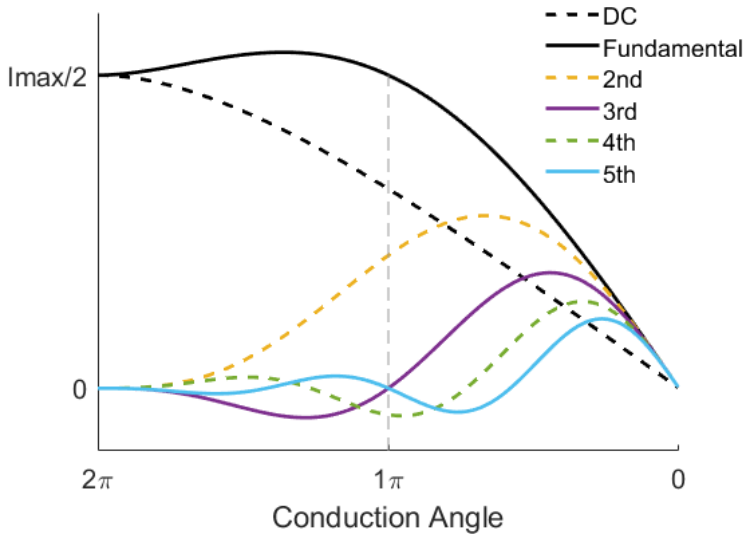


Figure 2.2: Harmonics current components vs conduction angle [1]. Conduction angle of 2π, 1π represent the class A and B configuration, respectively; while conduction angles less than 1π are classified as class C.

Referencing to Figure 2.2, class B configuration has a high 2nd harmonic current component, due to the rectifying effect caused by biasing below the pinch-off voltage [2]. In practice, the 2nd harmonic is short-circuited to restore the sinusoidal output current and engineer a tailored current waveform for achieving optimal efficiency [3, 4]. Considering the linearity, power, and efficiency performance of the ideal class B, they are the class of choice for designing highly efficient PAs at the peak power level. Note, in practical applications, PAs are often biased in class AB rather than class B due to better linearity performance. Class B operation is only linear in an ideal scenario, but real transistors have gain expansion characteristics at lower power levels [5].

However, modern communication systems have high peak-to-average-power-ratio (PAPR) (e.g. more than 12 dB and 15 dB for LTE and 5G signals [6]); which means although the designed PA needs to amplify at peak power level for the majority of the time it is operating at the back-off levels. This results in poor efficiency performance of simple PA architectures, such as class B, as the efficiency dramatically degrades at lower power levels as it is illustrated in Figure 2.3.

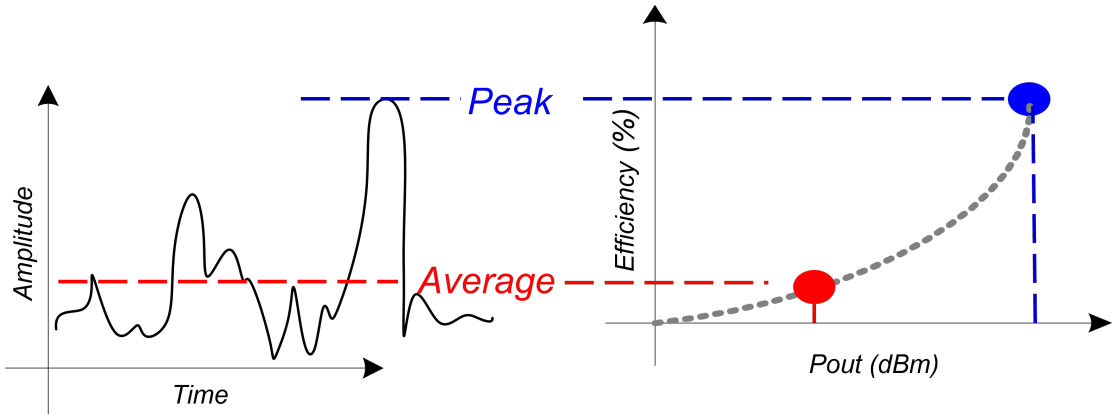


Figure 2.3: Demonstration of the signals with high PAPR and poor efficiency of the conventional class B PA's at the back-off power level.

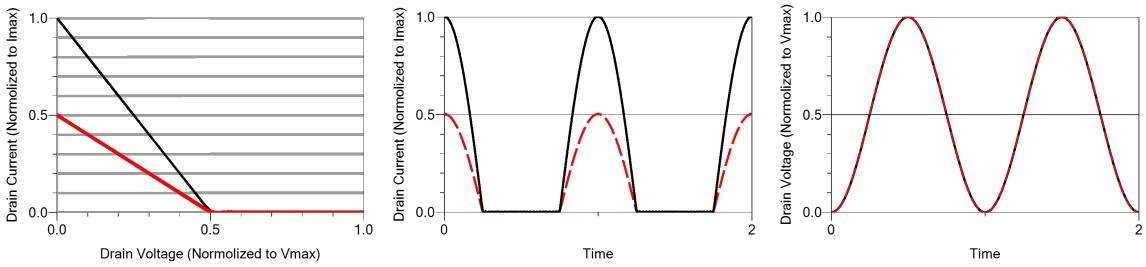
2.1. Efficiency Enhancement Techniques for Signals with High PAPR

To achieve better efficiency at the back-off power levels several efficiency-enhanced PA architectures have been developed. There are two main umbrella terms that describe all the efficiency enhancement efforts; they are load-modulation (e.g. Doherty, load-modulated balanced amplifier and outphasing) and supply-modulation (e.g. envelope tacking). In this section, an overview of these PA architectures is included.

2.1.1. Doherty Power Amplifiers

The concept of Doherty PA was first introduced by W. H. Doherty in 1936 [7] as a solution to design high efficiency power amplifiers for modulated broadcasting signals. In this classic paper, the author explains his "method of attack" by stating the concept that if a large enough load impedance presented to the device, which requires a large output voltage, high efficiency at any desired output power, can be achieved. In other words, the principal behind the Doherty architecture is to maintain the maximum output voltage at all times by manipulating the load impedance respective to the power level.

Figure 2.4 shows current and voltage response of an ideal class B PA, where its load resistance at back-off was adapted to the power level. Device response at the peak power level are shown in 'solid-black' lines and the 'dashed-red' representing the operation condition of the device at 6 dB back-off (BO) power.



(a) (b) (c)

Figure 2.4: Ideal class B (a) load line, (b) current waveform and (c) voltage waveform at maximum and 6 dB back-off power levels. At the back-off level, the load resistance is twice the optimum load at the full drive ($R_{BO} = 2 \times R_{opt}$).

As it is shown in Figure 2.4 (c), by using a larger impedance at BO the voltage waveforms at both BO and peak power levels are overlapping. As a result, the load-lines at both BO and peak power level cover the hole DC-IV plane (as shown in Figure 2.4 (a)) which means higher efficiency.

In practice, to achieve the load modulation in a Doherty power amplifier (DPA), two amplifiers ("main" and "auxiliary") are connected through a quarter-wavelength transmission line, as shown in Figure 2.5. The Main PA (also known as carrier PA) is normally biased in class B (or class AB for better linearity performance) where its load is dynamically modulated by the auxiliary PA (also known as peaking PA). At output back-off (OBO) power level, only the main PA is active, operating as a single-ended PA which is terminated at a load twice larger than what is expected for a conventional class-B PA design ($R_{OBO} = 2 \times R_{opt}$).

Referencing to Figure 2.5, the impedance inverter at the output is used to provide the correct load modulation (resistive impedance seen by the main stage goes down as the auxiliary device output current increases). The phase delay introduced by this impedance inverter is recovered by addition of a delay line at the input of the auxiliary device. The output matching network present R_{opt} at the saturation (P_{sat}), as in standard PAs. The offset lines [8] are added to the output sections of the main and auxiliary stages to optimise the Doherty performance at low power. Their characteristic impedance are equal to the

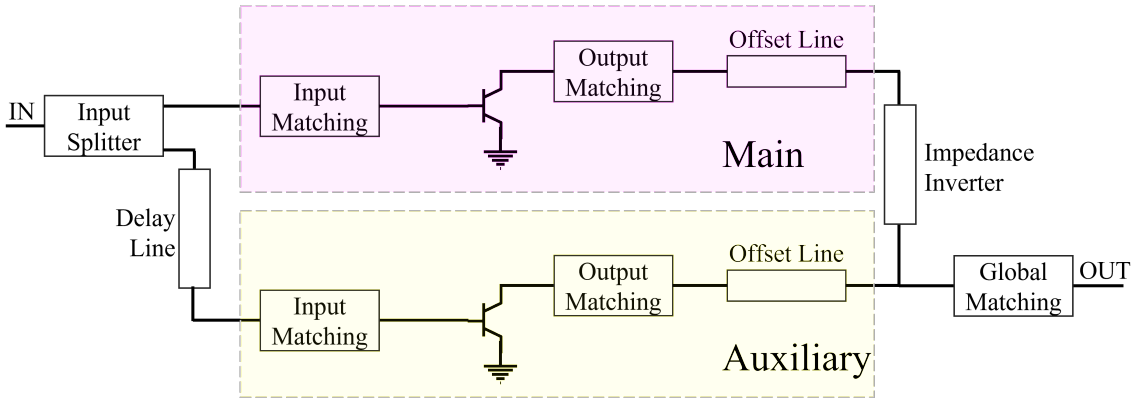


Figure 2.5: Typical Doherty Power amplifier (DPA) block scheme.

load impedance seen by the stage at saturation, in order to not to effect the saturated DPA behaviour. The auxiliary stage offset line ensures that the turned-off auxiliary does not affect the load seen by the main stage. The phase adjustment of the offset line causes the auxiliary PA to be open-circuited and prevents power leakage at the low power [8, 9]. For the main stage, offset line length is tuned to provide a purely real $2 \times R_{opt}$ load at the device output [10].

Figure 2.6 shows the normalised (a) current, (b) voltage, and (c) output power profile of the main and auxiliary stages of an ideal DPA. The input drive refers to the input voltage amplitude 'v_{in}', a normalised parameter sweeping from '0' to '1'. The '$v_{in} = 0.5$' is the voltage drive level where the main amplifier reaches its maximum output voltage and the auxiliary stage turns ON. At this drive level the output power is only a quarter of its maximum (6 dB OBO), as shown in Figure 2.6 (c).

Figure 2.7 shows a comparison of an ideal Doherty and class B PA at output back-off levels. As shown, the Doherty PA delivers the maximum efficiency at both 0 dB and 6 dB OBO. In contrast, efficiency of the ideal class B PA rapidly reduces for the lower power levels, and it delivers its maximum efficiency at only the peak power level (0 dB OBO).

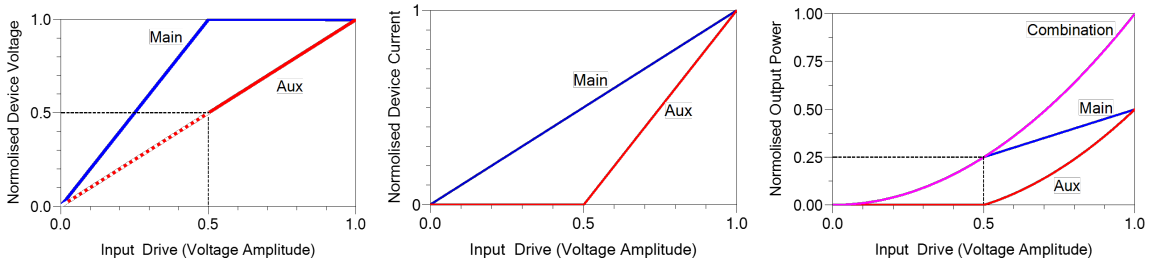


Figure 2.6: Ideal Doherty amplifier analysis. (a) Device voltage, (b) device current, and (c) output power. The input drive refers to the input voltage amplitude 'v_{in}', a normalised parameter sweeping from '0' to '1'.

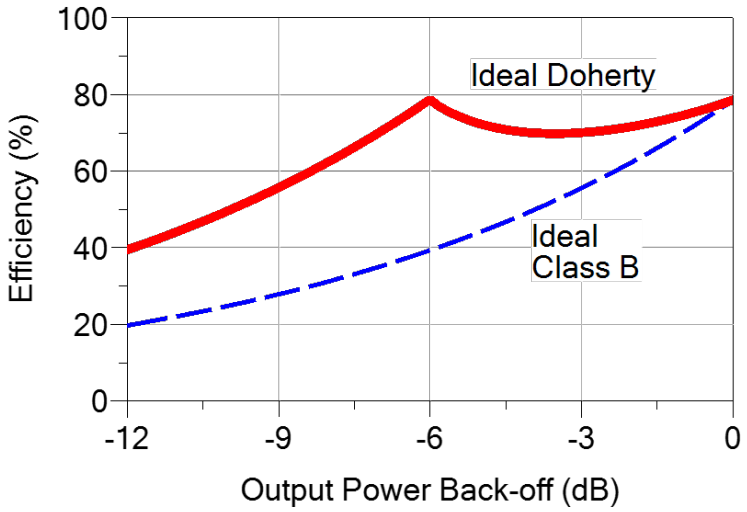
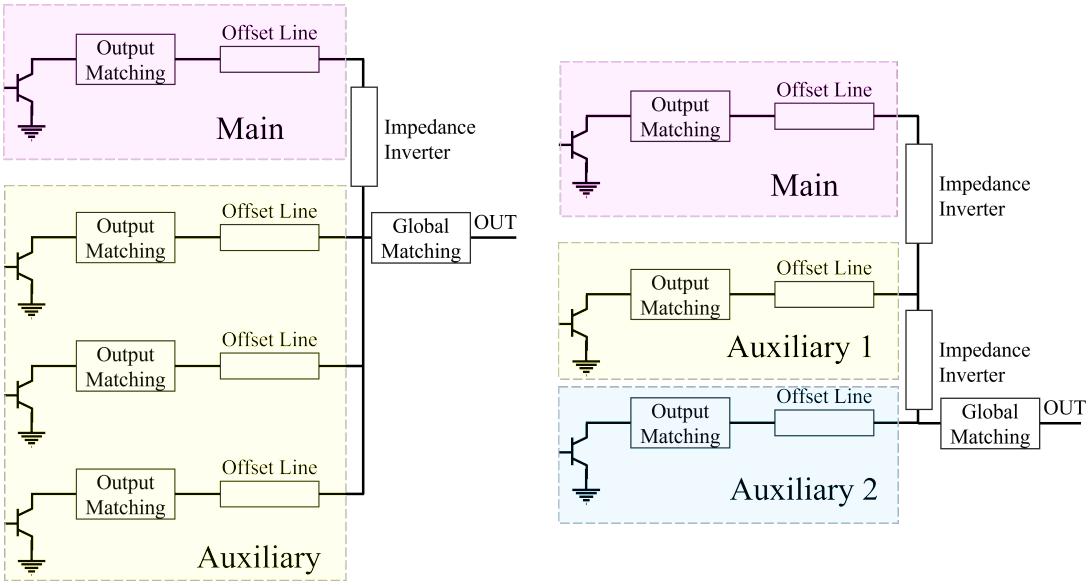


Figure 2.7: Comparison of ideal Doherty and Class B amplifiers efficiency at output power back-off.

2.1.1.1 Achieving higher back-off performance with Doherty PAs

The efficiency enhancement of conventional DPAs (where identical devices are used for both main and auxiliary stages) maximises at 6 dB OBO, see Figure 2.7. To improve the efficiency for the signals with larger PAPR (>6 dB), other variations of DPAs have been proposed.

Asymmetric DPAs, where the main stage operates at smaller output power compare to the auxiliary stages, can extend the high efficiency region over a wider output power range. For example 12 dB OBO can be achieved by a ratio of $\alpha = P_{main}/P_{aux} = 0.25$ [11]. In an asymmetric DPA structure, larger device periphery can be used for the auxiliary stage to deliver more output power. Alternatively, one can use identical device periphery to design N-way (asymmetric) DPA architectures, where the main amplifier is in parallel with (N-1) auxiliary amplifiers [12]. Figure 2.8 (a) shows output combiner of a 4-way asymmetric DPA.



(a) (b)

Figure 2.8: Output combiner of (a) a 4-way asymmetrical DPA, and (b) a 3-stage DPA (right) [10].

In an asymmetric DPA, the efficiency significantly drops in the region between the peak

efficiency points (Doherty region). In particular, this problem is more evident when the power ratio between the main and auxiliary PA is large [12]. However, it is possible to use multiple stages of auxiliary amplification to prevent this significant deterioration in the efficiency [11]. This is achieved with the so-called multistage DPA architectures [13].

Figure 2.8 (b) shows the output combiner of a 3-stage DPA. As shown, output of 2 auxiliary stages are combined using the impedance inverter component (quarter-wave transmission lines) to combine their power. Each auxiliary stage turns ON at a different power level to create an active load-pull effect and modulate the main PA's load.

Figure 2.9 shows the efficiency performance of a 3-stage DPA compared to a class B PA, conventional DPA (2-stage), and 4-way asymmetric DPA. As it is shown, the 3-stage DPA has significantly improved the efficiency deterioration at in the Doherty region compared to the asymmetric DPA.

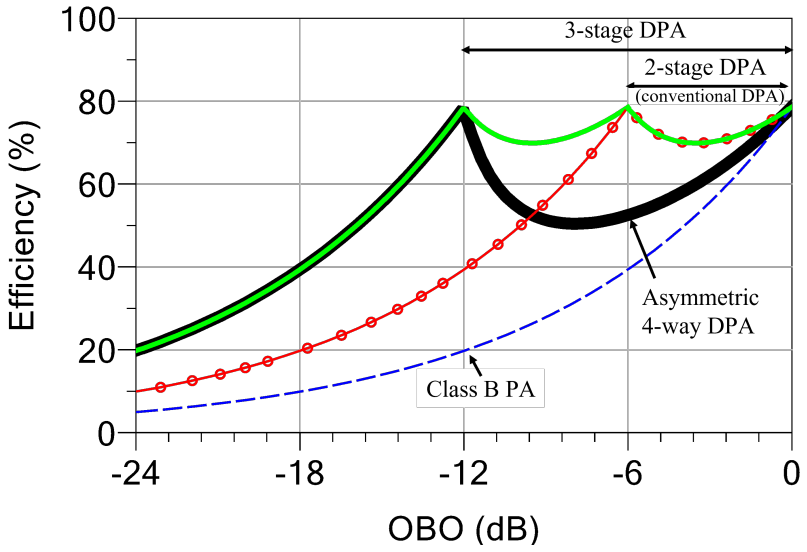


Figure 2.9: Efficiency of a class B PA, conventional DPA (also known as 2-stage 2-way DPA), a 4-way asymmetric DPA, and a 3-stage DPA.

Although N-way and multistage DPAs offer extended back-off efficiency, a major drawback of these techniques is the increased design complexity. For example a 3-stage DPA requires a three-way input splitter as well as complex output combining structures [14].

2.1.2. Load Modulated Balanced Amplifier

The concept of the load modulated balanced amplifier (LMBA), which was first proposed in [15] in 2016, has attracted much attention in recent years as it have demonstrated better ability to operate on wider frequency bands compared to DPAs. In an LMBA, as shown in Figure 2.10, a controlled signal power (CSP) is injected into the isolation port of the 90° coupler of the balanced amplifier (BPA). The CSP is added to the reflected power coming from the load; hence, modulates the load at each balanced device. Both 90° coupler and efficient amplifiers can be realised over a wide bandwidth, which potentially can result in the design of very wide-bandwidth power amplifiers with high efficiency at OBO.

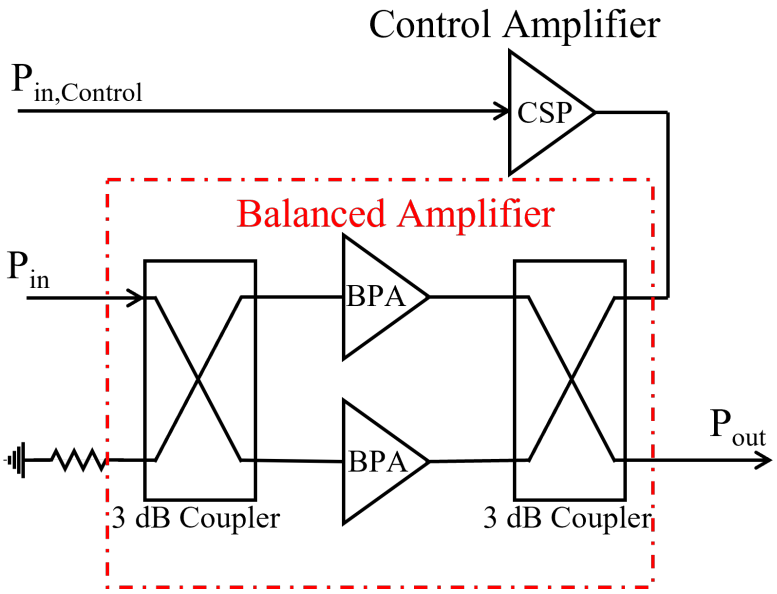


Figure 2.10: Block scheme of an load modulated balanced amplifier (LMBA). Instead of terminating the isolation port of the output 90° coupler, a controlled signal power (CSP) is injected to the power amplifiers.

To achieve high efficiency at OBO, initial works [15, 16] use the BPA as the main stage and the CSP as the auxiliary stage (turns ON only at higher power level). However, later work in [17] shows that there are some advantages, regarding the linearity, if the CSP is used as the main stage and the BPA as the auxiliary (so-called inverted-LMBA configuration).

2.1.3. Outphasing

The concept of outphasing technique was first presented by Chireix in 1935 [18]. The technique relies on generation of two constant amplitude phase-modulated (PM) signals which have the information of the original amplitude-modulated (AM) input signal. Figure 2.11 shows a block diagram of a basic outphasing PA, where the Signal Component Separator (SCS) is used to translate the input AM modulated signal into two constant amplitude PM signals with opposite phase. After amplification, the power combiner stage recombines the signals, thus the original AM modulation is retrieved. Since each amplification branch works with signals with constant-amplitude, they can operate efficiently at saturated power levels [1]. To achieve high efficiency at OBO it is critical to select a proper load compensation. The load compensation is achieved as part of the non-isolating output combiner network to correctly modulate load of the PAs as a function of power. Note that in outphasing architectures, non-isolating output combiners are preferred over isolating combiners because they do not waste power when the signals are not in phase [18, 19].

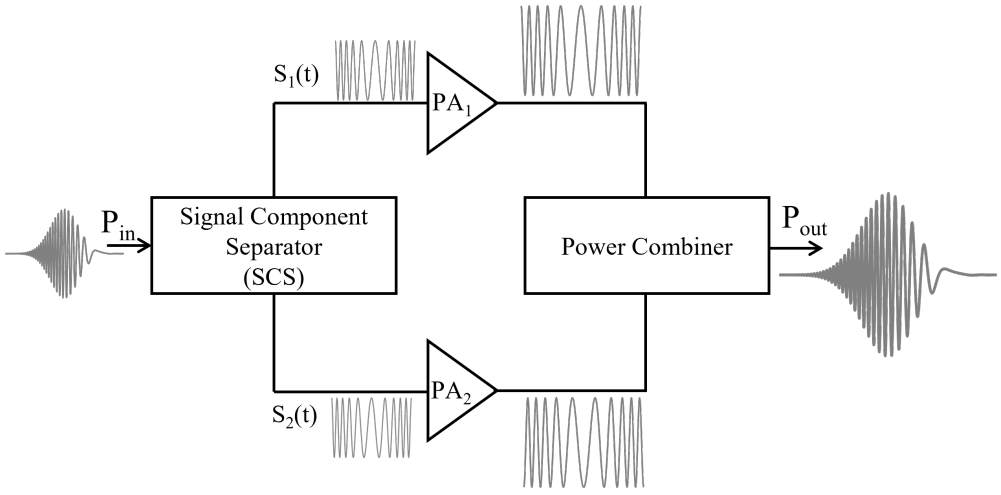


Figure 2.11: Block scheme of an outphasing PA. Signal Component Separator (SCS) is used to translate the input AM modulated signal into two constant amplitude PM signals with opposite phase. After amplification, the power combiner stage recombines the signals, thus the original AM modulation is retrieved.

Work in [20] provide a comparison between the ideal DPA and Chireix outphasing PAs

at 3, 6, and 9 dB OBO, where outphasing PA shows superior performance over the the DPA with minimal dip in the efficiency in the back-off region (as shown in Figure 2.12 for 9 dB OBO).

However, despite the potentially high performance of the outphasing with regard to efficiency, linearity and frequency bandwidth, they are less exploited by the industry and researchers compare to DPAs. This is mainly due to the difficulties, and complexity (the PM signals require bandwidths in the order of 10 times the bandwidth of the original signal), in the practical implementation of this architecture where the transistor's behaviour differs from the theoretical analysis [1, 21]. In addition, the outphasing PAs suffer from low power added efficiency (PAE) high thermal stress, and bandwidth limitation as discussed in [20].

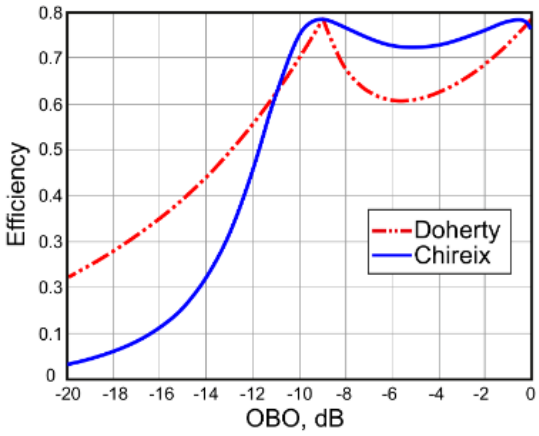


Figure 2.12: Comparison of an ideal asymmetric DPA and Chireix outphasing PA with 9 dB OBO [20]. Due to limitation in the practical implementation, despite the superior performance, the outphasing PAs are less exploited by the industry compare to Doherty PAs.

2.1.4. Envelope Tracking

The envelope tracking (ET) technique is based on a dynamic adaptation of the bias point to ensure that the amplifier is operating at its peak efficiency for instantaneous output power. Figure 2.13 shows a simplified schematic diagram of an ET PA.

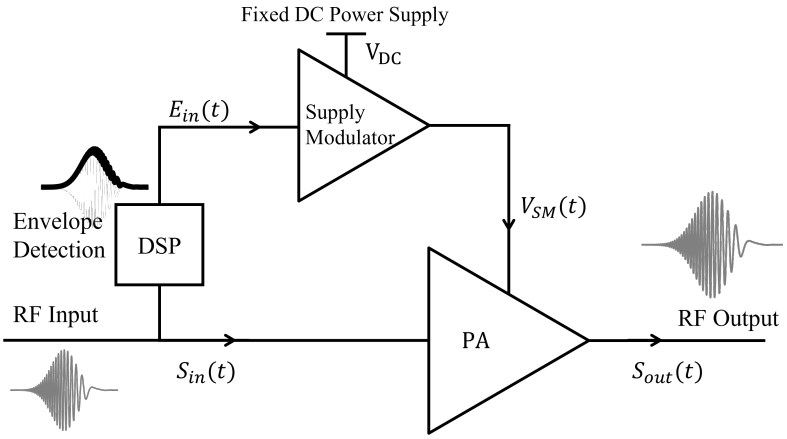


Figure 2.13: Overview of an Envelope Tracking architecture. Signal's envelopes information is fed to a modulator which adapts the supply voltage of the PA to the magnitude of input signal.

As shown Figure 2.13, the implementation of the ET relies on capturing and feeding the signal's envelope information ($E_{in}(t)$) to a supply modulator (SM) which then adapts the PA's supply voltage ($V_{SM}(t)$) to the signal's amplitude. This dynamic adaption of the supply voltage minimises the power loss and heat dissipation compared to the fixed supply voltage. Example in Figure 2.14 compares the voltage, power and efficiency of an ideal class B PA with and without envelope tracking [22].

Although the concept of the ET PAs is intuitive and simple, their practical implementation is relatively complex. The effectiveness of ET architectures is heavily reliant on correct detection of the envelope information which demands additional Digital Signal Processing (DSP) and the modulator which converts the constant DC voltage to the modulated supply voltage. The supply modulator (SM) must be highly efficient, low noise and broadband to benefit from the efficiency enhancement of ETs [23]. The efficiency of the SM needs to be taken in account to calculate the overall efficiency of an ET system. If the extra power consumed by the SM, and additional DSP, is significant, it might make the ET an impractical solution compared to other efficient PA architectures (e.g., DPA). As a rule of thumb the supply modulator is also required to have a bandwidth at least three times the

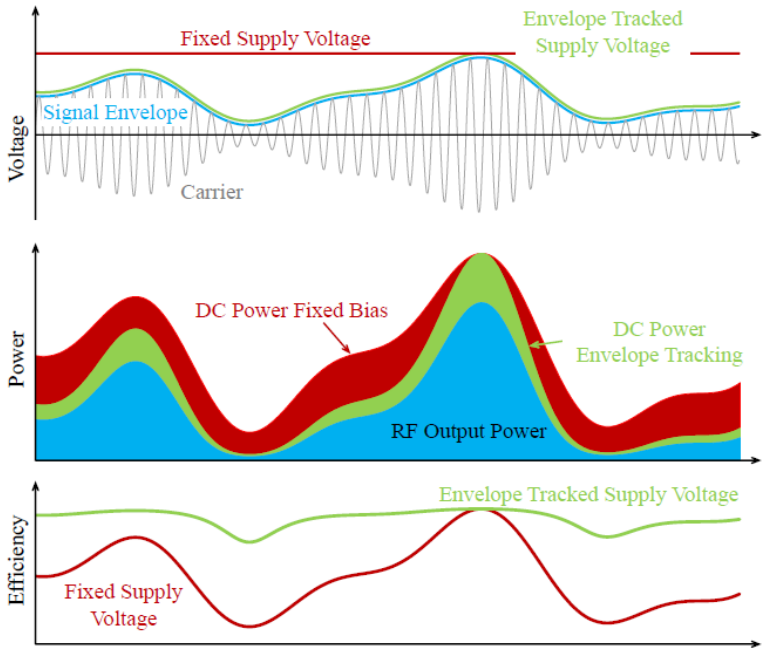


Figure 2.14: Demonstrating the benefit of envelope tracking. Comparison of voltage, power and efficiency of an ideal class B PA with and without envelope tracking [22].

RF channel bandwidth to provide linear amplification of the envelope [24].

One of the main challenges in the design of efficient supply modulators for ET systems is the requirement for fast and continuous tracking of the signal's envelope and adapting the DC supply voltage. It has been shown that for the switching mode supply modulators [25], the efficiency reduces as the switching speed increases [26]. One of the practical considerations to improve the efficiency of the SM is to adapt the DC supply voltage at a slower rate than the signals envelope modulation with the use of slew-rate reduction trajectories [27–29]. In a slew-rate reduction technique, instead of rapid adaption of the supply voltage to the fast-changing signal envelope, it is adapted to a slower-changing "envelope of the envelope" [28], as illustrated in Figure 2.15.

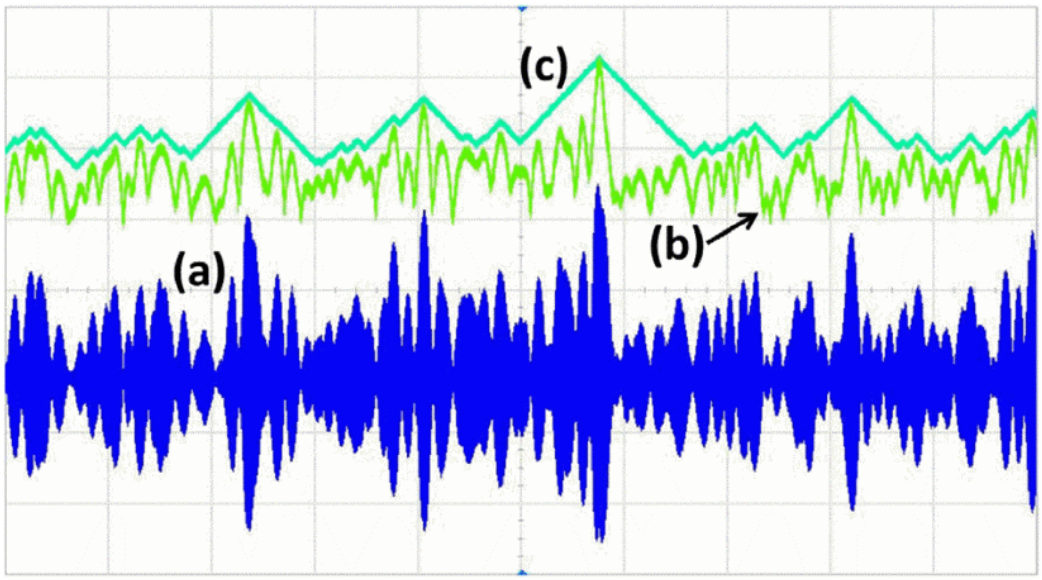


Figure 2.15: Slew-rate supply modulation trajectory. (a) OFDM 16-QAM RF signal at 2 GHz, (b) real envelope, and (c) slew-rate limited envelope [28]. To relax the speed requirement of the supply modulator, the slew-rate can be fed to modulator instead of faster changing signal envelope.

2.2. Doherty PAs and Average Power Tracking

The requirement of fast supply modulation can be further reduced by using discrete supply modulation [30–32] techniques. In this approach, instead of dynamic adaptation of the supply voltage to the signal's envelope, the PA's bias level is adjusted to the average power level (average power tracking (APT)) [33]. For example, using a lower DC supply voltage at low-traffic time and higher supply voltage at the peak-time when the data demand is higher. Work in [34] estimates that in an European country on average the number of active users can fluctuate from the minimum of nearly 2% to at the off-peak time (midnight to 6 am) to the maximum of 16% at the peak time (between 9 pm to 10 pm). Therefore, significant energy-saving can be made by adopting the power amplifier bias supply to this varying traffic load [35]. In fact, work in [36] emphasises that the APT techniques is one of the important "resource on-demand scaling" energy saving method for the modern 5G mobile base stations.

Currently, DPAs are the dominant PA-architecture for the mobile base stations [10]. With

the use of asymmetric (N-way) and multi-stage (N-stage) DPAs high efficiency at the higher OBO can be achieved. However, these techniques have their own limitation in terms of performance and complexity, as discussed in Section 2.1.1.1. The addition of the APT to the DPA has the potential to further advance the benefit of this efficient architecture. However, to fully utilise the benefit of APT in base stations it is critical to design DPAs which are capable to work at different DC bias voltages.

This concept has previously attracted attention in the literature. In an earlier paper [14] authors present their empirical findings based on a mixed-technology (LDMOS for the main and GaN for the auxiliary) DPA (790 MHz-960 MHz), where by adapting the DC supply voltage, different OBO performances were achieved. In addition, the DC supply voltage was modified to achieve optimal performance at different frequencies. Figure 2.16 shows the (a) efficiency and (b) gain performance of the DPA reported in [14].

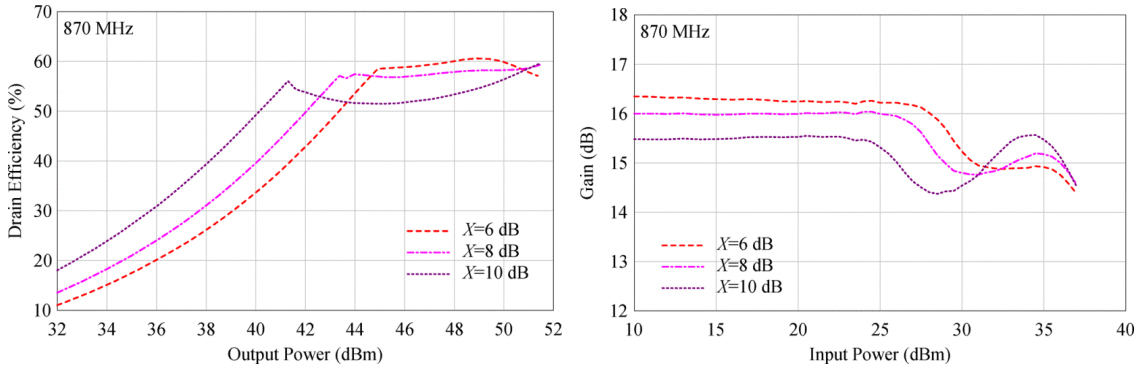


Figure 2.16: (a) efficiency and (b) gain performance of a re-configurable DPA from [14]. The drain bias of the main stage and gate bias of the auxiliary stage are modified to achieve peak efficiency at different BO level. (6, 8 and 10 dB).

Work in [37] presents the theoretical analysis explaining the effect of the gate (V_{gs}^{DC}) and drain (V_{ds}^{DC}) voltage on DPA's performance. It was shown, using measurement results of a GaN MMIC DPA (5.8 GHz-8.8 GHz), that by adapting the DC bias voltage efficiency performance of the DPA could be reconfigured. Although the main motivation of the paper is to use "modified" DC bias condition to achieve broader frequency bandwidth, the authors also

compare efficiency and gain performance of their DPA at different DC bias configurations. Similar to [14] it was shown that by adapting drain bias voltage of the main stage and gate bias of the auxiliary stage, different back-off efficiency can be achieved.

The work in [38] utilised the adaptive DC bias configuration for average power-tracking (APT) concept. The work presents measurement results of a 2-way DPA based on GaN technology at 1.94 GHz, capable of working at three different average output power levels (as shown in Figure 2.17). At each average power level same drain bias was used for both main and auxiliary stages. In addition to the drain bias, gate bias of the auxiliary was adjusted respective to the power level. A similar approach was used in [39] for a DPA with adaptive bias circuit for average power tracking based on a InGaP/GaAs hetero-junction bipolar transistor (HBT) technology at 1.9 GHz.

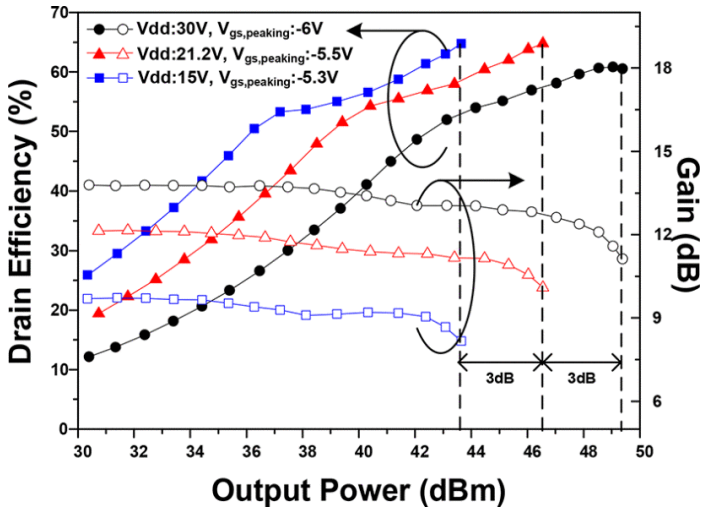


Figure 2.17: Efficiency and gain performance of a re-configurable DPA from [38]. Drain bias of both main and auxiliary (peaking) stages were adopted to the power level. At each power level the gate bias of the auxiliary stage was also adjusted to provide optimal Doherty performance.

2.3. Multi-Input-Single-Output Power Amplifiers

With the ever increasing complexity of advanced PA architectures it is now very common to use multiple transistors interacting non-linearly to achieve high performance over a wide

OBO level. For example Doherty PA which is almost a standard choice for the narrow-band base station transmitters [40] uses at least two different amplification stages (main and auxiliary PAs). Similarly, recently introduced load modulated balanced amplifier (LMBA) also uses multiple amplification stages [17].

Conventionally, passive splitters are used to divide the signals between the different stages from a single input signal, as shown in Figure 2.5 for a DPA. However, independently from the architecture of perspective, there are important advantages, from performance point of view, if multiple transistors can be driven by independent RF inputs, rather than derived from a single input by means of passive signal splitters. In fact, the so-called Multiple-Input, Single Output (MISO) PAs allow a "digital" signal splitting at baseband level, with the possibility of imposing non-linear relations between the several inputs which can help to optimise the RF performance [41], [42].

Work in [43] provide a detailed comparison between the single input ("analogue") and dual-input ("digital") DPA based on the measurement result of a proposed prototype using 10 W GaN Wolfspeed (Cree) [44] devices. The proposed DPA has output power of greater than 42 dBm with around 6 dB OBO. Figure 2.18 shows a comparison between the digital and analogue DPA at both peak an 6-7 dB OBO power levels.

As shown in Figure 2.18, significant improvement in the back-off region has been achieved as a result of using separate inputs. Work in [45] presents a re-configurable digital DPA with 6 dB OBO, where more than 49% efficiency was achieved over 1.5-2.4 GHz. Another digital DPA was also reported in [46] by the same research group with high efficiency performance over a very wide frequency range of 1-3 GHz.

Despite the evident advantages of digitally controlled separate inputs and degrees of freedom in using the PA, the search for an optimum configuration of the input signals becomes an interesting engineering problem. The search for the optimum input trajectory, either directly in measurement or with a circuit level simulation, can be time consuming. Therefore,

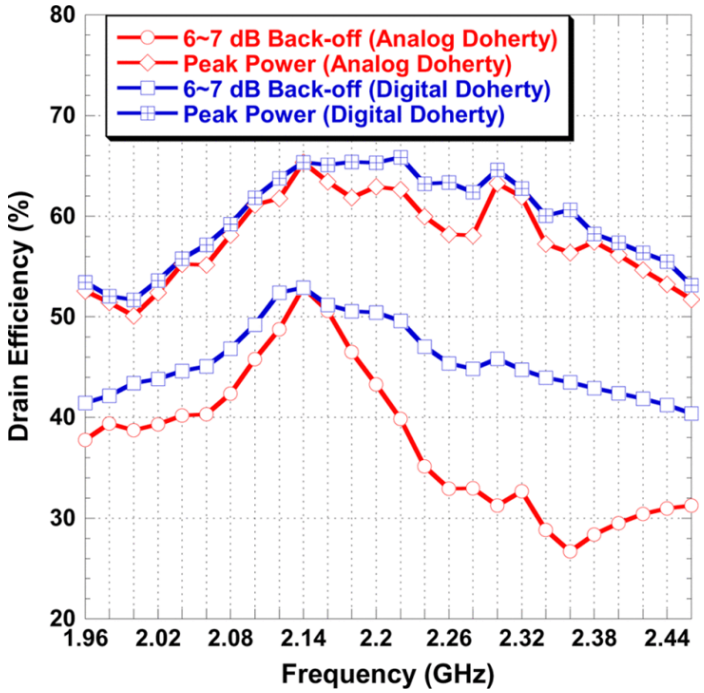


Figure 2.18: comparison of efficiency performance of a single input (analogue) and dual input (Digital) DPA [43] at the peak and 6-7 dB back-off power levels. The proposed prototype adopts 10 W GaN Wolfspeed (Cree) [44] devices, and shows an output power greater than 42 dBm, with 6 dB OBO efficiency larger than 40% over the 1.96–2.44 GHz bandwidth.

a behavioural model extracted on a few characterisation points that can still provide reasonable results on a denser exploration of the results is of great interest. For instance, work in [47] proposes a behavioural model based on expansion of multiple-input, multiple-output Voltera theory [48] for system level simulation of a PA with two input signal. In chapter 8, utilisation of the Cardiff nonlinear behavioural model for DISO PAs is discussed.

2.4. Nonlinear Transistor Models

An accurate and reliable transistor model with the ability to integrate within the computer-aided design (CAD) environment is a critical tool for the designers as it can significantly reduce the PA design's time and cost, compare to the more traditional "build and test" [49] design approach. The design of complex modern power amplifiers requires significantly more capability from the transistor models. For instance, a supply-modulated Doherty amplifiers requires the model to predict the device response under wide range of supply voltages, and capable of predicting the device response in class AB (for the main stage) as well as class C (for the auxiliary stage).

Development of nonlinear models for the new semiconductor technologies such as gallium-nitride (GaN) faces additional challenges as it needs to include the trapping effect [50] and extreme thermal behaviour. The performance of GaN technologies are susceptible to the variation in the supply voltage [51] and elevated temperature [52, 53].

Traditionally, transistors nonlinear models are classified in two general categories which are behavioural and physical models. In a behavioural model the measurement data are used to extract the model coefficients, without any prior knowledge about the physics of the device, which then can be used to mathematically describe the device behaviour. Physical models are based on the physics of the semiconductor device, where Boltzmann transport equation and the solution of the Poisson equation are derived to describe the carrier transport properties of the transistor and relate the physics of the device to its electrical behaviour [54, 55].

The physical models are suitable to predict the device performance as a function of material, geometry and process, and allows adjustment in the device without costly fabrication experiments. However, due to the lengthy analysis of "pure-physical" models (as it requires full 3-dimensional (3D) finite-element method (FEM) simulation [56, 57]), their application is often limited to the device studies and development [58]. For practical consideration and to reduce the computational intensity of the physical models, it is now common to use measurement data coupled with parameter extracted from physical property of the device to develop popular "state-function" models [59]; hence, even physical models are, at least partially, behavioural, blurring the line between behavioural and physical model [60].

The state-function (I-V, Q-V) based models (also referred to as "compact" models) are the most commonly used nonlinear models. These are arranged in a specific equivalent circuit topology in the time domain [59, 61]. Traditionally, DC and S-parameter measurements, and more recently large-signal measurements [62], are used to extract these "compact" large-signal models. However, the accuracy of these general-purpose models over all non-linear operating conditions is still a major concern for designers when working in the very challenging RFPA design domain [60, 63].

Currently, Cardiff university's Cardiff model [64] and Keysight's X-parameter model [65] are the industry leading behavioural models. The mathematical basis of these models was established on an accurate prediction of measurement data over a very limited operation domain surrounding the large signal operating point, LSOP. For example, set the DC bias point, the RF input drive level, the frequency, and the temperature.

Both compact and behavioural models have their own advantages and disadvantages. In particular, neither of these modelling solutions are capable to meet all the complexity, generality and accuracy requirement for advance PA design applications. The compact models are typically more general and can predict the device response over a wider LSOP at the cost of accuracy. On the other hand, the behavioural model can be very accurate over a limited LSOP. Therefore, to benefit from both generality of the compact models and

accuracy of the behavioural models, one can use different modelling solutions at different design stages. At the initial design stages more general compact model can be used to study the device performance over a wide range LSOP. At the later stages, more accurate behavioural models can be used to tune the design; hence, improving the chance of "first-pass" successful design [66, 67].

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CHAPTER 3

Load-pull Measurement Systems and Behavioural Device Modelling

The advancement of large signal measurement systems have enabled the users to collect critical information about the performance of their high frequency and high power transistors in a format which could be directly used within the CAD simulators. Mathematical behavioural models such as Cardiff model and X-parameters have been developed to provide means by which to use the data into the CAD simulator, with robust and accurate interpolation capability. This saves significant time in the measurement, and reduces the overall cost of design.

This chapter provides an overview of load-pull measurements and discusses the mathematical development of behavioural models, specifically the Cardiff model.

3.1. Load-pull Measurements

Historically, due to the lack of appropriate time-domain measurement systems, the standard measurement tools in the RF industry, generally, work in the frequency domain. The vector network analyser (VNA) is the well-known measurement tool which measures the S-parameters. S-parameters are widely used for characterisation and design of linear systems, where the DUT's performance is characterised under small stimulus signals [1–3].

However, S-parameters suffer from an inability to characterise the nonlinear behaviour of a device. Cripps in his book [4] explains the inefficiency of the S-parameters for the PA design

with an example, where he compares the compression characteristic of a class A amplifier at two different scenarios: "power match" (matched to the optimum load impedance from large-signal measurement) vs. "S-parameters" match (S_{22} match). This comparison is shown in Figure 3.1.

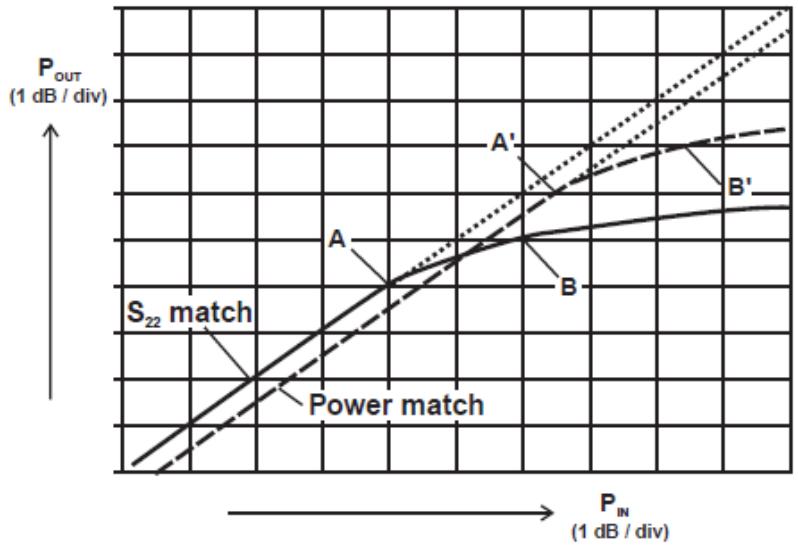


Figure 3.1: Compression characteristic for both S_{22} matched (solid line) and power matched (dashed line). Points A and A' are maximum linear power and point B and B' are the 1 dB compression points [4].

With reference to Figure 3.1, it can be noticed that at both 1 dB compression points (B and B') and maximum linear power points (A and A'), the power-match scenario delivers 2 dB more output power comparing to S_{22}-match. Although power-match scenario has less gain at lower input signal levels, it is preferable for the design of RFPAs as the maximum usage of the device deliverable-power capacity is desirable. Therefore, one can conclude that S-parameter characterisation are inadequate to describe large signal characteristic of power transistors [5].

Load-pull measurement is the alternative measurement system which can be used to overcome the shortcomings of the S-parameter measuring systems and support PA design. In a load-pull measurement set-up, the DUT's large signal behaviour is captured under vari-

ous load conditions. The collected data is usually presented in the form of contours on a Smith Chart to identify the optimal load to match the device, which is usually defined as a compromise between the often conflicting parameters such as efficiency, output power and linearity. For example, Figure 3.2 shows the 0.5 dB power and 3% efficiency contours for a 25 W GaN-on-SiC HEMT from Ampleon at 3.6 GHz. In this example, the "Optimum Load" refers to the point on the Smith Chart close to the maximum efficiency and power points where efficiency and power contours intersect.

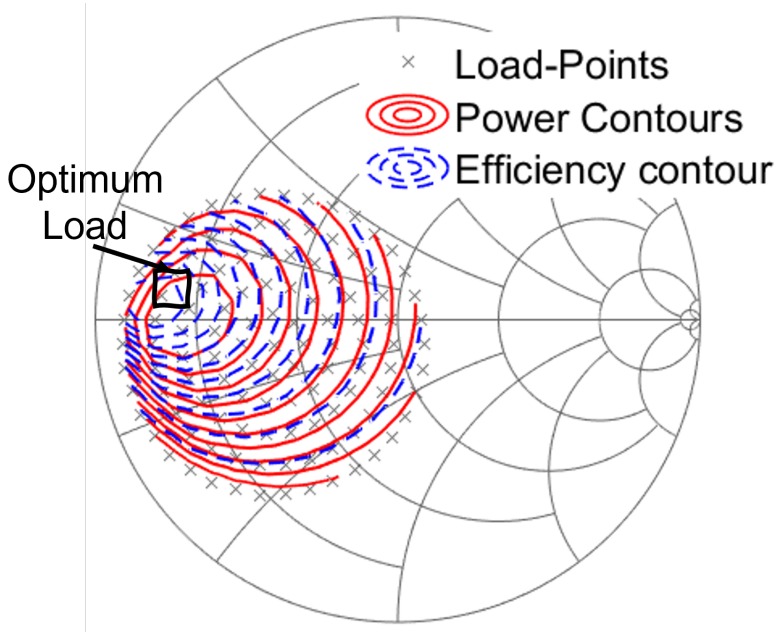


Figure 3.2: Load-pull contours of 25 W GaN-on-SiC HEMT device. The 0.5 dB Power and 3% efficiency contours from maximum of of 44 dBm and 60%, respectively. "Optimum Load" refers to the area on the Smith chart where maximum efficiency and power contours overlap.

The microwave measurement systems typically rely on measured travelling wave (A and B waves). Figure 3.3 shows the definition of A (incident) and B (reflected) travelling waves [6].

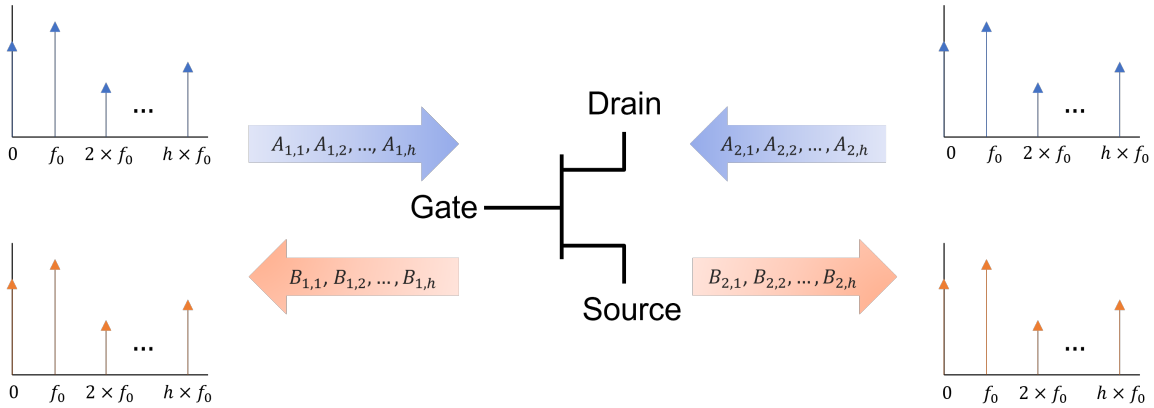


Figure 3.3: Illustration of A and B travelling waves on port one (Gate) and port 2 (Drain). f_0 is the fundamental frequency and $h \times f_0$ are the harmonic frequencies.

Note that the A and B waves are calculated from voltage and current, as shown in (3.1) and (3.2) [1].

$$A = \frac{V + Z_R I}{2\sqrt{R_R}}, \qquad B = \frac{V - Z_R{}^* I}{2\sqrt{R_R}} \tag{3.1}$$

$$I = \frac{A - B}{\sqrt{R_R}}, \qquad V = \frac{Z_R{}^* A + Z_R B}{\sqrt{R_R}} \tag{3.2}$$

where $Z_R = R_R + jX_R$ is the reference impedance, often set to $50\,\Omega$, which could also be a complex number.

In a load-pull measurement setup the DUT is excited by an input large signal stimulus signal at the fundamental frequency ($A_{1,1}$). This would result in generation of multi-harmonic incident and reflected waves at both input($A_{1,2\ldots h}$ and $B_{1,1\ldots h}$) and output($A_{2,1\ldots h}$ and $B_{2,1\ldots h}$). To load-pull a DUT means to present the DUT with a certain reflection coefficient ($\Gamma_{L,h} = A_{2,h}/B_{2,h}$). This can be achieved using the passive, active and hybrid (passive and active) load-pull systems.

3.1.1. Passive Load-pull

The concept of passive load-pull system is very intuitive to the PA designers where a passive load is presented at the output of the device. The passive tuner, which is typically a stub tuner impedance transformer as shown in Figure 3.4, is placed between the DUT and the 50 Ω measurement system impedance [7].

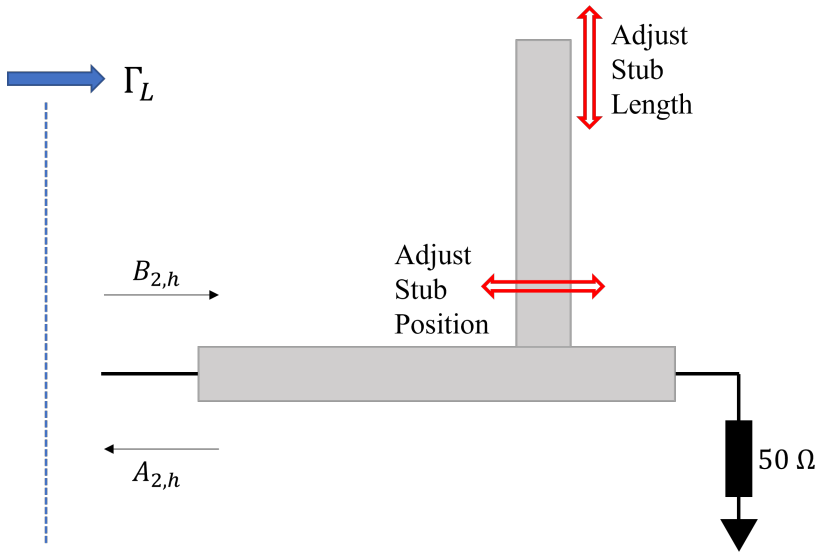


Figure 3.4: Stub tuner impedance transforming network (Passive Tuner). By adjusting the stub's length $|\Gamma_L|$ changes, and adjustment in the stub positioning would change the $\angle\Gamma_L$.

By changing the stub's length, the magnitude of the reflection coefficient $|\Gamma_L|$ is adjusted, and by varying the stub position its phase ($\angle\Gamma_L$) can be adjusted. In addition to fundamental frequency, harmonic load-pull control can be realised by adding two or more stubs [8]. To achieve improved repeatability and a computer-controlled system, the variation of the terminal impedance can be driven with precise stepper-motor-driven mechanical system [7, 9].

The main shortcoming of the passive load-pull systems is their limited load-pull range. High power DUT's have lower output impedance; hence, to capture their low optimum load impedance it is critical for the load-pull system to be able to cover the area close to the edge of the smith chart. Besides, efficient PA classes such as class B and J requires correct

termination of the 2nd harmonic which is ideally on the edge of Smith Chart ($|\Gamma| = 1$) [10]. Passive load-pull systems, however, inherently show insertion loss both within the tuners and the media between the tuner and the DUT (e.g. coaxial cables) [11, 12]. As shown in the example in Figure 3.5, due to the losses within the system, the optimum load of the 25 W DUT in Figure 3.2 cannot be targeted by a typical passive load-pull system.

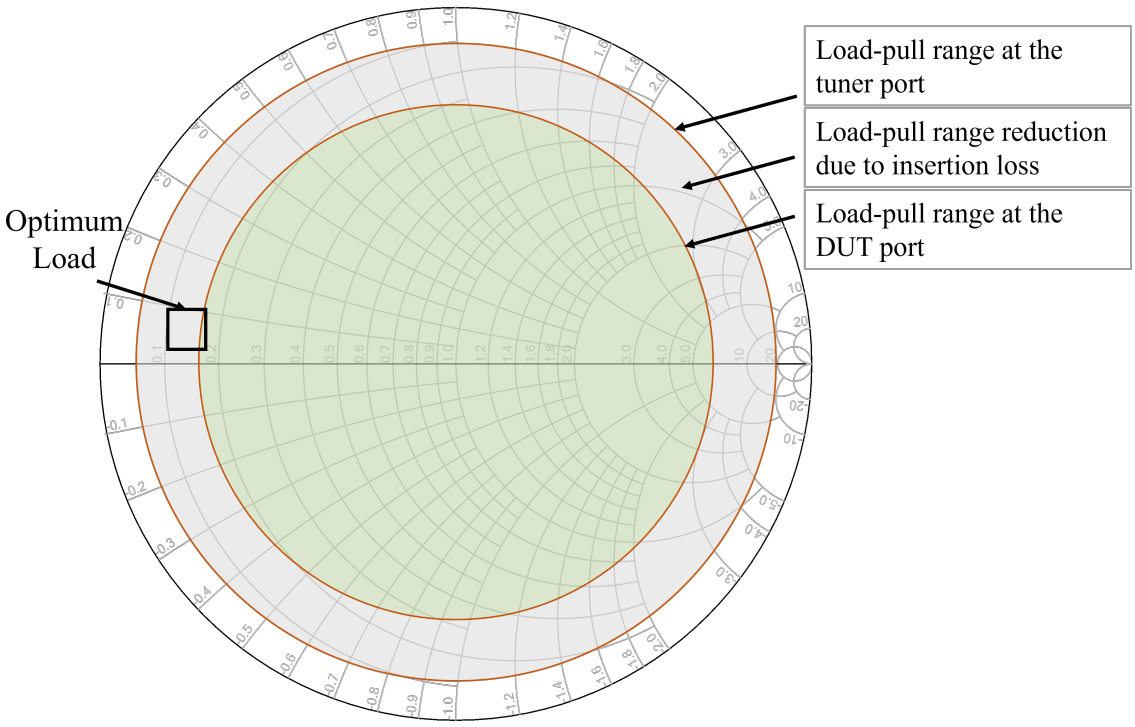


Figure 3.5: Limitation of passive load-pull systems. Effective load-pull range have been significantly reduced due to the insertion loss inherent to the system. The "Optimum Load" is the load-region where maximum efficiency and power contours overlap for the 25 W device in Figure 3.2.

3.1.2. Active Load-pull

The general principle of active load-pull is to overcome the losses in the system by amplifying the reflected signal '$A_{2,h}$'; hence, providing an unrestricted coverage of the impedance plane on a Smith Chart [13–15]. The concept of the active load-pull is perhaps not as intuitive as passive alternatives. To better understand the concept of active load-pull systems, it is

worth to consider the role of stub tuners in a passive system. In a passive load-pull system the reflected '$A_{2,h}$' is given as follows:

$$A_{2,h} = \Gamma \cdot B_{2,h} \tag{3.3}$$

Therefore, a different way of considering the role of stub tuner is that it provides a mean to adjust the magnitude and phase of the reflected $A_{2,h}$ wave [7]. Now consider replacing the stub tuner in Figure 3.4 by a simple circuit in Figure 3.6, representing an open-loop active load-pull system [16].

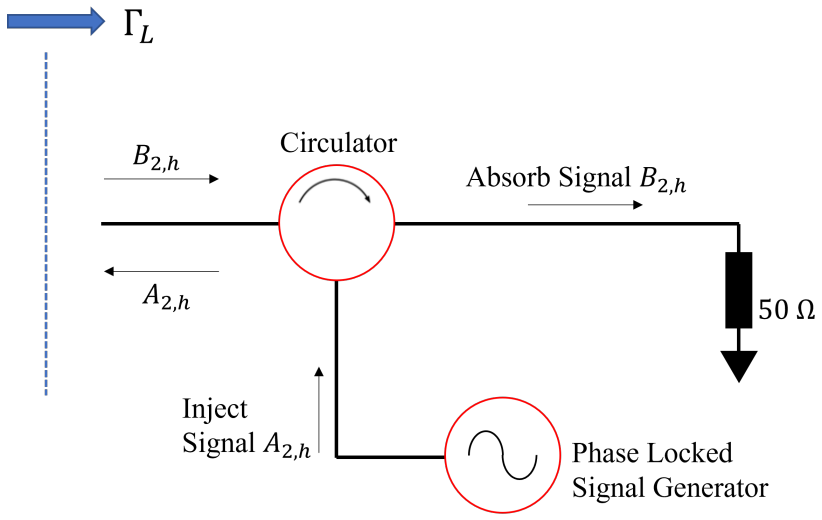


Figure 3.6: Active load-pull system. The circulator ensures 1) the incident $B_{2,h}$ signal is terminated at 50 Ω, and 2) the injected $A_{2,h}$ comes directly from the RF signal generator.

In Figure 3.6, the circulator ensures that 1) the incident $B_{2,h}$ is terminated to 50 Ω, and 2) the injected $A_{2,h}$ comes directly from the RF signal generator. Therefore, the role of the stub tuner, to vary the magnitude and phase of the $A_{2,h}$, can be replaced by simply varying the magnitude and the phase of the RF signal generator. The signal generator is phase locked to the input signal; hence, enables for an open-loop active load-pulling which eliminates the oscillation concerns of closed-loop systems [13, 14]. To achieve multi-harmonic load-pull,

multiple signal generators at each harmonic frequency are used, as shown in Figure 3.7. The driver PAs are used to amplify the injected signal amplitudes.

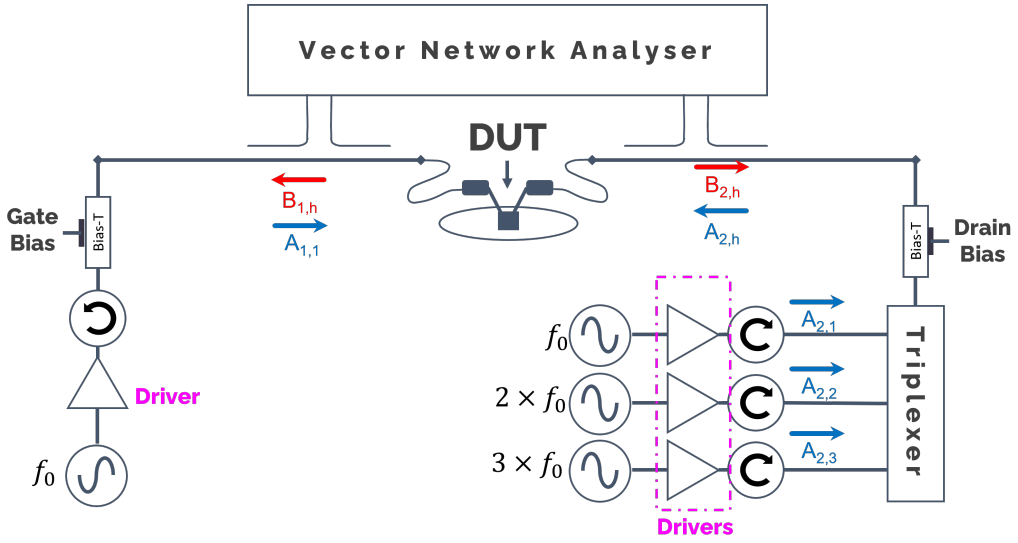


Figure 3.7: Multi-harmonic active load-pull system. Signal generators and driver PAs are used to generate and amplify the signals at each harmonics at the output.

The main disadvantage of the active load-pull systems is the cost of measurement set-up. As shown in Figure 3.7 multiple signal generator and driver amplifier are required to achieve multi-harmonic load-pull. In particular, high frequency and high power driver amplifiers can be very expensive. For instance, work in [17] characterises a GaN HEMT device using a three-harmonic active source-load pull set up with $f_0 = 900\,\text{MHz}$ where a total of 6 signal generators and 6 driver PAs were used.

3.1.3. Hybrid Load-pull

Hybrid load-pull systems, where a combination of active and passive load-pull are used in the same system, are an alternative load-pull solution. Different combinations of active injection and passive tuners can be used in a hybrid setup. For example, one can use both passive tuner and active injection to perform load-pull at fundamental frequency [11]. This solution is particularly desirable to load-pull high power DUT's to relax the power requirement of

the driver PA similar to the "pre-matching" technique used in [18], where authors considered a passive matching network on their test-fixture; hence, reduce the required magnitude of the injected $|A_{2,1}|$ signal to load-pull a 100 W device. Hybrid load-pull system can also be used to reduce the number of driver PAs in a multi-harmonic set-up. For instance, consider a scenario where passive load-pull is used for the fundamental frequency and active injection is used to load-pull at 2^{nd} harmonic [19].

3.2. Nonlinear Behavioural Modelling

The principle of behavioural modelling is based on the use of mathematical functions to fit a measured data without any knowledge about the physics of the device; hence, it can provide a relatively fast modelling solution purely based on the measurement while protecting the intellectual property (IP) of the manufacturer [20]. The real challenge in the field of behavioural modelling is to evolve an appropriate mathematical function which best represents the non-linear behaviour of a transistor. In other words, to model the load-pull data, the function ($F_{p,h}$) needs to predict the device response 'B' to the stimulus signal 'A', as it is illustrated by the general mathematical representation of "describing function" [21] in (3.4).

$$B_{p,h} = F_{p,h}(DC, A_{1,1}, A_{1,2}, \ldots, A_{1,h}, A_{2,1}, A_{2,2}, \ldots, A_{2,h}, \ldots, A_{p,1}, A_{p,2}, \ldots, A_{p,h}) \quad (3.4)$$

The subscript 'p' is the port index and 'h' is the harmonic index, referenced to the fundamental frequency 'f_0'. Note, visual illustration for the general describing function concept by showing a device response at the input ($B_{1,1\ldots h}$) and output ($B_{2,1\ldots h}$) to the multi-harmonic stimulus signals at both input ($A_{1,1\ldots h}$) and output ($A_{2,1\ldots h}$) was provided in Figure 3.3.

Referencing to (3.4), the describing function is very general and does not actually provide a mathematical insight in how to relate the A and B waves. In other words the mathematical

function ($F_{p,h}$) is unknown. However, its further development in [6] and introduction of the "Poly Harmonic Distortion (PHD)" modelling in 2006 was a major milestone in the development of the current nonlinear behavioural models. The PHD modelling provided a general polynomial framework based on the expansion of describing function which inspired the development of both currently industry-accepted behavioural models, Cardiff University's Cardiff model [22] and Keysight's X-parameters model [23].

The generality of the describing function in (3.4) comes at the cost of substantial complexity, as the device response is a nonlinear function of all the magnitudes and phases of stimulus phasors at every port. Modelling such a behaviour is impractical, if not impossible, in terms of data acquisition time, and model simulation speed [24]. Therefore, both X-parameter and Cardiff model have adopted different strategies, inspired by PHD modelling, to develop practical mathematical formulations (truncated polynomial formulation to reduce the number of coefficients) which are valid under a limited large signal operating point (LSOP). For example, a model formulation to predict the device response to an output stimulus signal $A_{2,1}$ at fixed input drive, and DC bias condition.

3.2.1. X-parameters

X-parameters represent an expanded version of S-parameters and utilise a frequency domain black-box behavioural modelling approach. Their development have been supported by Keysight, which has contributed to their more widespread adoption within the RF and Microwave industry [25].

To address practical considerations and minimise the number of model terms, the X-parameter incorporates the harmonic superposition principle, which is based on the PHD modelling approach [6]. This principle works under the assumption that all the generated harmonics are small in comparison with the amplitude of the fundamental stimulated signal A_{11}. The harmonic superposition principle is graphically illustrated in Figure 3.8.

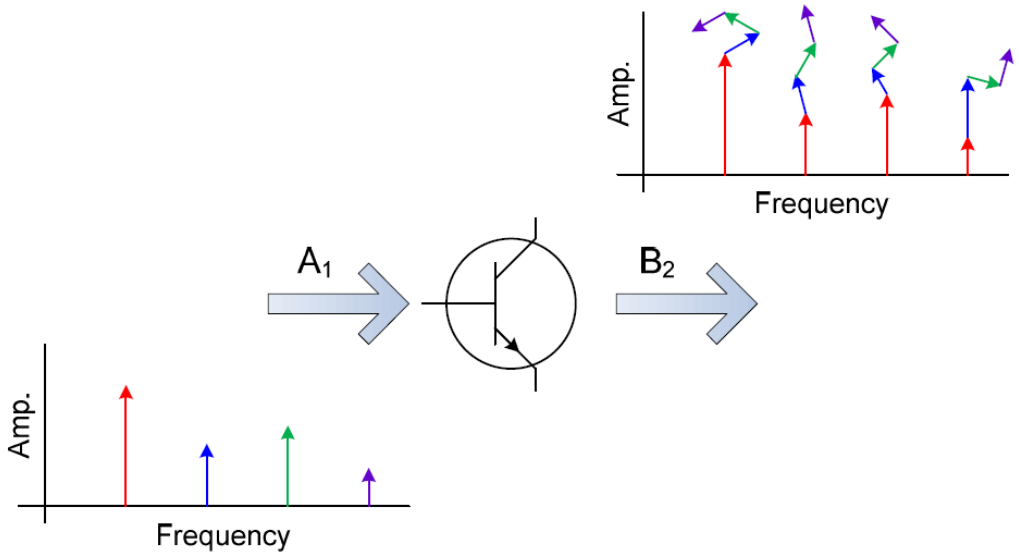


Figure 3.8: A visual representation of the harmonic superposition principle [6, 25].

The case in Figure,3.8 is a simplified scenario that only includes input $A_{1,h}$ and output $B_{2,h}$ signals, while neglecting the $A_{2,h}$ and $B_{1,h}$ signals. First, when considering only the input $A_{1,1}$, the corresponding red arrows indicate the generation of the first four components in $B_{2,h}$. When the $A_{1,1}$ remains constant, the addition of a relatively small $A_{1,2}$ (second harmonic at the input) causes a deviation in the output spectrum B_2 (blue arrows). The validity of this principle was experimentally verified for practical amplifier modes in [26].

Equation (3.5) [24] is a generalised X-parameter's equation that shows the device response '$B_{p,h}$' as being linear assumption of the stimulus '$A_{q,l\neq 1,1}$' and their conjugate (represented by the asterisk (*)) around the only large signal component '$A_{1,1}$'.

$$\begin{aligned} B_{p,h} = (\angle A_{1,1})^h \cdot X^{(F)}_{p,h}\left(DC, |A_{1,1}|\right) \\ \ldots, + \sum\nolimits_{(q,l)} X^{(S)}_{p,h,q,l}\left(DC, |A_{1,1}|\right) \cdot A_{q,l} \cdot (\angle A_{1,1})^{h-l} \\ \ldots, + \sum\nolimits_{(q,l)} X^{(T)}_{p,h,q,l}\left(DC, |A_{1,1}|\right) \cdot A^*_{q,l} \cdot (\angle A_{1,1})^{h+l} \end{aligned} \quad (3.5)$$

Note there are three sets of X-parameters $X^{(F)}_{p,h}$, $X^{(S)}_{p,h,q,l}$ and $X^{(T)}_{p,h,q,l}$. The subscript 'p' and 'h' correspond to the respective port and harmonic index of the response 'B'; 'q' and 'l' represent the respective port and harmonic index of the stimulus 'A'.

Equation (3.6) shows a more common, and practical, X-parameter formulation for fundamental only load-pull measurement at a fixed DC bias and $|A_{1,1}|$ level.

$$\begin{aligned} B_{2,1} = (\angle A_{1,1})^h \cdot X^{(F)}_{2,1}\left(DC, |A_{1,1}|\right), \\ \ldots, + X^{(S)}_{2,1}\left(DC, |A_{1,1}|\right) \cdot A_{2,l} \\ \ldots, + X^{(T)}_{2,1}\left(DC, |A_{1,1}|\right) \cdot A^*_{2,1} \cdot (\angle A_{1,1})^2 \end{aligned} \tag{3.6}$$

The $X^{(F)}_{2,1}$ is a distinct element as it handles the large-signal $A_{1,1}$, which falls outside of the harmonic superposition principle [25]. Note, as shown in (3.6), the model is normalised to the phase of the fundamental frequency at port 1 ($\angle A_{1,1}$). This phase normalisation establishes a time shift to ensure that each harmonic aligns when the phase of the fundamental is 0 °. Therefore, the model coefficients are only dependent on $|A_{1,1}|$, and not the $\angle A_{1,1}$. This not only simplifies the model's mathematical formulation, it also enforces the time-invariance of the model [24].

3.2.2. Cardiff Model

The Cardiff model started as a direct waveform look-up table (DWLUT) [27] in 2006 with the aim of providing a means for direct utilisation of load-pull measurement data into the nonlinear CAD simulators, such as the harmonic balance simulator. Equation (3.7) shows the DWLUT in 'A' and 'B' domain for fundamental-only load-pull [27, 28].

$$B_{p,h} = (\angle A_{1,1})^h \cdot K_{p,h}\left(|A_{1,1}|, DC, |A_{2,1}|, \frac{\angle A_{2,1}}{\angle A_{1,1}}, f_0\right) \tag{3.7}$$

As shown in (3.7)), model coefficients '$K_{p,h}$' were look-up parameters normalised to the phase of the input stimulus '$\angle A_{1,1}$' indexed against various parameters such as fundamental frequency 'f_0' , magnitude of the output stimulus signal '$|A_{2,1}|$', phase of the output stimulus signal '$\angle A_{2,1}$' and DC bias. The DWLT was unable to provide any relationship between the input and output of the device and it could only predict the measurement which it was based on.

3.2.2.1 Cardiff Model Development

In general, the transformation of the Cardiff DWLUT to the behavioural model is the result of an effort to eliminate as many of the look-up indexing terms as possible. First move toward the behavioural formulation was elimination of the phase vector '$\angle A_{2,1}/\angle A_{1,1}$' from indexing parameters as shown in equation (3.8) [22].

$$B_{p,h} = (\angle A_{1,1})^h . \sum_{n=-(w-1)/2}^{+(w+1)/2} K_{p,h,n}(|A_{1,1}|, DC, |A_{2,1}|, f_0) . \left(\frac{\angle A_{2,1}}{\angle A_{1,1}}\right)^n \tag{3.8}$$

Unlike X-parameter model, instead of using harmonic superposition, development of Cardiff model's polynomial formulation is based on mixing theory. The model accounts for the fact that when multiple CW harmonically related stimuli are injected into a multi-port non-linear system they interact ('mix'). Parameter 'w' is the mixing order which is directly used to calculate the phase exponent 'n'.

Next indexing parameter to be formulated was the magnitude of output stimulus ($|A_{2,1}|$). Tasker and Benedikt work in [2] proposed that the model coefficients extracted from equation (3.8) can be further developed to include the $|A_{2,1}|$ as explained in equation 3.9.

$$K_{p,h,n} = \sum_{m=?}^{m=?} L_{p,h,m} \cdot |A_{2,1}|^m \tag{3.9}$$

As it is noticeable from equation (3.9), at this stage, the value of parameter 'm' was not clear

and further work was required to fully incorporate the $|A_{2,1}|$ into the model formulation. Saini et el. work in [29] completes the formula in equation (3.9) by identifying the value of the magnitude related exponent 'm', as shown in equation (3.10).

$$K_{p,h,n} = \sum_{m=|n|}^{m=|n|+2r} L_{p,h}|A_{2,1}|^m \tag{3.10}$$

The variable 'r' is the magnitude indexing parameter which ranges from 0 to '$\frac{w-h}{2}$' (in practice, its maximum value is often forced to 1 $r_{max} = 1$). This was a huge milestone in the development of Cardiff behavioural model. The model coefficients were no longer indexed to neither phase nor magnitude of 'A_{21}', and could mathematically relate device output response to the stimulus signals. The general Cardiff behavioural model formulation, for fundamental load-pull only, is shown in equation (3.11) [25, 29].

$$B_{p,h} = (\angle A_{1,1})^h \cdot \sum_{r=0}^{r=(w-h)/2} \sum_{n=-((w-h)/2-r)}^{n=h+(w-h)/2} , \\ \ldots, K_{p,h,m,n}(|A_{1,1}|, DC, f_0) \cdot |A_{2,1}|^m \cdot \left(\frac{\angle A_{2,1}}{\angle A_{1,1}}\right)^n \tag{3.11}$$

Where $m = |n| + 2r$.

For the majority of the applications, the Cardiff model in (3.11) provides sufficient generality and interpolation capability. However, for more specific applications, e.g., predicting device performance at many frequency or input drive levels, further development was required to include these parameters into the model's formulation.

In this context, Koh's work in [30] includes a detailed study of the Cardiff model's coefficients relationship with respect to the frequency sweep with an aim of providing a frequency and size scalable model. It was shown, at the device intrinsic reference impedance, that the real part of the admittance domain (current and voltage) Cardiff model coefficients are

independent of the changes in frequency, while the imaginary parts have a linear relationship with frequency.

Note, based on the principles of physics, s, it is logical to describe the device behaviour in admittance domain (current response as a function stimulus voltage). However, as RF measurement systems rely on incident A and reflected B travelling waves [1], Cardiff model is often represented in travelling-wave domain (A, B domain). Equation (3.12)shows the Cardiff model in admittance domain.

$$I_{p,h} = (\angle V_{1,1})^h \cdot \sum_{r=0}^{r=(w-h)/2} \sum_{n=-((w-h)/2-r)}^{n=h+(w-h)/2} , \\ \ldots, D_{p,h,m,n}(|V_{1,1}|, DC, f_0) \cdot |v_{2,1}|^m \cdot \left(\frac{\angle V_{2,1}}{\angle V_{1,1}}\right)^n \quad (3.12)$$

Where the parameter V represents the voltage stimulus signal, the I is the device current response, and $D_{p,h,m,n}$ is the model coefficient in the admittance domain. Referencing to (3.12)), the model coefficients $D_{p,h,m,n}$ are indexed to the magnitude of the input voltage stimulus $|V_{1,1}|$. However, real world measurement systems are only capable to maintain a constant $|A_{1,1}|$; hence, maintaining a constant $|V_{1,1}|$ would be practically impossible.

To overcome this issue, Koh suggested an "indirect" extraction method where, Cardiff model's coefficients are, firstly, extracted in A and B domain, secondly, exported to Keysight's Advanced Design System (ADS) for a "voltage load-pull" (keeping the $|V_{1,1}|$ constant), finally, simulation results can be used to generate a new admittance domain model [30].

In a later study, Moure et al [31] proposed a new formulation for Cardiff model (as shown in (3.13) where $|V_{1,1}|$ was included into the formula and it no longer needed to be constant in the process of model extraction; hence, enabling direct extraction of the model's coefficient from load-pull measurement data.

$$I_{p,h} = (\angle V_{1,1})^h \cdot \sum_{t=0}^{t=(w-h)/2} \sum_{r=0}^{r=(w-h)/2-t} \sum_{n=-((w-h)/2-r)}^{h+(w-h)/2} , \\ \ldots, C_{p,h,m,n,x}(DC, f_0) \cdot |V_{1,1}|^x \cdot |v_{2,1}|^m \cdot \left(\frac{\angle V_{2,1}}{\angle V_{1,1}}\right)^n \quad (3.13)$$

Where '$x = |h - n| + 2t$' and the 't' is magnitude restricting indexing parameter of $|V_{1,1}|$. The $C_{p,h,m,n,x}$ is the general Cardiff model coefficients dependent of $|V_{1,1}|$. Similar formulation was proposed for A and B domain model as [31]:

$$B_{p,h} = (\angle A_{1,1})^h \cdot \sum_{t=0}^{t=(w-h)/2} \sum_{r=0}^{r=(w-h)/2-t} \sum_{n=-((w-h)/2-r)}^{n=h+(w-h)/2} , \\ \ldots, M_{p,h,m,n,x}(DC, f_0) \cdot |A_{1,1}|^x \cdot |A_{2,1}|^m \cdot \left(\frac{\angle A_{2,1}}{\angle A_{1,1}}\right)^n \quad (3.14)$$

where $M_{p,h,m,n,x}$ is the general Cardiff model coefficients dependent of $|A_1, 1|$. Note, this formula is limited in term of $|A_{1,1}|$ dynamic range it can model. This limitation and a new approach to include the $|A_{1,1}|$ is further discussed in Chapter 5.

At this stage, the generality of the Cardiff model was significantly improved. Depending on the application, one could generate a model capable of interpolating (or extrapolating) the load-pull data with regards to important parameters such as $|A_{1,1}|$, $|A_{2,h}|$, $\angle A_{2,h}$ and f_0. With regard to DC, however, it was still an indexing parameter and was not included into the Cardiff model (and also in X-parameter [32]) mathematical formulation. In the recent years, as supply-modulated PA architectures [33] have attracted much attraction, there is an increasing demand for DC-dependent models to help the designers to accurately simulate their PA's performance under various DC bias conditions. In this context, Chapter 4 dedicated to the inclusion of DC bias into the Cardiff model. This enables interpolation and extrapolation of the load-pull data with regard to DC bias; hence significantly reduces

quantity of the required load-pull data.

3.2.2.2 Spectral Analysis of Cardiff Model

Following a very specific measurement and data analysis procedure has always been a key element in the development of the Cardiff model formulation. For example, to include the phase of stimulus $\angle A_{p,h}$ (finding 'n') into the model formulation, specific data with fixed magnitude $|A_{p,h}|$ and sweeping phase from 0 to 2π were used [28, 34]. The process then was repeated in stepped values of magnitude (to find the values of 'm'), which resulted in a more general model formulation [29, 34]. As a result of this development, once the required complexity of the model is determined (or assumed) the model coefficients can be extracted from more traditional load-pull dataset using the least-mean-square technique [25].

For example, Figure 3.9 shows a comparison of the measured and modelled efficiency contours from a non-periodic (not recommended) load-pull pattern. Note, it is recommended, if possible, to use periodic load-pull (such as circular or spiral) patterns.

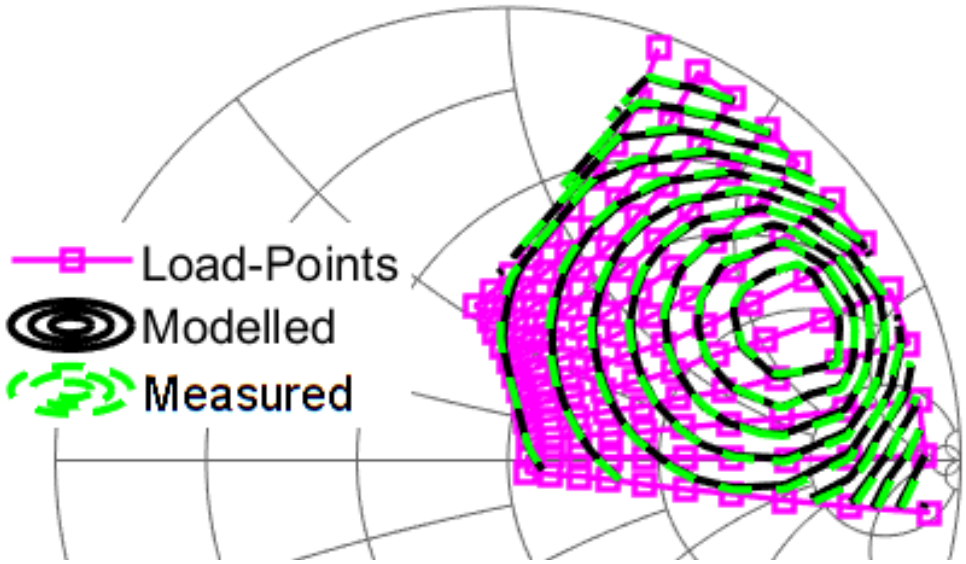


Figure 3.9: Cardiff model generated from non-periodic data (not recommended). Very good match between the measured and modelled efficiency contours (maximum efficiency is 48% and contour step is 5%). The load-pull data were collected from a 4 W GaN HEMT device from Ampleon. Original development of the Cardiff model was based on the data with periodic phase and stepped magnitude. However, the current formulation of the Cardiff model is capable to model the non-periodic load-pull data.

To use the current formulation of the Cardiff model, one needs to pre-define the mixing order 'w' which then determines the model complexity and number of coefficients. The recommended mixing order typically 3, 5 and 7 with corresponding 6, 10 and 14 coefficients [35] at f_0. Once the 'w' has been identified , the least-mean-square algorithm can be used to extract the Cardiff model coefficients $[k_{p,h}]$ from measured $[B_{p,h}]$ and $[A]$ matrices as shown in (3.15) [25].

$$[K_{p,h}] = \left([A]^H[A]\right)^{-1} \cdot [A]^H \cdot [B_{p,h}] \tag{3.15}$$

Referring to equation (3.15), after computing the coefficients, the $[B_{p,h}]$ matrix can be derived from the matrices $[A]$ and $[K_{p,h}]$ (i.e., $[B_{p,h}] = [A] \cdot [K_{p,h}]$). This derived matrix can then be compared to the measured $[B_{p,h}]$ using the Normalized Mean Square Error (NMSE).

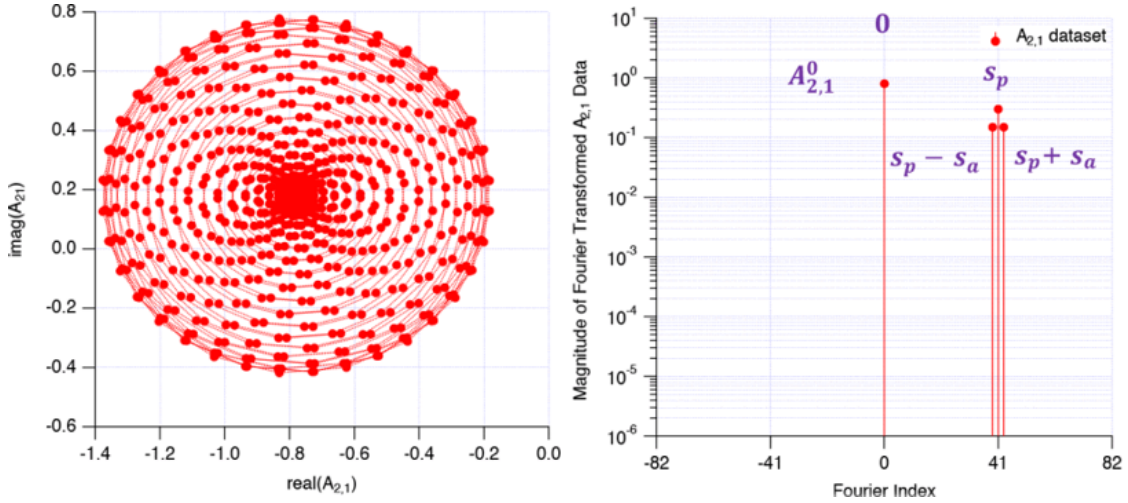
The NMSE serves as a guide for identifying the appropriate model complexity. Typically, the selection of model complexity is determined by comparing the calculated NMSE of models extracted at different complexities [35], and there is no established systematic method for justification.

Referring to Equation 3.15, after computing the coefficients, the $[B_{p,h}]$ matrix can be derived from the matrices $[A]$ and $[K_{p,h}]$. This derived matrix can then be compared to the measured $[B_{p,h}]$ using the Normalised Mean Square Error (NMSE). The NMSE serves as a guide for identifying the appropriate model complexity. Typically, the selection of model complexity is based on comparison of the calculated Normalised Mean Square Error (NMSE) of the models extracted from different complexity [35], and there is no systematic way to justify it.

However, Tasker in his recent work [36] proposes a promising "Robust" extraction strategy as an alternative to mixing order. Similar to initial development of the Cardiff model, the proposed method relies on carefully tailored load-pull dataset. The load-pull dataset were generated within the CAD simulator from magnitude and phase modulated $A_{2,1}$ trajectory in (4.12). The Fourier transformed spectral analysis of this tailored data can clearly identify the correct model coefficients, and minimum size of the dataset to extract a robust model.

$$A^{i}_{2,1} \quad = \quad A^{0}_{2,1} \; + \; \frac{A^{\Delta}_{2,1}}{2}\left(1 + cos\left(S^{\alpha}_{2,1}\frac{i}{N}\right)\right)\left(cos\left(S^{\beta}_{2,1}\frac{i}{N}\right) + jsin\left(S^{\beta}_{2,1}\frac{i}{N}\right)\right). \quad (3.16)$$

Where the $S^{\alpha}_{2,1}$ and $S^{\beta}_{2,1}$ are the amplitude and phase modulation rate about a reference $A^{0}_{2,1}$. The 'N' is the number of measurement and 'i' is the sweeping parameter ranging from '0' to '$N-1$'. Figure 3.10 shows the $A_{2,1}$ trajectory from [36] with $S^{\alpha}_{p,h} = 2$, $S^{\beta}_{2,1} = 41$ and $N = 739$.



(a) (b)

Figure 3.10: (a) Dataset modulated $A_{2,1}$ trajectory;(b) result of the Fourier transforming this data. The $S^{\alpha}_{p,h} = 2$, $S^{\beta}_{2,1} = 41$ and $N = 739$ [36].

As shown in Figure 3.10, the Fourier transformation of this tailored $A_{2,1}$ trajectory results in clear spectral lines at 0, $S^{\beta}_{2,1} = 41$ and $S^{\beta}_{2,1} \pm S^{\alpha}_{p,h}$. By analysing the resulting $B_{2,1}$ "spectral clusters" at $n \times S^{\beta}_{2,1}$ locations, the correct model terms can be identified as shown in Figure 3.11.

As shown in Figure 3.11, to target -60 dBc of accuracy, eleven (m,n) pairs are selected. First, the spectral lines at $n \times S^{\beta}_{2,1}$ locations with magnitude higher than -60 dBc were identified, which determine the parameter 'n'. Then, using $m = |n| + 2r$, the corresponding 'm' value were calculated to model the spectral lines at $\left((n \times S^{\beta}_{2,1}) \pm (r+1) \cdot S^{\alpha}_{p,h}\right)$ locations. Note, -40 dBc of accuracy can be achieved by using only the model terms (0,0), (1,-1) and (1,1).

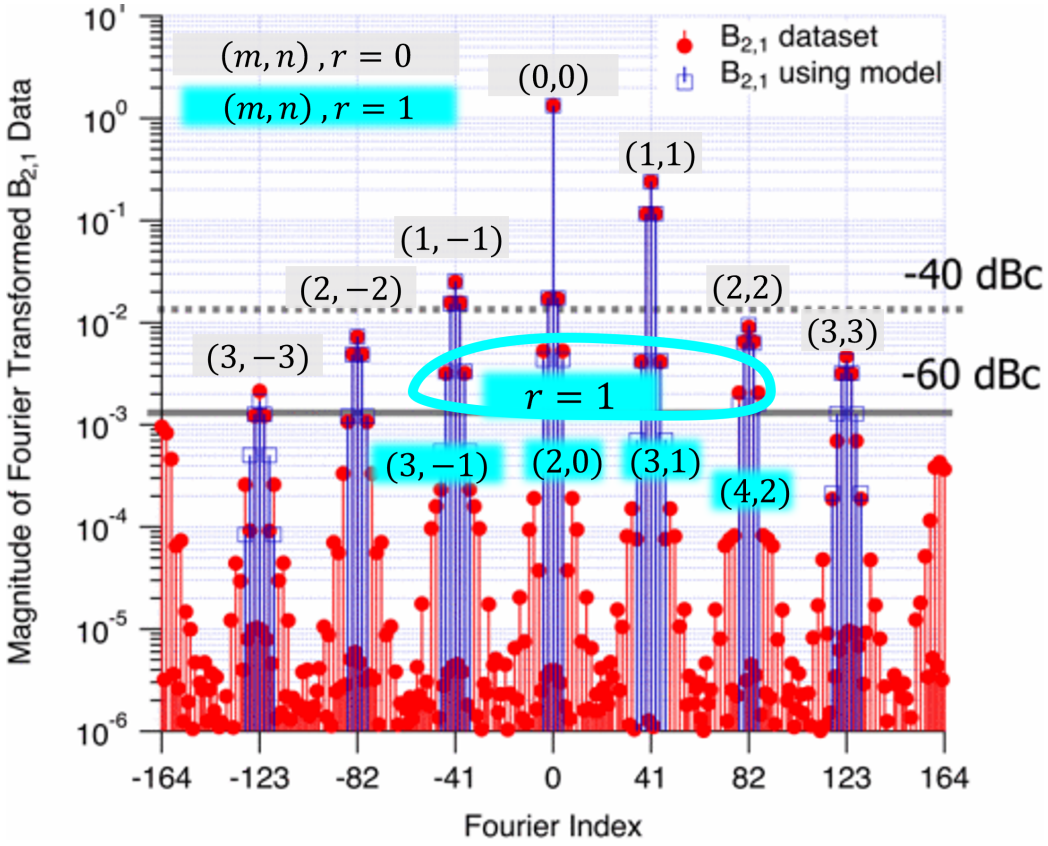


Figure 3.11: $B_{2,1}$ response to the $A_{2,1}$ trajectory in Figure3.10 [36]. To target -60 dBc model accuracy, eleven (m,n) pairs are selected. First, the spectral lines at $n \times S^{\beta}_{2,1}$ locations with magnitude higher than -60 dBc were identified. Then, using the $m = |n| + 2r$ the corresponding 'm' value were calculated to model the spectral lines at $(n \times S^{\beta}_{2,1}) \pm (r+1) \cdot S^{\alpha}_{p,h}$ locations. Note, -40 dBc of accuracy can be achieved by using only the model terms (0,0), (1,-1) and (1,1).

Using this method, in addition to robust extraction of the model coefficients one can identify the minimum size of the dataset. For example, referencing to Figure 3.11, there is a large space between the "modelled" spectral clusters (the red area between the blue spectral clusters which were not used to extract the model coefficients). Therefore, smaller $S^{\beta}_{2,1}$ value can be used to reduce the space between the spectral clusters; hence, identify the minimum required size of the dataset which does not effect the model accuracy. For this dataset, it was shown that size of the dataset could be reduced from N=739 to N=57 with maximum deviation of 2% in the model coefficient [36].

This robust extraction procedure is based on the tailored $A_{2,1}$ data with clear spectral lines. However, in practice, load-pull measurement systems are developed to target pre-selected Γ_L and not the $A_{2,1}$ trajectory. As a result, the $A_{2,1}$ trajectory is disturbed and additional spectral lines are produced. This issue can be overcome in active load-pull systems by developing algorithms which enable users to select an "A-pull" pattern (and not a load-pull pattern). Note, this would also significantly increase the speed of active systems as there is no iteration involved to target a certain pre-defined Γ_L. With regard to passive load-pull, however, perhaps conscious compromises have to be made to extract the model terms and one might struggle to truly relate the spectral clusters to physics of the device.

3.2.3. Behavioural models suitable for Doherty PA design

Suitability of the behavioural models have been mostly approved for the PA classes with more than 180° of conduction angle (e.g. class AB, J, and F) [2, 6] in high power region. Hence, modelling the small signal behaviour was not critical (except for stability analysis). For Doherty PA design, however, the model is required to predict the small-signal response of the auxiliary stage (biased in class C) where load-pull measurement is not feasible. This is mainly due to the limitation of the measurement systems which, in principal, cannot perform load-pull when there is no significant output current. Note, one possible solution to this problem can be development of A-pull systems [36] which are not iterative and enable users to record the DUT's response to the $A_{2,1}$ trajectory with no input stimulus signal ($|A_{1,1}|$=0).

Recent work in [37], proposes a new behavioural modelling method for Doherty PA design applications using an Artificial Neural Network (ANN). In their approach, authors collected simulated load-pull data from the commercially-available model in ADS. Then, the data was mathematically manipulated (by embedding the DUT's S-parameter data in the OFF stage) prior to ANN training so that the model was capable to predict the $B_{2,1}$ as a linear dependent of $A_{2,1}$ when $A_{1,1} = 0$. MATLAB toolbox was used to extract the ANN model

parameter which then implemented in ADS through an FDD block (very similar to Cardiff model implementation [25]), which enables the creation of nonlinear components based on user-defined equations, in the frequency domain. The proposed model is compared with the simulation results of the commercially-available model for a DPA, where high accuracy was achieved.

Chapter 5 is dedicated to development of Cardiff model which is suitable for DPA design. The model then was verified via design and fabrication of an asymmetric DPA which is covered in Chapter 6.

3.3. Thermal Modelling

Despite all the efforts by the industry to improve the PA's efficiency, inevitably a large amount of the energy is wasted in the form of heat, which can result in an increase in the device temperature. It is well known that elevated temperatures adversely affect RF performance parameters such as gain, output power, and linearity. For this reason, thermal management systems are typically used to both monitor and remove the excess heat generated by the RFPAs. In this way, a reasonably constant operating temperature is maintained [38].

Under certain conditions, effective thermal management may not be feasible, and the RFPA will have to operate at a higher temperature. This happens when, for example, compactness is desired or the ambient temperature is extremely high and cooling the device to a suitable temperature is either impossible or expensive (e.g. extreme high ambient temperature in Lut Desert in Iran (70.7 °C), and Death Valley in California (56.7 °C) [39]). In these harsh environments, it is critical to select a semiconductor technology that can withstand these high-temperature conditions.

In recent years, the high power density and efficiency of GaN HEMTs at microwave frequencies have made them a preferred technology for high-frequency and high-power PAs.

Moreover, GaN HEMTs are also remarkably suitable for high-temperature applications [40], even though their performance decreases at elevated temperatures [41], [42]. Hence, in order to design an RFPA, it is essential use a nonlinear CAD simulator that can predict the device behaviour at various temperatures.

With regard to temperature, to improve the accuracy of the nonlinear models, a "coupled" electrothermal model approach has been considered [43, 44]. In this approach, the large signal equivalent-circuit ("compact") model is coupled with a physics-based electrothermal model. While physics-based temperature-dependent models can be highly accurate, they are computationally demanding [45]. To reduce the computation intensity, work in [46] extracts a behavioural model from the full 3-dimensional (3D) physics-based finite-element method (FEM) simulation results, which was then coupled with a compact nonlinear model [47]. In this approach, only the behavioural model coefficients are imported into the nonlinear CAD simulator (with temperature being a look-up indexing parameter); hence, significantly improving the computational-efficiency of the temperature-dependent model. To use these physics-based methods, however, information about the geometry and material properties of the DUT is required.

An alternative modelling solution is to use temperature-dependent behavioural models. Since they are extracted directly from the measurement data, prior knowledge about the physical property of the DUT is not required. This approach can provide a fast an accurate modelling solution to simulate the DUT's performance at various temperature conditions. However, the current mathematical formulation of both the Cardiff model and X-parameters treats temperature variation as a look-up indexing parameter. Therefore, these models are unable to interpolate or extrapolate the measurement data. A temperature-dependent X-parameter model of a RFPA presented in [48] relies on the interpolation capability of the CAD simulator.

A novel expansion of the Cardiff model polynomial formulation incorporating temperature variation is presented in Chapter 7. Note, it is well established in the literature to

consider the thermal effect as a long-term memory [9, 49, 50], when its dynamic behaviour is considered. Our modelling approach instead considers the steady-state temperature of the DUT, where the model is capable of predicting the power and efficiency degradation caused by elevated temperature.

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CHAPTER 4

Including DC Supply Voltage into the Cardiff Model Formulation

The DC bias has always been a key factor in the design of power amplifiers (PAs). For example, different PA classes (such as A, B, AB and C) are defined based on their DC quiescent point, which is achieved by varying the gate voltage. In recent years, supply modulated power amplifiers have gained popularity as a way to improve efficiency in next-generation mobile base stations [1]. To design these complex PA architectures, accurate transistor models that can predict device behaviour under different bias conditions are crucial.

Developing a DC-dependent model using the current Cardiff model formulation [2] requires the execution of load-pull measurements at each DC bias point, which can be a very time-consuming process depending on the number of bias points needed. The new DC-dependent Cardiff model presented in this chapter significantly improves time-efficiency and effectiveness by allowing for the interpolation of load-pull data with regards to DC bias, avoiding the need for these time-consuming measurements. The new formula was developed based on the general mixing theory which was then verified through experimental data of a GaN-on-SiC HEMT device.

4.1. Mathematical development

The Cardiff model is founded on the principle of mixing theory [3], which has been utilised as a basis for the refinement and enhancement of the model's generality. In order to incorporate a DC bias sweep into the model, we will also use this established method and initiate our analysis with the general mixing theory equation (4.1). This equation serves as a fundamental framework for the development of the model.

$$I = \sum_{w=0}^{w=order} \sum_{u=0}^{u=w} A_{u,(w-u)} \left(v_{gs}^{RF}\right)^{u} \left(v_{ds}^{RF}\right)^{(w-u)} \tag{4.1}$$

Where 'I' is the device current response to input (v_{gs}^{RF}) and output (v_{ds}^{RF}) RF voltage stimulus. Model complexity, and number of coefficients ($A_{u,(w-u)}$), is determined by the mixing order 'w'. It is apparent that only RF contribution is included in (4.1).The contribution of the DC bias can be incorporated into the mixing equation as:

$$I = \sum_{w=0}^{w=order} \sum_{u=0}^{u=w} C_{u,(w-u)} \left(V_{gs}^{DC} + v_{gs}^{RF}\right)^{u} \left(V_{ds}^{DC} + v_{ds}^{RF}\right)^{(w-u)} \tag{4.2}$$

Where V_{gs}^{DC} and V_{ds}^{DC} are gate and drain DC bias voltage, respectively. The $C_{u,(w-u)}$ is the model coefficient. Equation (4.2) can be further expanded to (4.3) by including the mixing relationship between the RF and DC stimulus at both input and output of the device,

$$\begin{aligned} I = & \sum_{w=0}^{w=order} \sum_{u=0}^{u=w} C_{u,(w-u)}, \\ & \ldots, \left\{ \left\{ \sum_{x=0}^{x=u} C_{x}^{gs} \left(V_{gs}^{DC}\right)^{x} \left(v_{gs}^{RF}\right)^{u-x} \right\} \left\{ \sum_{y=0}^{y=(w-u)} C_{y}^{ds} \left(V_{ds}^{DC}\right)^{y} \left(v_{ds}^{RF}\right)^{(w-u)-y} \right\} \right\}. \end{aligned} \tag{4.3}$$

The (4.3) can be rearranged to separate the DC and RF contribution as:

$$I = \sum_{y=0}^{y=w} \sum_{x=0}^{x=y} \left\{ \sum_{u=0}^{u=u_{max}} \sum_{v=u}^{v=v_{max}} G_{y,u,(v-u)} \left(V_{gs}^{DC}\right)^{u} \left(V_{ds}^{DC}\right)^{(v-u)} \right\} \left(v_{gs}^{RF}\right)^{x} \left(v_{ds}^{RF}\right)^{y} \tag{4.4}$$

The coefficients of the Cardiff model are commonly extracted at a fixed input drive level ($v_{gs}^{RF} = constant$). At a fixed drive level the mixing equation in (4.4) can be simplified as:

$$I = \sum_{y=0}^{y=w} \sum_{x=0}^{x=y} \left\{ \sum_{u=0}^{u=u_{max}} \sum_{v=u}^{v=v_{max}} G_{y,u,v} \left(V_{gs}^{DC}\right)^{u} \left(V_{ds}^{DC}\right)^{v} \right\} \left(v_{ds}^{RF}\right)^{y} \tag{4.5}$$

Referencing to (3.11) and (3.12), the contribution of RF stimulus has been previously included into the Cardiff model. Therefore, by replacing the RF part of the (4.5) with the admittance domain Cardiff model formulation, a new Cardiff model formulation can be generated, as shown in (4.6), where both V_{gs}^{DC} and V_{ds}^{DC} are included into the model formulation.

$$I_{p,h} = (\angle V_{1,1})^{h} \sum_{r} \sum_{n} \left\{ \sum_{u=0}^{u=u_{max}} \sum_{v=u}^{v=v_{max}} R_{p,h,m,n,u,v} \left(V_{gs}^{DC}\right)^{u} \left(V_{ds}^{DC}\right)^{v} \right\}, \\ \ldots, |V_{2,1}|^{m} \left(\angle \frac{V_{2,1}}{V_{1,1}} \right)^{n} \tag{4.6}$$

The new model coefficient '$R_{p,h,m,n,u,(v-u)}$' is dependent on the DC bias voltage. The maximum fitting orders for the gate and drain DC voltage are represented by u_{max} and v_{max}, respectively. Similar to the RF mixing order 'w', which is typically determined based on the experimental data to fit a specific load-pull dataset, the DC fitting orders must also be empirically investigated. This will be discussed in the following section.

Equation (4.7) shows the new DC-inclusive Cardiff model, after transforming the RF part to the A,B domain which is more consistent with the experimental data. We recognise in

this transformation the model coefficients '$L_{p,h,m,n,u,(v-u)}$' and complexity might be different from the admittance model's equivalent.

$$B_{p,h} = (\angle A_{1,1})^h \sum_r \sum_n \left\{ \sum_{u=0}^{u=u_{max}} \sum_{v=u}^{v=v_{max}} L_{p,h,m,n,u,v)} \left(V_{gs}^{DC}\right)^u \left(V_{ds}^{DC}\right)^v \right\}, \\ \ldots, |A_{2,1}|^m \left(\frac{\angle A_{2,1}}{\angle A_{1,1}}\right)^n. \quad (4.7)$$

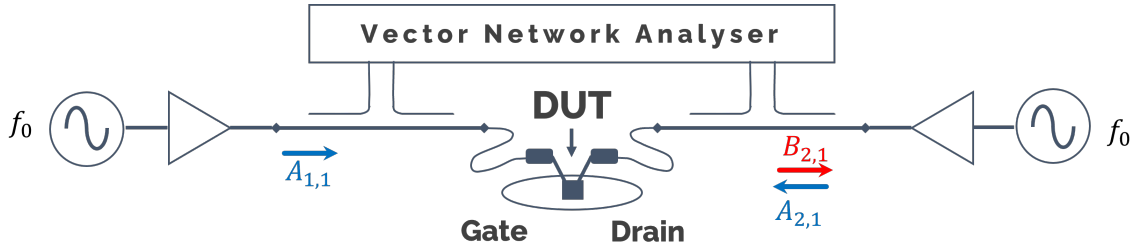
In theory, the new DC-inclusive Cardiff model formulation in (4.7) is capable of interpolation of load-pull data with respect to the DC bias voltages, thereby significantly reducing the required amount of the load-pull measurement data. However, the effectiveness of these new formulas must be verified using actual load-pull measurement data.

4.2. Verification of new formulation using measured load-pull data

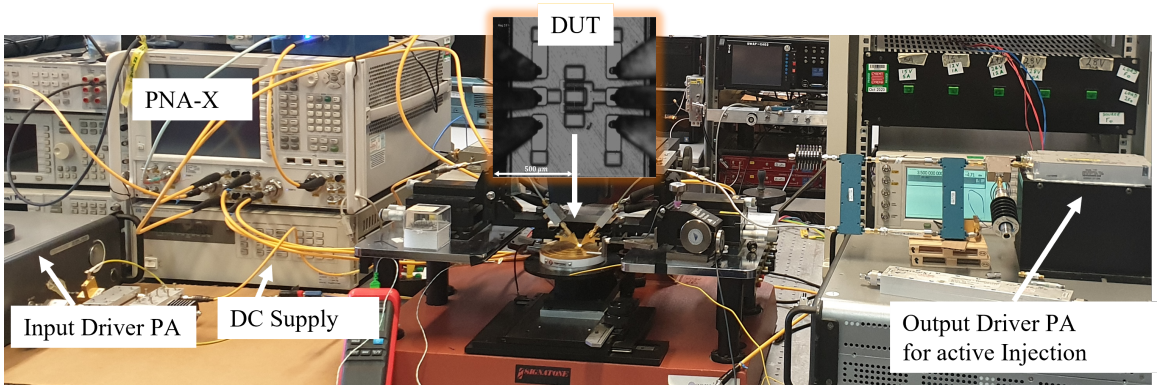
4.2.1. Measurement strategy

The measurements were conducted statically using continuous wave (CW) excitation at fundamental frequency of 3.5 GHz. For this experiment, only fundamental load-pull measurements were conducted, and harmonic frequencies were terminated at the system impedance. Figure 4.1 shows (a) the block diagram, and (b) the photograph of the active load-pull measurement system used for this experiment.

The device under test (DUT) was a 4 W GaN-on-SiC from Ampleon, whose V_{ds}^{DC} was swept from 20 V to 50 V with the step of 3 V , while V_{gs}^{DC} was swept from -3.0 V to -2.0 V with 0.1 V step. At each bias point 91 load points were measured using the grid shown in Figure 4.2.



(a)



(b)

Figure 4.1: Real-time, active load-pull system (a) Block diagram, and (b) photograph of the system at CHFE, Cardiff University.

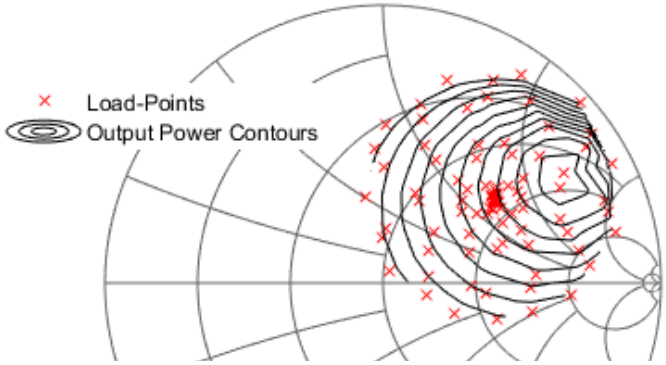


Figure 4.2: Load-pull measurement grid with 91 load points. The load-pull measurement was performed under a V_{ds}^{DC} sweep from 20 to 50 V with 3 V step at various V_{gs}^{DC} conditions from -3.0 V to -2.0 V with 0.1 V step. Load-pull grid are selected in a way to capture the optimum load points over all V_{ds}^{DC} voltages. The depicted output contours are at $V_{gs}^{DC} = -2.5$ V and $V_{ds}^{DC} = 35$ V with a maximum of 32.3 dBm and 0.5 dB step.

4.2.2. Normalised Mean Squared Error

The normalised mean squared error (NMSE) is a figure of merit which is used to quantify the deviation of the modelled data from actual measured data. In an ideal case (perfect match between the measured and modelled data), the NMSE value is equal to zero. The definition of NMSE is illustrated in (4.8) [4].

$$NMSE = \frac{\sum_i |{B_{21}}^{meas} - {B_{21}}^{model}|^2}{\sum_i |{B_{21}}^{meas}|^2} \tag{4.8}$$

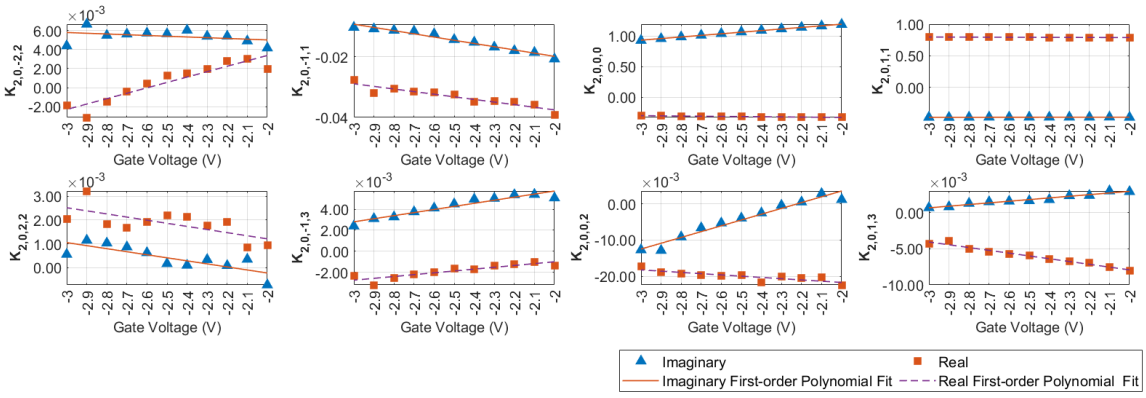
4.2.3. Finding the correct DC fitting orders

An empirical analysis of the model coefficients with respect to the gate and drain bias sweep can be used to determine the correct values of u_{max} and v_{max}. This analysis involves the following steps: 1) extracting DC-independent model coefficients (i.e, extracting conventional model $K_{p,h,m,n}$ coefficient using the formulation of the Cardiff model shown in (3.11)), 2) plotting the real and imaginary parts of the model coefficient against the gate and drain sweep, and 3) finding the polynomial order that best fits the data. This analysis was performed separately for the gate and drain bias. Once the correct fitting order was identified (i.e., starting with a first-order polynomial fit and selecting the lowest order with an NMSE value below -40 dB), it was verified on the new DC-dependent Cardiff model, in which the model coefficients are dependent on both the gate and drain bias.

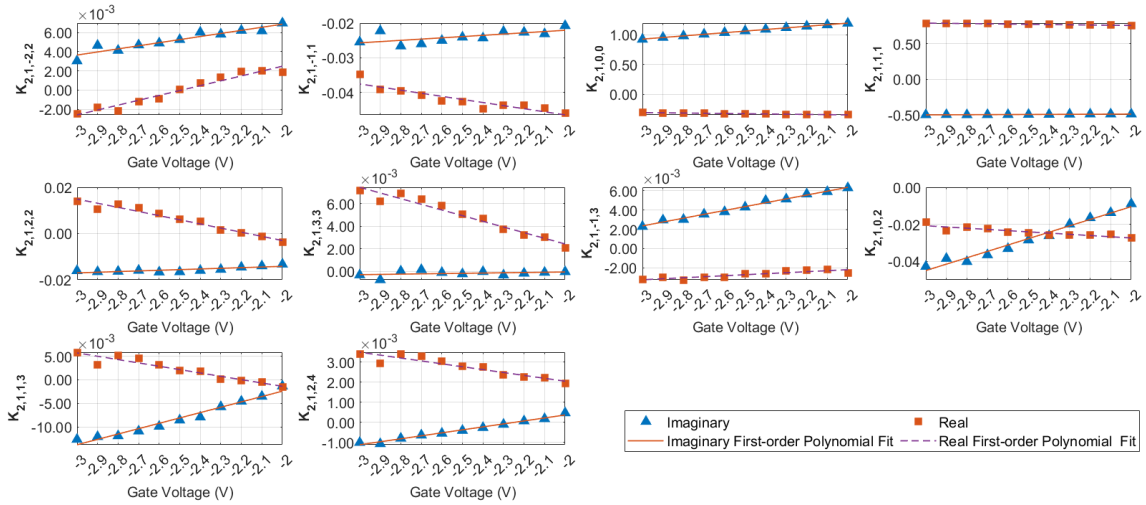
4.2.3.1 Finding gate bias fitting order u_{max}

Figure 4.3 demonstrates the response of the real and imaginary parts of the model coefficients ($K_{p,h,m,n}$) to changes in the gate bias, with the drain voltage fixed at 50 V ($v_{max} = 0$). As depicted, the real and imaginary parts of the model coefficients at both DC and f_0 exhibit behaviour that can be reasonably well approximated with a linear function ($u_{max} = 1$) with respect to the gate bias voltage. This can be mathematically represented as:

$$K_{p,h,m,n} = \sum_{u=0}^{u=1} L_{p,h,m,n,u} \left(V_{gs}^{DC}\right)^{u} \tag{4.9}$$



(a) DC



(b) f_0

Figure 4.3: Real and imaginary part of the model's coefficients (a) $K_{2,0,m,n}$ and (b) $K_{2,1,m,n}$ vs V_{gs} (symbols). First polynomial fitting (lines). The model order at the fundamental frequency is 5, while a 4$^{\text{th}}$ order model was used to model the output DC current (the model order at even harmonics and DC must be an even number).

Figure 4.4 shows the calculated NMSE (dB) value over a range of V_{gs}^{DC} sweep value. Only the measurement data at $V_{gs}^{DC} = -2.0$ V, -2.5 V and -3.0 V (highlighted in red) were used to generate the model and data at all the other V_{gs}^{DC} points are interpolated.

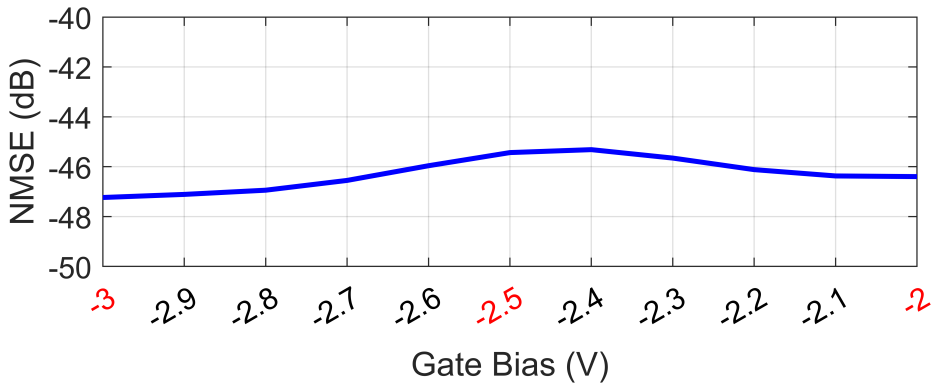
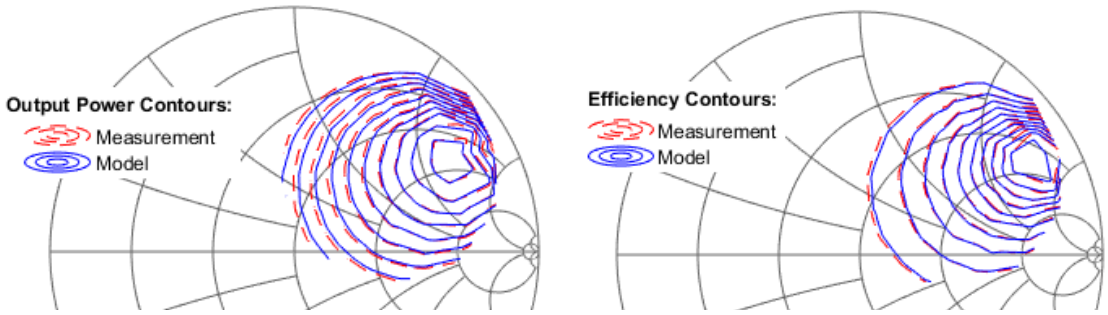


Figure 4.4: Calculated NMSE (dB) for $B_{2,1}$ at different V_{ds}^{DC} level. Only Measurement data at V_{gs}^{DC}=-3.0, -2.5 and -2.0 V (highlighted in 'red') were used to generate the model, and $B_{2,1}$ at all the other DC bias levels are interpolated. The NMSE value is less than -45 dB at all the V_{gs}^{DC} points.

As shown in Figure 4.4, the NMSE value is less than -45 dB over all the datasets. This validated the accuracy and effectiveness of the new model in interpolating load-pull data with respect to the gate voltage. This accurate interpolation is demonstrated in the form of load-pull contours in Figure 4.5, which compares the measured and interpolated load-pull contours at V_{gs}^{DC}=-2.7 V and V_{ds}^{DC}=50 V. The comparison confirms a very good match between the measured and interpolated data.

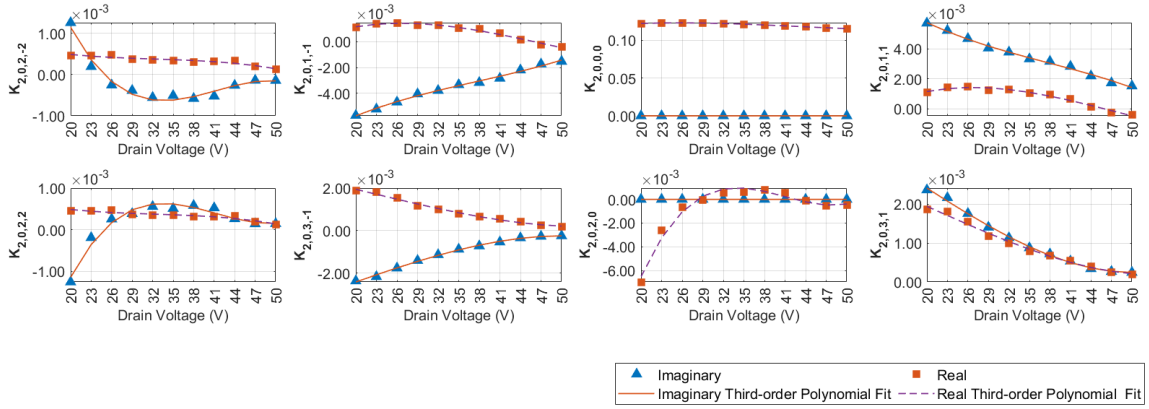


(a) (b)

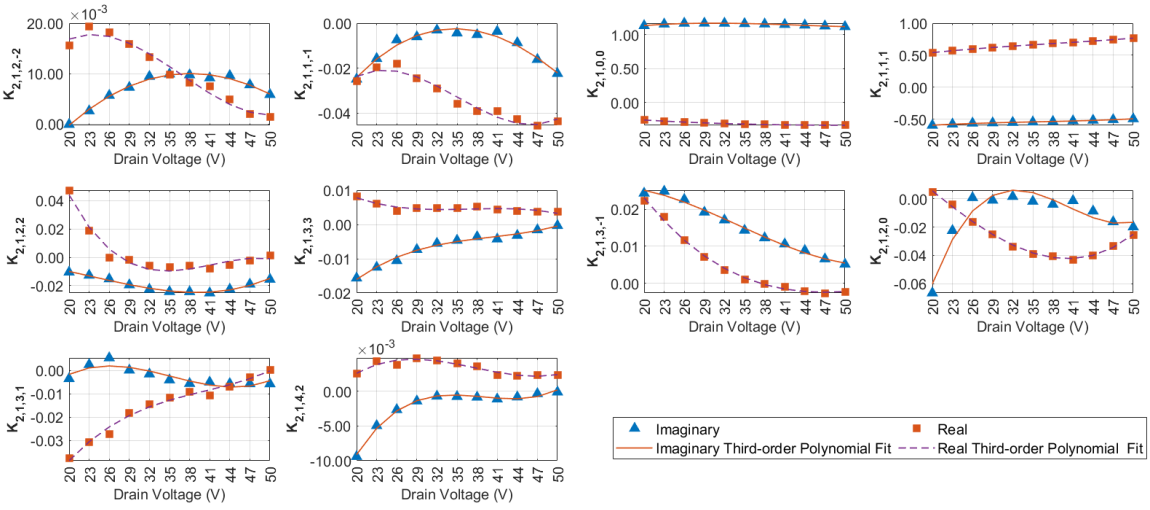
Figure 4.5: Comparison of measured and interpolated load-pull power contours (0.5 dB step from maximum of 33.7 dBm) and efficiency contours (5% step from a maximum of 56%) at V_{ds}^{DC}=50 V and V_{gs}^{DC}=-2.7 V.

4.2.3.2 Finding drain bias fitting order v_{max}

Figure 4.6 shows response of both real and imaginary part of the model coefficients ($K_{p,h,m,n}$) respective to the changes in drain bias voltage while gate bis was fixed (u_{max}=0) at -2.3 V .



(a)



(b)

Figure 4.6: Real and imaginary part of the model's coefficients (a) $K_{2,0,m,n}$ and (b) $K_{2,1,m,n}$ vs V_{ds} (symbols). Third-order polynomial fitting (lines). The model order at the fundamental frequency is 5, where a 4^{th} order model was used at DC (the model order at even harmonics and DC must be an even number).

Referencing to Figure 4.6, response of both imaginary and real part of the model coeffi-

cients can accurately be captured using a third-order polynomial function as:

$$K_{p,h,m,n} = \sum_{v=0}^{v=3} L_{p,h,m,n,u} \left(V_{ds}^{DC}\right)^{v} \tag{4.10}$$

Figure 4.7 shows the calculated NMSE (dB) value over various V_{ds}^{DC} levels at V_{gs}^{DC} =-2.3 V. Note, measurement data at only V_{ds}^{DC}=20, 29, 41, 50 V were used to extract the model's coefficients and $B_{2,1}$ data at all the other V_{ds}^{DC} were interpolated.

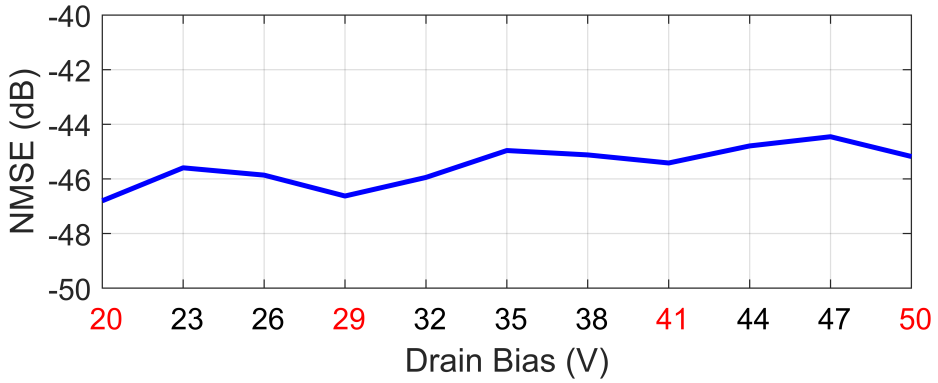
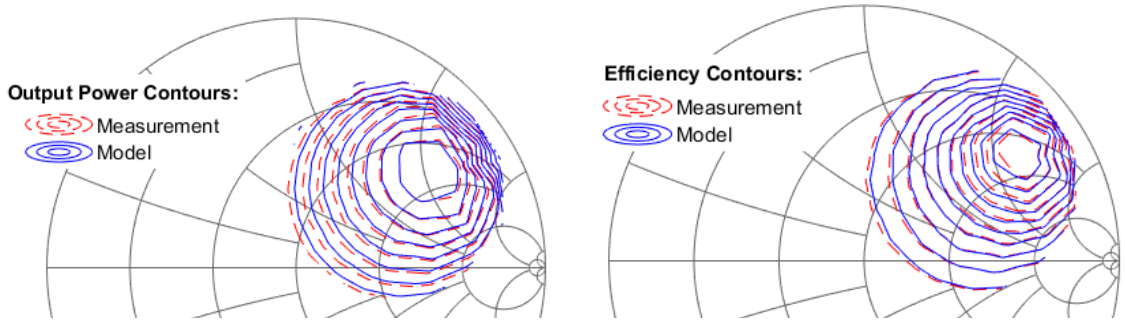


Figure 4.7: Calculated NMSE (dB) for $B_{2,1}$ at different V_{ds}^{DC} level. Only Measurement data at V_{ds}^{DC}=20, 29, 41, 50 V (highlighted in 'red') were used to generate the model, and $B_{2,1}$ at all the other DC bias levels are interpolated. The NMSE value is less than -44 dB at all the V_{ds}^{DC} points.

The new model demonstrated a high degree of accuracy in interpolating load-pull data with respect to gate voltage, as evidenced by the NMSE value being less than -44 dB for all drain voltages, corresponding to a maximum deviation of only 0.6% between the measured and modelled data. This is demonstrated in the load-pull contour comparison shown in Figure 4.8, which compares the measured and interpolated load-pull contours at V_{gs}^{DC}=-2.7 V and V_{ds}^{DC}=50 V and shows a good match between the two.

4.2.4. Verification of Bias-dependent Cardiff Model

In the previous section, the correct fitting order for the gate and drain bias sweep were identified as $u_{max} = 1$ and $V_{max} = 3$, respectively. Knowing the correct DC fitting order,



(a) (b)

Figure 4.8: Comparison of measured and interpolated load-pull power contours (0.5 dB step from maximum of 33.1 dBm) and efficiency contours (0.5% step from a maximum of 61%) at $V_{ds}^{DC} = 35\,V$.

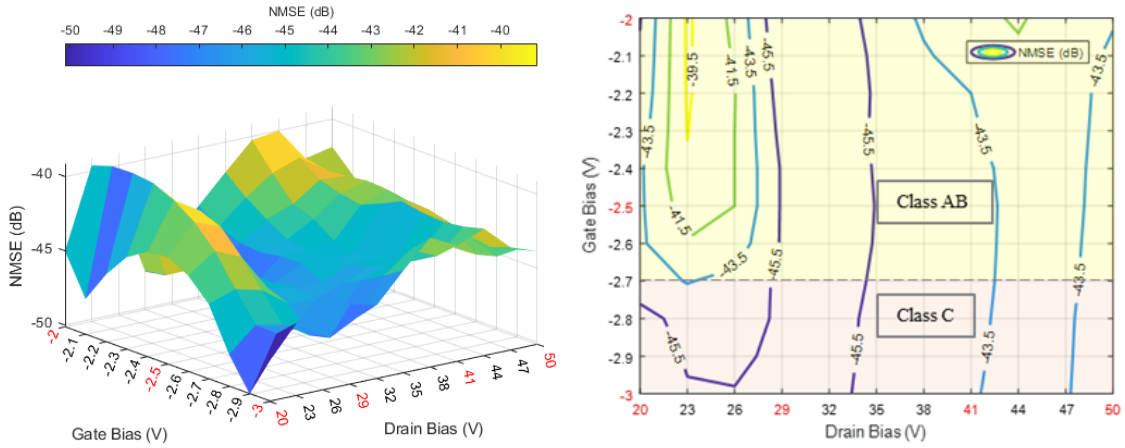
new DC-inclusive Cardiff model (4.7) can be updated as:

$$B_{p,h} = (\angle A_{1,1})^h \sum_r \sum_n \left\{ \sum_{u=0}^{u=1} \sum_{v=0}^{v=3} L_{p,h,m,n,u,v} \left(V_{gs}^{DC}\right)^u \left(V_{ds}^{DC}\right)^v \right\} |A_{2,1}|^m \left(\angle \frac{A_{2,1}}{A_{1,1}} \right)^n \quad (4.11)$$

The new formulation was tested on the entire dataset, which includes both gate and drain sweep data. The results of this testing are shown in Figure 4.9, which depicts the calculated NMSE (in dB) of '$B_{2,1}$' at various DC bias conditions. The new Cardiff model formulation (4.7) demonstrated a high degree of accuracy in predicting load-pull data, as the NMSE value was better than -39.5 dB across all datasets. This corresponds to a maximum deviation of only 1% between the measured and modelled data. Note, the pinch-off voltage was at V_{gs}^{DC}=-2.7 V and load-pull data has been successfully modelled across class AB and class C bias conditions.

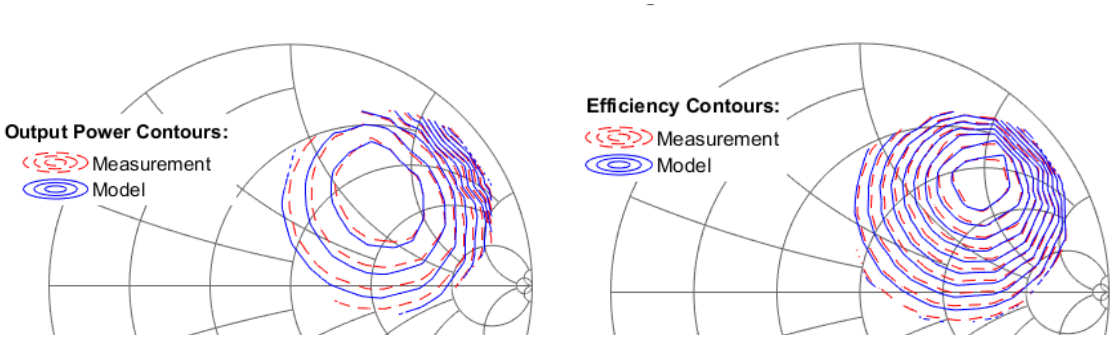
Figure 4.10 depicts a comparison between the measured and interpolated output power contours and the efficiency contour at V_{ds}^{DC}=23 V and V_{gs}^{DC}=-2.3 V (DC bias condition with the lowest accuracy in Figure 4.9).

In this example, using the load-pull data of only 12 bias points (4 V_{ds}^{DC} points and 3 V_{gs}^{DC} points), load-pull data of 121 bias points (11 V_{ds}^{DC} points and 11 V_{gs}^{DC} points) are predicted accurately. Compared to the conventional Cardiff model formulation, to generate the same



(a) (b)

Figure 4.9: NMSE (dB) of B_{21} at different DC bias conditions. The NMSE is better than -39.5 dB across all the DC bias conditions. The pinch-off voltage is at V_{gs}^{DC}=-2.7 V. Only DC bias points which are highlighted in 'red' were used to extract the model coefficients and the data at other bias points are interpolated.



(a) (b)

Figure 4.10: Comparison of measured and interpolated load-pull power contours (0.5 dB step from maximum of 31.3 dBm) and efficiency contours (0.5% step from a maximum of 61.8%) at V_{ds}^{DC}=23 V and V_{gs}^{DC}=-2.3 V.

model, the total number of required load-pull data points have significantly reduced from 11011 points (91 load points at 121 DC bias points) to only 1092 points. That is, in this case, more than a 90% reduction in the load-pull measurement points with respect to the DC bias points.

4.3. Spectral analysis as an alternative to mixing order

Traditionally, the mixing order has been used to truncate the polynomial terms and reduce the number of model coefficients. This allowed for the practical implementation of the Cardiff model while maintaining a high level of accuracy. The mixing order is selected based on experiments and is often adjusted to meet a certain performance metric, such as an acceptable NMSE value [5]. Similarly, in previous section, an empirical study of the response of the model coefficients to variations in DC bias was conducted to determine which fitting terms should include the DC bias.

The recent development of new spectral analysis technique, based on Fourier transformed load-pull data, offers a more analytical approach to selecting the correct model terms to achieve a desired level of accuracy [6]. This analysis ensures that the extracted model coefficients are well-suited for the particular dataset. Additionally, this analysis can be used to determine the minimum number of measurements required. In this section, the new methodology is adopted to extract the model coefficients for the DC-dependent Cardiff model. The analysis is based on the simulation data of a GaN HEMT device at 3.5 GHz.

4.3.1. Data Collection Strategy

The 3.5 GHz "measurements" are emulated by performing simulation in ADS on a 10 W GaN HEMT from Wolfspeed [7] at a fixed input drive of $A_{1,1}$=1.1 $\sqrt{\text{W}}$. Fig. 4.11 shows the simulation setup. Note, in this section for the gate bias voltage is represented as '$A_{1,0}$' and drain voltage as '$A_{2,0}$'.

DUT's performance was "measured" under a DC ($A_{1,0}$ & $A_{2,0}$) and RF ($A_{2,1}$) trajectory

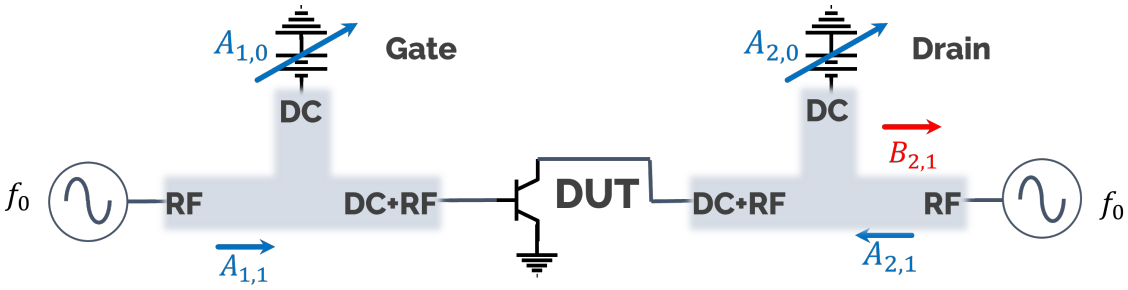


Figure 4.11: Simulation setup used to emulated the measurement data at 3.5 GHz.

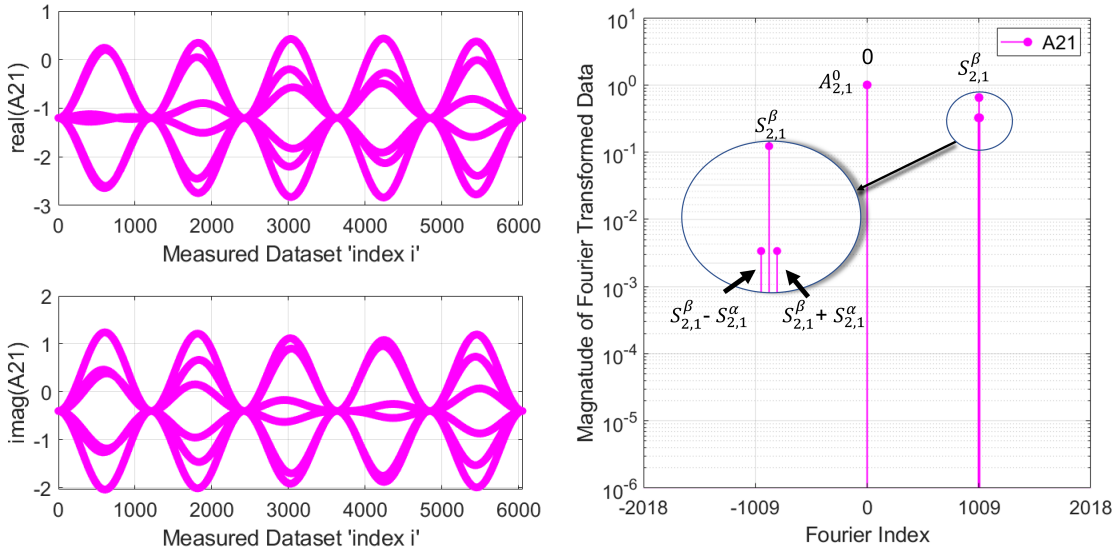
computed from (4.12) [6].

$$A^i_{p,h} = A^0_{p,h} + \frac{A^{\Delta}_{p,h}}{2}\left(1 + cos\left(S^{\alpha}_{p,h}\frac{i}{N}\right)\right)\left(cos\left(S^{\beta}_{p,h}\frac{i}{N}\right) + jsin\left(S^{\beta}_{p,h}\frac{i}{N}\right)\right) \quad (4.12)$$

where N' is the number of measurement and 'i' is the sweeping parameter ranging from '0' to '$N-1$'. The $S^{\alpha}_{p,h}$ and $S^{\beta}_{p,h}$ are the amplitude and phase modulation rates about a reference $A^0_{p,h}$. To limit the overlapping of Fourier transform spectral lines, it is advised to choose the values of $S^{\alpha}_{p,h}$ and $S^{\beta}_{p,h}$ as prime numbers [6].

For the DC trajectories, only the amplitude modulation were used, and the phase modulation terms were set to zero ($S^{\beta}_{p,0} = 0$). The amplitude modulation rate for the gate and drain trajectory were selected as $S^{\alpha}_{1,0}$=23 (ranging from -3.0 V to -2.0 V) and $S^{\alpha}_{2,0}$=103 (ranging from 15 V to 30 V), respectively. With regard to the RF stimulus, however, both amplitude and phase modulation rate were selected as non-zero prime numbers. Fig. 4.12 shows (a) dataset of the $A_{2,1}$ samples on a trajectory computed using $S^{\alpha}_{2,1}$=5 and $S^{\beta}_{2,1}$=1009 with N=6055, (b) the Fourier transformation of this dataset.

For this experiment, initially, large arbitrary prime numbers were chosen for $S^{\alpha}_{p,h}$ and $S^{\beta}_{p,h}$ to prevent overlap of the spectral line clusters. In the following section, this will be revisited as the minimum value of $S^{\beta}_{2,1}$ is investigated.



(a) (b)

Figure 4.12: (a) dataset of $A_{2,1}$ samples on a trajectory computed using $S^{\alpha}_{2,1}$=5 and $S^{\beta}_{2,1}$=1009 with N=6055, (b) the Fourier Transformation of this dataset.

4.3.2. Model Parameter Extraction

Following the extraction procedure in [6], the 'spectral line' clusters about the Fourier index locations on the $k \cdot (S^{\beta}_{2,1} = 1009)$ grid identifies the required values of 'n'. Fig. 4.13 shows how the 'measured' data directly identifies the model phase elements $(\angle A_{2,1}/A_{1,1})^n$ to target a accuracy of around -50 dBc. For each phase element, the corresponding magnitude term was also calculated, shown in the (m, n) format.

For the case presented in Fig. 4.13, spectral lines resulting from the RF stimuli $A_{2,1}$ are modelled (only spectral lines at $v = u = 0$ locations). Similarly, contribution of the DC trajectories can also be determined for each of the clusters around the $n \cdot S^{\beta}_{2,1}$ spectral lines.

Fig. 4.14 shows the terms corresponding to (a) gate bias ($A_{1,0}$) and (b) drain bias ($A_{2,0}$) trajectories around the centre spectral cluster ($n = 0$). As shown, spectral lines related to the gate and drain bias trajectories were modelled using the terms ($u = 0, 1, 2$) and ($v = 0, 1, 2, 3$), respectively. A similar approach was adopted to identify the DC terms

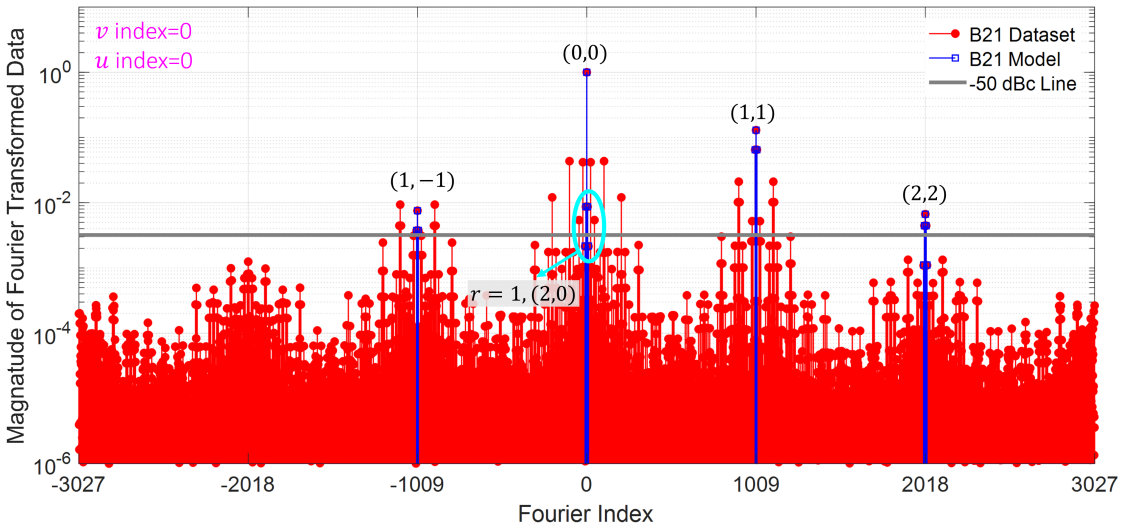


Figure 4.13: Analysing the Fourier transformation of the $B_{2,1}$ dataset (from $A_{2,1}$ trajectory of $S^{\alpha}_{2,1}$=5 and $S^{\beta}_{2,1}$=1009 with N=6055) to identify the relevant RF magnitude and phase terms (m, n).

around all the spectral line clusters at $(n \cdot S^{\beta}_{2,1} = n \cdot 1009)$ locations. Table 4.1 shows the full list of the model exponents and coefficients to model the B_{21} with NMSE of less than -40 dB, highlighting that there are also $(A_{1,0} \cdot A_{2,0})$ terms (coefficients number 6 and 15).

Fig. 4.15 shows a comparison between the Fourier transformed spectral lines of the modelled and original dataset for (a) $B_{2,0}$ and (b) $B_{2,1}$. Note, different sets of model coefficients were used to model the $B_{2,0}$ data. As depicted, by correctly selecting the model terms all the spectral lines above -50 dBC line are modelled.

The measurement results are usually presented in terms of load-pull contours. Fig. 4.16 compares the 'measured' and modelled load-pull contours at gate voltage of $A_{1,0}$=-2.5 V and drain voltage of $A_{2,0}$=22 V.

Initially, large value of $S^{\beta}_{2,1}$=1009 with $N = (2 \cdot k \cdot S^{\beta}_{2,1}) + 1 = 6055$ and $k = 3$ was used. This was to ensure that the spectral line clusters at $k \cdot S^{\beta}_{2,1}$ did not overlap. Now the necessary complexity of the Cardiff model has been identified, minimum value of the $S^{\beta}_{2,1}$ and N with consistent accuracy can be investigated. The goal is to find the minimum value

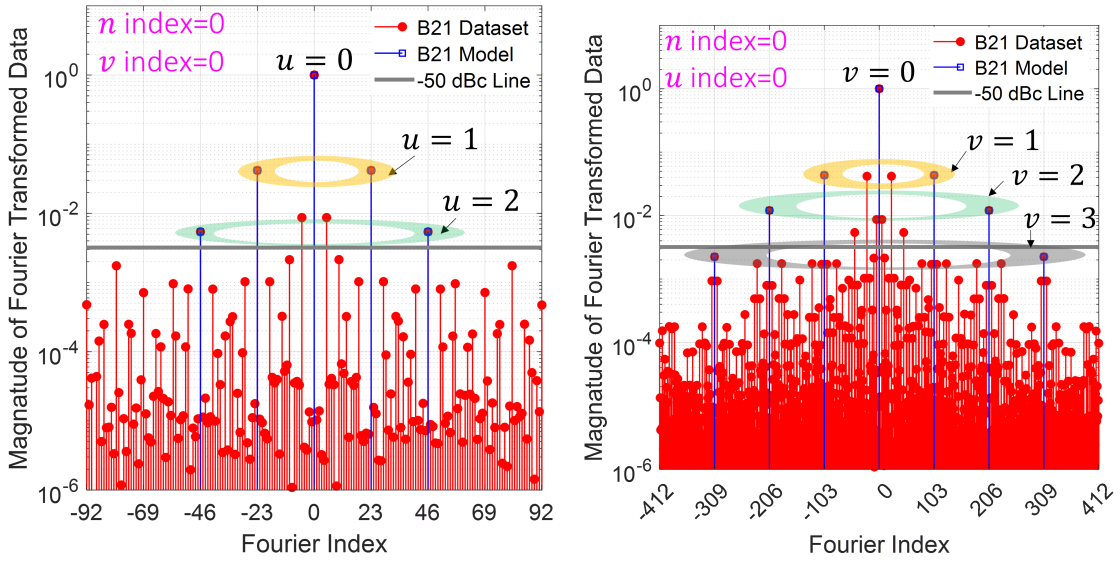


Figure 4.14: Analysing the Fourier transformation of the $B_{2,1}$ to identify the relevant DC terms around the centre spectral line $n = 0$. (a) Spectral lines related to the gate bias trajectory are at $u \cdot S^{\alpha}_{1,0} = u \cdot 23$, $u = 0, 1, 2$; (b) spectral lines related to the drain bias trajectory are at $u \cdot S^{\alpha}_{2,0} = v \cdot 103$, $v = 0, 1, 2, 3$;

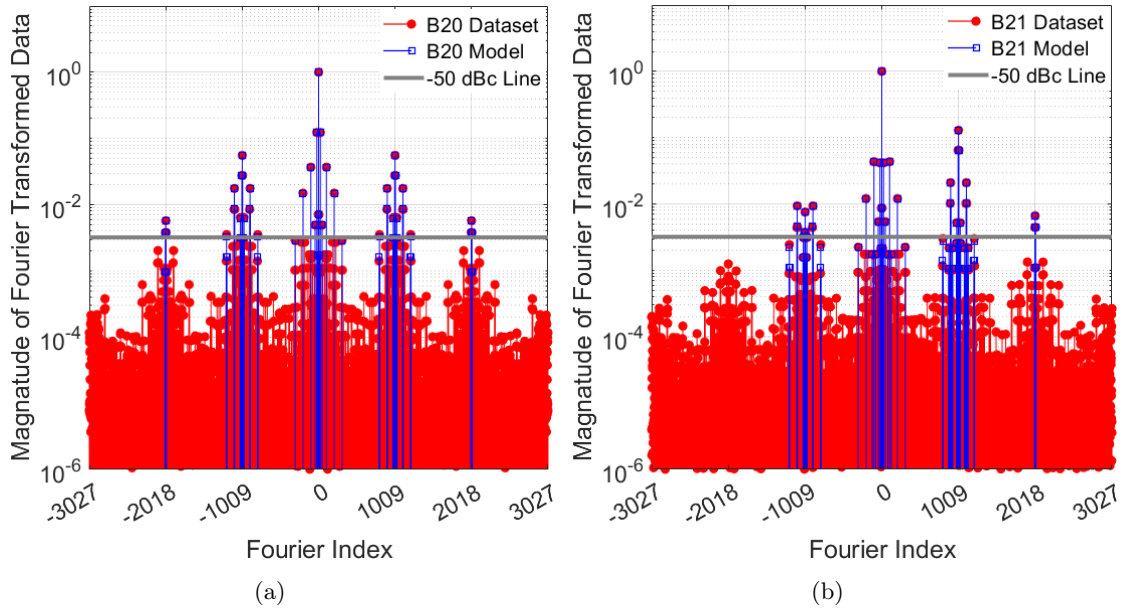


Figure 4.15: Comparison of the 'measured' and modelled (a) $B_{2,0}$ and (b) $B_{2,1}$.

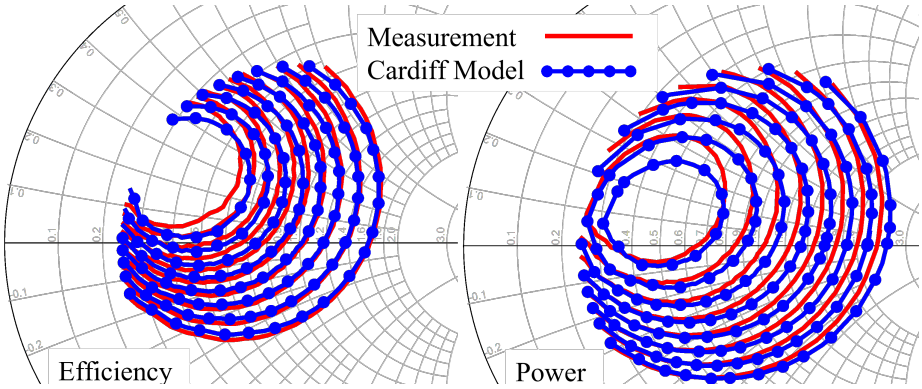


Figure 4.16: Comparison of the 'measured' and modeled load-pull power contours(0.5 dB step from maximum of 35.5 dBm) and efficiency contours (3% step from maximum of 50%) at gate voltage $A_{1,0}$=-2.5 V and drain voltage $A_{2,0}$=22 V. The extracted model coefficients were implemented in ADS to generate this comparison.

of the $S^{\beta}_{2,1}$, and the N, which avoids the overlapping of the spectral line clusters; hence, minimal effect on the extracted model coefficients.

Table 4.1 compares the model coefficients extracted from the smaller dataset of $S^{\beta}_{2,1} = 509, N = 3055$ with the original larger dataset. Despite the significant reduction in the size of the dataset (near 50% reduction) the impact on the extracted model coefficients is minimal.

The new spectral analysis method offers a clearer understanding of the required model coefficients and can help to determine the minimum number of required measurement points. However, its practical adoption has been hindered by limitations in the measurement setup, as this analysis requires a measurement system that allows users to define the measurement $A_{p,h}$ pattern. The current active load-pull measurement is designed for load-pull, not "A-pull" which is why the analysis presented in this section was based on simulation data. Fully verifying this method requires the development of a measurement system that can collect tailored A-Pull datasets, which is beyond the scope of this thesis. The author believes that the development of such a system could be revolutionary, as it could significantly improve the accuracy of model extraction and minimise the number of measurement points.

Table 4.1: Extracted model coefficients and corresponding exponents for two different dataset.

	Exponents				$L_{2,1,m,n,u,v}$			
					$S^{\beta}_{2,1}$=1009, N=6055, NMSE=-40.7 dB		**$\mathbf{S^{\beta}_{2,1}}$=509, N=3055, NMSE=-40.7 dB**	
No.	m	n	u	v	real	imag	**real**	**imag**
1	0	0	0	0	-0.7637	-0.1307	**-0.7761**	**-0.1467**
2	0	0	1	0	-0.3589	-0.7287	**-0.3608**	**-0.7287**
3	0	0	2	0	-0.1403	-0.2807	**-0.1406**	**-0.2807**
4	0	0	0	1	0.3794	0.0968	**0.3804**	**0.0989**
5	0	0	0	2	-0.0119	-0.0054	**-0.012**	**-0.0055**
6	0	0	1	1	0.0088	-0.0131	**0.0088**	**-0.0131**
7	0	0	0	3	0.0001	0.0001	**0.0001**	**0.0001**
8	1	1	0	0	-0.3152	1.6473	**-0.3176**	**1.6472**
9	1	-1	0	0	0.3325	-0.2671	**0.3287**	**-0.2727**
10	1	-1	1	0	-0.036	0.0417	**-0.0362**	**0.0418**
11	1	1	1	0	0.0618	0.3111	**0.0615**	**0.3109**
12	1	-1	0	1	-0.0361	0.022	**-0.0358**	**0.0226**
13	1	1	0	1	-0.009	-0.0881	**-0.0089**	**-0.0881**
14	1	1	0	2	0	0.0009	**0**	**0.0009**
15	1	1	1	1	-0.0016	-0.0099	**-0.0016**	**-0.0099**
16	1	-1	0	2	0.0006	-0.0004	**0.0006**	**-0.0004**
17	2	2	0	0	0.0117	-0.0209	**0.0117**	**-0.0207**
18	2	0	0	0	-0.0416	-0.0212	**-0.0418**	**-0.0213**

4.4. Summary

This chapter covered the development of a new DC-dependent Cardiff model and its accuracy and interpolation capability as verified by load-pull measurement data of a GaN-on-SiC HEMT device. An empirical analysis was conducted to determine the necessary complexity of the polynomial fit to include the DC bias. The example presented in this chapter showed that the new model was able to interpolate more than 90% of the dataset, resulting in a significant reduction in the quantity of required data compared to the previous model formulation.

In addition, spectral analysis of the Fourier transformed "A-pull" data collected from simulation was discussed. This analysis offered a clearer understanding of the choice of model terms and allowed for determining the minimum number of required data points to extract the correct model coefficients.

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CHAPTER 5

Cardiff Model Suitable for Doherty PA Design

ONE of the main challenges in using the Cardiff model for designing Doherty power amplifiers is that the model must take into account both the small signal and large signal response of the auxiliary stage. In the back-off state, when the auxiliary stage is turned off, there is no current induction, making it impossible to perform load-pull measurement on the device under test (DUT), which is essential for extracting a behavioural model. This chapter presents a novel approach for implementing the Cardiff model in computer-aided design (CAD) that allows the model to switch between the small signal and large signal models based on the input drive level.

Previous attempts to include the input drive level ($|A_{1,1}|$) in the Cardiff model have been limited by dynamic range issues and the requirement for different model coefficients at different power stages [1]. For instance, different sets of coefficients have been necessary for low, medium, and high power regions. This limitation is investigated in this chapter along with the proposal of a new modelling approach for incorporating the $|A_{1,1}|$ in the model. This new model formulation is capable of covering the entire power sweep range using a single set of model coefficients and eliminating the input drive level as a look-up indexing parameter.

Unless otherwise noted, the empirical analysis in this chapter is based on load-pull measurements of a 25 W GaN-on-SiC HEMT from Ampleon using pulsed RF excitation at 3.6 GHz. The device under test (DUT) was biased in class C configuration with a DC

gate-source voltage of V_{gs}^{DC}=-4 V and various drain bias voltages.

5.1. Limitation of the current $A_{1,1}$-dependent Cardiff model

The current Cardiff model, which includes $|A_{1,1}|$ was developed based on mixing theory principals first presented in [1]:

$$B_{p,h} = (\angle A_{1,1})^h \cdot \sum_{t=0}^{t_{max}} \sum_{r=0}^{r_{max}} \sum_{n=n_{min}}^{n_{max}} M_{p,h,m,n,x} \cdot |A_{1,1}|^x \cdot |A_{2,1}|^m \cdot \left(\angle \frac{A_{2,1}}{A_{1,1}}\right)^n \tag{5.1}$$

where,

$$\begin{cases} t_{max} = \left(\frac{w-h}{2}\right) \\ r_{max} = \left(\frac{w-h}{2}\right) - t \\ n_{\min} = -\left(\left(\frac{w-h}{2}\right) - t - r\right) \\ n_{\max} = h + \left(\left(\frac{w-h}{2}\right) - t - r\right) \\ m = |n| + 2r \\ x = |h-n| + 2t, \end{cases}$$

and for DC current ($h = 0$) the term "$B_{2,0} \triangleq I_{2,0}$".

The 'p' is the port index and 'h' is the harmonic index, referenced to the fundamental frequency 'f_0', The parameters 'm' and 'n' denote the coefficient related stimulus phasor '$A_{2,1}$' magnitude and phase exponents, respectively. The 'm' and 'n' are related as '$m = |n| + 2r$' where 'r' is the magnitude indexing term, usually restricted to the maximum of $r_{max} = 1$. The parameter x is magnitude exponent of the '$|A_{1,1}|$' and calculated according to mixing theory as $x = |h-n|+2t$. The 't' is the magnitude restricting term for the '$|A_{1,1}|$' can range from 0 to $+\infty$ often restricted to maximum of $t_{max} = 1$.

The parameter 'w' is the mixing order, which determines the complexity of the model and maximum order of its terms. For instance, consider a Cardiff model with '$w = 3$' at the fundamental frequency. The maximum order of the terms in this model would be 3, and the

model would include terms with orders 1 and 3. The terms with higher orders would not be included in the model. On the other hand, if '$w = 5$' were used, the model would include terms with orders up to 5, resulting in a more complex model with more terms. Note, based on the mixing theory principal, at odd harmonics (i.e., fundamental and third harmonic), it is generally recommended to use a Cardiff model with an odd mixing order (i.e., 'w' should be an odd number). Table 5.1 shows the model term's order for a 5^{th} order Cardiff model at the fundamental frequency ($h = 1$). For each individual model term, the order is calculated as ($order = |h - n| + |n| + 2t + 2r = m + x$).

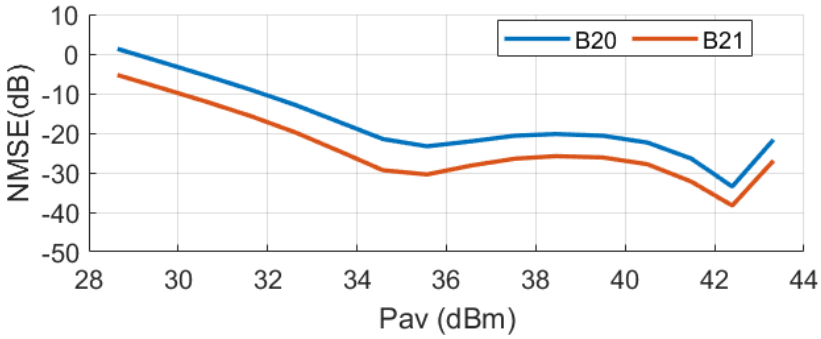
	t=0			**t=1**			**t=2**		
	r=0	r=1	r=2	r=0	r=1	r=2	r=0	r=1	r=2
n=-2	**5**	∄	∄	∄	∄	∄	∄	∄	∄
n=-1	**3**	**5**	∄	**5**	∄	∄	∄	∄	∄
n=0	**1**	**3**	5	**3**	**5**	∄	5	∄	∄
n=1	**1**	**3**	5	**3**	**5**	∄	5	∄	∄
n=2	**3**	**5**	∄	**5**	∄	∄	∄	∄	∄
n=3	5	∄	∄	∄	∄	∄	∄	∄	∄

Table 5.1: Calculated model term's order for a 5^{th} order Cardiff model at the fundamental frequency ($h = 1$). Term orders are calculated using ($order = |h-n|+|n|+2t+2r = m+x$). Wherever the model term does not exist, the symbol '∄' is placed in the table. Often, in practice, only the terms in **bold** are used to extract the model, and the maximum value of r and t is restricted to 1 ($r_{max} = t_{max} = 1$).

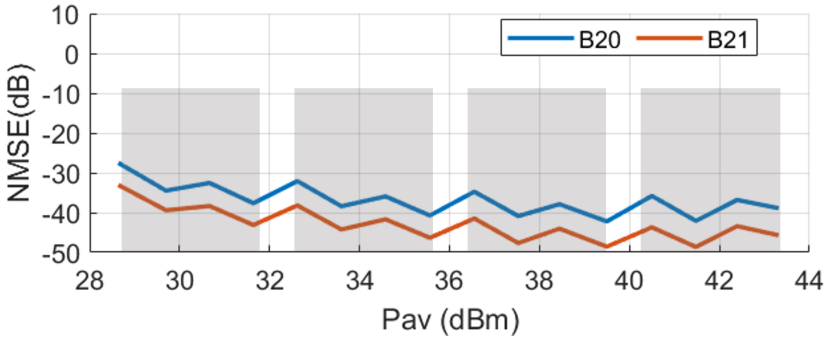
Modelling the behaviour of the DUT over a 16 dB dynamic range using the model formulation in (5.1) resulted in poor accuracy, as shown in Figure 5.1 (a) with poor performance in terms of normalised mean squared error (NMSE). However, the model was able to predict more accurately the device response when it was used over a limited range, with separate sets of model terms extracted for each 4 dB, as illustrated in Figure 5.1 (b).

5.2. Spectral analysis using simulated dataset

To gain an understanding of the correct model coefficients and potentially improve the model limitations in modelling the device behaviour over a wide power sweep, spectral analysis of



(a)



(b)

Figure 5.1: Power range limitation of the current $A_{1,1}$-dependent Cardiff model. (a) one set of model coefficients were used to model the whole dynamic-range (16 dB); (b) different set of model coefficients for each 4 dB section.

tailored A-pull data can be used. However, due to the limitations of the current load-pull measurement system, simulation in ADS was to emulate the measurement system. A-pull simulations were performed on a 10 W GaN device from Wolfspeed (Cree) [2] at 3.6 GHz. The DUT was biased at $V_{gs}^{DC} = -4$ V (in class C) and $V_{ds}^{DC} = 28$ V. The A-pull trajectories were generated using (5.2):

$$A_{p,h}^{i} = A_{p,h}^{0} + \frac{A_{p,h}^{\Delta}}{2}\left(1 + cos\left(S_{p,h}^{\alpha}\frac{i}{N}\right)\right)\left(cos\left(S_{p,h}^{\beta}\frac{i}{N}\right) + jsin\left(S_{p,h}^{\beta}\frac{i}{N}\right)\right) \tag{5.2}$$

Where the $S_{p,h}^{\alpha}$ and $S_{p,h}^{\beta}$ are the amplitude and phase modulation rate about a reference $A_{p,h}^{0}$. The 'N' is the number of measurement and 'i' is the sweeping parameter ranging from '0' to '$N-1$'. For the $|A_{1,1}|$ trajectory, only the amplitude modulation was used and phase modulation term was set to zero ($S_{1,1}^{\beta} = 0$) (this is because the model terms are normalised to the $\angle A_{1,1}$).

Figure 5.2 shows the dataset of $A_{1,1}$ and $A_{2,1}$ samples and their Fourier transformation on a trajectory computed using $S_{1,1}^{\alpha} = 23$, $S_{2,1}^{\alpha} = 3$, $S_{1,1}^{\beta} = 211$, and N=1689. Note, the phase modulation rate of the $A_{2,1}$ was selected as a relatively large number ($S_{1,1}^{\beta} = 211$) to avoid spectral overlapping between the $A_{1,1}$ and $A_{2,1}$ samples [3].

By analysing the Fourier-transformed $B_{2,1}$ data, the correct model terms for this data were identified. Figure 5.3 shows the measured and modelled $B_{2,1}$ response to the $A_{1,1}$ and $A_{2,1}$ trajectory. Model coefficients were selected in a way to model all the spectral lines over -60 dB. The identified model terms (m,n,x) for this data are: *{**(2,-2,0)**, (2,-2,1), (1,-1,0), **(1,-1,1)**, **(0,0,0)**, (0,0,1), **(0,0,2)**, (1,1,0), **(1,1,1)**, (1,1,2), **(2,2,0)**, (2,2,1), **(2,0,0)**, (3,1,0)}*. Surprisingly, this analysis revealed the need for certain model terms (in bold) which do not conform to the mixing principle outlined in (5.1).

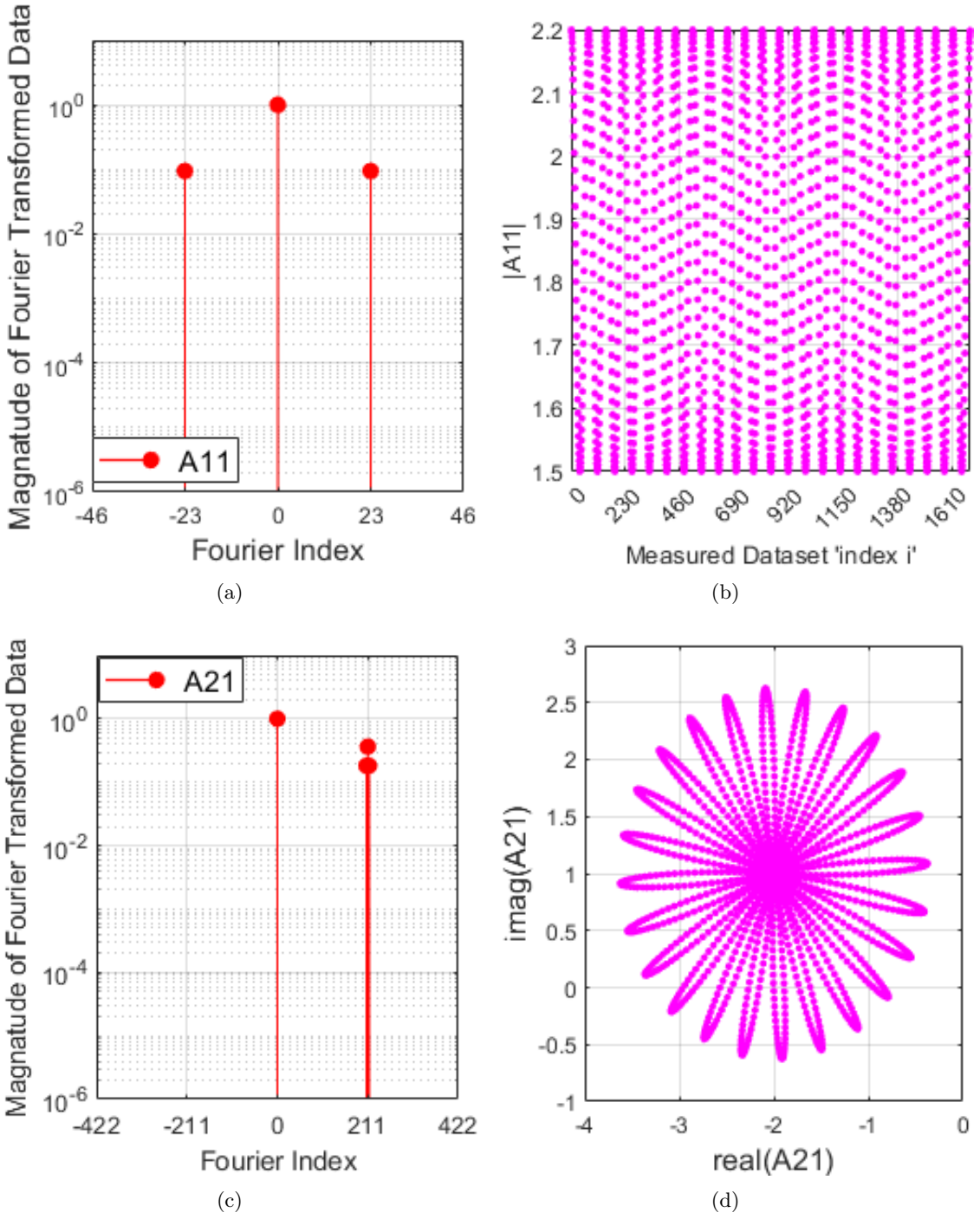


Figure 5.2: Dataset of $A_{1,1}$ and $A_{2,1}$ samples on a trajectory computed using $S_{a_{1,1}} = 23$, $S_{a_{2,1}} = 3$, $S_{p_{2,1}} = 211$, with N=1689. Also shown is the result of Fourier transforming this dataset.

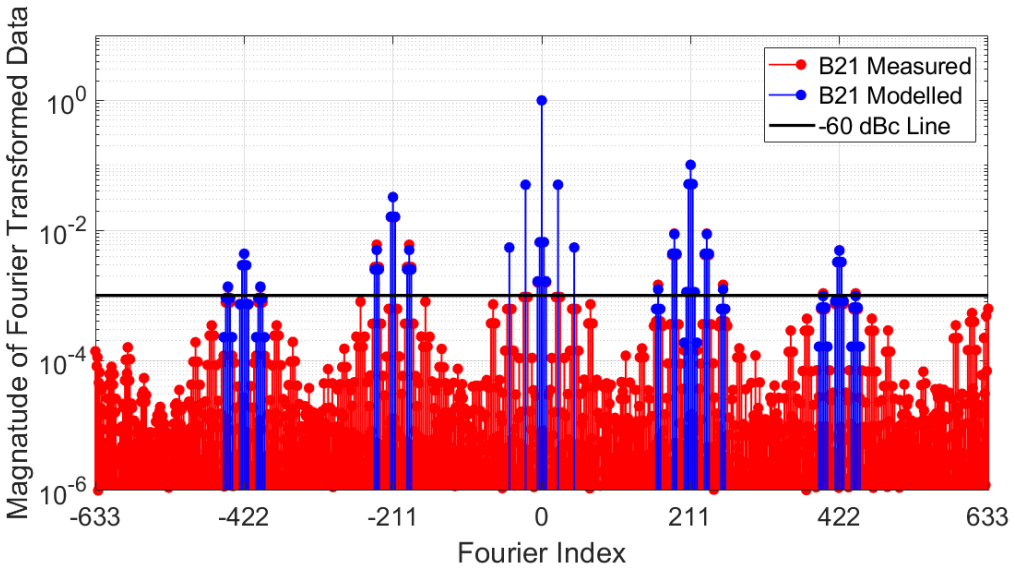


Figure 5.3: Comparison of measured and modelled $B_{2,1}$ response using $A_{1,1}$ and $A_{2,1}$ samples on trajectories computed using $S_{a_{1,1}} = 23$, $S_{a_{2,1}} = 3$, $S_{p_{2,1}} = 211$, with N=1689.

Note, as shown in Table 5.1 the model terms at f_0 are all 'odd-order'. However, The spectral analysis reveals the need for some 'even-order' model terms which are not aligned with the mixing principle.

In particular, the presence of term **(0,0,0)** is unexpected. A direct translation of this mathematical term to the physical domain is that the DUT is conducting even if there is no input stimulus signal, which is not a valid physical property of the DUT. An alternative explanation is that this model term exists as a result of polynomial truncation and spectral aliasing of higher model terms which can not be identified. Although this analysis can not conclusively explain the presence of these "non-physic-related" terms, it reveals the fact that perhaps a polynomial fit can be used to formulate $A_{1,1}$ into the Cardiff model as:

$$K_{p,h,m,n} = \sum_{x=0}^{x_{max}=?} R_{p,h,m,n,x} \cdot |A_{1,1}|^{x} \tag{5.3}$$

where $K_{p,h,m,n}$ is the model coefficients independent of $A_{1,1}$ and $R_{p,h,m,n,x}$ is the $A_{1,1}$-dependent model coefficients. The order of polynomial fit (x_{max} =?) can be identified by

investigating the relationship between the $K_{p,h,m,n}$ and the $A_{1,1}$ sweep (similar to inclusion of DC-dependence in Chapter 4).

5.3. Empirical investigation of the $A_{1,1}$ dependency

To investigate the relationship between the Cardiff model coefficients and the $|A_{1,1}|$ sweep: i) 5^{th} order conventional Cardiff model coefficients were extracted from load-pull measurement data of the 25 W device; ii) the real and imaginary part of the model were plotted separately against the $|A_{1,1}|$, as shown in Figure 5.4 for both DC (a) and fundamental frequency (b).

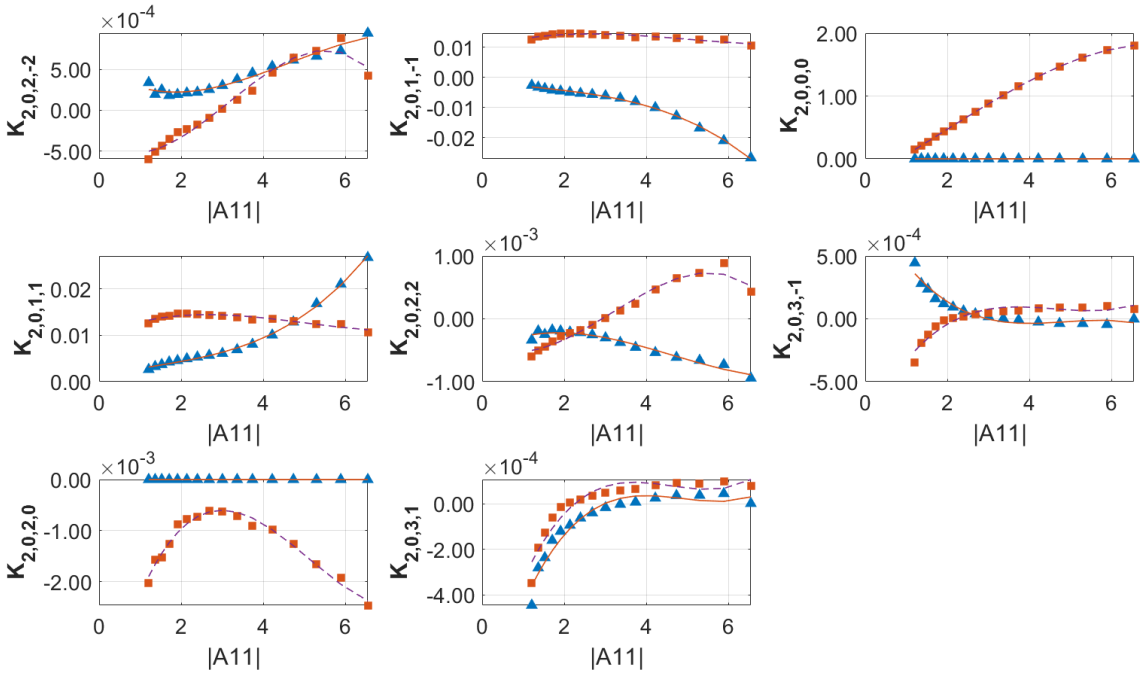
Referencing to Figure 5.4, a 3^{rd} order polynomial fit can be used to capture the response of the conventional Cardiff model ($K_{p,h,m,n}$) to the changes to the $|A_{1,1}|$. Therefore, (5.3) can be updated as:

$$K_{p,h,m,n} = \sum_{x=0}^{3} R_{p,h,m,n,x} \cdot |A_{1,1}|^x \tag{5.4}$$

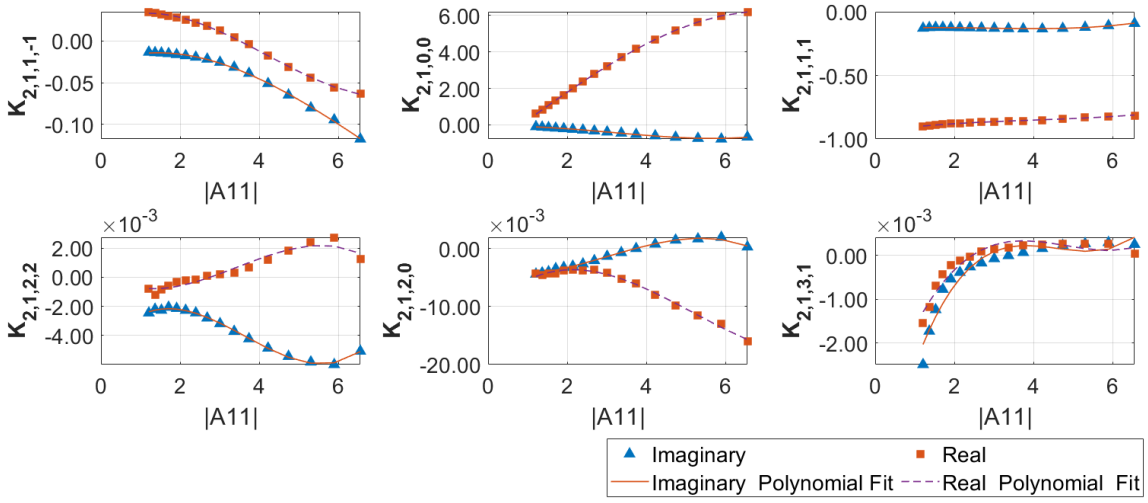
A new Cardiff model formulation can be developed which includes the $A_{1,1}$ dependency as:

$$B_{p,h} = (\angle A_{1,1})^h \cdot \sum\nolimits_r \sum\nolimits_n \left\{ \sum_{x=0}^{3} R_{p,h,m,n,x} \cdot |A_{1,1}|^x \right\} \cdot |A_{2,1}|^m \cdot (\angle \frac{A_{2,1}}{A_{1,1}})^n \tag{5.5}$$

Where $R_{p,h,m,n,x}$ is the new model coefficients which includes the $|A_{1,1}|$ variation. Figure 5.5 shows the NMSE (dB) value calculated for the fundamental frequency at the input ($B_{1,1}$), output ($B_{2,1}$) and also DC current ($B_{2,0}$); (a) at $V_{ds}^{DC} = 30\,\text{V}$ and (b) $V_{ds}^{DC} = 50\,\text{V}$.

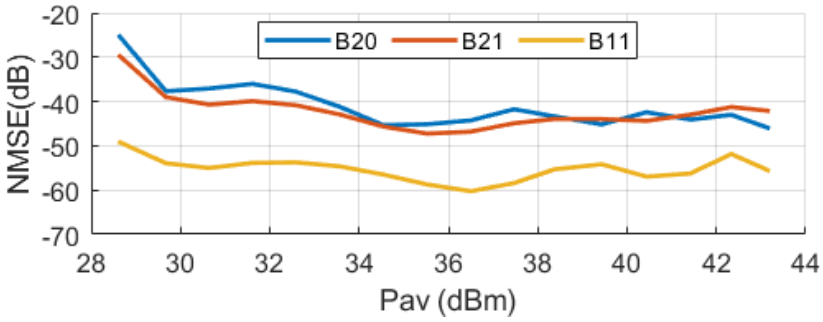


(a)

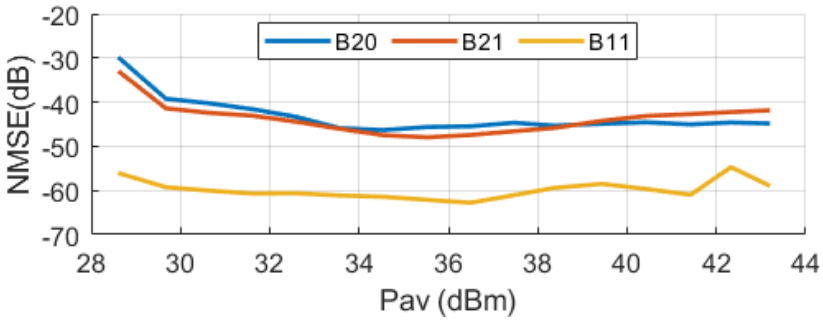


(b)

Figure 5.4: Real and imaginary part of the model's coefficients (symbols) (a) $K_{2,0,m,n}$ and (b) $K_{2,1,m,n}$ vs $|A_{1,1}|$. First order polynomial fitting (lines). The model order at the fundamental frequency is 3, where a 4^{th} order model was used at DC (the model order at even harmonics and DC must be an even number).



(a)

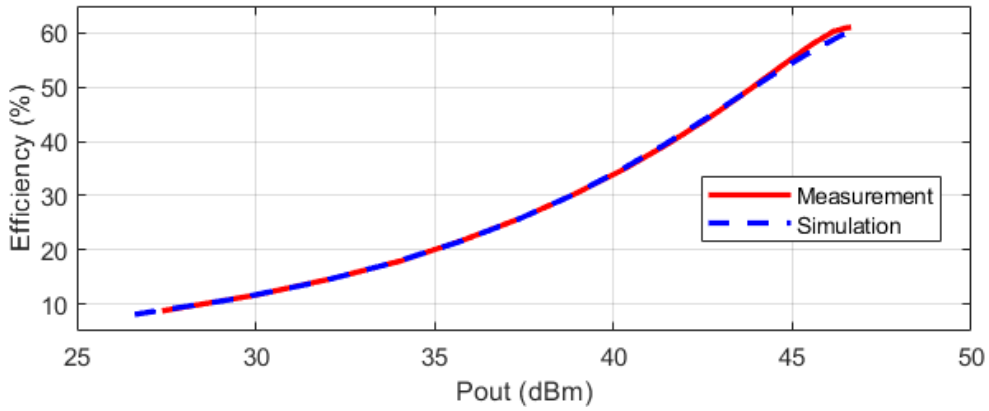


(b)

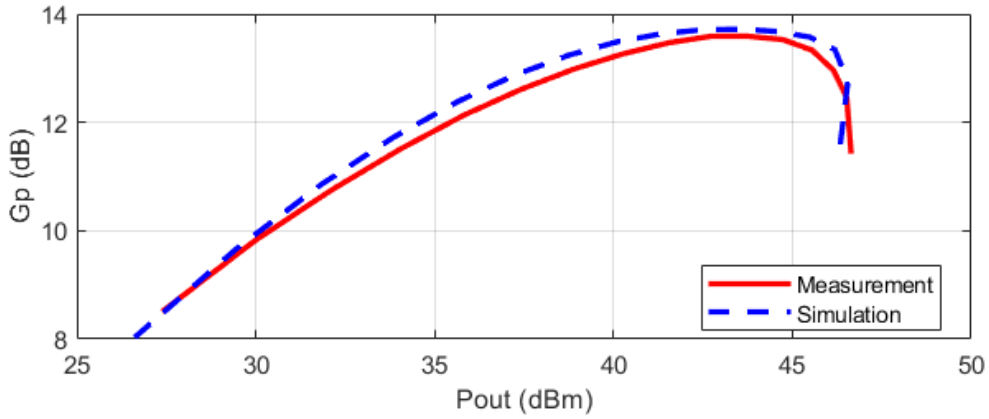
Figure 5.5: Comparison of measured and modelled data at (a) $V_{ds} = 30\,\text{V}$ and (b) $V_{ds} = 50\,\text{V}$. $|A_{1,1}|$ is included in the model formulation with a 3^{rd} order polynomial.

As shown in Figure 5.5, the model is capable of accurately predicting the load-pull data over the input drive (P_{av}) sweep with NMSE value of less than -30 dB at all the power levels. Compared to the previous model in (5.1) which had limitation in the power range (as it was shown in Figure 5.1), the new model (5.5) can predict the device response over the whole 16 dB power-range.

The model was then implemented in ADS and the simulation results were compared with the original measurement data, as shown in Figure 5.6 for the optimum load ($Z_L = (7.64 - 1.83j)\,\Omega$). The model was able to accurately predict the efficiency and gain response of the DUT over the entire power range. It is worth noting that the implementation of the Cardiff model in ADS was modified to incorporate the $A_{1,1}$ term in the model formulation.



(a)



(b)

Figure 5.6: Comparison of measured and simulated results of the new $A_{1,1}$-dependent Cardiff model at $V_{ds} = 50\,\text{V}$. The simulation results accurately match the measured (a) efficiency and (b) gain response over the whole power range.

5.4. Incorporating S-parameter response into the Cardiff model CAD implementation

At this stage, the model can accurately predict the large signal response of the device to variation of the $|A_{1,1}|$. However, this model is not capable of accurately extrapolating the device behaviour into the small-signal region as it is shown in Figure 5.7 (a).

As shown in Figure 5.7 (a), the extrapolated magnitude of $|B_{2,1}|$ tends to increase again

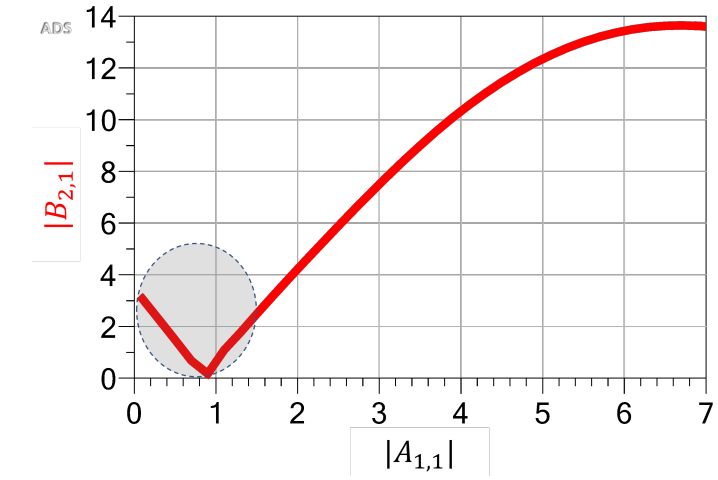
(shaded area on the plot) at low power levels ($|A_{1,1}| < 1$). However, because the device is biased in class C (no output conduction at very low input drive levels), it is expected that $B_{2,1}$ should approach zero as $A_{1,1}$ approaches zero:

$$\lim_{A_{1,1}\to 0} B_{2,1}\left(A_{1,1}\right) = 0 \tag{5.6}$$

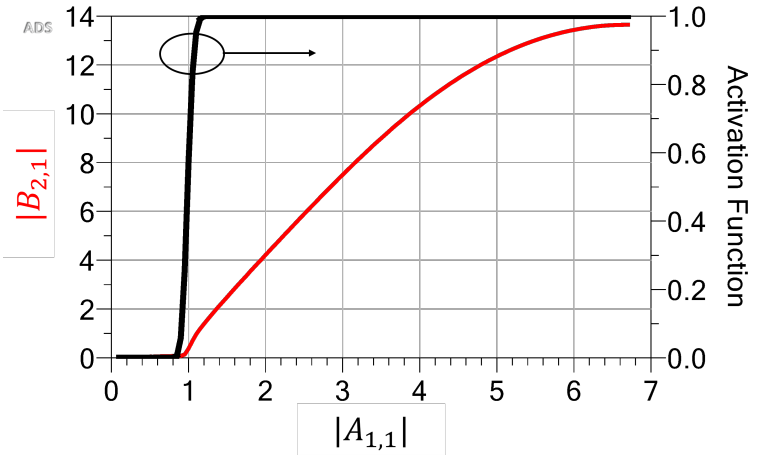
To enforce the condition stated in (5.6), an "activation function" (AF) can be used to regulate the simulation results at low power levels $|A_{1,1}| < 1$, and 'filter-out' the mathematical noise in Figure 5.7 (a). The AF should have a property of:

$$AF(A_{1,1}) \simeq 1 \text{ for } A_{1,1} \geq 1 \tag{5.7}$$

This function will effectively "deactivate" the large signal Cardiff model, by ensuring that $B_{2,1}$ is zero, for $|A_{1,1}| \ll 1$. For $|A_{1,1}| \geq 1$, the AF will "activate" the model and allow it to operate as normal. This can help to improve the accuracy of the model at low power levels while still maintaining its predictive capabilities at higher power levels. Therefore, a hyperbolic tangent ($tanh$) function can be used as the AF to force $B_{2,1}$ to approach zero as $|A_{1,1}| < 1$, as shown in Figure 5.7 (b). The $tanh$ function has the desired property of approaching zero for small input values and approaching unity for larger input values, making it well-suited for this purpose.



(a)



(b)

Figure 5.7: Using a *tanh* activation function to force the model response at the low power level to zero. Device response at $|A_{1,1}| < 1$ is extrapolated. (a) the model extrapolation at low power level, (b) with the use of the activation function device response was force to zero.

Now the extrapolated data in the $|A_{1,1}| < 1$ region are forced to zero; hence, more aligned with class C performance. However, to achieve more accuracy in simulation, the model needs to predict small signal performance of the device when the auxiliary stage is switched OFF ($|A_{1,1}| < 1$). To do so, the equation (5.8) was used in ADS implementation of the model capable to switch between the small and large signal model dependent of the input

drive level.

$$B'_{2,1} = B_{2,1} \times tanh\left(\alpha|A_{1,1}|\right)^{\beta} + b_{2,1} \times \left(1 - tanh\left(\alpha|A_{1,1}|\right)^{\beta}\right) \tag{5.8a}$$

$$B'_{1,1} = B_{1,1} \times tanh\left(\alpha|A_{1,1}|\right)^{\beta} + b_{1,1} \times \left(1 - tanh\left(\alpha|A_{1,1}|\right)^{\beta}\right) \tag{5.8b}$$

The $B_{1,1}$ and $B_{2,1}$ are the large signal response of the device calculated from Cardiff model coefficients, whereas $b_{1,1}$ and $b_{2,1}$ are the small signal response from S-parameter measurement. By multiplying the large signal response by $tanh\left(\alpha|A_{1,1}|\right)^{\beta}$ and small signal response by $\left(1 - tanh\left(\alpha|A_{1,1}|\right)^{\beta}\right)$ activation functions, the new implementation is capable of accurately modelling the behaviour of a device in class C bias configuration. Figure 5.8 shows model input impedance simulation results with drive level sweeping in a way capturing both small signal and large signal responses.

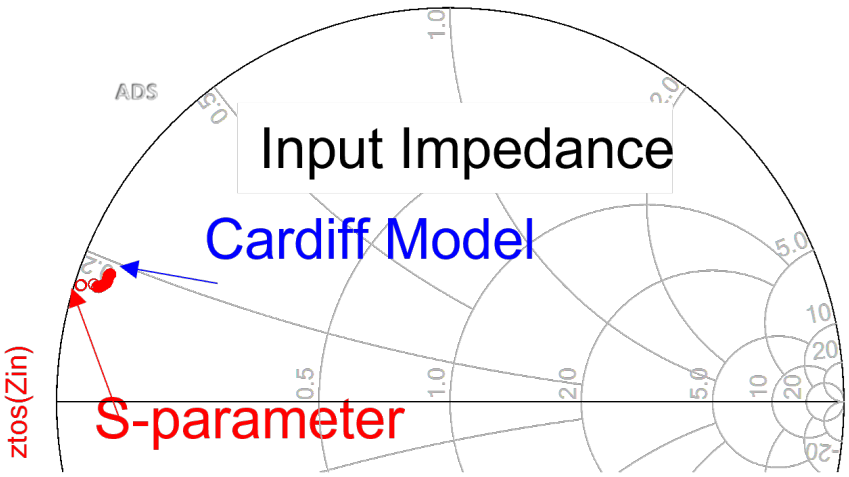
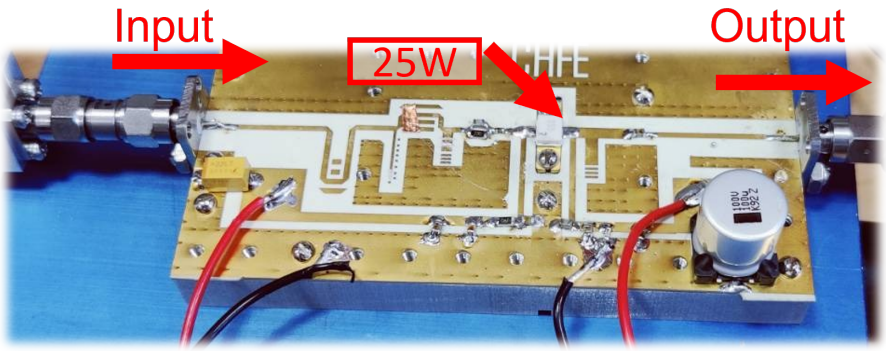


Figure 5.8: Input impedance simulation result. At very low power, simulation results are from S-parameter measurement. At higher power level, however, nonlinear Cardiff model formulation predicts the device response.

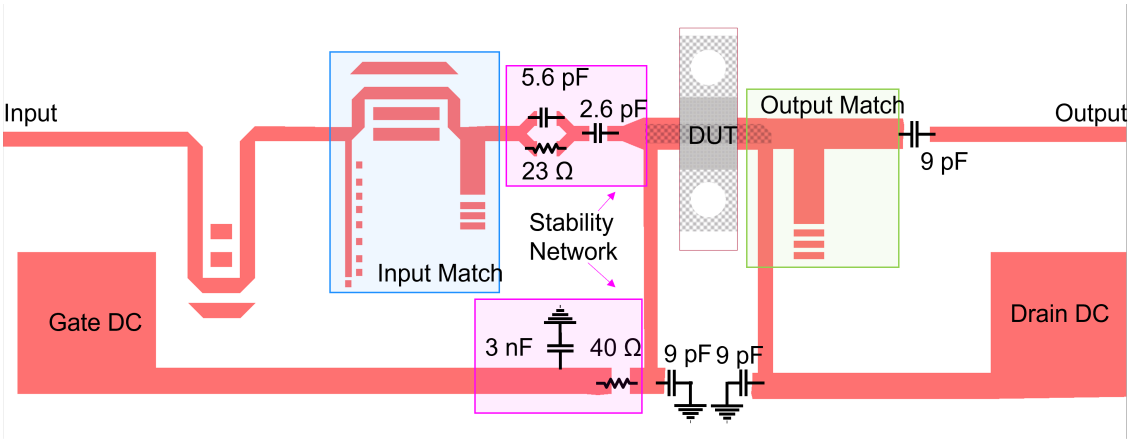
5.5. Verification with a PA design

To evaluate the suitability and accuracy of the new Cardiff model for designing the auxiliary stage of a Doherty power amplifier (DPA), a class C power amplifier was designed and its

performance was measured and compared with the corresponding simulation results. As shown in Figure 5.9, the fabricated and schematic design of the PA is depicted. The input matching network consists of two open stubs and a transmission line that match the input of the device from near the short circuit edge of the Smith chart (shown in Figure 5.8) to the centre of the Smith Chart ($\Gamma = 0$). For stability, a parallel R-C network of 5.6 pF and 23 Ω in series with a 2.6 pF capacitor was used on the RF input path, and a 40 Ω resistor on the gate DC path was used to further stabilise the circuit at very low frequencies. Note that the stability analysis was based on the S-parameter measurement of the DUT in a class AB bias environment from 100 MHz to 12 GHz, where the 'Rollet stability factor' (also known as 'K' factor) [4] was used as a figure of merit (K>1 was achieved over the whole frequency range). Several tuning microstrip elements [5] can be noticed at critical locations on the board, particularly at the input, as our previous design experience showed that the input match is very sensitive to variations in the manufacturing process, which can cause shifts in the frequency of operation and reductions in the gain. These elements allow for fine-tuning the circuit and compensating for variations in the PCB fabrication process.



(a)

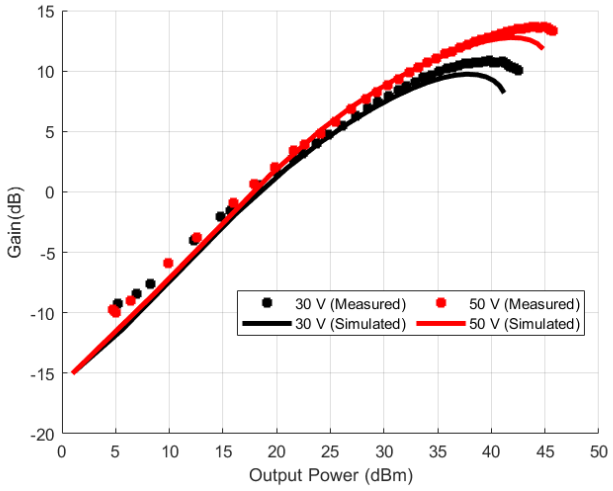


(b)

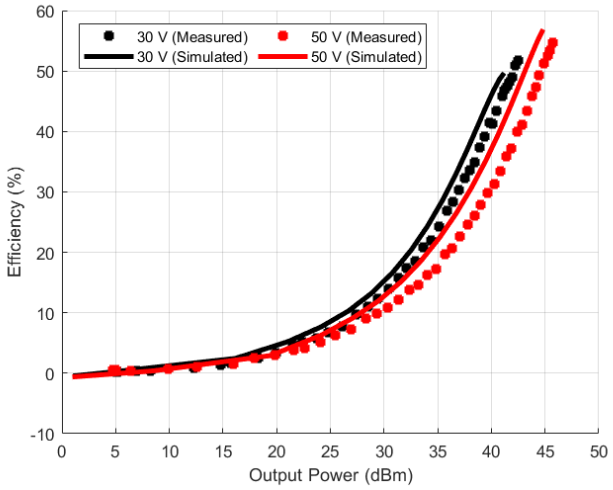
Figure 5.9: Class C power amplifier designed with the new A11-dependent Cardiff model, with a PCB size of 10 cm × 4.5 cm . The same design is used for the auxiliary stage of an asymmetric DPA which will be covered in Chapter 6.

Figure 5.10 shows a comparison between the measured and simulated results of the PA biased in class C with $V_{gs}^{DC} = -4\,V$ at both 30 V and 50 V drain bias voltages. As shown, the model has been able to predict accurately the device's gain and efficiency. Interestingly, the model is highly capable to predict the device response at the very low power level where the device is OFF. The deviations between model and measurements at high drive are expected as the harmonic termination between the original dataset (on which the model was based) and the designed power amplifier are different. The overall agreement between the model and measurements is good, indicating that the new Cardiff model is suitable for designing of class C power amplifiers (i.e, auxiliary stage in a Doherty). This class C amplifier was

then used as the auxiliary stage of an asymmetric DPA, which is discussed in more detail in Chapter 6.



(a)



(b)

Figure 5.10: Measurement vs simulation result at V_{ds}^{DC} = 30 V & 50 V. (a) gain vs output power, and (b) efficiency vs output power. There is a very good match between the measured and simulated result. The difference between the modelled and measured result can be witnessed at maximum power level. This deviation is caused by different harmonic termination between the original dataset (which the model was based on) and the designed PA.

5.5.1. Summary

In this chapter, a revised Cardiff model formulation that includes input power sweep was proposed. Compared to the previous work, the new formulation covers a wider power sweep range. The ADS implementation of this model was optimised in a way that it could switch between the small signal and large signal device responses based on the input drive amplitude, which is a key enabler for using this model to design the auxiliary stage of Doherty PAs. An activation function was used to enable this switch between the model responses. The proposed model functionality and accuracy were verified by designing a class C PA and comparing the measurement results of the PA at multiple DC bias voltages with the model's predictions, verifying its accuracy. The same PA will be used in Chapter 6 as the auxiliary stage of a Doherty PA.

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CHAPTER 6

Multi-Bias Asymmetric Doherty PA Design Using Cardiff Model

This chapter focuses on the design and measurement of a multi-bias asymmetric Doherty power amplifier (DPA) designed using Cardiff nonlinear behavioural model at 3.6 GHz. The design is based on a 10 W and a 25 W GaN-on-SiC technology devices. The design process of the main amplifier is discussed in detail here, in particular in relation to the load pull data analysis that was used to identify the correct load modulation scheme to achieve optimal performance. This analysis provided a benchmark result to optimise the combination of the main and auxiliary stage. The auxiliary stage amplifier is identical to the class C amplifier presented in Chapter 5. Using the same main and auxiliary stages, dual and single input variations of the DPA were fabricated.

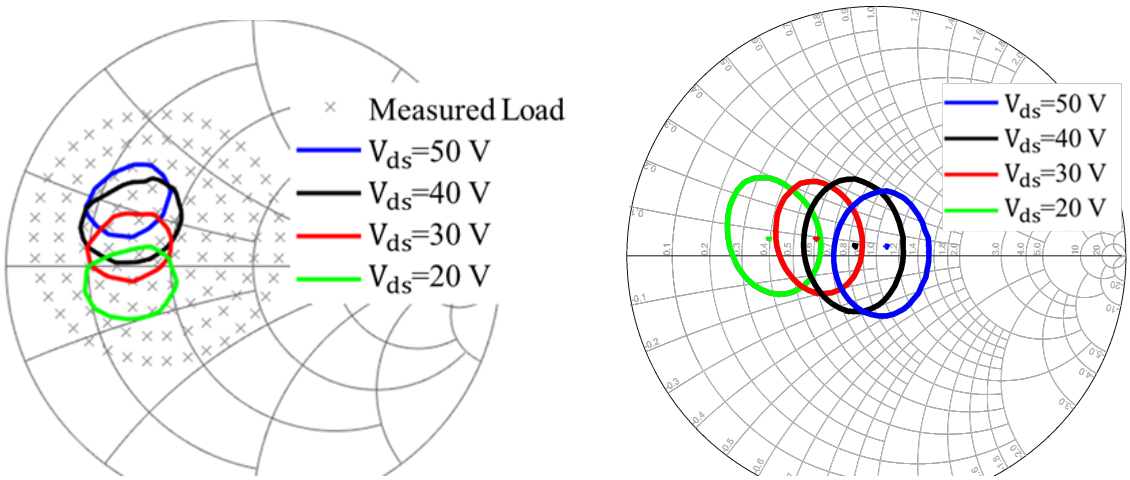
6.1. Main Stage Design

One of the main challenges of designing a DPA is identifying the correct load trajectory of the main stage to achieve high-efficiency at both back-off and peak power levels. In the "Doherty region" as the power increases to reach the peak level, the main stage load is gradually reduced through current injection from the auxiliary stage. In the case of multi-bias DPAs, the optimum load must also change with regard to the DC supply voltage variation which needs to be considered. In addition to efficiency, there are other load-dependent design parameters such as gain, linearity and frequency-bandwidth which need

to be taken in account. Therefore, it is critical to correctly characterise the behaviour of the main stage to identify its optimal performance. This section focuses on experimental characterisation of gain and efficiency of the 10 W GaN-on-SiC HEMT based on load-pull, aiming to provide a tailored framework for design of the main stage of a multi-bias DPA.

6.1.1. Load-pull measurement details

Fundamental load-pull measurements were performed by Ampleon at 3.6 GHz at 4 different DC supply voltages $V_{ds} = 20, 30, 40$ and 50 V using a hybrid load-pull set up. The load-pull grid was selected in a way to capture the optimum load points at all the V_{ds} levels, as shown in Figure 6.1. The DC-dependent Cardiff behavioural model (discussed in Chapter 4 [1]) was used to generate a model from the measurement data which was then imported into the ADS computer-aided design (CAD) simulator for further analysis.

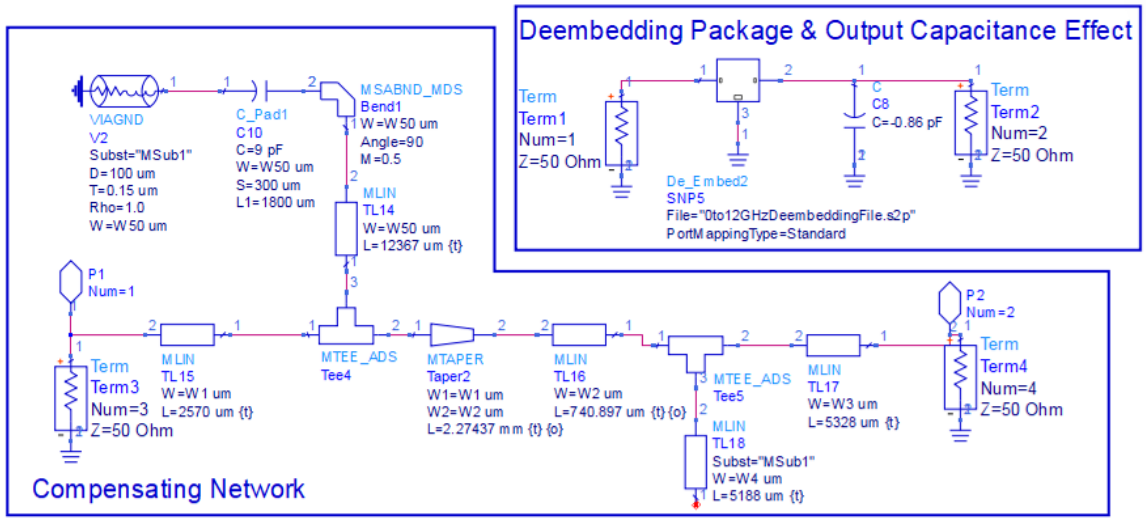


(a) (b)

Figure 6.1: Load-pull grid and 0.5 dB power contours at different V_{ds} levels: (a) at the package reference plane; (b) die plane. The load-pull grid was selected in a way to cover the area around the optimum loads at all the drain bias levels.

For this analysis two different DC supply voltages V_{ds}=30 V &50 V are considered. To negate the effect of output capacitance, associated with the package, the reference plane was moved to the die plane (as shown in Figure 6.1 (b)) by de-embedding process within the

CAD simulator. The de-embedding was done through a passive"compensating network" at the output of the device, as shown in Figure 6.2.



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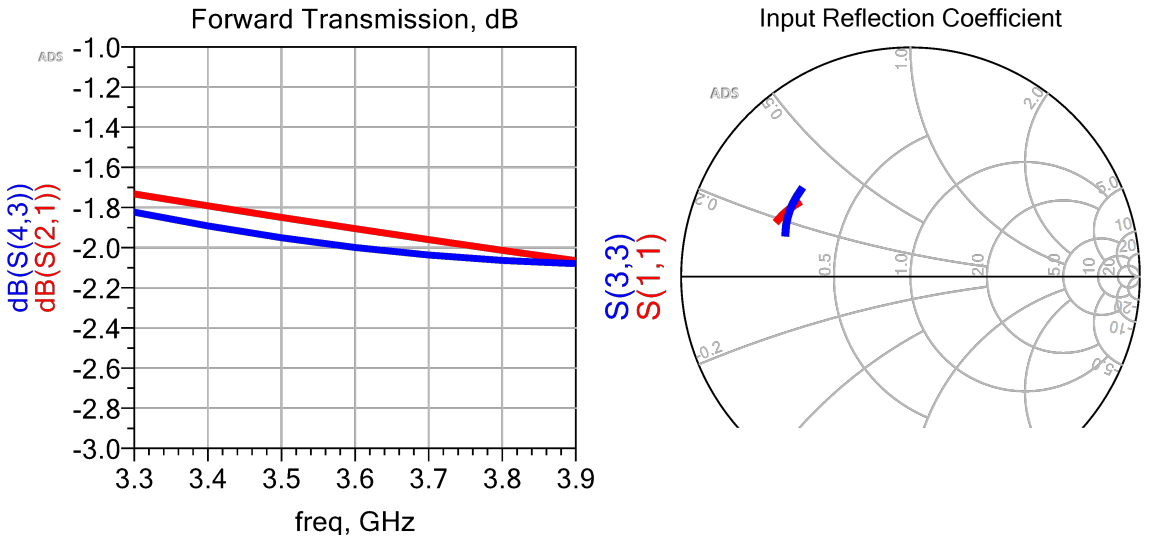


(b)

Figure 6.2: Designing a compensating passive network to de-embed the effect of the packaging and output capacitance of the transistor. (a) Schematic representation of the package deembedding file (S-parameter file generated from package EM simulation) alongside the output capacitance compared to the designed compensating network. (b) Comparing the simulation results of the deembedding file of the package and the output capacitance (S(1,1) and S(2,1)), and the designed compensating network (S(3,3) and S(4,3)). The network was designed in a way to replicate the S-parameters "inverse" of the package and output capacitance.

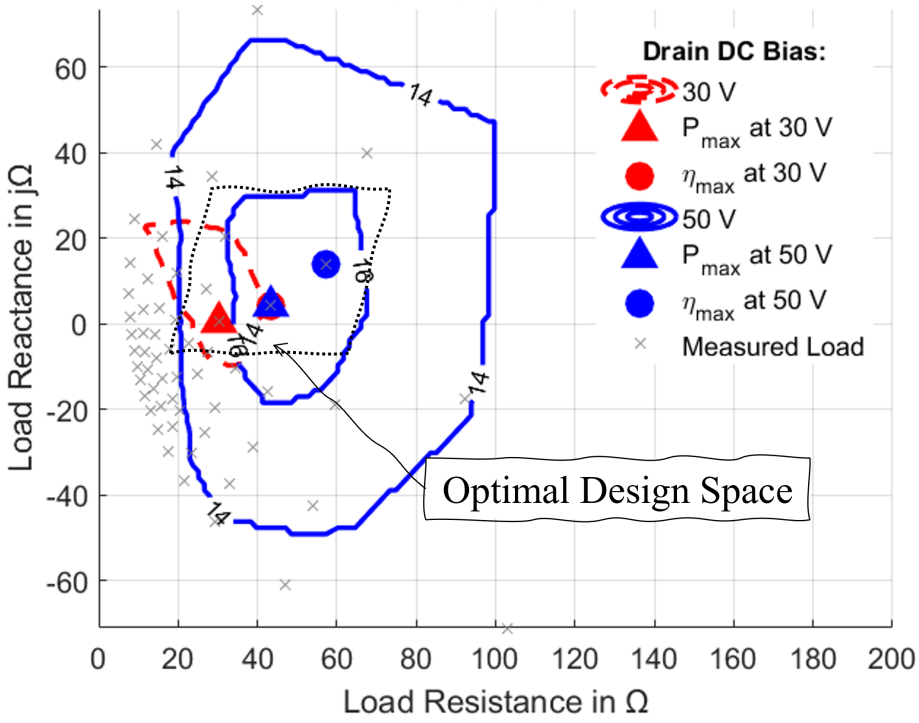
Referencing to Figure 6.2, pieces of microstrip transmission lines (MTLs) were used to design an output matching network which is compensating the packaging and output capacitance effect. The network was design in a way to replicate the S-parameters "inverse" of the package and output capacitance, as shown in Figure 6.2 (b). This will bring the optimum load of the device ($\Gamma_{L,opt}$) closer to the 'real' axis of the Smith Chart, which allows our experimental analysis to match more closely the typical description of Doherty load modulation found in textbooks.

6.1.2. Load-pull Data Analysis

6.1.2.1 Gain

One of the main challenges of designing "multi-bias" PAs is the strong gain reduction that can occur with reducing DC supply voltage, as it was studied in [2] for some GaN HEMT technologies. Therefore, it is critical to investigate the gain variation of the device respective to the changes of DC bias.

Figure 6.3. (a) illustrates that the DUT gain performance is dependent on the load impedance. The same plot also shows the optimum loads for maximum power and efficiency at both DC supply voltages. Thus, the region identified as the "Optimal Design Space" represents the range of load impedance that can be chosen to achieve a desired gain performance at different supply voltages while operating in a Doherty design space. Note, at this stage in our analysis, prior to designing the input matching network, power gain (G_p) is preferred over transducer gain (G_t).



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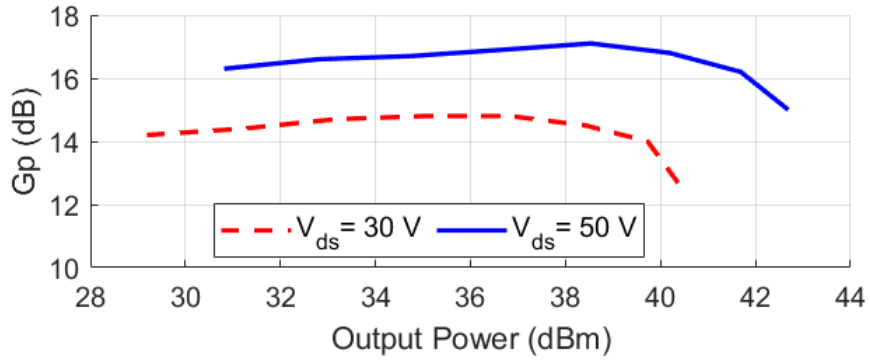


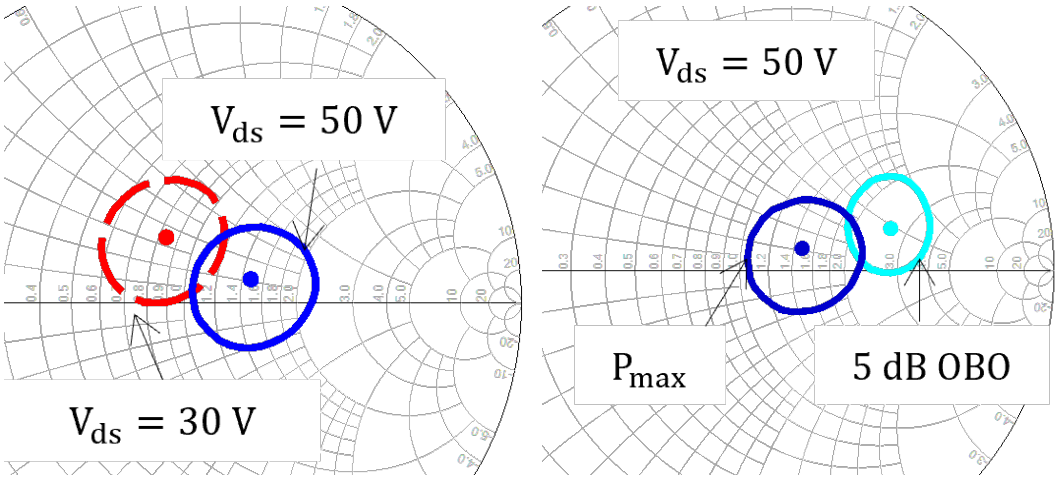
(b)

Figure 6.3: Gain (G_P) characterisation of the DUT at 30 V and 50 V. (a) 14 dB and 16 dB G_P contours and optimum load impedances for both supply voltages at the die reference plane. (b) G_P vs output power (P_{out}) at the optimum load of each supply voltage.

Figure 6.3 (b) shows the G_p performance vs output power for both supply voltages at their respective optimum load impedance for power. This information will be used as a benchmark to compare the final design of the main stage gain performance.

6.1.2.2 Efficiency

In general, the optimum efficiency load changes as a function of the available power P_{av}. The goal of designing a DPA is to correctly track this change and establish a load modulation scheme as a function of P_{av} ($\Gamma_{L,opt} = f(P_{av})$). For a design involving multiple supply voltages, an additional dimension needs to be considered in the load modulation scheme as the optimum load is now also dependent on the supply voltage ($\Gamma_{L,opt} = f(P_{av}, V_{ds})$). Figure 6.4 (a) illustrates the dependency of the optimum load on changes in supply voltages, while its dependency on P_{av} is depicted in Figure 6.4 (b).



(a) (b)

Figure 6.4: 3% efficiency contours at the die reference plane. (a) maximum drive level at $V_{ds} = 30\,\text{V}, 50\,\text{V}$. (b) is $V_{ds} = 50\,\text{V}$ at maximum drive level and 5 dB OBO.

As shown in Figure 6.4 (a), the optimum load has a tendency toward the lower resistive load as the V_{ds} is reduced. On the other hand, as shown in Figure 6.4 (b) for $V_{ds} = 50\,\text{V}$, larger resistive load is needed for an efficient main stage at OBO. Figure 6.5 comprehensively pictures the dependency of optimum load on both supply voltage and drive level ($\Gamma_{L,opt} = f(P_{av}, V_{ds})$).

The behaviour illustrated in Figure 6.5 can provide a benchmark to design a load-modulation scheme to achieve optimal efficiency performance at OBO at various supply voltages.

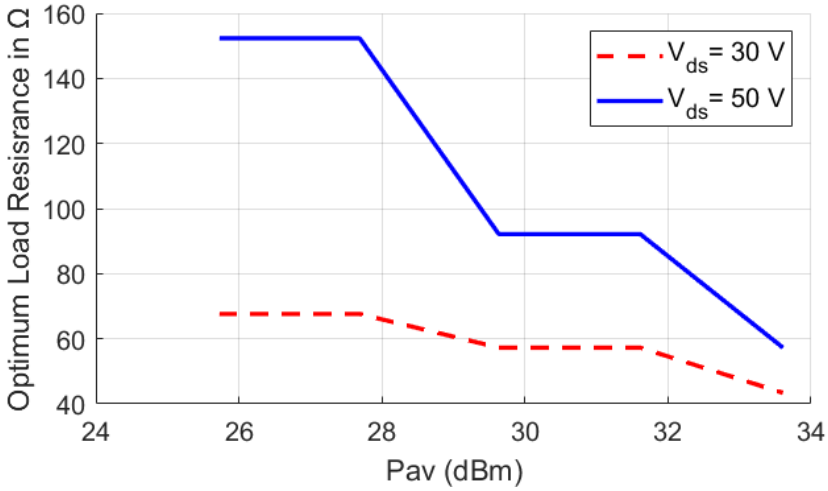


Figure 6.5: Optimum load resistance at the die reference plane vs P_{av} at V_{ds}=30&50 V.

6.1.3. Simulation Results

Based on the information presented in Figure 6.3 and Figure 6.5 a simulation template was designed to investigate the PA behaviour under different load-modulation scenarios. To do so, a look-up indexing table, similar to that shown in Table 6.1, was imported into the simulator environment providing the source power and corresponding load conditions.

Table 6.1: Example of look-up indexing table to, passively, modulate the Main PA load as a function of input drive level.

index	P_{av}	Z_L
1	P_1	Z_1
2	P_2	Z_2
3	P_3	Z_3
⋮	⋮	⋮
N	$P_N = max$	Z_N

As illustrated in Figure 6.5, in order to achieve peak efficiency at each supply voltage, a different load modulation would be preferred. However, this is impractical in a real Doherty where same or similar load modulation can be expected at different bias voltages since the current ratios between main and auxiliary are, in principle, not impacted by supply voltage,

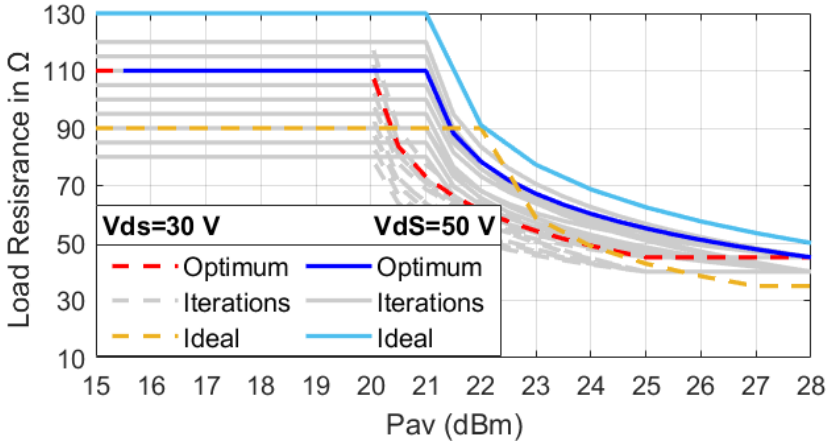
and the Doherty combiner is passive. Therefore, we can use the "look-up table" method proposed here to test load modulation trajectories maintained equal vs. bias conditions against the optimum, independent trajectories.

As an example, Figure 6.6 shows a series of different load modulations, with an OBO of ∼5 dB, compared to the "Ideal" load trajectory. The "Ideal" refers to the simulation setup where separate load modulations were used at each supply voltage to achieve the best Doherty performance at each supply voltage. The "Optimum" refers to the preferable performance under a more practical simulation setup, where the same load trajectory was used for both supply voltages.

As can be seen from Figure 6.6 using the proposed look-up indexing simulation method, the behaviour of the main PA can be investigated under many "Iterations" of the load trajectory. In this example, the "Optimum" load trajectory, ranging from 110 Ω to 45 Ω, provides the best compromise between the gain and efficiency at both supply voltages. Note, as we are only observing the main device, there is no contribution to the output power from an auxiliary PA, therefore OBO is less than 5 dB. However, this analysis sets a firm expectation on the performance of the auxiliary PA to provide a desired load modulation for the main PA.

Figure 6.6 (b) shows the transconductance gain (G_t) (not the G_p which was used initially). This is because the presented simulation results are from the completed circuit design of the main stage including the input match and stability network, as shown in Figure 6.7

Referencing to 6.7, the input matching network consists of two open stubs and a transmission line to match the input of the device from $\Gamma = |0.8|\angle 168°$ (near short circuit edge of the Smith chart) to the centre of the Smith Chart ($\Gamma = 0$). For stabilisation, a parallel R-C network of 3.5 pF and 110 Ω in series with a 2.6 pF capacitor was used on the RF's input path. In addition, a 30 Ω resistor on the gate's DC path was used to further stabilise the circuit at the very low frequencies. Note, the stabilisation analysis was based on the S-



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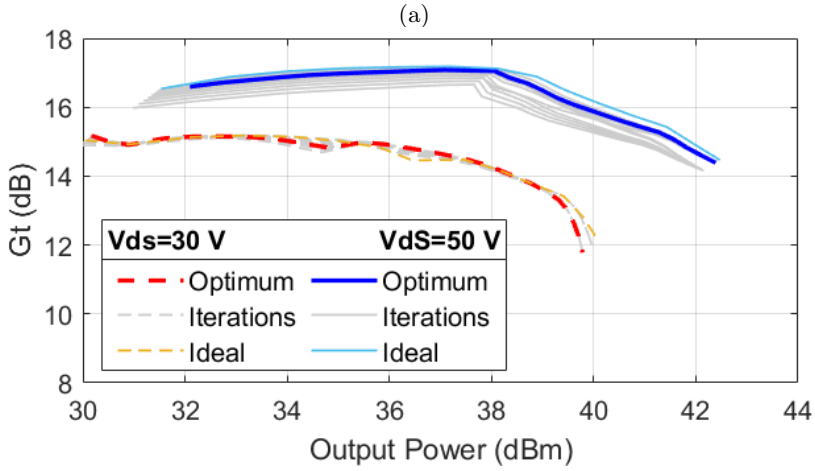

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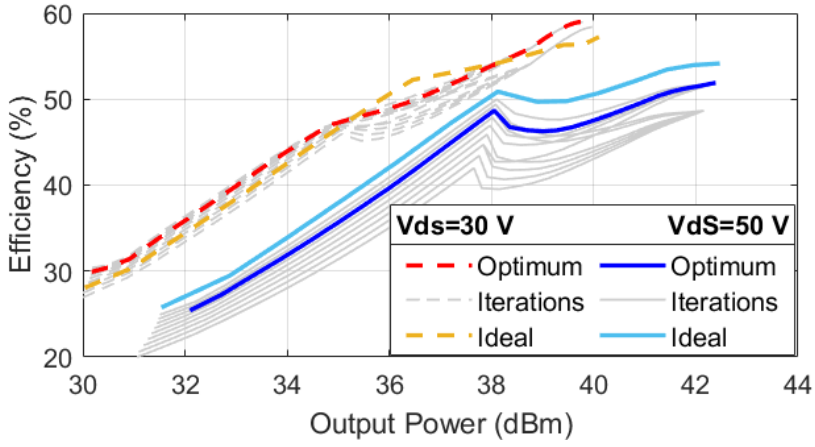


(c)

Figure 6.6: Simulation results of the main PA (Microstrip component design). (a) tested load modulations using a look-up table similar format to Table 6.1 and (b) gain; (c) Efficiency.

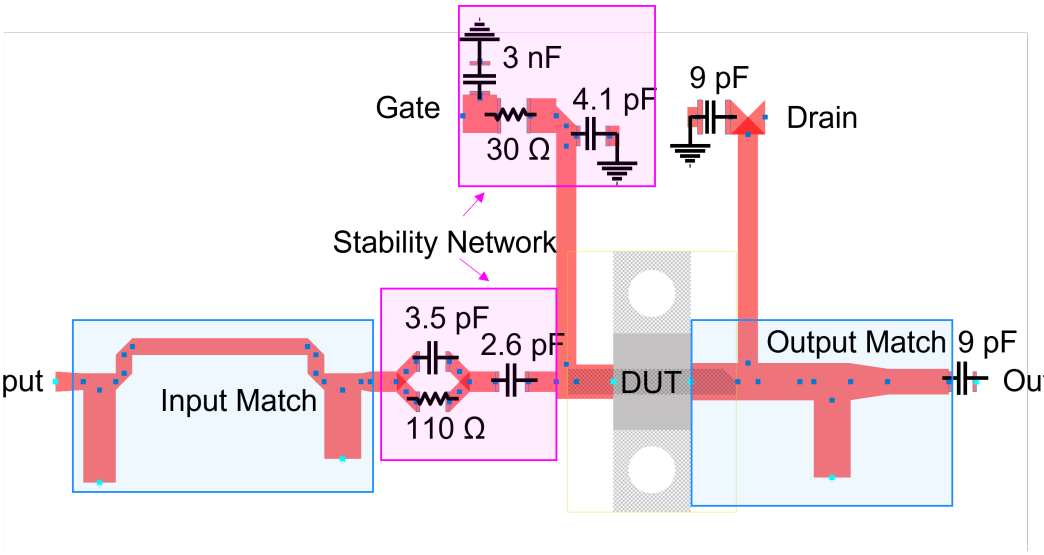


Figure 6.7: Main PA's layout design.

parameter measurement of the DUT from 100 MHz to 12 GHz, where 'stability factor' (also known as 'K' factor) [3] was used as a figure of merit (K>1 was achieved over the whole frequency range).

To this point, our analysis was based on the data at de-embedded reference plane. To evaluate the load trajectories at the package plane, Figure 6.8 shows the "Optimum" load modulation superimposed to the 3% efficiency contours of the DUT at maximum power level and OBO for both 30 V and 50 V supply voltages.

As shown in Figure 6.8 the optimum modulation follows a path from optimal efficiency contour at OBO to the one at maximum power level. However, at the package reference plane the information has lost their link to the theoretical explanation of DPAs (now the optimum load resistance at OBO is lower than at maximum power). On the other hand, as shown in Figure 6.8 it is impossible to distinguish between different iterations and identify the optimum trajectory. Therefore, one might struggle to justify their choice of design solely on the information given at the package reference plane.

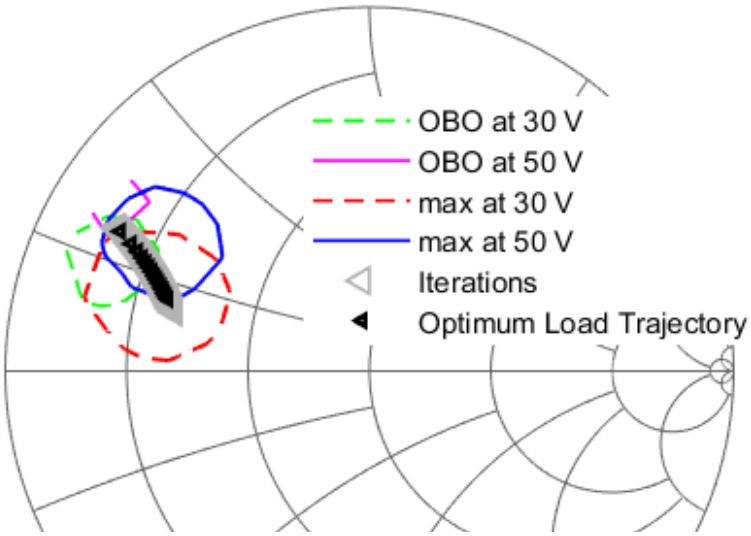


Figure 6.8: Load modulations superimposed to efficiency contours at package reference plane for both 30 V and 50 V supply voltages.

6.2. Combining the auxiliary and main stages

The design of the auxiliary PA was discussed in Chapter 5 where its measurement results were used to verify the capability of the newly developed Cardiff model in designing class C PAs (i.e., PAs with conduction angles less than 180°). A quarter-wave length transmission ($Z = 56\Omega$) line was used to combine the main and the auxiliary stages. Figure 6.9 shows the layout design of the dual-input DPA. The layout design is for a Rogers RO4350B high frequency PCB material with a thickness of and dielectric constant of ε_r=3.66 [4].

As shown in Figure 6.9, an offset line was added at the output of the auxiliary PA to reduce the RF current leakage from the main to the auxiliary stage at the low power level. The length of the offset line was selected in a way that the S_{22} simulation response of the auxiliary stage was around the open-circuit region of the Smith chart ($S_{22} \approx 1$).

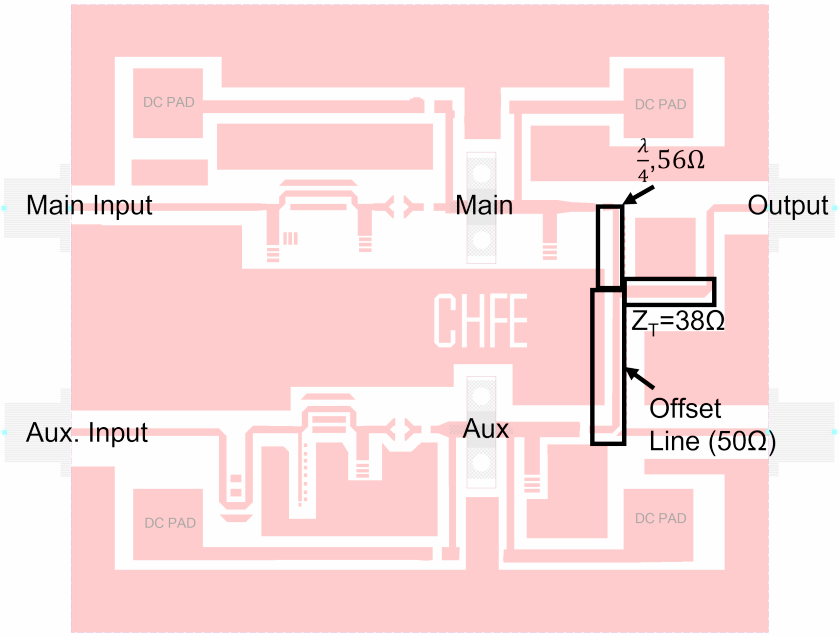


Figure 6.9: Layout design of the dual-input DPA.

6.3. Measurement results

The accuracy of the model was verified through the fabrication and measurement of a dual-input DPA and a single-input variation of the same design. The results from the measurement of the dual-input DPA were used to determine the model accuracy in predicting the input phase, gain, and efficiency. In addition to power measurement, digital predistortion (DPD) measurements were also performed on the single-input variation. The measurement results of both the dual-input and single-input versions are presented and compared in the following subsections.

The power measurement setup is shown in Figure 6.10. To create a pulsed RF signal (with a 10% duty cycle) from the continuous-wave (CW) signal provided by the signal generator (SG), RF switches were used. These switches were triggered by a pulse generator with a 10 μs period and 1 μs pulse width. The reflected and incident input power were measured at each input port using scalar power sensors connected to directional couplers. The output

port of the device under test (DUT) was terminated with a 40 dB high-power attenuator to protect the output power meter. The S-parameters of the attenuator and intermediate cable were used to calibrate the power readings. All of the instruments were connected and controlled using MATLAB, which allowed for flexibility in input phase and power sweep, as well as both RF and DC measurements.

6.3.1. The dual-input DPA

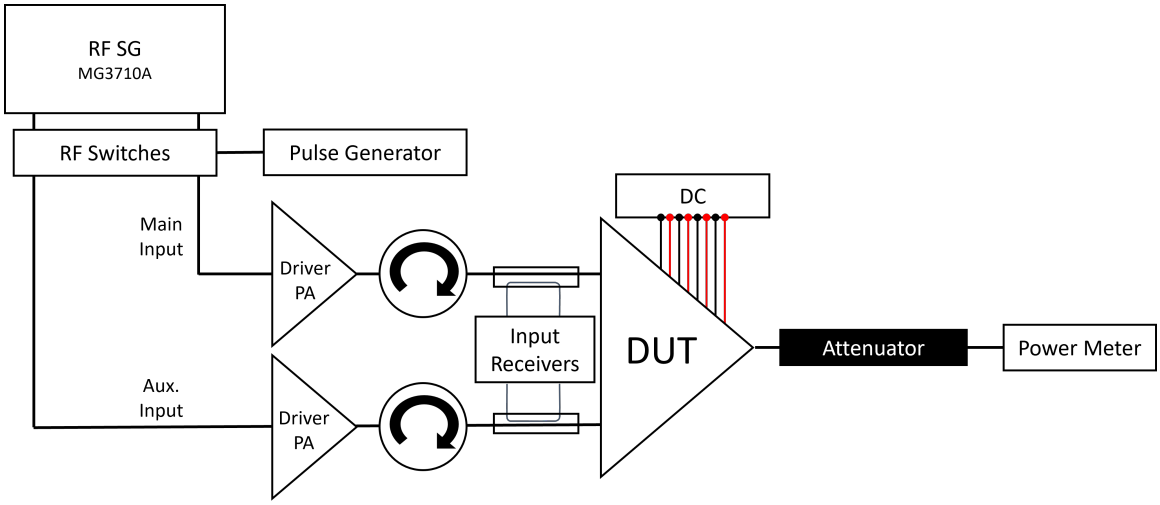
6.3.1.1 Model accuracy in predicting the input phase

For the dual-input DPA it is critical to first find the optimal input phase of the auxiliary PA (respective to the main PA). To find the optimal phase, performance of the DUT was measured over a 360° phase sweep of the auxiliary input with 5° step. The optimal phase was determined at 80°, as shown in Figure 6.11, where the peak output power is measured. The measurement results are referenced to the same planes as the simulation, which are the input connectors of the DUT. It is worth noting that due to the limitations of the measurement setup, the phase difference at the DUT ports could not be directly measured. However, by measuring a known 3-port device (a coupler), the system was calibrated and the correct phase difference at the DUT ports was obtained.

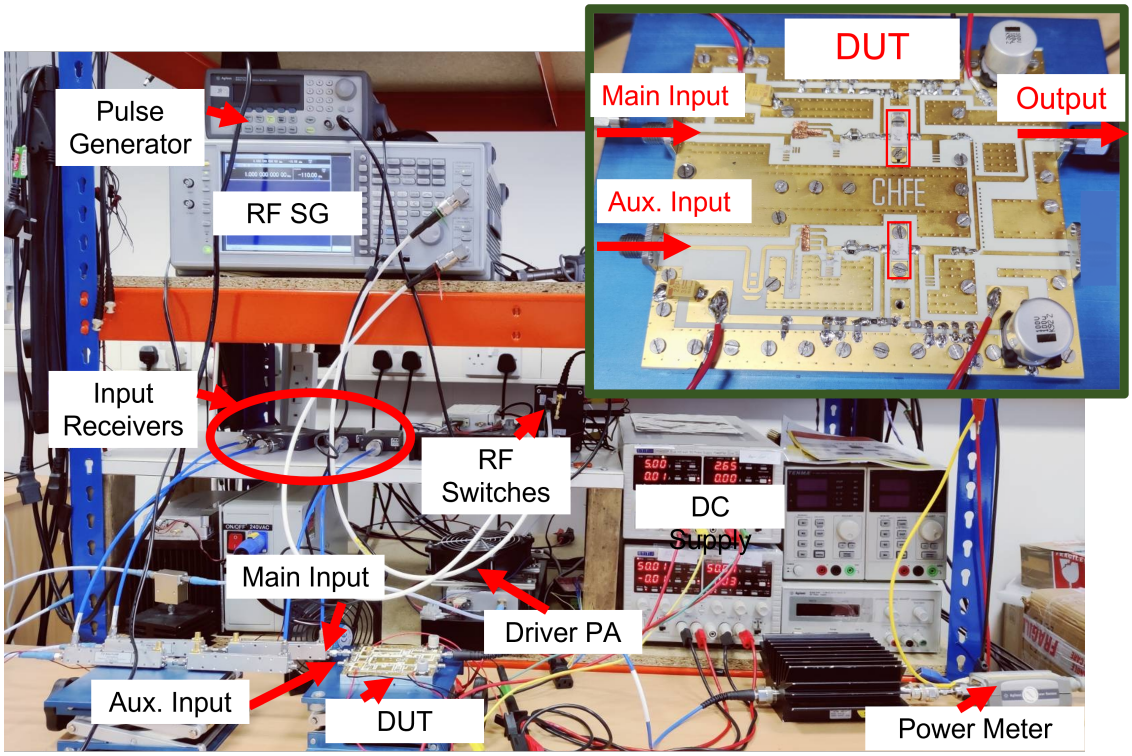
As shown in Figure 6.11, the optimal auxiliary phase predicted by the model was at 95°, which is 15° more than the measured phase. However, the deviation from the maximum power at 95° is small (less than 0.1 dB). This indicates that the model was able to predict the optimal input phase with reasonable accuracy.

6.3.1.2 Optimal performance at different drain bias conditions

After the optimal input phase had been identified, the performance of the dual-input DPA was measured for various combinations of input drive levels using a "nested" sweep algorithm in which the auxiliary power was the inner sweep and the main stage power was the outer



(a)



(b)

Figure 6.10: (a) Block diagram and (b) photograph of the measurement setup and the DUT (the dual-input DPA). Using RF switches (triggered by a pulse generator), a pulsed signal with 10% duty cycles was created from the original CW signal from SG.

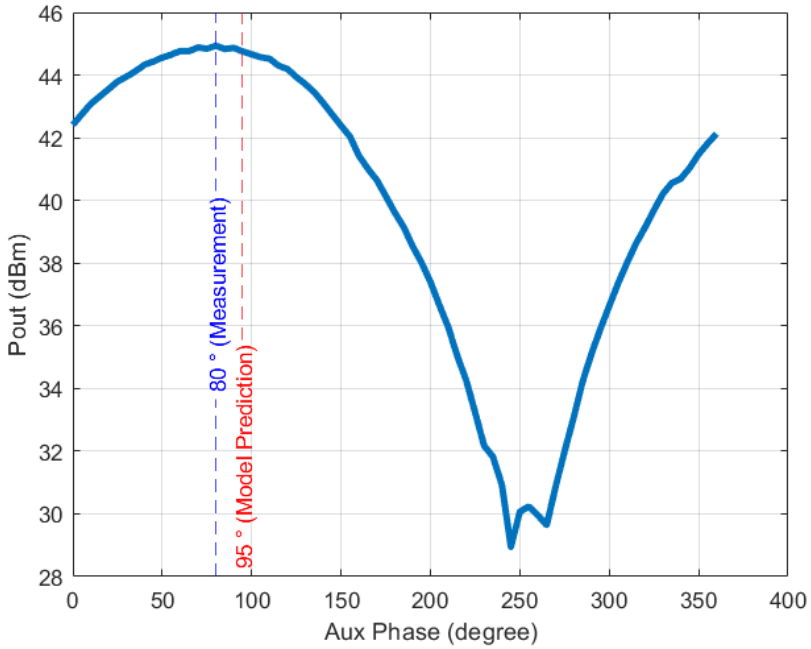
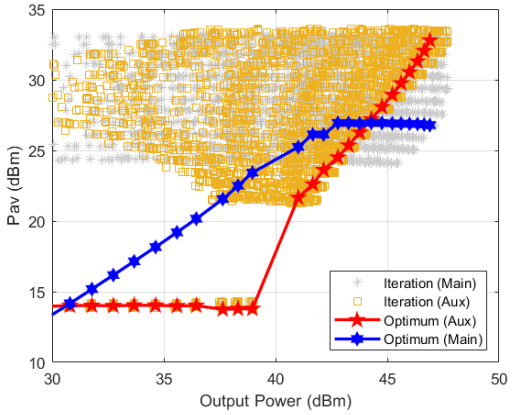


Figure 6.11: Output power performance of the dual-input DPA vs input phase sweep. The optimum phase are 80° and 95° from measurement and simulation results, respectively.

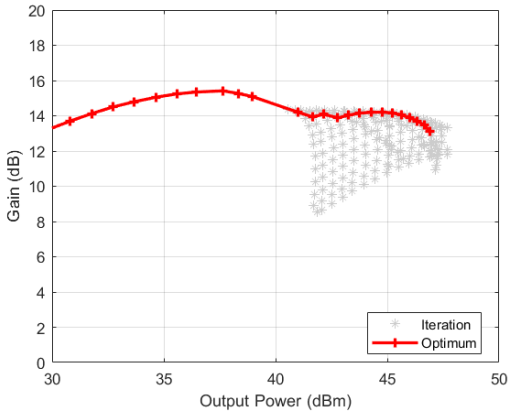
sweep. This resulted in a "cloud" of points from which optimal performance could be selected by choosing a desired set of input drive levels for the main and auxiliary stages. Figure 6.12 shows an example of "iteration" points and optimal performance at V_{ds}=50 V and f_0=3.6 GHz.

The device performance was measured at different DC drain supply voltages from 30 V to 50 V with 5 V steps where the gate bias was fixed at $V_{gs}(Main)$=-2.63 V and $V_{gs}(Aux.)$=-4 V. At each drain supply voltage optimal input trajectory was selected to achieve the efficiency and gain performance in 6.13.

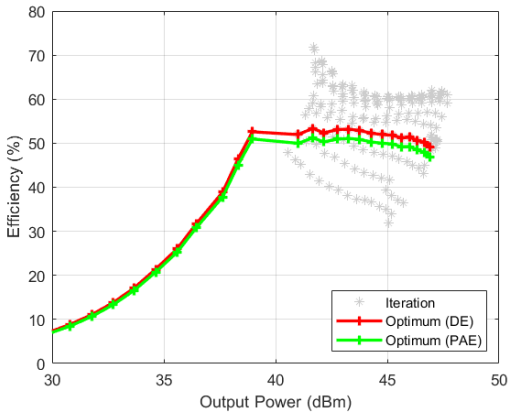
As shown in 6.13, more than 10 dB of gain have been achieved at all the supply voltages. Maximum output power is around 47 dBm at V_{ds}=50 V and the worst power level with 50% efficiency is around 35 dBm at V_{ds}=30 V. Comparing the OBO peak efficiency at 45 V to 50 V it is noticeable that there is a minimal improvement in the OBO performance (less than 0.5 dB improvement in the OBO level). However, a more substantial improvement (more



(a)



(b)



(c)

Figure 6.12: Cloud of "iteration" points and selected optimum performance: (a) available power;(b) gain; (c) efficiency.

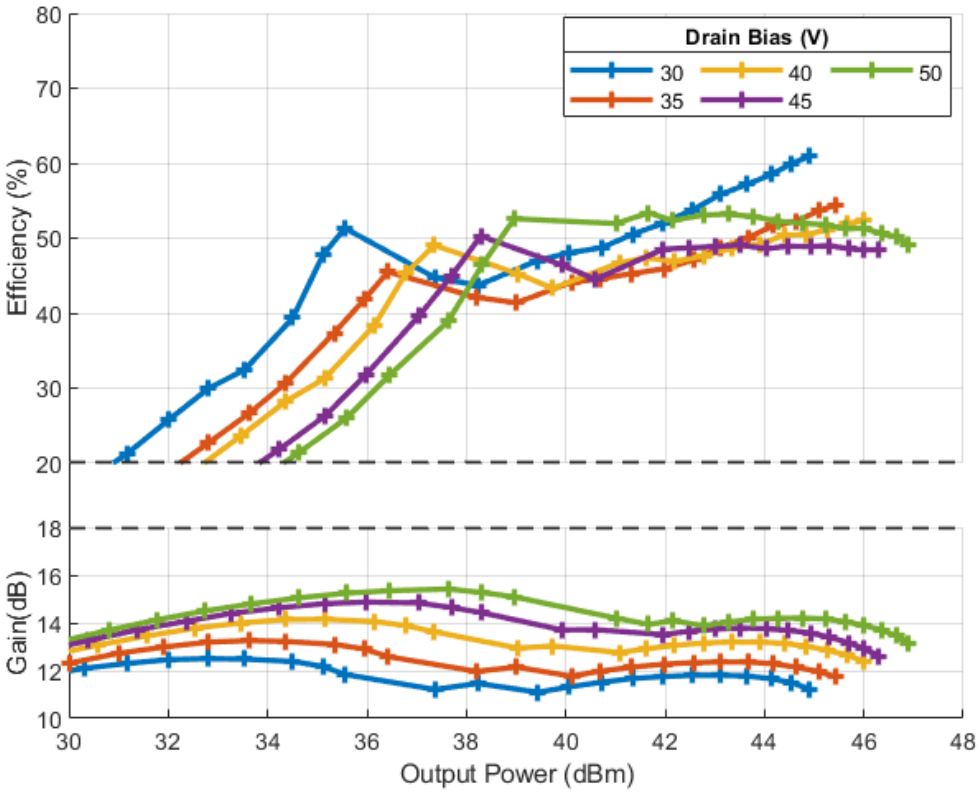
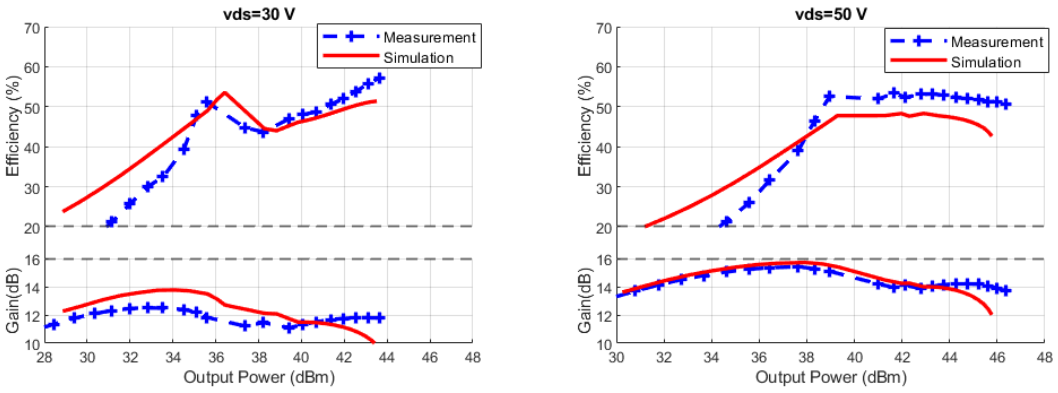


Figure 6.13: Optimal efficiency and gain performance of the dual-input DPA at different drain bias levels. The measurement results were collected at f_0=3.6 GHz, $V_{gs}(Main)$=-2.63 V and $V_{gs}(Aux.)$=-4 V.

than 1 dB improvement) in the OBO level was observed as the drain voltage changed to 40 V and 30 V.

6.3.1.3 Measurement vs simulation results

To compare the measurement results with the corresponding simulation results of the Cardiff model, the same optimal input trajectories at 30 V and 50 V from the measurement data were used within the CAD simulator. The simulation results were comparable with the measurement results, as shown in Figure 6.14.



(a) (b)

Figure 6.14: Measurement vs simulation results at (a) V_{ds}=30 V, (b) V_{ds}=50 V. The difference between the modelled and measured result in the high power regions could be ascribed to different harmonic termination between the original dataset (which the model was based on, with harmonics close to 50 Ω) and the designed PA, where harmonics where nearly short-circuited.

As it is notable from the comparison shown in Figure 6.14, the difference between the modelled and measured results can be witnessed at maximum power level. This deviation could be ascribed to different harmonic termination between the original dataset (which the model was based on, with harmonics close to 50 Ω) and the designed PA, where harmonics where nearly short-circuited.

6.3.1.4 Frequency response of the dual-input DPA

The large signal Cardiff model used in this design was only developed at 3.6 GHz. However, S-parameter simulation results were used to ensure that the matching networks are not narrow-band. Figure 6.15 shows performance of the dual-input DPA at both maximum power and 10 dB OBO levels over 400 MHz frequency bandwidth (a) at 30 V and (b) 50 V.

For the $V_{ds} = 30\,V$, the maximum output power (Pout_{max}) is higher than 43 dBm and the back-off efficiency (η_{OBO}) over the 3.3-3.7 GHz frequency band. At $V_{ds} = 50\,V$ the Pout_{max} is more than 45 dBm over the 3.35-3.75 GHz frequency band with more than 40% η_{OBO}. Due to the higher gain at back-off, there is only small difference (2 to 3%) between the drain efficiency (η_{OBO}) and the power added efficiency (PAE_{OBO}).

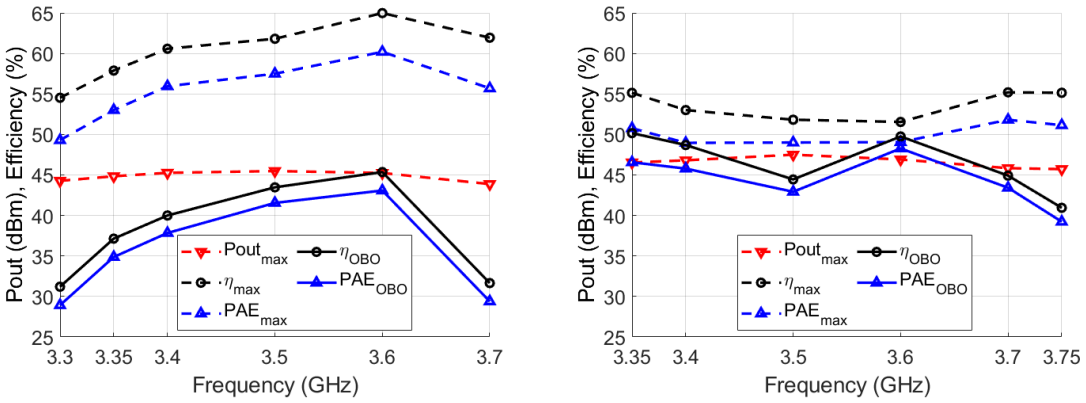


Figure 6.15: Bandwidth performance of the dual-input DPA: (a) V_{ds}=30 V; (b) V_{ds}=50 V.

6.3.2. Single-input DPA

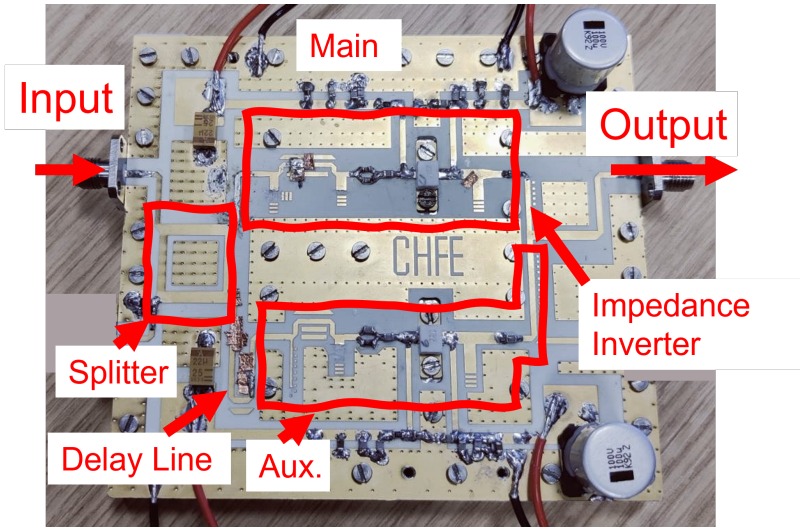
The dual-input DPA has the advantage of being able to independently control the auxiliary ON and OFF states, which adds additional flexibility. However, this also adds complexity in terms of finding the optimal combination of input signals to achieve desired performance, such as identifying the optimum input trajectory to attain optimal back-off efficiency.

In a single input DPA, signal path is divided by a passive splitter between the main and auxiliary stage. This allows limited adjustment (compared to the dual input DPA) which can be made by changing the gate bias voltages and unequal input signal split. For example, to achieve better back-off performance, the auxiliary can be biased in a deeper class C; hence, avoiding unwanted conduction by the auxiliary PA at the back-off. Deeper class C bias condition would result in lower gain at auxiliary stage. An unequal split allows for limited adaptability to compensate for the gain reduction and ensure that the auxiliary stage can reach its peak power level.

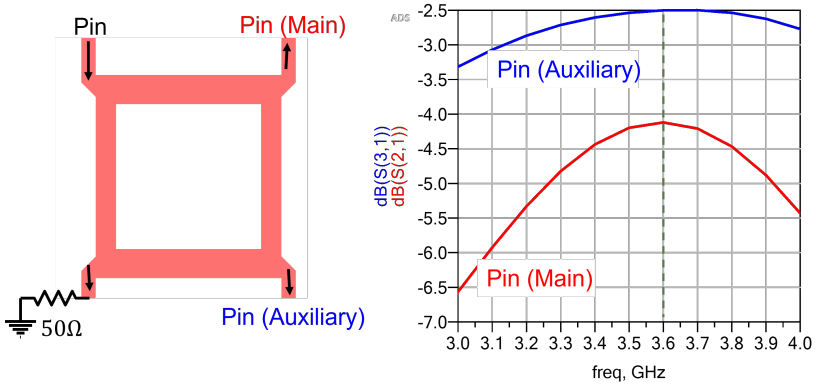
A single input version of the same design was also fabricated. The design was exactly the same as the dual-input DPA but the added unequal-split branch line coupler [5]. Due to the limitation in the data at deeper class C configuration (the lowest measured gate bias in the original data was -4 V) the simulation results of the single-input were not desirable. Instead, simulation results of the Dual-input DPA was used as a guide to design the unequal splitter. It was shown that the auxiliary's peak input power was 1.5 dB larger than main. Therefore, a 1.5 dB unequal splitter was designed. Figure 6.16 shows (a) Photograph of the single input DPA and (b) EM layout and simulation results of the unequal splitter.

6.3.2.1 Single vs dual input DPA

The optimum auxiliary gate bias voltage was empirically identified as -5V and -6V for for 30V and 50V drain supplies, respectively. Figure 6.17 compares power added efficiency (PAE) and gain performance of the dual and single input DPAs. It is clear that the dual-input DPA has a superior gain performance (more than 2 dB) compared to the single input PA. Reduced gain performance of the single input DPA is as a result of power loss in the passive splitter and the deeper class C bias condition. It is difficult to draw an apparent conclusion about the PAE performance based on these specific results. The outstanding 10 dB flat PAE performance (more than 45%) of the single input DPA at V_{ds}=50 V outperforms the dual-input DPA with around 8 dB OBO. At V_{ds}=30 V it is evident that the dual-input DPA



(a)



(b)

Figure 6.16: (a) Photograph of the single input Doherty power amplifier; (b) EM layout and simulation result of the input unequal-splitter. The input power level of the auxiliary is around 1.5 dB larger than main stage at 3.6 GHz

has superior power performance with more than 2 dB. On the other hand, single input DPA can perform more efficiently at the lower power levels. Based on these specific results, a different non-determinative conclusion can be drawn. The Dual-input DPA has a better gain and PAE performance up to 12 dB OBO. However, the single-input DPA can achieve further OBO (around 14 dB) with reduced gain and PAE.

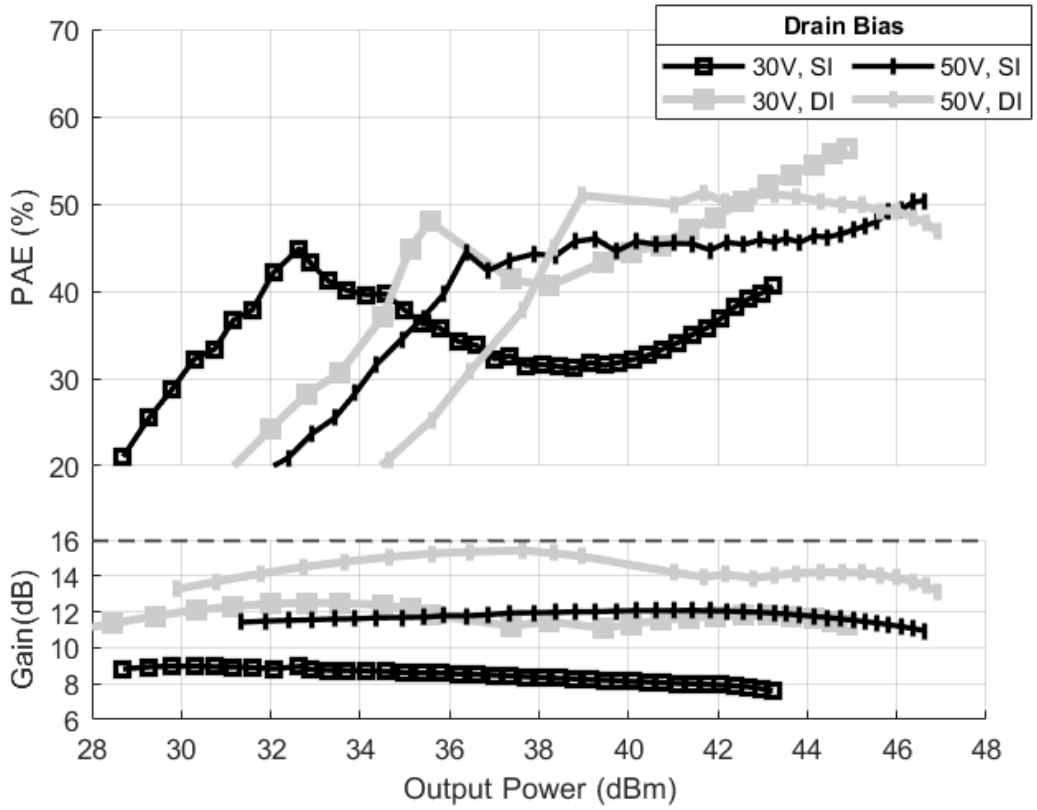


Figure 6.17: Single input DPA (black line) vs Dual-input (grey line) performance at different drain bias voltages at 3.6 GHz.

Performance of the single-input DPA was measured under 400 MHz bandwidth from 3.3 GHz to 3.7 GHZ with 50 MHz step. At each frequency, data at different combination of main and auxiliary gate bias conditions at $V_{ds} = 30, 50\,V$ was collected. This allowed for selecting the optimum gate bias condition to achieve optimum performance at each frequency. Figure 6.18 summarises performance of the single-input DPA at peak (dashed-lines) and 10 dB back-off(solid-lines) output power levels: (a) 30 V and (b) 50 V supply

voltages. The top x-axis shows the gate bias combination (i.e., in "main,auxiliary" format) at each frequency.

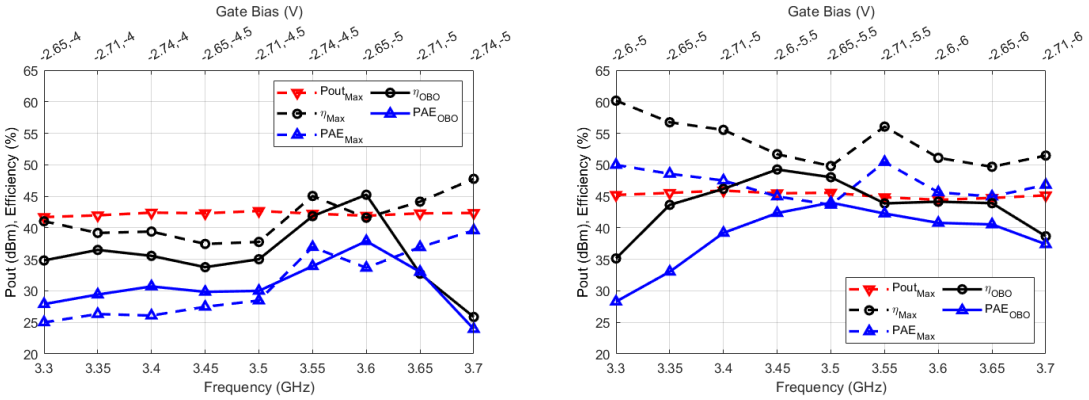
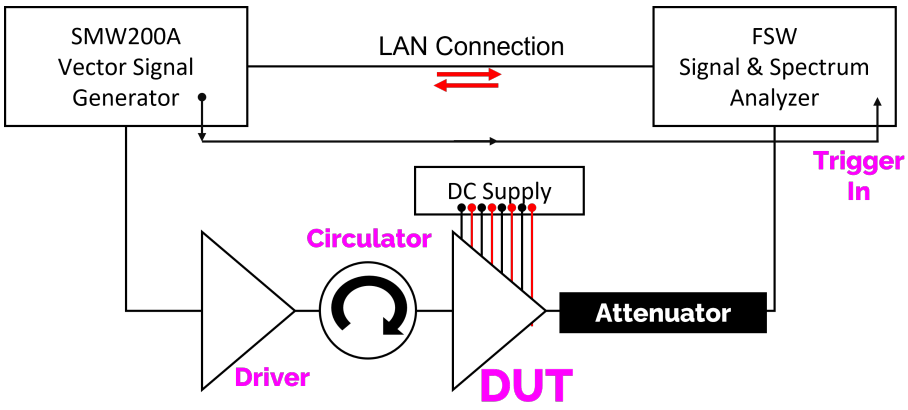


Figure 6.18: Single input DPA at frequency performance at the peak (dashed-lines) and 10 dB backe-off(solid-lines) output power levels. Drian supply voltage: (a) 30 V, and (b) 50 V.The top x-axis shows the corresponding gate bias combination (in the 'main,auxiliary' format) at each frequency.

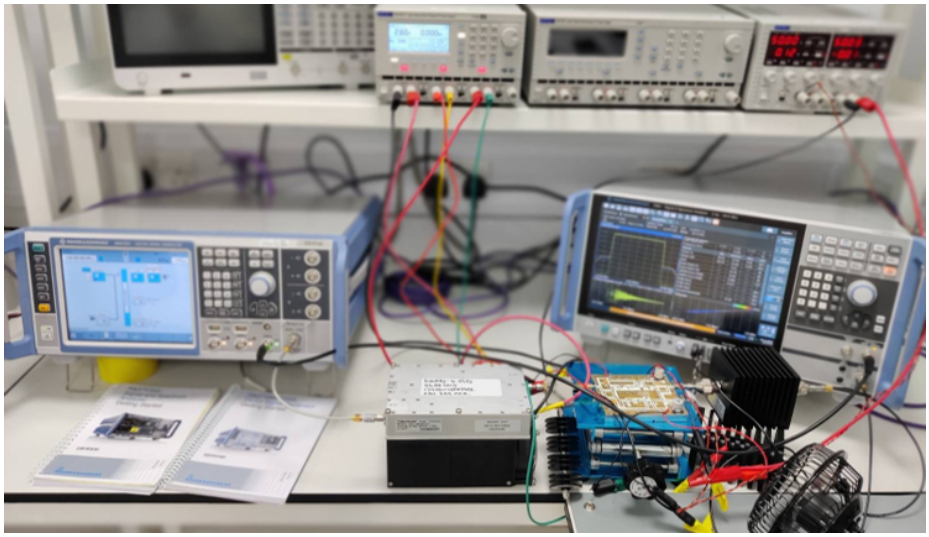
6.3.2.2 Linearity and digital pre-distortion (DPD)

For the single-input DPA, "system-level" characterisation was also performed using a 100 MHz down link 5G test signal with around 12 dB of PAPR. Figure 6.19 shows the block diagram of the digital pre-distortion (DPD) setup. An iterative DPD algorithm which is embedded within the FSW signal and vector analyser was used. The algorithm updates the SMW200A vector signal generator in real-time to achieve lowest error vector magnitude (EVM) across the measurement bandwidth (which was 300 MHz for this measurement).

Figure 6.19 reports the output spectra of the single input DPA with and without DPD at (a) V_{ds}=30 V and (b) V_{ds}=50 V. The native Adjacent Channel Leakage Ratio (ACLR) is around -25 dBc and -30 dBc at V_{ds}=30 V and $V_{ds} = 50\,V$, respectively. The adaption of DPD improves the ACLR to around -45 dBc with an EVM of less than -0.9%. The average efficiency was 52% and 47% at 30 V and 50 V bias, respectively.

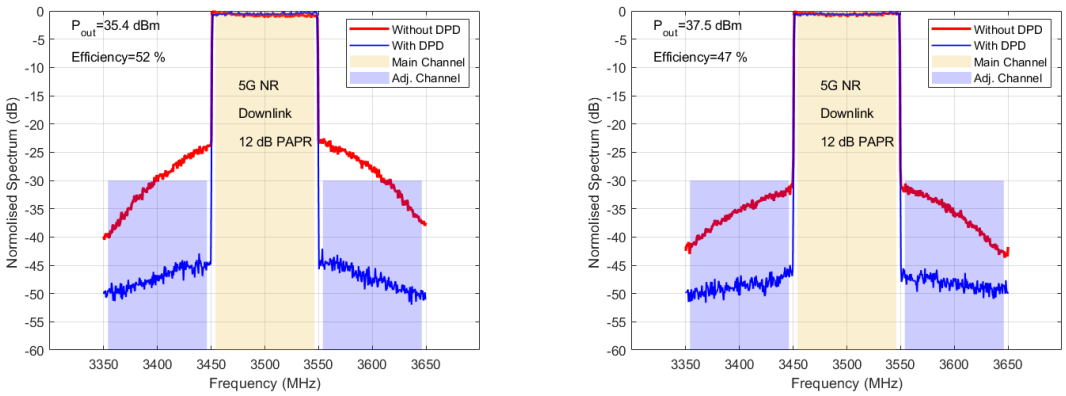


(a)



(b)

Figure 6.19: Block diagram and photograph of the DPD measurement setup. DPD is performed via an iterative algorithm on FSW Signal & spectrum analyzer which updates the SMW200A Vector Signal Generator via LAN connection in real-time.



(a) (b)

Figure 6.20: Measured spectra with 5G FR1 downlink test signal (100 MHz channel with 15 dB PAPR), single input. Without pre-distortion: red; With pre-distortion: blue. (a) V_{ds}=30 V and (b) V_{ds}=50 V.

6.3.3. Summary

In this chapter, the accuracy of the Cardiff model was verified by fabricating and measuring dual-input and single-input versions of a DPA. A detailed load-pull analysis, including the identification of the optimal load trajectory of the main stage and the design of the output matching network to compensate for the package's parasitic, was included. The optimal input phase of the dual-input DPA was empirically identified and compared with the simulation results. Its performance was measured for various combinations of input drive levels using a "nested" sweep algorithm. The measurement results were found to be in good agreement with the simulation results, verifying the accuracy and applicability of the newly developed Cardiff model for designing Doherty power amplifiers.

The single-input DPA had an unequal splitter at the input, leading to lower gain due to the relatively higher power delivered to the auxiliary which is OFF at small signal. The auxiliary is also biased at deeper class C, leading to output power reduction at saturation. By applying DPD measurement, an ACLR of less than -45 dBc with an efficiency of more than 47% was achieved for a 100 MHz 5G test signal at multiple bias points.

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CHAPTER 7

Temperature-Dependent Cardiff Model

Temperature is a crucial factor that must be taken into account when designing radio-frequency power amplifiers (RFPAs). By utilising a thermal-dependent model that considers self-heating effects, designers can accurately evaluate their circuit performance under different signal conditions. In addition, designers can evaluate the performance of their circuits under various thermal conditions and, if necessary, implement effective thermal management strategies to improve performance.

This chapter presents the development of a new Cardiff model formulation that takes into account the effects of temperature on device performance. The proposed model is validated using load-pull measurements of two GaN-on-SiC devices with different output power ratings. In addition, the model was implemented into the ADS simulator and used to design a class AB RFPA. The results of this design process demonstrated the accuracy and functionality of the new temperature-dependent Cardiff model.

7.1. Including Temperature Into Cardiff Model

So far, the Cardiff model coefficients have been independent of temperature variations. This means that by using the traditional Cardiff model (7.1) formulation, it is not possible to generate a temperature-dependent model that can interpolate or extrapolate with respect to temperature. Instead, temperature could be used as a look-up indexing parameter in the model. Hence, in order to generate a behavioural model capable of predicting the device's

performance at different temperature levels, load-pull data at each simulation temperature is required.

$$B_{p,h} = (\angle A_{1,1})^h \cdot \sum_{r=0}^{1} \sum_{n=n_{min}}^{n_{max}} K_{p,h,m,n} \cdot |A_{2,1}|^m \cdot \left(\angle \frac{A_{2,1}}{A_{1,1}}\right)^n \tag{7.1}$$

where,

$$\begin{cases} n_{\min} = -(w - h/2 - r) \\ n_{\max} = h + (w - h/2 - r), \end{cases}$$

and, the 'p' is the port index and 'h' is the harmonic index, referenced to the fundamental frequency 'f_0'. The parameters 'm' and 'n' denote the coefficient related to the magnitude and phase exponents, respectively, of the RF stimulus phasor '$A_{2,1}$', which is the incident wave at the fundamental at the output port of the device, representing the load pull operation. The 'm' and 'n' are related as '$m = |n| + 2r$' where 'r' is the magnitude indexing term. For DC current ($h = 0$) the term "$B_{2,0} \triangleq I_{2,0}$". The parameter '$w$', determines the mixing order and the number of coefficients of the model '$K_{p,h,m,n}$'.

To incorporate temperature variations into the Cardiff model formulation, temperature was treated as a stimulus that interacts with the RF stimulus. This approach is similar to the inclusion of DC bias, as discussed in Chapter 4. As a result, the coefficients $K_{p,h,m,n}$ become temperature dependent. This interaction can be mathematically represented as follows:

$$K_{p,h,m,n}(T) = \sum_{l=0}^{l_{max}} Q_{p,h,m,n,l} \cdot T^l \tag{7.2}$$

Where '$Q_{p,h,m,n,l}$' is the new temperature-dependent Cardiff model's coefficients. Parameter l_{max} is the temperature fitting order which needs to be defined using experimental data (covered in Section 7.2.1). Consequently, a new Cardiff model formulation can be generated by including temperature variation in the model's coefficients. The new formulation can be used to interpolate and/or extrapolate the load-pull measurement data at various temperatures:

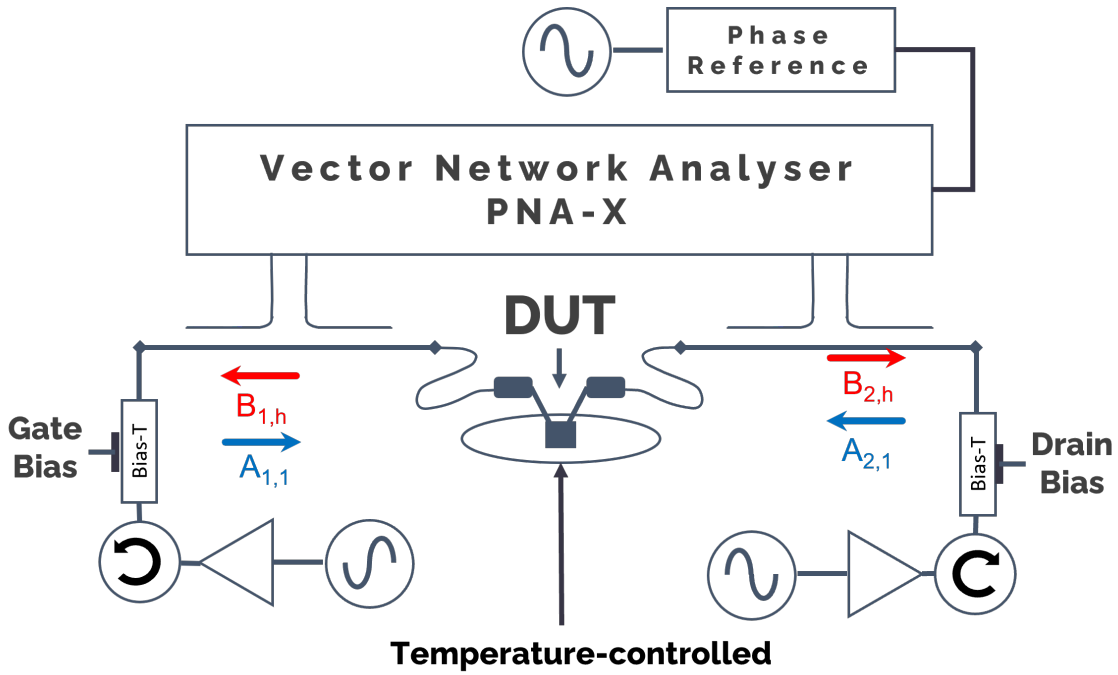
$$B_{p,h} = (\angle A_{1,1})^h \cdot \sum_{r=0}^{1} \sum_{n=n_{min}}^{n_{max}} \left\{ \sum_{l=0}^{l_{max}} Q_{p,h,m,n,l} \cdot T^l \right\} \cdot |A_{2,1}|^m \cdot \left(\angle \frac{A_{2,1}}{A_{1,1}} \right)^n \tag{7.3}$$

7.1.1. Measurement Strategy

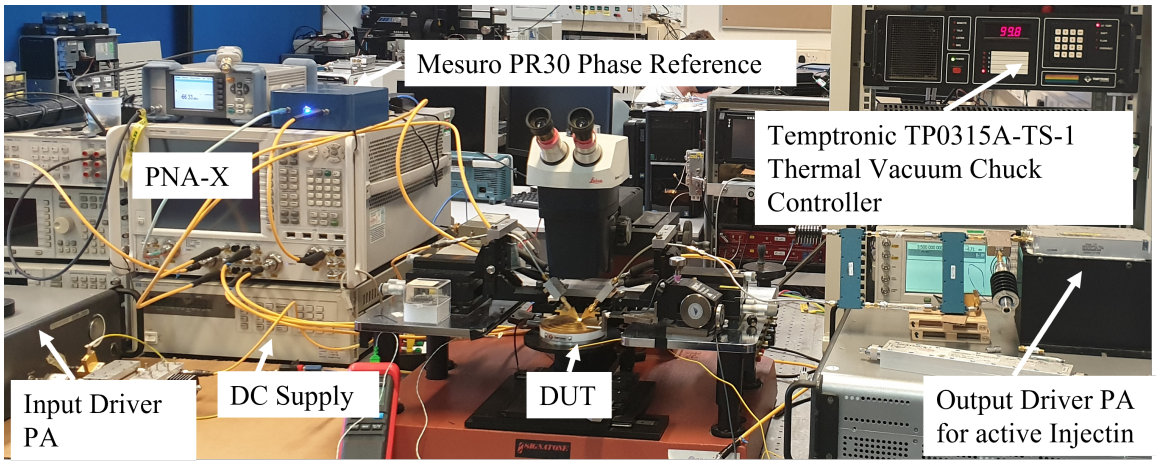
The load-pull measurements were conducted statically using continuous-wave (CW) excitation at 3.5 GHz. During this experiment, only fundamental load-pull measurements were performed, and harmonic frequencies were terminated at the system impedance. Figure 7.1 shows (a) a block diagram and (b) an image of the active load-pull measurement system used in this experiment. The device-under-test's (DUT's) performance was measured at various chuck temperatures (T_{chuck}), from 25 °C to 100 °C with a 15 °C step. This temperature range was chosen in a way taking into account both the limitations of the measurement setup and device safety. The controlled temperature starts at 25 °C, representing the lower limit, and the highest temperature was selected to ensure the safe operation of the DUTs under CW excitation. At the same time this range is significant for real world operation as it exceeds the standard 70 °C used for commercial application.

This temperature range was selected in a way to consider the measurement setup limitation and the device safety, as the lowest controlled temperature with the setupemperature of 25 °C as the and the highest temperature was selcted in a way to insure the safe operation of the DUTS under the CW excitation.

In the first instance, a GaN-on-SiC high electron mobility (HEMT) from Ampleon was measured (Device 'A' in Figure 7.2). The device was mounted on a copper carrier (case) using highly conductive thermal paste. The DUT was biased in class AB with drain voltage at V_{ds}^{DC}=50 V, and gate bias voltage V_{gs}^{DC}=-2.6 V with drain-source current of I_{ds}^{DC}=16.6 mA. An 4× larger device from the same technology was also measured (Device 'B' in Figure 7.2) at V_{ds}^{DC} = 50 V and V_{gs}^{DC}=-2.7 V with I_{ds}^{DC}=40 mA. Note, an additional packaged device (device C) was also measured which is discussed in Section 7.3. Table 7.1 compares the



(a)



(b)

Figure 7.1: Real-time, active load-pull system (a) Block diagram, and (b) photograph of the system at CHFE, Cardiff University. A temperature-controlled RF chuck was used to measure the device behaviour at various temperatures ranging from 25 °C to 100 °C.

different GaN HEMT devices whose measurement results are discussed in this chapter.

Table 7.1: Comparison of the different GaN HEMT devices used in this chapter.

Device ID	Manufacturer	Output Power	Package Type
A	Ampleon	2 W	Die
B	Ampleon	8 W	Die
C	Wolfspeed	10 W	Packaged

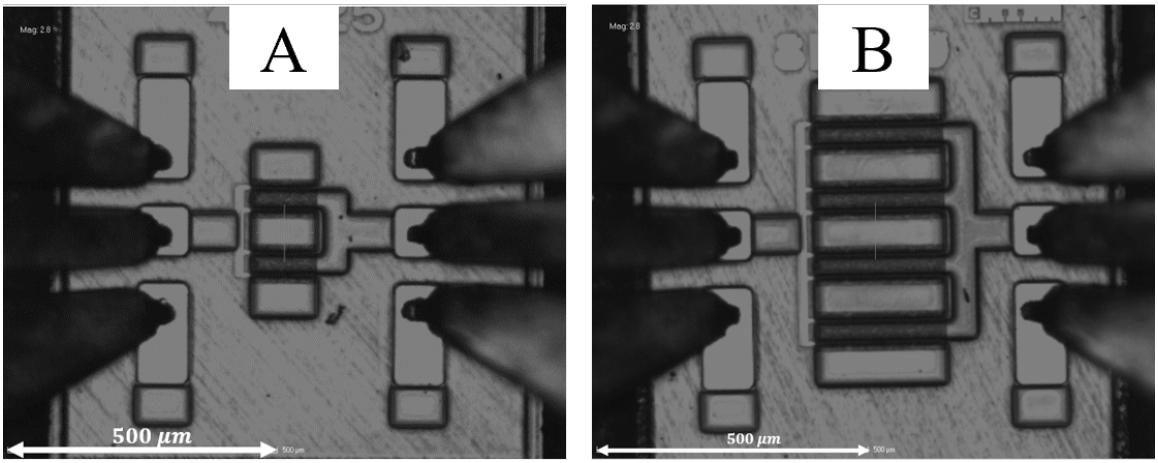


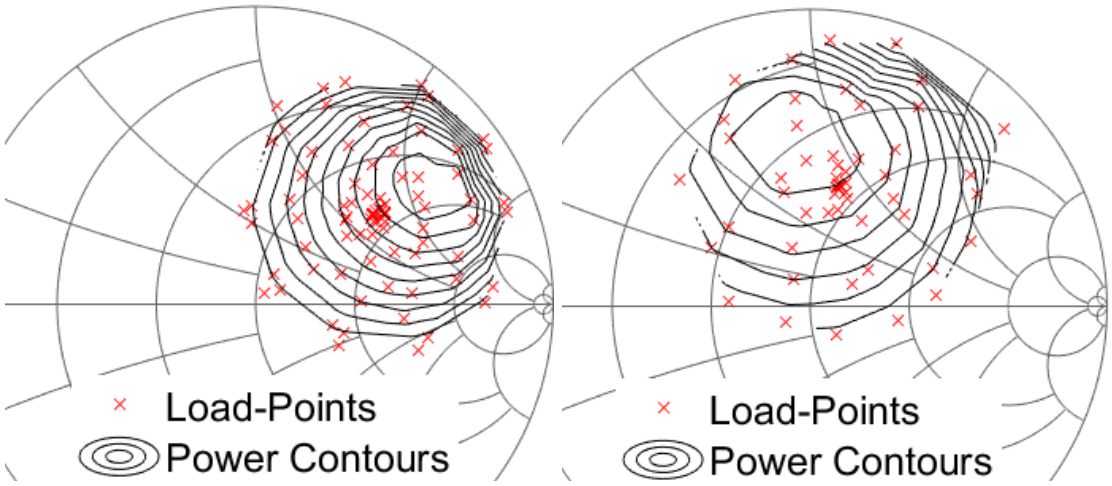
Figure 7.2: Device 'B' is 4 times larger in periphery than 'A'. Both devices were measured at various chuck temperatures from 25 °C to 100 °C with a 15°C step.

Figure 7.3 shows the load-pull measurement grid of, (a) the device 'A' with 91 load points, and (b) the device 'B' with 57 points. The grids were selected in a way to capture optimum load points. The 0.5 dB contours are also superimposed from maximum output power of (a) 34.6 dBm, and (b) 39.8 dBm at T_{chuck}=25 °C.

7.2. Verification

7.2.1. Finding temperature's mixing order 'l_{max}'.

Defining the correct mixing order is critical to accurately truncating the polynomial expansion and hence extract an accurate and practical Cardiff model. Cardiff model's users usually select a mixing order of between 3 and 7 for fundamental only load-pull data based



(a) (b)

Figure 7.3: (a) Load-pull measurement grid of the device 'A' with 91 load points. (b) Device 'B' load-pull grid with 57 points. The grids were selected in a way to capture optimum load points. The 0.5 dB contours are also plotted from maximum output power of (a) 34.6 dBm, and (b) 39.8 dBm at $T_{chuck} = 25\,^{\circ}\mathrm{C}$.

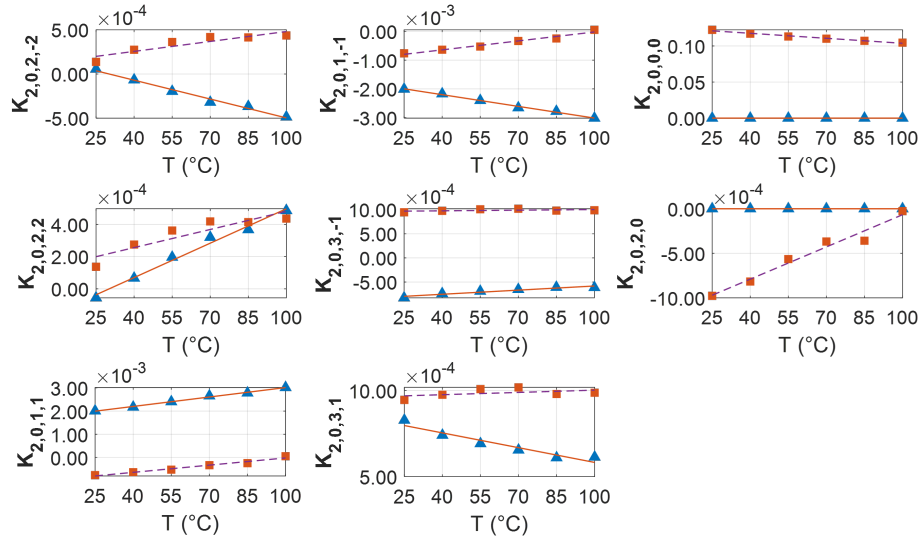
on accuracy requirements and past experience's [1].

Since the inclusion of temperature is a new feature, there was a need to decide the temperature fitting order ('l_{max}' in (7.3)) which has been achieved with the following steps:

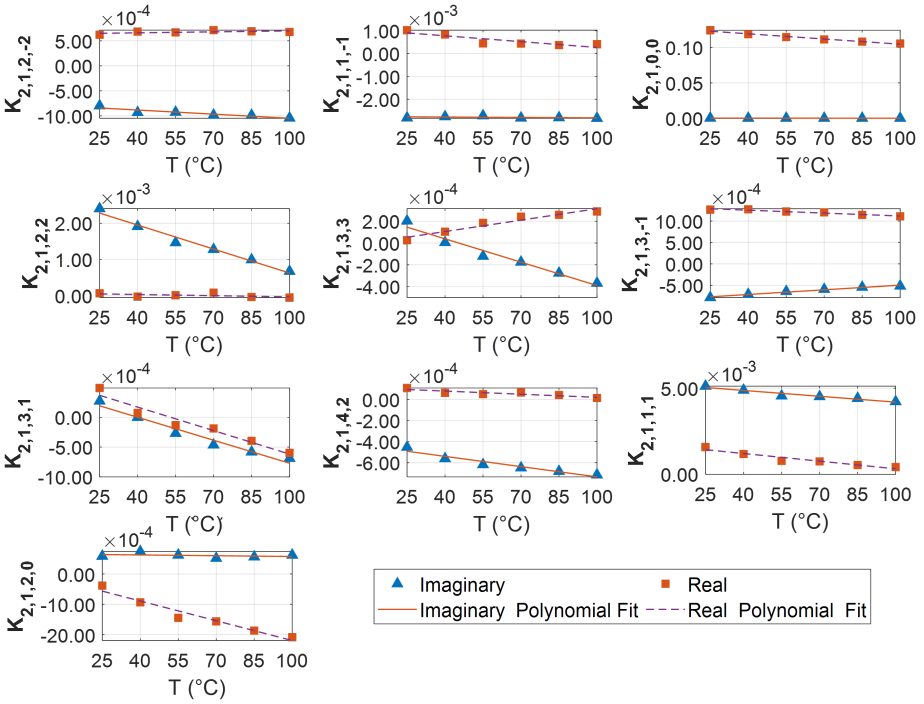
i) model coefficient '$K_{p,h,m,n}$' were extracted using a 5^{th} order conventional Cardiff formulation (7.1) at each T_{chuck}. Note, in this case it is valid to assume that T_{case}=T_{chuck}.

ii) real and imaginary part of each coefficients were separately plotted against T_{chuck} sweep, as shown in Figure 7.4 for coefficients relating to output response at (a) DC, and (b) f_0.

From Figure 7.4, we note that both real and imaginary parts of the coefficients, at both DC and f_0, show a behavior that can be approximated reasonably well with a linear polynomial function. This linear relationship between the conventional Cardiff model coefficients '$K_{p,h,m,n}$' and temperature 'T_{case}' can be mathematically represented as shown in (7.4)



(a) DC



(b) f_0

Figure 7.4: Real and imaginary part of the model's coefficients (a) $K_{2,0,m,n}$ and (b) $K_{2,1,m,n}$ vs T_{chuck} (symbols). First order polynomial fitting (lines).The model order at the fundamental frequency is 5, whereas a 4^{th} order model was used at DC (the model order at even harmonics and DC must be an even number).

where ($l_{max} = 1$).

$$K_{p,h,m,n}(T) = \sum_{l=0}^{1} Q_{p,h,m,n,l} \cdot (T_{case})^l \tag{7.4}$$

7.2.2. Verification of the new formulation.

The normalised mean squared error (NMSE) between the predicted $B_{p,h}$ wave and measured $B_{p,h}$ wave at each load is the figure of merit which is used to validate the new formulations of the Cardiff model. The definition of NMSE is illustrated in (8.2) [2].

$$NMSE = \frac{\sum_i |B_{p,h}^{Measured} - B_{p,h}^{Modeled}|^2}{\sum_i |B_{p,h}^{Measured}|^2} \tag{7.5}$$

7.2.2.1 Interpolation capability

To verify the interpolation capability of the new Cardiff model formulation (7.3) with respect to temperature, load-pull measurement data at $T_{chuck} = 25\,^{\circ}\text{C}$ and $T_{chuck} = 100\,^{\circ}\text{C}$ only were used to generate a temperature-dependent Cardiff model. Figure 7.5 shows the calculated NMSE (dB) value of $B_{2,1}$ data for (a) device 'A', (b) the device 'B'.

As shown in Figure 7.5, the NMSE value is less than -41 dB across all the data sets. In terms of percentage, it means only 0.9% deviation between the measured and interpolated data. Since load pull measurement data is typically presented in terms of output power and efficiency contours, Figure 7.6 shows a comparison of measured and interpolated contours at T_{chuck}=55 °C, where a very good match between the measured and interpolated contours can be witnessed.

7.2.2.2 Investigating extrapolation accuracy

Due to the linear relationship between the Cardiff model's coefficients '$K_{p,h,m,n}$' and temperature (as shown in Figure 7.4), there is a potential that the load-pull data could be accurately

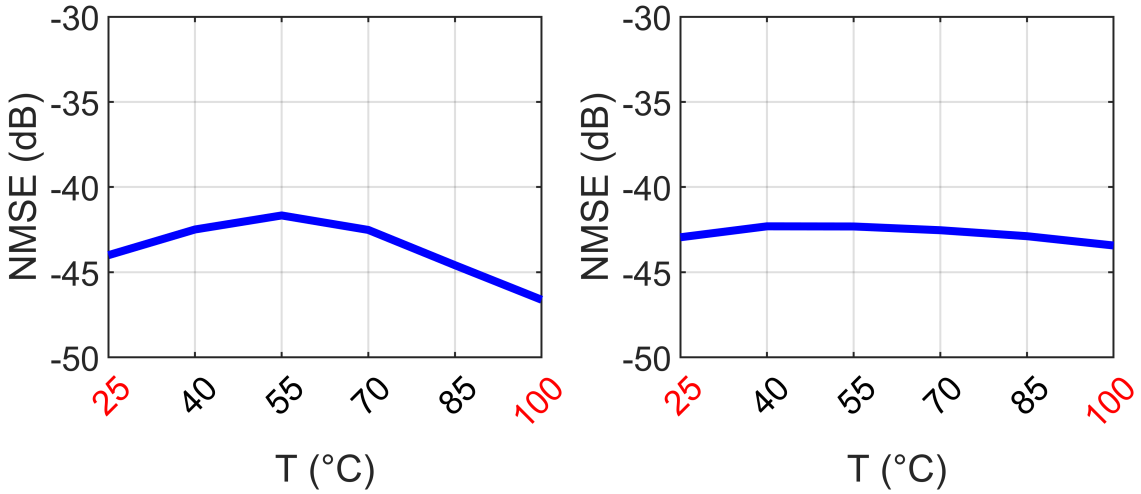


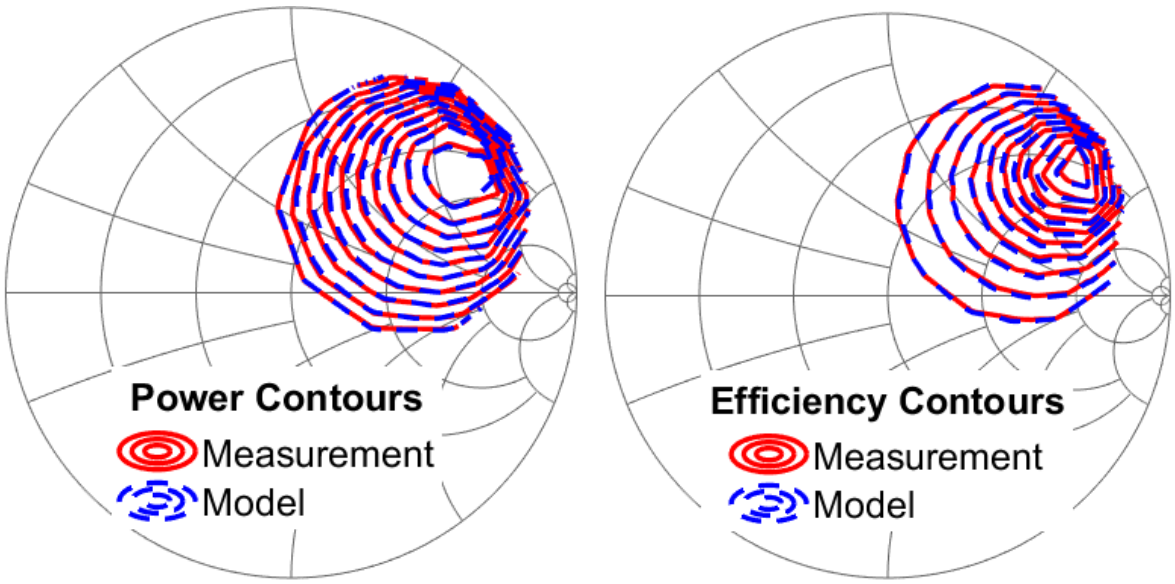
Figure 7.5: Comparing measured and modelled $B_{2,1}$ (a) device 'A', (b) device 'B'. Only measurement data at T_{chuck}=25 °C and 100 °C (highlighted in 'red') were used to generate the model, and $B_{2,1}$ at all the other temperature levels are interpolated.

extrapolated for higher temperature levels.

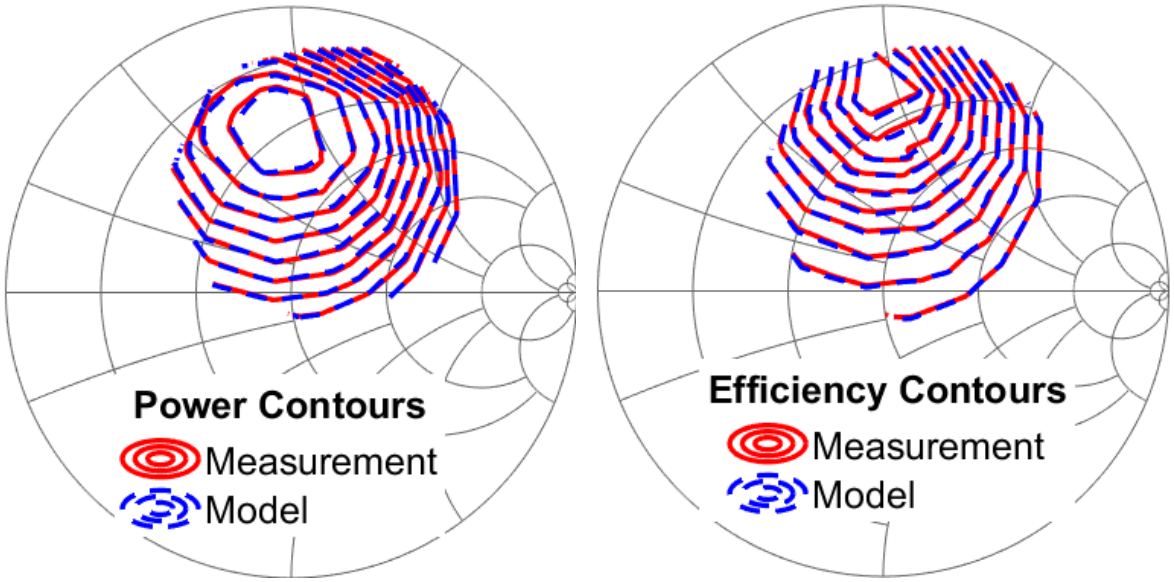
To test the extrapolation capability of the new model, load-pull data at only T_{chuck}=25 °C and 55 °C were used to generate a model, and data at T_{chuck}=70 °C, 85 °C and 100 °C were extrapolated. As anticipated, the model was capable of accurately extrapolating the load-pull data, as shown in Figure 7.7 for (a) device 'A', and (b) device 'B'.

The lowest accuracy is about -35 dB at T_{chuck}=100 °C for device 'A'. In terms of percentage, this is a 0.03 % deviation between extrapolated and measured data. Figure 7.8 compares the measured and extrapolated voltage and current waveforms of the device 'A' at T_{chuck}=100 °C (the point with the least accuracy in Figure 7.7).

As shown in Figure 7.8 there is a very good match between the measured and extrapolated voltage and current waveforms, meaning that also the prediction of harmonics' amplitude and phase is accurate..



(a)



(b)

Figure 7.6: Comparison of measured and interpolated load-pull contours (power and efficiency contours are plotted in 0.5 dB 5% step respectively) at T_{chuck}=55 °C, (a) device 'A', and (b) device 'B'. The maximum power and efficiency are: (a) 34.2 dBm and 58.8%, (b) 39.4 dBm and 62.2%.

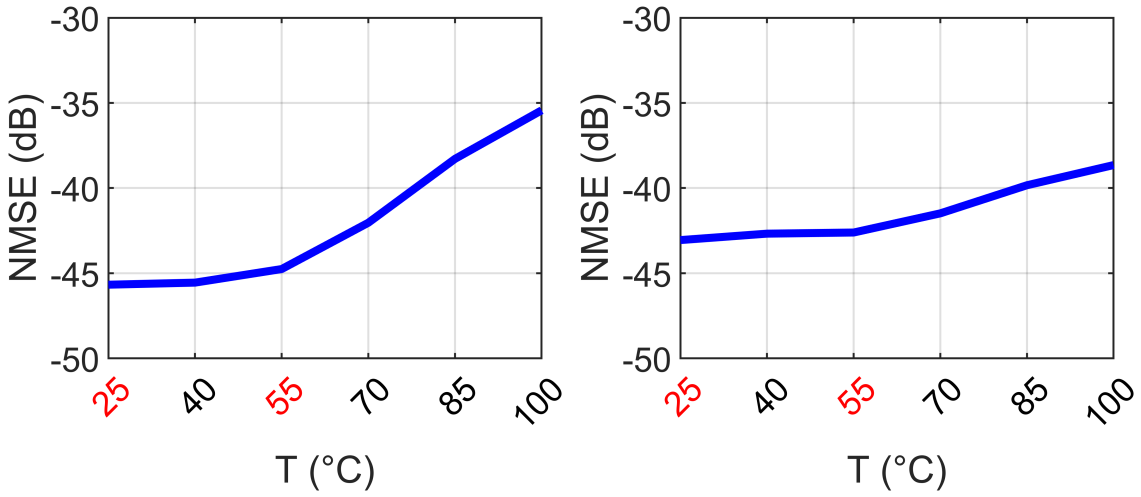


Figure 7.7: Calculated NMSE (dB) for $B_{2,1}$ at different temperature levels. Only measurement data at the temperature levels T_{chuck}=25 °C and 55 °C (highlighted in 'red') were used to generate the model, and $B_{2,1}$ at T_{chuck}=70 °C, 85 °C and 100 °C are extrapolated.

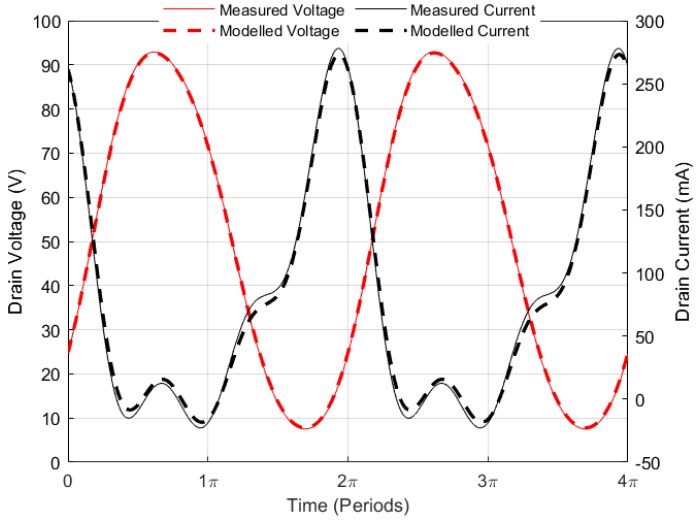


Figure 7.8: Voltage and current waveforms of device 'A' at T_{chuck}=100 °C. To generate the model, only load-pull data at T_{chuck}=25 °C and T_{chuck}=55 °C were used, and waveforms at 100 °C are extrapolated. The waveforms are at $\Gamma_L = |0.7|\angle 160$ which is the optimum load for maximum efficiency.

7.3. Verification by Power Amplifier Design

This section is dedicated to the design of a class AB power amplifier. This design is based on the new temperature-dependent Cardiff model extracted from load-pull measurement data of a 10 W GaN HEMT from Wolfspeed (device C) [3]. Fundamental load-pull data was collected at $f_0 = 3.5\,\text{GHz}$, and at various T_{chuck} ranging from 25 °C to 100 °C with 15 °C step. The device was biased in class AB condition with $V_{ds}^{DC} = 28\,\text{V}$, $V_{gs}^{DC} = -2.6$ V and $I_{ds}^{DC} = 50\,\text{mA}$ (at T_{chuck}=25 °C). The load-pull measurement was performed at 16 different input drive levels from P_{av}=18 dBm to P_{av}=33 dBm with 1 dB step. This package device was mounted on a test fixture with an aluminium base plate, in this case it cannot be assumed that $T_{case} = T_{chuck}$. Hence, the test-fixture was designed such that it allowed direct measurement of the device's case temperature T_{case} using a thermocouple sensor attached to the package's flange, as illustrated in Figure 7.9.

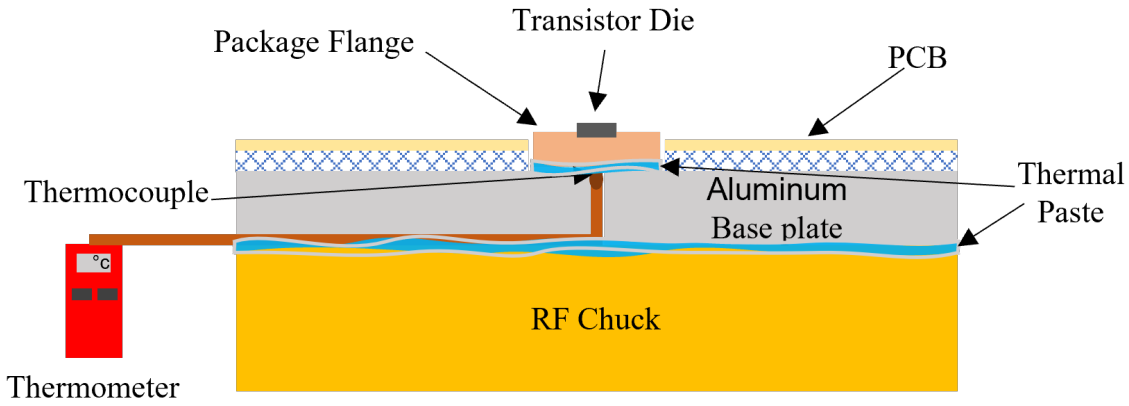


Figure 7.9: Test fixture used to measure the packaged device.

7.3.1. CAD implementation

As the device is mounted on the test fixture and is not in direct contact with the temperature-controlled RF chuck, there are two different reference temperatures to extract for the model from: I) chuck temperature T_{chuck}, and II) case temperature T_{case}. By calculating the thermal resistance of the aluminium base plate, and the thermal paste used at contact

points ($R_{th,test}$), the T_{case} can be related to T_{chuck} in a steady state condition [4]:

$$T_{case} = T_{chuck} + (R_{th,interface} \times P_{diss}), \tag{7.6}$$

where parameter P_{diss} is the average dissipated power, and $R_{th,interface} = R_{th,test}$.

In this case, the thermal resistivity of the test fixture was calculated as $R_{th,test}$=1.4 °C/W. Knowing the value of $R_{th,test}$, a temperature-dependent model was extracted directly from the load-pull data with respect to T_{case}. Figure 7.10 shows the NMSE (dB) values for $B_{1,1}$, $B_{2,0}$ and $B_{2,1}$.

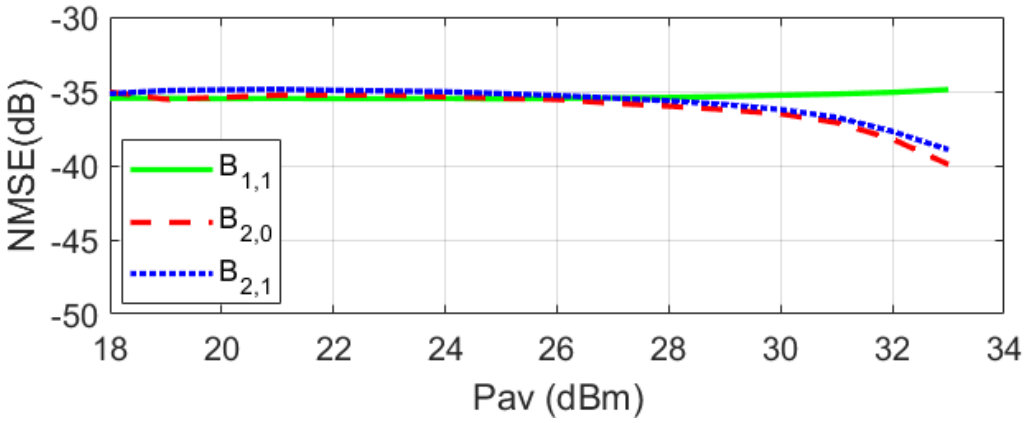


Figure 7.10: calculated NMSE (dB) value for$B_{1,1}$, $B_{2,1}$ and $B_{2,1}$. The NMSE plots compares measured and modeled data across all the dataset with model referenced to T_{case}.

As shown in Figure 7.10, the model is capable of accurately predicting the load-pull data with NMSE of better than -35 dB across all the datasets.

The schematic in Figure 7.11 illustrates the CAD implementation of temperature-dependent Cardiff model via a thermal feedback network. As shown in Figure 7.11 (a), T_{chuck} is defined as a voltage source followed by a resistor representing $R_{th,interface}$. The dissipated power is set to be the current flowing through the network. The value of the voltage node denoted by T_{case} is then fed back to the model for further computations.

Assuming that one has access to the case-to-junction thermal resistance ($R_{th,jc}$), the same

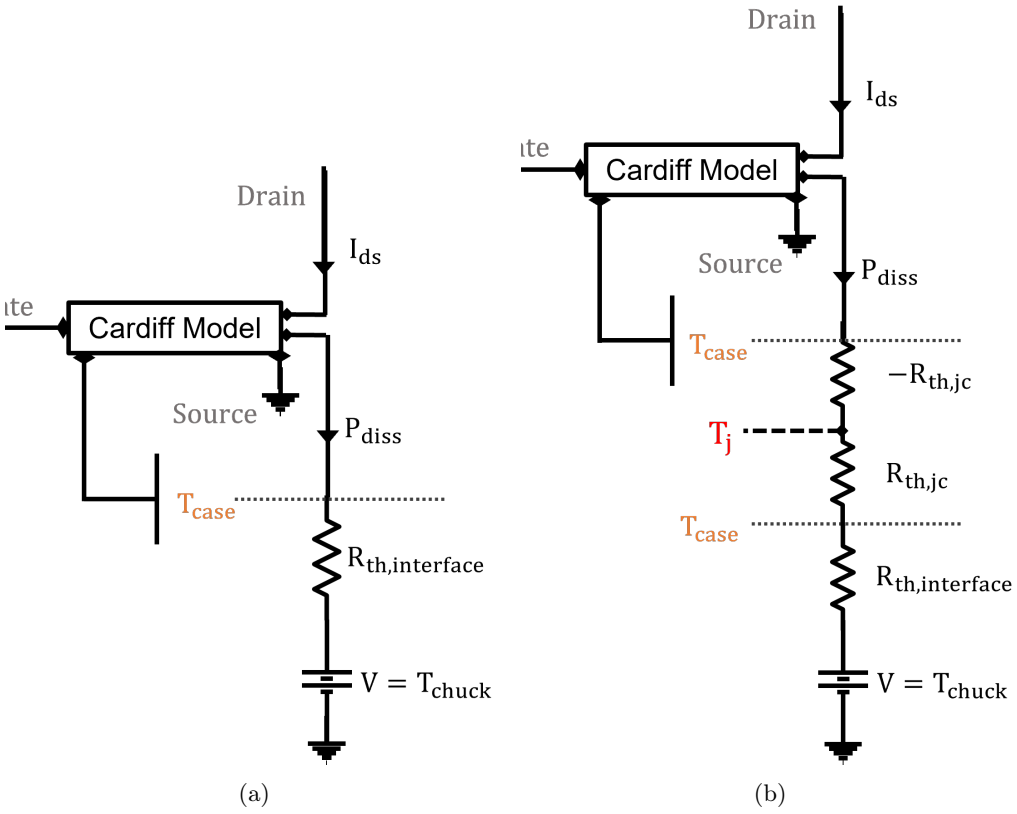


Figure 7.11: Temperature dependent model implementation in CAD simulator. Using thermal resistance, the reference temperature can be changed. In this example, by adding and then subtracting the thermal resistance of case-to-junction ($R_{th,jc}$) users can obtain information in relation to the junction temperature.

set of model coefficients can be used to also predict the associated junction temperature T_j within the CAD simulator. The capability of predicting the junction temperature T_j during the simulation can be achieved using the thermal model implementation in Figure 7.11 (b). This involves the addition of the junction-to-case thermal resistance $R_{th,jc}$ and a voltage node (T_j). The use of a negative value of $R_{th,jc}$ cancels its effect on the thermal feedback network, and the reference temperature remains unaffected. In this instance the '$R_{th,jc}$' of the transistor is given by the manufacturer as 7.83 °C/W [3]. Using this value, we were able to generate a simulation result in relation to the T_j. Figure 7.12 depicts a simulation example where both T_j and T_{case} are plotted versus output power when T_{chuck}=100 °C.

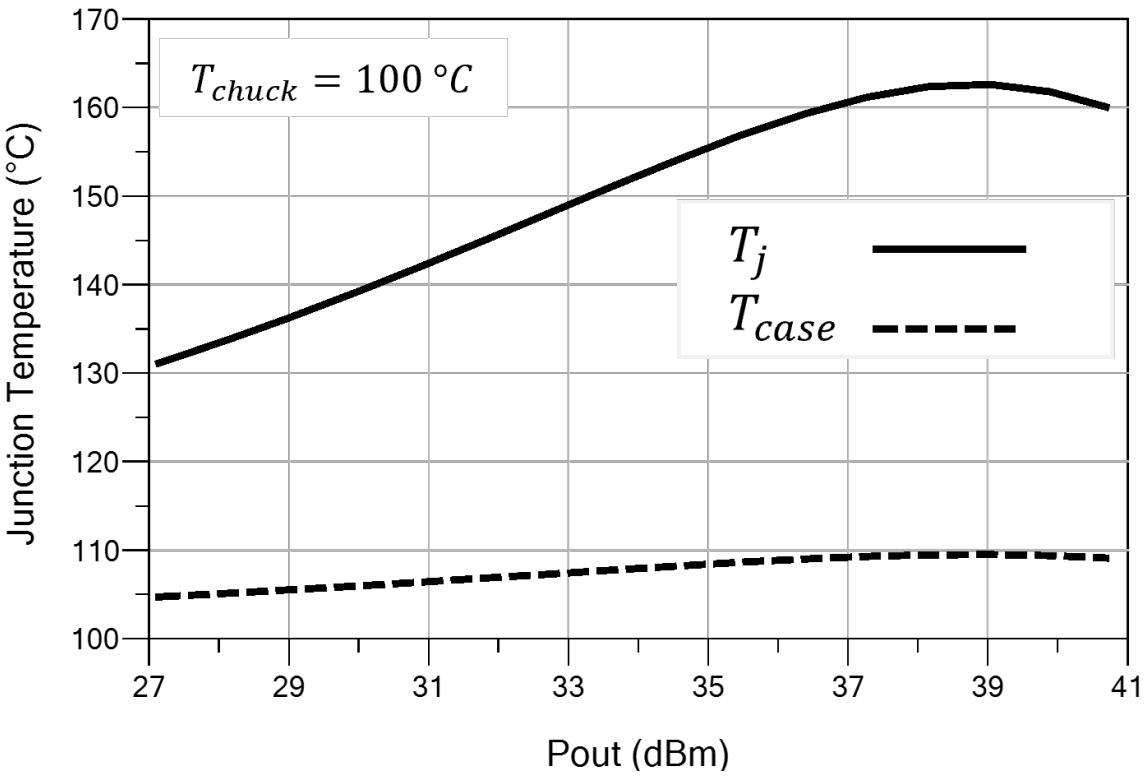


Figure 7.12: Simulation example: junction temperature (T_j) and case temperature (T_{case}) vs output power (P_{out}).

7.3.2. RFPA Design

Figure 7.13 shows the schematic of the RFPA which was designed in ADS using the new temperature-dependent Cardiff model. The objective of this design was to verify the capability of the new model in predicting the RFPA's performance under various temperature conditions.

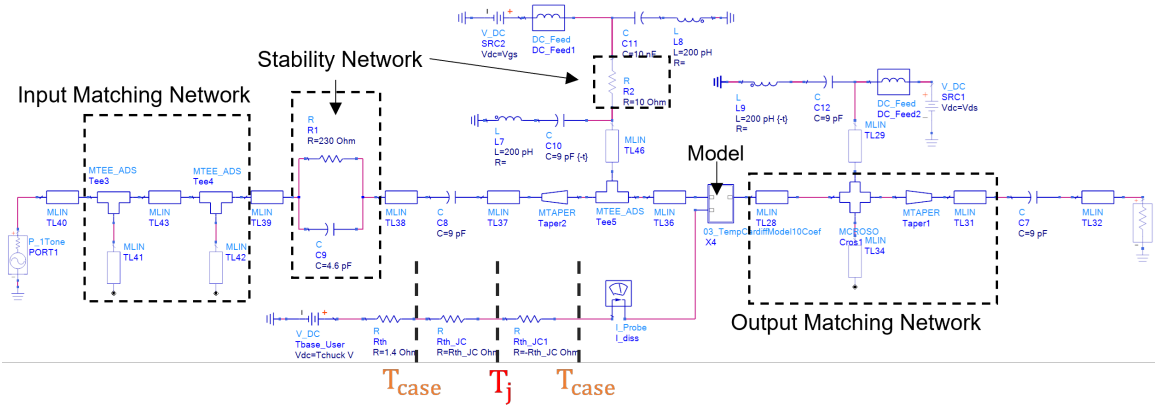


Figure 7.13: Circuit diagram of the RFPA in ADS. The output was matched to $\Gamma_L = |0.67|\angle 162$ using Microstrip transmission lines and an open-stub. For stability, a parallel R-C network (R=230 Ω and C=4.6 pF) was used at the input, and a 10 Ω resister in series with the gate DC bias network. To match the input, a 'π' network, consisting of two open-stub and a piece of transmission line, was used.

As shown in Figure 7.13, Microstrip transmission lines ("MLIN" in ADS) were used to design the matching networks. To design the output matching network, sections of MLIN and an open-stub were used. At the input, a "π" network, consisting of two open-stubs and a section of MLIN, was used to match the the input of the device to 50 Ω. Tapered lines ("MTAPER" in ADS) were used to provide an uninterrupted transition between the lines with different impedances, and avoid "stepped" impedance change. With regards to DC bias networks, at both input and output, sections of MLIN with electrical length of $\lambda/4$ at f_0=3.5 GHz were used which were short circuited via relatively large shunt capacitors (C=9 pF).

To design the Stability network, S-parameter measurement data from 0.1 GHz to 12 GHz

were used. As shown in Figure 7.13, a parallel 'R-C' network (R=230 Ω and C=4.6 pF) at the input combined with a 10 Ω resistor in series with the Gate DC bias were used to unconditionally stabilise the device across the frequency range (from 0.1 GHz to 12 GHz).

7.3.3. Verification: measurement vs simulation results of the power amplifier

The RFPA's circuit layout was fabricated on a gold-plated 0.5 mm Roger's RO4350 with dielectric constant of (ϵ_r=3.66) [5]. The circuit was mounted on a compatible aluminum base plate with same thermal resistivity of $R_{th,interface}$=1.4 °C/W.

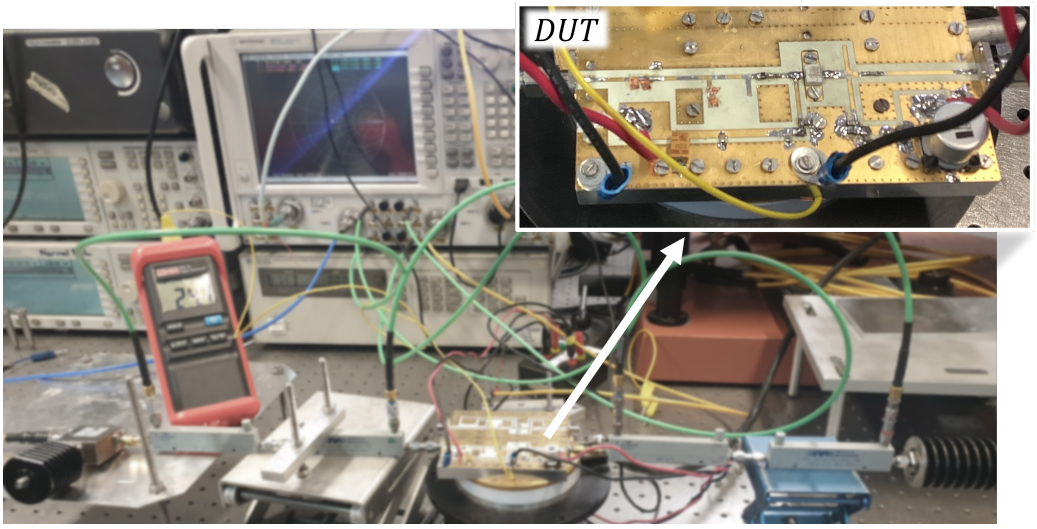
Figure 7.14 shows (a) photograph, and (b) block diagram of the measurement set-up which was used to measure the RFPA. The measurement set-up is very similar to the set-up shown in Figure 7.1 except for the 50 Ω termination of the load instead of the active injection. The photograph of the designed RFPA is also shown in Figure 7.14 (a).

Figure 7.15 shows the comparison between the measurement and simulation results. Gain (G_t (dB)) and efficiency (η (%)) performance of the RFPA at T_{chuck}=25 & 100 °C are plotted vs. the output power (P_{out} (dBm)).

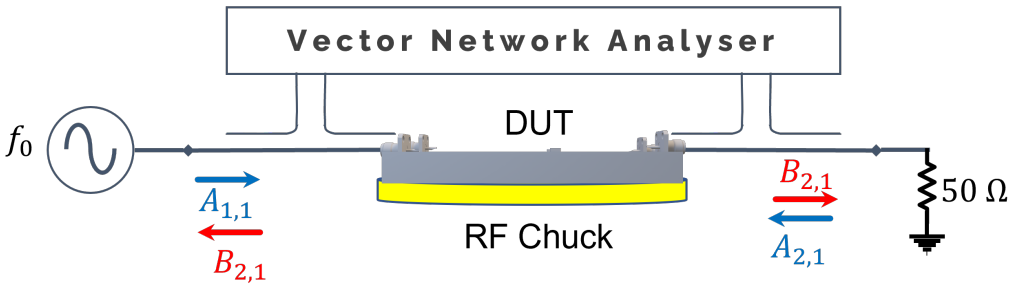
As evident by the data plotted in Figure 7.15, there is a very good match between the measured and simulated data at both T_{chuck}=25 & 100 °C. This means the new model can accurately predict the temperature-dependent behavior of the device. Slight difference between the modeled and measured efficiency appears only at maximum power level. This deviation can be ascribed to a different 2nd harmonic termination between the original dataset (which the model was based on) and the designed RFPA.

7.4. Summary

In this chapter, a new mathematical formulation for the Cardiff behavioural model was developed that is capable of predicting the temperature dependency of large-signal device performance. The new model has been extracted and verified using temperature dependent



(a)



(b)

Figure 7.14: Power amplifier's measurement. Photograph and block diagram of the system. The device is terminated to 50 Ω.

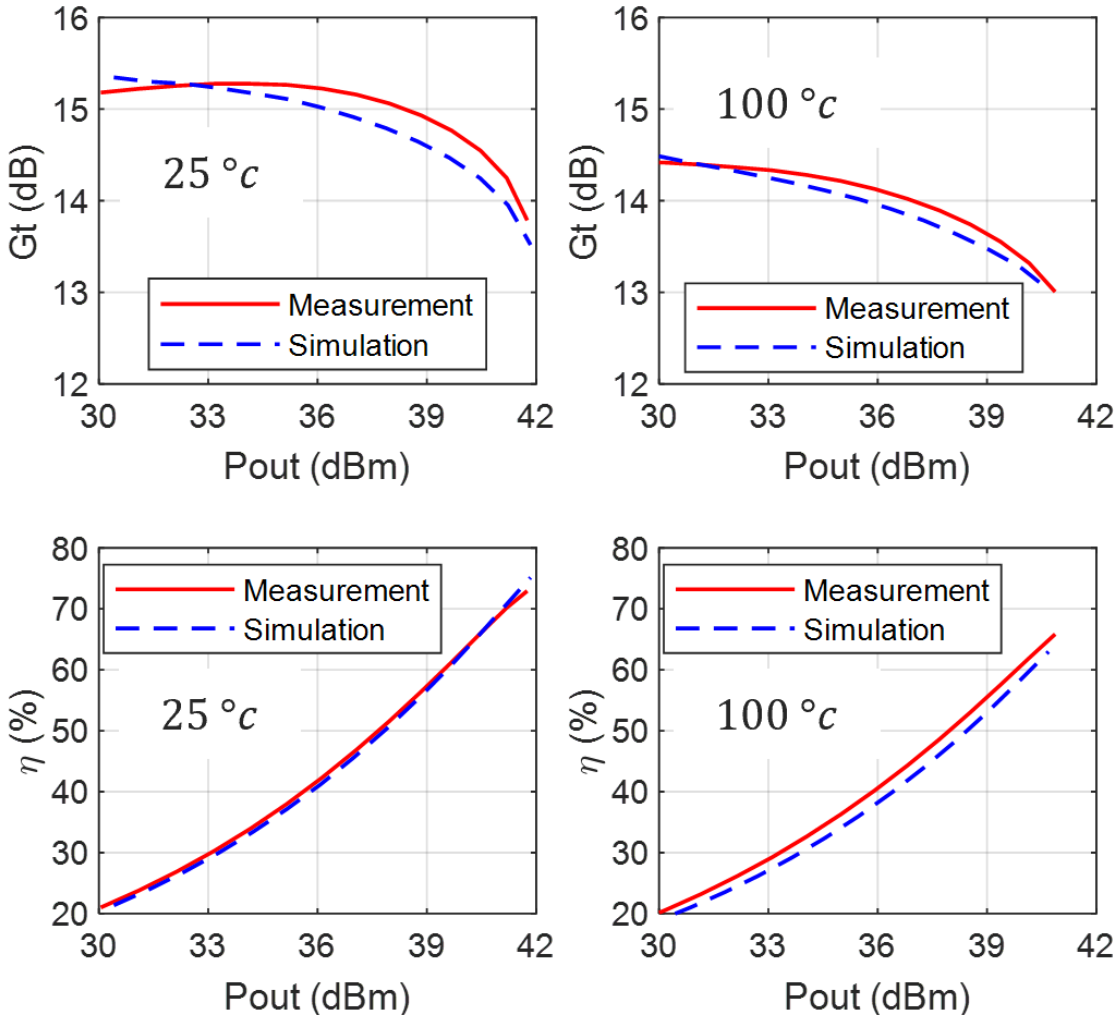


Figure 7.15: Comparison of measured and simulated gain (top) and efficiency (Bottom) vs. output power at T_{chuck}=25 & 100 °C of the RFPA at 3.5 GHz.

load-pull data on two GaN-on-SiC devices. To demonstrate that the model can provide RFPA designers with a tool to simulate their amplifier behaviour under realistic thermal environments, an RFPA was designed, fabricated and the predicted-performance experimentally verified.

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CHAPTER 8

Cardiff Model Utilisation for Predicting the Response of Multiple-Input Power Amplifiers

The application of the Cardiff behavioural model has been limited to the device-level. The model coefficients are often extracted from load-pull measurement data and used within a CAD simulator for the design of power amplifiers [1]. In other applications, the model is also used in algorithms for the development of high-speed active load-pull measurement systems [2, 3].

However, the Cardiff model's flexible mathematical formulation can be adopted for unconventional applications beyond the device level. For instance, it can be used to predict the response of a multi-input-single-output (MISO) power amplifier at the system level. Its general formulation can also be used to predict the response of any multi-port nonlinear system where at least two stimulus signals with varying phase and magnitude are interacting.

In this chapter, the Cardiff behavioural model will be used to predict the response of a dual-input inverted-LMBA. The focus of this chapter is on demonstrating a new application for the model, rather than development of the model formulation as it was in other model-related chapters. The mathematical formulation for the model will be presented, and the characterisation data will be analysed with different size to understand what is the minimum set needed to accurately model the PA response.

8.1. Cardiff Model Formulation

For the case of the MISO PAs, where the goal is to model the device's single output response ($B_{3,1}$ and $B_{3,0}$) to the varying two input stimulus signals ($A_{1,1}$ and $A_{2,1}$), the Cardiff model mathematical formulation in (8.1) can be used.

$$B_{3,h} = (\angle A_{1,1})^h \cdot \sum_x \sum_m \sum_n K_{p,h,m,n,x} \cdot |A_{1,1}|^x \cdot |A_{2,1}|^m \cdot (\angle \frac{A_{2,1}}{A_{1,1}})^n \tag{8.1}$$

Where the phase exponent parameter, 'n', can range from $-\infty$ to $+\infty$ and the corresponding magnitude exponents,'m' and 'x', can range from 0 to $+\infty$. Note, in this instance, as the output of the PA is matched to 50 Ω, the effect of the reflected signal at the output is ignored ($A_{3,1} = 0$).

As shown in (8.1), the model is normalised to the phase of the fundamental frequency at port 1 ($\angle A_{1,1}$). This phase normalisation establishes a time shift to ensure that each harmonic aligns when the phase of the fundamental is 0 °. Therefore, the model coefficients are only dependent on $|A_{1,1}|$, and not the $\angle A_{1,1}$. This not only simplifies the model's mathematical formulation, it also enforces the time invariance of the model [4].

8.2. Data collection strategy

The data was collected from simulations of a 300 W inverted-LMBA at 2.1 GHz. The Auxiliary PA (biased in class C) consists of two 170 W GaN HEMTs [5] in balanced configuration. For the Main PA (biased in class AB), a 40 W GaN HEMT [6] is used.

Figure 8.1 shows the block diagram of the inverted-LMBA. As shown, separate input ports are used for the Auxiliary (port 1) and Main (port 2) PA. The input stimulus signals $A_{1,1}$ and $A_{2,1}$ are injected into the port 1 and 2, respectively. The device response at the output (port 3) is represented by $B_{3,1}$.

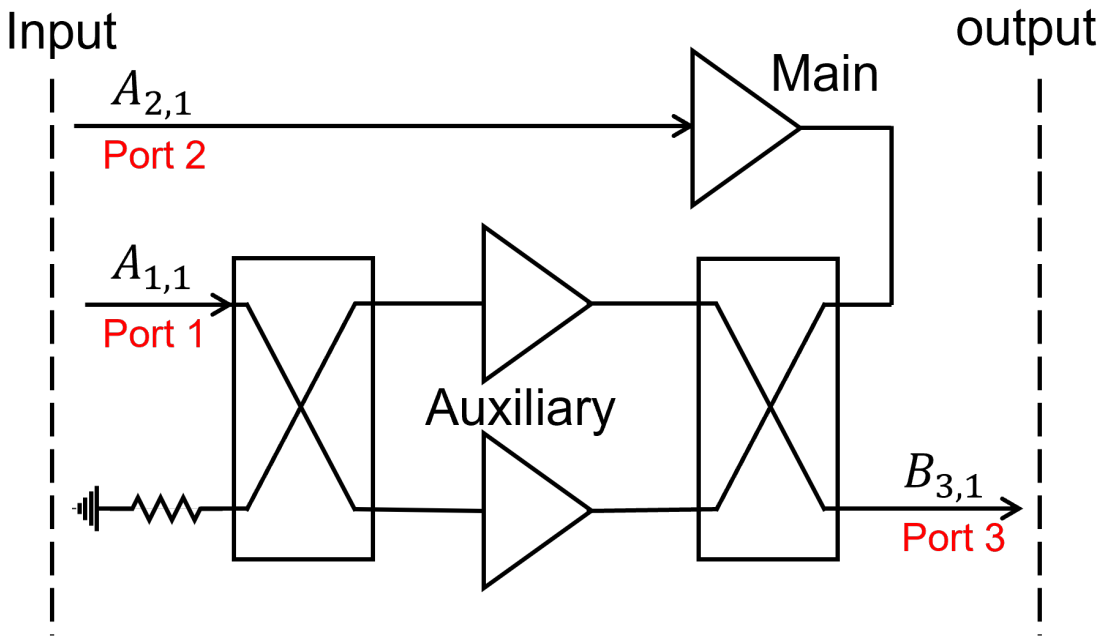


Figure 8.1: Block diagram of a MISO PA with two inputs and one output. The Cardiff model formulation can be used to predict the PA's output response $B_{3,1}$ respective to the two input stimulus signals, $A_{1,1}$ and $A_{2,1}$.

As only the relative phase between the two input trajectory ($\angle A_{2,1}/A_{1,1}$) is required, the "measurement" data, the $\angle A_{1,1}$was fixed at 0 ° and only data at different $|A_{1,1}|$ was collected. With regard to the trajectory at port 2, both magnitude and phase of the $A_{2,1}$ were swept. Initially, a smaller set of data points with total of '$N_1 = 26 \times 276 = 7562$' were used (where '26' and '276' are the number of $|A_{1,1}|$ and $A_{2,1}$ sweep points, respectively) . The model's interpolation capability was tested using a larger dataset with '$N_2 = 79 \times 2412 = 190548$' points. The simulation time between the two data sets increased almost proportionally to the increase in the number of points.

8.3. Model verification against "measurement" data

The normalized mean square error (NMSE) (8.2) is used to investigate the accuracy of the model and validate it across all the dataset. Figure 8.2 (a) shows the calculated NMSE (dB) value for both $B_{3,1}$ and $B_{3,0}$ (for DC current (h=0) the term '$B_{3,0} \triangleq I_{3,0}$') vs. input

drive level (P_{av}). Each data point on the graph represents the deviation of the model from measured dataset at specific P_{av} level. Figure 8.2 (b) and (c) show a comparison between the measured and modeled $B_{3,1}$ and $B_{3,0}$, respectively, while $|A_{1,1}| = max_i(A_{1,1,i})$.

As shown in Figure 8.2 the model is capable to accurately predicting the device response with an NMSE value of less than -30 dB, with NMSE defined as:

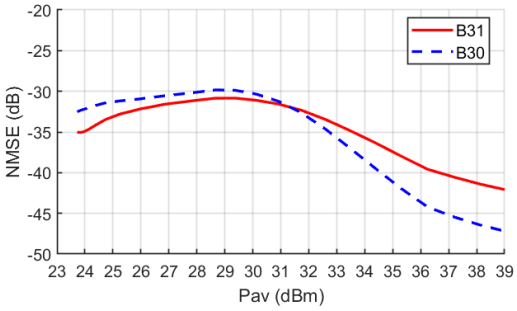
$$NMSE = \frac{\sum_i |B_{p,h}^{Measured} - B_{p,h}^{Modeled}|^2}{\sum_i |B_{p,h}^{Measured}|^2} \tag{8.2}$$

In terms of percentage, this is only a 3% deviation between the modelled and measured dataset.

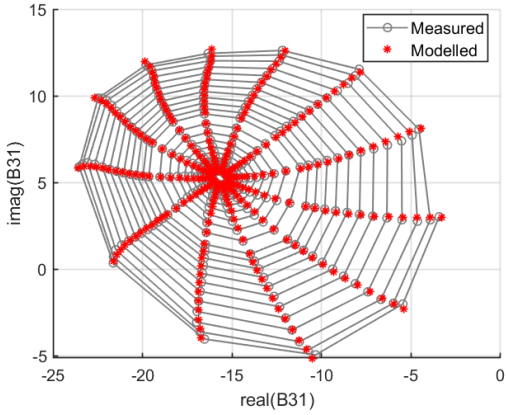
8.4. Interpolation verification

One of the main advantages of using a behavioural model is that there is a significant reduction in the size of the required dataset due to the interpolation between the measured points. In order to verify this capability of the model, the larger dataset with $N_2 = 190548$ points was tested using the model coefficients extracted only from $N_1 = 7562$. Figure 8.3 (a) shows the NMSE (dB) value for $B_{3,1}$ and $B_{3,0}$ over the range of P_{av}; Figure 8.3 (b) and (c) shows a comparison between the modelled $B_{3,1}$ and $B_{3,0}$ while $|A_{1,1}| = max_i(A_{1,1,i})$.

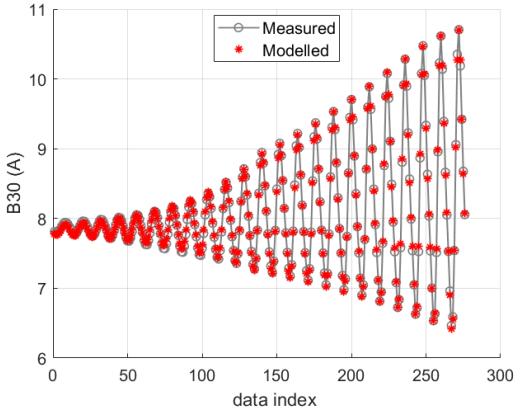
As shown in Figure 8.3, the model is capable of accurately interpolating the measured data with NMSE value of less than -30 dB. In this example, the total number of required data points to model the device behaviour was reduced from '190548' to '7562', which is more than a 96 % reduction in the required dataset's size.



(a)

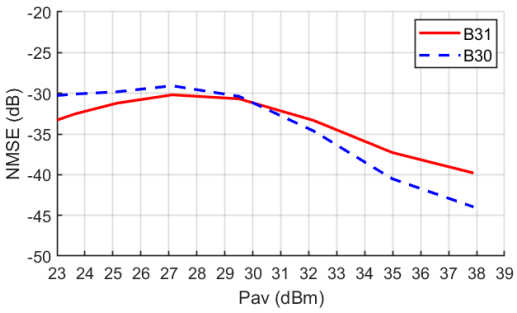


(b)

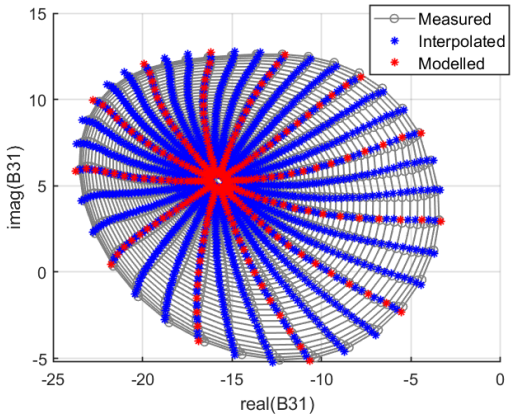


(c)

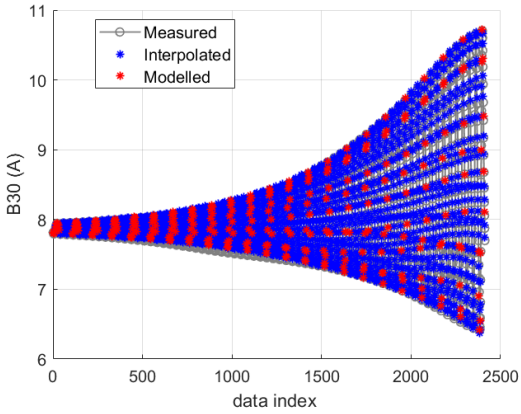
Figure 8.2: Comparison of modelled and measured data. (a) NMSE (dB) vs P_{av}, and (b) measured vs. modelled $B_{3,1}$; (c) measured vs. modelled $B_{3,0}$. The model was generated from the smaller dataset '$N_1 = 7562$'.



(a)



(b)



(c)

Figure 8.3: Comparison of measured and interpolated dataset. (a) NMSE (dB) vs. P_{av} (dBm), (b) comparing the interpolated and modelled $B_{3,1}$ at maximum input drive. The model was generated from the smaller dataset '$N_1 = 7562$' which is capable to predict a a larger dataset '$N_2 = 19548$'. This means a 96 % reduction in the size of the required dataset via interpolation capability of the model.

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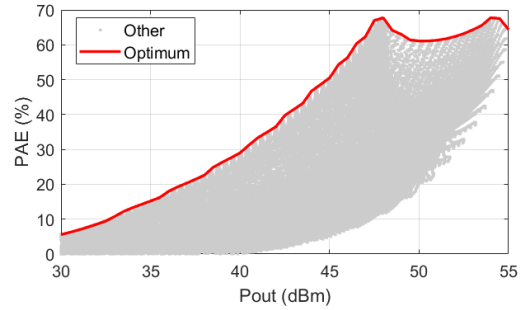
8.5. Optimum Input Trajectory

The model's prediction of the device output response respective to the input stimulus signals can be used to identify the optimum input trajectory leading to a desired performance (e.g., to achieve the maximum efficiency). Figure 8.4(a) shows the power added efficiency (PAE) vs. output power. The grey cloud of points shows all the possible combination of the inputs, while the solid line highlights the maximum PAE that can be achieved by properly selecting the inputs. Figure 8.4(b) shows the input settings that lead to the optimum PAE, specifically the relative phase ($\angle A_{2,1}/A_{1,1}$), and the available power at the two inputs. Finally, Figure 8.4 (c) the gain vs. output power with highlighted the gain resulting from selecting the input settings for optimum PAE.

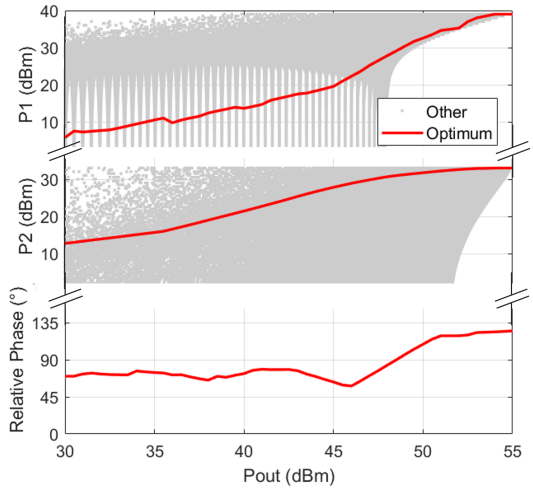
As shown in Figure 8.4 (a), if the 'Optimum' trajectory is selected, PAE of more than 50 % can be achieved at 10 dB output back-off (OBO), with peaks of around 67 % at both maximum power level and ≈7 dB OBO level. As expected, to achieve this optimal performance, a phase shift at the input is required in the OBO region (from around 60 ° to around 120 °), as shown in Figure 8.4 (b). This type of power-dependent phase offset was also reported for the dual input Doherty PA in [7], where a digitally controlled adaptive phase alignment at the input is proposed. As shown in Figure 8.4 (c) the optimal PAE is achieved by a compromise in the gain performance. Depending on the application and requirements a different set of combinations can be used, for example if maximum gain is required than different ($\angle A_{2,1}/A_{1,1}$) can be selected.

8.6. Summary

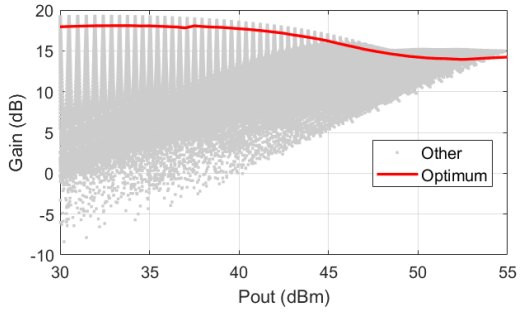
The Cardiff behavioural model can be used to accurately predict the output response of a MISO PA to the input stimulus signals. The model coefficients can be used to interpolate between the measurement data, hence, significantly reducing the required data when trying to identify the optimal driving conditions. In this work, the model has been verified, using



(a)



(b)



(c)

Figure 8.4: (a) PAE (%) vs. output power; (b) Relative phase between the two input drives ($\angle A_{2,1}/A_{1,1}$) vs. output power (P1 (dBm) and P2 (dBm) are available powers at port 1 and 2, respectively); (c) Gain vs. output power. The 'Optimum' refers to the data points with highest PAE (%) value at each output power level, where 'Other' refers to the rest of the dataset.

the simulation data of a 300 W inverted-LMBA with NMSE value of less than -30 dB. The model shows the dataset needed to accurately predict the original dataset can be reduced by 96 % while still maintaining good accuracy.

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CHAPTER 9

Conclusion

Doherty power amplifiers have become the standard architecture of choice in mobile base stations and are likely to remain popular in the near future. This is due to their simpler implementation compared to other efficiency enhancement techniques such as envelope tracking. Multi-bias Doherty power amplifiers are a promising architecture to achieve high efficiency over even larger power range and enable system-level power savings by adapting the power output to user traffic. Unlike the envelope tracking architecture, which requires very fast and dynamic adaptation of DC power supply, this method only requires stepped DC bias modulation by tracking the average power.

An accurate nonlinear transistor model is a critical component in designing advanced PA architectures. It enables designers to trust their simulation results and develop innovative data analysis and PA architectures. Without an accurate model, designers may hesitate to invest time and resources in developing new solutions based on simulation data, as they cannot be certain of the model's accuracy in the specific domain in which they are working. Accurate transistor modelling is essential for predicting the performance of a PA under varying operating conditions, such as temperature and bias. It also allows for the optimisation of the design and the prediction of the power amplifier performance before any physical prototypes are built. This can save significant time and resources in the development process.

Nonlinear behavioural models have traditionally been highly accurate, but only within a limited range of large-signal operating points (LSOPs). However, as the development

of behavioural models progressed, their generality improved, allowing them to cover larger LSOPs. This thesis focused on the development of the Cardiff behavioural model's mathematical formulation to include DC bias variation. This allowed for interpolation of load-pull data with regard to DC and significantly reduced the density of the required data. Additionally, the thesis revisited the model formulation to include input power sweep and proposed a revised formulation to improve the model's functionality and cover a larger power range. This served as a foundation for further improvement in the model, making it suitable for advanced multi-stage power amplifiers such as Doherty. The model implementation was also improved to provide a simulation experience that could switch between the small signal and large signal models depending on the magnitude of the input drive level.

The accuracy and functionality of the model were tested on the design of asymmetric Doherty PA based on 10 W and 25 W GaN HEMT devices from Ampleon. The model was able to accurately predict the response of the dual-input ("digital") DPA at different DC supply voltages at 3.6 GHz. A single-input version of the same design was also fabricated, and it demonstrated good back-off performance when tested at 30 V and 50 V supply voltage with a 100 MHz 5G test signal. An efficiency of more than 47% and an ACLR of less than -45 dBc were observed. This verified the model's ability to accurately predict the performance of the PA under varying operating conditions and its applicability in the Doherty design process. Confidence in the accuracy of the model in predicting the device response was a key enabler in the development of a load-pull data analysis method for identifying the correct load trajectory for the main amplifier to achieve optimal performance. This had a significant impact in the successful design of the power amplifier. The ability to accurately predict the performance of the device under different operating conditions allowed for the optimisation of auxiliary stage and the combining network to achieve performance that is as close as possible to the benchmark, identified during the analysis. This ultimately led to the successful design of the power amplifier.

Temperature is another parameter which was added into the Cardiff model mathematical

formulation. Load-pull measurement data of two GaN HEMT dies from Ampleon were used to capture the conventional Cardiff model coefficients response over a temperature range from 25 $°C$ to 100 $°C$. The model's ability to interpolate and extrapolate was then verified. The new temperature-dependent Cardiff model was then tested through the design and measurement of a class AB power amplifier using a 10 W Cree package device (CG2H40010F). In order to perform load-pull measurements on this package device, it was mounted on a test fixture , which its thermal conductivity was considered in the ADS implementation of the model via a thermal feedback network. This demonstrated the model's ability to accurately predict the performance of the device under varying temperature conditions. Furthermore, the new temperature-dependent model provides the first stepping stone into evolving the Cardiff model to include memory effects for simulations with modulated signal conditions, as self-heating is the main contributor to long-term memory effects in GaN transistors.

In an unconventional application, the Cardiff model formulation was used to model the output response of a Dual-input LMBA. A smaller dataset with varying input trajectories was used to extract the model coefficients, which was then tested on a much larger dataset. The device response at different input trajectories was then used to identify the optimal combination of input signals considering their magnitude and phase to achieve optimal PAE performance. This demonstrated the versatility and flexibility of the Cardiff model in predicting the response of multi-port nonlinear devices, such as the dual-input LMBA, and its ability to be used in system-level simulations.

Future Work

This work included various aspects related to behavioural models and power amplifiers, and expanded the existing body of knowledge in these areas. However, there are still opportunities for further exploration. There are multiple avenues through which the research presented in this thesis could be continued and expanded upon, which are detailed in the subsequent paragraphs.

The main drive in the development of Cardiff model formulation have been mainly to

improve its generality and interpolation capability. In the same context, several chapters of this thesis was dedicated to include the DC bias, temperature and input drive level. Now the generality of the model have improved, the future of the Cardiff model development relies on its extraction procedure. Tasker's recent work on spectral analysis of the tailored load-pull data [1] provides an alternative model extraction method which is more robust and better links with the device's physics. In Chapters 4 and 5 this analytical method was used to extract the model terms as a part of the study to include DC and input drive into the Cardiff model. However, currently, this method have been verified only on simulation data due to the limitation of active load-pull systems to collect the required data in the real world. The development of an active load-pull system which allows for the acquisition of the required tailored dataset, and full validation of new extraction method using measurement data has the potential to revolutionise the application of active load-pull systems and behavioural models.

Currently, the algorithms of active load-pull systems are designed to achieve a target load ($\Gamma_{L,h} = A_{2,h}/B_{2,h}$) through an iterative process that involves altering the magnitude and phase of $A_{2,h}$ and subsequently measuring and comparing the obtained '$A_{2,h}/B_{2,h}$' with the target load. This iterative process is performed repeatedly until the measured load is within a predefined tolerance of the target load. In this process the active load-pull system is "utilised" to replicate the behaviour of the passive load-pull system with added advantage of covering wider range of Γ_L values on the Smith Chart in comparison to the passive load-pull systems. Here, the question arises as to whether load-pull data in a specific load 'pattern' or 'region' is actually necessary. Work in [1] suggests that data collected from a well-defined and tailored "A-pull" pattern may be more advantageous than a load-pull pattern to extract robust model terms. Therefore, it may be highly beneficial to develop an A-pull active system that allows users to cover a specific area of the Smith Chart (e.g. around the optimum load) by setting a modulated $A_{2,h}$ pattern. This eliminates the need for an iterative process to reach a specific target load, as the A-pull system is only required to collect data for the set $A_{2,h}$ pattern, thus simplifying the process. Furthermore, this approach facilitates an

automated procedure for extracting the Cardiff model, as the spectral analysis of the data can reveal the appropriate model complexity and terms, hence eliminating the need for user intervention to adjust the model complexity.

While the proof-of-concept for the design of multi-bias Doherty PA's using the Cardiff model for average power tracking in base station applications has been presented in this thesis, a complete demonstration of this method for higher power (e.g. excessive of 200 W output power) and broadband PA's (e.g. LMBAs) remains an intriguing topic for future research. Specifically, load-pull measurements of higher power transistors can be challenging and costly, thus, combining the frequency and size scalable Cardiff model in [2] with the models developed in this thesis could be highly beneficial. In contrast to other variations of the Cardiff model that are used in the travelling-wave A, B-domain, the scalable Cardiff models are based on the admittance domain (voltage-and-current) and on the device current-source plane. Hence, the precise de-embedding of device parasitic and extrinsic equivalent circuit elements is essential for their accuracy.

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