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To cite this article: Zhao Yan and Qiang Li 2024 *J. Phys. D: Appl. Phys.* **57** 213001

OPEN ACCESS
IOP Publishing
Journal of Physics D: Applied Physics
J. Phys. D: Appl. Phys. **57** (2024) 213001 (21pp)
https://doi.org/10.1088/1361-6463/ad26cd

Topical Review

Recent progress in epitaxial growth of dislocation tolerant and dislocation free III–V lasers on silicon

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Received 25 July 2023, revised 15 November 2023
Accepted for publication 6 February 2024
Published 29 February 2024

Abstract

Epitaxial integration of III–V optical functionalities on silicon (Si) is the key to complement current Si photonics, facilitating the development of scalable, compact photonic integrated circuits. Here we aim to outline this field, focusing on the III–V semiconductor materials and the III–V lasers grown on Si. This paper is divided into two main parts: in the first part, we discuss III–V materials grown on Si, including the low-index {hhl} facets, (001) Si surface and anti-phase boundary, and dislocation engineering. The second part centres at III–V lasers grown on Si: we will first discuss III–V lasers that are highly tolerant to dislocations, including quantum dot/dash diode lasers, interband cascade, and quantum cascade lasers grown on Si from near infrared to long-wave infrared. We then move to the selective heteroepitaxy of low dislocation density III–Vs for the bufferless lasers. Finally, we review the III–V nanowire photonic crystal lasers grown on Si, which offers a different approach to overcome material mismatch and grow dislocation free III–V structures on silicon. We start with briefly introducing the recent progress of each technology, followed with a discussion of its key advantages, research challenge and opportunities.

Keywords: III-V lasers on Si, Si photonics, epitaxy

1. Introduction

The evolution of electronic integrated circuits (ICs) over the past six decades, and more recently silicon photonics, has been fundamentally shaped by silicon [1, 2]. This versatile semiconductor forms the bedrock for the relentless scaling and performance improvement in metal-oxide-semiconductor field-effect transistors, owing to the high manufacturability of silicon and its exceptional interface quality with gate dielectrics. In the realm of silicon photonics, the silicon-on-insulator (SOI) substrates of large diameter have primarily been used to fabricate various silicon-based optical circuits in the telecom band [3]. High-performance silicon-based electro-optic modulators have been developed and commercialized by exploiting the plasma dispersion effect [4]. The large index contrast with SiO_2 allows for compact passive optical devices. The development of low-loss SiN waveguides on Si substrates further expanded the spectrum of integrated photonics to submicrometer wavelengths [5]. The SOI and SiN/Si platforms thus collectively provide comprehensive spectral coverage, spanning from the visible, telecom, up

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to the mid-infrared regions [6]. Silicon photonic integrated circuits (PICs) have been advancing rapidly, leveraging the high throughput and scalable microelectronic manufacturing capability [7]. However, the indirect bandgap of Si and other group IV semiconductors restricts their application in light-emitting devices [8]. In contrast, III–V semiconductors with direct bandgaps have been widely utilized in the optoelectronic field. Harnessing quantum confinement effects and flexible band-structure engineering, many laser technologies, including strained quantum well lasers, quantum dot/dash lasers, interband cascade lasers (ICLs), and quantum cascade lasers (QCLs), have been developed. These lasers cover a broad spectrum, ranging from visible to near- and mid-infrared wavelengths. Integrating III–V materials on Si would synergize the efficient light emission properties of III–V semiconductors and the superior waveguiding properties of the Si platform, providing a solution for high-performance PICs and optoelectronic integrated circuits [7–9].

To date, integration of III–V materials on Si has evolved from hybrid integration with off-chip coupling, progressed to heterogeneous integration through wafer/die bonding or transfer printing, and now embraces monolithic integration by direct heteroepitaxy [10]. The use of high quality III–V materials has enabled the commercialization of products using the first two approaches. High performance devices have been demonstrated using bonded III–V wafers/dies on SOI substrate [7]. However, direct III–V epitaxy on Si provides several key advantages that are not accessible by heterogeneous integration. Direct III–V growth can bypass the need for bulky and costly III–V native wafers required for bonding. A monolithic III–V-on-Si platform can be used to implement various functionalities, such as optical communications, sensing, photodetector focal plane arrays, etc. enabling compact and densely integrated PICs with high scalability and reduced cost. Epitaxy of III–V lasers onto Si-photonic chips has recently gained intense momentum from both academia and industry, with significant progress made. In this paper, we begin by presenting an overview of III–V materials grown on Si, and subsequently focus on III–V lasers grown on Si. Specifically, section 2 outlines the defect engineering techniques in III–V/Si heteroepitaxy. Sections 3–5 centers at the III–V lasers grown on Si: section 3 focuses on the III–V lasers with dislocation insensitive gain medium, including quantum dot/dash, interband cascade and QCLs extending the spectrum range from telecom to mid- and long-wave infrared. Section 4 discusses the selective heteroepitaxy of low dislocation density and dislocation-free III–V materials, and the bufferless lasers grown on Si. Section 5 reviews the III–V nanowire photonic crystal lasers grown on Si. We begin with introducing the basic concepts and unique advantages of each technology, and then discuss the research challenges and potential solutions.

2. III–V semiconductor materials grown on Si

The study of III–V materials grown on Si primarily addresses the challenges associated with crystalline defects arising from material mismatches. The polarity mismatch results in the anti-phase boundary (APB), while lattice and thermal mismatches lead to the formation of misfit and threading dislocations (TDs). It is important to prevent or annihilate APBs, while simultaneously reduce the density of TDs. This section begins with an overview of the low-index {hhl} facets within the cubic lattice, specifically focusing on the zincblende III–V crystal. The manifestation of various low-index {hhl} facets is commonly observed in III–V heteroepitaxy and selective area epitaxy, and the control of the faceting propagation has implications in processes such as the APB annihilation. Following this, we will elaborate on the atomic structure of the (001) Si surface, and delve into the different strategies aimed at preventing APB formation or facilitating their annihilation. We will then move to a summary of the TDs in III–V growth on Si, along with a discussion of methods for dislocation filtering.

2.1. Low-index {hhl} facets in III–V zincblende crystals

The low-index facets, specifically those {hkl} facets with two or three identical Miller indices, are most commonly formed in III–V growth. This section starts with an overview of the {hhl} facets in zincblende/diamond crystals, where more than one of the three Miller indices are either identical or have opposite values. III–V crystals are entirely composed of atoms in sp^3 hybridization. Figure 1(a) provides a visual representation of the staggered configuration in the zincblende crystal [11, 12]. In this illustration, considering atom '0', the atoms '1', '2', and '3' represent the first, second, and third nearest atoms, respectively. When strong covalent bonds form, such as the Ga-As and In-As bonds, the third nearest atom is repelled from atom '0' (as depicted in figure 1(a)), thus establishing the staggered structure characteristic of the zincblende phase. On the other hand, if the material incorporates elements with high electronegativity (e.g. GaN crystal with high ionicity), the third nearest atom will be at the shortest distance to atom '0', creating an eclipsed configuration for the wurtzite phase. Figure 1(b) displays two unit cells of the zincblende lattice, with one of the staggered structures highlighted.

Given that both diamond and zincblende crystals are cubic lattices, we can present the <hhl> orientations as shown in figure 1(b). These orientations radiate from the origin, residing in the same plane (refer to the grey plane in figure 1(b)). Therefore, we can identify the corresponding {hhl} facets, which can be adjusted to intersect along the same line, as shown in figure 1(c). Examining the {hh0} facets within a cubic lattice, specifically the {110} facets, there exist 12 {110} facets. This is due to the flexibility of placing the number '0' at any of the three different Miller indices and assigning a negative sign to the two non-zero axes. If we exclude facets that are opposite to each other (for example, the (110) and (-1-10) facets), we are left with a total of 6 {110} facets. Similarly, for {hhl} facets where h and l $\neq 0$, there are 24 possible facets. Here, 'l' can be assigned to any of the three different axes, and the negative sign can be placed on any of the three different h, h, l axes. Disregarding once again the pairs of facets facing in opposite directions (for example, the (112) and (-1-1-2) facets depicted in figure 1(c)), we have a total of 12 {hhl} facets. Therefore, as illustrated in figures 1(c), a single

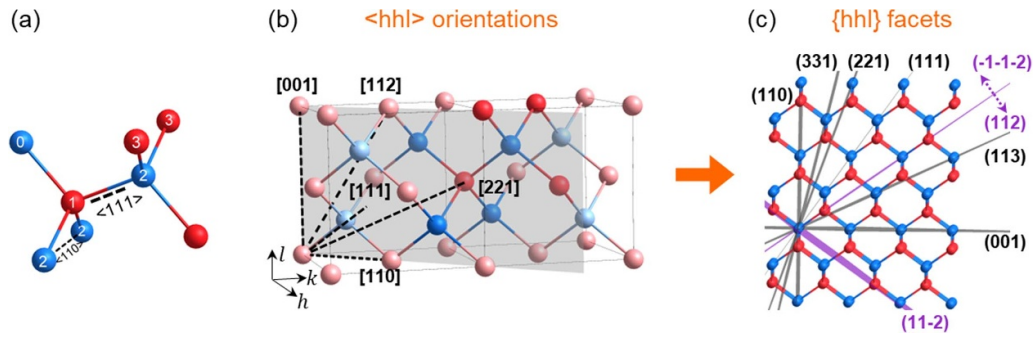

Figure 1. Low index {hhl} facets. (a) Staggered configuration of zincblende crystal. (b) Two unit cells of zincblende crystal with one staggered structure highlighted. The <hhl> orientations spread from the origin and locate in the grey plane. (c) The corresponding {hhl} facets. One (110) facet in relation to two {hhl} facets.

Table 1. The angle between the planar (001) facet and the low-index {hhl} facets.

Facet	(113)	(112)	(111)	(221)	(331)	(110)
Angle to (001) facet	25.2°	35.3°	54.7°	70.5°	76.7°	90.0°

{110} facet corresponds to two {hhl} facets that can intersect along the same line. This is exemplified by the alignment of the (110) and the (112), (11–2) facets in figure 1(c). Such alignments among these different low-index {hhl} facets are often observed in III–V epitaxy and will appear again in subsequent sections of this paper. The angle between two {hkl} facets can be calculated by

$$\cos\theta = \frac{(h_1k_1l_1)\cdot(h_2k_2l_2)}{\sqrt{h_1^2+k_1^2+l_1^2}\times\sqrt{h_2^2+k_2^2+l_2^2}}.$$

Table 1 lists the angle between the different {hhl} facets and the planar (001) facet.

2.2. (001) Si surface and APB engineering

Figure 2 illustrates the atomic structure on the surface of (001) Si substrates. Both diamond (Si) and zincblende (III–V) crystals can be viewed as two sets of face-centered cubic (FCC) lattice with a 1/4 [111] offset. In the diamond phase, the two FCC lattices consist of the same species, whereas for zincblende phase, the two FCC lattices are populated by group III and group V species, respectively. The surface of freshly polished (001) Si substrates typically exhibits atomic-scale steps. Figure 2(a) reveals a single atomic step on the (001) Si surface: across this monoatomic step, the topmost Si atoms are derived from the two respective FCC lattices. The surface dangling bonds of both the relaxed and the reconstructed (001) Si surface are illustrated. On a relaxed (001) Si surface, dangling bonds at differing terrace heights (for instance, those from the two FCC lattices) are along different orientations. In practice, these dangling bonds tend to form Si–Si dimer bonds to reduce surface energy. The orientation of the Si–Si dimer bond is dictated by the direction of the relaxed surface dangling bond. This results in two distinct types of monoatomic steps: for the S_B step, the upper terrace Si dimers align parallel to the step edge; for the S_A step, the upper terrace Si dimers align perpendicularly to the step edge [13].

Given that the topmost Si atoms across the monoatomic step originate from the two FCC sub-lattices, when a zincblende lattice is grown atop, different phases of the zincblende crystal form across this monoatomic step. This is assuming that the group V element is the initial layer deposited on the Si surface. The two different zincblende phases can be identified as the main-phase domain and the anti-phase domain, and as a result, group III–III or V–V bonds form the APBs at the boundary of the two phases (this will be further discussed in figure 3(d)). This scenario is also applicable to Si surfaces characterized by steps of an odd number of atomic layers in height. In contrast, for a double atomic step (refer to figure 2(b)), the topmost Si atoms on the upper and lower terrace originate from the same FCC lattice, regardless of whether it is a D_A or D_B type step. Consequently, the zincblende crystal deposited across the double atomic step would be of the same phase, thereby avoiding the formation of APBs. This scenario can also be applied to Si surface steps with an even number of atomic layers in height. APBs with homopolar III–III or V–V bonds represent electrically charged defects, and it is necessary to eliminate them before growing the active device region.

To date, several strategies have been developed to either prevent the formation of APBs (figures 3(a) and (b)) or annihilate them within the III–V buffers (figures 3(c) and (d)). One effective method to prevent APB formation involves growing III–V alloys on V-grooved Si enclosed with the {111} Si facets [14, 15]. It is therefore possible to use on-axis, CMOS-standard (001) Si substrates without any intentional offcut. The Si V-grooves can be fabricated by anisotropic wet etching of <110> direction stripe-patterned (001) Si substrates. A variety of APB-free III–V nano-ridge and thin films can be grown on the Si V-grooves [16–18]. The III–V thin films can be generated either by lateral coalescence of the nano-ridges or through one-step growth on V-grooved Si substrates [19, 20].

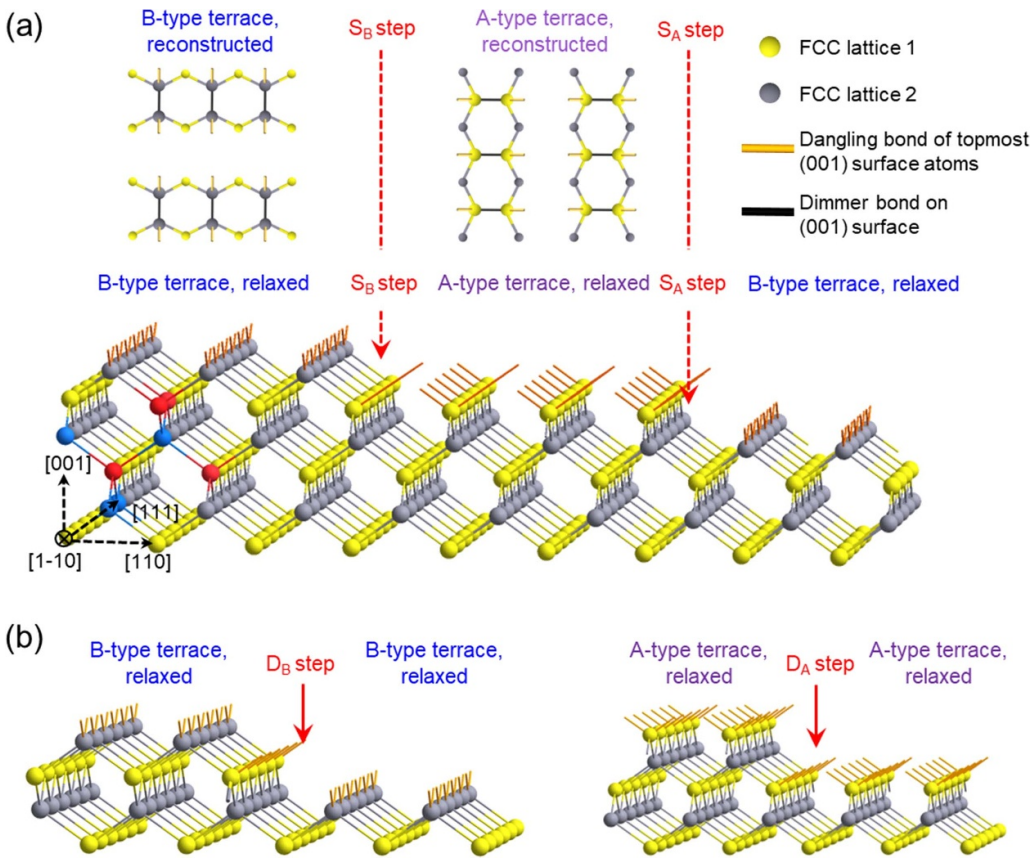

Figure 2. Atomic structure on (001) Si surface. (a) Schematic illustrating the reconstructed and relaxed (001) Si surface with monoatomic step. (b) Side-view of relaxed (001) Si surface with double atomic step.

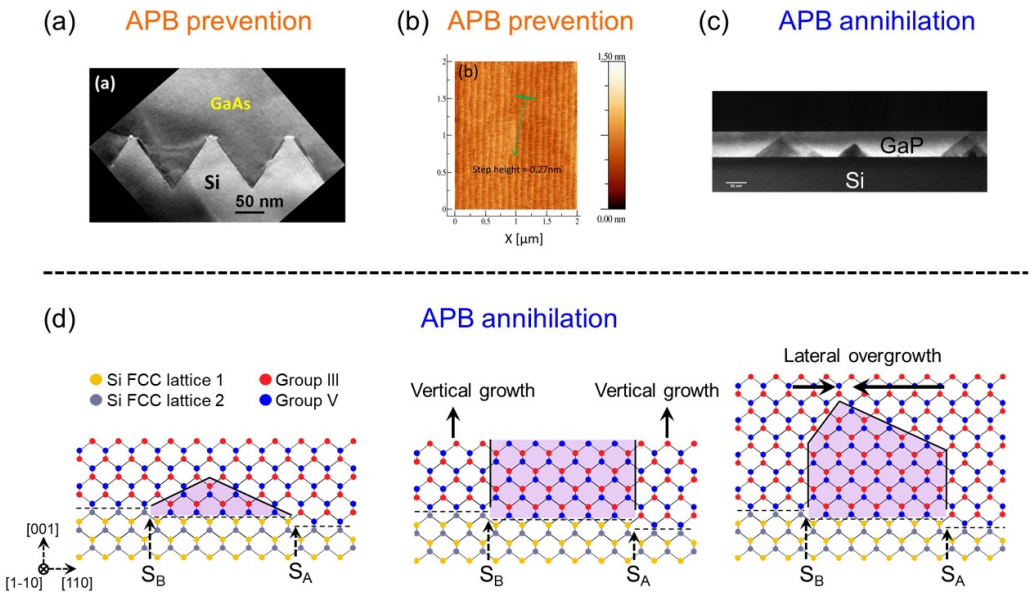

Figure 3. APB prevention (a), (b) and APB annihilation (c), (d). (a) APB-free GaAs grown on V-grooved Si. Reprinted from [15], with the permission of AIP Publishing. (b) AFM image of 0.15° (001) Si after treatment, exhibiting double atomic step. Reproduced from [22]. CC BY 4.0. (c) GaP grown on Si. Reprinted from [28], Copyright (2011), with permission from Elsevier. (d) APBs along different planes, at the same S_B- and S_A-type monoatomic Si step.

As discussed in figure 2, another tactic to prevent the APB formation involves forming double atomic steps on (001) Si surface. Early studies employed offcut Si substrates 4–6° tilted towards one of the two <110> directions. Under high-temperature conditions, monoatomic steps restructure into the energetically more favourable double atomic steps [21].

However, as the Si industry typically uses (001) Si wafers without a large offcut angle, new growth methods need to be developed on (001) Si substrates with an offcut angle <0.5°. This often entails meticulous surface pre-treatment on the (001) Si surface to form double atomic steps and reduce the APB density at the GaAs on Si interface (figure 3(b)) and/or specially designed growth methods to annihilate the APBs within the III–V buffers (figures 3(c) and (d)). APB-free GaAs grown on nominal (001) Si substrates with 0.15° offcut towards [110] direction was reported using plasma and high-temperature pre-treatment to form double atomic steps, a method that has produced 300 mm GaAs-on-Si templates [22, 23].

If APBs form at the III–V/Si interface, it is crucial to annihilate them within the III–V buffers. As depicted by the schematic of figure 3(d), vertical APBs along the {110} plane penetrate to the wafer surface, while inclined APBs along other {hhl} planes can be annihilated. Figure 3(d) provides a schematic illustrating the APBs along different {hhl} planes. In the three sketches of figure 3(d), despite the presence of the same S_B- and S_A- type monoatomic steps on Si surface, the APBs can be situated on varying crystal planes. The planes on which the APBs form could be more closely associated with the relative lateral growth rate of the main phase and the anti-phase, whereby inclined APBs can be buried within the III–V buffers. This has been demonstrated in recent studies through preconditioning of the Si surface or by manipulating the growth of nucleation layer, resulting in APB-free III–V templates grown on on-axis (001) Si [24–26]. Pseudo-morphic growth of GaP on Si has also been developed [27, 28], with 300 mm GaP/Si templates now commercially available by the $NASP_{III–V}$.

2.3. *Dislocation engineering of III–V templates grown on Si*

Dislocations are one-dimensional line defects characterized by their Burgers vector and the line vector along the dislocation line (e.g. the core of the dislocation). Two basic types of dislocations can be classified based on the angle between the Burgers vector and the line vector: edge dislocations, where the Burgers vector is perpendicular to the line vector (refer to figure 4(a)), represent an extra half plane existing in a perfect crystal; screw dislocations, where the Burgers vector is parallel to the line vector, signify shear lattice deformation along the line vector. In material systems with low to moderate misfit, such as (001) GaAs/Si or (001) InP/GaAs with ∼4% lattice mismatch, 60° dislocations, which have both edge and screw components, are the most common type. Figure 4(c) provides a schematic of a mobile (glissile) 60° dislocation, in which the Burgers vector forms a 60° angle with the <110> line direction [29]. This type of dislocation can glide readily with a threading segment along the {111} slip plane [30]. In high misfit material systems, such as (001) GaSb/GaAs with ∼8% lattice mismatch, an interfacial misfit array with a large portion of pure edge dislocations tend to form to relieve the strain, as demonstrated in figure 4(b) [31].

Various dislocation filtering methods have been developed in III–V/Si heteroepitaxy to minimize the threading dislocation density (TDD). Thermal cycle annealing (TCA),

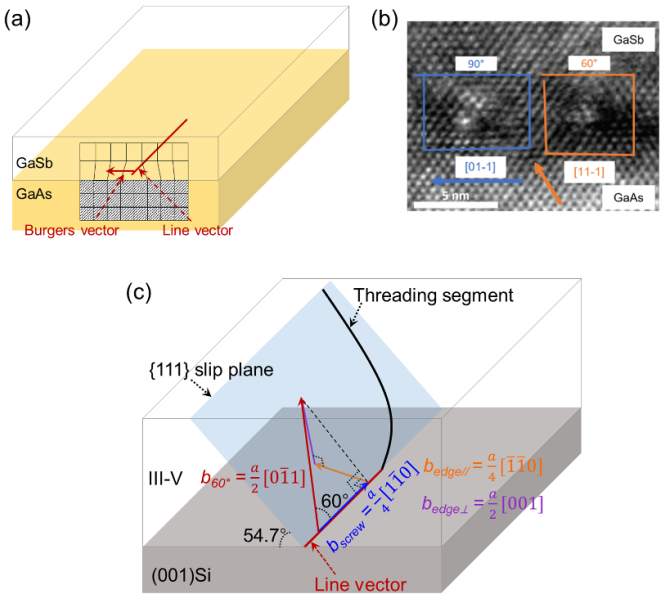

Figure 4. Edge dislocations and 60° dislocations. (a) Schematic illustrating the edge dislocations. (b) TEM at the GaSb/GaAs heterointerface. Reproduced from [31]. CC BY 4.0. (c) Schematic illustrating the geometry of a glissile (a/2)[011], 60° dislocation. The different dislocation components are indicated [29].

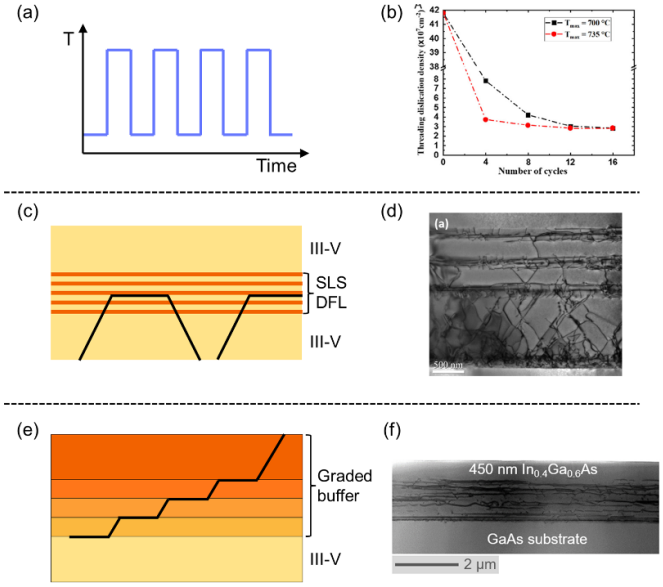

Figure 5. Dislocation filtering techniques. The growth approaches of (a) thermal cycle annealing (TCA), (c) strained-layer superlattice (SLS) as dislocation filters (DFL), and (e) Composition graded buffer. (b) Reduction of TD density as a function of TCA. Reproduced from [33]. CC BY 4.0. (d) TEM of TD reduction by SLS as DFL. Reproduced from [35]. CC BY 4.0. (f) TEM of InGaAs graded buffer. Reprinted from [38], with the permission of AIP Publishing.

for example, utilizes *in-situ* periodic temperature cycles (figure 5(a)). The oscillating temperature range encompasses the III–V growth temperature, thus inducing different strain signs and magnitudes in the III–V thin films due to the different thermal expansion coefficients between III–V and

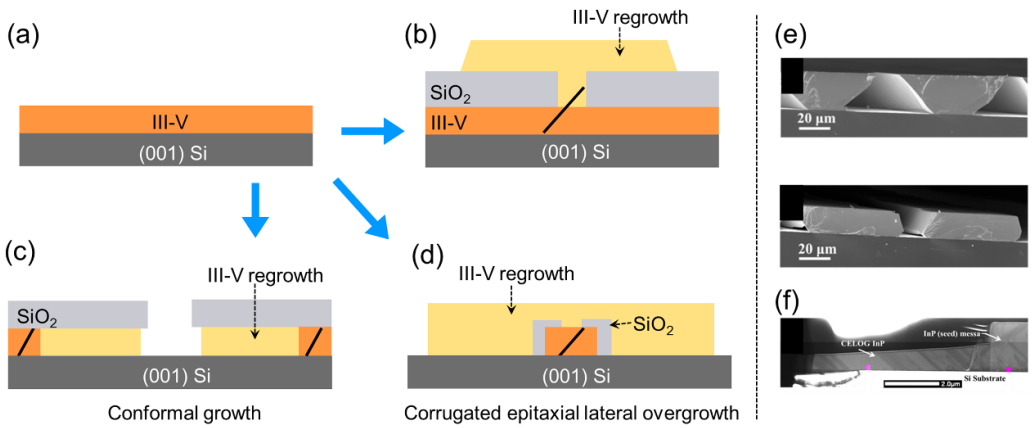

Figure 6. Schematic showing the (b) lateral overgrowth on III–V thin films [39, 40], (c) conformal growth [41], and (d) corrugated epitaxial lateral overgrowth (CELOG) [42]. (e) Tilted SEM and (f) cross-sectional TEM of InP grown on Si using CELOG. Reproduced from [42]. © IOP Publishing Ltd. All rights reserved.

Si. These periodic temperature fluctuations can instigate thermally driven dislocation motion, facilitating annihilation of TDs [32]. The effect of TCA is enhanced in thicker III–V thin films due to greater strain build-up. After the initial few cycles of thermal annealing, the TDD in GaAs/Si templates can be rapidly reduced from the order of 10^8 cm^{-2} to 10^7 cm^{-2} (figure 5(b)) [33]. Strained-layer superlattice (SLS) can act as a dislocation filter by intentionally applying strain fields to interact with dislocations, bending dislocations laterally towards the sample edge or enhancing their annihilation (figure 5(c)). The forces propelling the TDs are proportional to the strain applied (e.g. the lattice mismatch of SLS) and the layer thickness [34]. Applying four periods of SLS filters has been reported to reduce the TDD in GaAs/Si templates to the order of 10^6 cm^{-2} [35]. Both TCA and SLS filters can also be used for TD reduction in growing InP and GaSb buffers on Si. A compositionally graded buffer is another method used to bridge the lattice constants, as seen in the compositionally graded Ge_xSi_{1-x} or $In_xGa_{1-x}As$ buffers [36–38]. This approach promotes the formation of long misfit dislocations (figure 5(e)), instead of numerous short misfit dislocations associated with TDs.

In addition to the aforementioned dislocation engineering approaches in blanket heteroepitaxy, geometrically defined selective area growth can yield III–V materials with further reduced TDD, and even dislocation-free III–V layers. This includes techniques such as epitaxial lateral overgrowth (ELOG), depicted in figure 6, and the bufferless III–V growth on Si which will be discussed in section 4. In ELOG, beginning with a III–V template grown on Si (figure 6(a)), a SiO_2 pattern is defined on the III–V surface for subsequent III–V regrowth [39, 40]. This setup effectively blocks TDs located right underneath the SiO_2 growth mask. Besides, the SiO_2 trench with large aspect ratios can confine additional TDs (as indicated by the dark line in figure 6(b)), allowing for high-quality III–V layers on top of the SiO_2. In the conformal growth scheme, a patterned SiO_2 mask is designed to enable an undercut process of the III–V thin film and subsequent III–V lateral regrowth (figure 6(c)) [41]. Another technique, referred to as the corrugated epitaxial lateral overgrowth (CELOG), involves patterning the III–V thin film into segments and performing III–V regrowth from the openings of SiO_2-encapsulated III–V segments (figure 6(d)) [42]. In all these approaches, the crystalline defects can be blocked by the geometric confinement as evidenced by the TEM inspection (figure 6(f)). It is also possible to extend the III–V materials up to tens of micrometers (figure 6(e)).

3. Dislocation less-sensitive III–V lasers grown on Si

The epitaxial integration of lasers on Si can be generally categorized into two routes: In the first strategy, a gain medium that is less sensitive to dislocations is combined with a III–V buffer optimised using various techniques discussed previously. Examples include quantum dot/dash lasers, interband cascade lasers, and QCLs (refer to figure 7), which have demonstrated comparable thresholds and good lifetimes to their counterparts on native III–V substrates. With promising results first reported from lasers at telecom O-band and C-band, this has extended to the submicron and mid-wave and long-wave infrared wavelengths (refer to figure 8). The second strategy focuses on achieving near dislocation-free III–V materials grown on Si, by selective nano-heteroepitaxy of III–V on (001) Si, which will be discussed in section 4, and III–V nanowire growth on (111) Si, which will be covered in section 5.

3.1. Quantum dot and quantum dash diode lasers grown on Si

Conventional GaAs-based multi-quantum well (QW) lasers are notably sensitive to crystalline dislocations, which often leads to device early failure [44]. The key challenges of III–V lasers grown on Si has been to realize laser devices with superior performance and exceptional reliability. QDs are much less susceptible to TDs compared to conventional QWs due to reduced carrier lateral diffusion (refer to figures 7(a) and (b)). Research in the last decade has established QD laser growth

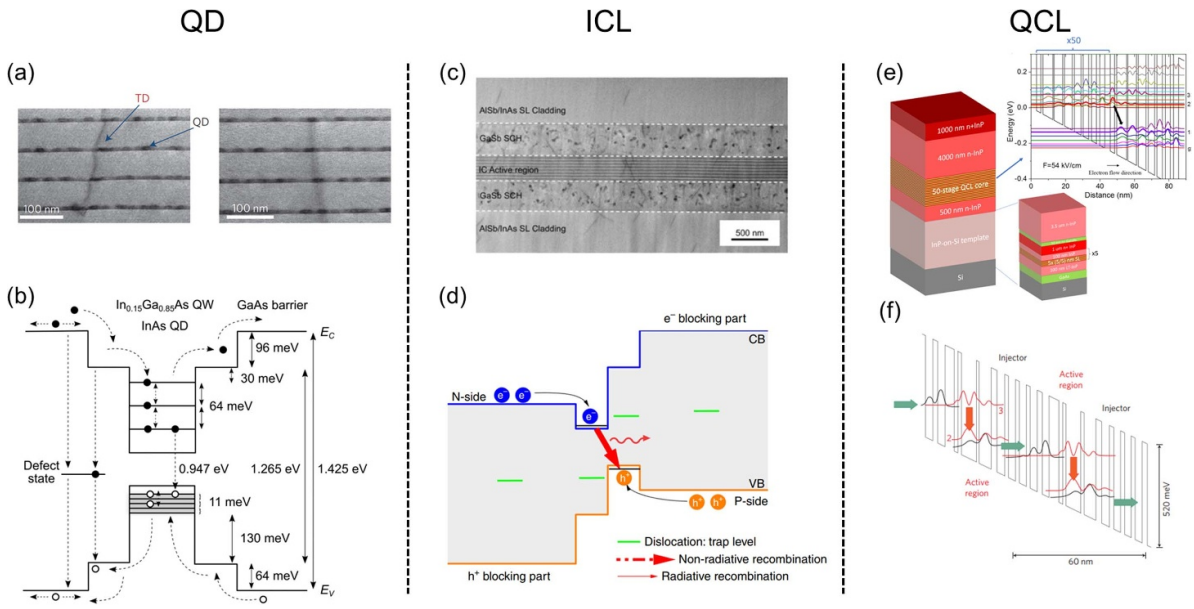

Figure 7. Dislocation less-sensitive III–V lasers grown on Si, including the quantum dot (QD), interband cascade lasers (ICL), and quantum cascade lasers (QCL). (a) TEM images showing the interactions between dislocations and QDs. Reproduced from [43], with permission from Springer Nature. (b) Band diagram of InAs/GaAs QD laser, showing the in-plane capture of carriers inside QDs. © [2020] IEEE. Reprinted, with permission, from [44]. (c), (d) Dislocation tolerant ICL grown on Si. Reprinted with permission from [45] © The optical Society. (e) Structure and band diagram for one cascade stage of the QCL lasers grown on Si. © [2023] IEEE. Reprinted, with permission, from [46]. (f) Simplified schematic of the conduction band structure for a QCL. Reproduced from [47], with permission from Springer Nature.

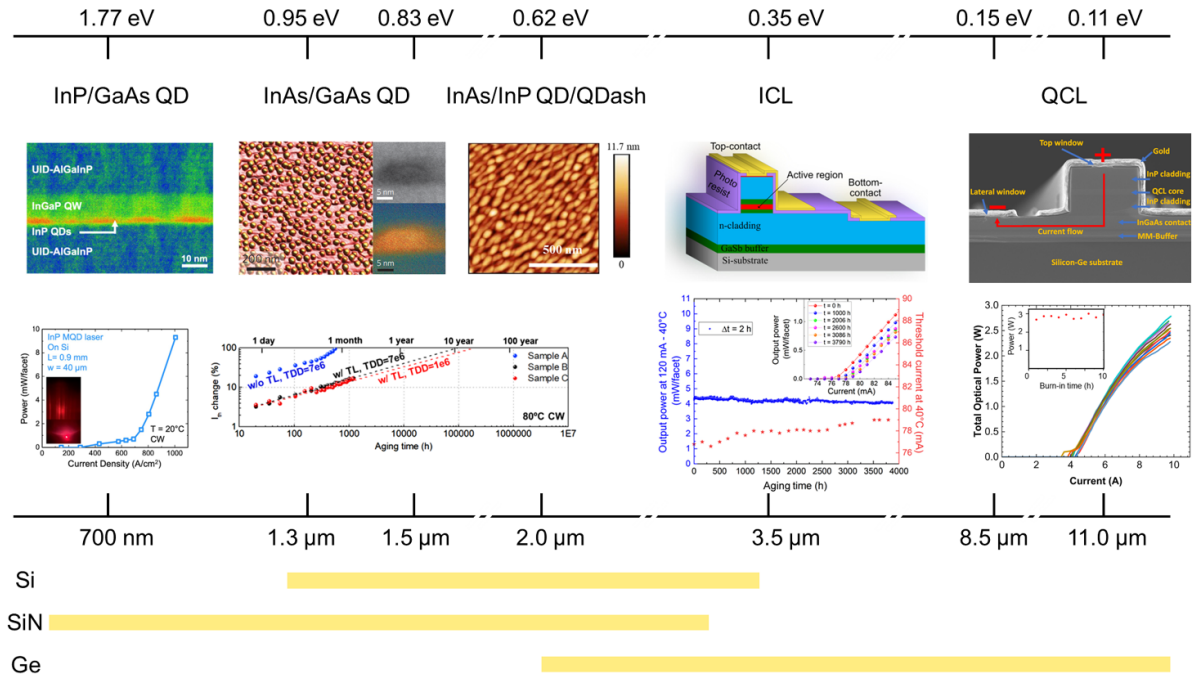

Figure 8. Dislocation less-sensitive quantum dot/dash, interband cascade, and quantum cascade lasers grown on Si, covering the spectrum range from 700 nm to above 11.5 μm. From left to right: Reprodued with permission from [61] © The optical Society. Reproduced from [43], with permission from Springer Nature. Reproduced with permission from [48] © The optical Society. Reproduced from [62]. CC BY 4.0. Reproduced with permission from [45] © The optical Society. Reprinted from [63], with the permission of AIP Publishing. The bottom diagram represents the transparency window of the Si, SiN, Ge waveguide, respectively.

on Si as a viable device technology [43]. 1.3 μm InAs/GaAs based QD lasers grown on Si with a TDD of 7×10^6 cm^{-2} and misfit dislocation filters have reported an extrapolated lifetime exceeding ten years [48]. Additionally, zero-dimensional QDs, with their delta function-like density of states, can benefit the laser performance in aspects such as temperature stability,

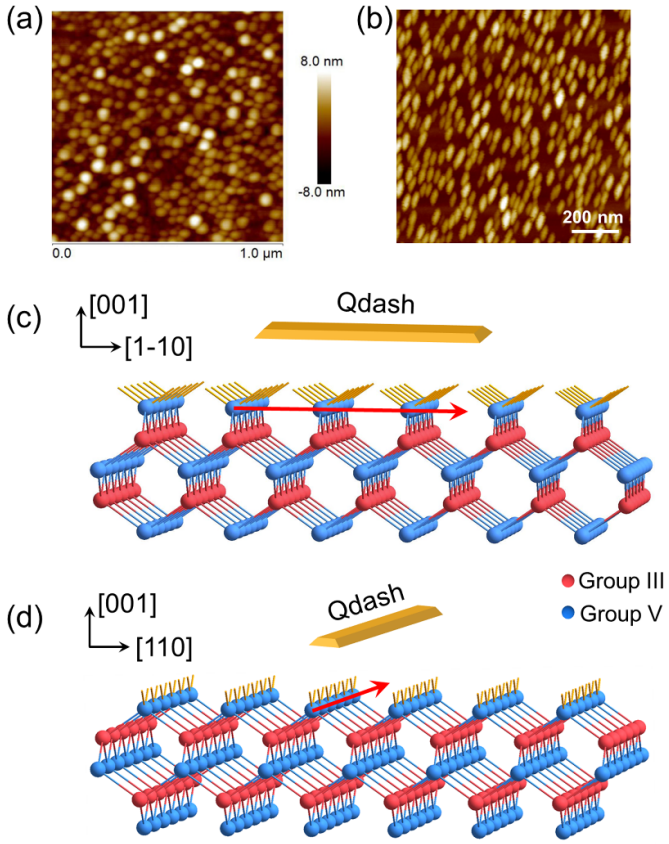

Figure 9. The formation of QD and Qdash. (a) InAs QD and (b) InAs Qdash grown on InP-based compounds. Reprinted from [64], with the permission of AIP Publishing. (c) and (d) Group-V stabilized surface with relaxation, along the two orthogonal <110> direction, respectively, showing the formation of elongated Qdash.

reduced threshold, reduced sensitivity to external reflections and narrow linewidth. To date, a variety of 1.3 μm InAs/GaAs QD lasers have been integrated on Si by direct epitaxy, including Fabry–Perot lasers, micro-disk/ring lasers, photonic crystal lasers, distributed feedback (DFB) lasers, and mode-locked lasers [49–55]. For detailed discussions, readers can refer to previous review articles [56–60].

The growth of self-assembled QDs hinges on strain, or lattice mismatch, with the underlying layer. The ensuing elastic strain relaxation facilitates the formation of discrete dots via the Stranski–Krastanov growth mode. In the case of InAs/GaAs based QDs, a 7% lattice mismatch facilitates the formation of symmetrically shaped dots. The construction of 1.55 μm C-band lasers requires the growth of InAs QDs on InP-based materials or metamorphic buffers. However, the 3% lattice mismatch between InAs and InP yields less strain for dot formation. QDs with smaller height/diameter aspect ratios or quantum dashes (Qdash) are usually observed (figures 9(a) and (b)), influenced by the specific growth conditions [64, 65]. Given the relatively weaker strain, surface reconstruction can play a more prominent role in the formation of InAs/InP Qdash elongated along the [1–10] direction. This elongation could be attributed to the anisotropic surface reconstruction along the two orthogonal <110> directions. On the group V stabilized surface, the relaxed surface dangling bonds (as indicated in figure 9(c)) will form group V-group V dimers along the [1–10] direction [66, 67], which induces the formation of InAs Qdash along the same direction. In the orthogonal [110] direction (figure 9(d)), bond distortion between the dimer pairs could encourage easier aggregation orthogonal to the Qdash direction. Through engineering the size/shape of the dots and their surrounding cladding matrix, QD/Qdash lasers can access a wide range of wavelengths [61, 62, 68–70]. Combining the QD/Qdash gain medium with optimized III–V/Si templates that exhibit low TD density, it becomes feasible to grow and fabricate diode lasers on Si ranging from 700 nm to 2 μm in wavelength (see figure 8).

3.2. *Mid-infrared interband cascade and QCLs grown on Si*

Although conventional type-I QWs with interband carrier transitions are sensitive to the dislocations, the ICLs and QCLs, which are commonly utilized as mid-infrared light sources, can exhibit a higher tolerance to dislocations. For ICL utilizing type-II carrier transitions, the conduction and valence band edges can be engineered to modify the relative positioning between the type-II transition and the defect state located within the mid-bandgap (refer to figures 7(c) and (d)). This enhances the probability of radiative recombination and mitigates the effects of the dislocations on device performances. This has been demonstrated by GaInSb/InAs type-II QW ICLs grown on GaSb/Si templates, lasing at the 3.5 μm wavelength [45]. Despite a relatively high TD density ($\sim 5 \times 10^8$ cm^{-2}) observed in the active region, an extracted lifetime of 312 000 h under continuous wave (CW) operation at 40 °C was achieved. This type-II QW band-structure can be further explored in other material systems to produce lasers grown on Si with dislocation tolerance. Additionally, the recent advancement in GaSb growth on V-grooved Si have resulted in a low TD density of 2×10^7 cm^{-2} and a smooth surface [20]. The improved GaSb/Si buffers, in conjunction with the ICL and QCL, could potentially elevate the performance and lifetime of mid-infrared lasers grown on Si. In relation to the Sb-based type-II superlattice (T2SL), recent studies have also suggested that the Ga-free InAs/InAsSb T2SL could exhibit dislocation tolerant characteristics [71]. This could be another avenue for mid-infrared detectors grown on Si.

Moving to longer wavelength, QCLs exploit the electron transition between different minibands within the conduction band. Their unipolar carrier transport can bypass dislocation assisted electron-hole recombination (refer to figures 7(e) and (f)) [47, 72]. Consequently, QCLs grown on Si can exhibit performance comparable to those grown on native III–V substrates [73, 74]. In this scenario, rather than acting as non-radiative recombination centres, dislocations could affect the barrier/well interface quality, leading to poor electron tunnelling, reduced carrier lifetime, increased carrier leakage, and increased internal loss [72]. By tailoring the conduction band offset, QCLs based on different material systems can cover wavelengths ranging from $\sim$3 μm up to 18 μm. Recently, Slivken and Razeghi demonstrated CW operation of 8.5 μm InP-based QCLs grown on InP/Si templates up to 343 K,

achieving output power >0.7 W at near room temperature [46]. In addition to the mid-infrared (MIR) lasers grown on Si, the epitaxial integration could also incorporate MIR optical waveguides. Germanium (Ge), which is often utilized as a buffer layer grown on Si to bridge the lattice constant difference between Si and GaAs, has a large transparency window in the MIR region than the Si or SiN waveguide (figure 8), making it attractive for MIR photonic integration. Growth of 11.5 μm QCLs on 8-inch diameter Ge-coated Si substrates (see figure 8) showcased an output power exceeding 3 W at room temperature, and good near-term reliability [63].

3.3. State-of-the-art performance of III–V lasers grown on Si

Table 2 presents a range of high-performance III–V lasers produced using the blanket heteroepitaxy approach, spanning spectral coverage from ∼700 nm to near-infrared, and extending to mid and long infrared wavelengths. Depending on the desired applications, these lasers are constructed on various III–V/Si templates, such as the GaAs/Si, InP/Si, and GaSb/Si buffers. They employ dislocation less-sensitive gain mediums, including QD/Qdash, ICL, and QCL. To date, long-lived 1.3 μm QD lasers and mid-infrared ICLs have been more successfully demonstrated. The performance of 1.5 μm QD/Qdash lasers grown on Si requires further improvement and their reliability is not yet fully established.

As the high-performance 1.3 μm QD lasers grown on Si progresses towards practical applications and developing reliable longer-wavelength lasers on Si becomes more prevalent, the subsequent query pertains to the on-chip coupling of these lasers to optical waveguides. The blanket heteroepitaxy of III–V lasers on Si wafers can access technologies already established in InP-based generic integration, such as selective-area QD intermixing, butt-joint regrowth, etc., to combine different bandgaps and implement light emission, modulation, and transmission all within the III–V layer. Alternatively, epitaxial III–V lasers on Si can be integrated onto the Si photonic platform or the high thermal conductivity silicon carbide (SiC) platform through heterogeneous bonding or transfer printing techniques. In both cases, heteroepitaxy on Si reduces substrate cost and provides scalability to 300 mm Si technology.

Perhaps a true monolithic integration path to couple QD lasers to Si-photonic waveguides could be achieved through selective growth of the lasers onto the SOI substrates. One main challenge here is the thick III–V buffers required for defect reduction. Recent research has focused on growing lasers inside SOI recesses to vertically align the laser active region with Si-photonic waveguides (figure 10) [75, 76]. Wei *et al* designed a fork-shaped edge coupler and measured output power of a few mW coupled out of the Si waveguide, yielding an estimated coupling efficiency of approximately −6.7 dB [75]. Remis *et al* demonstrated the 2.3 μm GaSb-based diode lasers grown in the recess of pre-patterned Si photonic substrates (figure 10(c)) [77]. These GaSb-based laser, with dry-etched facets, were butt-coupled to SiN waveguides with around 10% light coupling efficiency.

4. III–V bufferless lasers selectively grown on Si

4.1. Bufferless III–V growth on Si for optically pumped lasers

Although epitaxial lasers on III–V buffers grown on Si have produced long-lived 1.3 μm QD lasers, a parallel effort focusing on bufferless III–V lasers selectively grown on Si demonstrates unique advantages. The bufferless feature allows close placement between the III–V gain medium and the passive waveguides, which can potentially help implement advanced couplers, including evanescent coupling and adiabatic coupling, for enhanced coupling efficiency. In this case, geometrically defined growth methods harnessing the epitaxial necking effect, for instance aspect ratio trapping (ART), are used to filter out/block TDs quickly and produce III–V materials with a low TD density [78]. The pairing of Si V-groove epitaxy with ART can further exclude APBs, resulting in highly uniform III–V nano-ridges grown on Si [79]. Han *et al* successfully demonstrated the growth of InP/InGaAs nano-ridges on SOI substrates, achieving room-temperature optically pumped lasing in the 1.5 μm band from the fabricated nano-ridge laser arrays (figures 11(a)–(d)) [80–82]. Direct growth of these nano-ridge lasers on the Si photonics 220 nm SOI substrates was also reported [83].

Building on the ART growth on V-grooved Si, III–V nano-ridge lasers outside the growth trenches have been developed (figure 11(e)) [84]. The shape of the nano-ridge laser cavity and the positioning of the quantum wells can be engineered by tuning growth parameters. Shi *et al* demonstrated 1 μm wavelength optically pumped nano-ridge lasers with index-coupled DFB gratings and loss-coupled DFB metal gratings (figure 11(g)) [85, 86]. Colucci *et al* used the InGaAs nano-ridges with inserted MQWs to reach 1.3 μm O-band lasing [87]. Simulations have been used to investigate different coupling schemes [88]. The air-cladded III–V nano-ridges with sub-micrometer dimensions promote tight optical confinement inside the laser cavity. A carefully designed metal layout is necessary to minimize the overlap of the metal with the optical field. The developed loss-coupled DFB metal grating could potentially be used to realize metal contacts needed for an electrically driven laser.

Instead of performing selective area epitaxy along the vertical growth direction, lateral epitaxy methods, including template-assisted selective epitaxy (TASE), lateral ART or tunnel epitaxy, opens a new growth paradigm to realize in-plane dislocation-free III–V materials onto Si or insulator platforms. In the TASE approach, the growth of III–V materials is initiated from a restricted Si surface (generally <100 nm) to facilitate elastic strain relaxation and prevent the dislocation formation [89]. The III–V seed is subsequently guided by a hollow SiO_2 template which provides a great control over the shape and dimension of the resultant III–V crystals. Direct growth of vertical, horizontal and stacked nanowires and nanowire heterojunctions have been achieved [90]. Co-integration of diverse III–V materials also becomes possible

Table 2. Key metrics of high-performance dislocation less-sensitive III–V lasers by blanket heteroepitaxy. All the lasers operate under electrical injection. (I_{th}: threshold current, J_{th}: threshold current density, T_{max}: maximum lasing temperature, T_0: characteristic temperature (at room temperature), RT: room temperature, CW: continuous-wave, FP: Fabry–Pérot, DFB: distributed feedback, WG: waveguide).

Year	Gain medium	λ (nm)	Laser type	Cavity size (μm^2)	Operation condition	I_{th} (mA) /J_{th} (A cm^{-2})	Slope efficiency (W/A)	Output power (mW)	T_{max} (°C) /T_0 (K)	Advantages	References
2021	InP QD	726	FP	40 × 900	RT, CW	NA/690	—	>5	50/65	On-axis (001) Si	[61]
2022	InP/GaAsP QD	750	FP	70 × 2000	RT, pulse	NA/657	—	>10	95/74	On-axis (001) Si	[68]
2016	InAs/GaAs QD	1316	FP	50 × 3200	RT, CW	NA/62.5	0.165	>10	120/51	Extrapolated lifetime 100 158 h, (001) Si	[43]
2017	InAs/GaAs QD	1300	Ring	5 μm radius	RT, CW	0.6/NA	—	>1	100/197	On-axis (001) Si	[50]
2018	InAs/GaAs QD	1300	DFB	2.2 × 1500	RT, CW	12/550	0.024	>0.5	N/A	(001) Si	[51]
2019	InAs/GaAs QD	1230	Tunable	—	RT, CW	33/NA	—	2.7	N/A	On-axis (001) Si	[52]
2019	InAs/GaAs QD	1300	Mode locked	—	RT, CW	42/NA	—	>10	N/A	On-axis (001) Si	[53]
2020	InAs/GaAs QD	1310	DFB	3 × 1500	RT, CW	20/440	—	4.4	70/NA	On-axis (001) Si	[54]
2021	InAs/GaAs QD	1300	DFB	3 × 800	RT, CW	4/250	—	2.8	75/103	Directly bonded on SOI	[55]
2021	InAs/GaAs QD	1300	FP	4 × 1500	RT, CW	NA/266	0.158	65	108/167	Extrapolated lifetime > 22 years On-axis (001) Si	[48]
2023	InAs/GaAs QD	1300	FP	3 × 3000	RT, CW	65/NA	0.025	6.8	85/108.1	Si-WG coupled, Embedded laser	[75]
2018	InAs/InAlGaAs QD	1500	FP	10 × 5000	RT, pulse	NA/1600	0.15	110	80/58.7	On-axis (001) Si	[69]
2020	InAs/InAlGaAs Qdash	1580	FP	6 × 1500	RT, CW	50/1300	—	44	59/44.8	On-axis (001) Si	[70]
2021	GaSb-based ICL	3490	FP	8 × 2000	RT, CW	45/NA	0.3	20	50/43	Extrapolated lifetime 312 000 h, On-axis (001) Si	[45]
2020	InAs/AlSb QCL	8000	FP	14.5 × 3600	RT, pulse	NA/920	—	>50	NA/136	On-axis (001) Si	[73]
2023	InP-based QCL	8100	FP	25 × 3000	RT, pulse	NA/1500	0.72	1640	79/167	On-axis (001) Si	[74]
2023	InP-based QCL	8350	FP	11 × 5000	RT, CW	NA	—	>0.7	69/NA	(001) Si	[46]
2023	InP-based QCL	11 500	FP	26 × 3000	RT, pulse	NA/4300	—	3000	N/A	Ge-coated (001) Si	[63]

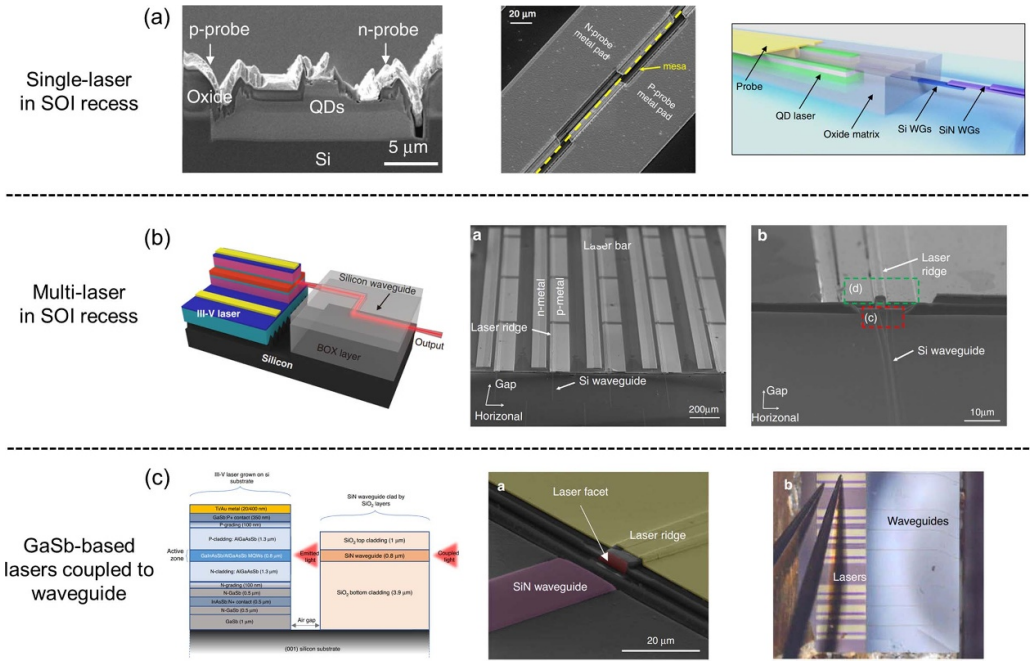

Figure 10. III–V lasers grown in SOI recess for coupling with waveguides. (a) Single QD laser grown in SOI recess. Reproduced from [76]. CC BY 4.0. (b) Multi QD laser array grown in SOI recess and fork-shaped Si edge coupler. Reproduced from [75]. CC BY 4.0. (c) 2.3 μm GaSb-based lasers grown in SOI recess coupled with SiN waveguide. Reproduced from [77]. CC BY 4.0.

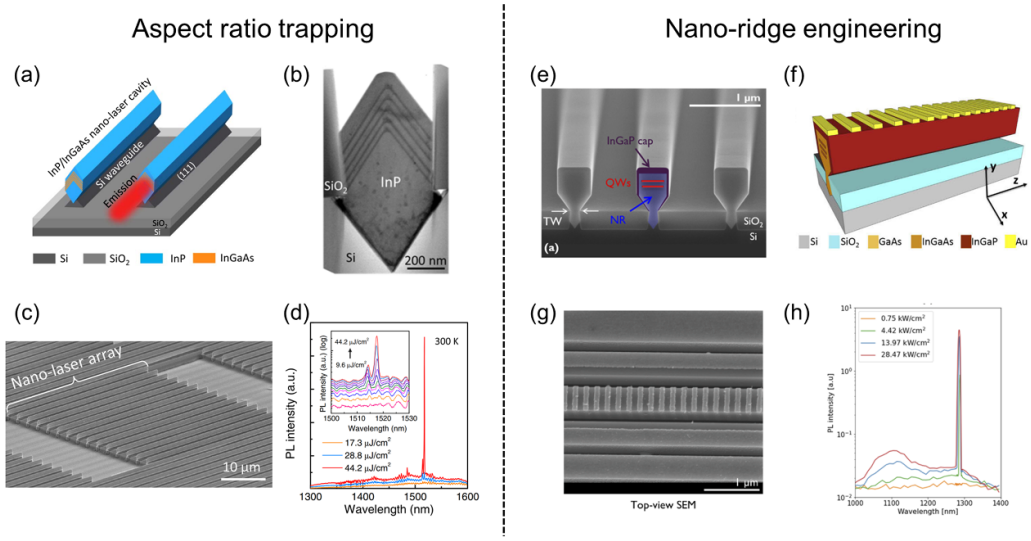

Figure 11. III–V bufferless lasers selectively grown on Si. (a) Schematic of InP/InGaAs nano-ridge laser array grown on SOI substrate. (c) 1.5 μm-band InP/InGaAs nano-laser array grown on SOI and (d) the lasing spectrum. (a), (c), (d) Reprinted with permission from [81] © The optical Society. (b) Cross-section TEM image. Reprinted with permission from [80] © The optical Society. (e) Nano-ridge engineering on Si. (g) SEM image of the nano-ridge laser with loss-coupled DFB metal gratings. (h) Nano-ridge DFB laser emitting at O-band. Reprinted with permission from [87] © The optical Society. (f) Schematic of nano-ridge with DFB metallic grating. Reprinted with permission from [86] © The optical Society.

by tailoring template design [91]. By expanding the template dimensions, the III–V crystal can evolve into micro-disks or rings, which have enabled room temperature optically pumped lasing at the 850 nm and 920 nm bands [92]. Room temperature telecom band lasing has also been achieved by applying III–V TASE in a Si photonic crystal cavity (figure 12(b)) [93]. The flexible placement of alternating III–V gain materials and Si dielectric (loss) nanorods is also interesting for implementing the Su–Schrieffer–Heeger topological photonic lattice to explore the interface mode for single-mode lasing [94]. Furthermore, the side-by-side placement of the III–V and Si enables direct butt coupling from the photodetectors (PD) to the in-plane Si waveguide, as depicted in figure 12(c). The Si waveguide-coupled PiN nano-PD demonstrated a responsivity of up to 0.2 A/W at −2 V and a 3 dB bandwidth exceeding 70 GHz [95].

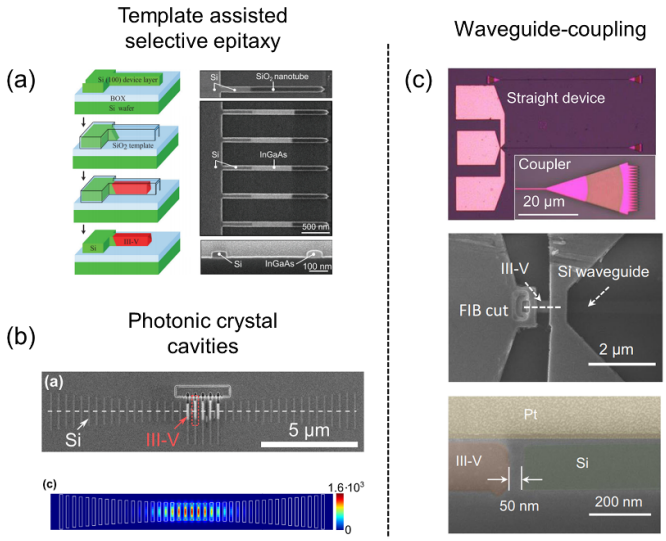

Figure 12. Templated assisted selective epitaxy (TASE). (a) Basic concept of template assisted selective epitaxy. Reprinted from [89], with the permission of AIP Publishing. (b) Photonic crystal laser at telecom band by TASE. Reprinted with permission from [93]. Copyright (2020) American Chemical Society. (c) Si waveguide coupled III–V photodetectors on (001) SOI by TASE. Reproduced from [95]. CC BY 4.0.

To further expand the area of defect-free III–V materials usable for fabricating electrically driven lasers with sufficient output power, the lateral ART or tunnel epitaxy approach have been developed, with one example depicted in figure 13(a) [96]. Plan-view TEM investigations have evidenced effective dislocation trapping in lateral epitaxy [97]. Here, the lateral aspect ratio is the ratio of the epitaxial width of the III–V membrane to its thickness. Hence, the wider the lateral growth, the better the dislocation necking effect [98, 99]. From TASE to lateral ART approach, growth of InP nanowire arrays and large dimension InP membranes have been reported (figures 13(b) and (c)). Yan *et al* demonstrated such a monolithic InP on SOI platform, where the epitaxial width of the InP was extended to 7 μm (figure 13(d)) [96]. The large dimension InP membrane-on-insulator demonstrates an atomically flat top surface (figure 13(e)), enabling subsequent top-down processing for various optical pumped devices including InP microwire arrays, square cavity lasers, and microdisk lasers (figure 13(f)). The insertion of InGaAs MQWs further led to telecom band optically pumped lasers [100]. The monolithic InP/SOI platform permits the implementation of optical functionalities using the III–V wire array and membranes, as well as the interfacing of light with Si-based passive waveguides [101]. Xue *et al* demonstrated InP/InGaAs PiN photodetectors coupled with a Si waveguide on the monolithic InP/SOI platform (figure 13(g)). The PDs exhibited a low dark current of 0.002 A cm^{-2}, responsivity of 0.4 A/W at 1.3 μm, and a 3 dB bandwidth exceeding 52 GHz [102].

4.2. Towards electrically injected bufferless lasers fully-integrated with Si photonics

The bufferless epitaxy of III–V materials on patterned Si or SOI substrates uses geometrically confined methods to achieve low defect density. As a result, the realization of electrically injected lasers are largely dictated by their specific growth technique. With limited volume of the micro- and nano-sized materials available to form laser cavities, introducing metal contacts for electrical injection lasers requires careful mitigation of resultant metal-induced optical losses. For nano-ridge lasers on V-grooved Si, a narrow p-metal contact on the tip of the nano-ridges (figure 14(a)) [103, 104], or a loss-coupled DFB metal grating can be designed to minimize the overlap with optical modes, thereby reducing metal-induced optical losses [86]. The n-metal contact can be deposited on the n-Si layer, inclusive of the defective III–V/Si interface within the electrical pathway. To couple light to Si waveguides, various coupling schemes, such as the directional coupler and adiabatic coupler, have been proposed (figure 14(b)) [88]. In terms of the lateral ART or lateral tunnel epitaxy, it is feasible to produce in-plane membranes with increased size, as dictated by the lateral growth width, for laser fabrication. Yan *et al* developed a monolithic InP/SOI platform, featuring InP membranes with a 7 μm InP epitaxial width [96]. This allows for the patterning of metal contacts at both ends of the membrane, without involving the defective III–V/Si interface, to mitigate metal loss (figure 14(c)) [105]. The active gain medium can be either inserted during lateral epitaxy, or selectively regrown on top of the InP membrane [106]. Although experimental demonstration is not established yet, such membrane lasers using InP bonded onto the SOI substrates have demonstrated remarkable performance [107]. As illustrated in figure 14(d), the membrane lasers produced by lateral ART or lateral tunnel epitaxy can be configured for butt coupling with Si waveguides. Evanescent coupling to Si or SiN waveguides is also feasible by engineering the growth templates.

5. III–V nanowire photonic crystal lasers grown on Si

5.1. Dislocation-free epitaxy of nanowires on mismatched substrates

Nanowire heteroepitaxy offers a unique platform for monolithic III–V/Si integration. By confining the III–V/Si heterointerface at tens of nanometres scale, the lateral elastic relaxation towards nanowire sidewalls can increase critical thicknesses significantly [108] and therefore, dislocation-free III–V nanowires can be grown on Si. Epitaxial growth of III–V nanowires can be categorized by two approaches: metal-catalyzed growth and catalyst-free selective area growth. The metal-catalyzed method employs a metal nanoparticle to assist nanowire growth via the vapor-liquid-solid (VLS) growth mode. Nanowire growth occurs through the precipitation of

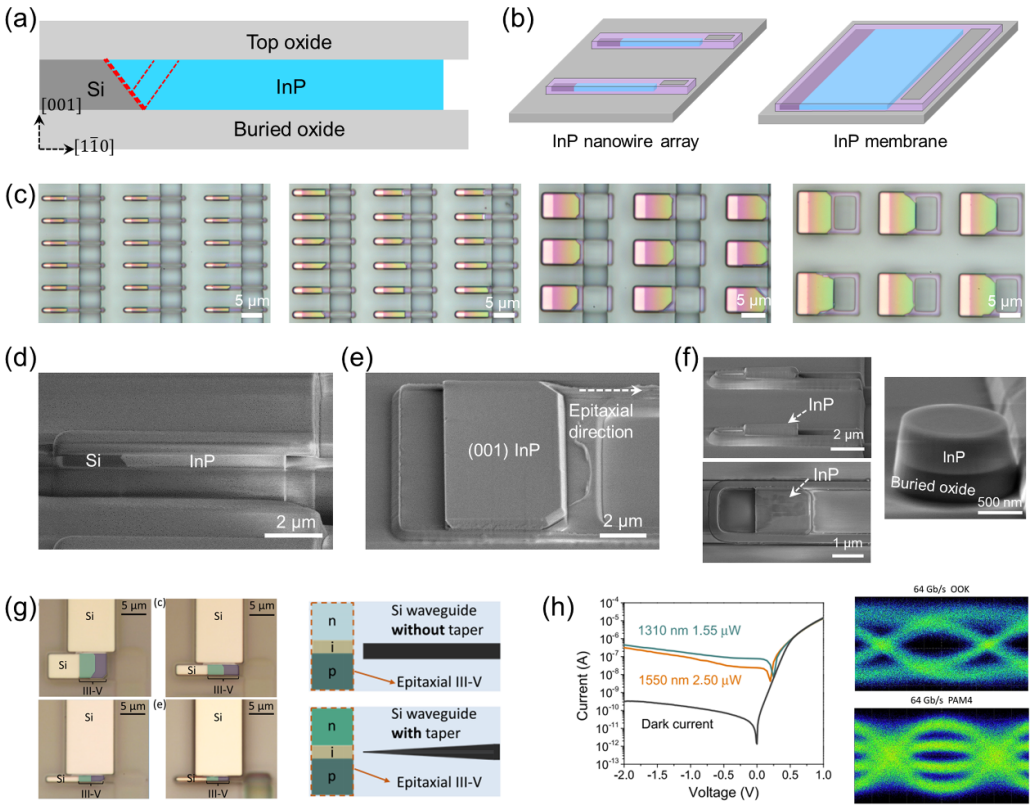

Figure 13. (a) Concept of lateral ART and lateral tunnel epitaxy technique. (b) Schematic showing monolithic InP/SOI platform with InP nanowire array and large-dimension membranes on (001) SOI wafers. (c) Optical microscope images of as-grown InP nanowire and membrane array. (d) Cross-sectional SEM image showing the InP-on-insulator with 7 μm width. (e) SEM image of InP membrane on SOI. (f) Nanowire lasers, square cavity and microdisk lasers demonstrated on the InP/SOI platform. Reproduced from [96]. CC BY 4.0. (g), (h) High-performance InP/InGaAs PiN PDs coupled with Si waveguide on the InP/SOI platform. (g), (h) Reprinted with permission from [102] © The optical Society.

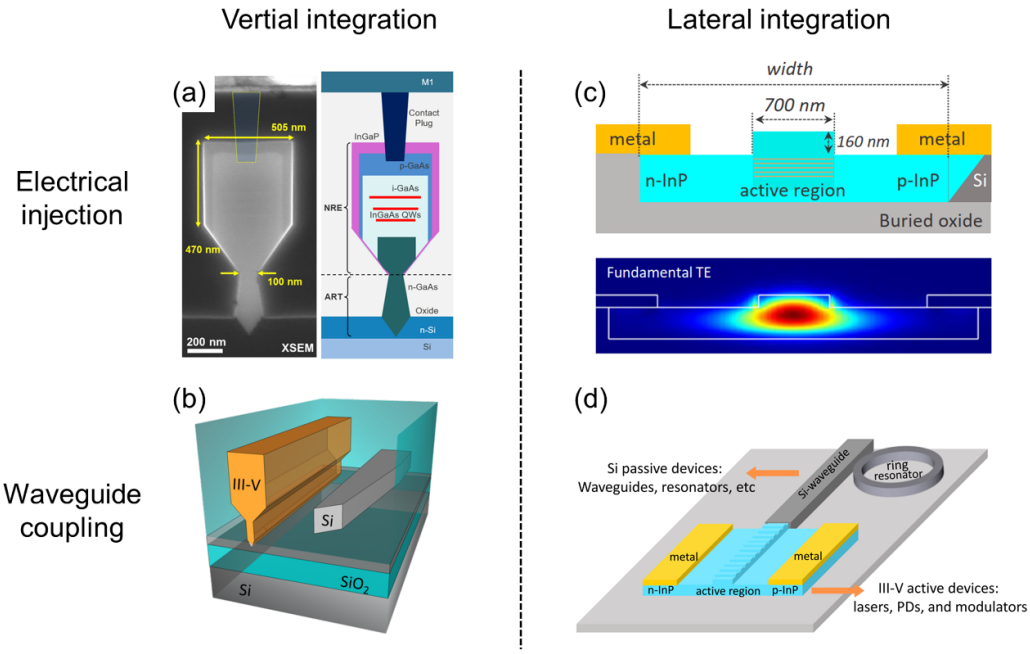

Figure 14. (a) Cross-section SEM photo of a GaAs nano-ridge. © [2021] IEEE. Reprinted, with permission, from [103]. (b) Coupler design from the nano-ridge laser to Si waveguides. Reprinted with permission from [88] © The optical Society. (c) Proposed electrically injected bufferless lasers by lateral ART approach. (d) Schematic illustrating the direct butt coupling between membrane laser and Si waveguides. © [2021] IEEE. Reprinted, with permission, from [105].

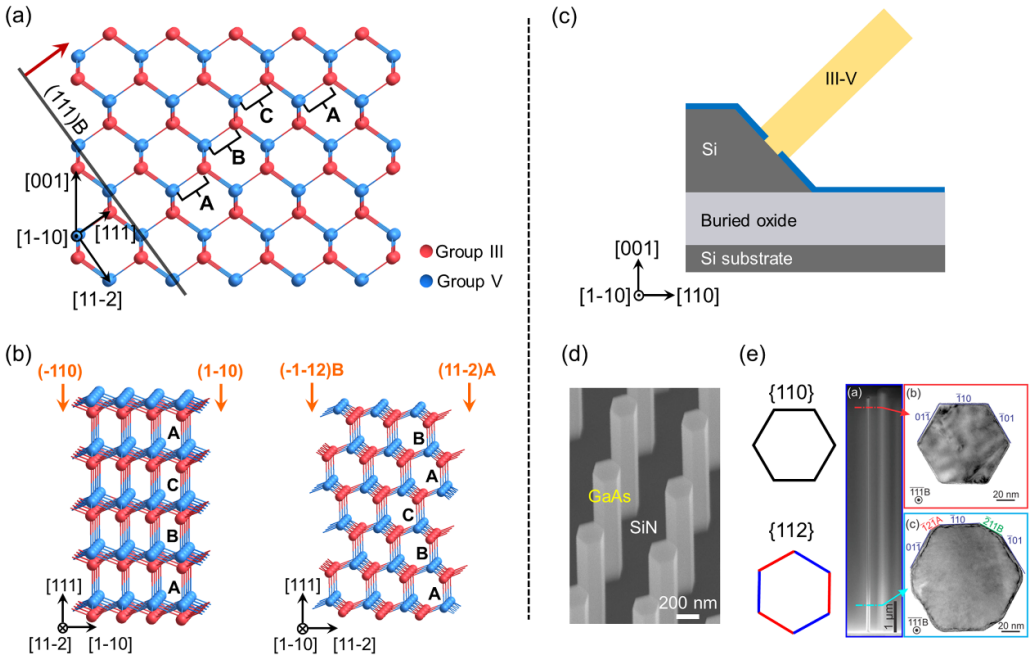

Figure 15. (a) Schematic to show inclined {111}-orientated nanowires on (001) substrates. (b) The {110} and {112} facets on (111) substrates. (c) Schematic to illustrate III–V nanowires grown from {111} Si facets on (001) SOI substates. (d) Vertical GaAs nanowires grown on (111) Si substrates. (e) SEM and TEM images showing the side-facets of nanowires. Reprinted with permission from [113]. Copyright (2014) American Chemical Society.

material from an oversaturated droplet catalyst. Depending on the way of introducing metal particles, metal-catalyzed VLS growth can be further divided into the foreign metal (usually gold) catalyzed and self-catalyzed (group-III elements) growth of III–V nanowires [109, 110]. The catalyst-free selective area growth of nanowires employs the same vapor-solid (VS) growth mode as conventional selective area growth. A mask layer is used to define growth openings [111]. Nanowire formation is driven by facet formation, where facets with high growth rates vanish during the nucleation process, and the nanowire is enclosed by facets with low growth rates. Position-controlled III–V nanowires on Si substrates with exceptional uniformity can be produced, important for practical applications in nanometer-scale electronic and photonic devices. Notably, photonic crystal lasers can be constructed utilizing these Si-based nanowires. This section will focus on the catalyst-free III–V nanowires for photonic crystal lasers on SOI substrates, which include photonic crystal defect-mode lasers, photonic crystal band edge lasers, as well as for the topological lasers and electrically injected lasers.

III–V nanowires typically exhibit a preferred growth direction towards the [111] direction, with III-As, III-Sb nanowires showing the (111)B preference, while InP nanowires generally presents the (111)A orientation. It is also possible to grow nanowires on the CMOS-standard (001)-oriented SOI substrates by creating inclined (111) Si facets for mask patterning (figure 15(c)) [112]. Figure 15(a) schematically illustrates the 'ABC'-type stacking in the (001)-oriented zincblende crystal, where each layer in the ABC stacking includes one group III layer and one group V layer. The 'ABC'-stacking direction is towards the [111] direction, indicating the orientation of the inclined nanowire on (001) substrates. To facilitate nanowire growth in the vertical direction, (111)-oriented substrates are often used, as shown by the SEM photo of vertical GaAs nanowires on (111) Si substrates (figure 15(d)). These nanowires typically present a hexagonal cross-section, with the six side-facets oriented along the low-energy {110} planes. In instances where the side-facets are under-developed, the {112} planes, another set of the low-index facets, may also emerge at the intersections of the {110} planes. This is illustrated by the arrangement of the six {110} and {112} facets in figure 15(e) [113]. Figure 15(b) schematically illustrates the non-polar {110} and the polar {112} facets in zincblende crystal along the vertical [111] direction.

5.2. *Photonic crystal nanowire lasers*

The capability to grow III–V nanowires on pre-defined positions with high uniformity provides a bottom-up approach for constructing photonic crystal lasers and even topological lasers. Compared with the top-down etching approach, bottom-up epitaxy of nanowires can bypass the constraints from material mismatch, allowing photonic crystal lasers integrated onto dissimilar substrates with ultra-small device footprint. The vertical and smooth side-facets and the capability of *in-situ* surface passivation can offer both minimized optical propagation loss and reduced non-radiative surface recombination [114]. The catalyst-free selective growth

Table 3. Key metrics of III–V photonic crystal nanowire lasers (MQW: multi-quantum well, PDMS: polydimethylsiloxane, RT: room temperature, CW: continuous wave).

Year	λ	Gain medium	Cavity	Optical/electrical pump	Threshold	Operation condition	Substrate	Reference
2011	1000 nm	InGaAs	Photonic crystal	Optical	625 W cm^{-2}	RT, pulse	Transferred by PDMS	[114]
2017	1120 nm–1440 nm	InGaAs	Nanobeam	Optical	80–110 μJ cm^{-2}	RT, pulse	SOI	[115]
2017	1100 nm	InGaAs	Nanobeam	Optical	100 μJ cm^{-2}	RT, pulse	SOI	[116]
2017	1100 nm–1300 nm	InGaAs	Square lattice	Optical	45 μJ cm^{-2}	RT, pulse	SOI	[117]
2018	1300 nm	InGaAs	Square lattice	Optical	200 μJ cm^{-2}	RT, pulse	SOI	[118]
2019	369 nm	GaN/AlGaN disk	Triangular lattice	Electrical	2.1 kA cm^{-2}	RT, CW	Sapphire	[119]
2020	523 nm	InGaN/AlGaN disk	Triangular lattice	Electrical	400 A cm^{-2}	RT, CW	Sapphire	[120]
2021	488 nm	InGaN/GaN MQW	Triangular lattice	Electrical	780 A cm^{-2}	RT, CW	Sapphire	[121]
2021	850 nm	InP	Triangular lattice	Optical	14 μJ cm^{-2}	RT, pulse (CW, 77 K)	InP	[122]
2022	1280 nm	InGaAs	Stretched/ Compressed honeycomb lattice	Optical	1.25 μJ cm^{-2}	RT, pulse	SOI	[123]

approach has yielded nanowire arrays with high uniformity, which have been implemented for photonic crystal defect-mode lasers, band edge lasers and topological photonic cavities [114–123]. Table 3 chronologically lists the key metrics of these photonic crystal nanowire lasers.

Nanowire based photonic crystal defect mode lasers have been realized using both 2D and 1D engineered nanowire arrays. Scofield *et al* demonstrated the photonic bandgap effect inside an array of GaAs/InGaAs/GaAs nanowires by controlling the diameter and pitch of the nanowires [114]. As the nanowires were grown on (111)B GaAs substrates, the nanowire array was embedded in a low refractive index polydimethylsiloxane (PDMS) layer and removed from the GaAs substrate for out-of-plane optical confinement. Room temperature lasing at 1 μm band wavelength was achieved. To realize lasing from nanowires directly grown on Si, one dimensional InGaAs nanowire based nanobeam lasers were grown on SOI substrates (figures 16(a) and (b)) [115, 116]. Given the similar refractive index of Si and III–V materials at the telecom band, the Si device layer has been thinned down to ∼50 nm thickness or etched into mesa structure for improved optical confinement. The nanobeam cavity consists of a reflector at both ends and a tapered cavity in the middle, where the pitch of nanowires is modulated to minimize radiation loss at both ends. With the growth of InGaAs nanowires, indium compositions can be varied to achieve photoluminescence (PL) emission ranging from 1.2 μm to 1.5 μm (figure 16(c)). The fabricated nanobeam lasers thus span the full telecom wavelength. By varying the dimensions of the photonic crystal cavities, the nanobeam lasers fabricated on a single chip can cover a lasing wavelength range of ∼70 nm (figure 16(d)). These nanobeam lasers can also be grown on the (001) orientated SOI substrates by creating nanohole on inclined {111} Si facets [124]. For photonic crystal defect mode laser, a key challenge lies at the trade-off between the cavity's Q factor and the coupling efficiency with adjacent waveguides. To address this, the same group fabricated a 220 nm silicon waveguide at one end of the nanobeam (figures 16(b)), where the coupling efficiency can be improved through adjusting the nanobeam cavity.

2D nanowire arrays can also be used for band edge lasers and photonic crystal surface emitting lasers (PCSELs). PCSELs leverage the photonic band edge mode for enhanced resonance at a single frequency, where the group velocity vanishes at the band edge resulting in gain enhancement. Thanks to the extensive in-plane coherent oscillation and the first-order Bragg diffraction, the vertically diffracted light beam from PCSEL can possess high brightness and good beam quality. Lee *et al* reported the application of a square lattice in the creation of InGaAs nanowire band edge lasers on SOI substrates (figure 17(a)). Room temperature lasing from both 1 μm wavelength and 1.3 μm O-band has been realized [117]. Simulation results suggest the optical mode is effectively confined in the center of the band-edge laser (figure 17(b)). In another study, Tu *et al* demonstrated the triangular lattice InP nanowire array [122]. Interestingly, even though the nanowires were grown on InP substrates without the bottom optical confinement, optical lasing at the 850 nm band was achieved. This could be attributed to the enhanced in-plane light oscillation at the photonic crystal Γ point, as well as the sufficient height (1 μm) of the nanowires. Simulations show the vertically emitted light possesses an average off-normal angle of ∼6° from a lasing area with a 7 μm diameter, which aligns with the far-field measurements in the Fourier plane. Moreover, recent

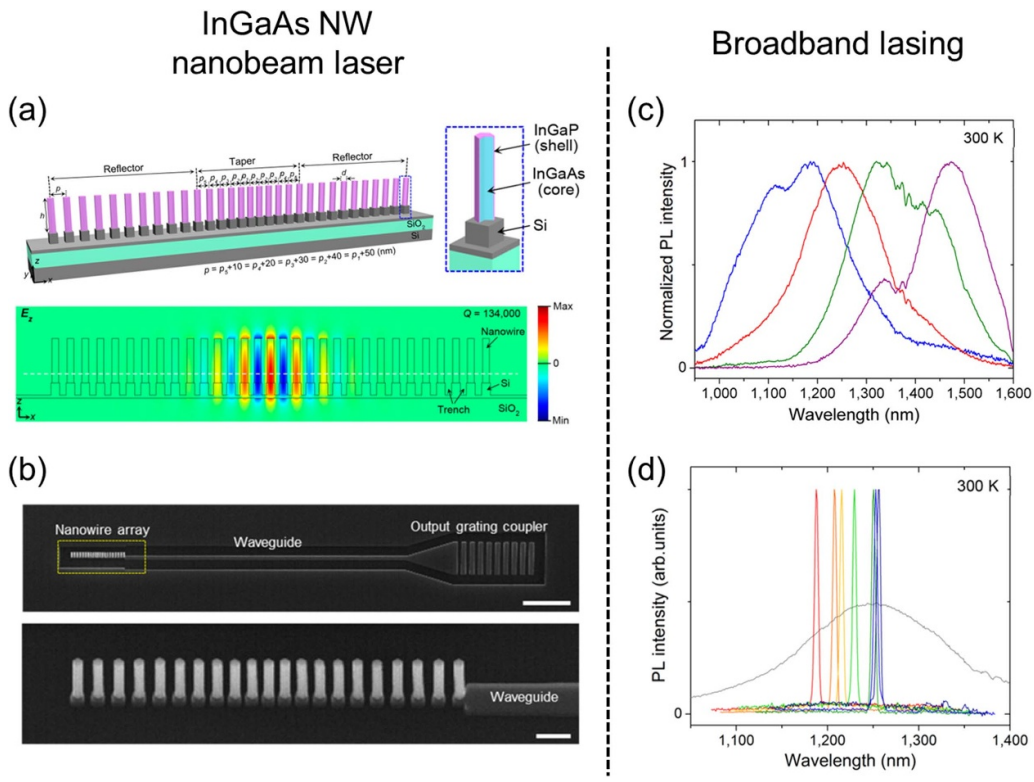

Figure 16. Nanobeam lasers on SOI. (a) Schematic and (b) SEM of nanobeam lases on (111) SOI substrates and coupled with Si waveguides. (c) PL spectra of InGaAs nanowires with different indium composition. (d) Nanobeam lasers with lithography controllable wavelengths on a single chip. Reprinted with permission from [115]. Copyright (2017) American Chemical Society. Reprinted with permission from [116]. Copyright (2017) American Chemical Society.

study indicates the InP nanowire array can function as a polarization converter, which could be applicable for the PICs or optical sensors [125].

The ability to arrange nanowires into photonic crystal structures and to engineer the nanowire array parameters (e.g. nanowire diameter, pitch) on the same chip creates exciting opportunities for emerging topological lasers. A deformed honeycomb lattice structure, including both stretched and compressed honeycomb lattices made of InGaAs/GaAs nanowires, has been realized on SOI substrates for highly directional vertical emission at the Γ point [123]. Room-temperature photonic band edge mode lasing at the 1.3 μm wavelength has been achieved. A topological cavity is fabricated by combining the compressed and stretched honeycomb lattices into one device, as evidenced by the SEM image of figure 18(d). The bottom-up nanowire honeycomb lattice thereby presents a Si-based platform for both band edge lasers and topological surface emitting lasers.

The main roadblock for achieving electrically injected nanowire lasers stem from the small dimension of nanowires and the ensuing significant metal-induced optical loss. One approach towards electrically injected photonic crystal nanowire lasers involves increasing the nanowire height to separate the metal contact away from the optical mode. For catalyst-free GaAs nanowires, the aspect ratio of the nanowire can be manipulated by controlling the growth conditions to favor axial growth for high nanowires. For surface emitting lasers, a circular top metal contact is typically utilized, and the current spreading over the entire photonic crystal nanowire laser must be considered. In a recent demonstration of InGaN/GaN nanocrystal cavity surface emitting lasers, Ra *et al* utilized a thin metal contact (a few nanometers) on the semiconductor surface and a transparent conductive layer to spread the current [120]. Electrical injection CW lasing of 523 nm green light was achieved at room temperature.

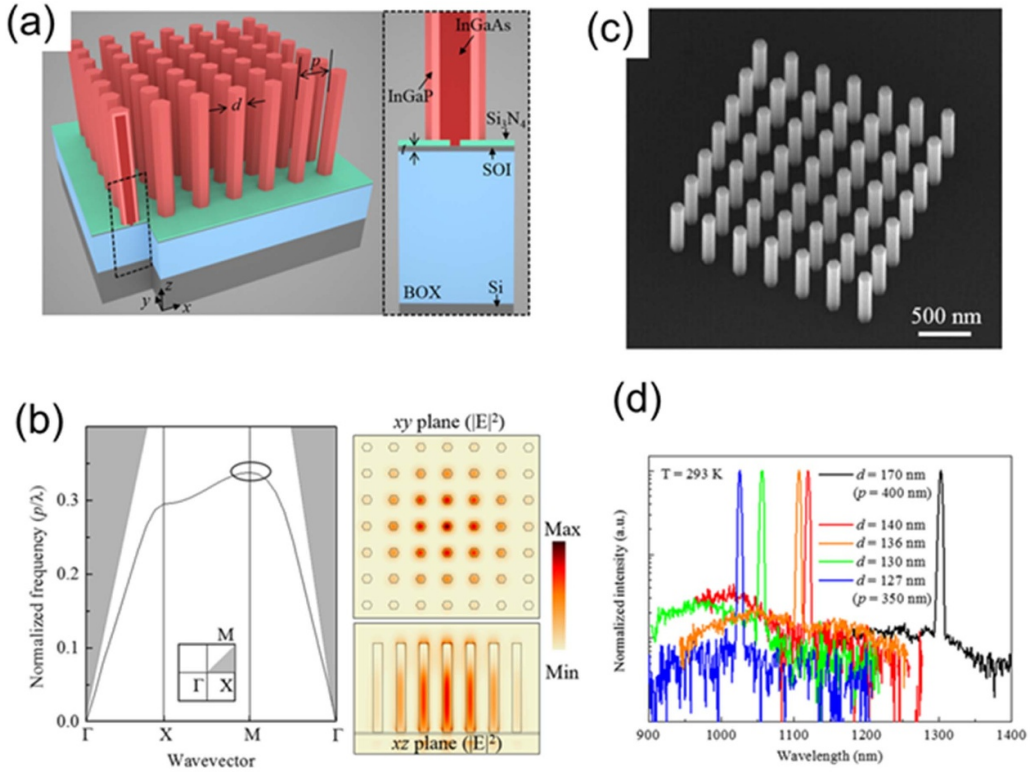

Figure 17. Photonic crystal band edge nanowire lasers. (a)–(d) Square lattice bandedge nanowire lasers on SOI substrates. Reproduced from [117]. CC BY 4.0.

6. Conclusion

In this paper, we first discussed the heteroepitaxy of III–V thin films on Si, followed by a review of III–V lasers grown on Si. Recent progress has yielded APB-free III–V/Si templates suitable to integrate with dislocation insensitive gain mediums. Quantum dot/dash lasers, interband cascade and QCLs, with spectrum ranging from 700 nm to above 11.5 μm, have been effectively demonstrated on Si, exhibiting performance comparable to their counterparts grown on native III–V substrates. Some of these Si-based lasers have shown promising long-term or near-term reliability, making significant strides towards practical applications. The selective bufferless growth methods present the prospects of growing dislocation-free III–V materials on silicon or insulator structures and intimate placement of lasers with Si photonic device, which is promising to integrate with Si photonics. Furthermore, III–V nanowires present a bottom-up platform for photonic crystal and topological lasers, with potential for surface-emitting applications. In light of the rapid progress of growing III–V lasers on Si using these methods, epitaxial integration holds the promise to realize reliable, compact, and cost-effective III–V photonic devices on silicon photonic chips, thereby accelerating the evolution of high-performance, scalable, and commercialized optical systems.

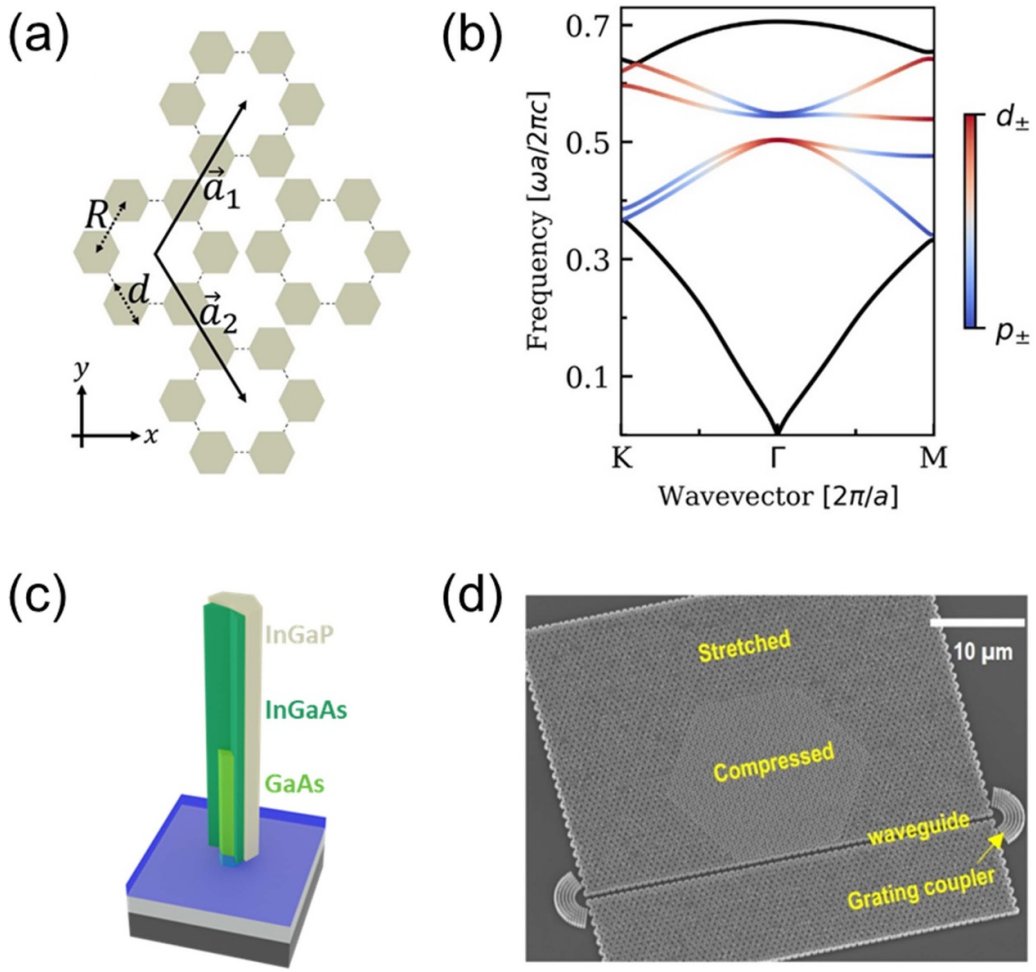

Figure 18. InGaAs/GaAs nanowire platform on SOI. (a) Schematic of a honeycomb lattice. (b) Calculated photonic band structure of the stretched honeycomb lattice. (c) Schematic of InGaAs/GaAs nanowires on SOI. (d) SEM image of a topological optical cavity comprised of the compressed and stretched nanowire honeycomb lattice. Reproduced from [123]. CC BY 4.0.

Data availability statement

No new data were created or analysed in this study.

Acknowledgments

This work was supported by Engineering and Physical Sciences Research Council (Grant Numbers EP/T01105X/1 and EP/V029681/1) and the UKRI Strength in Places Fund (Grant Number 107134). The authors also acknowledge the funding from the Royal Society (IEC\NSFC\211054).

Conflict of interest

The authors declare no conflict of interest.

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