Received: 22 November 2023 | Revised: 13 April 2024 | Accepted: 20 May 2024

IET Power Electronics

DOI: 10.1049/pel2.12726

The Institution of Engineering and Technology WILEY

ORIGINAL RESEARCH

Optimized ultra high voltage gain DC–DC converter with current stress reduction for photovoltaic application

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Abstract

This paper presents a non-isolated DC-DC converter designed to validate ultra-high voltage gain using a modified double boost mode. The objective is to achieve exceptionally high voltage gain by integrating a modified triple boost technique (MTBT), interleaved with second main and auxiliary third MOSFETs, and a modified switched inductor-capacitor (MSLC), effectively doubling the voltage transfer gain. Furthermore, MSLC is combined with the auxiliary third and double main MOSFET to double the voltage gain while concurrently mitigating voltage stress on the auxiliary MOSFET and diodes in the proposed converter (the PC). Additionally, all diodes in the MTBT operate under zero current switching (ZCS) and the double main and auxiliary third MOSFET face very low current stress at ultra-high voltage gain. The input current of the PC remains steady without pulsating at a low duty ratio, making the PC more suitable for renewable energy systems. The PC offers numerous advantages, exhibiting high efficiency and ensuring minimal voltage stress on power devices with low current stress on the power switches. Notably, PC aims to elevate input voltages from 30 V to a variable output range of 335 to 600 V, delivering 440 watts at 96.1% efficiency.

1 | INTRODUCTION

In recent years, the surging demand for renewable energy systems has spurred extensive research in power electronics, specifically focusing on the development of high-gain non-isolated DC-DC converters [1, 2]. These converters play a crucial role in efficiently transforming and managing energy in applications such as photovoltaic (PV) systems, electric vehicles (EVs), and other renewable energy sources. The pursuit of increased voltage gain, enhanced efficiency, and reduced component count has given rise to various innovative converter topologies. Solar and wind energy have gained widespread acceptance on a global scale among these sources. However, a significant challenge associated with photovoltaic solar panels is their inherent variability in producing low-voltage outputs, rendering them unsuitable for applications requiring high DC supply voltages [3]. In [4, 5], to overcome this limitation, the integration of DC–DC converters has become crucial. This integration enables the enhancement of voltage levels for various applications, including LED street lighting, microgrid systems, uninterruptible power supplies, and medical equipment.

Various researchers have suggested different technological approaches for utilizing coupled inductors (CI) in non-isolated DC–DC converters. In [6] suggests an integrated Boost-SEPIC with soft switching for semiconductor devices, ensuring high efficiency. Modified techniques are explored in [7], which introduces a non-isolated high step-up DC–DC converter using a diode-capacitor technique and coupled inductors. Similarly, [8] employs coupled inductors and switched-capacitor cells (SC) to minimize current ripple through an interleaved structure. In [9], a high step-up DC–DC converter is introduced with a modified super-lift structure and coupled inductors, offering snubber-less operation and a reduced component count. Coupled inductors take centre stage in [10], where a high step-up DC–DC converter based on SC and coupled inductors achieves enhanced voltage gain without additional capacitors. These converters have demonstrated significant success in achieving high voltage gain. However, they encounter specific limitations that affect their overall effectiveness. These limitations include the

extensive use of active and passive components, which leads to an increase in parasitic resistance in capacitors and inductors, subsequently reducing voltage gain and efficiency. Moreover, they utilize a low switching frequency to achieve high voltage gain, but this approach necessitates high values of capacitors and inductors. Additionally, the use of silicon power MOSFETs with high internal resistance significantly impacts system efficiency. Furthermore, employing silicon diodes with high reverse recovery currents adversely affects the output voltage and system efficiency. Furthermore, as mentioned in [7], attempts to enhance the voltage transfer gain by modifying the turn ratio of coupled inductors can lead to an increase in internal resistance, which may compromise the overall efficiency of the system. Moreover, in [4, 5, 9–24] converters with coupled inductors experience increased spike voltages on the power switch's during off state because of the inductance with parasitic capacitance of the MOSFETs. While a clamped circuit is employed to address this issue [9, 10], it introduces a potential trade-off, leading to reduced efficiency and increased costs due to the effects of parasitic elements.

One topology, as explored in [2], is the high-gain non-isolated buck-boost DC–DC converter derived from the SEPIC converter. This converter ensures remarkable step-up voltage gain with continuous input current, providing an efficient solution for energy harvesting applications. Building upon this foundation, [3] introduces a new high-step-up DC–DC converter that integrates active-passive inductor cells (APIC), achieving substantial gains through parallel charging and series discharging. In [6, 7, 25–29], a different approach is taken, where a high-gain DC–DC converter combines a modified quadratic boost converter (MQBC) with a unique voltage multiplier (VM) cell, contributing to enhanced efficiency. The pursuit of PV-oriented solutions is evident in [26], where a high step-up three-level DC–DC converter is designed to achieve efficient operation with low input ripples and zero current switching (ZCS) conditions. Bidirectional converters have also garnered attention, as demonstrated in [27] with the introduction of an advanced bidirectional DC–DC converter for heightened gain and efficiency, featuring improved auxiliary networks. The application scope broadens in [28], where a switched inductor-based bidirectional DC–DC converter tailored for EVs and solar PV systems achieves high voltage gain. However, these high-gain converters face obstacles. The increased duty ratio results in higher conduction and switching losses, lowering power density and efficiency. This also places significant stress on power switches and diodes, impacting their reliability and lifespan.

In [30], a high-efficiency, non-isolated, interleaved DC-DC converter is proposed, featuring two modified step-up KY converters. The goal is to achieve increased voltage conversion ratios without the use of coupled inductors. In [5] demonstrates the integration of boosting modules with conventional topologies, resulting in higher voltage gain. In [11] introduces a non-isolated high step-up DC–DC converter employing active SL and SC cells. Transformer-less solutions are investigated in [12], showcasing a high-gain DC–DC converter with reduced duty ratios. The pursuit of high voltage gain is detailed in [14], where a DC–DC boost converter is introduced, achieving six times the gain of a standard boost converter. This design utilizes SL and SC, incorporating a modified (VM) cell for enhanced efficiency and reduced voltage stress. Simplicity and efficiency converge in [15], which introduces a new design for a high-gain DC/DC boost converter ideal for low input voltage applications. Cascading additional cells further increases voltage gain while minimizing passive components. The integration of discontinuous-current quasi-Z-source and SC networks is explored in [16], presenting a solution with low input current ripple and a wide voltage gain range. Although these converters exhibit the potential for substantial voltage transfer gain, they face limitations that hinder overall performance and limit adaptability. These challenges include the need for a high-duty cycle to achieve increased voltage gain, resulting in heightened conduction and switching losses that reduce efficiency.

The DC–DC converter in [17] uses a VM technique for high gain in three modes. In [18] emphasizes a transformer-free design, combining a dual boost converter with an SL structure for non-isolated high-voltage gain. In [19] suggests converters with active and passive SL, SC cells, and an auxiliary switch for high voltage gain in a non-isolated configuration. In [20] employs (SL)/(SC) networks for a high step-up non-isolated DC–DC converter, reducing voltage stress and enabling extension for higher voltage gain. Despite their potential for high gain, these converters face challenges. The elevated duty ratio increases conduction and switching losses, impacting power density and efficiency. The heightened duty ratio also stresses power switches and diodes, affecting reliability. The preference for double inductors and low switching frequencies introduces parasitic resistance, compromising overall performance. In [21] introduces a boost DC–DC converter based on the voltage lift (VL) technique, emphasizing simplicity, low input current ripple, and high voltage gain. In [22] proposes an SL double switch DC–DC converter for compactness and superior performance with fewer components. In [23] presents a transformerless single-switch high-gain DC–DC converter with a (SC)/(SL) cell and a voltage multiplier stage. In [31] adopts an SL/ VM cell for an expandable structure with high current stress. To explore high-gain non-isolated DC–DC converters, [32, 33] introduces four new non-isolated boost topologies using four-terminal PWM high-gain switch cells with an inductor-switch network (LSN). While these converters offer higher gain, challenges include obstacles from various components, impacting system efficiency and performance. There's notable current stress on power switches and high voltage stress on power devices. The complex gate control circuit requires a significantly large space [34].

This paper designs an innovative non-isolated DC–DC converter to validate ultra-high voltage gain and current stress reduction by using a modified double boost mode (MDBM) interleaved with modified triple boost technique (MTBT) and modified switched inductor-capacitor (MSLC). The objective is to achieve exceptionally ultra-voltage gain by merging an MTBT, interleaved with second main and auxiliary third MOSFETs, and an MSLC, effectively doubling the voltage transfer gain. Furthermore, the MSLC is combined with the auxiliary third and double main MOSFET to double the voltage gain while

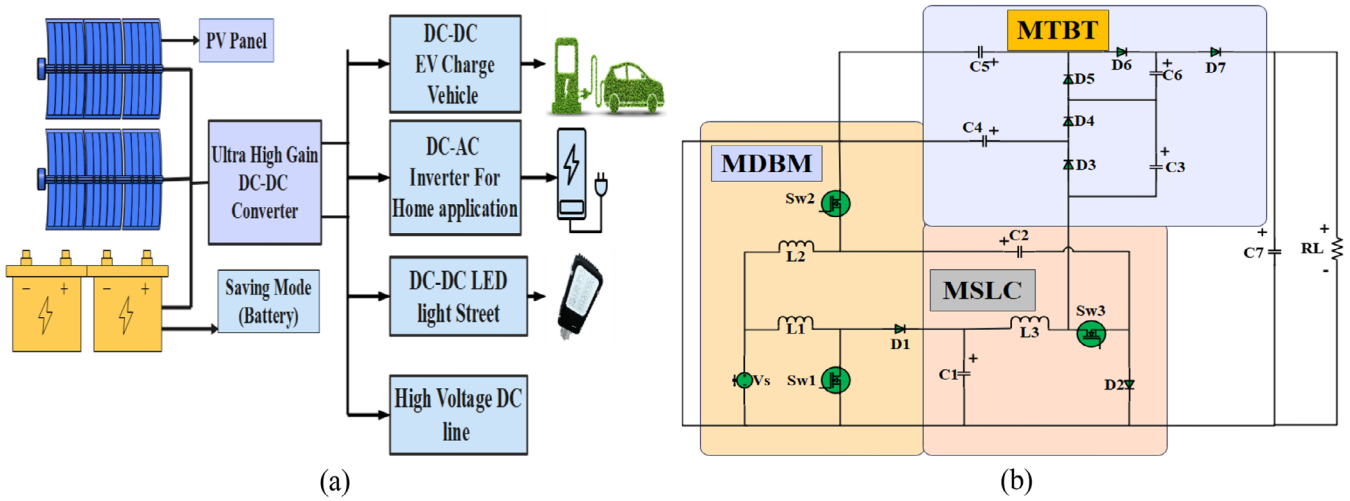


FIGURE 1 (a) The proposed converter, integrated with solar panels (PV) and a battery, is designed for 'Saving Mode' usage, enabling it to supply a wide range of applications. (b) The proposed converter circuit diagram.

concurrently mitigating voltage stress on the auxiliary MOSFET and diodes in the proposed converter. Additionally, all diodes in the MTBT operate under ZCS and the double main and auxiliary third MOSFET face very low current stress at ultra-high voltage gain when the proposed converter provides 600 V at 440 W. The input current of the proposed converter remains steady without pulsating at a low duty ratio, making the proposed converter more suitable for PV applications. The proposed converter demonstrates remarkably high efficiency at elevated power levels, achieving 96.1% efficiency at 440 W by utilizing SiC MOSFETs and diodes at a high switching frequency. Additionally, when supplying 600 V, the voltage stress on both the main and third MOSFETs is significantly reduced, leading to substantially lower switching losses. Furthermore, all power switches experience low current stress even at these high-power levels. Moreover, this reduction in current stress across all power switches and diodes leads to a significant decrease in conduction loss. Cumulatively, these reductions enable the proposed converter to operate with enhanced efficiency and performance. The proposed converter is capable of stepping up very low input voltages to high output voltages, which could result in a reduced number of photovoltaic (PV) panels, thereby saving space and cost.

2 | THE PRINCIPAL OPERATION AND STRUCTURE OF THE PC

In Figure 1a, the integration of the photovoltaic converter (PC) with solar panels is demonstrated, highlighting its potential for use in energy saving mode. Moreover, the proposed converter, featuring a wide range of output voltages, is suitable for various applications, such as electric vehicle charging (EV), electric home appliances, high-voltage DC lines, and LED lighting systems. In Figure 1b, the presentation of the proposed converter circuit diagram is made, featuring three small values primary inductors, seven capacitors, and three power switches (with Sw_1 as the first main switch, Sw_2 as the second main switch, and Sw_3 as the axillary third switch), along with seven diodes. Several notable advantages are designed to be provided by this circuit. One of the key advantages of this converter is the elimination of the need for isolated coupled inductors and transformers, which are typically essential for voltage step-up. Additionally, a SiC MOSFET with low on-state resistance is employed in the proposed converter to achieve ultra-high voltage gain while minimizing conduction and switching losses. Utilizing SiC MOSFETs and diodes at a high switching frequency aims to achieve high efficiency and elevated power density with reduced switching losses. The efficiency of the proposed converter can be significantly enhanced by operating at a high switching frequency, which leads to a reduction in the values of inductors and capacitors. The implementation of the proposed converter structure is intended to be easy and all switches turn on and off simultaneously. The reliability of this design is greatly improved, especially in photovoltaic applications, by the feature of the input current (I_i) at very low duty cycles having zero pulsation. Furthermore, concerns about voltage across on both the double primary and third switches and all diodes are addressed in the system. In addition, low voltage stress is faced by the inductors at high voltage gain. Also, the current stress through both the double main and third auxiliary switches is intended to be reduced when the system supplies 440 W at 600 V output voltage, with V_s equal to 30 V. In comparison to earlier DC–DC converters, a superior voltage gain is aimed to be achieved by the proposed converter while utilizing a minimal number of capacitors and inductors. The control mechanism is intended to be streamlined by the synchronous turning on and off of three power devices, contributing to the overall efficiency and effectiveness of the suggested converter. Additionally, the gate control circuit is simple and small in size.

2.1 | Operation of the PC

Two modes of operation are employed by the PC: discontinues conduction mode (DCM) (low duty cycle, below 57%) for light load application, and continues conduction mode (CCM) (higher duty cycle, above 57%) for higher load situations (as depicted in Figure 4).

2.2 | Operation of the PC at DCM

In DCM, a CCM is maintained by the input current without pulsations, while L_3 operates in DCM when the proposed converter supply 600 V output voltage at 440 W. The six operation modes for this scenario are visually delineated in Figure 3a, and the corresponding current waveforms of the converter in DCM are presented.

Mode 1: [0 to *t*0]. Three MOSFETs, Sw_1, Sw_2, and Sw_3, are in the on state. All diodes are in the off state, as illustrated in Figure 3a. During this phase, L_1 and L_2 begin to charge energy from the input source (Vs). Simultaneously, L_3 starts accumulating energy from C_1, which is in series with it. C_2 discharges current through Sw_2, and this current flows from both L_2 and C_2 during this mode.

D_4 and D_6 operates at ZCS at period, m. C_7 discharges its energy to supply current to the load. The converter for this mode is shown in Figure 2a. The equations during Mode 1 are as follows:

$$\left.\begin{aligned} VL_1 &= Vs \\ VL_2 &= Vs \\ VL_3 &= Vc_1 + Vc_2 \\ VL_2 &= Vc_1 + Vc_3 - Vc_4 \\ Vc_7 &= V_o \end{aligned}\right\} \tag{1}$$

$$\left.\begin{aligned} Ii &= iL_1 + iL_2 \\ I_{SW1} &= iL_1 \\ I_{SW2} &= iL_2 - Ic_2 \\ Isw_3 &= Ic_1 = iL_3 \\ iL_3 &= Ic_1 \\ Io &= Ic_7 \end{aligned}\right\} \tag{2}$$

where Vs is the input voltage, VL is the inductor voltage, Vc is the capacitor voltage, V_o is the output voltage, Ii is the input current, iL is the current through the inductor, I_{sw} is the current through the power MOSFETs, Io is the output current, and Ic is the current through the capacitor.

Mode 2: [*t*0–*t*1]. Three MOSFETs, Sw_1, Sw_2, and Sw_3, are still in the on state. D_1, D_2, D_3, D_5, and D_7 are in the off state, as illustrated in Figure 3a. While D_4 and D_6 are in the on state after a period m, both of them operate at ZCS. During this phase, L_1 and L_2 still charge energy from Vs and, L_3 starts accumulating energy from C_1. Still, C_7 discharges its energy to supply current to the load. The current through Sw_3 will come from L_3 and be subtracted from C_3, which means the current through Sw_3 is reduced during this mode. In addition, the current through Sw_2 is reduced after the current reduction in Sw_3. Moreover, the current through D_4 is the same as the current through C_4, and the current through D_6 is the same as the current through C_5. The PC for this mode is shown in Figure 2b. After the reduction in the C_2 current, this approach is designed to reduce current stress on both Sw_3 and Sw_2, resulting in the PC operating at high performance. Additionally, conduction loss is significantly reduced during this mode. In addition, current stress reduction would let the PC provide ultra-high voltage gain with a small volume of the heat sink in the PC. That means the size of the PC is significantly reduced. The current equations for components during Mode 2 are as follows: Where, the D_4 and D_6 operate at ZCS during time m, where, the value of m can be found in Equation (5).

$$\left.\begin{aligned} Ic_5 = Id_6 &= Ic_6 \\ Ic_4 &= Id_4 \\ -Ic_3 &= Ic_6 - Ic_4 \end{aligned}\right\} from \quad (0 < t < m) \tag{3}$$

$$\left.\begin{aligned} Isw_3 = iL_3 &= Ic_1 - Ic_3 \\ Isw_2 &= iL_2 - Ic_2 \end{aligned}\right\} \tag{4}$$

$$Where, m = \frac{DTs}{0.69\sqrt{\left(\frac{1}{(C_1+C_2)}\right)(L_2+L_3)}} \tag{5}$$

Mode 3: [*t*1–*t*2]. Three MOSFETs, Sw_1, Sw_2, and Sw_3, are turned off, and diodes D_1, D_2, and D_7 are turned on, while D_3, D_4, D_5, and D_6 are in the off state. During this phase, L_1 begins to release energy to charge C_1 through D_1 and to supply current to the load by adding the current of L_3, as shown in the circuit diagram of the converter in Figure 2c. L_2 starts to release energy to charge C_2 through D_2. Additionally, L_3 supplies current to the load with the added current from L_1. This means that D_3 and D_5 are in the "off" state and both will operate under ZCS at **h/2**. The equations during Mode 3 are as follows:

$$\left.\begin{aligned} VL_1 &= Vc_1 - Vs \\ VL_2 &= Vc_2 - Vs \\ VL_3 &= Vc_1 - Vc_4 \\ Vc_5 &= Vc_4 + Vc_3 \\ Vc_7 = V_o &= Vc_5 + Vc_6 \end{aligned}\right\} \tag{6}$$

$$\left.\begin{aligned} Ii &= iL_1 + iL_2 \\ iL_1 &= Ic_1 + iL_3 \\ iL_2 &= Ic_2 = Id_2 \\ iL_3 &= Ic_3 = Ic_6 \\ Ic_6 &= Id_7 \\ Ic_6 &= Ic_7 + Io \end{aligned}\right\} \tag{7}$$

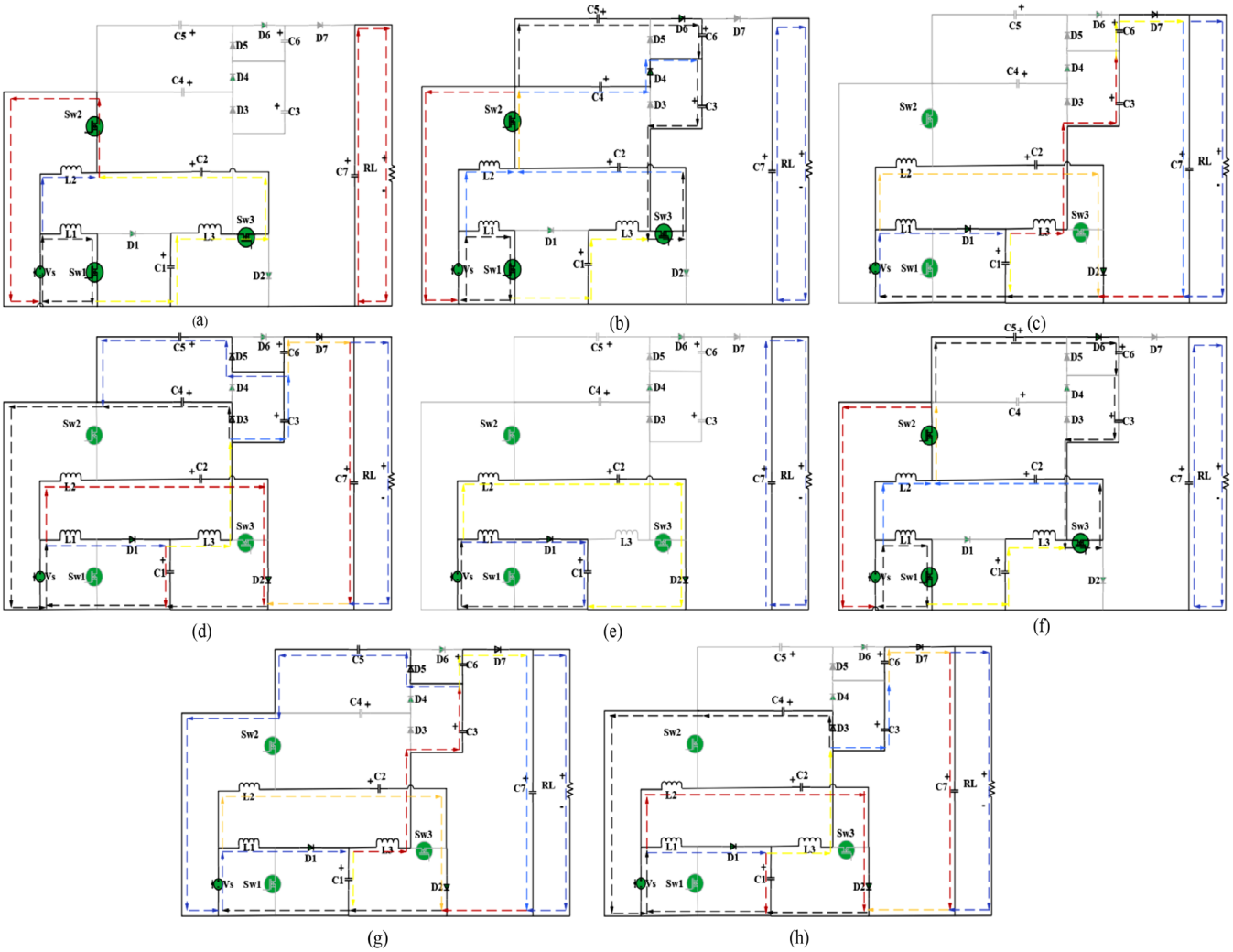


FIGURE 2 (a) Mode (1) DCM; (b)Mode (2) DCM, Mode (2) CCM; (c) Mode (3) DCM, Mode (5) DCM; (d) Mode (4) DCM, Mode (4)CCM; (e) Mode (6) DCM; (f) Mode (1) CCM; (g) Mode (3) CCM; (h) Mode (5) CCM.

Mode 4: [*t*2–*t*3]. Three MOSFETs, Sw_1, Sw_2, and Sw_3, are still turned off, and diodes D_1, D_2, and D_7 are still turned on, while D_4 and D_6 are in the off state. D_3 and D_5 are in the on state during this phase after time **h/2**. L_1 continues to discharge energy to charge C_1 through D_1 and to supply current to the load by adding the current of L_3, as shown in the circuit diagram of the converter in Figure 2d. L_2 starts to discharge energy to charge C_2 through D_2. Additionally, L_3 supplies current to charge C_3 and C_4, and, the current through C_3 charges C_5 through D_5 and charges C_6. In addition, the C_6 current charges C_7 and supplies load current. This means that D_3 and D_5 are in the "off" state, and both will operate under ZCS at **h/2**, where h can be found in Equation (9). The current equations during Mode 4 are as follows:

$$\left.\begin{aligned} iL_3 &= -Ic_3 + Ic_4 \\ -Ic_3 &= -Ic_6 + Ic_5 \\ Id_5 &= Ic_5 \\ Id_3 &= Ic_4 \end{aligned}\right\} from \quad \left(\frac{h}{2} < t < \left(1 - D - \frac{h}{2}\right)\right) \tag{8}$$

$$Where, h = \frac{(1-D)Ts}{0.69\sqrt{((\frac{1}{(C_3+C_6)} + C_7) + (C_4))L_3}} \tag{9}$$

Mode 5: [*t*3–*t*4]. Three MOSFETs, Sw_1, Sw_2, and Sw_3, are still turned off, and diodes D_1, D_2, and D_7 are turned on, while D_3, D_4, D_5, and D_6 are in the off state. L_1 continues to discharge energy to charge C_1 through D_1 and to supply current to the load by adding the current of L_3, as shown in the circuit diagram of the PC in Figure 2c. L_2 continues to discharge energy to charge C_2 through D_2. Additionally, L_3 supplies current to the load with current from L_1. This means that D_3 and D_5 are in the "off" state, and both will operate under ZCS at time (**h/2**). The equations during Mode 5 are the same as those in Mode 3.

Mode 6: [*t*4-*t*5]. Three MOSFETs, Sw_1, Sw_2, and Sw_3, are still turned off, and diodes D_1 and D_2 are still turned on, while D_3, D_4, D_5, and D_6 are still in the off-state and, D_7 is changed to the off-state during this mode. L_1 continues to discharge energy to charge C_1 through D_1, and L_2 continues to discharge energy

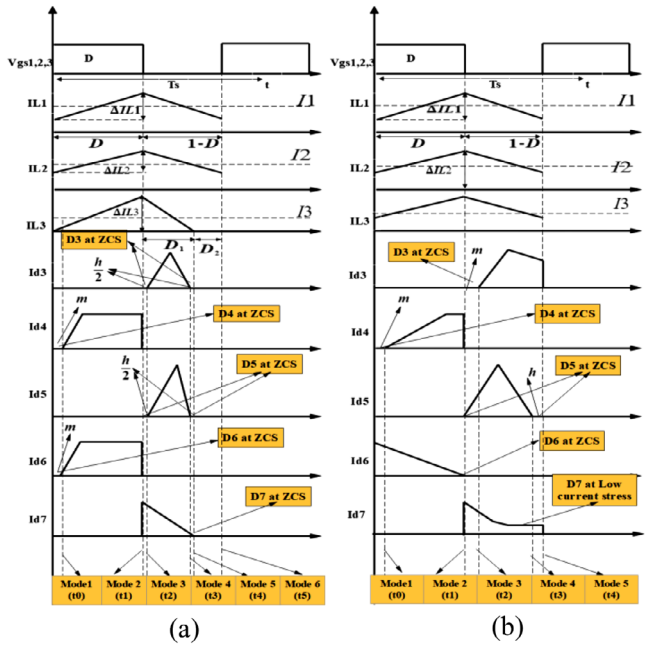


FIGURE 3 Waveform of the PC (a) in DCM, (b) in CCM.

to charge C_2 through D_2, while L_3 has zero charges at D_2. Additionally, C_7 supplies current to the load. The configuration of the PC in this mode is displayed in Figure 2e. Notably, the equations are the same as in the previous mode.

$$iL_1 = Ic_1 = Id_1 \tag{10}$$

As a result, when the proposed converter operates in DCM, it supplies a high load voltage of 600 V at 440 W. In this mode, all the MTBT diodes operate at ZCS, reducing the current stress across them and minimizing conduction loss due to diode internal resistance. Additionally, the current stress across Sw_1, Sw_2, and Sw_3 is markedly reduced when the PC achieves ultra-high voltage gain. Moreover, the voltage stress across all power diodes and power switches is significantly reduced at V_o = 600 V and high load power. This implies that the PC, utilizing SiC MOSFETs and diodes, can operate with very high efficiency and performance. Furthermore, the input current of the system does not pulsate at low-duty cycles, making the PC more suitable for PV applications.

2.3 | The PC operation in CCM

When the load current increases, the PC operates in CCM, as illustrated in Figure 3b. In CCM, both the input current and the L_3 inductor current adhere to the CCM pattern. This dynamic response results in a significant boost in the voltage gain ratio of the PC. Figure 3b provides a representation of the five operational modes and a visual representation of the current waveforms of the PC during CCM.

Mode 1: [0 to *t*0]. Three MOSFETs, Sw_1, Sw_2, and Sw_3, are in the on state. Diodes D_1, D_2, D_3, D_4, D_5, and D_7 are in the off state, as illustrated in Figure 3a. While only D_6 is in on state. During this phase, L_1 and L_2 begin to charge energy from the Vs and, L_3 starts accumulating energy from C_1. C_2 discharges current through Sw_2 and this current flows from both L_2 and C_2 during this mode. D_4 operates at ZCS during this time m where the period of m can be found in Equation (5). C_7 discharges its energy to supply current to the load. The PC for this mode is shown in Figure 2f. The equations during Mode 1 are as follows:

Mode 2: [*t*0–*t*1]. This mode is similar to Mode 2 in DCM

$$\left.\begin{aligned} Isw_3 &= -Ic_3 + iL_3 \\ Ic_3 &= Ic_6 = Ic_5 \\ Id_5 &= Ic_5 \end{aligned}\right\} from(0 < t < m) \tag{11}$$

Mode 3: [*t*1–*t*2]. Three MOSFETs, Sw_1, Sw_2, and Sw_3, turned off, and diodes D_1, D_2, and D_7 are turned on, while D_4 and D_6 are in the off state. D_5 is in the on state during this mode. L_1 continues to discharge energy to charge C_1 through D_1 and to supply current to the load by adding the current of L_3, as shown in the circuit diagram of the PC in Figure 2g. L_2 starts to discharge energy to charge C_2 through D_2. Additionally, L_3 supplies current to charge C_3, C_5 and C_6. The current through C_3 charges C_5 through D_5 and charges C_6. In addition, the C_6 current charges C_7 and supplies load current. This means that D_3 is in the "off" state, and will operate under ZCS at time m. The current equations during Mode 3 are as follows:

$$\left.\begin{aligned} iL_3 &= Ic_3 = Ic_5 + Ic_6 \\ Id_5 &= Ic_5 \end{aligned}\right\} \tag{12}$$

Mode 4: [*t*2–*t*3]: this mode is similar to Mode 4 in DCM

Mode 5: [*t*3–*t*4]: During this mode, Sw_1, Sw_2, and Sw_3, are turned off, and diodes D_1, D_2, D_3, and D_7 are turned on, while D_4 and D_6 are in the off state. In this phase, L_1 continues to release energy to charge C_1 through D_1 and to provide current to the load by combining with the current from L_3, as depicted in the circuit diagram of the PC in Figure 2h. Simultaneously, L_2 begins to release energy to charge C_2 through D_2. Additionally, L_3 contributes current to charge C_3, C_4, and C_6. The current flowing through C_3 charges C_4 through D_3 and charges C_6. Furthermore, the C_6 current charges C_7 and supplies the load current. It is important to note that D_5 is in the "off" state during this period, and D_5 operate under ZCS at time, ***h***. The current equations during Mode 5 are as follows:

$$\left.\begin{aligned} iL_3 &= Ic_3 + Ic_4 \\ Ic_3 &= Ic_6 = Id_7 \end{aligned}\right\} \tag{13}$$

3 | VOLTAGE GAIN AT CCM

In CCM, the PC is operated when a high load current is supplied. Therefore, the voltage gain of the PC is derived at CCM, as illustrated in the equations below.

$$\frac{1}{Ts}\left(\int_0^{DTs}(2Vs+Vc_1+Vc_2)dt+\int_D^{Ts}(Vc_1-Vs)dt\right.$$
$$\left.+\int_D^{Ts}(Vc_2-Vs)dt\int_D^{Ts}(Vc_1-Vc_4)dt=0\right\} \quad (14)$$

$$\frac{1}{Ts}\left(\int_0^{DTs}(Vc_1+Vc_2)dt+\int_D^{Ts}(Vc_1-Vc_4)dt=0\right. \quad (15)$$

$$\frac{1}{Ts}\left(\int_0^{DTs}(Vc_1+Vc_3-Vc_4)dt+\int_D^{Ts}(Vc_1-Vc_4)dt=0\right. \quad (16)$$

Applying the volt-second balance to L_1, L_2, and L_3 using Equations (1) and (6) results in Equation (14). Deriving Equation (15) involves applying a volt-second balance specifically to L_3 to determine Vc_4. Subsequently, Equation (20) are obtained. Furthermore, determining Vc_3 is the outcome of applying volt-second balance to L_3, leading to the formulation of Equation (16). Applying volt-second balance individually to L_1 and L_2, utilizing Equations (1) and (6), gives rise to Equations (17) and (18) in the quest to determine Vc_1 and Vc_2, respectively.

$$Vc_1=\frac{Vs}{(1-D)} \quad (17)$$

$$Vc_2=\frac{Vs}{(1-D)} \quad (18)$$

$$Vc_3=\frac{2Vs}{(1-D)^2} \quad (19)$$

$$Vc_4=\frac{Vs(D+1)}{(1-D)^2} \quad (20)$$

Equation (23) represents the output voltage of the PC, equating to the sum of Equations (21) and (22). Describing the Mdc voltage gain equation of the PC in CCM, Equation (24) is presented. It is worth highlighting that the PC demonstrates a superior voltage gain compared to its predecessors.

$$Vc_5=\frac{2Vs(D+1)}{(1-D)^2} \quad (21)$$

$$Vc_6=\frac{2Vs}{(1-D)^2} \quad (22)$$

$$V_o=Vc_5+Vc_6 \quad (23)$$

$$Mdc(CCM)=\frac{V_o}{Vs}=\frac{(4+2D)}{(1-D)^2} \quad (24)$$

4 | VOLTAGE GAIN AT DCM

By applying the volt-second balance principle to inductors L_1, L_2, and L_3, Equation (25) is derived from Equations (1) and (6), resulting in insightful equations in (26) upon solving. Significantly, the discharging time of L_3 is represented by D_1 in Equation (26), and Equation (28) offer clarity on the average inductor current within L_3. Furthermore, Equation (29) articulates the output current as an average value, while Equation (27) defines the peak current of inductor L_3 during DCM.

$$\frac{1}{Ts}\left(\int_0^{DTs}(2Vs-Vc_2-Vc_1)dt+\int_D^{Ts}(Vc_2-Vs)dt+\right.$$
$$\left.\int_D^{Ts}(Vc_1-Vs)dt+\int_D^{D1Ts}(Vc_1+Vc_3-V_o)dt=0\right\} \quad (25)$$

$$D1=\frac{2Vs(2+D)}{Vo(1-D)} \quad (26)$$

$$iL_{3peak}=\frac{2VsD}{fsL_3(1-D)} \quad (27)$$

$$<I_3>=\frac{VsD(D+D1)}{fsL_3(1-D)} \quad (28)$$

$$I_o=\frac{(Vc_1+Vc_2)DD1}{2fsL_3} \quad (29)$$

Remarkably, the correlation between V_o and V_s in the DCM operation of the PC is established by Equation (30). The voltage gain, as revealed by Equation (30), is contingent on crucial factors—such as the duty cycle (D), load resistor (RL), and switching frequency (Fs). Furthermore, Equation (30) expresses the PC voltage gain as a function of (K), representing the loadless factor and shedding light on its behaviour. To identify the pivotal value of K (Kcrit), Equation (32) is derived by utilizing Equation (31). Equation (33) precisely defines the boundary condition that differentiates between the CCM and DCM operation modes, as explicitly stated in the same Equation (33).

$$Mdc(DCM)=\frac{VsDRL(4+2D)}{fsL_3V_o(1-D)^2} \quad (30)$$

$$Mdc\,(DCM)=\frac{1}{(1-D)}\sqrt{\frac{2D(4+2D)}{K}},\ Where\ \mathrm{K}=\frac{2L_3}{RLTs} \quad (31)$$

$$k_{crit}=\frac{D(1-D)^2}{(2+D)} \quad (32)$$

$$k_{crit}=\begin{cases} if\ \mathrm{Kcrit}>\mathrm{K\ The\ (PC)\ operatein\ DCM} \\ if\ \mathrm{Kcrit}<\mathrm{K\ The\ (PC)\ operatein\ CCM} \end{cases} \quad (33)$$

Figure 4 illustrates the dynamic performance of the proposed converter in both CCM and DCM. It is evident that, based on the condition outlined in Equation (33), when the duty cycle is below 0.57, the proposed converter operates in DCM. On the flip side, as the load current rises and the duty cycle surpasses 57%, the proposed converter transitions into CCM.

5 | VOLTAGE STRESS ANALYSIS

Analysing the evaluation of voltage stresses across the MOSFETs, diodes, and capacitors is crucial. By referring

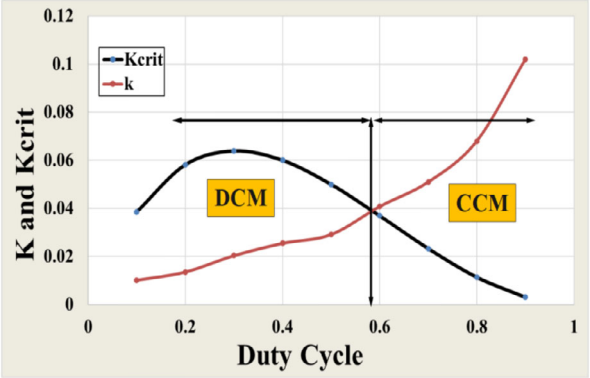


FIGURE 4 Dynamic performance of the PC Kcrit and K versus D.

to Equations (34), the voltage across D_1 and D_2 can be determined, remaining relatively small depending on Vs. Equations (35) and (36) offer insights into the voltage levels across D_3, D_4, D_5, D_6, and D_7. Notably, the voltage across the diodes mentioned in Equations (35) to (36) consistently remains lower than half of Vo.

$$VD_1 = \frac{Vs}{(1-D)} = VD_2 \tag{34}$$

$$VD_3 = \frac{2Vs}{(1-D)^2} = VD_4 \tag{35}$$

$$VD_5 = \frac{2Vs}{(1-D)^2} = VD_6 = VD_7 \tag{36}$$

Equations (37) and (38) are utilized to calculate the voltage across MOSFETs, yielding values that are notably small. Specifically, the voltage across Sw_1 equals Vc_1, and the voltage across Sw_2 equals Vc_2. Additionally, the voltage across Sw_3, as expressed in Equation (39), is equal to Vc_4, which is relatively lower than half of V_o. Consequently, as the PC generates a high V_o which is equal to 600 V while, the voltage across the power MOSFETs significantly decreases. That means the switching losses of these power switches are significantly reduced when the PC supplies a high load voltage of about 600 V.

$$Vsw_1 = \frac{Vs}{(1-D)} \tag{37}$$

$$Vsw_2 = \frac{Vs}{(1-D)} \tag{38}$$

$$Vsw_3 = \frac{Vs(D+1)}{(1-D)^2} \tag{39}$$

Equations (40) and (41) illustrate the voltage across C_1 and C_2. Equations (42) and (43) provide details on the voltage across C_3, C_4, and C_6. Equation (44) pertains to the voltage across C_5. Equation (45) reveals the voltage across C_7, which equals V_o. Notably, the voltage stress on the MOSFETs and power diodes significantly decreases when the PC handles a 440 W load, with L_3 operating in DCM and L_1 and L_2 in CCM at a 600 V output voltage at Vs is 31 V.

TABLE 1 Prototype components design of the PC.

SiC MOSFETs (Sw_1 and Sw_2) (SiC, Silicon carbide) SiC MOSFETs (Sw_3)	**650 V, 40 A(TW048N65C) R_{on} = 40 mΩ 1200 V, 30 A(SCTW40N120G2VAG), 40 mΩ**
SiC Schottcky diodes	1200 V, 30 A(IDW15G120C5B),
$L_1 = L_2$	10 μH, 2.9 mΩ
L_3	68 μH, 1.9 mΩ
$C_1 = C_2$	100 μF, 100 V, rc = 0.035 Ω
$C_3 = C_4 = C_5 = C_6$	100 μF, 500 V, rc = 0.05 Ω
C_7	74 μF, 900 V, rc = 0.025 Ω
$V_{o\ (Output\ Voltage)}$	600 V
Vs (Input Voltage)	30–40 V
Fs (Switching frequency)	150 KHz
D duty cycle	48% at 600 V output voltage
Output Power	440 W
Ic drive circuit	1EDI60N12AF 600 V output side
Inductors size	(*L*/2.85 cm**W*/2.75 cm**H*/2.35 cm)
The proposed converter size	*L* = 12.3 cm, *H* = 4.2 cm, *W* = 9.3 cm

$$Vc_1 = \frac{Vs}{(1-D)} \tag{40}$$

$$Vc_2 = \frac{Vs}{(1-D)} \tag{41}$$

$$Vc_3 = \frac{2Vs}{(1-D)^2} = Vc_6 \tag{42}$$

$$Vc_4 = \frac{Vs(D+1)}{(1-D)^2} \tag{43}$$

$$Vc_5 = \frac{2Vs(D+1)}{(1-D)^2} \tag{44}$$

$$Vc_7 = V_o \tag{45}$$

6 | COMPONENTS DESIGN OF THE PC

The essential components of the 440 W prototype for the PC include capacitors, inductors, MOSFETs, and power diodes. Achieving a high voltage gain requires careful design of these components. The PC comprises three inductors with small values and seven capacitors with small values, as outlined in Table 1, providing clarity on the prototype design parameters.

$$L_1 = \frac{VsDTs}{\Delta iL_1} = L_2 \tag{46}$$

$$L_3 = \frac{2VsDTs}{(1-D)\Delta iL_3} \tag{47}$$

$$C_1 = \frac{V_o(2+D)}{\Delta vc_1 R_L fs(1-D)} \tag{48}$$

$$C_2 = \frac{V_o(2+D)}{\Delta vc_2 R_L fs(1-D)} \tag{49}$$

$$C_3 = \frac{V_o(2+D)}{\Delta vc_3 R_L fs(1-D)} = C_6 \tag{50}$$

$$C_5 = \frac{V_o(2+D)D}{\Delta vc_5 R_L fs(1-D)^2} = C_4 \tag{51}$$

$$C_7 = \frac{V_o D}{\Delta V_o FsRL} \tag{52}$$

Table 1 emphasizes a significant decrease in inductor values as switching frequencies rise. Furthermore, the low internal resistance of these inductors contributes to minimized power losses in the proposed converter. In designing the inductors for the 440 W converter, L_1 and L_2 can be crafted using Equation (46), and the value of L_3 can be ascertained through Equation (47). The determination of capacitor values can be accomplished using Equations (48) to (52).

Remarkably, Table 1 underscores that employing ferrite cores with flat wire inductors measuring (2.85 cm x 2.75 cm x 2.35 cm) at an exceptionally high switching frequency results in remarkably low internal resistance for the inductors. In addition, a SiC MOSFET with low on-state resistance is employed in the proposed converter to validate ultra-high voltage gain while minimizing conduction and switching losses. Using SiC MOSFETs at a high switching frequency aims to achieve high efficiency at elevated power density with reduced switching losses [35].

The proposed converter is designed at a high switching frequency. If Si MOSFETs are used, power dissipation would be excessively high, necessitating the use of a large heat sink. Furthermore, the efficiency and performance of the proposed converter's output voltage would decrease when Si MOSFETs are employed at high switching frequencies [4, 5, 9–24, 31–36]. Moreover, designing the proposed converter at a low switching frequency would result in significantly higher values for inductors and capacitors. This means that the internal resistance of L and C would be high, significantly affecting the performance of the proposed converter, and leading to a significantly larger converter size. In addition, SiC Schottky diodes with zero reverse recovery current and no forward recovery, make the system operate with high efficiency and performance.

7 | THE PC AND ITS CONTROL STRATEGY

A pair of Proportional Integral (PI) controllers for the proposed converter, depicted in Figure 5a, is employed to ensure optimal performance. The stable load current is ensured by the first PI controller, which functions as an internal controller. At the same time, the desired output voltage is supervised by the second PI controller, serving as an outer controller. The error, $E(t)$, resulting from subtracting the actual output voltage from the target voltage, is utilized as input for the first PI voltage controller. The reference current for the load is determined by the computation performed by the PI voltage controller's output. Deliberate restrictions are imposed on this reference current to prevent excessive current draw. The feedback current is subtracted from the limited reference current, forming the input for the PI current controller governed by Equation (53), where the output of the PWM generator serves as the input to the IC drive of the PC. The schematic of the gate drive circuit of the PC is illustrated in Figure 5b. To implement the control strategy, an Arduino UNO is utilized as the controller for the proposed converter. The controller's design employs trial-and-error tuning to ensure optimal output voltage results. In terms of utilizing a dual PI controller, the inner loop, which is the current controller, has KP and KI parameters that are slower compared to the KP and KI of the PI voltage controller. Consequently, the KP and KI parameters for the PI voltage controller are ten times faster than those for the PI current controller. This is demonstrated where $Gci(s)$ represents the current PI controller and $Gcv(s)$ denotes the voltage PI controller, as shown in Equation (54).

$$U(t) = Kpe(t) + Ki\int e(t) \tag{53}$$

$$\left.\begin{aligned} Gci(s) &= \frac{0.03s+5}{s} \\ Gcv(s) &= \frac{0.5s+70}{s} \end{aligned}\right\} \tag{54}$$

8 | PERFORMANCE COMPARISON OF THE PC WITH PREVIOUS HIGH-GAIN CONVERTERS

A comparison has been conducted between the proposed converter and its predecessors among DC–DC converters. Previous high-gain converters underwent simulation in PLECS and MATLAB software under identical conditions. Additionally, simulations of the converters presented in Figure 6 were conducted in both DCM and CCM to verify the voltage and current stresses across power devices under different conditions. In Figure 6a, it becomes apparent that the proposed achieves superior voltage gain compared to prior boosting converters. This heightened gain at a low-duty cycle signifies a reduction in conduction and switching losses, leading to enhanced efficiency. From Figure 6a, it can be seen that the proposed converter can provide high output voltage by stepping up low input voltage, which is equal to 31 V. This means (Mdc is 20). Moreover, the proposed converter can provide a higher voltage gain when the duty cycle is about 0.3, as shown in Figure 6a. Moving to Figure 6b, it is evident that the power switch devices in the proposed converter experience lower voltage stress compared to those in the aforementioned converters. In addition, low voltage stress across power switches means low switching losses, which will lead to an increase in the efficiency of the proposed converter.

In Figure 6c, it is evident that the voltage stress on the diode in the PC is lower than in previous converter designs. The voltage across all diodes in the proposed converter has low voltage stress when the proposed system supplies V_o = 600 V. This means low voltage stress on power diodes, which will result in

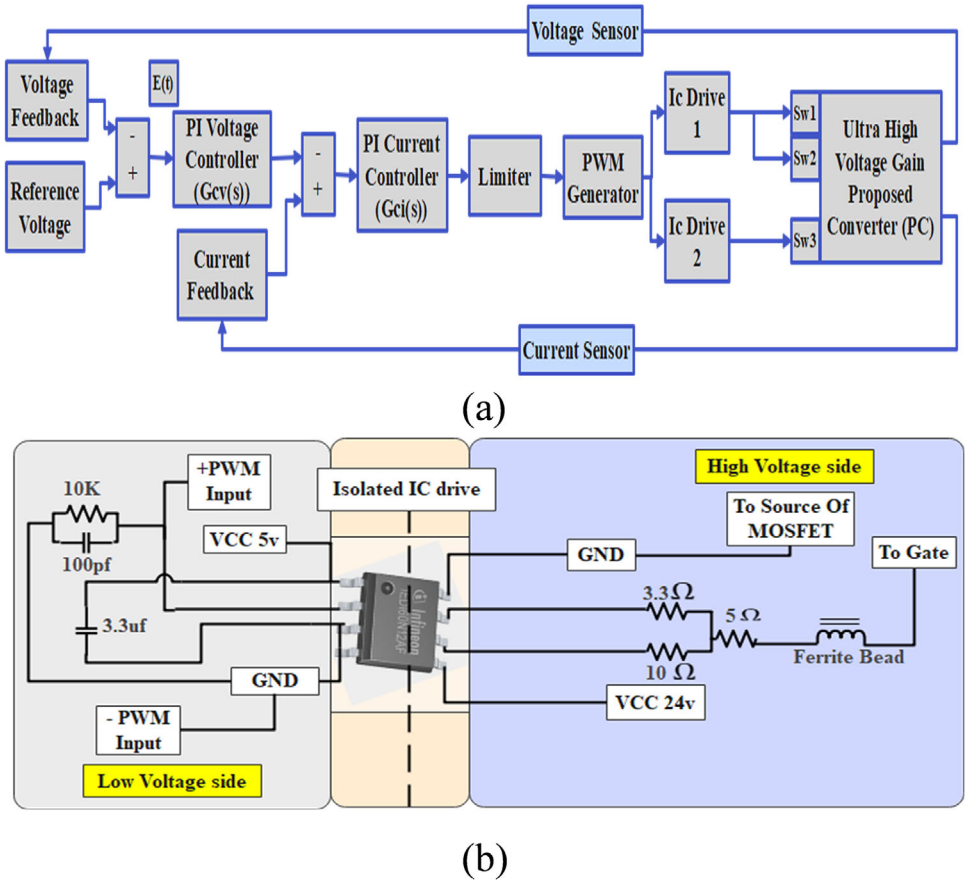


FIGURE 5 (a) Control strategy of the proposed converter. (b) Schematic of the gate drive circuit of the PC.

a reduction in the use of heat sinks and a decrease in the size of the proposed converter. In Figure 6d, it can be seen that the stress current through the MOSFETs in the PC is lower than the current stress experienced by the power switches in previous boosting converters. Additionally, when the system operates at a voltage transfer gain of 20 and supplies 440 W, the normalized current stress through the switch to load current is measured at 4.3, as depicted in Figure 6d. Additionally, from Figure 11c,d, it can be seen that the current stress across Sw_1 is 8 A, Sw_2 is 11.5 A, and Sw_3 is 8 A when the PC supplies power at 440 W at V_o = 600 V. This means the stress current through double main and auxiliary third switches is significantly reduced at V_o = 600 V and is lower than power switches in previous DC–DC converters.

In Figure 7a, it is observed that the PC achieves a higher gain than the previous converter, with a reduced number of power switches. Additionally, all power switches in the PC turn on and off simultaneously. In Figure 7b, the PC is demonstrated to have a higher gain compared to its predecessor, once again with fewer inductors. In Figure 7c, it is observed that the PC achieves a higher gain than the previous converter, with a lower count of power diodes. In Figure 7d, it is observed that the PC achieves a higher gain than the previous converter, with a lower count of total elements. Furthermore, it can be seen that the PC can attain higher efficiency than previous DC–DC converters, with all power diodes operating at ZCS. The current stress on all power switches is significantly reduced at Vo = 600 V and 440 W. Additionally, all power switches turn on and off simultaneously without any complexity in the circuit of the control signal. Moreover, the three power switches are SiC MOSFETs with low on-state resistance at high switching frequency. This implies that the PC voltage gain is higher than the previous converter, with low conduction and switching losses.

In Table 2, the PC operates at a higher switching frequency, allowing for smaller components and reduced parasitic resistance. This results in a compact, lightweight, and cost-effective system. Unlike previous converters, it excels in both size efficiency and cost-effectiveness. While earlier converters achieved high voltage gain through a high-duty cycle, the PC efficiently boosts low Vs to a variable V_o (335–600 V) with a low D. Additionally, it features fewer power diodes, all operating under ZCS, which reduces losses from forward voltage and internal resistance.

Concerning input current, the PC maintains stability with zero pulsation at both low and high duty cycles. Table 2 illustrates that the PC exhibits higher efficiency compared to previous converters. Furthermore, it boasts a higher power output than the previous work. In terms of gate control (refer to Figure 1b), all power MOSFETs switch on and off simultaneously with a simple gate control circuit. In contrast,

TABLE 2 Analysing the PC in comparison to previous high-boosting converters.

Items	PC	Ref. [2]	Ref. [3]	Ref. [25]	Ref. [29]	Ref. [37]	Ref. [30]	Ref. [5]	Ref. [13]	Ref. [16]	Ref. [18]	Ref. [20]	Ref. [23]	Ref. [31]	Ref. [32]	Ref. [33]	Ref. [36]	Ref. [7]
F_S (KHz)	150	30	20	50	20	20	30	24	20	100	1	100	31.3	50	50	50	50	50
Vs	30	25	20	20	15	48	29	20	24	300	24	15	20	25	48	21	48	11
V_o	600	110	160	200	183	178	325	172	350	800	221	384	200	200	408	400	650	192
NL	3	4	6	5	2	4	4	3	2	3	4	2	2	2	2	4	2	CI $n=1$
NC	7	6	1	8	4	3	6	3	4	7	2	4	5	5	2	3	5	5
ND	7	3	14	6	5	4	4	3	5	4	8	4	7	4	2	9	5	5
NSW	3	1	2	1	1	4	2	1	1	1	2	2	1	1	2	3	2	2
NT	20	14	23	20	12	15	16	10	12	15	16	12	15	12	8	19	14	CI+12
Duty cycle (%)	48	60	60	60	60	65	73	70	80	60	42	77	50	72	73	$D_1=50$, $D_2=30$	66	65
Power (W)	300	110	200	200	176	130	220	100	200	800	200	200	150	200	425	400	400	200
Input current pulsating	No	Yes	Yes	No	No	No	No	No	Yes	No	Yes	Yes	No	No	Yes	Yes	yes	No
Efficiency (%)	96.3	92	95.5	90	92	92.5	95.6	91.4	95	95	93	94.2	94.5	94.2	91.5	94	95	95.8
Mdc	$\frac{(4+2D)}{(1-D)^2}$	$\frac{3D}{(1-D)}$	$\frac{(1+7D)}{(1-D)}$	$\frac{1+3D-3D^2}{(1-D)^2}\frac{2}{(1-D)^2}$		$\frac{1}{(1-D)}$	$\frac{(1+3D)}{(1-D)}$	$\frac{D}{(1-D)^2}$	$\frac{4}{(1-D)}$	$\frac{(2+2D)}{(1-D)}$	$\frac{(1+18.25D)}{(1-0.25D)}$	$\frac{2}{(1-D)^2}$	$\frac{(3-D)}{(1-D)^2}$	$\frac{(2+D)}{(1-D)}$	$\frac{(3+D)}{(1-D)}$	$\frac{(3+D1+3D2)}{(1-D1-D2)}$	$\frac{(5-4D+D^2)}{(1-D)^2}$	$\frac{(3+n(1+D)}{(1-D)}$
Mdc at $D=0.55$	25.18	3.6	10.7	8.6	9.8	2.22	5.8	2.71	8.8	6.8	12.7	9.8	12	5.7	7.9	22	15.3	10.11

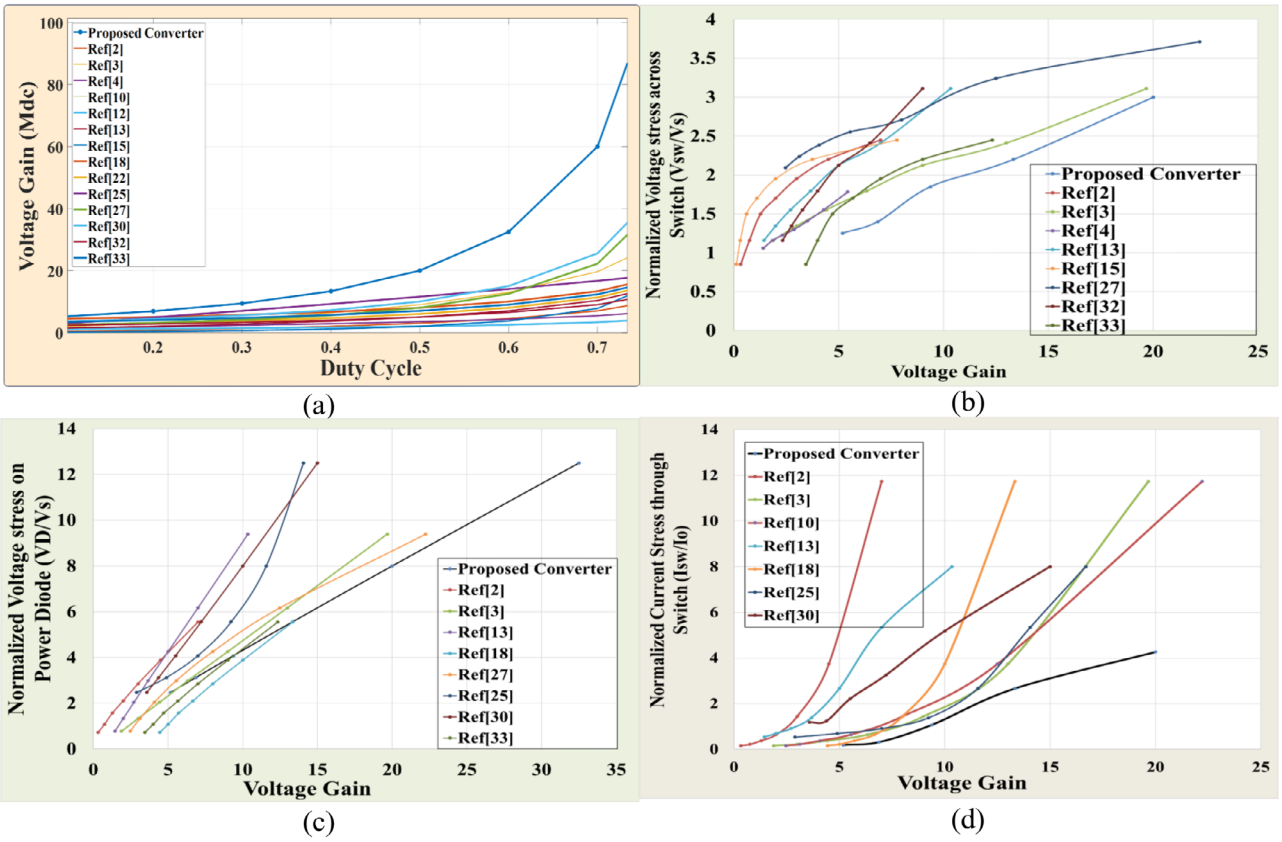


FIGURE 6 (a) Comparisons voltage gain (Mdc) versus duty ratio. (b) Vsw/Vs versus Mdc; (c) V_D/Vs versus Mdc; (d) Isw/Io versus Mdc.

the gate control circuit in ref. [33] is quite complex, involving two different duty cycles to achieve high voltage gain.

Examining the voltage gain equation, it is evident that the PC achieves a higher gain than previous converters at $D = 0.48$. This suggests that the PC is well-suited for RES requiring variable and fixed high-output voltages across a wider range of duty cycles, achieving an impressive 96.3% efficiency.

9 | EFFICIENCY CALCULATION OF THE PROPOSED CONVERTER

The Proposed converter is composed of seven capacitors, three inductors, seven diodes, and three power switches—indispensable elements that, despite their significance, are not immune to constraints. Internal resistance is inherent in these components, and the power diode contributes to two specific types of losses: forward voltage (Vf) and internal resistance. Furthermore, the MOSFET devices introduce switching and conduction losses. Hence, a thorough assessment of the PC should account for these various sources of losses.

To ascertain the current stress on power switches, Equations (55), (56) and (57) are employed to calculate the root mean square (rms) current flowing through Sw_1, Sw_2, and Sw_3, respectively

$$Isw_{1rms} = \frac{Io(2+D)\sqrt{D}}{(1-D)^2} \tag{55}$$

$$Isw_{2rms} = \frac{IoD(2+D)\sqrt{(2-D)}}{(1-D)^2} \tag{56}$$

$$Isw_{3rms} = \frac{Io(2+D)\sqrt{(D-m)(1-D^2)}}{(1-D)^2} \tag{57}$$

In the interim, Equations (58) to (63) come into play for determining the effective currents coursing through the power diodes. Notably, it is observable that the currents through D_3, D_4 and D_6 experience significant reductions when operating under ZCS, contingent on the value of m as determined by Equation (5). Moreover, the rms current through D_5 undergoes a reduction when operating under ZCS.

$$ID_{1rms} = ID_{2rms} = \frac{Io(2+D)}{\sqrt{(1-D)^3}} \tag{58}$$

$$ID_{3rms} = \frac{Io(2+D)\sqrt{(m-1)}}{2(1-D)} \tag{59}$$

$$ID_{4rms} = \frac{Io(2+D)\sqrt{(D-m)}}{2(1-D)^2} \tag{60}$$

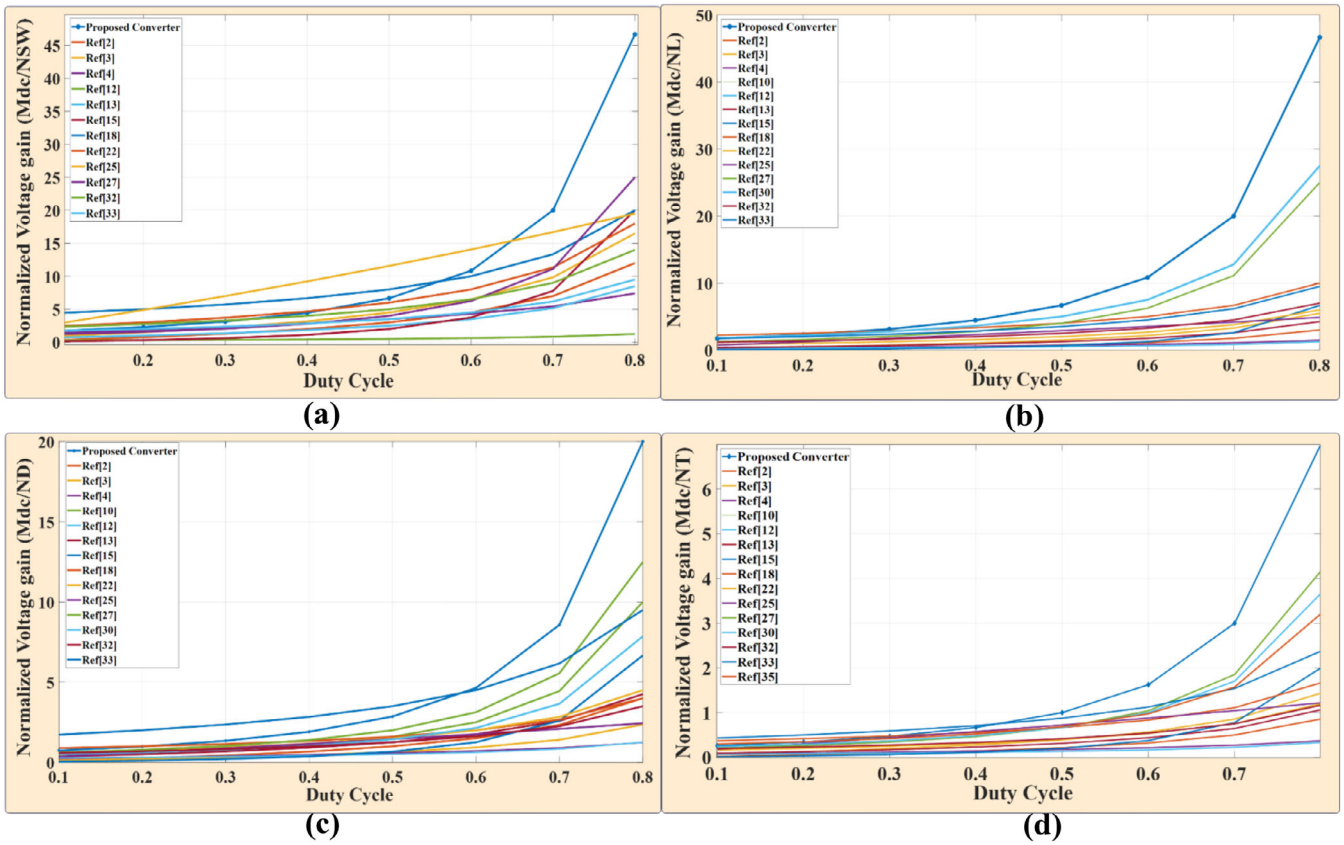


FIGURE 7 Normalized voltage gain (Mdc) (a) to number of switches NSW versus duty cycle (b) to number of inductors NL versus duty cycle (c) to number of diodes ND versus duty cycle,(d) to total number of elements NT versus duty cycle.

$$ID_{5rms} = \frac{Io(2+D)\sqrt{(1-2D-h)}}{2(1-D)} \tag{61}$$

$$ID_{6rms} = \frac{Io(2+D)\sqrt{(D-m)}}{2(1-D)^2} \tag{62}$$

$$ID_{7rms} = \frac{Io(2+D)}{2\sqrt{(1-D)}} \tag{63}$$

To calculate the rms input current, which is equal to the rms current through L_1 and L_2 refer to Equations (64). Equation (65) describes the effective current flowing through inductors L_3.

$$iL_1 rms = \frac{Io(2+D)}{(1-D)^2} = iL_2 rms \tag{64}$$

$$iL_{3rms} = \frac{Io(2+D)}{(1-D)} \tag{65}$$

Equations (66) to (72) present the effective current through capacitors. It can see that the rms current through C_4 is function of m, where m can be found in Equation (5).

$$Ic_1 rms = \frac{Io(2+D)}{(1-D)^2} \tag{66}$$

$$Ic_{2rms} = \frac{Io(2+D)\sqrt{1+D+D^2}}{\sqrt{(1-D)^3}} \tag{67}$$

$$Ic_{3rms} = \frac{Io(2+D)\sqrt{D+(1-D)^3}}{(1-D)^2} \tag{68}$$

$$Ic_{4rms} = \frac{Io(2+D)\sqrt{0.25(D-m)+(1-D)^3}}{(1-D)^2} \tag{69}$$

$$Ic_{5rms} = \frac{Io(2+D)\sqrt{0.25D+(1-D)^2(1-2D-h)}}{(1-D)^2} \tag{70}$$

$$Ic_{6rms} = \frac{Io(2+D)\sqrt{D+(1-D)^3}}{(1-D)^2} \tag{71}$$

$$Ic_{7rms} = \frac{Io\sqrt{4+5D}}{\sqrt{(1-D)}} \tag{72}$$

9.1 | Losses calculation for MOSFET devices

To analyse power losses in power MOSFETs, we categorize them into two types: conduction and switching losses. Equation (73) is utilized to calculate the MOSFET power conduction losses (*Pcd*). To determine the power switching loss of the MOSFET (*Psw*), both turn-on losses and turn-off losses are computed using Equation (74) in [31]. In this equation, Co represents the MOSFET's output capacitor, and Fs denotes the switching frequency. *Iswrms* refers to the rms switching current, while *tr* and *tf* refer to the on-rise and off-fall times of the switch, respectively.

The comprehensive evaluation of MOSFET power loss is encapsulated in Equation (75), identified as S_{PL}. This equation integrates both Equations (73) and (74), offering a holistic perspective on the overall power losses of MOSFETs.

$$Pcd = Isw_{rms}^2 rds \tag{73}$$

$$Psw = 0.5Vsw^2 CoFsw + 0.5FswVswI_{SWrms}(tr + tf) \tag{74}$$

$$S_{PL} = Isw_{rms}^2 rds + Psw \tag{75}$$

9.2 | Losses in power diode

The power losses in the diodes can be classified into two categories: internal resistance losses (*rd*) and forward diode voltage (*Vf*). It's imperative to consider all power losses associated with the seven diodes in the PC. The power losses (*Pvf*) arising from forward voltage are defined by Equation (76). The diode's average current can be computed using Equations (77) to (83). Equation (84) illustrates the diode power losses attributed to rd (P_{Dr}). The aggregation of all diode losses is necessary to determine the total diode power losses (D_{PL}) across the seven diodes, as expressed in Equation (85).

$$Pvf = I_{Dave} Vf \tag{76}$$

$$ID_{1ave} = \frac{Io(2+D)}{(1-D)} \tag{77}$$

$$ID_{2ave} = \frac{Io(2+D)}{(1-D)} \tag{78}$$

$$ID_{3ave} = \frac{Io(2+D)(1-D-m)}{(1-D)} \tag{79}$$

$$ID_{4ave} = \frac{Io(2+D)(D-m)}{2(1-D)^2} \tag{80}$$

$$ID_{5ave} = \frac{Io(2+D)(1-D-h)}{2(1-D)} \tag{81}$$

$$ID_{6ave} = \frac{Io(2+D)D}{2(1-D)} \tag{82}$$

$$ID_{7ave} = Io(2+D) \tag{83}$$

$$PDr = ID_{rms}^2 rd \tag{84}$$

$$D_{PL} = PDr + PVf \tag{85}$$

9.3 | Losses in inductors and capacitors

Equations (86) and (87) are instrumental in determining inductor (L_{PL}) and capacitor (C_{PL}) power losses. The total power loss in the PC, denoted as T_{PLPC}, can be found in Equation (88), encompassing losses from MOSFETs, diodes, inductors, and capacitors. Efficiency is calculated using Equation (89). The use of inductors characterized by minimal parasitic resistance values serves to enhance the performance and efficiency of the PC.

$$L_{PL} = iLrms^2 rl \tag{86}$$

$$C_{PL} = Icrms^2 rc \tag{87}$$

9.4 | Total power losses in the PC

$$T_{PLPC} = S_{PL} + \mathrm{D_{PL}} + \mathrm{L_{PL}} + \mathrm{C_{PL}} \tag{88}$$

$$\eta = \frac{P_o}{P_o + T_{PLPC}} 100\% \tag{89}$$

In Figure 8a, the adoption of flat wire inductors with low internal resistance leads to a substantial reduction in the overall power loss in the PC. Moreover, the efficiency of the PC sees improvement with the integration of components such as SiC MOSFETs, SiC diodes, and low-resistance capacitors. The proposed converter, featuring new interleaving, showcases a decrease in current stress through D_3, D_4, D_5, D_6 and D_7 when supplying 440 W, contributing to its heightened efficiency and performance.

In Figure 8b, it can be seen that the conduction losses of the switches of the proposed converter are significantly small when the system provides 440 W at V_o = 600 V. Moreover, it can be seen that Sw_1 has 0.35 W, Sw_2 has 1.13 W, and Sw_3 has 0.318 W when the PC provides high load power. In Figure 8c, it can be seen that the switching losses of the switches of the PC are significantly small when the proposed converter provides 440 W at V_o = 600 V. In addition, the reduction of voltage stress on all power switches significantly decreases switching power loss. Furthermore, the selection of SiC MOSFETs with very low output capacitance also contributes to a reduction in switching power loss.

In Figure 8d, it becomes apparent that a significant portion of the power loss is attributed to the capacitors and diodes. Additionally, losses arise from the intrinsic resistance of inductors and power switches within the system.

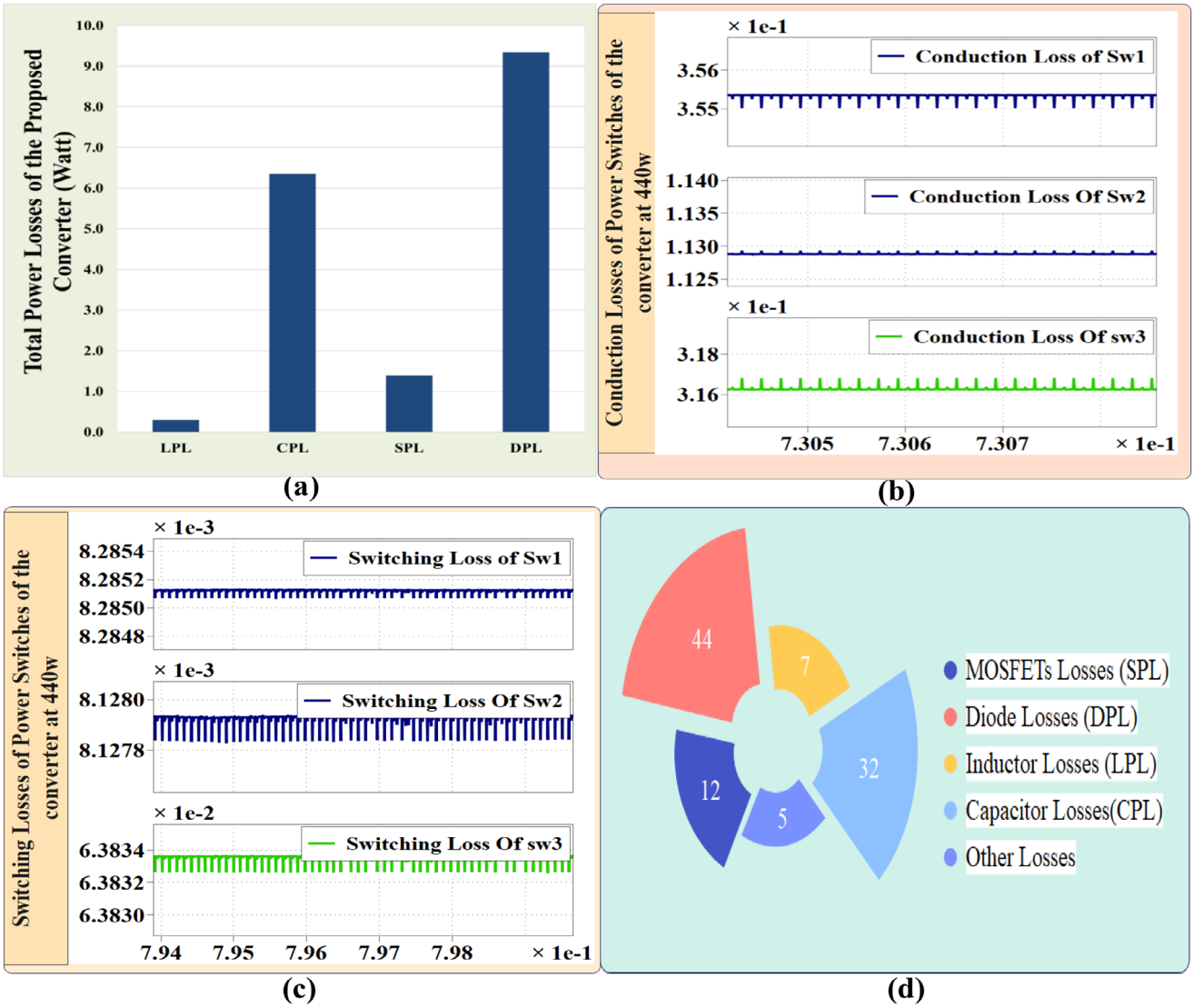


FIGURE 8 (a) Total power losses in PC (T_{PLPC}). (b) Conduction losses of all switches at 440 W of the PC. (c) Switching losses of all switches at 440 W of the PC. (d) Percentage losses of the elements in the PC.

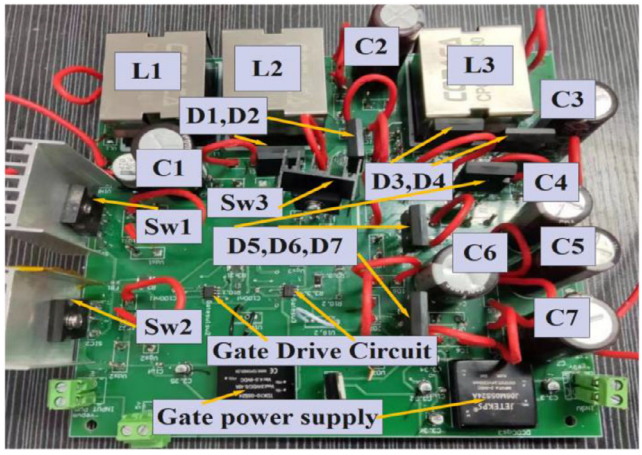


FIGURE 9 440 W PCB prototype of the PC.

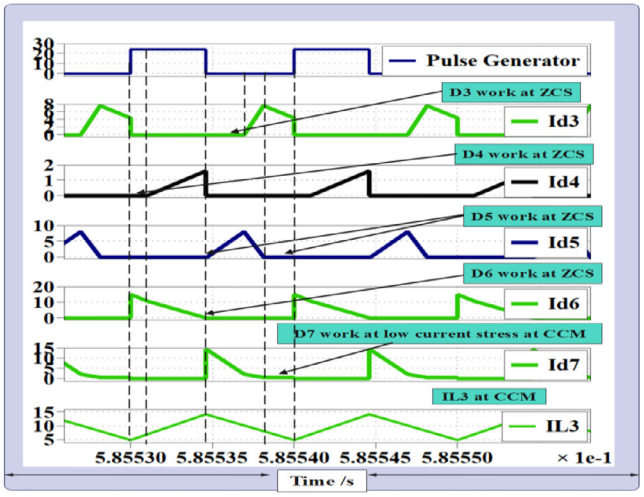


FIGURE 10 Gate voltage, Id_3, Id_4, Id_5, Id_6 and Id_7 at CCM.

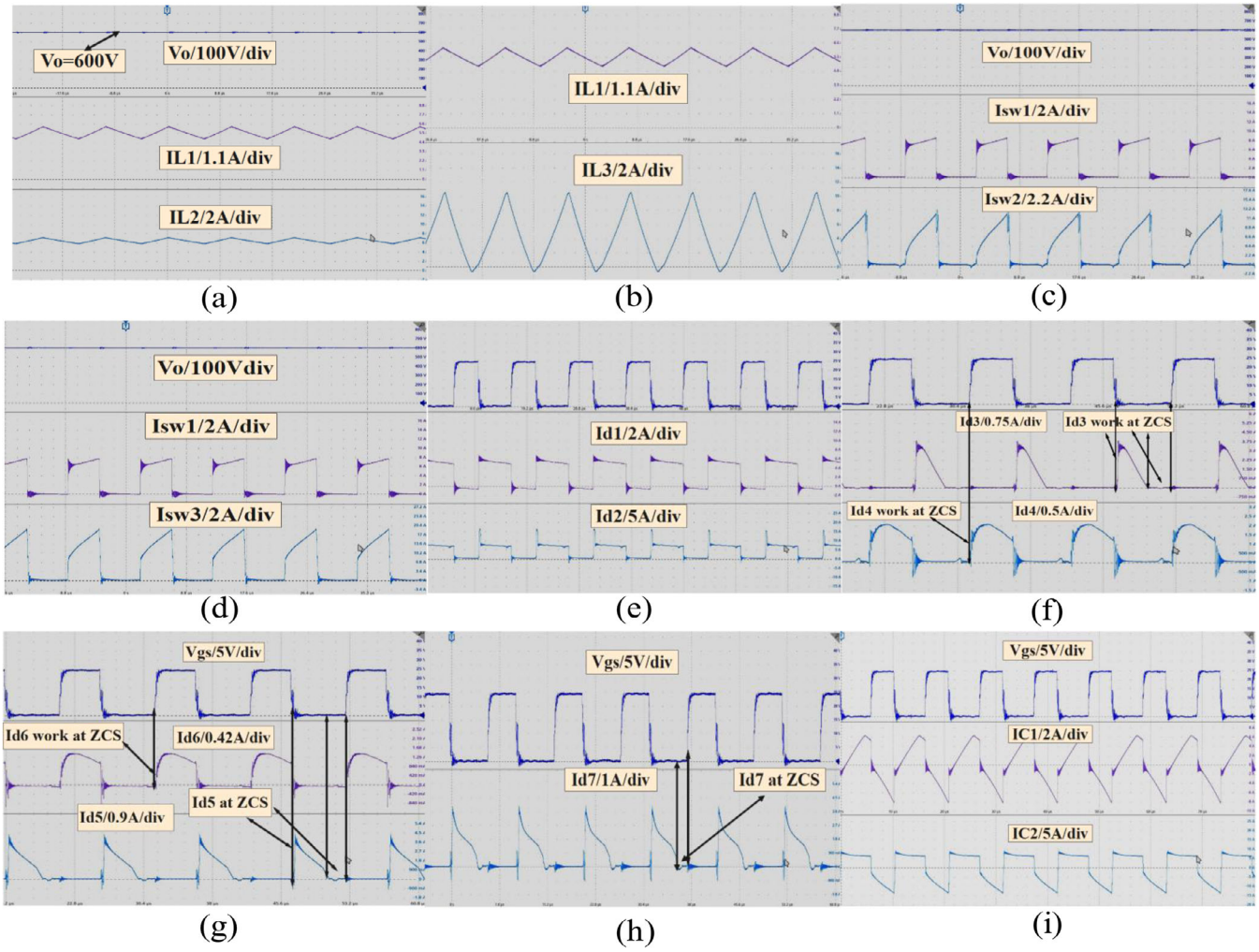


FIGURE 11 (a) $V_o = 600$ V, IL_1 and IL_2; (b) IL_1 and IL_3; (c) $Vo = 600$ V, Isw_1 and Isw_2; (d) Isw_1 and Isw_3; (e) Id_1 and Id_2; (f) Id_3 and Id_4; (g) Id_6 and Id_5; (h) Id_7; (i) Ic_1 and Ic_2.

10 | EXPERIMENTAL RESULTS AND DISCUSSIONS

The experimental results for the proposed converter were validated using a 440 W PCB prototype, as illustrated in Figure 9. The components used in the proposed converter are listed in Table 1, including all part numbers for MOSFETs and diodes. Where, the proposed converter has three power MOSFETs, seven capacitors, three inductors with small values and seven diodes. Rigorous quality validation and robustness assurance were achieved through the use of simulation tools such as MATLAB Simulink and PLECS software. These tools played a crucial role in verifying the results under diverse scenarios, thus reinforcing the effectiveness of the converter. To ensure even more robust verification, the same simulation software was used to recreate and cross-check the experimental outcomes under various conditions, further affirming the converter's functionality.

Figure 10 demonstrates that ZCS is achieved by D_3, D_4, D_5, and D_6, while the operation of the PC is in CCM. This signifies a significant reduction in current stress across diodes as the load current increases in the PC. As a result, there is a noteworthy decrease in conduction losses of the power diodes. Furthermore, the PC can maintain high efficiency and performance levels.

In Figure 11a, we observe the inductor currents, IL_1 and IL_2, when the PC operates in DCM mode at a 600 V output voltage and 440 W power with a duty cycle of 48%. In Figure 11b, we observe the inductor currents, IL_1 and IL_3, when the PC operates in DCM mode at $V_o = 600$ V. In Figure 11c,d, we see the currents through Sw_1, Sw_2, and Sw_3. These currents are significantly lower when the PC supplies a 440 W load, indicating a substantial reduction in conduction losses of three MOSFETs, leading to improved performance and efficiency for the PC. The pulse currents of Sw_1, Sw_2, and Sw_3 are equal to 8, 11.2, and 8 A, respectively.

In Figure 11e, we observe the current through D_1 and D_2 with low-stress current across them when the PC provides 440 W. Figure 11f shows the current through D_3 and D_4, where both of them operates under ZCS. Figure 11g displays the

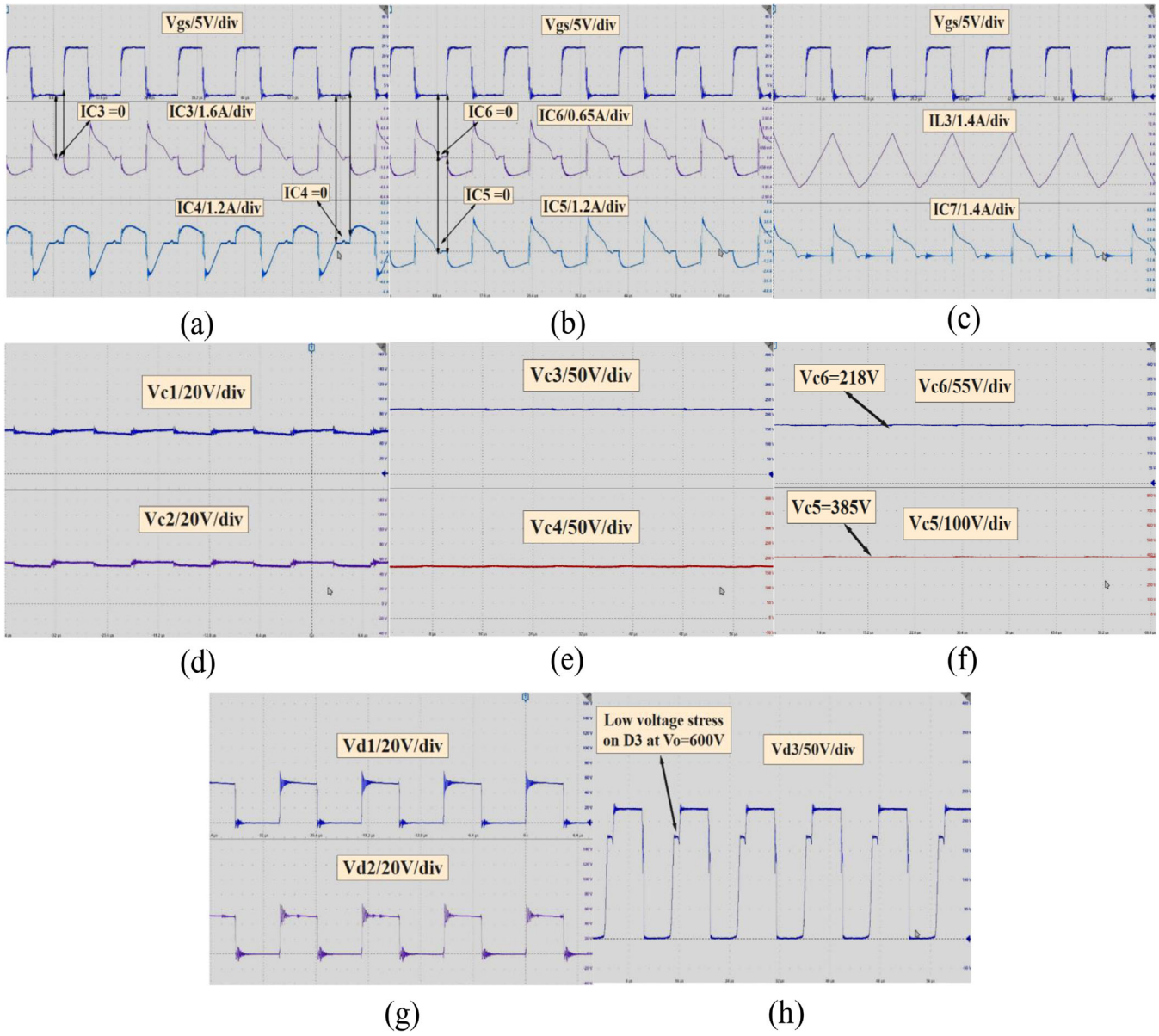


FIGURE 12 (a) Ic_3 and Ic_4; (b) Ic_6 and Ic_5; (c) IL_3 and Ic_7; (d) Vc_1 and Vc_2; (e) Vc_3 and Vc_4; (f) Vc_6 and Vc_7; (g) Vd_1 and Vd_2; (h) Vd_3.

current through D_6 and D_5, with both operating under ZCS. Figure 11h illustrates the current through D_7, with both operating under ZCS. Finally, in Figure 11i, we observe the current through C_1 and C_2 when the PC supplies 440 W at a duty cycle of 48%.

Figure 12a, it shows the current through C_3 and C_4 when the PC supplies 440 W, where, the current through C_3 and C_4 are same but in reverse direction and equal to zero during off state. Figure 12b, it shows the current through C_5 and C_6 where, the current through C_5 and C_6 are same but in reverse direction and equal to zero during off state. Figure 12c, it shows the current through IL_3 and C_7 where, the current through C_7 is equal to Io during off state.

Figure 12d, it can see the voltages across C_1 and C_2, respectively, can be observed which is equal to 60 V. Figure 12e, it can see the voltages across C_3 and C_4, respectively, can be observed where the voltage across C_3 is equal to 220 V and the voltage across C_4 is equal to 175 V. Figure 12f shows the voltage across C_5 and C_6, with the voltage across C_5 at 385 V and across C_6 at 218 V. The output voltage of the PC is the sum of Vc_5 and Vc_6, totalling 603 V. Figure 12g it is evident that the voltage stress across D_1 and D_2 is kept considerably low which is equal to 60 V at off state. Figure 12h it can see the voltage across D_3 which is very low voltage.

In Figure 13a,b the voltages across D_3, D_4, D_5, and D_6 show significant reductions when the PC operates at a high voltage gain of 600 V, where the voltage across the diodes is almost equal to half of the output voltage. Figure 13c displays the voltage across inductors L_1 and L_2 which equals the input voltage source, set at 31 V with an output voltage of 600 V. Figure 13d,

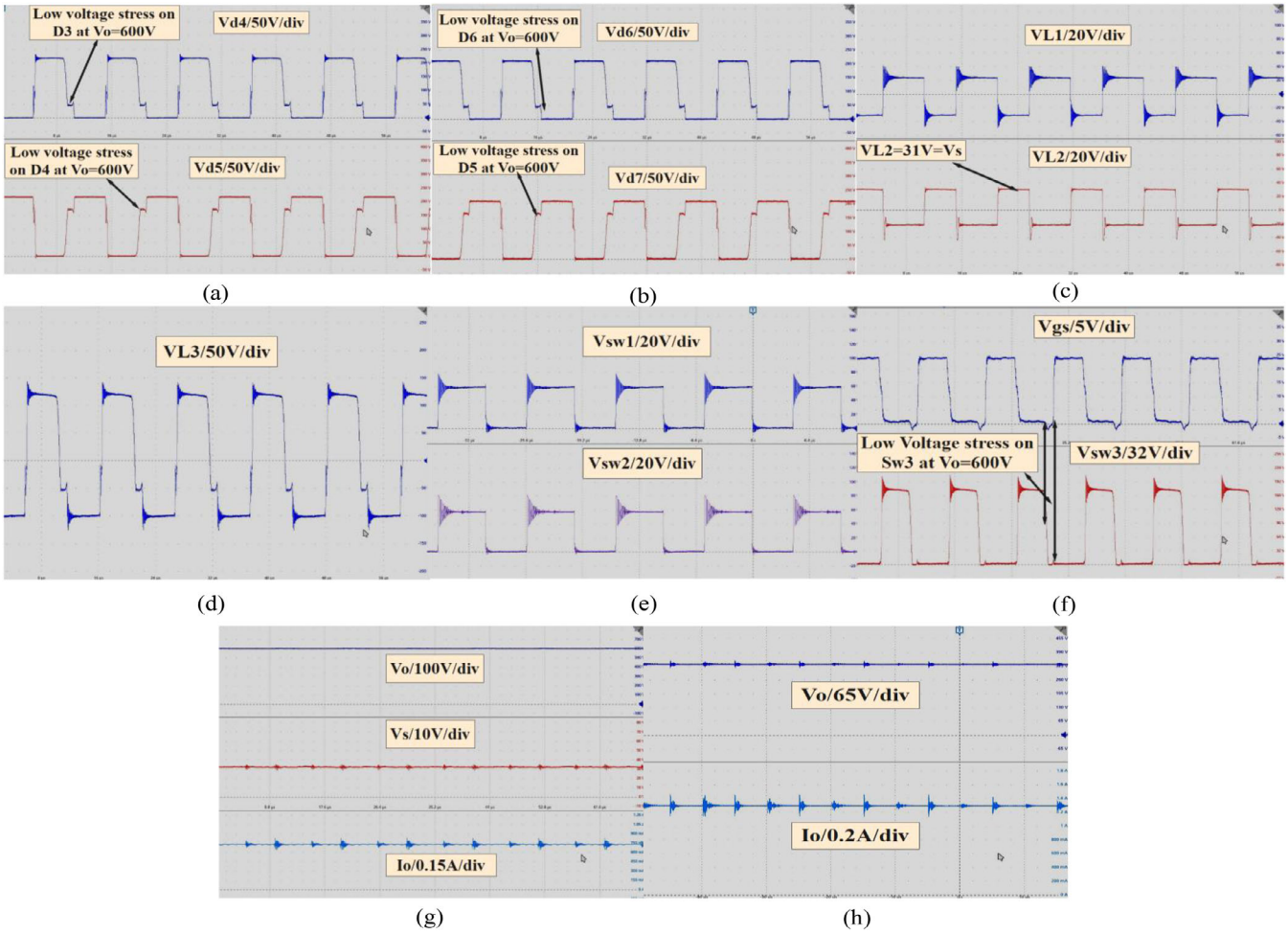
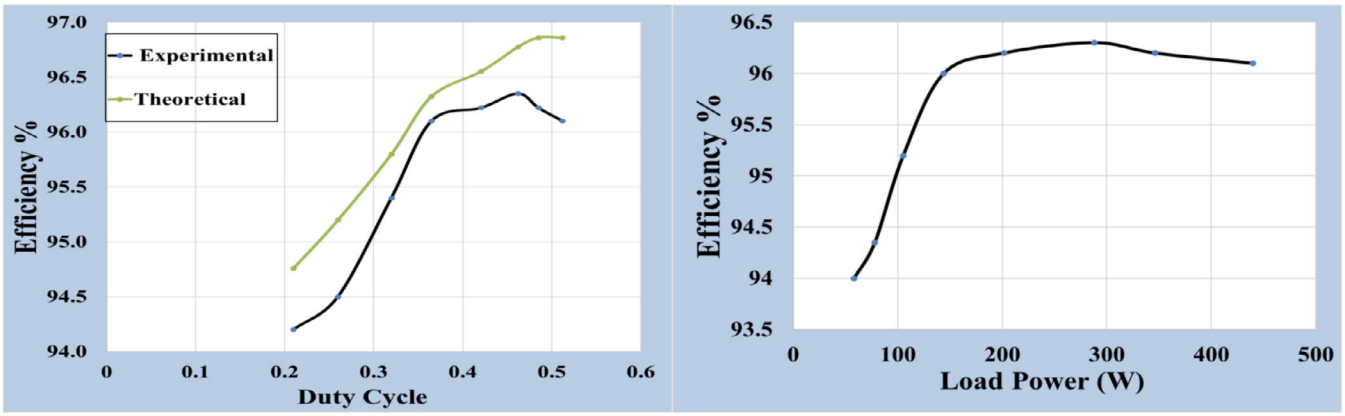


FIGURE 13 (a) Vd_4 and Vd_5; (b) Vd_6 and Vd_7; (c) VL_1 and VL_2; (d) VL_3; (e) Vsw_1 and Vsw_2; (f) Vsw_3; (g) $Vo = 600$ V, $Vs = 31$ V, $Io = 0.733$ A; (h) $Vo = 335$ V at 1.3 A at 440 W.

we see the voltage across inductor L_3, which remains at 120 V during the on state, equivalent to ($Vc_1 + Vc_2$). Figure 13e displays the S_{W1} and Sw_2 voltage across, which is very low and equivalent to the Vc_1 and Vc_2, respectively. Figure 13f, the voltage across S_{W3} is observed to be equal to 160 V with zero voltage switching when the PC operates at DCM at $V_o = 600$ V at 440 W. This implies that the power device's voltage stress is considerably diminished when the PC operates at a high output voltage. Consequently, the power MOSFETs switching losses are greatly minimized, enabling the PC to operate with high efficiency and performance. Figure 13g, we observe that the PC can supply 440 W at a high output voltage. Additionally, the load voltage is maintained at 600 V with a load current of 0.733 A at $Vs = 31$ V. Figure 13h, it can see that the PC can supply 335 V at 440 W at 1.33 A load current.

The converter efficiently steps up a 30 V input to 600 V output under a 440 W load, notably reducing stress on all diodes in MTBT. Where all diodes in MTBT achieve ZCS at specific times. To minimize current through S_{W2} and S_{W3}, this switch's stress also decreases when capacitor C_4 and C_5 charge reaches zero. The voltage stress on power diodes, MOSFETs, and inductors decreases considerably with $V_o = 600$ V at 440 W. This leads to a substantial reduction in switching and conduction losses for power devices, resulting in a substantial boost in efficiency. In essence, the PC performs at elevated levels of efficiency during high-load conditions. In Figure 14a,b, it is evident that the proposed converter PC exhibits high efficiency. Based on experimental calculations, it reaches 96.1% at a load voltage of 600 V and a load power of 440 W. In contrast, the theoretical calculation suggests that the efficiency of the proposed converter at 440 W is ≈96.6%, indicating a slight discrepancy when compared with the experimental efficiency test results.

Furthermore, it is noteworthy that the PC can operate with a duty cycle of 48% while maintaining an impressive efficiency of 96.1% under the same load conditions. It is essential to highlight that the inductors employed in the design of the PC are constructed using flat wire with exceptionally low internal resistance. Additionally, SiC MOSFET devices, known for their low internal resistance (R_{on}), have been strategically incorporated into the converter's design. Moreover, SiC diodes featuring low forward voltage (V_f) have been chosen to validate the high voltage gain achievable with this converter while maintaining high efficiency. Furthermore, it is worth noting that the input current of the PC exhibits minimal pulsation across a wide range of duty



(a) (b)

FIGURE 14 Efficiency of the PC (a) versus duty cycle at simulation and experimental test at 440 W at 600 V output voltage (b), versus output power of PC.

cycles, rendering the system exceptionally well-suited for integration into renewable energy systems. The incorporation of the ZCS technique in the PC significantly contributes to its ability to operate efficiently and deliver outstanding performance.

11 | CONCLUSION

As a result, an innovative non-isolated DC–DC converter has been designed to achieve ultra-high voltage gain while reducing current stress. This is accomplished by employing a MDBM interleaved with an MTBT and an MSLC. The primary objective is to attain an exceptionally high voltage gain, which is achieved by integrating the MTBT interleaved with secondary main and auxiliary third switches, along with an MSLC. This integration effectively doubles the voltage transfer gain. Additionally, the MSLC is combined with the auxiliary third and double main MOSFETs to further double the voltage gain, while simultaneously mitigating the voltage across the auxiliary MOSFET and diodes in the proposed converter. Furthermore, all diodes in the MTBT operate under zero current switching, ensuring that both the double main and auxiliary third MOSFETs experience very low current stress at ultra-high voltage gains. This efficiency is evident when the converter delivers 600 V at 440 W with an efficiency of 96.1% at a very low duty cycle. The input current of the proposed converter remains steady without pulsation at a low duty ratio, making the system more suitable for photovoltaic systems. The advantages of this converter include its ability to exhibit very high efficiency at high power levels, and to ensure minimal voltage stress on all MOSFETs, with low current stress on all power switches. After reducing current stress through all power switches, conduction loss is significantly decreased. Moreover, the voltage across all switches and diodes is remarkably low, resulting in very low switching loss.

AUTHOR CONTRIBUTIONS

Ammar Falah Algamluoli: Writing—original draft; methodology; software. **Xiaohua Wu**: Supervision; conceptualization. **Hayder K. Jahanger**: Resources; writing—review and editing.

CONFLICT OF INTEREST STATEMENT

The authors declare no conflicts of interest.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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How to cite this article: ALgamluoli, A.F., Wu, X., Jahanger, H.K.: Optimized ultra high voltage gain DC–DC converter with current stress reduction for photovoltaic application. IET Power Electron. 1–20 (2024). https://doi.org/10.1049/pel2.12726