Analytical Calculation Models for Bipolar MMC-HVDC Systems under Valve-side Single-phase-to-ground Faults

Pingyang Sun, *Graduate Student Member, IEEE,* Gen Li, *Senior Member, IEEE,* Hanwen Zhang, *Graduate Student Member, IEEE,* Jun Liang, *Fellow, IEEE,* Georgios Konstantinou, *Senior Member, IEEE*

***Abstract*—This paper proposes two analytical valve-side single-phase-to-ground (SPG) fault calculation models for bipolar modular multilevel converter-based high-voltage direct current (MMC-HVDC) system. The first model is applicable to the half-bridge submodule (HBSM) configuration, and the second is suitable for the full-bridge submodules (FBSMs) or hybrid SMs with different FBSM ratios. In each calculation model, two post-fault equivalent MMC circuits are established following converter blocking for the independent study of the upper and lower arms. The detailed expression of the post-fault voltages and currents in each arm, valve-side, and grid-side are obtained from the proposed calculation models. Moreover, the applicability of the calculation models for solid, inductive, and resistive dc-grounding methods is also demonstrated, along with a further discussion on the influence of MMC arm/grid-side resistance as well as varying fault-grounding impedance. Multiple bipolar MMC-HVDC systems, incorporating HBSM, FBSM, and hybrid SM configurations, are developed in PSCAD/EMTDC to validate the accuracy of the proposed analytical calculation models.**

***Index Terms*—Calculation model, high-voltage direct current (HVDC), modular multilevel converter (MMC), single-phase-to-ground (SPG) fault, valve-side ac fault.**

NOMENCLATURE

$\tilde{I}_{lox}, \tilde{I}_{vx}, \tilde{I}_G$	Current vectors for the lower arm currents, valve-side ac currents, grounding point current
$\tilde{U}_{Tx2}, \tilde{U}_{vx}$	Phase/line voltage vectors on the secondary side of transformer, valve-side phase voltage vectors
$I^{blk}_{loa,hb}$	Current flowing into the lower arm of faulted phase a at the blocking moment
k_T	Transformer voltage ratio (primary/secondary)
$L_{v,eq}, L_{arm}, L_{DG}, L_{FG}$	Valve-side equivalent inductance, arm inductance, dc-grounding inductance, fault-grounding inductance
m	MMC modulation index
N_t, N_{FB}	Total number of SMs in each arm, number of FBSMs in each arm
u_{upx}, u_{lox}	upper arm currents, lower arm currents
$U_{v,line}, U_{g,line}$	RMS line voltage on the valve-side, grid-side
u_{vx}, i_{vx}	valve-side ac voltages, currents under normal operation
u'_{vx}, i'_{vx}, i'_{gx}	post-fault valve-side ac voltages, valve-side ac currents, grid-side ac currents
V_C, ΔV_{Cux}, ΔV_{Clx}	Average capacitor voltage, SM capacitor voltage deviations of the upper arms, lower arms
V_{dc}, I_{dc}	Dc-link voltage, current

The work of Pingyang Sun and Georgios Konstantinou was supported under Australian Research Council's Discovery Project (DP210102294).

P. Sun, G. Konstantinou are with the School of Electrical Engineering and Telecommunications, UNSW Sydney, Australia (email: pingyang.sun@unsw.edu.au; g.konstantinou@unsw.edu.au).

G. Li is with the Energy Technology and Computer Science Section, Department of Engineering Technology, Technical University of Denmark (DTU), 2750 Ballerup, Denmark (email: genli@dtu.dk).

H. Zhang is with the Department of Energy Technology, Aalborg University, Denmark (email: hzha@energy.aau.dk).

J. Liang is with the School of Engineering, Cardiff University, UK (email: liangj1@cardiff.ac.uk).

I. INTRODUCTION

MODULAR multilevel converter-based high-voltage direct current (MMC-HVDC) systems are a crucial component of modern power grids, providing a more efficient solution for long-distance power transmission [1]. Different submodule (SM) configurations can be adopted in MMCs, such as half-bridge SMs (HBSMs), full-bridge SM (FBSMs) and hybrid SMs [2]. Bipolar MMC-HVDC systems have been used in commissioned projects, e.g., Xiamen [3] and Zhangbei [4].

Single-phase-to-ground (SPG) faults can occur on the valve-side of MMCs in either the positive or negative pole, often due to wall bushing insulation failures [5]–[8]. Unlike grid-side ac faults, valve-side ac faults occur at the interface between the transformer's secondary side and the valve group,

directly impacting MMC operation and potentially causing more severe overvoltage or overcurrent in the converter arms. To be specific, a valve-side SPG fault will lead to three significant problems: *i*) non-zero-crossings in grid-side currents for MMCs with HBSMs [5], *ii)* continuous charging of the lower arm SM capacitors for MMCs with low ratio of FBSMs in hybrid MMCs [9], and *iii)* continuous charging of upper arm SM capacitors for MMCs regardless of SM configurations [10], [11].

The first problem is present in MMCs with HBSMs. SM capacitors in the lower arms are bypassed by the diodes following converter blocking. The lower arm currents can only flow unidirectionally from the converter dc-side grounding point, through the lower-arm diodes, to the ac-side. This current flow leads to consistently positive or negative values of valve-side ac currents, which further results in high dc offset in the grid-side ac currents [5]. Therefore, grid-side ac circuit-breakers (ACCBs) may face challenges in interrupting fault currents [12].

The second problem appears in the lower arms of the MMC with low FBSM ratios (less than $0.866m$, m refers to the modulation index) in each arm [9]. Unlike the MMC with HBSMs, utilising a certain number of FBSMs can address the non-zero-crossing grid-side currents by using capacitor voltages to extinguish lower arm currents [13]. However, the FBSMs in the lower arms will be charged if the ratio of FBSMs in each arm is less than $0.866m$, until the lower arm voltage reaches the post-fault valve-side ac voltage. Continuous SM charging can lead to severe upper arm overvoltage, further threatening SM capacitors and MMC insulations.

The third problem emerges in the upper arms of the MMC with HBSMs, FBSMs or any ratios of FBSMs in each arm [9], [10]. After converter blocking, the upper arm currents flow from the positive point of the dc-side to the ac-side. Moreover, the currents also flow through upper arm capacitors in all SMs, creating potential charging paths. For unfaulted phases, the upper arm SM capacitors will be charged during the negative-cycle of the valve-side ac voltages. Although the valve-side ac voltage is zero for the faulted phase, the upper arm SM capacitors in the faulted phase will still charge if the dc voltage is increased [10].

Fault behaviours were analysed for the bipolar MMC with different SM configurations, and related protection schemes were presented to address the three issues in the current literature. The MMC with HBSMs under valve-side SPG faults was widely studied due to its simple SM configuration. The corresponding issue of non-zero-crossing in the grid currents can be addressed by three methods: 1) reduction of the lower arm current by using an LR circuit as the dc-side grounding [5]; 2) transfer of the lower arm current by arranging an antiparallel thyristor branch in parallel with each lower arm [12]; 3) blocking of the lower arm current by installing thyristor-pairs and damping SMs in series with each lower arm [14].

The use of FBSM [10] or hybrid SM [9] schemes has also been reported to demonstrate that FBSMs can ensure grid current zero-crossing. For both SM configurations, the upper arm overvoltage can be solved by: 1) redirecting the upper arm fault currents into a dc-link thyristor branch [13] or antiparallel thyristors in parallel with upper arms [10]; 2) blocking the upper arm by switching off the thyristor-pairs in series with the upper arms [14].

However, detailed analytical calculation models for bipolar MMC-HVDC systems with different SM configurations under valve-side SPG faults have not been established to accurately describe the steady-state post-fault system behaviours. This paper addresses this gap by proposing two analytical calculation models: one for HBSM configuration, and another for FBSM or hybrid SM configuration. Two post-fault equivalent MMC circuits following converter blocking are also built to analyse the upper and lower arms independently in each calculation model. The detailed voltage/current expressions including magnitudes and phases in the MMC arms, valve-side, and grid-side are derived through a thorough circuit analysis.

Multiple bipolar MMC-HVDC systems with three SM configurations (MMC with HBSMs, FBSMs, hybrid SMs) are developed in PSCAD/EMTDC to verify the accuracy of the proposed analytical calculation models. In addition, the influence of different dc-grounding methods (solid, inductive, resistive grounding [15]) and system resistors (MMC arm and ac grid resistors) is also examined to verify the broad applicability of the proposed analytical calculation models.

II. Operation Principle of Bipolar MMCs under Valve-Side SPG Faults

Fig. 1(a) shows a bipolar MMC-HVDC link. The circuit diagram of the positive pole MMC is shown in Fig. 1(b). Each arm includes in total N_t HBSMs, FBSMs or hybrid HBSMs & FBSMs, and one arm inductor (L_{arm}) [16], [17]. The valve-side phase voltages (u_{vx}) can be expressed as (1), and the upper and lower arm currents (i_{upa}, i_{loa}) in phase a are determined by (2) considering the circulating currents $i_{circa} = I_{dc}/3 + \sqrt{2}I_{2a}\sin(2\omega t + \phi)$, where I_{dc} is the dc current, I_{2a} refers to the RMS value of secondary harmonic current component in phase a [18].

$$u_{vx} = \frac{V_{dc}}{2} - \frac{L_{arm}}{2}\cdot\frac{di_{vx}}{dt} + \frac{u_{lox} - u_{upx}}{2} \quad (x = a, b, c), \tag{1}$$

$$\begin{cases} i_{upa} = \dfrac{i_{va}}{2} + \dfrac{I_{dc}}{3} + \sqrt{2}I_{2a}\sin(2\omega t + \phi) \\ i_{loa} = \dfrac{i_{va}}{2} - \dfrac{I_{dc}}{3} - \sqrt{2}I_{2a}\sin(2\omega t + \phi) \end{cases}, \tag{2}$$

where V_{dc} is the dc voltage, i_{vx} is the current flowing into the valve-side, u_{upx} and u_{lox} are the voltages produced by all SMs in the upper and lower arms. The transformer is wired in a Ynd configuration to block zero-sequence currents on the valve side, thereby eliminating triplen harmonics [19]. Several other transformer wiring configurations, including Dyn, Ynyn, and Yny, are also utilized in MMC projects. The Dyn method, used in the Nanhui project [20], and the Ynyn method, applied in the Luxi back-to-back project [21], are commonly implemented in symmetrical monopole MMC stations to provide an additional grounding point on the valve side. Moreover, the Yny method is used in bipolar UHVDC systems for reducing the winding insulation level, e.g. the two

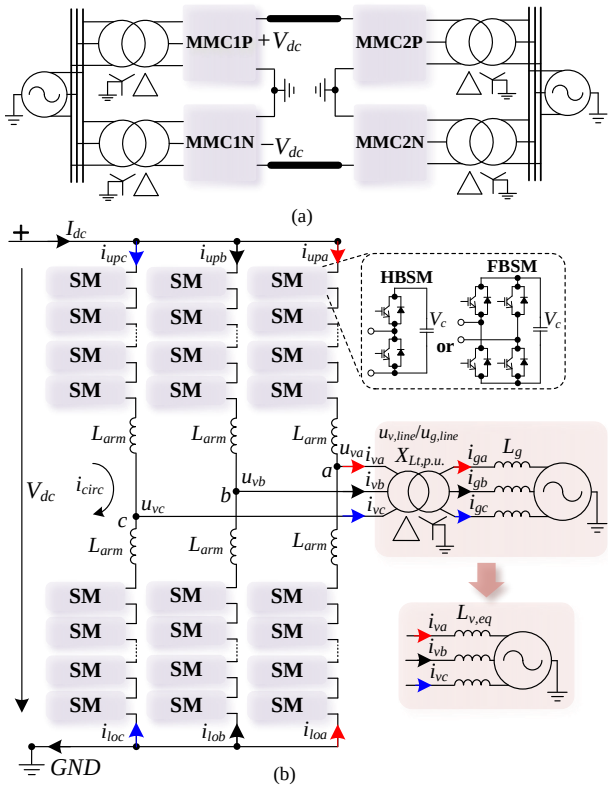


Fig. 1. A bipolar MMC-HVDC link: (a) System diagram, and (b) circuit diagram of the positive pole MMC (MMC1P).

MMC stations in Kunliulong hybrid UHVDC project [22]. The equivalent ac inductance ($L_{v,eq}$) referred to the valve-side for each phase can be calculated as:

$$L_{v,eq} = \frac{U_{v,line}^2}{S_{base}} \cdot \frac{X_{Lt,p.u.}}{\omega} + (\frac{U_{v,line}}{U_{g,line}})^2 \cdot L_g, \tag{3}$$

where $U_{v,line}$ is the RMS line voltage on the valve-side expressed by (4), $U_{g,line}$ is the RMS line voltage on the grid-side, S_{base} is the system base power represented by the power rating of the MMC in this paper, $X_{Lt,p.u.}$ is the per unit leakage inductance value in the transformer, and L_g refers to the inductor on the grid-side.

$$U_{v,line} = \frac{m \cdot \sqrt{3} V_{dc}}{2\sqrt{2}}, \tag{4}$$

where m is the modulation index of the MMC.

Following a valve-side SPG fault, the MMC should be blocked immediately to prevent large fault currents flowing through IGBTs. Figs. 2(a)-(c) present the equivalent circuits for a blocked MMC with HBSMs, FBSMs, and hybrid SMs, respectively, after a valve-side SPG fault occurring at t_0. For the MMC with HBSMs [Fig. 2(a)], the currents will flow from the dc-link (positive pole or dc-grounding point), through diodes D_{ua2}, D_{ub2}, D_{uc2} in the upper arms and D_{la1}, D_{lb1}, D_{lc1} in the lower arms, into the ac valve-side and grid-side. There is a capacitor charging path for each upper arm, leading to significant upper arm overvoltage as (5), which can also be applied for the MMC with FBSMs and hybrid SMs.

$$u_{upx} = V_{dc} - L_{arm} \cdot \frac{di_{upx}}{dt} - u'_{vx}, \tag{5}$$

where u'_{vx} indicates the post-fault valve-side ac phase voltages. All capacitors in the lower arms are bypassed by diodes, hence the lower arm voltage $u_{lox,hb}$ for the MMC with HBSMs is zero ($u_{lox,hb} = 0$), if the forward voltage drop in diodes is ignored. In addition, closed current loops are also formed through the lower arms in non-faulted phases and the converter dc-grounding, thereby resulting in non-zero-crossing of the grid currents [5].

For the MMC with FBSMs [Fig. 2(b)], the counter electromotive force (CEMF) provided by the lower arm capacitors will block the fault currents flowing from the dc-grounding point into the lower arms (through D_{l3} and D_{l4} in each lower arm), hence solving the issue of non-zero-crossing of the grid currents [10]. However, the upper arm overvoltage is still serious as the fault currents will flow from the positive pole to the ac-side, through diodes D_{u1} and D_{u2} in each upper arm. For the MMC with hybrid SMs [Fig. 2(c)], the upper arms will experience overvoltage as the upper arm currents flow through D_{u1}, D_{u2} in FBSMs and D_{u6} in HBSMs. Moreover, the lower arms may also experience overvoltage as the capacitors in the FBSMs can be charged through diodes D_{l3} and D_{l4} in each arm, even though all HBSMs are bypassed by diodes D_{la5}, D_{lb5} and D_{lc5}. This occurs when the ratio of FBSMs in each arm is less than $0.866m$ [9]. The lower arm voltage after a valve-side SPG fault for the MMC with FBSMs $u_{lox,fb}$ and hybrid SMs $u_{lox,hyb}$ can be respectively expressed as:

$$u_{lox,fb} = L_{arm} \cdot \frac{di_{lox,fb}}{dt} + u'_{vx,fb}, \quad \text{and} \tag{6}$$

$$u_{lox,hyb} = u^{FB}_{lox,hyb} = L_{arm} \cdot \frac{di_{lox,hyb}}{dt} + u'_{vx,hyb}, \tag{7}$$

where $u^{FB}_{lox,hyb}$ refers to the lower arm voltage generated by FBSMs in the MMC with hybrid SMs.

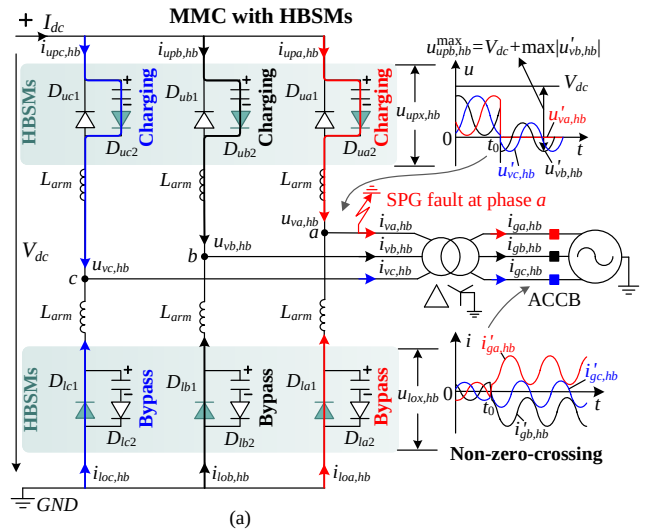
III. Modelling of the MMC with HBSMs

The proposed analytical calculation model for the MMC with HBSMs is described in this section. Since the fault currents flowing into the upper and lower arms originate from the dc-link to the ac-side as shown in Fig. 2, the upper and lower arms can be analysed separately. Therefore, two equivalent post-fault circuits (Fig. 3) for the lower and upper arms are established, while the detailed influence from the ac and dc sides are also considered to ensure the comprehensiveness of the analytical calculation model.

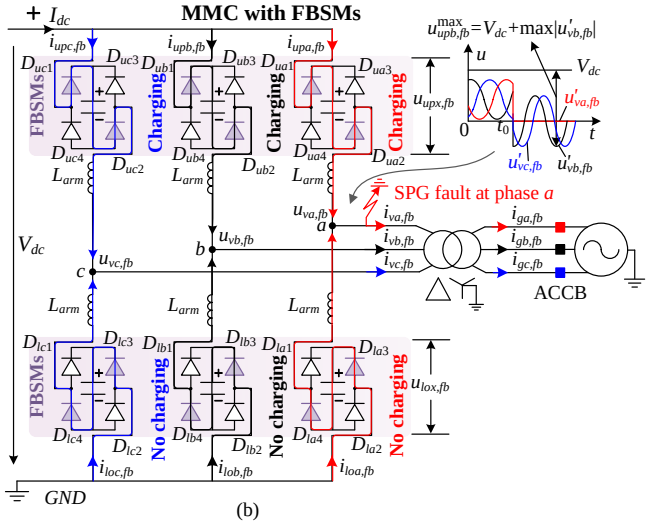
A. Lower Arm Post-fault Equivalent Circuit

The equivalent lower arm post-fault circuit is studied first, due to its direct impact on the valve-side ac voltage. As the SPG faults occur on the valve side, the grid-side ac voltage experiences no voltage drop, resulting in unchanged phase and line voltages (before the leakage inductance) on the secondary side of the transformer. Moreover, the phase voltage is equal to the line voltage for a delta connection, hence the three-phase phase/line voltage vectors on the secondary side of the transformer are expressed as:

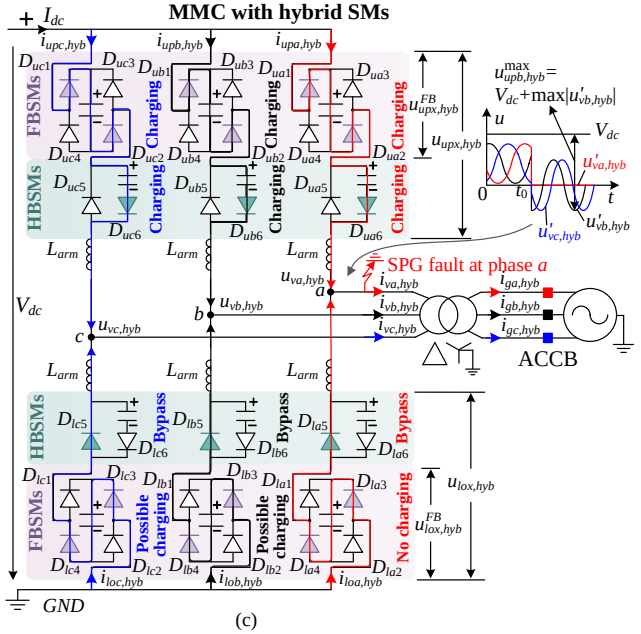
$$\begin{cases} \tilde{U}_{Ta2} = \sqrt{2} U_{v,line} \angle \theta^\circ \\ \tilde{U}_{Tb2} = \sqrt{2} U_{v,line} \angle (-120 + \theta)^\circ \\ \tilde{U}_{Tc2} = \sqrt{2} U_{v,line} \angle (120 + \theta)^\circ \end{cases}, \tag{8}$$



(a)



(b)



(c)

Fig. 2. Post-fault circuits of a blocked MMC: (a) MMC with HBSMs, (b) MMC with FBSMs, and (c) MMC with hybrid SMs.

where θ is the phase shift from the secondary side (delta-side) to the primary side (star-side) of the transformer, e.g., $\theta = 30°$ if the secondary side leads the primary side by $30°$. The detailed influence of the transformer wiring method will be discussed in Section III-C.

Fig. 3(a) depicts the equivalent post-fault circuit for the lower arms under a valve-side SPG fault occurred at phase a. In this equivalent circuit, it is assumed that the dc-grounding and the fault-grounding share a common grounding point GND. Because the diodes (D_{la1}, D_{lb1}, D_{lc1}) in the three lower arms allow current to flow only in one direction from the dc-grounding point to the ac-side, the loop current method can be applied in this direction to determine current values in different loops. To obtain the currents flowing into the three lower arms and the grounding-point, three current loops ($Loop1l$, $Loop2l$, $Loop3l$) are used and the following equation set can be established by loop-current method [23]:

$$\begin{cases} j\omega L_{arm}\tilde{I}_{loa} - j\omega L_G\tilde{I}_G = 0 \\ j\omega(L_{arm}+L_{v,eq})\tilde{I}_{lob} - j\omega L_G\tilde{I}_G - j\omega L_{v,eq}\tilde{I}_{va} = -\tilde{U}_{Tb2} \\ j\omega(L_{arm}+L_{v,eq})\tilde{I}_{loc} - j\omega L_G\tilde{I}_G - j\omega L_{v,eq}\tilde{I}_{va} = \tilde{U}_{Ta2} \\ \tilde{I}_{loa}+\tilde{I}_{lob}+\tilde{I}_{loc}+\tilde{I}_G = 0 \\ \tilde{I}_{loa}+\tilde{I}_G-\tilde{I}_{va} = 0 \end{cases}, \quad (9)$$

where $\omega L_G = \omega(L_{DG} + L_{FG})$, with L_{DG} referring to the dc-grounding inductance and L_{FG} representing the fault-grounding inductance. Moreover, (9) can be expressed as a vector matrix equation:

$$j\boldsymbol{X_L}\cdot\boldsymbol{I} = \boldsymbol{U}, \quad (10)$$

where

$$\boldsymbol{X_L} = \begin{bmatrix} \omega L_{arm} & 0 & 0 & -\omega L_G & 0 \\ 0 & \omega(L_{arm}+L_{v,eq}) & 0 & -\omega L_G & -\omega L_{v,eq} \\ 0 & 0 & \omega(L_{arm}+L_{v,eq}) & -\omega L_G & -\omega L_{v,eq} \\ -j & -j & -j & -j & 0 \\ -j & 0 & 0 & -j & j \end{bmatrix} \quad (11)$$

$$\boldsymbol{I} = \left[\tilde{I}_{loa}, \quad \tilde{I}_{lob}, \quad \tilde{I}_{loc}, \quad \tilde{I}_G, \quad \tilde{I}_{va}\right]^{-1} \quad (12)$$

$$\boldsymbol{U} = \left[0, \quad -\tilde{U}_{Tb2}, \quad \tilde{U}_{Ta2}, \quad 0, \quad 0\right]^{-1} \quad (13)$$

The current vectors for the lower arm currents, grounding point current, and valve-side ac currents can be obtained by solving (10), as (14), respectively. In addition, the phase voltage on the valve-side can also be derived as (15) from (10). If the dc-grounding and fault-grounding reactance $\omega(L_{DG} + L_{FG})$ are ignored (zero grounding impedance), (14) and (15) can be simplified as (16) and (17), respectively.

$$\begin{cases} \tilde{I}_{loa} = I^{blk}_{loa,hb} \\ \tilde{I}_G = \tilde{I}_{va} = \dfrac{L_{arm}(\tilde{U}_{Tb2}-\tilde{U}_{Ta2})}{j\omega L_{arm}(L_{arm}+3L_{v,eq})} \\ \tilde{I}_{lob} = \tilde{I}_{vb} = \dfrac{-L_{arm}\left[L_{v,eq}(2\tilde{U}_{Tb2}+\tilde{U}_{Ta2})+L_{arm}\tilde{U}_{Tb2}\right]}{j\omega L_{arm}(L_{arm}+L_{v,eq})(L_{arm}+3L_{v,eq})} \\ \tilde{I}_{loc} = \tilde{I}_{vc} = \dfrac{L_{arm}\left[L_{v,eq}(2\tilde{U}_{Ta2}+\tilde{U}_{Tb2})+L_{arm}\tilde{U}_{Ta2}\right]}{j\omega L_{arm}(L_{arm}+L_{v,eq})(L_{arm}+3L_{v,eq})} \end{cases}, \quad (16)$$

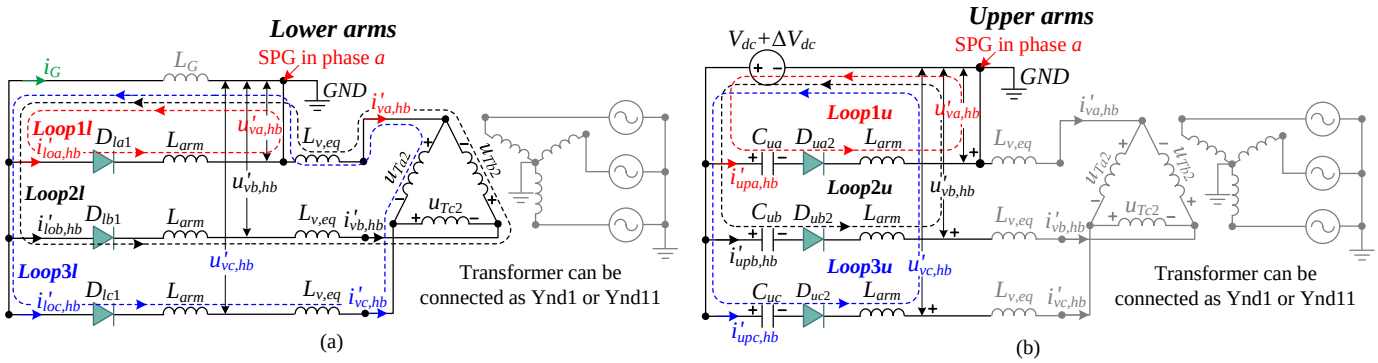


Fig. 3. Equivalent circuits for the MMC with HBSMs under a valve-side SPG fault: (a) lower arms, and (b) upper arms.

$$\begin{cases} \tilde{I}_{loa} = \dfrac{L_G(\tilde{U}_{Tb2}-\tilde{U}_{Ta2})}{j\omega\left[(L_{arm}+L_G)(L_{arm}+3L_{v,eq})+2L_{arm}L_G\right]} \\ \tilde{I}_{lob} = \tilde{I}_{vb} = \dfrac{-L_{arm}L_G(\tilde{U}_{Ta2}+\tilde{U}_{Tb2})-(L_{arm}+L_G)\left[L_{v,eq}(2\tilde{U}_{Tb2}+\tilde{U}_{Ta2})+L_{arm}\tilde{U}_{Tb2}\right]}{j\omega(L_{arm}+L_{v,eq})\left[(L_{arm}+L_G)(L_{arm}+3L_{v,eq})+2L_{arm}L_G\right]} \\ \tilde{I}_{loc} = \tilde{I}_{vc} = \dfrac{L_{arm}L_G(\tilde{U}_{Ta2}+\tilde{U}_{Tb2})+(L_{arm}+L_G)\left[L_{v,eq}(2\tilde{U}_{Ta2}+\tilde{U}_{Tb2})+L_{arm}\tilde{U}_{Ta2}\right]}{j\omega(L_{arm}+L_{v,eq})\left[(L_{arm}+L_G)(L_{arm}+3L_{v,eq})+2L_{arm}L_G\right]} \\ \tilde{I}_G = \dfrac{L_{arm}(\tilde{U}_{Tb2}-\tilde{U}_{Ta2})}{j\omega\left[(L_{arm}+L_G)(L_{arm}+3L_{v,eq})+2L_{arm}L_G\right]} \\ \tilde{I}_{va} = \tilde{I}_{loa}+\tilde{I}_G = \dfrac{(L_{arm}+L_G)(\tilde{U}_{Tb2}-\tilde{U}_{Ta2})}{j\omega\left[(L_{arm}+L_G)(L_{arm}+3L_{v,eq})+2L_GL_{arm}\right]} \end{cases} \tag{14}$$

$$\begin{cases} \tilde{U}_{va} = j\omega L_{FG}\cdot\tilde{I}_G = \dfrac{L_{FG}L_{arm}(\tilde{U}_{Tb2}-\tilde{U}_{Ta2})}{(L_{arm}+L_G)(L_{arm}+3L_{v,eq})+2L_{arm}L_G} \\ \tilde{U}_{vb} = j\omega L_{arm}\cdot\tilde{I}_{lob}-j\omega L_{DG}\cdot\tilde{I}_G = \dfrac{-L_{arm}(3L_{arm}L_{DG}+3L_{v,eq}L_{DG}+2L_{arm}L_{v,eq}+L_{arm}^2)\tilde{U}_{Tb2}-L_{arm}^2L_{v,eq}\tilde{U}_{Ta2}}{(L_{arm}+L_{v,eq})\left[(L_{arm}+L_{DG})(L_{arm}+3L_{v,eq})+2L_{arm}L_{DG}\right]} \\ \tilde{U}_{vc} = j\omega L_{arm}\cdot\tilde{I}_{loc}-j\omega L_{DG}\cdot\tilde{I}_G = \dfrac{L_{arm}(3L_{arm}L_{DG}+3L_{v,eq}L_{DG}+2L_{arm}L_{v,eq}+L_{arm}^2)\tilde{U}_{Ta2}+L_{arm}^2L_{v,eq}\tilde{U}_{Tb2}}{(L_{arm}+L_{v,eq})\left[(L_{arm}+L_{DG})(L_{arm}+3L_{v,eq})+2L_{arm}L_{DG}\right]} \end{cases} \tag{15}$$

where $I_{loa,hb}^{blk}$ is the current flowing into the lower arm of phase a at the blocking moment.

$$\begin{cases} \tilde{U}_{va} = 0 \\ \tilde{U}_{vb} = \dfrac{-L_{arm}^2(2L_{v,eq}+L_{arm})\tilde{U}_{Tb2}-L_{arm}^2L_{v,eq}\tilde{U}_{Ta2}}{L_{arm}(L_{arm}+L_{v,eq})(L_{arm}+3L_{v,eq})} \\ \tilde{U}_{vc} = \dfrac{L_{arm}^2(2L_{v,eq}+L_{arm})\tilde{U}_{Ta2}+L_{arm}^2L_{v,eq}\tilde{U}_{Tb2}}{L_{arm}(L_{arm}+L_{v,eq})(L_{arm}+3L_{v,eq})} \end{cases} \tag{17}$$

It is noted that all three lower arm currents have dc offsets due to the presence of arm diodes, hence:

$$\begin{cases} i'_{loa,hb} = I_{loa,hb}^{blk} = 0, \quad \text{if arm resistor is considered} \\ i'_{lob,hb} = i'_{vb,hb} = \left|\tilde{I}_{lob}\right|\left[\sin(\omega t)+\tan^{-1}\left(\dfrac{\mathrm{Im}(\tilde{I}_{lob})}{\mathrm{Re}(\tilde{I}_{lob})}\right)\right]+\left|\tilde{I}_{lob}\right| \geq 0 \\ i'_{loc,hb} = i'_{vc,hb} = \left|\tilde{I}_{loc}\right|\left[\sin(\omega t)+\tan^{-1}\left(\dfrac{\mathrm{Im}(\tilde{I}_{loc})}{\mathrm{Re}(\tilde{I}_{loc})}\right)\right]+\left|\tilde{I}_{loc}\right| \geq 0 \end{cases} \tag{18}$$

which also shows the valve-side ac currents of the two non-faulted phases are always positive. Thus, the valve-side ac current of the faulted phase is always negative as:

$$i'_{va,hb} = -(i'_{vb,hb}+i'_{vc,hb}) < 0 \tag{19}$$

For the valve-side ac voltages, there are no dc offsets because the dc-link voltage is zero in the lower arm equivalent circuit, hence the three-phase valve-side ac voltages are expressed as:

$$\begin{cases} u'_{va,hb} = 0, \\ u'_{vb,hb} = \left|\tilde{U}_{vb}\right|\left[\sin(\omega t)+\tan^{-1}\left(\dfrac{\mathrm{Im}(\tilde{U}_{vb})}{\mathrm{Re}(\tilde{U}_{vb})}\right)\right], \\ u'_{vc,hb} = \left|\tilde{U}_{vc}\right|\left[\sin(\omega t)+\tan^{-1}\left(\dfrac{\mathrm{Im}(\tilde{U}_{vc})}{\mathrm{Re}(\tilde{U}_{vc})}\right)\right] \end{cases} \tag{20}$$

where $|\tilde{U}_{vb}| = |\tilde{U}_{vc}| < \sqrt{2}U_{v,line}$. Moreover, the voltage across each lower arm $u_{lox,hb}$ is zero for the MMC with HBSMs.

B. Upper Arm Post-fault Equivalent Circuit

Fig. 3(b) shows the equivalent post-fault circuit for the upper arms under a valve-side SPG fault. Since the post-fault valve-side ac voltages (20) have derived in Section III-A, they can be directly used in the analysis for the upper arms. There are three current loops (*Loop*1u, *Loop*2u, *Loop*3u) in this equivalent circuit, clearly showing that the SM capacitors in the upper arms will be charged until the diodes D_{ua}, D_{ub}, and D_{uc} are reversely biased. Hence, the upper arm voltages are derived as (21), once the SM capacitor charging process is complete and the upper arm currents decrease to zero (22).

$$\begin{cases} u_{upa,hb} = -u'_{va,hb}+V_{dc} = V_{dc} \\ u_{upb,hb} = -u'_{vb,hb}+V_{dc} \\ u_{upc,hb} = -u'_{vc,hb}+V_{dc} \end{cases} \tag{21}$$

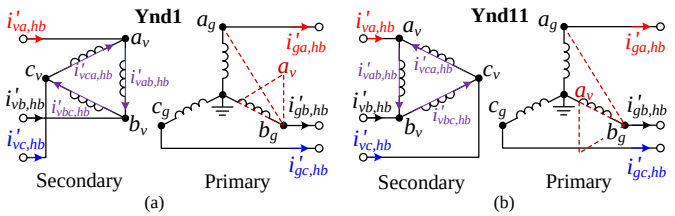


Fig. 4. Transformer wiring configurations: (a) Ynd1, and (b) Ynd11.

$$i'_{upa,hb} = i'_{upb,hb} = i'_{upc,hb} = 0 \tag{22}$$

To rearrange (21) and consider $V_{dc} = N_t V_C$ (V_C refers to the average capacitor voltage), the post-fault SM capacitor voltage deviation in each upper arm is derived as:

$$\begin{cases} \Delta V_{Cua,hb} = \max|u'_{va,hb}|/N_t = |\tilde{U}_{va}|/N_t = 0 \\ \Delta V_{Cub,hb} = \max|u'_{vb,hb}|/N_t = |\tilde{U}_{vb}|/N_t \\ \Delta V_{Cuc,hb} = \max|u'_{vc,hb}|/N_t = |\tilde{U}_{vc}|/N_t \end{cases} . \tag{23}$$

However, the actual SM capacitor voltage deviation may exceed the calculated values (23) due to the transient voltage deviations in the dc-link and the valve-side following valve-side SPG faults.

C. DC Offsets in Grid-side AC Currents

It is demonstrated in Section III-A that the valve-side ac currents contain high dc offsets in all three phases (18), (19) following a valve-side SPG fault. This section will discuss how the post-fault valve-side ac currents influence the grid-side ac currents. Fig. 4 shows two widely used transformer wiring configurations (Ynd1 and Ynd11) in the MMC where the secondary side (delta-side) lags or leads the primary side (star-side) by 30° [24]. For the first connection [Ynd1 - Fig. 4(a)], the relationship between the valve-side and grid-side ac currents can be established as:

$$\begin{cases} i'_{va,hb} = i'_{vab,hb} - i'_{vca,hb} = \dfrac{k_T(i'_{ga,hb} - i'_{gc,hb})}{\sqrt{3}} \\ i'_{vb,hb} = i'_{vbc,hb} - i'_{vab,hb} = \dfrac{k_T(i'_{gb,hb} - i'_{ga,hb})}{\sqrt{3}} \\ i'_{vc,hb} = i'_{vca,hb} - i'_{vbc,hb} = \dfrac{k_T(i'_{gc,hb} - i'_{gb,hb})}{\sqrt{3}} \end{cases} , \quad \text{for Ynd1} \tag{24}$$

where k_T is the transformer voltage ratio and $k_T = U_{g,line}/U_{v,line}$. This relationship for the second connection [Ynd11 - Fig. 4(b)] follows:

$$\begin{cases} i'_{va,hb} = i'_{vab,hb} - i'_{vca,hb} = \dfrac{k_T(i'_{ga,hb} - i'_{gb,hb})}{\sqrt{3}} \\ i'_{vb,hb} = i'_{vbc,hb} - i'_{vab,hb} = \dfrac{k_T(i'_{gc,hb} - i'_{ga,hb})}{\sqrt{3}} \\ i'_{vc,hb} = i'_{vca,hb} - i'_{vbc,hb} = \dfrac{k_T(i'_{gb,hb} - i'_{gc,hb})}{\sqrt{3}} \end{cases} , \quad \text{for Ynd11} \tag{25}$$

Since the zero-sequence current is not present on the primary side, the grid currents satisfy:

$$i'_{ga,hb} + i'_{gb,hb} + i'_{gc,hb} = 0. \tag{26}$$

By combining (24), (26) for Ynd1, and (25), (26) for Ynd11, the grid currents for the two wiring methods (27), (28) can be obtained, respectively.

$$\begin{cases} i'_{ga,hb} = -\dfrac{(2i'_{vb,hb} + i'_{vc,hb})}{\sqrt{3}k_T} < 0 \\ i'_{gb,hb} = \dfrac{(i'_{vb,hb} - i'_{vc,hb})}{\sqrt{3}k_T} \\ i'_{gc,hb} = \dfrac{(i'_{vb,hb} + 2i'_{vc,hb})}{\sqrt{3}k_T} > 0 \end{cases} , \quad \text{for Ynd1} \tag{27}$$

$$\begin{cases} i'_{ga,hb} = -\dfrac{(2i'_{vb,hb} + i'_{vc,hb})}{\sqrt{3}k_T} < 0 \\ i'_{gb,hb} = \dfrac{(i'_{vb,hb} + 2i'_{vc,hb})}{\sqrt{3}k_T} > 0 \\ i'_{gc,hb} = \dfrac{(i'_{vb,hb} - i'_{vc,hb})}{\sqrt{3}k_T} \end{cases} , \quad \text{for Ynd11} \tag{28}$$

The two equations show that the post-fault grid currents in two phases are always positive or negative for both the two wiring options ($i'_{ga,hb}$, $i'_{gc,hb}$ for Ynd1, $i'_{ga,hb}$, $i'_{gb,hb}$ for Ynd11). Therefore, the grid-side ACCBs encounter difficulties in interrupting the fault currents after a valve-side SPG fault in the MMC with HBSMs.

IV. Modelling of the MMC with FBSMs or Hybrid SMs

This section provides a detailed description the proposed analytical calculation model for the MMC with FBSMs or hybrid SMs. Two SM configurations can share the same calculation model, since they have identical equivalent post-fault upper and lower arm circuits as shown in Fig. 5. Similar to the analysis in the MMC with HBSMs, the upper and lower arms are analyzed separately to specifically study the overvoltage level in each arm.

A. Lower Arm Post-fault Equivalent Circuit

Unlike the MMC with HBSMs, there are no post-fault arm currents in any of the three lower arms (29) because the CEMF provided by the FBSM capacitors (C_{la}, C_{lb}, C_{lc} in Fig. 5(a)) will extinguish the arm fault currents. However, lower arm overvoltage may occur with a low ratio of FBSMs in each arm.

$$i'_{loa,fb(hyb)} = i'_{lob,fb(hyb)} = i'_{loc,fb(hyb)} = 0 \tag{29}$$

The post-fault, valve-side, phase-to-ground voltage transitions to the line voltage on the secondary side (delta-side) of the transformer. This occurs as the voltage in the faulted phase drops to zero (assuming zero grounding impedance), resulting in the grounding point shifting away from the neutral point as shown in Fig. 6. Moreover, the phase difference between the two non-faulted phases changes from 120° to 60°:

$$\begin{cases} u'_{va,fb(hyb)} = 0, \\ u'_{vb,fb(hyb)} = \sqrt{2}U_{v,line}\sin(\omega t - 120° + \theta) \\ u'_{vc,fb(hyb)} = \sqrt{2}U_{v,line}\sin(\omega t - 180° + \theta) \end{cases} . \tag{30}$$

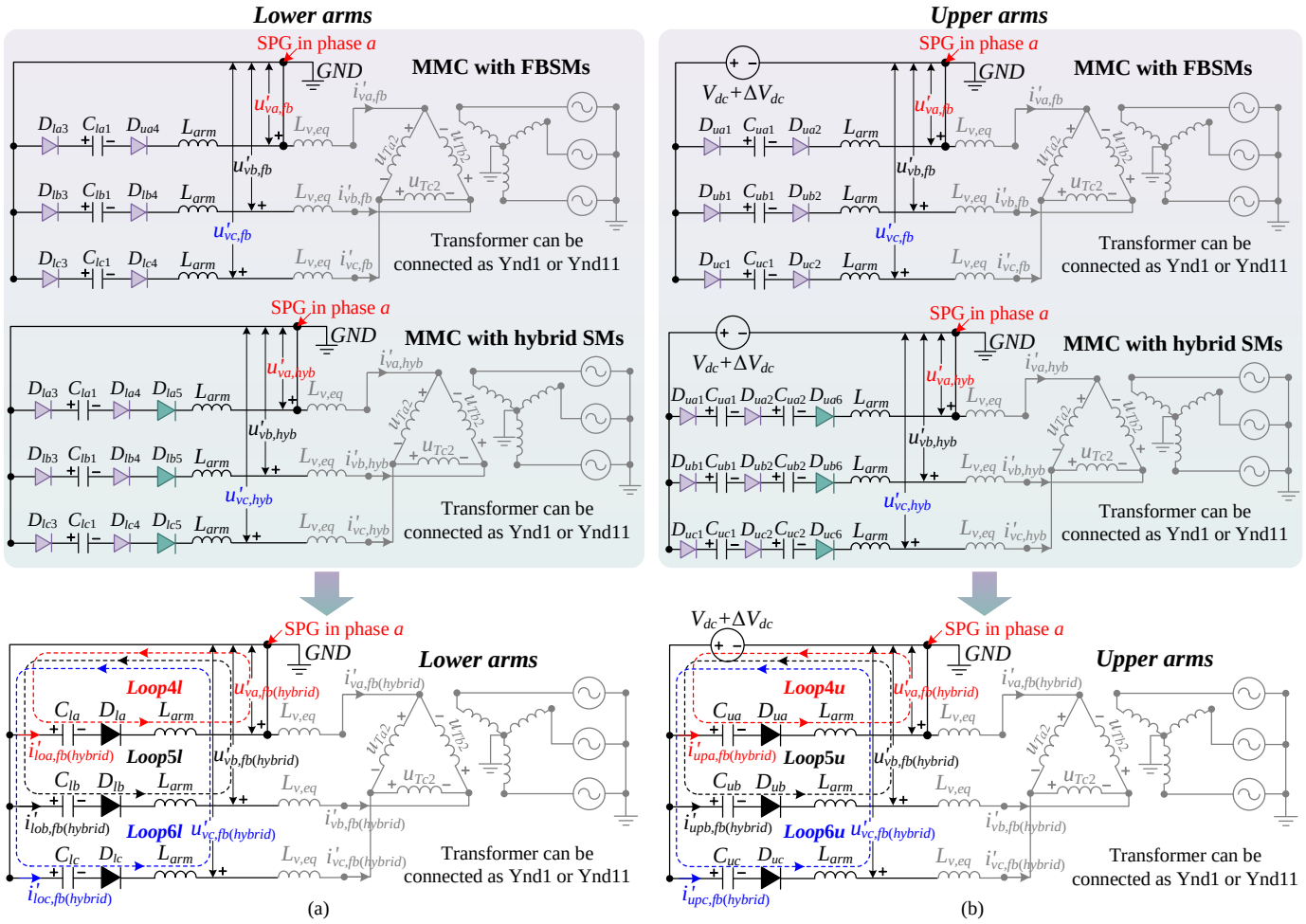


Fig. 5. Equivalent circuits for the MMC with FBSMs or hybrid SMs under a valve-side SPG fault: (a) lower arms, and (b) upper arms.

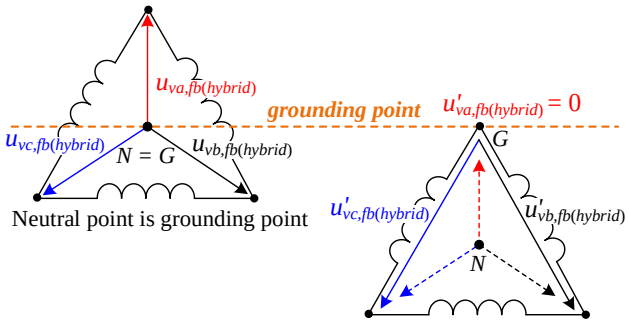


Fig. 6. Valve-side phase voltage under a valve-side SPG fault for the MMC with FBSMs or hybrid SMs.

1) MMC with FBSMs: In all three loops (*Loop4l*, *Loop5l*, *Loop6l*) shown in Fig. 5(a), the pre-fault capacitor voltage is larger than the maximum post-fault valve-side voltage:

$$\begin{cases} V_{C_{la,fb}} = N_t V_C > 0, \\ V_{C_{lb,fb}} = N_t V_C > \max|u'_{vb,fb}| = \sqrt{2}U_{v,line} \\ V_{C_{lc,fb}} = N_t V_C > \max|u'_{vc,fb}| = \sqrt{2}U_{v,line} \end{cases}, \tag{31}$$

thus the diodes D_{la}, D_{lb}, D_{lc} in the three lower arms will be inversely biased immediately after converter blocking, preventing any overvoltage in the lower arms for the MMC with FBSMs. Combining (6) and (29), the steady-state post-fault lower arm voltage is:

$$\begin{cases} u_{loa,fb} = 0 \\ u_{lob,fb} = u'_{vb,fb} \\ u_{loc,fb} = u'_{vc,fb} \end{cases}. \tag{32}$$

2) MMC with Hybrid SMs: As the post-fault lower arm currents will be gradually decreased to zero (29) in the MMC with hybrid SMs, the lower arm voltage is changed to (33) by combining (7) and (29). Therefore, the FBSM capacitors could be charged if the pre-fault capacitor voltage in the FBSMs is smaller than the post-fault valve-side voltage.

$$\begin{cases} u_{loa,hyb} = u^{FB}_{loa,hyb} = 0 \\ u_{lob,hyb} = u^{FB}_{lob,hyb} = u'_{vb,hyb} \\ u_{loc,hyb} = u^{FB}_{loc,hyb} = u'_{vc,hyb} \end{cases} \tag{33}$$

The minimum number of FBSMs required in each arm to prevent lower arm overvoltage is determined by (34), considering the relationship between the dc voltage and the valve-side line voltage (4) [9].

$$N^{\min}_{FB} = \frac{\max|u'_{vb,hyb}|}{V_C} = \frac{\max|u'_{vc,hyb}|}{V_C} = \frac{\sqrt{2}U_{v,line}}{V_C} = 0.866 \cdot m \cdot N_t \tag{34}$$

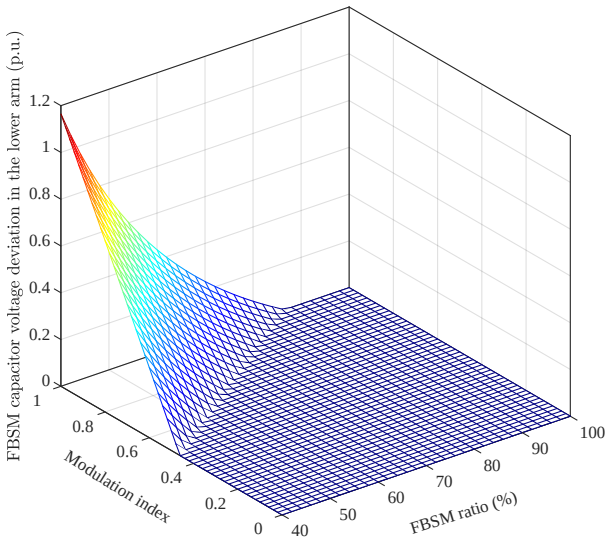


Fig. 7. Overvoltage level in the lower arms of the MMC with hybrid SMs.

Since the post-fault valve-side ac voltage in faulted phase a is zero, the FBSM capacitor C_{la} is not charged ($Loop4l$):

$$\Delta V_{Cla,hyb}^{FB} = 0. \tag{35}$$

However, the FBSM capacitor will be charged (36) in non-faulted phases b and c ($Loop5l$, $Loop6l$) if the used number of FBSMs in each arm is less than $0.866 \cdot m \cdot N_t$ ($N_{FB} < N_{FB}^{\min}$), while the FBSM capacitor will remain at the pre-fault voltage level if $N_{FB} \geq N_{FB}^{\min}$ (37).

$$\begin{cases} \Delta V_{Clb,hyb}^{FB} = \max |u'_{vb,hyb}|/N_{FB} - V_C \\ \Delta V_{Clc,hyb}^{FB} = \max |u'_{vc,hyb}|/N_{FB} - V_C \end{cases}, \quad N_{FB} < N_{FB}^{\min} \tag{36}$$

$$\Delta V_{Clb,hyb}^{FB} = \Delta V_{Clc,hyb}^{FB} = 0, \quad N_{FB} \geq N_{FB}^{\min} \tag{37}$$

To describe the overvoltage level in the lower arms of the MMC with hybrid SMs, (38) is derived by combining (34), (36) and (37).

$$\begin{cases} \dfrac{\Delta V_{Clx',hyb}^{FB}}{V_C} = \dfrac{0.866 \cdot m}{N_{FB}/N_t} - 1, \quad N_{FB} < N_{FB}^{\min} \\ \dfrac{\Delta V_{Clx',hyb}^{FB}}{V_C} = 0, \quad N_{FB} \geq N_{FB}^{\min} \end{cases} \quad (x' = b, c) \tag{38}$$

It shows the relationship between the post-fault FBSM capacitor voltage deviation (p.u. value) in the lower arms of the two non-faulted phases and the modulation index, which is also depicted in Fig. 7.

B. Upper Arm Post-fault Equivalent Circuit

Fig. 5(b) shows the post-fault equivalent upper arm circuit for the MMC with FBSMs or hybrid SMs. This circuit is similar to the equivalent upper arm circuit for the MMC with HBSMs, as all HBSM and FBSM capacitors (C_{ua}, C_{ub}, C_{uc}) are charged through $Loop4u$, $Loop5u$ and $Loop6u$ following converter blocking; (21) is also satisfied. However, the post-fault valve-side voltage is determined by (30), which indicates that the post-fault valve-side voltage for the MMC with FBSMs or hybrid SMs is higher than that for the MMC with HBSMs ($\sqrt{2}U_{v,line} > |\tilde{U}_{vb}|$ or $|\tilde{U}_{vc}|$ in (23)). When the SM capacitor charging process is complete, all upper arm diodes are reverse biased and the SM capacitor voltage deviation in each upper arm reaches:

$$\begin{cases} \Delta V_{Cua,fb(hyb)} = \max |u'_{va,fb(hyb)}|/N_t = 0 \\ \Delta V_{Cub,fb(hyb)} = \max |u'_{vb,fb(hyb)}|/N_t = \sqrt{2}U_{v,line}/N_t \\ \Delta V_{Cuc,fb(hyb)} = \max |u'_{vc,fb(hyb)}|/N_t = \sqrt{2}U_{v,line}/N_t \end{cases}. \tag{39}$$

V. Discussion on Resistor Effects & Varying Fault-Grounding Impedance

The presence of grounding resistors (dc-grounding resistor, fault-grounding resistor) and system resistance (MMC arm resistance, ac grid resistance) introduces additional dynamic components to the expressions for post-fault voltage and current. This significantly complicates the analytical formulations due to the inclusion of complex, multiple time-scale decaying components. In addition, the fault-grounding impedance could vary with time that the grounding resistance or inductance is not constant, with zero grounding impedance representing the worst-case scenario.

A. DC-Grounding and Fault-Grounding Resistor Effects

When adopting resistive dc-grounding or fault-grounding methods, the proposed calculation model for the FBSM or hybrid SM configurations remains effective, as the upper and lower arm currents reduce to zero, resulting in the same valve-side voltage change as (30).

For the HBSM configuration, the resistive grounding affects the analysis in Section III due to the continuous current flowing paths in the lower arms, introducing damped oscillations and exponentially decaying terms into the post-fault voltage and current expressions. However, a low-resistance dc-grounding method is preferred in practical MMC-HVDC systems to minimize power losses [15], rendering the analysis based on the solid dc-grounding assumption applicable to such scenarios. Moreover, although the resistive fault-grounding method is not explicitly considered in the analysis for the HBSM configuration, the proposed calculation models remain valid for the most severe scenario of zero or very low resistance.

B. System Resistance Effects

In an MMC-HVDC system, the system resistance (MMC arm and ac grid resistance) is much smaller than the inductive reactance [25]. Therefore, the post-fault performance of the MMC remains similar, regardless of whether the system resistance is included. It should be mentioned that the lower arm currents in the MMC with HBSMs will be gradually decreased to zero following the converter blocking if the lower arm resistors are considered:

$$\tilde{I}_{loa} = I_{loa,hb}^{blk} \cdot e^{-\dfrac{R_{arm} \cdot t}{L_{arm}}} \to 0 \tag{40}$$

in (16). Although the upper arm currents in the MMC with HBSMs and all arm currents in the MMC with FBSMs or hybrid SMs are forced to decrease to zero due to the CEMF

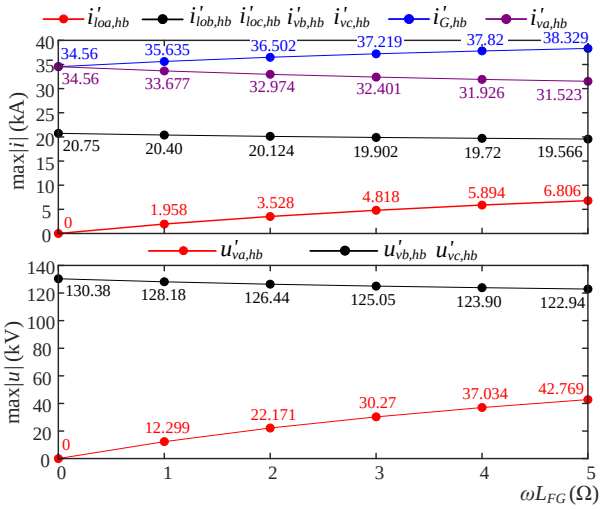


Fig. 8. Post-fault steady-state absolute peak values of lower arm currents, grounding point current, and valve-side currents/voltages with increasing fault-grounding reactance for the HBSM configuration.

generated by the SM capacitors, the arm resistors can suppress the transient current spikes and facilitate a faster current reduction.

C. Varying Fault-Grounding Impedance

For the FBSM and hybrid SM configurations, the time-varying fault-grounding impedance affects only the transient performance, with the post-fault valve-side phase voltage eventually transitioning to the line voltage as (30) when no current flows through the upper/lower arms.

However, the difference in impedance values of the bipolar MMC with HBSMs affects the post-fault steady-state performance. For the inductive fault-grounding, the analysis in Section III for the HBSM configuration is still applicable. Assuming a zero dc-grounding inductance ($L_{DG} = 0$), Fig. 8 shows the changes in steady-state peak values of lower arm currents $i'_{lo,hb}$, grounding point current $i'_{G,hb}$, valve-side currents/voltages $i'_{v,hb}, u'_{v,hb}$ with fault-grounding reactance ωL_{FG} increasing from 0 to 5 Ω (1 Ω step), by replacing corresponding parameters from Tables I and II into (14), (15), (18) and (20). For the varying resistive fault-grounding, the variation trends of $i'_{lo,hb}$, $i'_{G,hb}$, $i'_{v,hb}$, and $u'_{v,hb}$ are consistent with those obtained for inductive fault-grounding as the grounding resistance increases, even though the expressions cannot be directly obtained from the analysis in Section III. In addition, for both resistive and inductive fault-grounding methods, the post-fault arm voltage and the SM capacitor voltage deviation for the upper arm of the faulted phase a are:

$$\begin{cases} u_{upa,hb} = -u'_{va,hb} + V_{dc} \\ \Delta V_{Cua,hb} = \max|u'_{va,hb}|/N_t = |\tilde{U}_{va}|/N_t > 0 \end{cases}. \quad (41)$$

It is important to note that the proposed calculation models are not suitable for time-sequence analysis involving time-varying fault-grounding impedance. However, they can be used to describe the steady-state post-fault system behaviours under fixed system parameters, such as a constant fault-grounding inductance.

VI. Simulation Verification

Multiple bipolar MMC-HVDC systems are implemented in PSCAD/EMTDC, as shown in Fig. 9, to verify the accuracy of the proposed analytical calculation models. Three SM configurations are adopted, including 1) MMC with HBSMs, 2) MMC with FBSMs, and 3) MMC with hybrid SMs where 15 FBSMs ($N_{FB} \approx 0.433mN_t$) and 30 FBSMs ($N_{FB} \approx 0.866mN_t$) are used in each arm. Table I lists the detailed system parameters, derived from the Zhangbei dc project [4], considering the three SM configurations. Although actual MMC projects involve hundreds of SMs in each arm (e.g. 250 SMs with nominal capacitor voltage of 2 kV), 40 SMs are used per arm in the PSCAD simulation to accelerate the simulation speed. The total arm energy remains consistent, and this choice does not compromise the accuracy or reliability of the results.

In the bipolar MMC-HVDC system, the P_{ac}/Q_{ac} controlled MMC1P and MMC1N operate as rectifier stations, delivering power to MMC2P and MMC2N at the inverter side, which control the dc voltage and ac reactive power (V_{dc}/Q_{ac}). If a valve-side SPG occurs in the V_{dc}-controlled MMC operating as an inverter station, the dc voltage will continuously increase, leading to sustained SM capacitor charging in the upper arms due to the uninterrupted delivery from the P_{ac}-controlled MMC without converter blocking. To simulate the most severe upper arm overvoltage (SM capacitor charging), a valve-side SPG fault is set in phase a at $t_0 = 1$ s with a 0.001 Ω grounding resistance in the V_{dc}/Q_{ac}-controlled MMC2P (inverter side). Moreover, all MMCs in the bipolar system are blocked when any arm currents exceed 4.5 kA (1.5 times the dc current) following the fault.

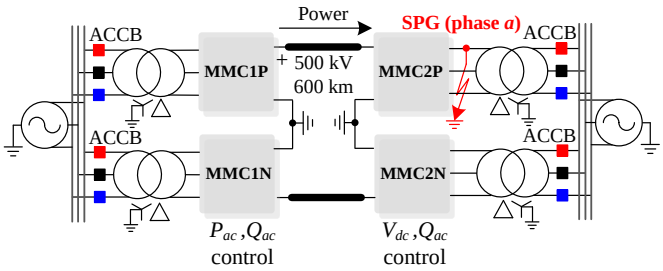


Fig. 9. Bipolar MMC-HVDC test system.

A. MMC with HBSMs

In the equivalent circuits used for the upper and lower arms of the MMC with HBSMs (Fig. 3), the secondary-side phase/line voltage $\tilde{U}_{Tx2}$, arm reactance X_{arm} and equivalent ac reactance $X_{v,eq}$ are first derived and listed in Table II. These values can also be used for analysis in the other two SM configurations.

The lower arm/valve-side current vectors and valve-side voltage vectors can be obtained by solving (16) and (17) (solid dc-grounding, $L_G = 0$) with the initial parameters provided in Table II. Therefore, the detailed expressions for the current and voltage in the upper and lower arms, as well as on the valve-side, can be obtained. Moreover, the calculation of grid-side current follows (28) or (28) for a Ynd1 or Ynd11 transformer

TABLE I
SYSTEM PARAMETERS OF THE MMC-HVDC SYSTEM.

Parameters	Config. 1	Config. 2	Config. 3
MMC power rating P (MW)	1500	1500	1500
Rated dc voltage V_{dc} (kV)	±500	±500	±500
Transf. ratio k_T (kV/kV)	230/260.26	230/260.26	230/260.26
Transf. leakage reactance $X_{Lt,p.u.}$	0.15	0.15	0.15
Transf. wiring connection	Ynd1 or Ynd11	Ynd11	Ynd11
Number of SMs in each arm N_t	40 40 HBSMs	40 15/30 FBSMs	40 40 FBSMs
SM capacitance C_{eq} (mF)	2.4	2.4	2.4
Modulation index m	0.85	0.85	0.85
Arm inductance L_{arm} (H)	0.04	0.04	0.04
Grid-side inductance L_g (H)	0.011	0.011	0.011
Transmission line parameters			
Line type	Overhead line (OHL) - Frequency dependent model		
Length of OHL (km)	600		
Line resistance (Ω/km)	0.00996		

TABLE II
INITIAL PARAMETERS IN THE EQUIVALENT UPPER/LOWER CIRCUITS.

Parameters	Values
Secondary-side phase/line voltage (kV)*	$\tilde{U}_{Ta2} = 368.06\angle 30°$ $\tilde{U}_{Tb2} = 368.06\angle -90°$ $\tilde{U}_{Tc2} = 368.06\angle 150°$
Arm reactance (Ω)	12.5664
Equivalent ac reactance (Ω)	11.1984

*: Ynd11 transformer wiring connection, and $\tilde{U}_{Ta2} = 368.06\angle -30°$, $\tilde{U}_{Tb2} = 368.06\angle -150°$, $\tilde{U}_{Tc2} = 368.06\angle 90°$ for the Ynd1 wiring connection.

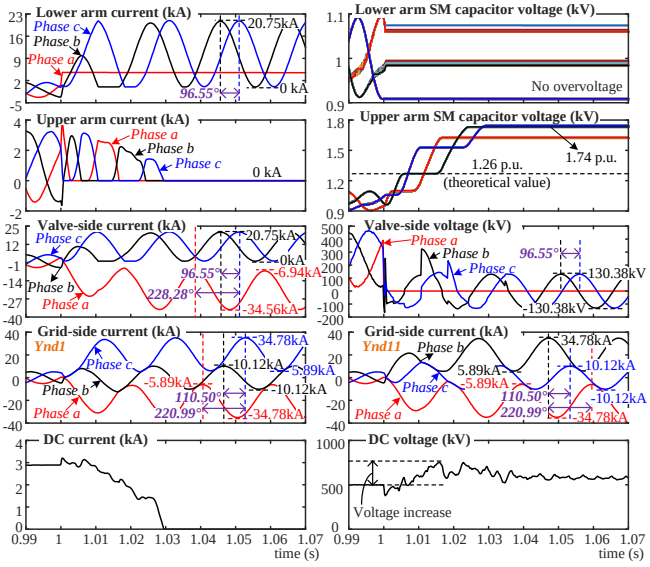


Fig. 10. Simulation results of the MMC with HBSMs under the valve-side SPG fault.

connection. The previous analysis also indicates the capacitor voltage deviation in the upper arms of non-faulted phases b and c will at least reach to 3.26 kV (0.26 p.u.). Fig. 10 shows the simulation results of the MMC with HBSMs under the valve-side SPG fault. Although the upper arm capacitor voltage reaches 1.74 p.u. in simulation due to the transient dc voltage increase, the steady-state results of the remaining parameters align with the calculated values listed in Table III.

TABLE III
CALCULATION RESULTS FOR THE MMC WITH HBSMS.

Parameters	Values
Lower arm current (kA)	$i'_{loa,hb} = I^{blk}_{loa,hb} = 0$, if arm resistor is considered $i'_{lob,hb} = 10.375\sin(\omega t + 18.277°) + 10.375$ $i'_{loc,hb} = 10.375\sin(\omega t - 78.277°) + 10.375$
Lower arm voltage (kV)	$u_{loa,hb} = u_{lob,hb} = u_{loc,hb} = 0$
Upper arm current (kA)	$i'_{loa,hb} = i'_{lob,hb} = i'_{loc,hb} = 0$
Upper arm voltage (kV)	$u_{upa,hb} = 500$ $u_{upb,hb} = 500 - u'_{vb,hb}$ $u_{upc,hb} = 500 - u'_{vc,hb}$
Upper arm capacitor voltage deviation (kV)	$\Delta V_{Cua,hb} = 0$ $\Delta V_{Cub,hb} = 3.26$ (0.26 p.u.) $\Delta V_{Cuc,hb} = 3.26$ (0.26 p.u.)
Valve-side current (kA)	$i'_{va,hb} = -13.810\sin(\omega t - 30°) - 20.75$ $i'_{vb,hb} = 10.375\sin(\omega t + 18.277°) + 10.375$ $i'_{vc,hb} = 10.375\sin(\omega t - 78.277°) + 10.375$
Valve-side voltage (kV)	$u'_{va,hb} = 0$ $u'_{vb,hb} = 130.38\sin(\omega t + 108.277°)$ $u'_{vc,hb} = 130.38\sin(\omega t + 11.723°)$
Grid-side current (kA) Ynd1	$i'_{ga,hb} = -14.448\sin(\omega t - 9.503°) - 20.334$ $i'_{gb,hb} = 10.118\sin(\omega t + 60°)$ $i'_{gc,hb} = 14.448\sin(\omega t - 50.497°) + 20.334$
Grid-side current (kA) Ynd11	$i'_{ga,hb} = -14.448\sin(\omega t + 9.503°) - 20.334$ $i'_{gb,hb} = 14.448\sin(\omega t + 50.497°) + 20.334$ $i'_{gc,hb} = 10.118\sin(\omega t - 60°)$

B. MMC with FBSMs and Hybrid SMs

Using the equivalent circuits (Fig. 5) for the upper and lower arms of the MMC with FBSMs or hybrid SMs, the steady-state system parameters of the MMC following the valve-side SPG fault are obtained and listed in Table IV. Since the upper and lower arm capacitors can provide CEMF following converter blocking to extinguish the fault currents in the converter arms, the arm currents and valve/grid-side ac currents gradually decrease to zero. The current valve-side ac voltage is determined by (30), with the magnitude in non-faulted phases being larger than that of the MMC with HBSMs (368.06 kV>130.38 kV).

The upper arm overvoltage occurs in both the MMC with FBSMs (Fig. 11) and hybrid SMs (Figs. 12 and 13). For both the MMC with FBSMs and the MMC with hybrid SMs using 30 FBSMs per arm, the upper arm voltage is 1.736 p.u. in calculation and 1.77 p.u. in simulation as the transient increase of the dc voltage, while the upper arm voltage is increased to 2.1 p.u. in simulation when 15 FBSMs are used in each arm. In addition, the lower arm overvoltage is present in the MMC with hybrid SMs using 15 FBSMs per arm and the calculated overvoltage level (1.96 p.u.) agrees with the simulation result, due to no dc voltage deviation in the dc-grounding point.

C. Influence of DC-grounding Methods and System Resistors

To demonstrate the applicability of the proposed analytical calculation models, both inductive and resistive dc-grounding methods are considered, and the influence of the arm and ac grid resistance is also discussed by using the HBSM configuration. The comparison between the calculation (dashed lines) and simulation (solid lines) results for the inductive

TABLE IV
CALCULATION RESULTS FOR THE MMC WITH FBSMS AND HYBRID SMS.

Parameters	Values
Lower arm current (kA)	$i'_{loa,fb(hyb)} = i'_{lob,fb(hyb)} = i'_{loc,fb(hyb)} = 0$
Lower arm voltage (kV)	$u_{loa,fb(hyb)} = 0$ $u_{lob,fb(hyb)} = u'_{vb,fb(hyb)}$ $u_{loc,fb(hyb)} = u'_{vc,fb(hyb)}$
Lower arm capacitor voltage deviation (kV) −hybrid SMs	$\Delta V^{FB}_{Cla,hyb} = 0$ $\Delta V^{FB}_{Clb,hyb} = 12.04$ (0.963 p.u.) $\Delta V^{FB}_{Clc,hyb} = 12.04$ (0.963 p.u.)
Upper arm current (kA)	$i'_{loa,fb(hyb)} = i'_{lob,fb(hyb)} = i'_{loc,fb(hyb)} = 0$
Upper arm voltage (kV)	$u_{upa,fb(hyb)} = 500$ $u_{upb,fb(hyb)} = 500 - u'_{vb,fb(hyb)}$ $u_{upc,fb(hyb)} = 500 - u'_{vc,fb(hyb)}$
Upper arm capacitor voltage deviation (kV)	$\Delta V_{Cua,fb(hyb)} = 0$ $\Delta V_{Cub,fb(hyb)} = 9.20$ (0.736 p.u.) $\Delta V_{Cuc,fb(hyb)} = 9.20$ (0.736 p.u.)
Upper arm current (kA)	$i'_{loa,fb(hyb)} = i'_{lob,fb(hyb)} = i'_{loc,fb(hyb)} = 0$
Valve-side voltage (kV)	$u'_{va,fb(hyb)} = 0$ $u'_{vb,fb(hyb)} = 368.06\sin(\omega t - 90°)$ $u'_{vc,fb(hyb)} = 368.06\sin(\omega t - 150°)$

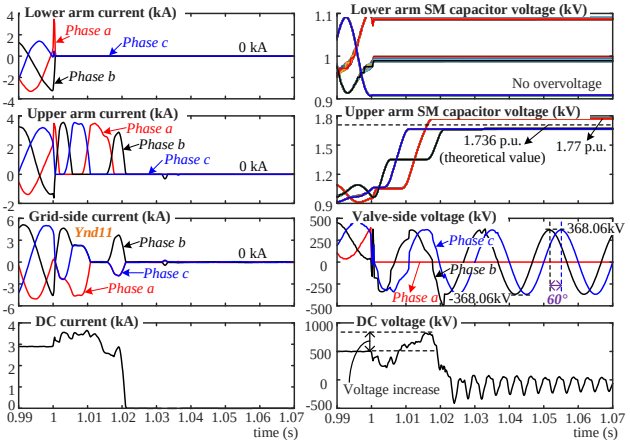


Fig. 11. Simulation results of the MMC with FBSMs.

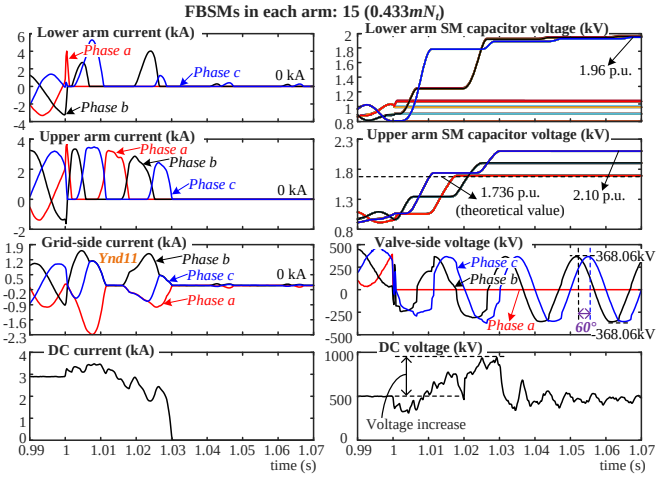


Fig. 12. Simulation results of the MMC with hybrid SMs (15 FBSMs in each arm - $N_{FB} \approx 0.433mN_t$).

($X_L = 2\ \Omega$) and resistive ($X_R = 2\ \Omega$) dc-grounding methods is shown in Fig. 14(a) and Fig. 14(b), respectively.

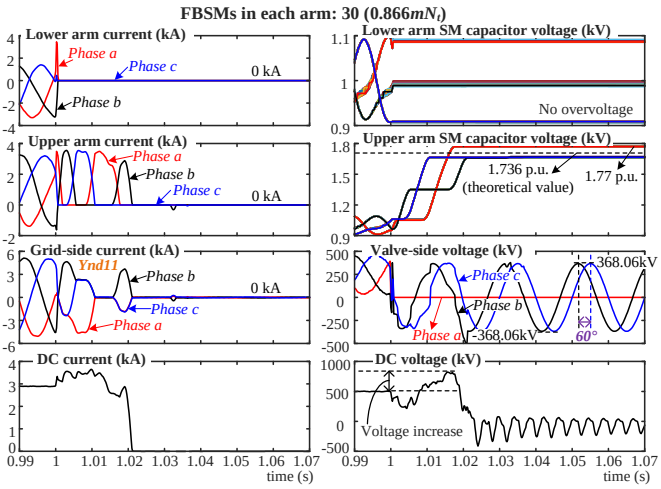


Fig. 13. Simulation results of the MMC with hybrid SMs (30 FBSMs in each arm - $N_{FB} \approx 0.866mN_t$).

The results demonstrate that the proposed calculation model can accurately describe the system behaviours (14), (15) of a bipolar MMC with inductive dc-grounding method after a valve-side SPG fault. As discussed in Section V, the resistive dc-grounding introduces complex time-scale decaying components to the steady-state voltage and current expressions of the HBSM configuration, significantly complicating the analytical analysis. However, high resistance is not expected in actual MMC-HVDC systems, as it will lead to additional steady-state power losses [15]. Therefore, the calculation for solid dc-grounding method can still be used to approximately model a resistive dc-grounding bipolar MMC-HVDC system with low grounding impedance.

The presence of grounding resistors (dc-grounding resistor, fault-grounding resistor) and system resistance (MMC arm resistance, ac grid resistance) introduces additional dynamic components to the expressions for post-fault voltage and current. This significantly complicates the analytical formulations due to the inclusion of complex, multiple time-scale decaying components.

In addition, the system resistance (MMC arm and ac grid resistance) is much smaller than the inductive reactance in an MMC-HVDC system [25], resulting in a similar post-fault system performance whether or not the system resistors are included. Fig. 15 demonstrates the results of calculation and simulation comparisons, confirming the proposed calculation model remains effective with minimal errors when system resistors are included (arm resistance R_{arm} is 0.1 Ω and ac grid resistance R_g is 0.351 Ω in simulation).

VII. CONCLUSION

Valve-side SPG faults will lead to significant overcurrent and overvoltage issues in a bipolar MMC-HVDC system. Therefore, it is essential to evaluate the detailed post-fault overcurrent and overvoltage levels for the adoption of passive and active protection methods, as well as the design and implementation of effective relay protection schemes. Two analytical calculation models are proposed in this paper to describe the post-fault system behaviours for the bipolar

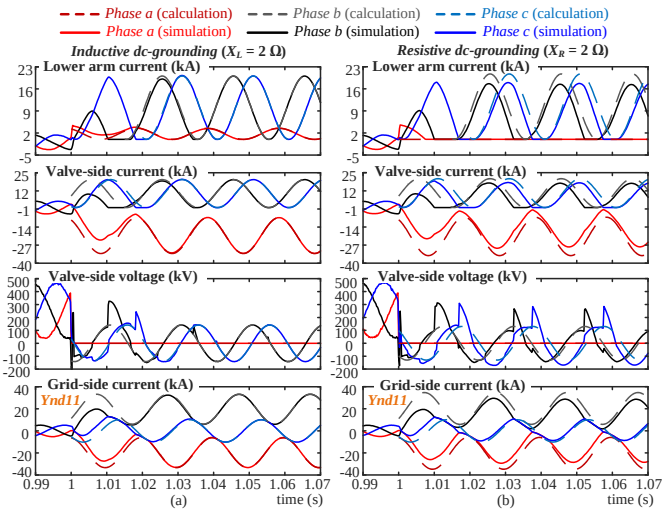


Fig. 14. Comparison between the calculation and simulation results for different dc-grounding methods: (a) inductive dc-grounding, and (b) resistive dc-grounding.

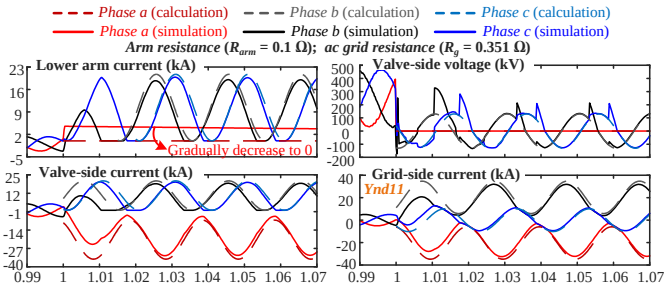


Fig. 15. Comparison between the calculation and simulation results with the inclusion of arm and ac grid resistors.

MMC-HVDC systems with 1) HBSMs, and 2) FBSMs or 3) hybrid SMs with different FBSM ratios in each arm, under a valve-side SPG fault following the converter blocking.

Using the post-fault equivalent upper and lower arm circuits of each calculation model, accurate expressions of the post-fault voltages and currents in MMC arms, valve- and grid-sides are derived for solid and inductive dc-grounding/fault-grounding methods. To be specific, the following conclusions can be obtained:

1) The valve-side phase voltages transition into the line voltages across all SM configurations, with peak values of $\sqrt{2}U_{v,line}$ for the FBSM and hybrid SM configurations. For the HBSM configuration, the peak values are reduced, influenced by the ac equivalent inductance $L_{v,eq}$, arm inductance L_{arm}, dc-grounding inductance L_{DG}, and fault-grounding inductance L_{FG}.
2) The valve-side ac currents for the FBSM and hybrid SM configurations gradually decrease to zero following the converter blocking. However, dc-offsets are present in the valve-side ac currents for the HBSM configuration (with a $\tilde{I}_{lo}$ offset for the currents of the two non-faulted phases), further leading to non-zero-crossings in the grid-side currents.
3) The upper arm currents decrease to zero for all SM configurations, and the lower arm currents also reduce to zero in the FBSM and hybrid SM configurations. Nevertheless, the lower arm currents of the two non-faulted phases for the HBSM configuration are equal to the valve-side ac currents, while the lower arm current of the faulted phase decreases exponentially, following a decay characterised by $e^{-\frac{R_{arm}}{L_{arm}}\cdot t}$ when the arm resistor is considered.
4) The upper arm voltages for all SM configurations ($u_{upx} = -u'_{vx} + V_{dc}$) are influenced by the dc voltage deviation and the valve-side ac voltage change, and all upper arm SM capacitors are overcharged to $(\max|u'_{vx}| + V_{dc})/N_t$. In addition, the lower arm voltages for the HBSM configuration decrease to zero following the converter blocking, and the lower arm SM capacitors are bypassed. However, the lower arm voltages of the FBSM and hybrid SM configurations ($u_{lox,fb(hyb)} = u'_{vx,fb(hyb)}$) are impacted by the valve-side ac voltage change, while the lower arm FBSM capacitors for the hybrid SM configuration are overcharged to $\max|u'_{vx,hyb}|/N_{FB}$ if the ratio of FBSMs in each arm is less than $0.866m$ (m refers to the MMC modulation index).
5) The proposed analytical calculation models can also approximate post-fault system behaviours for bipolar MMCs with low dc-grounding and fault-grounding resistance, as well as scenarios involving MMC arm and grid-side resistors, demonstrating their applicability across a wide range of practical conditions.

Future work could investigate the detailed post-fault dynamic response of the bipolar MMC-HVDC systems, and extend the model for real-time analysis and integration into relay protection systems.

REFERENCES

[1] P. Sun, Y. Tian, J. Pou, and G. Konstantinou, "Beyond the MMC: Extended modular multilevel converter topologies and applications," *IEEE Open J. Power Electron.*, vol. 3, pp. 317–333, May 2022.

[2] P. Sun, F. Arrano-Vargas, H. R. Wickramasinghe, and G. Konstantinou, "Benchmark models for HVDC systems and DC-grid studies," in *ICPES 2019, Perth, WA*, Dec. 2019.

[3] X. Guo, M. Deng, and K. Wang, "Characteristics and performance of xiamen VSC-HVDC transmission demonstration project," in *2016 IEEE International Conference on High Voltage Engineering and Application (ICHVE)*, Sep. 2016, pp. 1–4.

[4] H. Pang and X. Wei, "Research on Key Technology and Equipment for Zhangbei 500kV DC Grid," in *2018 Int. Power Electron. Conf.*, May 2018, pp. 2343–2351.

[5] G. Li, J. Liang, F. Ma, C. E. Ugalde-Loo, and H. Liang, "Analysis of single-phase-to-ground faults at the valve-side of HB-MMCs in HVDC systems," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2444–2453, Mar. 2019.

[6] W. Liu, J. Yu, G. Li, J. Liang, C. E. Ugalde-Loo, and A. Moon, "Analysis and protection of converter-side AC faults in a cascaded converter-based MVDC link: ANGLE-DC project," *IEEE Transactions on Smart Grid*, vol. 13, no. 5, pp. 4046–4056, Sep. 2022.

[7] H. Zhou, W. Yao, K. Sun, X. Ai, J. Wen, and S. Cheng, "Characteristic investigation and overvoltage suppression of MMC-HVDC integrated offshore wind farms under onshore valve-side SPG fault," *IEEE Trans. Power Syst.*, vol. 39, no. 1, pp. 1346–1359, Jan. 2024.

[8] H. Li, F. Deng, J. Tian, Y. Lu, G. Li, and J. Lin, "Grounded thyristor loop-based hybrid MMCs for valve-side single-phase-to-ground faults in bipolar HVdc systems," *IEEE Trans. Power Electron.*, vol. 39, no. 5, pp. 6298–6311, May 2024.

[9] P. Sun, G. Li, H. Wang, J. Liang, and G. Konstantinou, "Valve-side single-phase-to-ground fault analysis in bipolar MMC-HVDC systems with hybrid SMs," *IEEE Trans. Power Del.*, vol. 39, no. 5, pp. 3001–3004, Oct. 2024.

[10] G. Li, J. Liang, C. E. Ugalde-Loo, F. Ma, H. Liang, and Z. Song, "Protection for submodule overvoltage caused by converter valve-side single-phase-to-ground faults in FB-MMC based bipolar HVDC systems," *IEEE Trans. Power Del.*, vol. 35, no. 6, pp. 2641–2650, Dec. 2020.

[11] W. Yang, Q. Song, H. Rao, S. Xu, and Z. Zhu, "Converter side phase-to-ground fault protection of full-bridge modular multilevel converter-based bipolar HVDC," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, Oct. 2017, pp. 185–189.

[12] G. Li, W. Liu, T. Joseph, J. Liang, and Z. Song, "Double-thyristor-based protection for valve-side single-phase-to-ground faults in HB-MMC-based bipolar HVDC systems," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5810–5815, Jul. 2020.

[13] W. Liu, G. Li, J. Liang, C. E. Ugalde-Loo, C. Li, and X. Guillaud, "Protection of single-phase fault at the transformer valve side of FB-MMC-based bipolar HVdc systems," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8416–8427, Oct. 2020.

[14] X. Liu, G. Li, T. Zheng, X. Yang, and J. M. Guerrero, "Thyristor-pair- and damping-submodule-based protection against valve-side single-phase-to-ground faults in MMC-MTDC systems," *IEEE Trans. Power Del.*, vol. 37, no. 4, pp. 3257–3269, Aug. 2022.

[15] W. Leterme, P. Tielens, S. De Boeck, and D. Van Hertem, "Overview of grounding and configuration options for meshed HVDC grids," *IEEE Trans. Power Del.*, vol. 29, no. 6, pp. 2467–2475, Sep. 2014.

[16] P. Sun, H. R. Wickramasinghe, M. Khalid, and G. Konstantinou, "AC/DC fault handling and expanded DC power flow expression in hybrid multi-converter DC grids," *Int. J. of Elect. Power & Energy Syst.*, vol. 141, p. 107989, Oct. 2022.

[17] P. Huang and L. Vanfretti, "Adaptive damping control of MMC to suppress high-frequency resonance," *IEEE Trans. Ind. Appl.*, vol. 59, no. 6, pp. 7224–7237, Nov.-Dec. 2023.

[18] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.

[19] R. Li, J. E. Fletcher, L. Xu, and B. W. Williams, "Enhanced flat-topped modulation for MMC control in HVDC transmission systems," *IEEE Trans. Power Del.*, vol. 32, no. 1, pp. 152–161, May 2017.

[20] Y. Yuefeng, Y. Jie, H. Zhiyuan, and W. Haitian, "Research on control and protection system for shanghai nanhui MMC VSC-HVDC demonstration project," in *10th IET International Conference on AC and DC Power Transmission (ACDC 2012)*, Dec. 2012, pp. 1–6.

[21] W. Huang, Y. Lu, X. Li, Y. Huang, S. Xu, M. Li, and T. Liu, "A calculation method for maximum steady-state loss of VSC-HVDC grounding resistor in luxi back-back HVDC interconnector," in *12th IET International Conference on AC and DC Power Transmission (ACDC 2016)*, May 2016, pp. 1–5.

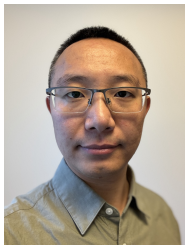
[22] J. Li, B. Zhu, Y. Guo, Z. Liang, H. Wu, and H. Liu, "The simulation of kunliulong flexible DC project with single station operation and out of operation," in *2021 IEEE/IAS Industrial and Commercial Power System Asia (I&CPS Asia)*, Jul. 2021, pp. 1028–1034.

[23] G. E. Chatzarakis, M. D. Tortoreli, and A. D. Tziolas, "Fundamental loop-current method using 'virtual voltage sources' technique for special cases," *Int. J. of Elect. Eng. & Edu.*, vol. 40, no. 3, pp. 188–207, Jul. 2003.

[24] M. A. Salam, *Transformer: Principles and Practices*. Singapore: Springer Singapore, Feb. 2020, pp. 45–109.

[25] J. B. Soomro, F. Akhtar, R. Hussain, J. Ahmed Ansari, and H. M. Munir, "A detailed review of MMC circuit topologies and modelling issues," *Int. Trans. Elect. Energy Syst.*, vol. 2022, no. 1, p. 8734010, Mar. 2022.

Pingyang Sun (Graduate Student Member, IEEE) received the B.Eng. degree in Electrical Engineering from Qilu University of Technology (Shandong Academy of Sciences), Jinan, China, in 2018, the M.Phil degree in electrical engineering at the School of Electrical engineering and Telecommunications, the University of New South Wales (UNSW), Sydney, Australia, in 2021. He is currently pursuing his Ph.D. degree at UNSW. He was an exchange student at the School of Electronics and Information, Kyung Hee University (KHU), Suwon, Korea, in 2017, and a guest Ph.D student at the Technical University of Denmark (DTU), Ballerup, Denmark, in 2024. His research interests include system modeling and benchmarking from MVDC to HVDC systems.



Gen Li (Senior Member, IEEE) received the B.Eng. degree in Electrical Engineering from Northeast Electric Power University, Jilin, China, in 2011, the M.Sc. degree in Power Engineering from Nanyang Technological University, Singapore, in 2013 and the Ph.D. degree in Electrical Engineering from Cardiff University, Cardiff, U.K., in 2018.

He is now an Associate Professor at Technical University of Denmark (DTU), Denmark. From 2013 to 2016, he has been a Marie Curie Early Stage Research Fellow funded by European Commission's MEDOW project. He has been a Visiting Researcher at China Electric Power Research Institute, China, at Elia, Belgium and at Toshiba International (Europe), U.K. He was a Research Associate at Cardiff University from 2018 to 2022. His research interests include control and protection of HV and MV DC technologies, offshore wind and offshore energy islands.

Dr. Li is a Chartered Engineer in the U.K., an IET Professional Registration Advisor, a Young Editorial Board Member of Applied Energy, an Associate Editor of the CSEE Journal of Power and Energy Systems and IET Energy Systems Integration, an Editorial Board Member of CIGRE ELECTRA and Global Energy Interconnection. He received the CIGRE NGN Significant Contribution Award in 2024 and the First CIGRE Thesis Award in 2018. He is now a Steering Committee Member of CIGRE Denmark NGN, a Member of CIGRE Working Group B4.96 and a Member of IEEE PELS Publicity Committee.

Hanwen Zhang (Graduate Student Member, IEEE) received the B.Eng. and M.Sc. degrees in Electrical Engineering from Northeast Electric Power University, Jilin, China, in 2017 and 2020, respectively. In 2018, he was a visiting student with the School of Engineering, Cardiff University, Cardiff, UK. Since 2021, he has been working toward the Ph.D. degree with AAU Energy, Aalborg University, Aalborg, Denmark. Since 2022, he has been involved in The European DEMOnstration Power Plant project as a Ph.D. student researcher, under the EUROfusion Consortium, Framework Programme 9 of the European Union. In 2023, he was a visiting Ph.D. student with the Department of Industrial Engineering, University of Rome "Tor Vergata", Rome, Italy. In 2024, he was a visiting Ph.D. student with Department of Engineering Technology and Didactics, Technical University of Denmark, Ballerup, Denmark. His research interests include DC microgrids, multiport DC/DC converters, DC circuit breakers, FACTS, and nuclear fusion power plant power systems.

Jun Liang (Fellow, IEEE) received the B.S. degree in electric power system and its automation from the Huazhong University of Science and Technology, Wuhan, China, in 1992 and the M.S. and Ph.D. degrees in electric power system and its automation from the China Electric Power Research Institute (CEPRI), Beijing, China, in 1995 and 1998, respectively.

From 1998 to 2001, he was a Senior Engineer with CEPRI. From 2001 to 2005, he was a Research Associate with Imperial College London, London, U.K. From 2005 to 2007, he was a Senior Lecturer with the University of Glamorgan. He is currently a Professor in power electronics with the School of Engineering, Cardiff University, Cardiff, U.K. He is the Coordinator and Scientist-in-Charge of two European Commission Marie-Curie Action ITN/ETN projects: MEDOW (€3.9M) and InnoDC (€3.9M). His research interests include HVDC, MVDC, FACTS, power system stability control, power electronics, and renewable power generation.

Dr. Liang is a Fellow of the Institution of Engineering and Technology. He is the Chair of IEEE U.K. and Ireland Power Electronics Chapter. He is an Editorial Board Member of CSEE JPES. He is an Editor for IEEE Transactions on Sustainable Energy.

Georgios Konstantinou (Senior Member, IEEE) received the B.Eng. degree in electrical and computer engineering from the Aristotle University of Thessaloniki, Thessaloniki, Greece, in 2007 and the Ph.D. degree in electrical engineering from UNSW Sydney (The University of New South Wales), Australia, in 2012. From 2013 to 2016, he was a Senior Research Associate with the University of New South Wales, Sydney, NSW, Australia, where he was part of the Australian Energy Research Institute. Since 2017, he has been with the School of Electrical Engineering and Telecommunications, UNSW Sydney, where he is currently an Associate Professor with the Energy Systems Research Group and the Real-time Simulations Laboratory (RTS@UNSW). He is an Associate Editor for IEEE Transactions on Power Electronics.