ADVANCED LOAD MODULATED POWER AMPLIFIERS FOR WIRELESS TELECOM APPLICATIONS

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Dedicated to the adventurous spirit and loving memory of Laura Tietz.

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ABSTRACT

This thesis demonstrates a design approach for load modulated RF power amplifiers based on the use of circuit simulation to provide comprehensive visibility into the true behaviors of current and voltage waveforms when they diverge from ideal theory. While RF circuit simulations are standard design tools, identifying and monitoring the numerous interactions of passive and active components as a design transitions from concept to manufacturable circuit remains challenging. This work presents measurement and display techniques to analyze a set of key performance indicators at all design stages of RF power amplifier design. The design approach framework is discussed and demonstrated through the analysis and design of Doherty Power Amplifiers as they make use of active load modulation. The Doherty architecture has been studied extensively since its initial conception in 1936 and is a frequent choice for 5G MIMO applications.

The Doherty power amplifier architecture uses one or more auxiliary transistors to generate synthetic load impedances at the output of the amplifiers that help maintain high efficiency even at reduced output power levels. This ability is compelling because it operates without external control circuitry or logic, making it ideal for modern communication signals, which often have high Peak-to-Average Power Ratios due to the need for high data rates within limited bandwidths.

Transistors exhibit non-linear and complex behaviors when driven by time-varying input signals. The simplifying assumptions of ideal Doherty amplifier design formulas are often invalidated by these non-linearities and the real-world characteristics of other components.

Acknowledging these complexities, a pragmatic design process for load-modulated amplifiers has been developed and tested using modern non-linear RF circuit simulators. This process begins by formalizing key Doherty architecture properties, creating systems to measure and evaluate them, and aligning the design process with these metrics. This approach ensures clarity as non-ideal components are integrated and complex behaviors result, providing measurable objectives throughout the design stages.

The fabricated 5G mid-band basestation amplifier operating between 3.4 and 3.8 GHz achieves a peak power of 46.25 dBm with an efficiency of 62.5 % at saturation and 48 % at the target average power level of 8.5 dB below peak. When driven with a 10 MHz bandwidth OFDM signal it delivers a 38 dBm average power output at 43 % efficiency and an ACLR of -51 dBc. Additionally, the design was implemented within a compact 56.1 x 43.5 mm total size. These performance results compare favorably with other designs in published literature, validating that the design process results in an effective design.

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ACRONYMS

4G	4th Generation Cellular Standard also known as LTE
5G	5th Generation Cellular Standard
ADS	Advanced Design System
ACLR	Adjacent Channel Leakage Ratio
AWGN	Additive White Gaussian Noise
AM	Amplitude Modulation
DPD	Digital Pre-Distortion
DUT	Device Under Test
EVM	Error Vector Magnitude
FEM	Finite Element Method
FET	Field Effect Transistor
FM	Frequency Modulation
FSK	Frequency-Shift Keying
FDMA	Frequency Division Multiple Access
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GMSK	Gaussian Minimum Shift Keying
HEMT	High Electron Mobility Transistor
OBO	Output power Back-Off
PAE	Power-Added Efficiency
PA	Power Amplifier
PAPR	Peak to Average Power Ratio
PCB	Printed Circuit Board
RRC	Root Raised Cosine

TDMA Time Division multiple Access

LTE Long Term Evolution

LMBA Load Modulated Balanced Amplifier

OFDM Orthogonal Frequency-Division Multiplexing

QAM Quadrature Amplitude Modulation

QPSK Quadrature Phase Shift Keying

1

INTRODUCTION

1.1 BACKGROUND

The Doherty radio frequency Power Amplifier architecture focused on by this thesis was developed in 1936, which remarkably surged in relevance again 88 years after its initial creation [1]. When William Doherty published his method for "varying circuit impedance over the modulation cycle" using a circuit architecture which soon bore his name, wireless telecommunications was in its infancy. Since then, analog broadcast communications and later digital duplex communications have changed nearly every aspect of society. The construction and improvement of telecommunications infrastructure has led to increased economic growth and development [2]. The methodology and technology of designing amplifiers has changed to meet the needs of evolving telecommunications systems.

Between 1890 and 1900, Reginald Fessenden developed an early form of continuous wave oscillator able to create a signal with energy focused on a single frequency [3]. By the end of 1906 he was able to transmit audio of both speech and music clearly enough to be understood [4]. This technique still used spark-gap

transmitters but at a much higher pulse rate than those used in radiotelegraphy. He and others advanced this technology over the next decade to become the early form of broadcast radio using Amplitude Modulation (AM) transmissions. Over 8 years, the invention and improvement of vacuum tube technology, starting with the thermionic triode in 1907, led to devices able to amplify the radio signals at both higher power and frequency than previously possible. In 1920 radio stations in Argentina, the United Kingdom, and United States were regularly broadcasting music, news, and voice as public and commercial services [5].

During the 1920s and 1930s in the United States, AM broadcast stations transmitted signals with powers up to 50,000 Watts at frequencies typically between 550 kHz and 1.35 MHz. These signals were typically direct AM or later Double Sideband AM with a suppressed carrier (DSB-SC). The output power of the radio signals varied depending on the loudness of the audio signals with peaks of over four times the average power. This difference, referred to as the Peak to Average Power Ratio (PAPR) became a key motivating factor in the development of novel RF power amplifier architectures during this time period for reasons explained in Section 2.1.7. Doherty's first commercial amplifier using the Doherty architecture had a saturated power of 50 000 W and was used by the AM broadcast station WHAS in Kentucky [6].

Morse code, a pulsed On-Off Keyed constant amplitude signal, was the earliest form of digital encoding of information in wireless communications. After Morse code, techniques used for sending images and videos via wired communication

were adapted to be carried (modulated) onto double and single sideband AM signals as seen with Radiofax, which continues to be used today to transmit weather data for maritime use. Analog frequency modulation was developed and spread rapidly during the first half of the 20th century [7].

The invention and rapid development of programmable electronic digital computers (Colossus 1943-1945) and transistors (Bell Labs 1947) created a use and demand for digital radio communications. Radio Relay systems which replaced wired telephone backbones started with Bell Labs' TDX experiments in 1947 [8]. Digital Radio Relay systems were first commercially used in 1968 in Japan [8]. These used 4 level Frequency-Shift Keying (FSK) in the 2 GHz band and with a capacity of 240 voice channels. Packet radio system experiments were done in the 1970s starting with ALOHAnet in 1970, and continued by SRI International, previously known as the Stanford Research Institute [9, 10].

The use of radio telecommunications for cellular networks started with trials in the late 1970s and early commercial networks started operating in 1979 (Japan Nippon Telegraph and Telephone) and 1981 (Nordic countries, NMT standard). These first generation (1G) networks used digital signaling and analog Frequency Modulation (FM) modulation for the audio. Figure 1.1 shows a variety of standards which have competed and evolved in the mobile market over time.

Cellular communications grew steadily to the present day with the dominant service becoming mobile broadband data to smartphones. An increasingly large percentage of connected subscribers are industrial and 'Internet of Things' devices

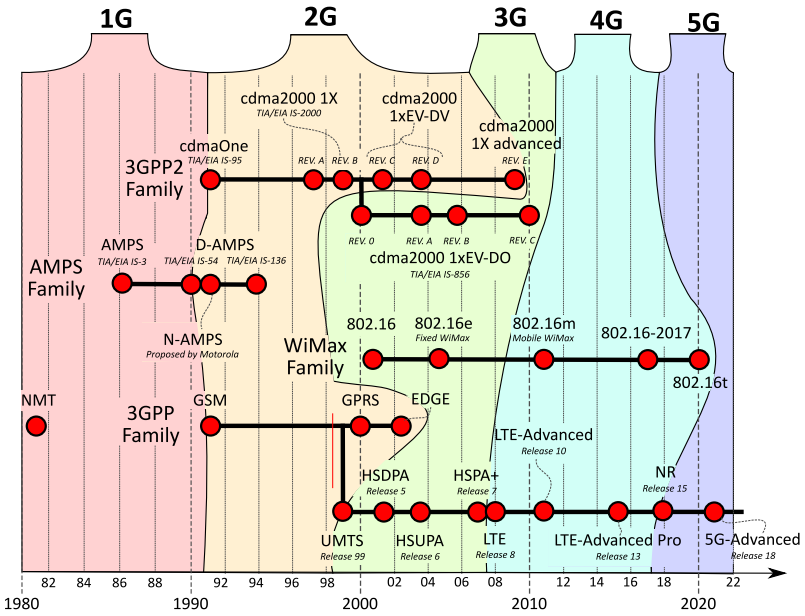


Figure 1.1: Timeline of Cellular Network Standards (reproduced from [11])

[12, 13]. Additionally, with the 4th Generation Cellular Standard also known as LTE (4G) and 5th Generation Cellular Standard (5G) standards able to deliver data rates and volumes competitive with standard DSL and broadband wired home internet services, the market for Fixed Wireless Access to cover the "last mile" of infrastructure to homes has grown.

5G is expected to have more subscribers than 4G by 2028, reaching 4.69 Billion subscribers [14]. Over the next 5 years, it is expected that the average mobile data subscriber will increase their usage from 21 GB to 56 GB per year. Combined with the growth in subscriber numbers, this means the total network traffic of 210 EB per month in 2023 will increase to 483 EB in 2028. This growing demand for data to be delivered at a higher speed and volume to more individual users has driven changes in the signal waveforms, with implications on the demands that power

amplifiers need to be designed for. Ericsson does not expect 6G to be commercial deployments to start until 2030 at least.

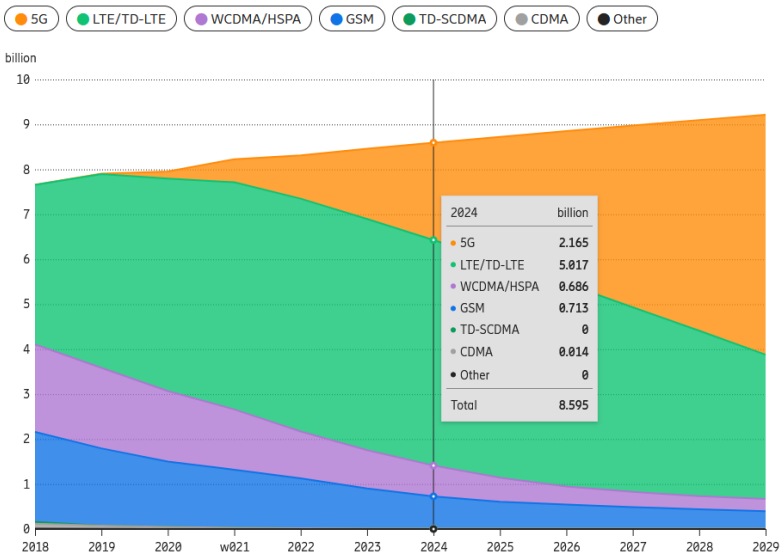


Figure 1.2: Growth and Distribution of Mobile Subscribers [14]

1.1.1 *Efficiency in Infrastructure*

The value of reducing energy consumption is broadly accepted in society but can be weighed more accurately in this circumstance by examining the scale and impact of energy usage in mobile network radios. It was estimated that 52 % of CO_2 emissions from the telecommunications sector in 2020 would be attributable to mobile networks, with fixed narrowband networks and fixed broadband networks leading to a further 20 % and 14 % respectively [16]. All three of these network types use Power Amplifiers (PAs) in the transmission of their signals so PA improvements would have a beneficial impact on all three, dependent on the modulation type in

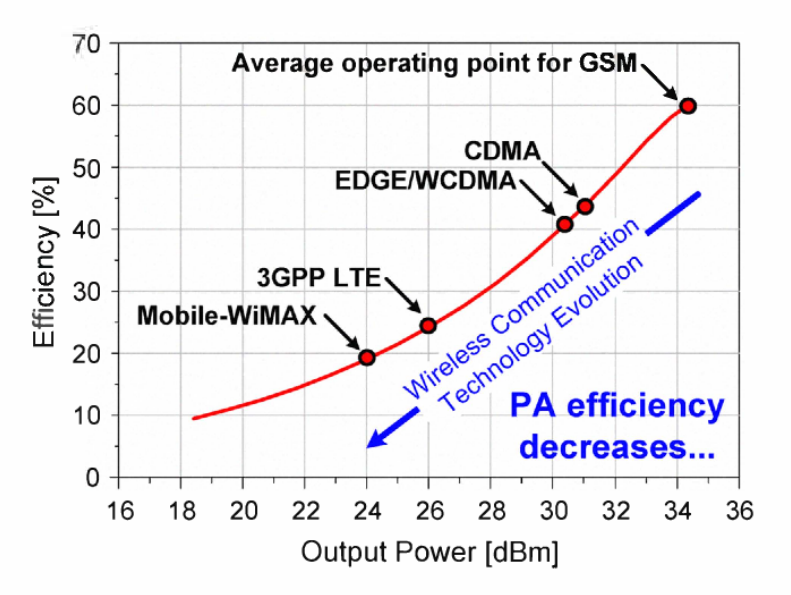


Figure 1.3: Basic PA efficiency impact (reproduced from [15])

use. As previously described, there is a strong link between the ability to transmit high rate data and waveforms with high PAPR. The energy consumption broken down by component shows 50 to 80 % of the usage in a radio base station is from the PA and associated feeder hardware [16]. Nokia provides a slightly different breakdown where the radio hardware consumes 64 % of the power used by the base station and highlights that additional power equal to 1.52 times the radio's usage is needed for cooling [17]. Improving the efficiency of the power amplifier can significantly reduce the cooling requirements and save additional capital and operating expenses.

1.1.2 *Modulation*

Modern wireless communications schemes use complex modulations with large amplitude dynamics in order to achieve higher data rates and more efficiently use the limited spectral resources. GSM uses Gaussian Minimum Shift Keying (GMSK) modulation, a 2-FSK scheme where the frequency shift is plus or minus 67.708 kHz and filtered with a Gaussian filter to reduce the occupied bandwidth. It has a data rate of 270.833 kbit/sec. GSM uses Time Division multiple Access (TDMA) to allocate data bandwidth to multiple users and pairs of frequency channels for uplink and downlink, a Frequency Division Multiple Access (FDMA) system. EDGE uses $3\pi/8$ 8-PSK which triples the physical data rate but is no longer a fully constant amplitude signal. It has a PAPR of 3.2 dB. For mobile base stations, Orthogonal Frequency-Division Multiplexing (OFDM) is the current standard, which results in waveforms with typical PAPR of around 8.5 dB for 4G Long Term Evolution (LTE) and up to 14 dB for 5G.

These modern communication waveforms contain amplitude variations in order to carry information content. This can be due to AM, Quadrature Amplitude Modulation (QAM), multi carrier modulation schemes such as OFDM, or multiple independent channels served by the same radio. The end result is that the average power of the signal can be much lower than the peak power required. Techniques such as Crest Factor Reduction reduce this issue, but at the cost of distorting the

signal and reducing its performance, measured by Bit Error Rate or Error Vector Magnitude (EVM).

1.1.3 *Motivation for non-zero PAPR*

The purpose of wireless communications is to move information between locations. Claude Shannon published a theory of noisy channel coding in 1948 which defined the theoretical bound on how many bits can be sent per second in a given bandwidth for a set signal power and Additive White Gaussian Noise (AWGN) level [18]. The limited nature of spectrum bandwidth and the demand for data exceeding the available capacity drives the need to use spectrum efficiently. The ITU published a list of use-cases for 5G technology including transportation, industrial automation, security and public safety, and healthcare, in addition to the common voice and data services used by individuals [19]. The allocation of spectrum to organizations and companies for use in telecommunications is often done at auctions run by national regulatory agencies, with a 2021 auction in the US for 280 MHz of spectrum between 3.7 and 3.98 GHz producing a net proceed of $81.1 Billion [20, 21]. Two other auctions around 3.45 GHz and 3.8 GHz raised $22.4 Billion and $4.5 Billion respectively.

The high value of spectrum bandwidth has driven innovation in the modulation schemes used in cellular communications to transport data more efficiently, approaching the "Shannon Limit" of the available bandwidths. The output power of a

transmitter will have a maximum possible value determined by hardware or legal limits. On a complex sample plane this power limitation will result in a circle of possible transmission states bounded by the maximum amplitude; a circle with a radius equal to the maximum power and encompassing all lower powers and all possible phase values.

$$x = A * e^{j\omega}, A \in [0,1], \omega \in (-\pi, \pi] \tag{1.1}$$

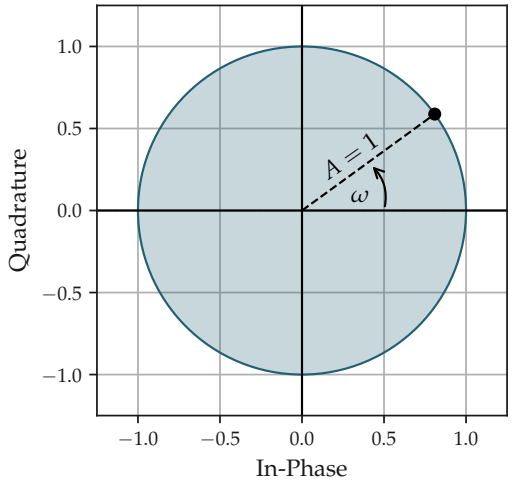
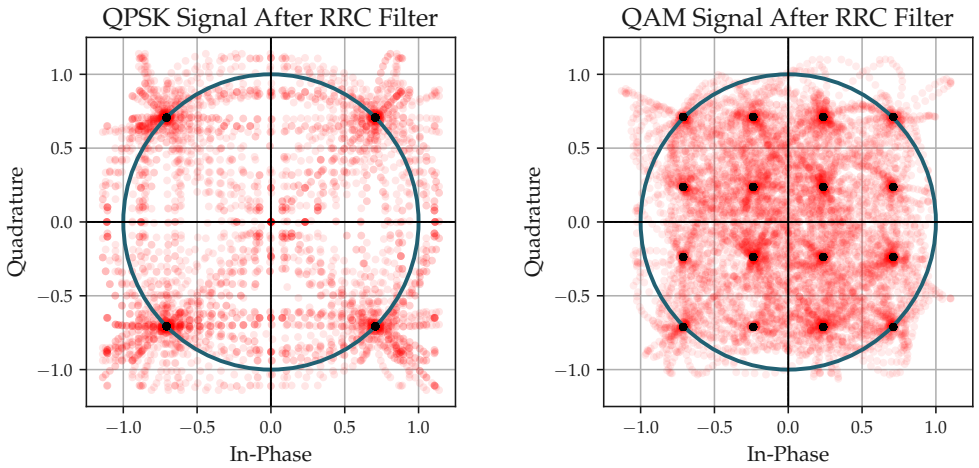


Figure 1.4: Region of possible operating states

Given a constant amplitude, digital symbols must be selected along the perimeter of the operating space. As the number of unique digital symbols (the arity) increases, more bits can be encoded and transmitted per symbol period, $bits = log_2(arity)$. As the spacing between constellation points decreases the likelihood of errors increases monotonically with the decrease in spacing. This motivates the use of the additional dimension of amplitude to increase the distance between points.

Even if symbols are placed only on the perimeter of constant amplitude the actual RF waveform may have a non-constant amplitude due to the waveform having to transition between constellation points. Figure 1.5a shows a standard Quadrature Phase Shift Keying (QPSK) constellation (black points) with the actual waveform plotted in red. The inter-symbol waveform must transition between each ideal constellation point and that of the next symbol. This path is defined, in-part, by the matched filter applied to the symbol waveform, often a Root Raised Cosine (RRC) filter. GMSK, used by GSM, uses specific design choices for the frequency of its tones to cause the transition paths to be along the constant amplitude perimeter, but is an exception. Most possible modulation schemes will have transitions crossing the interior of the operating space, resulting in the waveform having a lower average power level than the maximum.



(a) QPSK constellation

(b) 16-QAM constellation

Figure 1.5: Constellations showing inter-symbol transitions

Some common Quadrature Amplitude Modulation constellations position points on regular polar or rectangular grids to balance human readability and maximizing average distance between points. Figure 1.5b shows a 16 point QAM constellation and inter-symbol transitions. As performance requirements on digital communication systems have continued to rise, systems have begun to use numerically optimized constellations which do not use straightforward grids [22].

Increasing the arity of the constellations is one axis for increasing the bitrate of transmissions. Another is increasing the number of constellation symbols sent per second. For a given power level this decreases the amount of energy devoted to each symbol as it is transmitted for a shorter duration. Eventually the signal to noise ratio will reach a threshold where the probability of decoding it incorrectly increases and the bit error rate becomes unacceptable. Once the limits of a single modulated carrier have been reached, system designers turn to the use of multiple parallel transmissions occupying separate frequency ranges. This frequency domain multiplexing provides an additional parameter for distributing the available RF PA power to the information carrying symbols to maximize the throughput. OFDM arranges a grid of carriers such that the modulation on each carrier is orthogonal to the other carriers. While each individual modulated carrier may have a lower PAPR the multiple PAPRs are cumulative.

Unfortunately, this direction for increasing spectral utilization leads to problems with energy efficiency. The energy consumption in most wireless high frequency front-ends is dominated by the RF PA which maximizes its efficiency when operated

near saturation. However, the PA cannot be driven with a carrier power too close to saturation in order to avoid excessive distortion due to compression or clipping of the signal. Therefore, an Output power Back-Off (OBO) is applied to achieve the required linearity. This means that a standard linear PA will operate with low efficiency for signals with variable amplitude and an average power level significantly below the saturated power. This back-off reduces the average power compared to the PA's maximum capacity, an effect which is in addition to the signal's own PAPR.

To overcome this linearity vs. efficiency trade-off, several solutions have been proposed. First of all, at signal level, crest reduction factors are applied most of the time, and the PAPR numbers indicated to PA designers usually take these into account already. Hence, they do not improve the situation for the PA but at least they eliminate very large peaks that might damage the PA or create unnecessary distortion.

At PA level, the most studied solutions are the Doherty PA [1, 23], the current *de-facto* standard in mobile base-stations, the Chireix Outphasing [24], and Envelope tracking [25]. The Chireix and Envelope tracking require significant changes to the architecture therefore can be seen more as transmitter solutions rather than a PA solution. On the other hand, the success of the Doherty is that it is a PA solution requiring minimal change to the transmitter architecture when replacing a standard, linear PA. The more recently introduced Load Modulated Balanced

Amplifier (LMBA) [26] offers more flexibility in load modulation compared to the Doherty PA, but it is fundamentally based on the same concept.

This thesis will discuss the basic theory of the Doherty PA; how it can be used as a starting point and reference for a complete Doherty PA design, and how a template can be used to facilitate this process.

1.1.4 *Transistor Technologies*

Semiconductor technologies have evolved continuously since the initial discovery of a Germanium point-contact transistor in 1947 at Bell Labs in the United States. Simultaneously, the "Transistron" was created at Telefunken in Europe [27, 28]. RF Power Amplifiers for wireless communications have most frequently made use of silicon Laterally-diffused MOSFETs (LDMOS), Gallium Arsenide (GaAs), and Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) [29].

METRIC	GaN	GaAs	LDMOS
Operating Frequency	Up to 30 GHz	Up to 160 GHz	Up to 4 GHz
Bandgap	3.4 eV	1.4 eV	2.9 eV
Power Density	5-10 W/mm	1.5 W/mm	1-1.5 W/mm
Cost	4-5 $/W	1-2 $/W	1-2 $/W

Table 1.1: Performance Overview of semiconductor technologies [30, 31]

Multiple factors such as power density, frequency response, price, and power capacity influence the selection of technology for specific applications. The design approach detailed in this thesis is in-essence agnostic of the underlying transistor technology, but has been solely demonstrated using GaN HEMTs due to their availability and applicability to the chosen mid-band cellular base station application specifications.

Gallium Nitride is the newest popular semiconductor relevant to PAs, with GaN HEMT devices becoming commercially available in 2006 [32]. It faced manufacturing and design challenges but is now used in many designs operating above 3 GHz where high output power is a requirement [33].

In 2018 when this thesis' focus and scope were established, LDMOS was not competitive with GaN HEMT in the 3 - 4 GHz range. Recent work has shown that as LDMOS technology continues to advance and it can perform well in the sub 6 GHz range though GaN usually out-performs despite having fewer generations of manufacturing experience [34, 35]. GaN continues to lead in efficiency on wideband designs thanks to its beneficial physical properties listed in Table 1.1. The high power density of GaN transistors enables narrower gate widths for a given output power, while their higher operating voltage allows the required power levels to be achieved with lower current [36]. Consequently, this combination leads to higher optimal load impedances for GaN transistors compared to LDMOS at equivalent power levels. This higher impedance reduces the disparity between intrinsic and external loads, making it easier for matching networks to adapt. As a

result, the matching networks can achieve broader bandwidth. Additionally, the Silicon Carbide substrate frequently used with GaN has over double the thermal conductivity of LDMOS' Silicon substrate: $3.5\,\mathrm{W\,cm^{-1}\,K^{-1}}$ vs $1.4\,\mathrm{W\,cm^{-1}\,K^{-1}}$ [37]. The higher conductivity allows heat to be removed from the junction more rapidly. A wider bandgap, listed in Table 1.1, allows GaN to operate at higher voltages before experiencing avalanche breakdown. This is beneficial both for output power and to support the waveforms with high PAPR. The bandgap on both GaN and LDMOS decreases as the material temperature rises, however GaN's decreases less per degree of temperature rise and has a higher value at all operating temperatures.

1.2 RESEARCH MOTIVATION

The most common objective of power amplifier design is to achieve the maximum performance given a set of requirements. The primary metrics will be defined and examined in Chapter 2 as well as some of the ideal theory to design a Doherty amplifier. It will be shown that the ideal theory makes use of simplifying assumptions on transistor behavior which lead to complexities in real designs and deviations from theory.

The Doherty circuit architecture was introduced 87 years ago and its applicability to meet the fundamental requirements of modern wireless communications systems has lead to extensive research in recent decades. The ideal theory of the architecture becomes incomplete when applied to real components with parasitics and non-

linear behaviors. Much of the published work on Doherty architectures has focused on expanding the ideal theory by adding additional circuit elements, usually relying on standard ideal assumptions such as piece-wise linear transconductance in transistors.

Taking offset line theory as an example: [38, 39]. Even after multiple iterations on the base theory of using offset lines to compensate for phase shifts over power, the true behavior of the transistors and the introduction of parasitic reactive elements inherent to the manufacture of transmission lines on Printed Circuit Board (PCB)s continues to lead to designs where the maximum achievable performance requires deviating from ideal targets. The layout and deviations from ideal performance tend to increase as frequency increases, creating issues already in the cellular mid-bands from 2-4 GHz and increasing as designs are created to target 28 GHz and higher frequencies for 5G mm-wave bands.

The advances in transistor active device modeling have made available behavioral models which are both fast enough to be used for interactive simulations and accurate enough to reproduce complex influences on the signal waveforms. These include time domain memory effects, thermal variations, and nuanced compression. The models can include packaging parasitics, on-die parasitics, and make available a de-embedded node at the intrinsic plane. With this information it is possible to apply the ideal theory, which is usually based on designing outwards from an ideal intrinsic current generator, and display the key metrics relative to the achieved waveforms at that plane.

A beguiling approach is to place these behavioral models into a simulated circuit with the classical transmission line components drawn from Doherty's original architecture and perhaps the additional elements such as offset lines, which have been contributed by further research. This simulated circuit could have all the key dimensions and properties of the layout elements parameterized and a global optimization algorithm used to design the circuit based on a given objective function and the application's requirements.

At the current level of maturity and performance, the optimizers available in microwave RF simulation tools are unlikely to converge on a solution given such a large set of possible operating states and the likelihood of creating circuit conditions which present highly suboptimal loads to the active devices. Providing domain specific knowledge to the circuit, an initial state based on well known measurements of the transistors, and building the metrics around specific elements of the circuit theory provide a smaller and more controlled search space for the optimizer or for manual tuning by the designer.

1.3 RESEARCH OBJECTIVES

To develop a design approach, based on the use of modern non-linear circuit simulation, to expose the behaviors and key metrics of individual portions of a Doherty architecture PA as well as the more common overall performance measurements through the examination of currents and voltages throughout the circuit.

1.4 KEY CONTRIBUTIONS

Several original contributions have been made during the course of the research and will be discussed in this thesis.

1. Created of a simulation template for a load-modulated power amplifier which focuses on monitoring key parameters and metrics from design to layout finalization
2. Validated the template by designing and testing a miniaturized Doherty power amplifier for a 5G mid-band basestation application
3. Improved and validated an RF Power Amplifier measurement system with support for multiple, phase aligned signal sources

1.5 THESIS ORGANIZATION

This thesis is structured into six chapters, progressively building a comprehensive study of the design, implementation, and validation of a load-modulated power amplifier, with a particular focus on the Doherty architecture. The core of this work lies in Chapters 3 through 5, which present the novel design framework developed during this research and demonstrate its practical effectiveness.

Chapter 2 Theory

This chapter lays the theoretical groundwork necessary for understanding RF power amplifier design, focusing on load modulation techniques critical to the Doherty architecture. It covers fundamental concepts such as impedance parameters, transistor modeling, and amplifier efficiency, setting the stage for the design approach presented in the following chapters.

Chapter 3 Doherty Design Template

This chapter introduces the Design Template that represents the primary methodological contribution of this thesis. It integrates ideal theoretical models with advanced simulation tools to create a systematic approach for developing Doherty power amplifiers. The chapter details the structure and application of the template, showing how it can streamline the design process while maintaining high performance standards.

Chapter 4 Design and Implementation of an Amplifier using the Template

In this chapter, the effectiveness of the Design Template is demonstrated through the creation of a miniaturized Doherty power amplifier for a 5G mid-band base station application. The chapter provides a detailed account of the design process, including component selection and simulation, and discusses how the template guides designers in overcoming practical challenges. The results underscore the template's value in achieving optimal performance in real-world applications.

Chapter 5 Fabricating and Measuring the Amplifier

This chapter validates the practical applicability of the Design Template by fabricating the designed amplifier and measuring its performance. It covers the

translation of the simulated design into a physical prototype, addressing challenges such as PCB layout and assembly. The measurement results are analyzed to demonstrate the amplifier's alignment with design goals, further confirming the utility of the template in producing high-efficiency, high-performance amplifiers.

Chapter 6 Conclusion and Future Work

The final chapter summarizes the research contributions, highlighting the significance of the developed Design Template and its successful application in amplifier design. It also explores potential directions for future research, including the adaptation of the template to other amplifier architectures and the investigation of emerging semiconductor technologies.

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2

THEORY

2.1 BACKGROUND

The theory of designing RF microwave amplifiers requires understanding transistors and the necessary supporting elements to bridge them efficiently and effectively to the rest of the system. The core theory of amplifier design is covered comprehensively in textbooks, particularly in those by Cripps, Colantonio, and Walker. [40–43] This chapter selects and describes specific aspects of amplifier theory salient to load modulated amplifiers and the simulation based framework.

2.1.1 *Impedance Parameters*

An amplifier or transistor can be considered and analyzed as a generic two port network. Figure 2.1 details a two port device or Device Under Test (DUT) with a source connected to the input and a load at the output. This configuration is the most relevant for discussions of standard amplifiers as an external signal is only expected at the input and the output is a passive load. It will be shown that the

equations remain relevant when the load is formed by signals traveling into port two of the device.

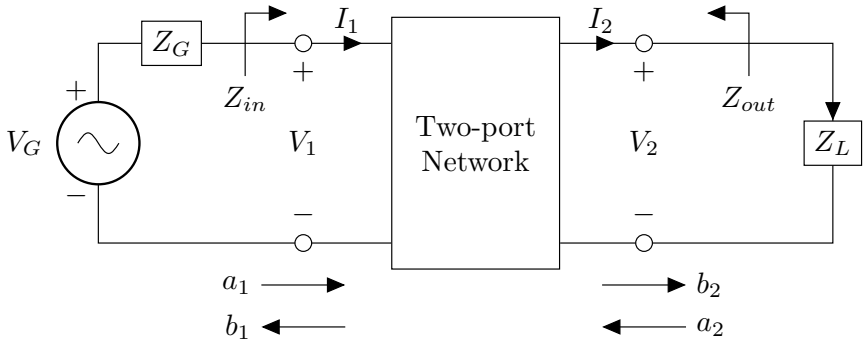


Figure 2.1: Two port network with a generator and load. Reproduced from [44]

The circuit analysis can be performed in several domains; voltages and currents, impedances, and traveling waves. These domains can be converted into each other which is useful for both analysis and measurements.

$$Z_{in} = \frac{V_1}{I_1} \qquad\qquad Z_L = \frac{V_2}{I_2} \tag{2.1}$$

The equations in 2.1 are simplified forms of the general two-port network equations, made possible by the inclusion of specific source and load impedances. It is crucial to recognize that these impedances, as well as the associated voltages and currents, are frequency-dependent. In power amplifier design, a single-tone test is often employed to facilitate analysis using a harmonic balance approach. This method allows for the evaluation of all circuit variables by considering the DC component (0 Hz), the fundamental frequency, and its integer harmonics.

Γ is the reflection coefficient, a ratio of the traveling waves entering and leaving a port of the device. Traveling waves are a useful domain as they are expressed in power and phase. Considering port 1 in Figure 2.1 the a_1 wave is the forward power incident into the port and b_1 is the reflected power traveling in the backward or reverse direction away from the port.

Traveling waves are defined such that the a wave is always forward into the port and the b wave backward or reflected from it.

$$\begin{aligned} \Gamma_{in} &= \frac{b_1}{a_1} & \Gamma_L &= \frac{a_2}{b_2} \\ &= \frac{Z_{in} - Z_0}{Z_{in} + Z_0} & &= \frac{Z_L - Z_0}{Z_L + Z_0} \end{aligned} \tag{2.2}$$

These equations transform currents and voltages to and from traveling waves using an arbitrary reference impedance, Z_0. For the specific setup shown in Figure 2.1 Z_0 is Z_G and Z_L for the input and output respectively.

$$\begin{aligned} V_1 &= \sqrt{Z_0}\,(a_1 + b_1) & V_2 &= \sqrt{Z_0}\,(a_2 + b_2) \\ I_1 &= \frac{1}{\sqrt{Z_0}}\,(a_1 - b_1) & I_2 &= \frac{1}{\sqrt{Z_0}}\,(a_2 - (-b_2)) \end{aligned} \tag{2.3}$$

2.1.2 *Transistor Models*

FET Small Signal Model

The small signal model of a Field Effect Transistor matches the Norton equivalent circuit of the 2 port DUT shown in Figure 2.1 with the Gate-Source voltage V_{gs} controlling the intrinsic current source such that the Drain-Source current is $V_{gs}g_m$ and the Drain-Source voltage V_{ds} is $V_{\mathrm{gs}}g_{\mathrm{m}}r_{\mathrm{d}}$. The transconductance, $-g_{\mathrm{m}}$, is the transfer function $\Delta I_{\mathrm{ds}}/\Delta V_{\mathrm{gs}}$.

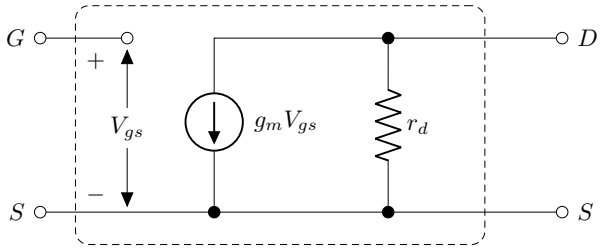


Figure 2.2: FET Small Signal Model

The small signal model offers a convenient simplification by assuming a constant transconductance. This assumption holds true at low signal levels, where the transistor operates linearly around its quiescent point, and the input signal variations are minimal enough to maintain a nearly constant transconductance. This simplification enables the use of linear circuit techniques, allowing engineers to predict the behavior of the transistor with a high degree of accuracy. Such an approach significantly streamlines the analysis and design process, making it an

invaluable tool in the initial stages of RF circuit development.

FET Large Signal Model

The Field Effect Transistor (FET) Large Signal Model describes the drain current as a nonlinear function of both the drain-source voltage and the gate-source voltage. Unlike the small signal model, the large signal model captures the full range of transistor operation, including the cutoff, triode, and saturation regions. In this model, the drain current is typically expressed through complex equations or lookup tables derived from empirical data, reflecting how I_D varies with changes in V_{DS} and V_{GS}. Additionally, the model includes parasitic elements such as capacitances and resistances associated with the gate, drain, and source terminals, which impact the frequency response and overall behavior of the transistor under large signal conditions. These parasitics are essential for accurately predicting the performance of FETs in circuits with significant voltage and current variations, such as in RF applications and power electronics.

The ability of the transistor to turn off (when V_{GS} is below the threshold voltage) allows it to operate in different modes, which is essential for achieving high efficiency in RFPA. In the off state, the FET exhibits very high impedance, minimizing leakage current and power dissipation. This characteristic is exploited in digital circuits and power electronics to achieve efficient switching. In the linear or triode region, the FET operates as a variable resistor, useful for analog applications and

signal modulation. In the saturation region, the FET provides a stable current source, essential for amplification. By accurately modeling these modes and their transitions, the large signal model enables the design of circuits with optimized performance, taking into account efficiency, thermal management, and reliability under large signal conditions. This comprehensive modeling is particularly important in high-power and RF applications, where precise control over the transistor's behavior is critical for system performance.

Large signal models can be circuit based or purely behavioral. Circuit based models are designed to accurately predict the performance of FETs under high power conditions, where nonlinearities and other complex behaviors become significant. Circuit-based large signal models typically include detailed representations of the FET's physical and electrical characteristics, allowing for precise simulation of its behavior in various operating conditions.

Some of the well-known circuit-based large signal FET models include the Curtice and Angelov models, each with variations as research continues [45].

The Curtice model is widely used for MESFETs and HEMTs and incorporates nonlinear elements to represent the FET's behavior under large signal conditions [46]. It includes parameters that describe the transistor's I-V characteristics, capacitances, and other nonlinear effects. It was originally designed for GaAs.

The Angelov model was developed for GaAs and GaN HEMTs and provides a comprehensive approach to modeling large signal behaviors, including self-heating

effects and charge trapping [47]. It is known for its accuracy in predicting large signal performance in power amplifiers.

These circuit-based large signal models are essential for designing and optimizing RF and microwave circuits, as they provide a detailed and accurate representation of the FET's behavior under realistic operating conditions.

Some models, such as the Root model, combine physical and circuit properties with empirical equations to model a transistor. The Root model includes equations relating the gate and drain voltages with drain current directly, removing the need to calculate the internal circuit states for to obtain these values [48]. Some circuit elements are still included in the model so the approach is a combination of a compact circuit model and one which focuses on observable behaviors.

2.1.2.1 *Behavioral Models*

Separate from models based on extracting physical values to create an equivalent circuit, it is also possible to model the actions of a transistor or amplifier through behavioral models. Unlike compact models, which focus on the detailed physical properties and internal mechanisms of the device, behavioral models emphasize the input-output behavior of the device. These models are particularly useful when the detailed internal mechanisms are either too complex to model accurately, unnecessary for the specific analysis, or unknown. Models such as the Volterra series, General Memory Polynomials, X-Parameters, and Cardiff Models use polynomial

equations which can usually be computed much more efficiently than an equivalent circuit [49–54].

Behavioral models excel in speed and simplicity, making them ideal for system-level simulations where detailed device-level accuracy is less critical. However, a key limitation of behavioral models is their tendency to lose accuracy outside the range of operating parameters for which they were developed. Since behavioral models are typically constructed based on data from a specific set of operating conditions, their ability to extrapolate beyond this range is often limited. This can result in significant inaccuracies when these models are applied to conditions that differ from those initially considered.

In contrast, compact models, which are often built using a broader range of measurements covering multiple domains, tend to offer better extrapolation capabilities. This is because compact models incorporate a more comprehensive understanding of the physical behavior of the device, allowing them to maintain accuracy over a wider range of operating conditions. However, this improved accuracy comes at the cost of increased complexity and computational effort, as compact models require more detailed information and longer development times.

Behavioral models, by comparison, are quicker to create and can achieve equivalent or greater accuracy within their intended operating space. For applications where speed and simplicity are paramount, and the operating conditions are well-defined, behavioral models provide a practical and efficient solution. Nevertheless,

designers should be aware of their limitations and consider the potential need for compact models when working outside the model's validated range.

The latest approach to behavioral modeling makes use of Artificial Neural-Networks [55–57]. This modeling approach has been shown to provide sufficient accuracy, including for cut-off and saturated states, to design effective Doherty amplifiers [58].

2.1.3 *Fundamental Amplifier Parameters*

The core properties or state of an amplifier system can be stated using values decomposed into Fourier components. For example, the value of a steady-state periodic voltage will contain energy at one or more fundamental frequencies as well as DC, harmonic, and mixing product frequencies. Working with the magnitude and phases of these components of the signal provide a mathematically convenient approach to calculating the system's properties.

The input and output powers are given by Equations 2.4. From these, the factor by which the amplifier has changed the input power level is given by Equation 2.5.

$$\begin{aligned} P_{\text{in}} = P_{\text{in}}(f) &= \frac{1}{2}\text{Re}\{V_{\text{in}} * I_{\text{in}}^*\} \\ P_{\text{out}} = P_{\text{out}}(f) &= \frac{1}{2}\text{Re}\{V_{\text{out}} * I_{\text{out}}^*\} \end{aligned} \tag{2.4}$$

$$G(f) = \frac{P_{\text{out}}(f)}{P_{\text{in}}(f)} \tag{2.5}$$

As the input power rises the amplifier will reach a point where physical limitations cause the output voltage and current to be limited. At this point the achieved power gain will start to fall (compress) as input power continues rising and the output power saturates. It is common to use the point at which gain has compressed 1 dB or 3 dB as the point of maximum or saturated power, P_{sat}.

An RF power amplifier takes an input RF signal with P_{in} and produces an output signal with a higher P_{out} through the constructive use of DC power, P_{DC}, supplied to the active device(s). For a single input tone:

$$P_{\text{DC}} = V_{\text{dc}} \frac{1}{T} \int_0^T I_{\text{dc}}(t) dt \tag{2.6}$$

The efficiency of conversion of DC power to output power is given by:

$$\eta = \frac{P_{\text{out}}}{P_{\text{DC}}} \tag{2.7}$$

This thesis will only be discussing the use of Field Effect Transistors so the efficiency is further specified as the drain efficiency η_{d}, as the gate bias power is assumed to be negligible. The drain efficiency ignores the input signal power required to drive the amplifier to the target output power. This input power can

be a significant percentage relative to the output power at the power gain values achievable by individual active devices at GHz frequencies. For instance at 10 dB gain the input power is 10 % of the output power. The efficiency definition can be extended to account for this additional power requirement and provide us with the effectiveness at which power is added to the signal, Power-Added Efficiency (PAE).

$$\eta_{add} = \text{PAE} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}} \tag{2.8}$$

Figure 2.3 shows the typical behaviors of output power, gain, drain efficiency, and PAE as input power increases for a conventional single device amplifier.

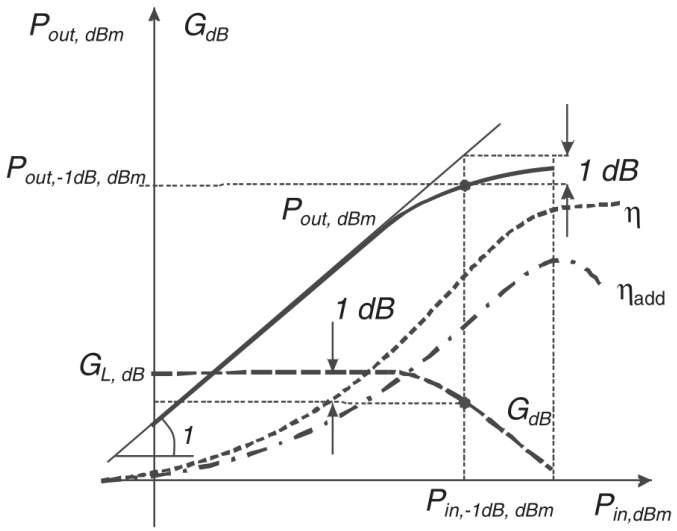


Figure 2.3: Typical performance in a PA as a function of input power (reproduced from [42])

2.1.4 *Loadline Analysis*

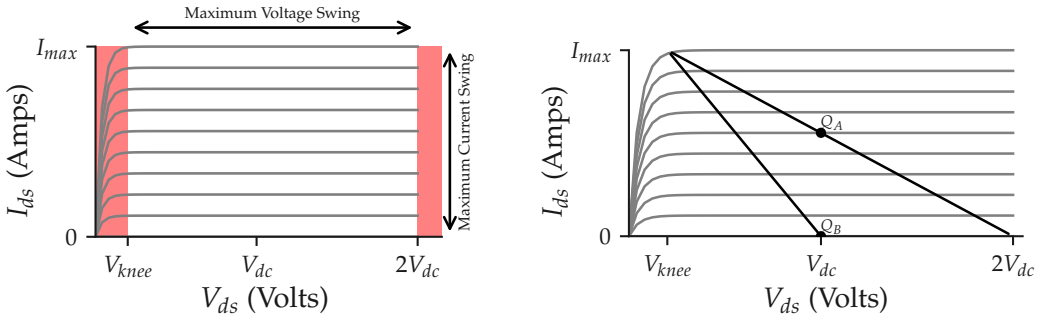
The power delivered by a transistor varies based on the load impedance observed by the drain terminal of the transistor. As an ideal transistor is a pure transconductance device the output current is controlled by the voltage between gate and source terminals.

$$i_{\mathrm{d}} = I_{\mathrm{dc}} + \Delta i_{\mathrm{d}} = I_{\mathrm{dc}} + -g_m \Delta v_{\mathrm{gs}} \tag{2.9}$$

Given a fixed load R_{L} connected across the drain and source terminals, a voltage of $v_{\mathrm{L}} = V_{\mathrm{dc}} + R_{\mathrm{L}} \Delta i_{\mathrm{d}}$ will be produced. The possible range which this voltage can achieve is limited by the transistor's knee voltage, breakdown voltage, and V_{dd} drain bias voltage. The range of I_{d} current values is limited by the device channel pinchoff, the point at which the gate-source potential has depleted the availability of charge carriers preventing current flow. In practice the maximum current is also limited by the necessity of dissipating waste heat.

Figure 2.4a shows the behavior of a near-ideal FET at a series of discrete gate bias voltages as the drain current is swept from zero to two times a nominal DC bias point. This shows the current and voltage operating space of the transistor under DC conditions and is referred to as a DCIV plot.

Figure 2.4b shows the ideal loadlines of class A and class B amplifiers. In class B it is assumed that the load impedance at all harmonics of the fundamental



(a) Typical FET IV characteristics

(b) Class A and B Ideal Load Lines

Figure 2.4: FET IV Characteristics and Amplifier Load Lines

are shorted, giving a pure sinusoidal voltage output. A key observation with the loadlines is that for all positive real load impedances the drain current will be at its maximum when the V_{ds} is at its minimum, unless the voltage swing extends down into the knee region. Equation 2.15 will show that power is dissipated (wasted as heat) equal to the product of the drain voltage and current.

2.1.5 *Class A Amplifiers*

The loadline above for a class A amplifier contains information on several key properties which are formalized below. The bias-point Q_{A} is set such that without an input signal ($V_{\mathrm{gs}} = 0$) there will be a quiescent current of $I_{\mathrm{max}}/2$. At saturation the voltage swing will range from V_{knee} to V_{max}, symmetrically around V_{dc}. Figure 2.5 shows the current and voltage waveforms assuming $V_{\mathrm{knee}} = 0$ and constant g_{m} (linear amplification).

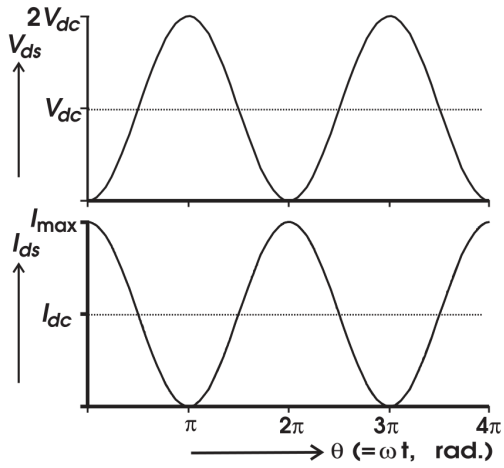


Figure 2.5: Ideal Class A current and voltage waveforms [43]

$$P_{\text{rf}} = \frac{V_{\text{dc}} - V_{\text{knee}}}{\sqrt{2}} \frac{I_{\text{dc}}}{\sqrt{2}} = \frac{V_{\text{dc}} - V_{\text{knee}}}{2} I_{\text{dc}} \tag{2.10}$$

$$\eta_{\text{pbo}} = \frac{V_{\text{dc}} - V_{\text{knee}}}{2V_{\text{dc}}} = \frac{1}{2}\left(1 - \frac{V_{\text{knee}}}{V_{\text{dc}}}\right) \tag{2.11}$$

2.1.6 *Class B Amplifiers*

The class B PA is defined as the gate being biased exactly at its threshold point, where the channel is just cut off from conduction. This results in the drain current waveform being cut off below its inflection point, conducting for 50 % of the waveform period. The optimum load produces a voltage swing from V_{k} to V_{dd}.

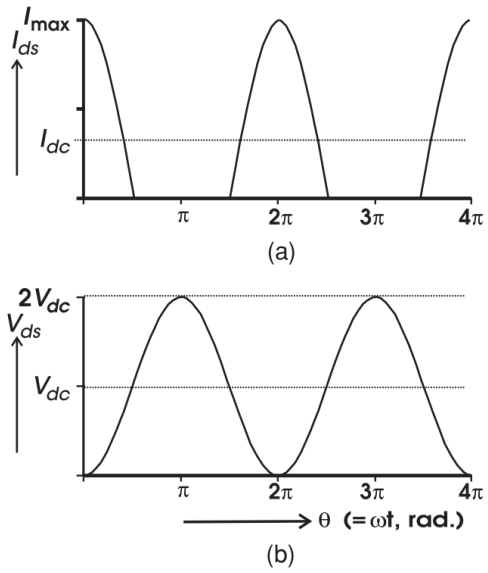


Figure 2.6: Ideal Class B current and voltage waveforms [43]

$$R_{\text{opt}} = 2 * \frac{(V_{\text{dd}} - V_{\text{k}})}{I_{\text{max}}} \tag{2.12}$$

The efficiency of a class B amplifier is dependent on the voltage swing produced at a given power level. Additionally, the efficiency decreases more slowly than class A as output power is backed off.

$$\eta = \frac{\pi}{4} \cdot \frac{V_{\text{out}}}{V_{\text{dd}}} \tag{2.13}$$

The efficiency can be made independent of the output power by observing that output power is related to the drain supply voltage and the load impedance.

$$P_{\text{out}} = \frac{V_{\text{dd}}^2}{2R_{\text{L}}} \tag{2.14}$$

This is independent of the actual drain current required to produce the voltage swing, therefore it can be achieved at any specific power level less than or equal to the saturated power by choosing an appropriately large load impedance. This observation is key in the derivation of the Doherty Power Amplifier circuit in the next section.

2.1.7 *Dissipated Power*

In the time domain, the power dissipated in the transistor is the product of the voltage and current waveforms over a given time period. As nearly all analysis is done on ideal sinusoidal waveforms composed of a fundamental frequency and harmonics of that frequency, the dissipated power can be calculated over a single period of the fundamental.

$$P_{\text{diss,out}} = \frac{1}{T}\int_0^T v_{\text{ds}}(t) \cdot i_{\text{ds}}(t) \cdot dt \tag{2.15}$$

The dissipated power is the primary loss of power between the input signal and DC supply and the ouput signal. Given Power-Added Efficiency as defined in Equation 2.8, the $P_{\text{diss,out}}$ can also be related to the PAE.

2.1.8 *Efficiency in Backoff*

A key consideration and benefit of class B operation compared to A is that the ideal efficiency is higher at both saturated and backoff cases.

CLASS	SATURATED EFFICIENCY	BACKOFF EFFICIENCY
A	50%	$\frac{1}{2}\frac{P_{\text{rf}}}{R_{\text{max}}}$
B	$\pi/4 = 78.5\%$	$\frac{1}{2}\sqrt{\frac{P_{\text{rf}}}{R_{\text{max}}}}$

Table 2.1: Ideal Power Amplifier Efficiencies

Here we observe that the efficiency of the class B amplifier falls as the square root of the backoff as compared to a linear decrease from the class A.

Techniques such as envelope tracking and Doherty amplification dynamically adjust supply voltage and load impedance respectively, optimizing the intrinsic waveforms for higher efficiency.

Maintaining linearity and signal integrity is crucial for high-quality communication. Nonlinearities in the intrinsic current-voltage (I-V) characteristics of the transistor can lead to signal distortion.

Advanced modulation schemes demand highly linear and efficient amplification across a wide range of power levels, making the precise control of intrinsic current and voltage waveforms essential. Accurate measurement and characterization techniques, such as load-pull measurements and network analysis, provide critical insights into the intrinsic behavior of transistors. This data informs the design and optimization process, enabling precise adjustments to the waveforms to achieve desired performance metrics. Ultimately, waveform engineering manipulates these intrinsic waveforms to enhance RF power amplifier performance, driving advancements in modern communication systems.

2.2 LOAD MODULATION

The load line based design approach maps information about the properties of intrinsic current and voltages within a transistor to design objectives such as the load impedances. In RF PA design these parameters directly influence performance characteristics such as efficiency, linearity, and signal integrity. Efficient PA operation requires minimizing power loss within the transistor by shaping the intrinsic voltage and current waveforms to reduce their overlap during the switching cycle, as mentioned in section 2.1.7.

This approach is formalized in the concept of Waveform Engineering [59]. By examining the waveforms and applying knowledge of their influence on different performance objectives, it is possible to discover additional amplifier classes and

more generically entire continua of operating spaces which provide desirable properties [60–62]. Doherty designs are an example of controlling the intrinsic waveforms in a way which varies with output power, as will be described below.

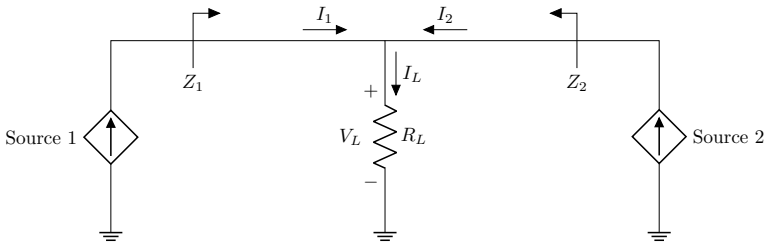


Figure 2.7: Ideal circuit of current generators with a common load

If a second FET is connected to the same load as another FET, as shown in Figure 2.7, then the voltage developed will depend on both transistors.

$$V_{\mathrm{L}} = R_{\mathrm{L}}(I_1 + I_2) \tag{2.16}$$

From the perspective of the first current generator, the voltage across the load is increasing without the first current generator's output changing. This effect is as if the value of the load were increasing to a new value R'_{L}. Combined with the previous result of Kirchoff's current law, the effective load of the first current generator can be expressed as:

$$\begin{aligned} Z_1 &= \frac{V_{\mathrm{L}}}{I_{\mathrm{L}}} \\ &= \frac{R_{\mathrm{L}}(I_1 + I_2)}{I_1} \end{aligned} \tag{2.17}$$

For the second current generator, the effect is identical.

$$Z_2 = \frac{R_L(I_1 + I_2)}{I_2} \tag{2.18}$$

This dependence of the observed load on the currents of each transistor allows for the control, or modulation, of the load by varying the current supplied by either or both of the transistors. An important observation; for the transistor to contribute positively to the total output power, each current generator's contribution can only range from zero to positive (or, seen in another way, the currents are in phase at the load), meaning the effective load impedance will always increase from the nominal value due to the other generator's current contribution.

2.3 DOHERTY DESIGN

2.3.1 *Core Theory*

The Doherty Amplifier architecture links two transistors to a common load and controls the current each supplies to modulate the load each sees as a function of input power [1]. These two transistors are referred to as Main and Auxiliary, or sometimes as Main and Peaking.

As observed before, the efficiency of a transistor rises as it supplies more power, reaching its peak as the voltage swing reaches its maximum range. This leads to a

desire that one transistor supply all of the power whilst in backoff. If the power were split between both transistors, regardless of the ratio, the overall efficiency would be less than a single transistor supplying all the power. The transistor used first is referred to as the Main.

As the Main transistor reaches its maximum voltage swing, additional current must be supplied by the Auxiliary to continue producing further power. This behavior, with the Auxiliary supplying current when the signal level peaks, is where the alternative name of "Peaking" comes from. However, if current is supplied from the Auxiliary transistor into the common load then the effective load of the Main transistor will increase, as seen in Equation 2.17.

When the voltage swing available to the Main transistor is reached (where it is maximally efficient without current waveform clipping), R'_{L} should not be increased else clipping, and therefore gain compression and distortion, would result. Instead, if the Auxiliary's additional current leads to a decrease of R'_L after the maximum voltage swing is achieved, it would allow the Main to be driven further (more current) without clipping the waveform.

An impedance inverter allows for the increase in load at the common node (which is unavoidable when combining currents in phase) to be transformed to an effective reduction of impedance at the Main. This allows the Main's voltage to be maintained just below clipping, therefore being efficient without unwanted distortion. Most commonly the impedance inverter is constructed using a quarter-wave transmission line as a transformer.

Figure 2.8 shows the modified load modulation circuit. As Z_1' increases due to the current I_2 flowing into R_L the inverter will cause Z_1 to be transformed in a ratio set by the characteristic impedance Z_T of the transmission line segment [63].

$$Z_1 = \frac{Z_T^2}{Z_1'} \tag{2.19}$$

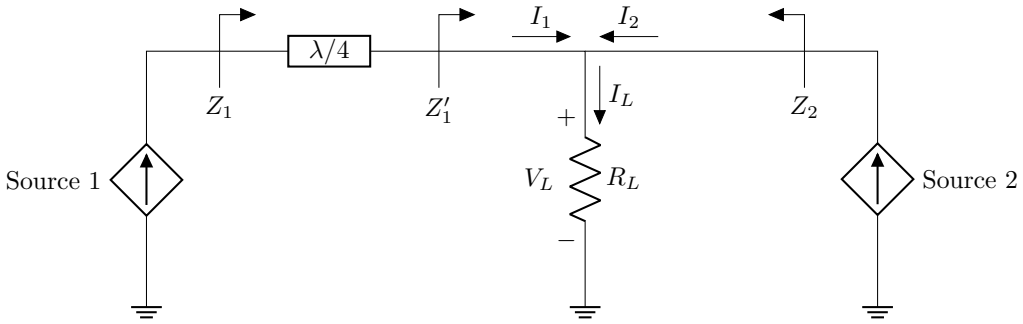


Figure 2.8: Ideal Inverted Load Modulation

This generic circuit is shown again using the terminology and labels of the Doherty architecture in Figure 2.9, focusing first on the Main amplifier.

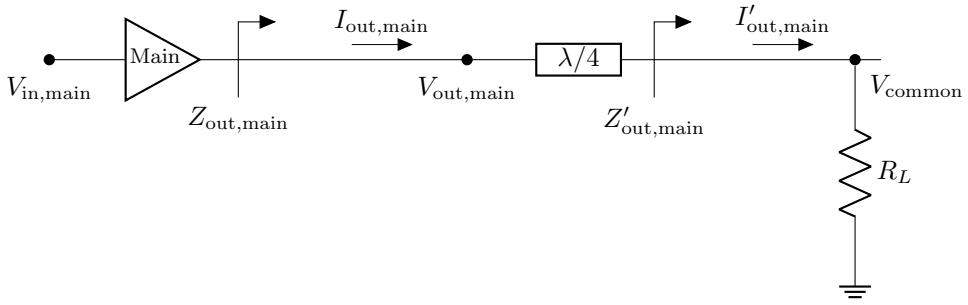


Figure 2.9: Ideal Output Network of the Main Transistor

This Main transistor is combined with the Auxiliary and then matched to the external load presented by the next system component, often a circulator, coaxial cable, or antenna, usually a $50\,\Omega$ impedance. A splitter divides input power and a length of transmission line is added before the Auxiliary transistor, such that both paths have an equal phase length between the splitter and common combining node, as required for constructive addition. The final circuit is shown in Figure 2.10.

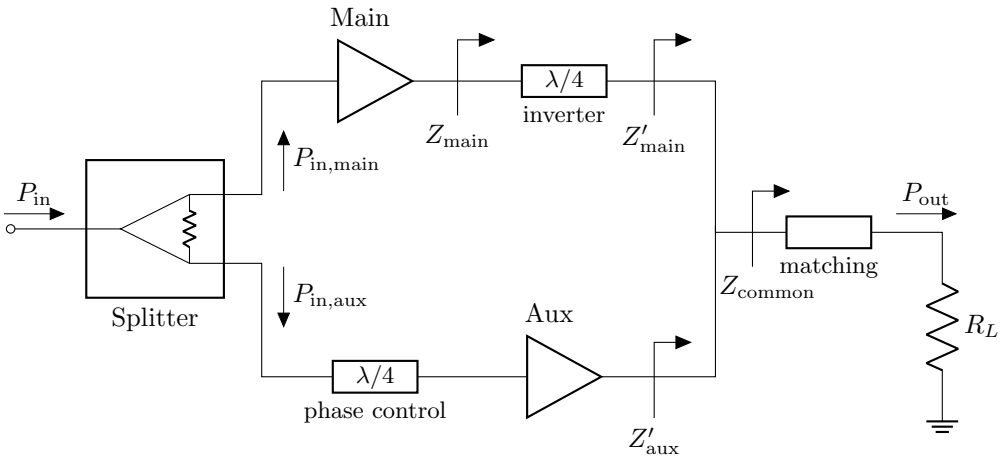


Figure 2.10: Complete Ideal Doherty Schematic

The result of this circuit arrangement is a set of loadlines for the Main and Auxiliary amplifiers shown in Figure 2.11. The Main amplifier's loadline is static while input powers are low, with the Auxiliary inactive and loaded with effectively an infinite resistance (as its output "sees" a voltage, but provides zero current). As the Auxiliary begins turning on, the load of both of the amplifiers begins modulating to a lower value, extracting additional current from both devices. This synergistic arrangement allows the Main to continue operating at V_{max} from the OBO point till peak power.

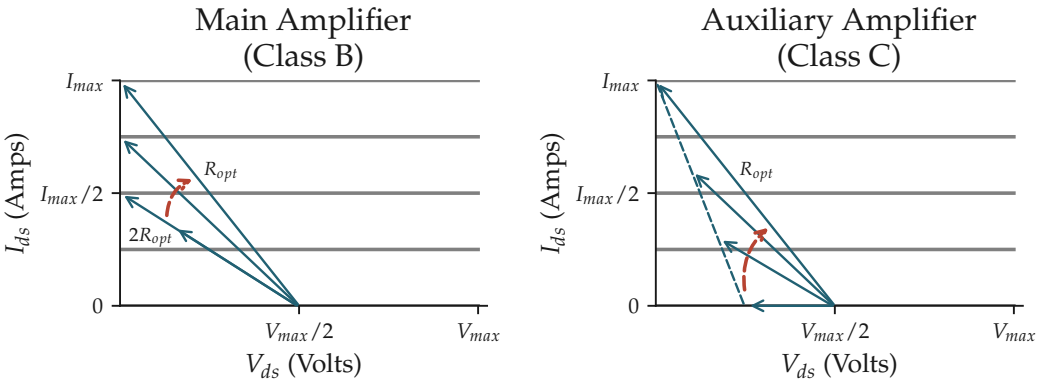


Figure 2.11: Loadlines of the Main and Auxiliary Amplifiers. The red curved arrow indicates the direction which the load changes as power increases.

The original analysis by Doherty was for two identical valve devices, or equivalently for two transistors which respond to input signals and biases in the same way. In this configuration the two transistors will each supply half of the total current for the amplifier when driven to peak power. The load on the main will be modulated by a factor of two as the Auxiliary goes from fully off ($I_{\text{out,aux}} = 0$) to fully on ($I_{\text{out,aux}} = I_{\text{max}}/2$). This results in the load being 50 % lower at peak power than at backoff so to achieve maximum utilization of the transistor its loads should move from 2 R_{opt} to R_{opt}. As shown in the loadline section, a load impedance higher than R_{opt} will result in a class B/C amplifier saturating its voltage swing earlier than it saturates its potential to generate current, as desired.

Given this ratio of currents it can be seen that the Main will be the only source of output power at the OBO point, supplying $P = (V_{\text{max}} * I_{\text{max}})\ /4$ or one quarter of the total peak power. This sets the initial saturation point of the Main at 6 dB below the amplifier's maximum output.

As covered in section 1.1, modern communication waveforms have PAPRs exceeding 6 dB. Matching the Doherty backoff point to the PAPR specification provides a useful efficiency maximum at the average power level of the waveform. This analysis so far has used equally sized transistors supplying an equal current at saturation. This ratio is a degree of freedom which can be used. By increasing the amount of current supplied by the Auxiliary at saturation, the amount of load modulation the Main experiences increases, allowing for the initial saturation peak to be achieved at a greater backoff. Hence, by knowing the target OBO it is possible to calculate, in first approximation, the ratio of the output power that the two active devices must provide at saturation. By definition:

$$OBO = \frac{P_{\text{total,max}}}{P_{\text{total,obo}}} \tag{2.20}$$

However, at the backoff, only the main amplifier operates, so:

$$P_{\text{total,obo}} = P_{\text{main,obo}} \tag{2.21}$$

Since the voltage of the Main PA is kept constant between the backoff point and saturation, the output power of the Main only increases because of the current contribution, therefore following a square-root response:

$$P_{\text{main,max}} = \sqrt{OBO}\, P_{\text{main,obo}} \tag{2.22}$$

This means

$$P_{\text{total,max}} = \sqrt{OBO}\, P_{\text{main,max}} = P_{\text{main,max}} + P_{\text{aux,max}} \tag{2.23}$$

we can therefore relate the power of the two devices:

$$\frac{P_{\text{aux,max}}}{P_{\text{main,max}}} = \sqrt{OBO} - 1 \tag{2.24}$$

Figure 2.12 plots equation 2.24 up to an OBO of 14 dB.

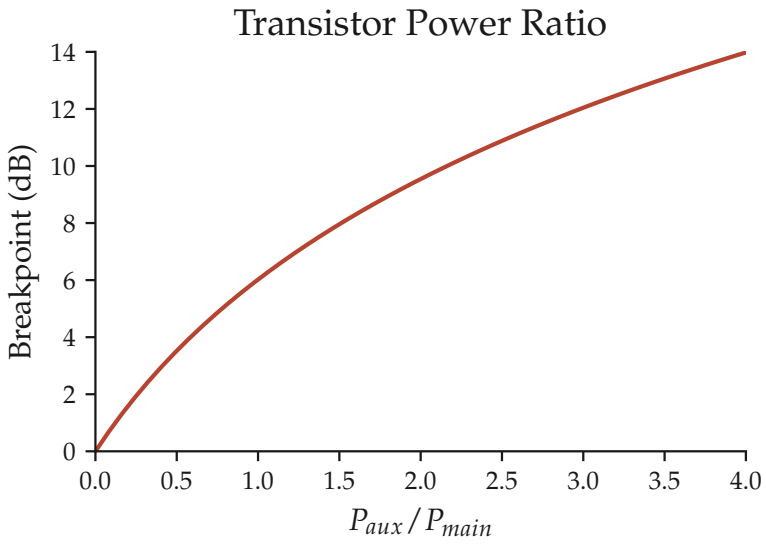


Figure 2.12: Relationship between OBO target and transistor power selection

2.3.2 *AC Design*

Now with the understanding of how to calculate the ratio of currents necessary to build a Doherty amplifier with an efficiency peak at a given backoff value, the analysis can turn to determining the specific loads and key component values to deliver the currents.

The analytical design so far has been purely ideal and this section will admit only a small imperfection, the knee region of the transistor's operating space where the transconductance falls and current output diminishes dramatically. By reducing the target voltage swing the distortion can be substantially reduced.

$$V_{\max} = V_{\mathrm{DD}} - V_{\mathrm{knee}} \tag{2.25}$$

The equations for calculating the values of each circuit component are derived in *RF Power Amplifiers for Wireless Communciations* with the Main and Auxiliary transistors being "identical, both in terms of parameters, bias, and drive level" [40]. What follows is a replication of the results of the derivation, adapted for asymmetric operation by the introduction of a term β. This analysis maintains the classical Doherty assumption of the transistors having an equal $V_{\max}$.

$$\begin{aligned}\beta &= \frac{P_{\text{max,main}}}{P_{\text{max,main}} + P_{\text{max,aux}}} \\ &= \frac{I_{\text{max,main}}}{I_{\text{max,main}} + I_{\text{max,aux}}}\end{aligned} \tag{2.26}$$

Amplifier specifications almost invariably begin with a rated or target output power, P_{max}, making it a valuable parameter to introduce early in the analysis. This allows the maximum current supplied by the Main and Auxiliary transistors to be given by:

$$\begin{aligned}I_{\text{max,main}} &= \frac{4\beta P_{\text{max}}}{V_{\text{max}}} \\ I_{\text{max,aux}} &= \frac{4(1-\beta) P_{\text{max}}}{V_{\text{max}}}\end{aligned} \tag{2.27}$$

These currents and voltages set the optimal required loads at the OBO and max operating points.

$$\begin{aligned}R_{\text{main,opt}} &= \frac{2V_{\text{max}}}{I_{\text{main,max}}} \\ R_{\text{main,obo}} &= \frac{R_{\text{main,opt}}}{\beta} \\ R_{\text{aux,opt}} &= \frac{2V_{\text{max}}}{I_{\text{aux,max}}}\end{aligned} \tag{2.28}$$

With the classical Doherty configuration of just one impedance inverter between the output of the Main transistor and the common combining node, the impedance

of the combining node must be a factor of $1 - \beta$ greater than $R_{\text{aux,opt}}$. This leads to the Auxiliary being correctly loaded when the amplifier is at peak power. With the common node impedance fixed, the characteristic impedances of the inverter to the Main as well as an additional inverter to match the node to $50\,\Omega$ are fixed as well.

$$\begin{aligned} R_{\text{common}} &= R_{\text{aux,opt}}(1-\beta) \\ Z_{\text{main,inv}} &= \sqrt{R_{\text{common}} \frac{R_{\text{main,opt}}}{\beta}} \\ Z_{\text{global,inv}} &= \sqrt{R_{\text{common}}\, 50} \end{aligned} \tag{2.29}$$

2.3.3 *AC Simulation*

These equations can be brought into a circuit simulator to provide a dynamic and interactive environment for analysis. Keysight ADS includes a non-linear circuit simulator which can provide extensive information about the behavior of an RF circuit using nuanced models of components including GaN HEMTs. These simulations however involve numerous linear algebra operations and iterative calculations of the circuit state, which leads to long runtimes. These are invaluable in the design process, but not necessary to explore the ideal Doherty load modulation.

By simplifying the calculations to involve fixed current and voltage magnitudes, an AC model can be created which can be evaluated nearly instantaneously. The transistors are modeled as ideal current sources. The circuit is analyzed in two

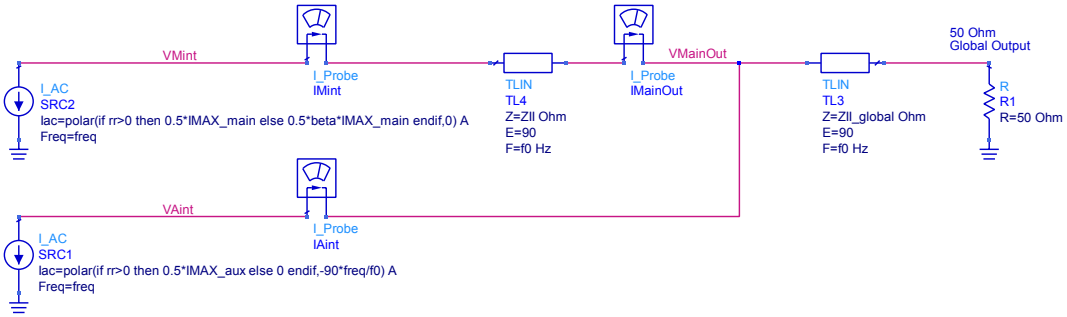


Figure 2.13: ADS AC Schematic of an ideal Doherty

states; the Doherty breakpoint, alternatively called the Transition point in literature, and full output power. The simulation omits the input side of a practical Doherty amplifier so a phase shift of $-90^\circ * f/f_0$ is included in the Auxiliary current generator's phasor.

$$I_{\text{main}} = \begin{cases} 0.5 * I_{\text{main,max}} * \beta & rr \leq 0 \\ 0.5 * I_{\text{main,max}} & rr > 0 \end{cases}$$

$$I_{\text{aux}} = \begin{cases} 0 & rr \leq 0 \\ 0.5 * I_{\text{aux,max}} & rr > 0 \end{cases}$$

The results of the AC simulation provide target load impedances and an indication of how those loads will vary over frequency given the simple output matching network. In chapter 4 this AC simulation will be used as the initial step for designing

a complete amplifier which was fabricated and measured, with the results shown in chapter 5.

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3

DOHERTY DESIGN TEMPLATE

3.0.1 *Top Level Testbench*

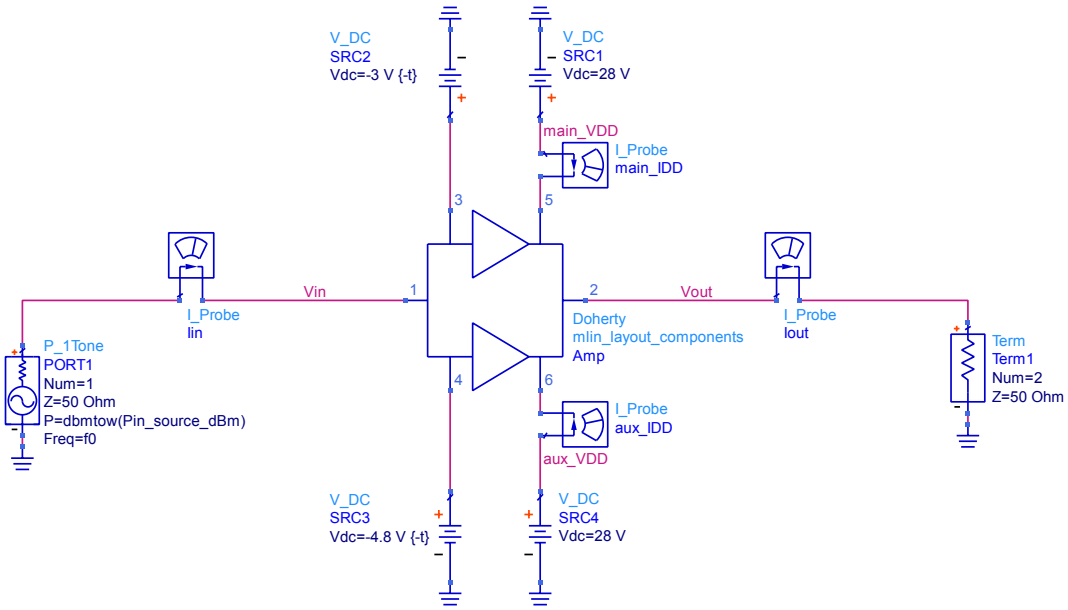


Figure 3.1: Top level testbench in Keysight Pathwave ADS

Keysight's Advanced Design System (ADS) software provides an environment which supports simulation of the Doherty circuit with multiple techniques from simple, ideal AC models through full 2.5 or 3D electromagnetic simulation. A top level testbench schematic, shown in Figure 3.1 provides consistent stimuli, bias

voltages, and measurement of the output waveform. These form the complete interface between the amplifier circuit and surrounding system. ADS has the ability for a single design "cell" to have multiple variations of the design defined, including schematics, layouts, and EM models. We use this feature to create a generic Doherty cell which holds the variations at each stage of the design process. Finally the testbench is also linked with the primary Data Display which calculates and plots the key Doherty properties and parameters defined in previous sections.

The top level testbench contains an S-Parameter simulation for stability and basic circuit properties such as input match and small signal gain. This simulation is useful as it provides quick validation of these values, but is limited in the level of detail to which its outputs can be used to examine the Doherty behavior. The S-Parameter stability analysis is used to analyze the Main and Auxiliary amplifiers independently as the k-factor method is not valid when multiple active devices are between the two test ports being considered [64, 65]. Analyzing the stability of the entire Doherty amplifier is possible using various forms of loop analysis [66, 67].

A harmonic balance simulation with swept frequency and input power is the primary tool used to exercise the design. Defining the simulations and order of the sweeps in this singular top-level testbench makes the test data directly comparable between design stages, simplifying the investigation of performance changes between steps.

Simple, high-level measurements are defined and calculated by the top-level testbench including P_{out}, P_{in}, P_{DC}, transducer and power gains, DC-to-RF drain

efficiency and Power-Added Efficiency based on the voltage and current probes at this level.

3.0.2 *Circuit Probes*

The Doherty circuit itself is held in an ADS cell with ports to connect gate and drain supplies, an input for the stimulus signal, and an output of the amplified signal. Probes are inserted inside of the circuit schematic of the amplifier to non-invasively monitor currents and voltages throughout the design.

The input matching networks for a Doherty amplifier are largely identical to those of conventional, single-device amplifiers so are not explored in this thesis. The design template however does include probes to measure the input impedance before the power divider, the power division ratio of the input signal to the Main and Auxiliary devices, the input impedances after the divider, and the input impedances at the gate terminal of each transistor. By using current and voltage waveforms, these values can be calculated and used during the harmonic balance simulation and directly related to the behaviors of the output networks and overall amplifier, which are analyzed in depth. Using values from the S-Parameter simulations was initially explored but rejected as improved overall performance and clarity on the causes of changes in performance after each design step was obtained by having the additional information from the power sweep and easy access to the harmonic content of the waveforms.

The output matching networks contain the majority of the complexity in the Doherty Architecture. Despite that, only a few probe points are required to derive all of the metrics discussed previously and to create expressive plots to monitor them. In Figure 3.2 we can note pairs of voltage and current probes for the Main, Auxiliary, and output paths of the common combining node. The Wolfspeed Modelithics device models expose internal probe nodes for the intrinsic current generator current and voltages. If these were not present in the model, pairs of probes could be added after de-embedding the output parasitics by using standard techniques (such as Cold-FET bias extraction) or a non-linear technique (which can include properties such as the gate-drain capacitance, C_{gd}) [68, 69]. For this specific design two additional probe points were added: one between the two auxiliary inverters and another between the two stages of the output matching network.

This chapter will use an example design to show the design features of the template. The selected design is a simplistic symmetric Doherty using ideal transmission lines and biasing networks. The transistors are Wolfspeed 15W devices which will be examined more closely in the following chapter, for the purposes of this demonstration the transistors are partially idealized using negative capacitors to cancel their output capacitance. No effort has been made to improve the design for performance. A full design using the template will be shown in Chapter 4.

From these measurements, the impedances and phase relationships between different points in the output network can be calculated and their behavior shown over

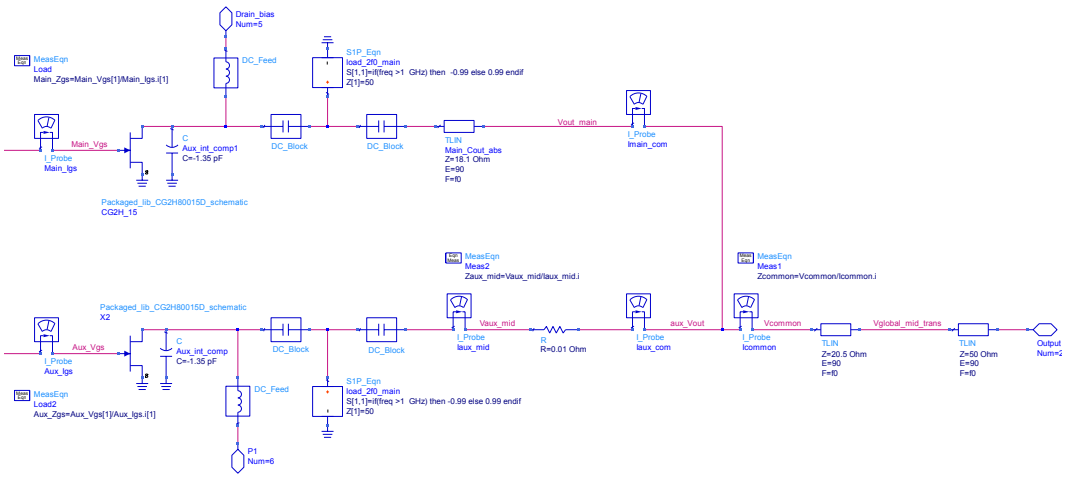


Figure 3.2: Ideal transmission line implementation of a Doherty

frequency and power level. The testbench Data Display formats this information into several plots emphasizing different aspects of the Doherty behavior.

3.0.3 *Data Displays*

The Doherty architecture maximizes the voltage swing of the Main amplifier at a point backed off from full power, then extracts additional current at that voltage level by modulating the effective load to a lower value as the input signal level continues to rise. Loadline plots display this behavior most directly by combining the DCIV data measured at the start of the design process with the intrinsic plane current and voltage waveforms of the simulated signal. Figure 3.3 shows this data for an amplifier simulated just at the backoff point. In the interactive Data Display, sliders allow the stimulus frequency and power level to be selected to drive the

data plots. The red trace shows the dynamic behavior of the waveform at a single selected power level, in this example with the Main transistor reaching the knee voltage while sourcing a current of $\sim 1/3\ I_{\max}$ and the Auxiliary amplifier not yet conducting current. The thin blue trace shows the path of the maximum power point of load-line over the entire range of the power sweep, demonstrating the behavior seen in Figure 2.11.

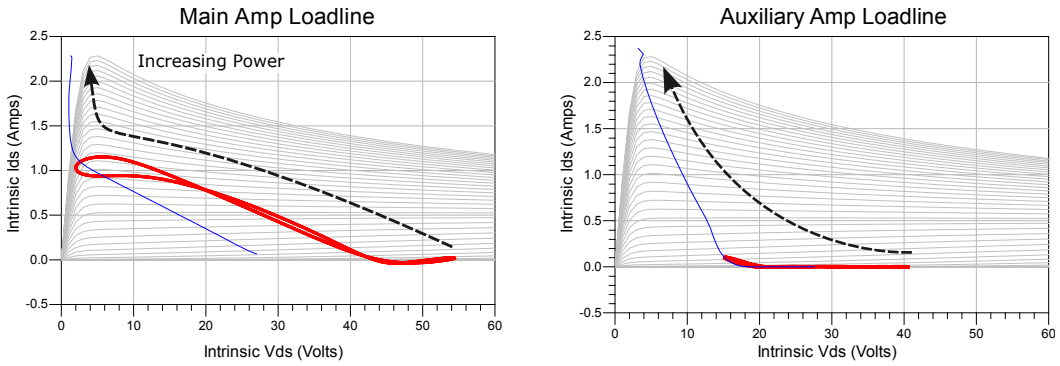
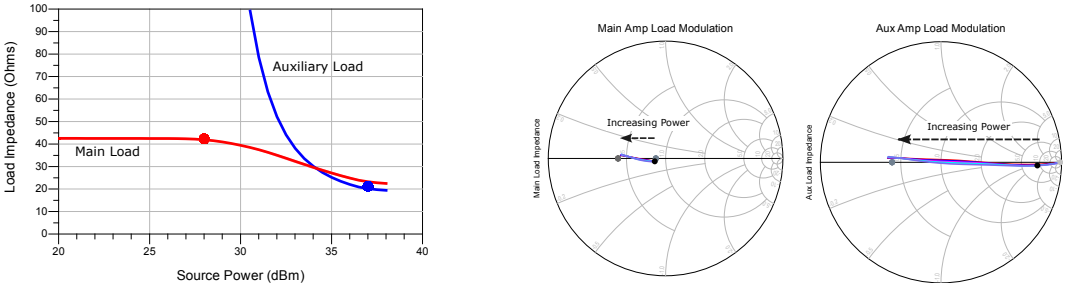


Figure 3.3: Load lines at the intrinsic generator planes. The red trace shows the path of the output waveform at a specific power level. The blue trace shows location of each waveform's maximum power point as input power is swept.

This data can alternatively be shown as the effective load impedances presented to the transistors at the fundamental frequency. Figure 3.4 displays the real value of the loads as well as their complex values on a Smith chart. The real-valued chart provides quick access to the load values at any given source power level without visual transformation of the Smith chart's grid. This is highly useful during tuning of the characteristic impedances of the inverters, as the match at both backoff and peak power is visible. Issues of insufficient load modulation are immediately apparent as well as errors in the achieved loads. The calculated ideal loads are noted by markers and in this figure it can be seen that the Main's load

reaches its target neither at backoff or saturation. The Main amplifier's load is also capacitive at maximum power, a deviation from ideal theory, which produced marked improvements in efficiency. This may be due to incomplete de-embedding of parasitics in the model. The transistor manufacturer's model included a node for currents and voltages at the intrinisc plane. No additional de-embedding was done to modify that node.



(a) Real component of the effective loads

(b) Complex effective loads

Figure 3.4: Load Modulation at the intrinsic generator planes

3.1 ANALYZING THE TRANSISTORS

3.1.1 *DCIV*

Keysight ADS includes a FET Curve Tracing template to measure DCIV information. These curves are then used in the Doherty design template to display the loadlines during simulation of the amplifier. Figure 3.5 shows the template and simulated IV curves.

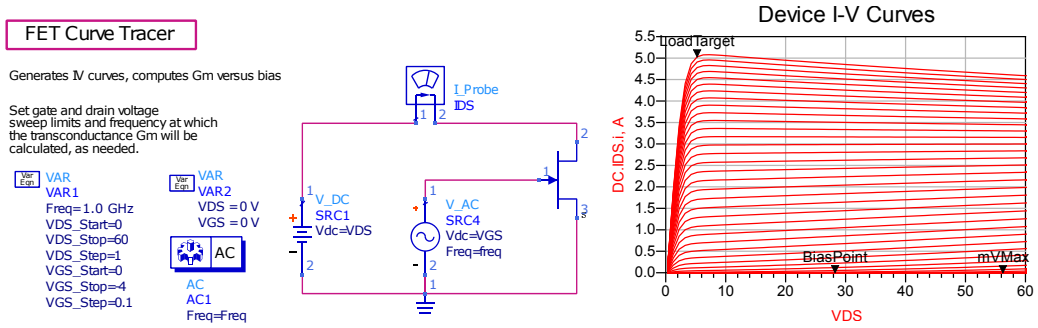


Figure 3.5: ADS FET Curve Tracer and Results

3.1.2 *Load-Pull*

Once the DC behavior of the amplifier is measured, load-pull allows the large signal behavior of the transistor to be examined. The AC simulation described in section 2.3.3 requires the potential maximum power of the Main and Auxiliary transistors as input values. In the next chapter we will find that load-pull can also be used to de-embed the output parasitics.

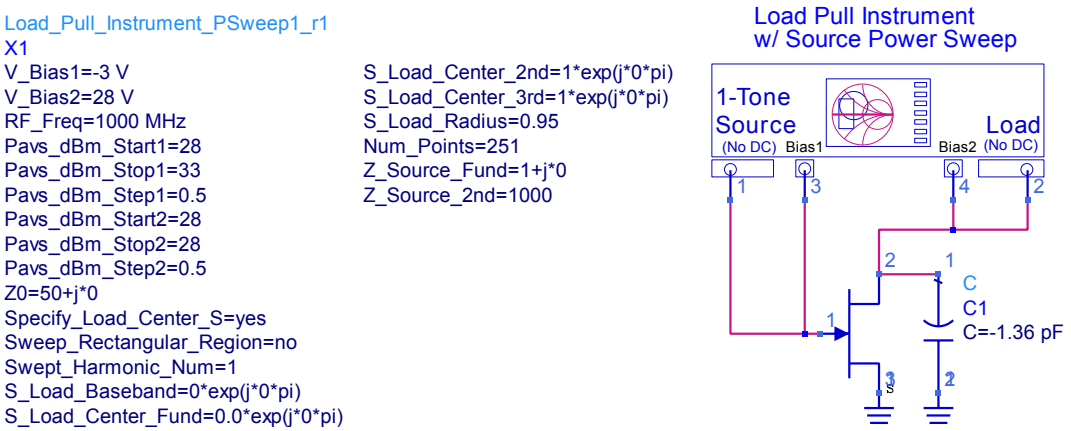


Figure 3.6: ADS Loadpull Schematic with C_{out} canceled

Figure 3.6 shows the block diagram of a load-pull system in Keysight ADS. This load-pull setup configures a source impedance and static bias voltages to the gate

and drain. The load impedance for the fundamental or second harmonic is swept over a grid configured by setting a center point and radius. The non-swept load is configured to a static value. This system also supports performing an available source power sweep, useful to identify when gain saturation occurs. The template's data displays calculate both transducer and power gains.

3.2 ADS AC SIMULATION

Load-pull analysis provides the maximum potential power values required for the the AC circuit equations derived in section 2.3.2. The equations can be built into an ADS AC simulation as as shown in section 2.3.3 and the results used to evaluate the load modulation effects.

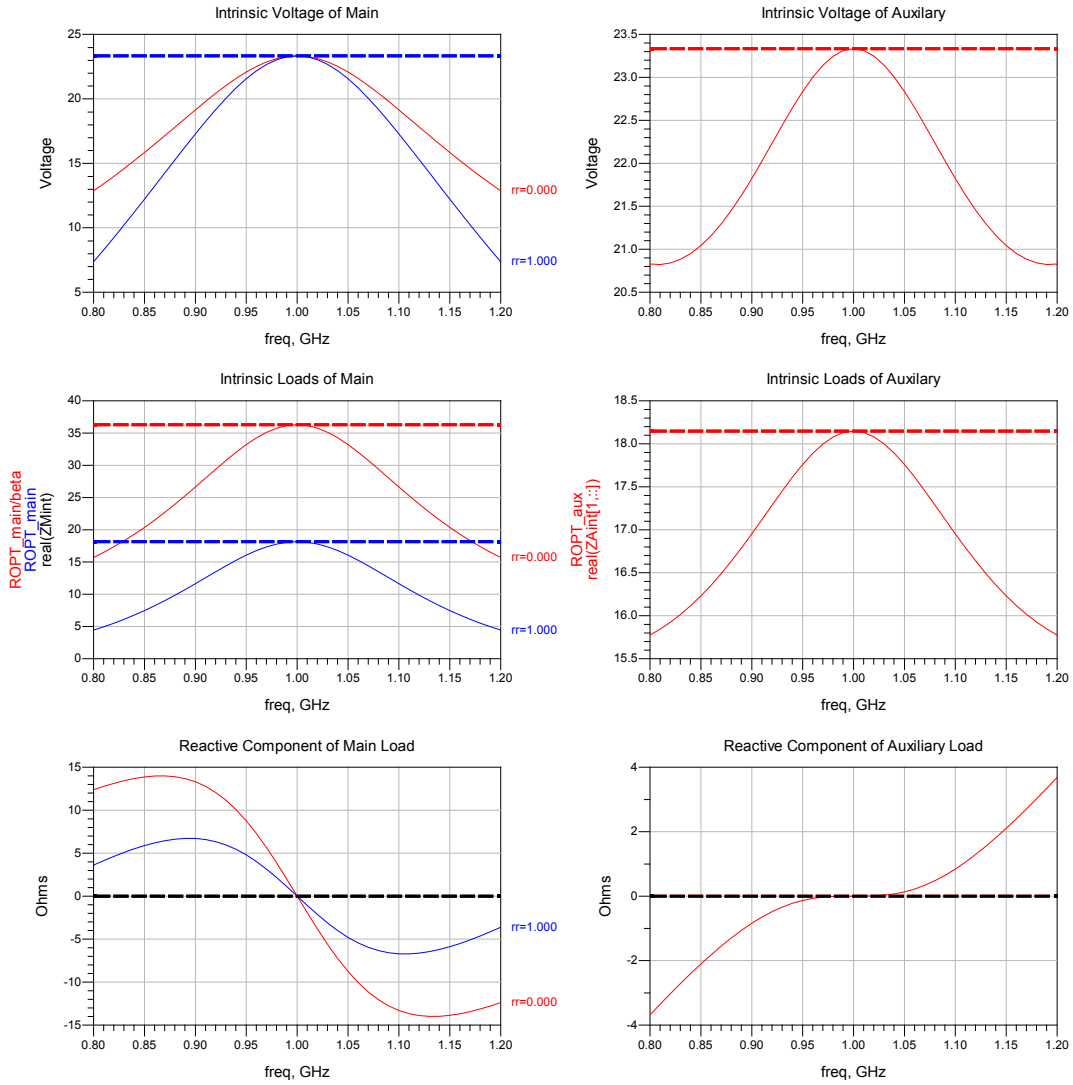


Figure 3.7: ADS AC results of an ideal symmetric Doherty

Figure 3.7 has three plots each for the Main and Auxiliary transistors. The results here are for a classical symmetric Doherty with two equal transistors. The dashed lines show the targets calculated by theory. At the center frequency it can be seen that the load impedance of the Main transistor varies from 18.1 Ω at the breakpoint to 36.2 Ω at the saturation point, an exact load modulation factor of 2.

3.3 ADS HARMONIC BALANCE

Harmonic balance is a frequency-domain analysis technique used to find the steady-state solutions of dynamic non-linear systems subjected to a periodic excitation. This method is particularly applicable to RF PAs as it efficiently handles the non-linearities inherent in the transistors and other circuit elements. By focusing on the steady-state response, harmonic balance provides insight into how the PA will behave under continuous operation.

To analyze the Doherty behavior a single-tone excitation is used meaning the responses are obtained for the direct current (DC), the fundamental frequency, and a finite number of harmonics. This approach simplifies the analysis by limiting the frequency components considered. By doing so, the harmonic balance method effectively captures the essential behavior of the RF PA without the computational complexity of considering an exhaustive range of harmonics. As a practical consideration, the circuit component models are only valid for a certain frequency range and power is expected to be significantly lower at higher harmonics. The load-pull simulation uses Harmonic Balance to obtain accurate measurements of the high power properties of the transistors.

3.4 KEY METRIC VISUALIZATION

3.4.1 *General Amplifier Metrics*

The design template includes a section with common overall performance information such as efficiency, gain, and output power. Figure 3.8 shows the significant efficiency boost at backoff that a Doherty provides, achieving nearly 55 % PAE at 6 dB backoff. Figure 3.9 shows the maximum output power, power and transducer gains, and gain compression vs frequency for the example ideal symmetric Doherty operating at 1 GHz. This example amplifier illustrates the essential Doherty behavior, though the performance could be improved were it an actual design. For instance, the gain falls significantly at the Doherty OBO point and continues to fall consistently through the region the Auxiliary is active. Changing the Auxiliary's gate bias may be able to restore this lost gain, but was unimportant for the purposes of this example. The measurement is performed across a sweep of frequencies, in this example five evenly spaced around 1 GHz. Some performance variation can be seen, with gain increasing by 0.75 dB from the lowest frequency to the highest.

Figure 3.10 tracks the amplifier's output power and its compression from maximum gain. The compression behavior is important to monitor as it provides information on the linearity of the amplifier. With a Doherty design, it is possible for either or both of the amplifiers to saturate at unexpected times if the loads, load modulation, or biasing are not correctly balanced. The 1 dB compression point has

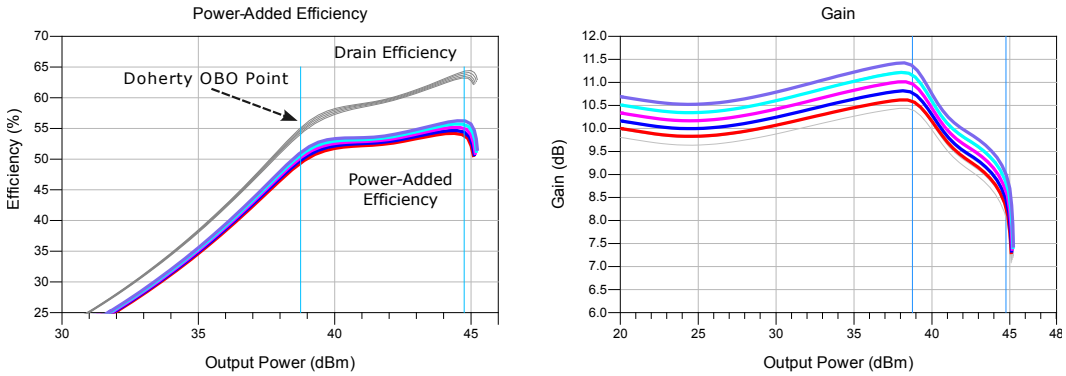


Figure 3.8: Simulated Gain and Efficiency Performance

historically been considered the end of linear amplification with GaAs and Silicon LDMOS transistors delivering very little additional power after this point. With GaN there is notable additional power available at the cost of additional compression [70, 71]. All transistors produce less gain when nearing their maximum output power. With GaN this reduction begins at a larger backoff from the maximum saturated power level than LDMOS or GaAs but the gain falls at a slower rate per additional dB of output power. This means that the 1 dB point occurs at a greater backoff from the maximum power level and designs can take extract the most power from the transistor by driving the amplifier deeper into compression.

The main focus of the Doherty theory is on the effects of the current at the primary frequency on the transistor loads. However, the individual amplifiers still generate energy at harmonic frequencies and are affected by the load impedances at those frequencies. The second and third harmonic loads have the greatest influence, and a variety of amplifier classes which improve efficiency and/or output power have been identified which rely on specific loads being presented [72–74]. Figure 3.11 shows these loads for the Main and Auxiliary amplifiers. The Auxiliary amplifier's

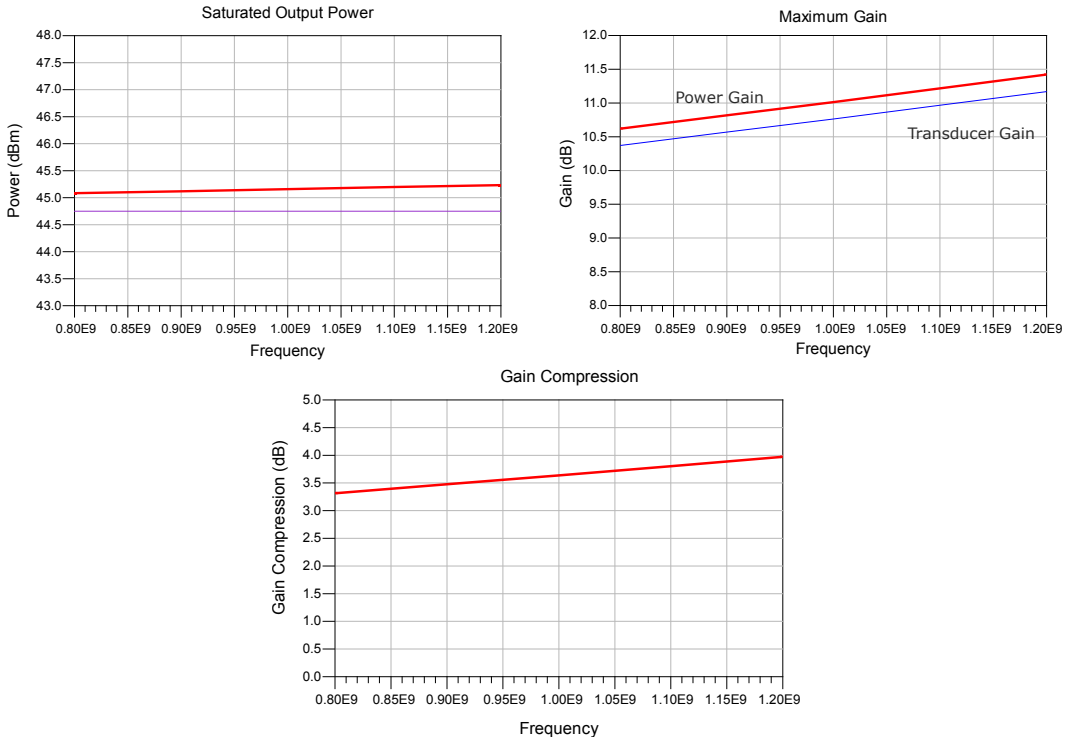


Figure 3.9: P_{sat}, Maximum Gain, and Compression versus Frequency

loads are shown for the input power values between it turning on (the Doherty breakpoint) and it saturating.

The result of all of the load impedances, load modulation, and transistor's small and large signal behaviors is the actual amplification between input voltage waveform and output currents and voltages. Figures 3.12 and 3.13 show the output waveforms. Having a view of these waveforms at the intrinsic planes is useful for identifying both potential issues and potential desirable enhancements [40]. In this particular example, a symmetric nearly-ideal Doherty, the waveforms are shown from the breakpoint (the point at which the Auxiliary turns on) to saturated power range. The dark and thick traces are at the breakpoint. Figure 3.12 shows the Main amplifier's measurements. The voltage traces show a nearly ideal behavior with

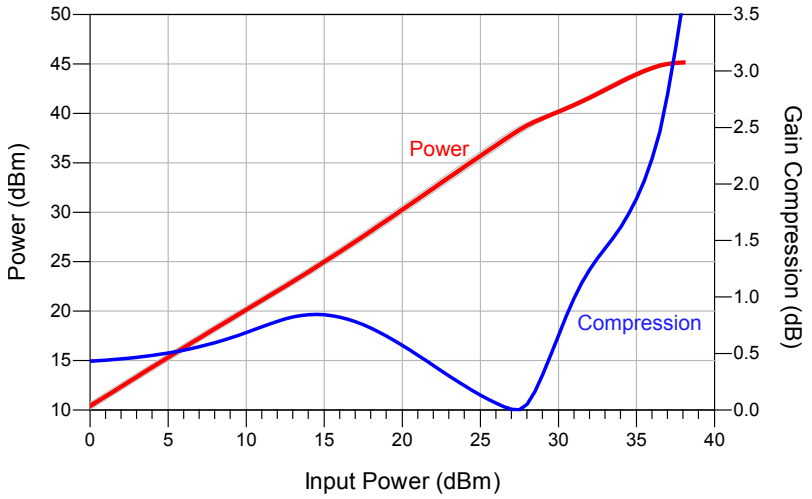


Figure 3.10: Output power and Compression

little variation across the power sweep. The current traces show a smooth increase, almost exactly doubling between the breakpoint and saturation as predicted by theory. The current waveform shows a notch where the voltage waveform clips into the knee region, reducing the current. The Auxiliary's current starts close to zero, then rises, showing the transistor's channel is correctly pinched off by the deep class C bias in backoff and also turns on at the correct input power level. The Auxiliary's voltage waveform is asymmetric both around the 28 V drain bias point and between the rising and falling edges, pointing towards potential issues with the load being reactive or mismatched at a harmonic.

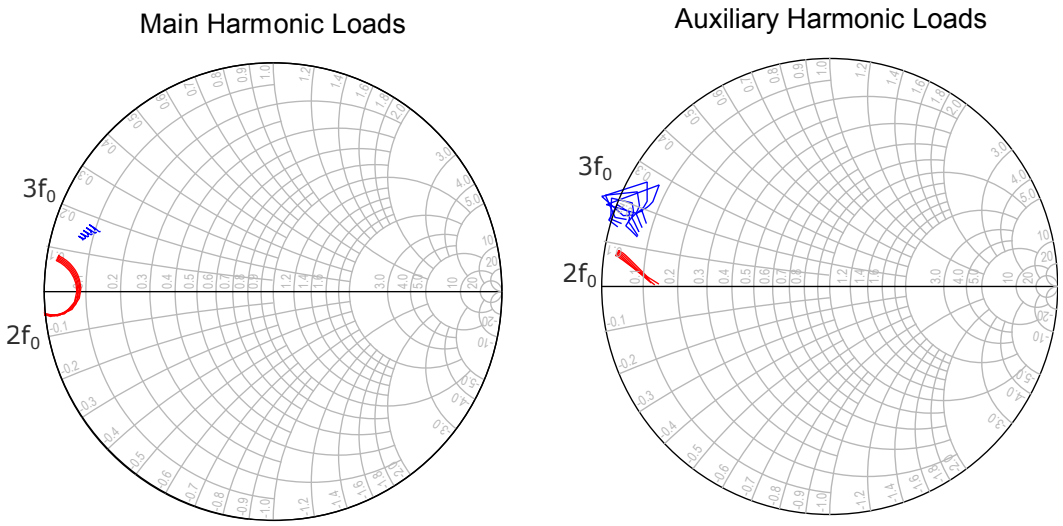


Figure 3.11: Harmonic loads at the Intrinsic plane

3.4.2 *Doherty Architecture Metrics*

The performance metrics measured and plotted in the preceding section are applicable to power amplifiers in general. This section covers measurements and metrics which are more specific to Doherty amplifiers.

Figure 3.14 shows the achieved ratios of the fundamental portion of drain currents vs frequency. As the current contributions are directly related to the load modulation, these plots should show nearly identical behaviors with any difference being likely due to an issue with the impedance inverter. In this specific case, ideal theory would have the current ratio equal to 1, with both transistors delivering the same current at saturation. The Auxiliary ends up supplying very slightly more than the Main, indicating some potential room for improvement in this example circuit. The Main amplifier's load should be modulated by a factor of 2 and is

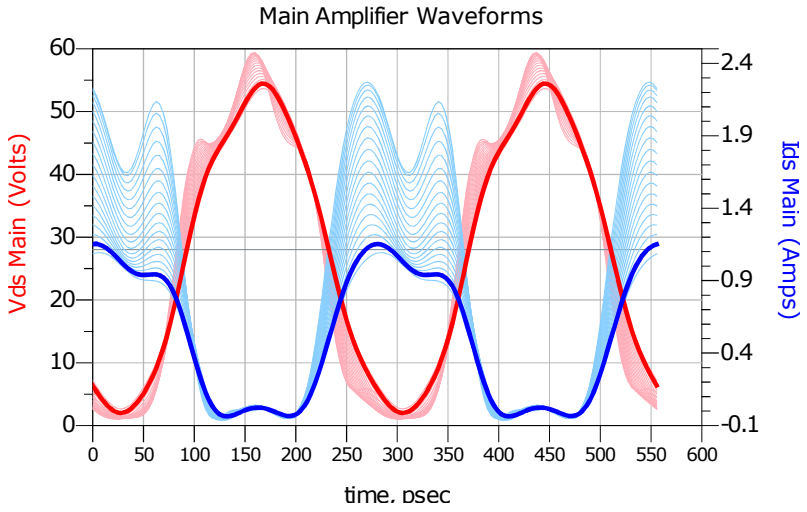


Figure 3.12: Current and Voltage waveforms at the Main's Intrinsic plane

actually $\simeq$1.9. The Main transistor delivers more current as its load is modulated more, so this is potentially the cause of the current ratio being slightly imbalanced.

The ratios only provide information about the amplifier operating at its saturation point. The behavior is far more nuanced when the input power is swept at a single frequency. Figure 3.15 shows the current and voltage values for the fundamental input frequency. These plots provide a clear view of the relative current contributions of the amplifiers. The slopes should ideally be piece-wise linear. In this example some small deviations can be seen, with the Auxiliary's current turning on a little slowly, though at the correct input voltage. On the voltage plot the Main overshoots slightly before being modulated back closer to its ideal value.

A matching network almost always exists between the output combiner node and the exterior circuit in order to convert the standard 50 Ω impedance to the load necessary for the amplifiers to correctly operate. As described in the Doherty theory each port of the combiner will observe different effective impedances depending

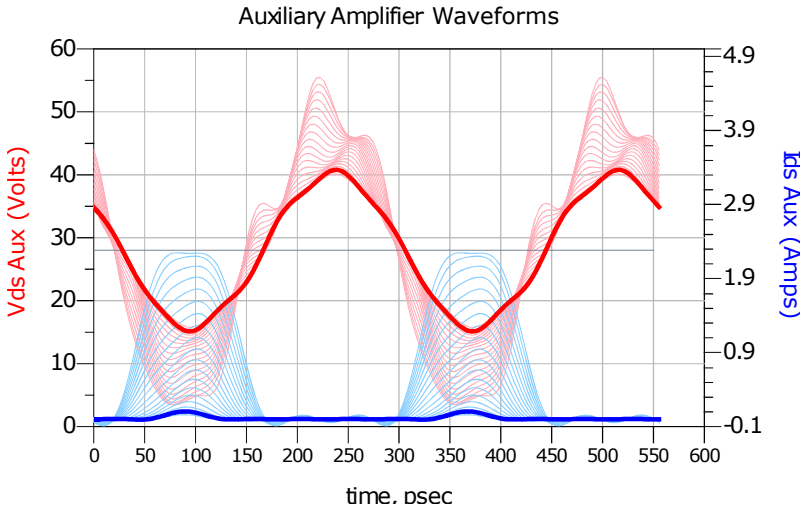


Figure 3.13: Current and Voltage waveforms at the Auxiliary's Intrinsic plane

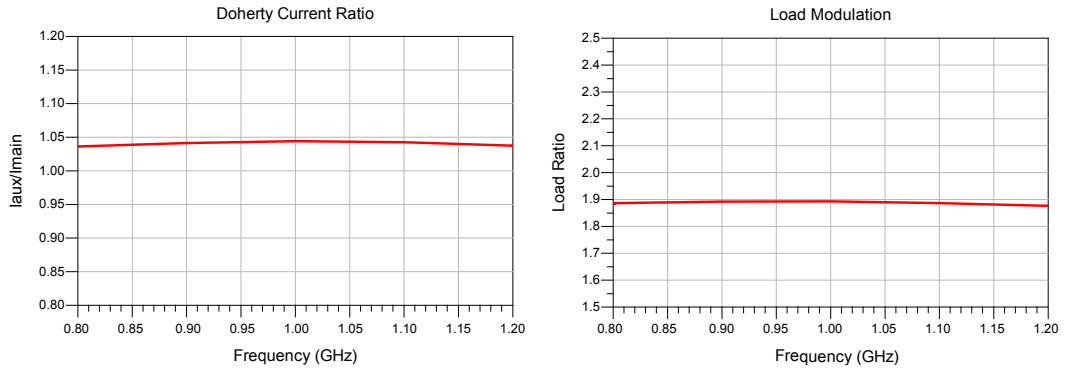


Figure 3.14: Current and Load Modulation Ratios

on the ratio of currents present. At low input powers, with only the Main sourcing current, the common node impedance will be the load seen by the port connected to the Main. The port connected from the Auxiliary will experience an effectively infinite load regardless of the matching network's performance. As the Auxiliary contributes current the effective load will modulate but the load after the combiner stays constant.

Figure 3.16 shows this information with traces for several frequencies across the band. The example has very similar behavior across frequency, but a more realistic

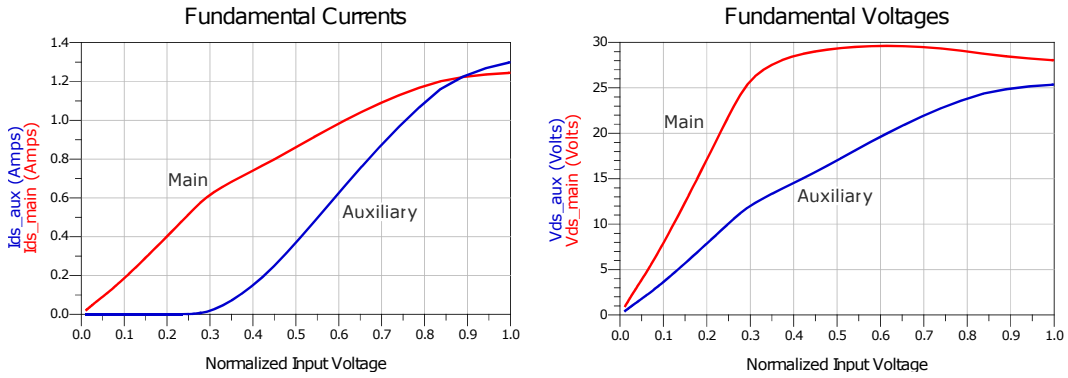


Figure 3.15: Magnitude of Fundamental Voltage and Currents

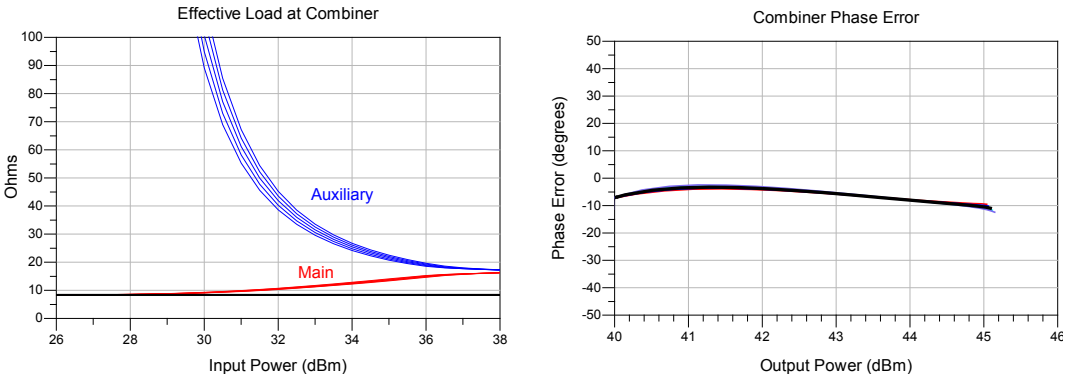


Figure 3.16: Load and Phase Relationship at the Output Combiner

design often has significant variance which it is useful to monitor and attempt to correct or balance with another part of the design.

The second plot shows the difference between the phase of the currents coming from the Main and Auxiliary amplifiers into the common node of the combiner. In this example there are no transmission line elements forming the combiner. In a practical design, the actual point of current combining will be a distributed area within an intersection of multiple transmission lines, or inside another microwave component such as a hybrid combiner. This introduces some uncertainty about

what the exact desired value should be. In this case, ideal constructive interference of the waveforms will be at a phase difference of 0°.

The phase offset can be affected by almost any modification to the circuit, meaning it needs continual correction throughout the design steps. An error in the phase offset causes changes in power output, efficiency, load modulation, and other metrics, often without a clear connection to the modification being made. This can cause confusion and attempts at resolving the issue in the wrong areas. Having a clear view of the combiner phasing allows the issue to be identified directly and resolved properly.

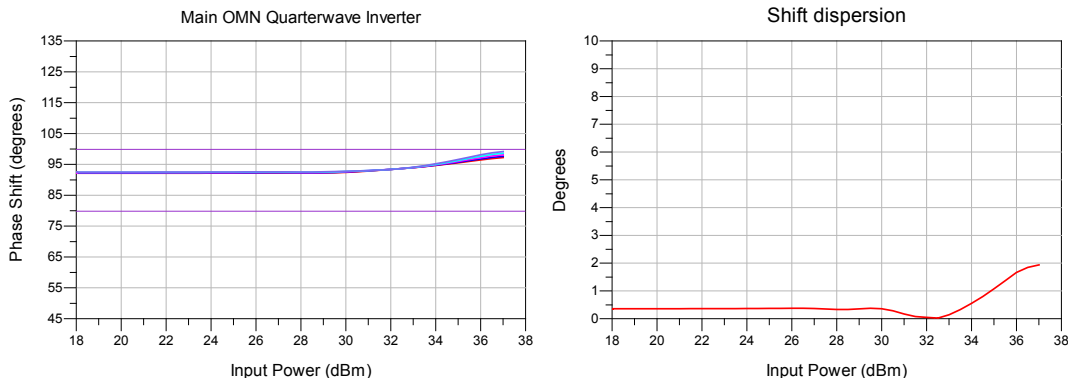


Figure 3.17: Phase Shift and Dispersion of the Auxiliary Quarterwave Inverter

This portion of the template's data display is illustrated by Figure 3.17. The Doherty design involves at least one impedance inverter, frequently implemented with a quarterwave transmission line impedance inverter, and other phasing elements. The behavior of these elements versus frequency and power is critical to the architecture and needs to be monitored and controlled. This display shows both the absolute phase behavior and the dispersion versus input power. In this ideal

design the inverter's length self-adjusts to be perfect for the simulation frequency so the dispersion is under one degree until the transistors are heavily saturated.

3.5 SUMMARY

The design template includes over two dozen plots which present both a broad overview of the amplifier's behavior and specific, key values particular to the Doherty architecture. Visualizing a consistent set of parameters and metrics throughout the design process, from ideal elements to EM analyzed PCB, improves the mapping of theory to final behavior and increases designer visibility into the causes of nuanced interactions. The design template is flexible to other target specifications and extendable to include other design techniques. By acknowledging the inevitable non-ideal nature of the devices and circuits in a real application, the template enables designers to apply their domain knowledge and techniques with the aid of pre-configured testbenches and measurement displays.

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4

DESIGN AND IMPLEMENTATION OF A DOHERTY AMPLIFIER

The Doherty design template constructed in chapter 3 provides the base design and detailed data displays to analyze the behavior and efficacy of each primary component. The template was presented using near-ideal transistors and ideal components to focus on the template itself.

This chapter describes an RFPA circuit designed using non-linear models of commercially available transistors to investigate and demonstrate the applicability of the design template to realistic transistors and non-ideal circuit components. The design uses industry standard GaN HEMT transistors and RF PCB substrates and focuses on the size of the final design to best reflect the requirements of real-world use.

4.1 PERFORMANCE OBJECTIVES

The most common use-case in communications for high-efficiency, high-power RF amplifiers is cellular communications, as described in Section 1.1.1. The requirements of a 5G C-band system PA have been used to guide the selection of

performance objectives. The specifications are to operate between 3.4-3.8 GHz, $P_{out,max}$ >40 W, a gain of 10 dB, and to work with a PAPR of 8.5 dB.

PROPERTY	TARGET
Frequency	$3.4 - 3.8$ GHz
Output Power	40 Watts
Gain	10 dBm
Efficiency	40 %
PAPR	8.5 dB

Table 4.1: Performance Objectives

4.2 TRANSISTOR SELECTION

To achieve exactly 8.5 dB of OBO, the power ratio of the devices given by Equation 2.24 is $\simeq$ 1.7, which is difficult to obtain with off-the-shelf components. On the other hand, a ratio of 2 is much easier to acquire with standard compenents, and should lead to a conservative OBO of $\simeq$ 9.5 dB. It is usually necessary and beneficial to bias the Auxiliary transistor at a point in deep class C which impacts the ability to fully reach the transistor's potential current. Having extra potential power available from the Auxiliary will provide a margin within the design to reach the required Doherty backoff point. Considering the target output power is in excess of 40 W, Cree Wolfspeed GaN on Silicon Carbide die transistors with

nominal output power of 15 W (CG2H80015D) and 30 W (CG2H80030D) were selected. These transistors have the additional benefit of being readily available and accurately characterized. Since the expected maximum voltage on these two devices is the same, the maximum currents are therefore also in a 2:1 ratio, meaning that the common load will be modulated by 3:1 on the Main side and 1.5:1 on the Auxiliary side.

Figure 4.1 shows this selection process graphically. The target breakpoint of 8.5 dB is selected and used to identify the P_{aux}/P_{main} ratio which results in that breakpoint. The nearest purchasable ratio is selected, 2.0, and the realizable breakpoint found.

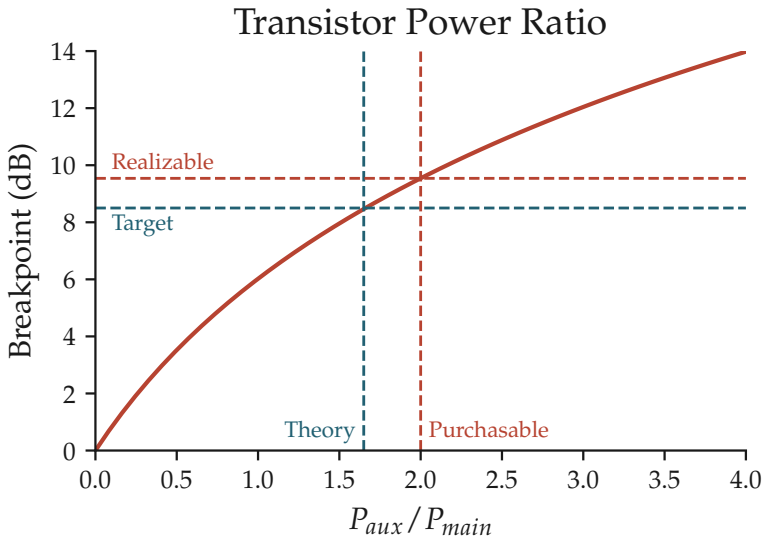


Figure 4.1: Relationship between target PAPR and transistor power selection

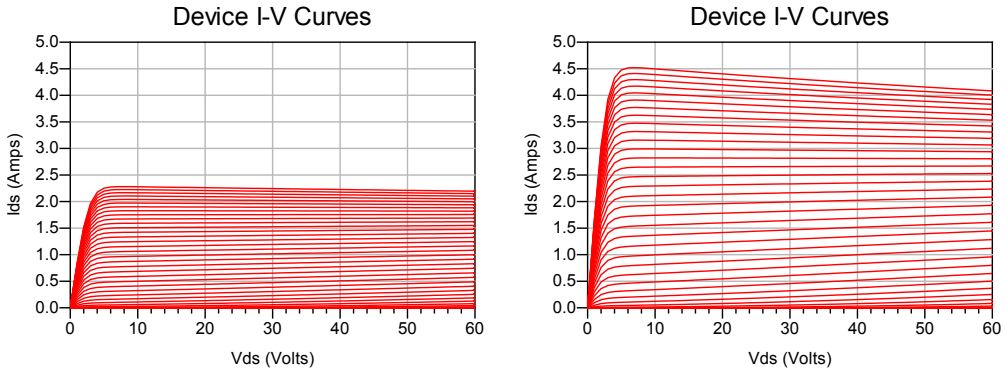
The optimum intrinsic load impedance of the devices can be estimated as:

$$R_{\text{opt}} = \frac{2(V_{\text{DD}} - V_{\text{knee}})}{I_{\text{max}}} \tag{4.1}$$

	CG2H80015D	CG2H80030D
I_{max}	2.28 Amps	4.49 Amps
V_{knee}	4 Volts	4 Volts
R_{opt}	21.2 Ohms	10.7 Ohms

Table 4.2: Static approximation characteristics of the devices

where V_{DD} is the drain bias voltage, V_{knee} is the knee voltage and I_{max} the maximum device current. For each device, these values can be read from the DCIV simulations of the devices, see Figure 4.2a and 4.2b, leading to the results of Table 4.2.



(a) CG2H80015D (b) CG2H80030D

Figure 4.2: DCIV Results simulated in ADS

There is now enough information to start running a basic AC simulation with ideal current sources. This will show how the ideal load modulation will work in a perfect Doherty that uses these devices to target the specified OBO. See Figure 4.3 that shows the simulation template and Figure 4.4 for the load modulation at the Main and Auxiliary devices.

The AC simulation uses the I_{max} values from Table 4.2 for the current generators and calculates ideal component values for the two transmission line quarter wave

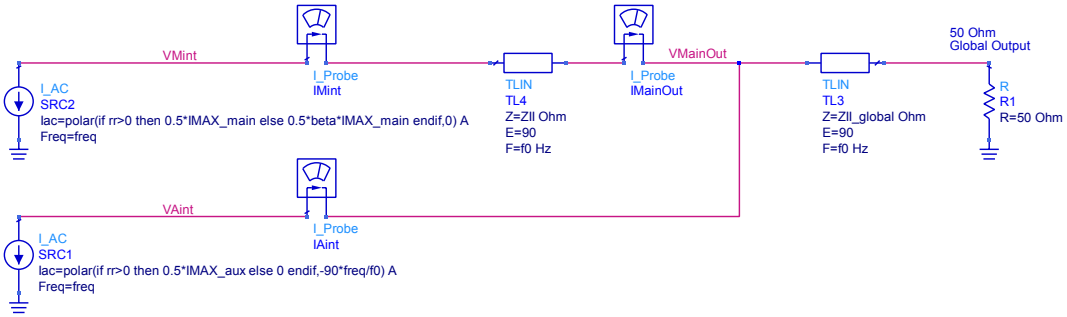


Figure 4.3: AC schematic of an ideal Doherty

impedance inverters using the equations shown in Chapter 2. The plots show the achieved $V_{\max}$, real component of $R_{\text{load,intrinsic}}$, and the reactive component of the load. The top row shows the results of the Main at the OBO breakpoint, labeled with 'rr=0.0', and at the peak power condition, labeled with 'rr=1.0'. The bottom row shows the Auxiliary at the peak power condition.

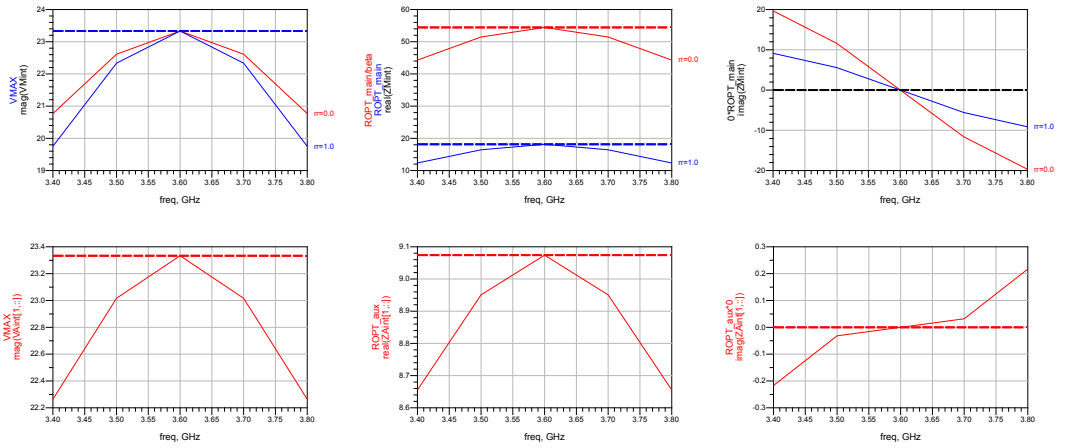


Figure 4.4: AC simulation results of an ideal 2:1 Asymmetric Doherty

The first column shows the voltage developed at the current sources, both very close to the maximal theoretical 24 V given the 28 V drain supply voltage and avoiding the 4 V knee region. The plots in the middle column show that at 3.6 GHz the Main transistor is loaded with 54 Ω at the OBO breakpoint, 19 Ω at peak power,

and the Auxiliary is loaded with 9 Ω at peak power. These values are close to fully utilizing the potential power of the transistors.

The load impedances deviate from the ideal as frequency moves away from the center of the targeted band due to the phase length of the transmission line inverters being less than or greater than 90°. The impedance decreases as it diverges from the center, leading to an easy improvement in overall performance by increasing the target load such that the average error in impedance is reduced within the bandwidth. This optimization has been analyzed in depth in literature [75].

The third column of plots shows the reactive component of the effective loads, which ideally would be completely real. Even in this AC simulation with ideal transmission line elements, the change in phase length as frequency is swept causes the load to move from inductive to capacitive. The Auxiliary's load reactive component is approximately 1 % of the real component and is unlikely to cause design or performance issues. The Main however has a reactive component which is up to 30 % magnitude of the real component. The reactive component is greater at the OBO point than at saturation, but at both points its magnitude is significant relative to the real load. These loads are shown on a Smith chart in Figure 4.5 where the sweeping behavior can be more clearly seen.

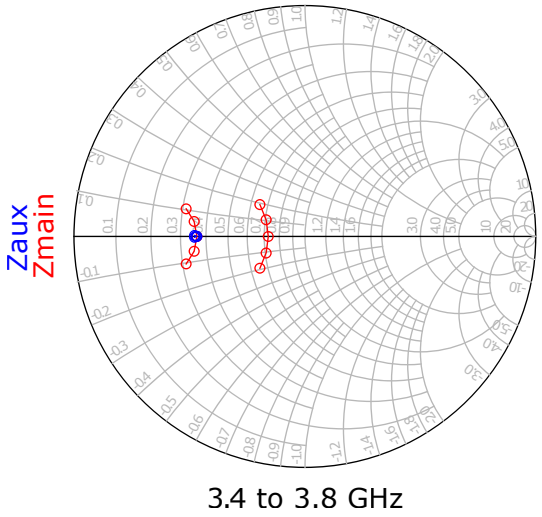


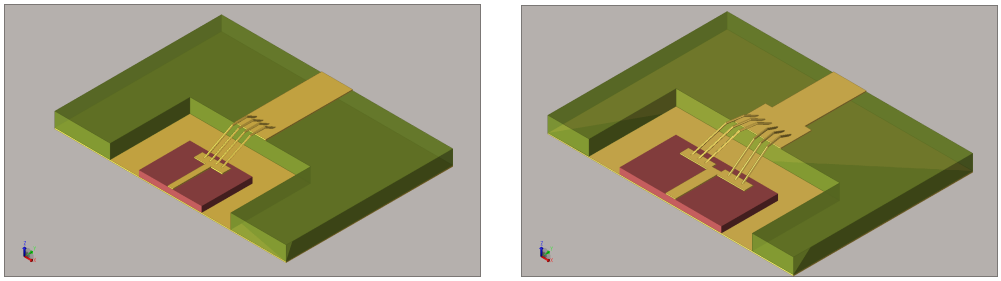
Figure 4.5: Main and Auxiliary Load Modulation at Breakpoint and Saturation

4.3 PARASITICS - DIE TO PCB TRANSITION

The main difficulty in high frequency power amplifier design is dealing with reactive and parasitic effects of the transistors, which must be compensated for to avoid losing output power and efficiency. These effects and their compensations both limit the achievable bandwidth of the design.

Choosing bare die devices instead of packaged ones gives more options to control the parasitics of the interconnection between the device and the microstrip networks, but does not allow elimination of them completely. In particular, the drain and gate device pads will need to be connected to the microstrip using bond wires. The bond wires contribute a series inductance, followed by a small shunt capacitance caused by the landing pad on the PCB. Design started with selection of a mounting method for the dies and the launch to the PCB. The two principal

options were mounting the die directly to the PCB top layer or mounting to a metal carrier through a cutout in the PCB.



(a) CG2H80015D (b) CG2H80030D

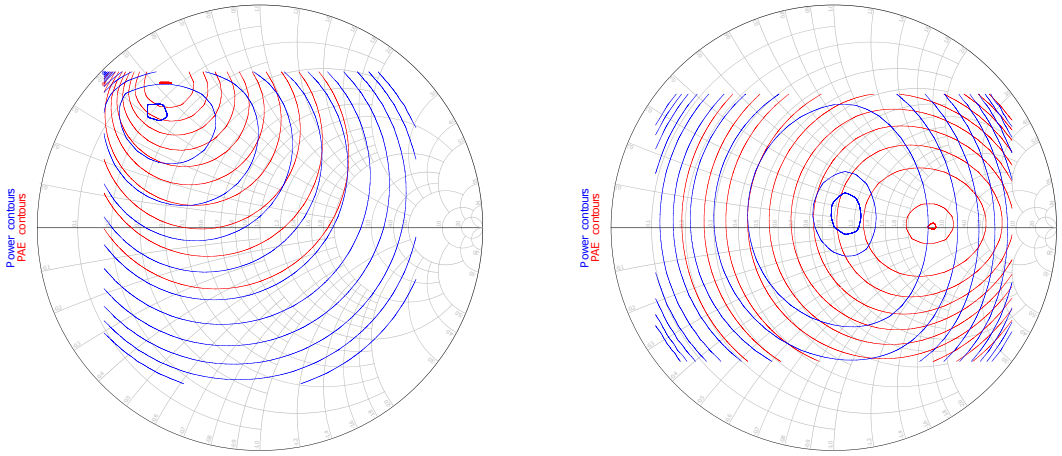
Figure 4.6: EMPro Models of GC2H Transistor Die to PCB wirebonds

A 3D Finite Element Method (FEM) simulation has been performed to predict the 2-port passive network that represents this connection, which results in a dominant, equivalent inductance at the design frequency band. With the goal of minimizing this inductance, the active device will be placed within a PCB recess as close as possible to the PCB walls and die attached directly to the underlying metal carrier. Bonding the die to the carrier also provides the lowest thermal resistance between the transistor and heatsink. The maximum number of bond wires that would fit on the device pads was selected. The equivalent inductance L_{BW} for the two devices' launchers have been estimated as 0.22 nH for the Main, and 0.31 nH for the Auxiliary by converting the S-Parameter results.

$$\begin{aligned} Y &= \text{stoy}\,(S) \\ L &= \frac{-\Im(1/Y_{12})}{\omega} \end{aligned} \tag{4.2}$$

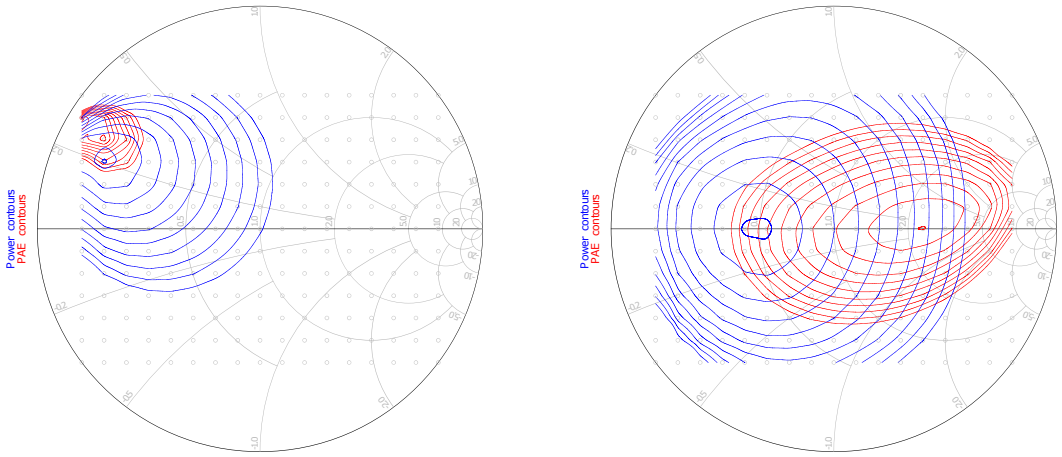
The dominant reactive effect at the output of a transistor however is capacitive, and related to the drain-to-source and drain-to-gate capacitance. For PA design purposes, it is better to consider the output capacitance as a behavioral capacitive response rather than relate it directly to physical capacitance within the device. To do so, the optimum power load versus frequency can be analysed to see if it can be approximated with an admittance with constant conductance ($1/R_{OPT}$) and negative susceptance proportional to frequency, which means the perfect compensation for an equivalent output capacitance C_{OUT}.

The optimal intrinsic load for both power and efficiency is expected to be purely real. A fundamental Load Pull simulation shows the impact of the parastics in Figures 4.7a and 4.8a. Even a bare die transistor will have output parasitics more complex than just a shunt capacitance, however this is expected to be the largest contributor. The value of C_{OUT} was estimated by adding a negative shunt capacitance between the drain and source nodes of each transistor. The value of these capacitances was varied until the optimal points lay on the real axis as shown in Figure 4.7b and 4.8b. The final estimate is 1.35 pF for the Main device, and 2.7 pF for the Auxiliary device. These values were tested across the frequency band of interest and no significant variation was found. The power contour optimum remained at a real value and the PAE optimum moved minimally, causing less than a 1 % decrease in efficiency.



(a) Bare Die (b) Deembedding 1.35 pF Shunt Capacitance

Figure 4.7: Load Pull of 15 W Die at 3.6 GHz



(a) Bare Die (b) Deembedding 2.7 pF Shunt Capacitance

Figure 4.8: Load Pull of 30 W Die at 3.6 GHz

4.3.1 *Main Amplifier*

To achieve a compact layout, one option for approaching the Doherty design is to use the Main matching network directly as the Doherty impedance inverter [76].

While the most common way of realizing impedance inverters in Doherty PAs is by quarter wave transmission lines, an impedance inverter can also be realized using lumped components, and the equivalent output capacitance and inductance of the device can be part of the lumped impedance inverter. Topologically, the output of the device looks like a low-pass filter, with a shunt C_{OUT} and a series L_{BW}. This could be completed by another series inductance L_{ADD} and another shunt capacitance C_{OUT} to create a symmetrical low-pass Π network. This network will behave as a perfect impedance inverter of equivalent characteristic impedance Z_0 at frequency ω_0 if all the three branch impedances have the value $|Z_0|$. Therefore, by choosing

$$Z_0 = -X_{C_{OUT}} = \frac{1}{\omega_0 C_{OUT}} \tag{4.3}$$

we can complete an impedance inverter by imposing:

$$L_{OUT} = L_{BW} + L_{ADD} = \frac{Z_0}{\omega_0} \tag{4.4}$$

Having imposed an impedance inverter with Z_0, and by knowing the impedance at backoff is $Z_{main,obo} = 3\ R_{main,opt} = 63.6\,\Omega$, the common node impedance can be determined:

$$Z_{CN} = \frac{Z_0^2}{Z_{main,obo}} = 14.62\,\Omega \tag{4.5}$$

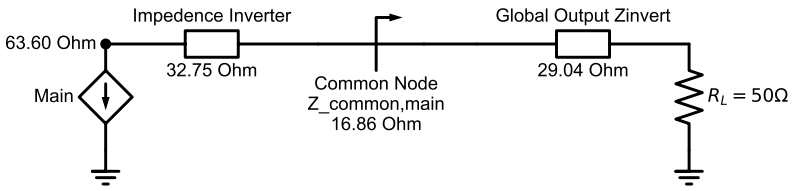


Figure 4.9: Main Output Matching Network with Transmission Lines

The ideal transmission line values were then converted to lumped element components using these formulas:

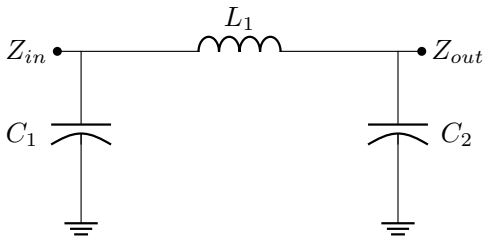


Figure 4.10: Equivalent model of a transmission line using lumped elements

$$\begin{aligned} Z_0 &= \sqrt{Z_L Z_{in}} \\ &= \sqrt{\frac{R + j\omega L}{G + j\omega C}} \end{aligned} \tag{4.6}$$

$$\begin{aligned} X_L &= Z_0 & X_C &= Z_0 \\ &= 2\pi f L & &= 1/\left(2\pi f C\right) \\ L &= \frac{Z_0}{2\pi f} & C &= \frac{1}{2\pi f Z_0} \end{aligned} \tag{4.7}$$

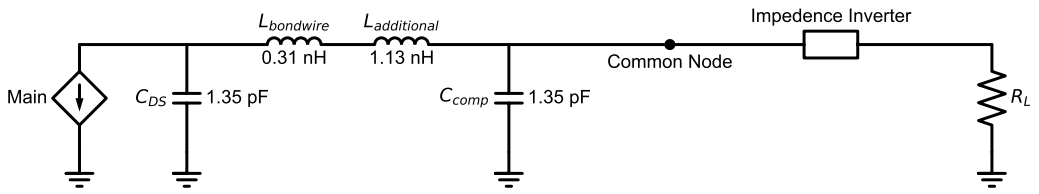


Figure 4.11: Main Output Matching Network absorbing parasitics

Initial simulations with a single quarterwave line matching the common node to the external 50 Ω load showed significant deviation in the achieved Z_{CN} across the frequency band of interest as the transformer's length deviated from the ideal 90°. This error which was then increased multiplicatively by the load modulation effect. A two stage quarterwave matching was chosen to reduce this source of error across the required bandwidth [77].

4.3.2 *Auxiliary Amplifier*

Since the common node impedance is now forced by the output capacitance of the Main, the Auxiliary device should not be connected directly at the common node as this impedance will not be the optimum one. It was chosen to use the same approach as the on the Main; to build a lumped impedance inverter using the output capacitance, in this case of equivalent impedance of $Z_{0,\mathrm{A}} = 16.37\,\Omega$, which then requires a load $Z_{\mathrm{A}} = Z_{0,\mathrm{A}}^2 / R_{\mathrm{OPT,AUX}} = 25.0\,\Omega$. As Z_{A} is forced by the output capacitance of the Auxiliary, an additional matching network is required to reach Z_{CN}. Additionally, the output matching of the Auxiliary must be non-inverting for the Doherty to operate correctly, therefore another impedance inverter, this

time made with a quarter-wave transmission line, is added. The impedance of the latter is chosen so that the impedance observed at the common node by the Main, which will be modulated at 1.5 Z_{CN}, is transformed to Z_{A} (denoted $Z_{common,aux}$ in Figure 4.12).

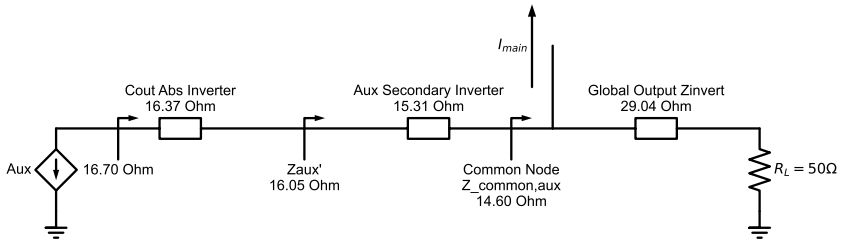


Figure 4.12: Auxiliary Output Matching Network with Transmission Lines

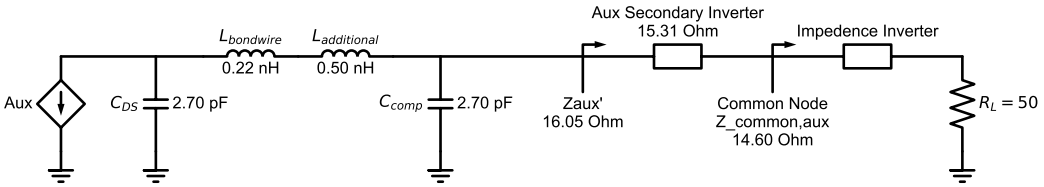


Figure 4.13: Auxiliary Output Matching Network absorbing parasitics

4.3.3 *AC Simulation*

The introduction of the equivalent transmission lines using lumped element components and an additional inverter on the Auxiliary's output are likely to have changed the performance of the network. The AC Simulation template shown in Figure 4.3 can be extended to assess these modifications.

The simulation results show that the new networks still reach their targets at the design center frequency of 3.6 GHz, but the trends are now monotonic with

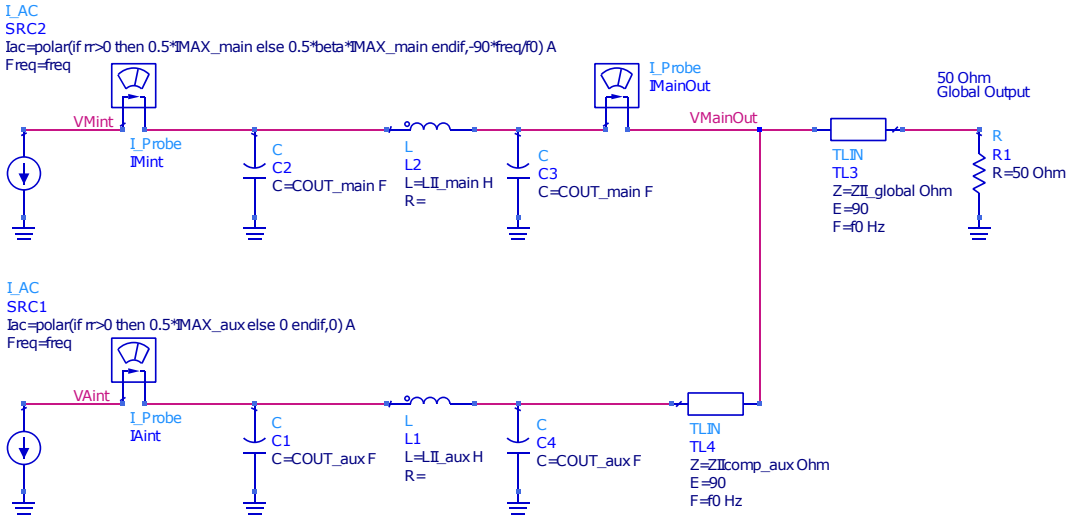


Figure 4.14: AC Simulation of the Doherty with lumped element inverters

frequency rather than symmetrical around the center frequency, compared to the results in Figure 4.4.

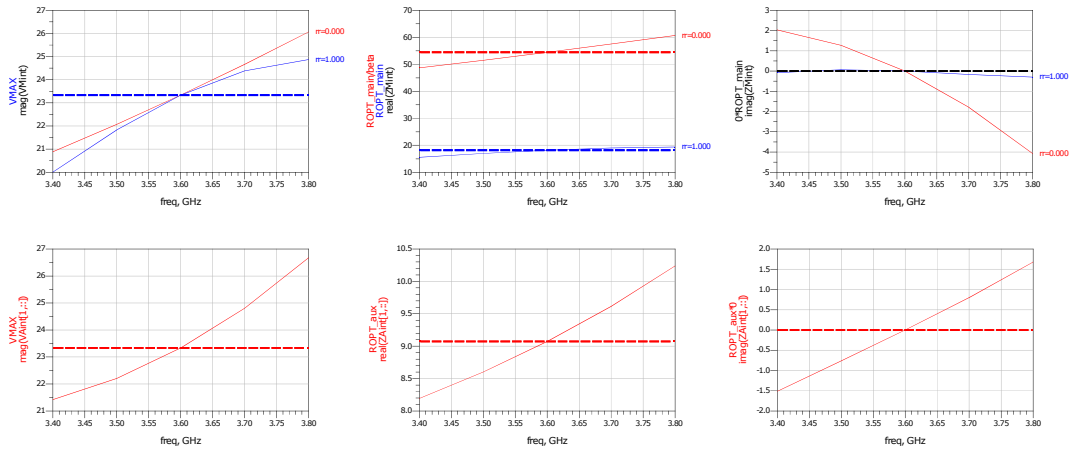


Figure 4.15: AC Simulation Results of a Symmetric Doherty

This completes the theoretical Doherty combiner, which will work ideally at the frequency ω_0 and gives a solid reference to take the design forward. However, to design with real device models over a significant bandwidth, it is necessary to keep

an eye on the transistors loading and performance in a large signal simulation environment.

4.4 ACTUAL COMBINER DESIGN

With the ideal layout of the output network chosen, the techniques of the design template can be applied to inform the design decisions required to produce a manufacturable circuit.

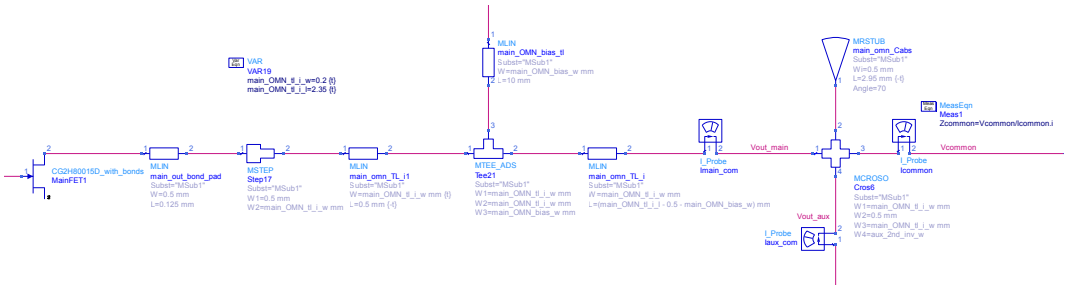


Figure 4.16: Final schematic of the Main output inverter

The Main amplifier's output matching network is a single impedance inverter between the transistor's intrinsic generator plane and the common node. The lumped element transmission line model shown in Figure 4.11 uses the output capacitance of the transistor and inductance of the drain bondwires as the first portion of the inverter and extends them with an $L_{\text{additional}}$ series inductance and a shunt capacitor of identical value to complete the transmission line. While there are ideal equations for determining the dimensions of a microstrip transmission line with an equivalent inductance, these do not account for the effects of a bond wire landing pad, a branching trace for bias injection, and the geometry of a four

way intersection to join the Main and Auxiliary lines with the combined output and shunt capacitance. Figure 4.16 shows the final ADS schematic of the microstrip elements present in the Main device's output inverter. The shunt capacitance is created using a radial stub as it is a critical and sensitive part of the matching network. The microstrip stub could be analyzed in the existing electromagnetic simulation and did not introduce the complexity of parasitics inherent to the solder pads and component geometry of an SMD capacitor.

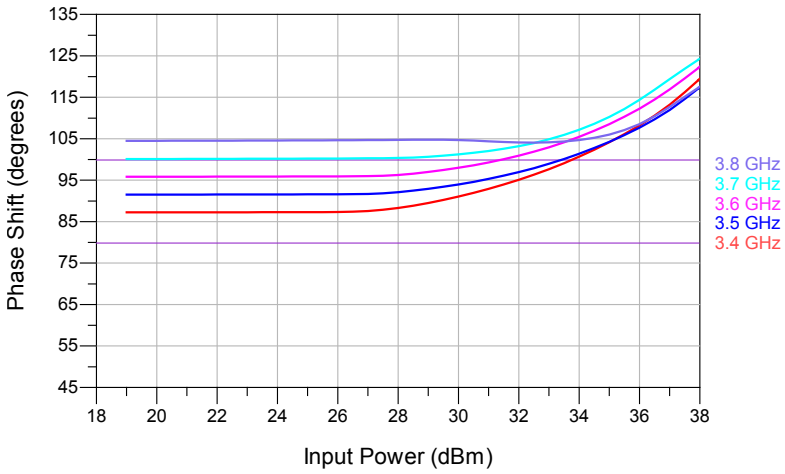


Figure 4.17: Simulated phase shift of Main output inverter

Figure 4.17 shows the phase shift versus power for five frequencies across the fundamental band. In backoff, the circuit is only influenced by the Main transistor and the phase shift can be seen to vary from ∼86° at 3.4 GHz to ∼105° at 3.8 GHz. This is a 19° dispersion across the frequency band and is closest to the ideal 90° shift at 3.5 GHz, below the center of the frequency band.

The same approach when applied to the Auxiliary inverters shows that the phase shift converges close to 90° in the Doherty region when the Auxiliary transistor

is supplying power. The first stage inverter, absorbing the transistor parasitics, again uses a radial stub for the shunt capacitance and has a four-way intersection merging the microstrip elements together.

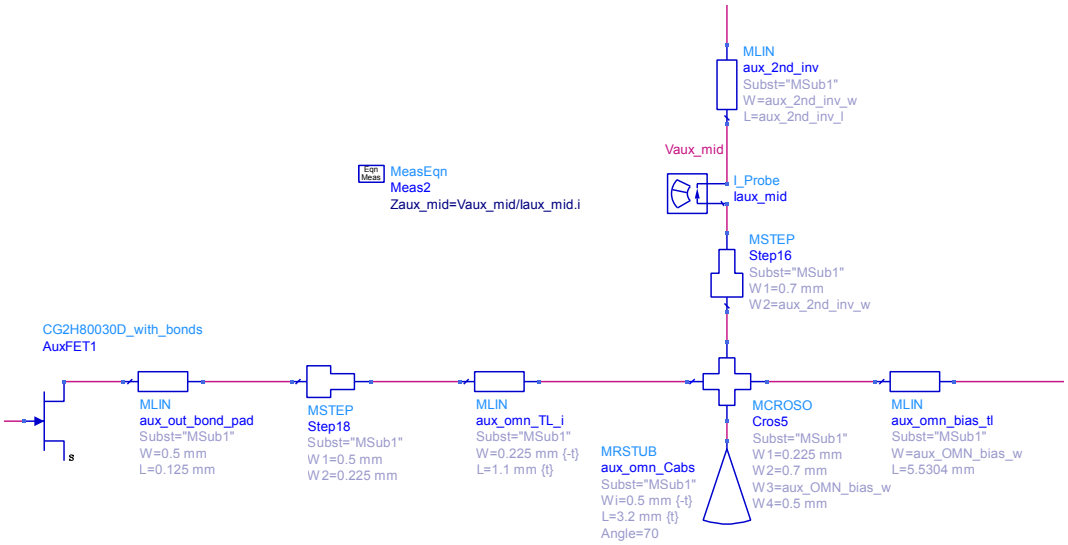


Figure 4.18: Final schematic of the Aux output inverters

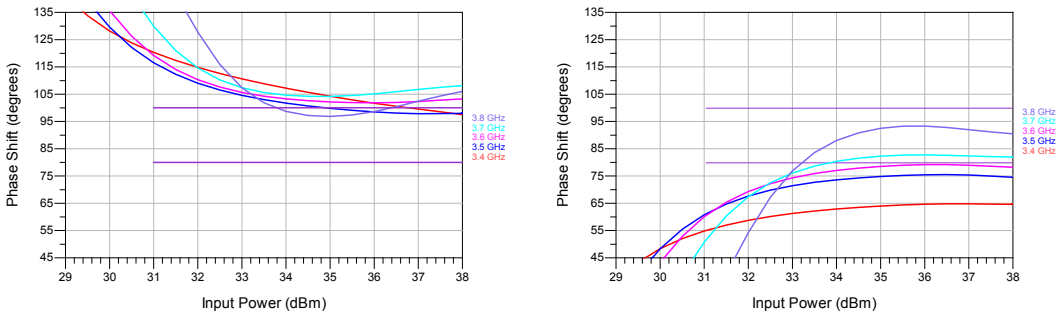


Figure 4.19: Simulated phase shift of Aux output inverters

A limitation in rigidly mapping theory to these simulated measurements is the distributed nature of the microstrip circuitry. The simulator can only probe the voltage and current at an intersection point between components, while the true analog behaviors occur continuously throughout the circuit. While the probed

values may not match ideal theory, the trends are useful to indicate approximate behavior and, subjectively, were even more useful in showing changes in behavior throughout the design process. In this specific case, the pair of inverters can be seen to combine to be very close to 180° in total, indicating that there will be a point in the middle of the microstrips which better divides the two into the target of 90° each.

4.5 KEY PERFORMANCE POINTS

4.5.1 *Output Matching Network*

The essence of the Doherty architecture is the load modulation, expected to be a purely real transformation at the intrinsic plane. Figure 4.20 shows the simulated loads swept across 3.4-3.6 GHz with higher frequencies indicated by darker lines. In both cases, the load impedances are higher at higher frequencies than at lower frequencies. The theoretical target impedances at the breakpoint and peak power are marked. The load modulation behavior is clearly visible, with the Main having a stable load up to approximately 29 dBm and the Auxiliary turning on and both impedances decreasing until deep compression is reached. The Auxiliary reaches its target load with the exception of the high edge of the band while the Main amplifier's load is not modulated sufficiently to reach the target.

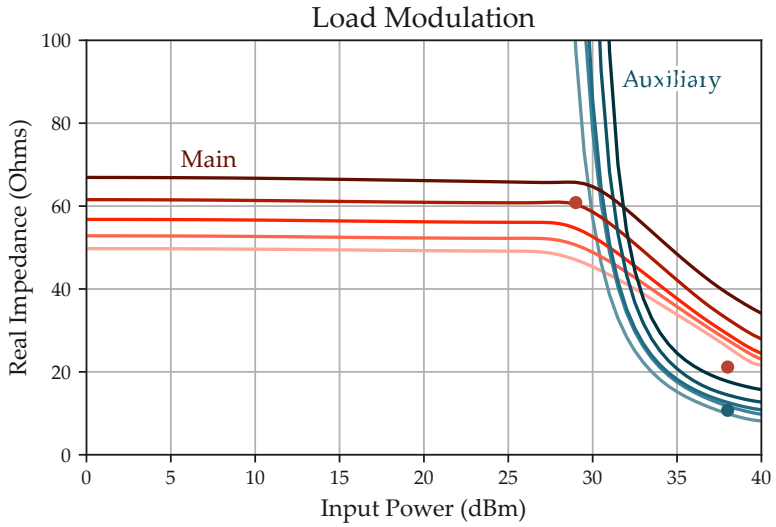


Figure 4.20: Intrinsic Load Modulation of Main and Auxiliary Amplifiers. Frequency sweep from 3.4 to 3.6 GHz in 100 MHz steps.

Viewing the loads on a Smith chart in Figures 4.21 and 4.22, it is apparent that both loads become reactive at points in the power sweep. The Auxiliary has a nearly perfectly real load throughout the sweep at 3.6 GHz, and at all frequencies the load is purely real both while shut off in backoff and when fully on at saturation. The Main amplifier's load becomes increasingly capacitive as power increases.

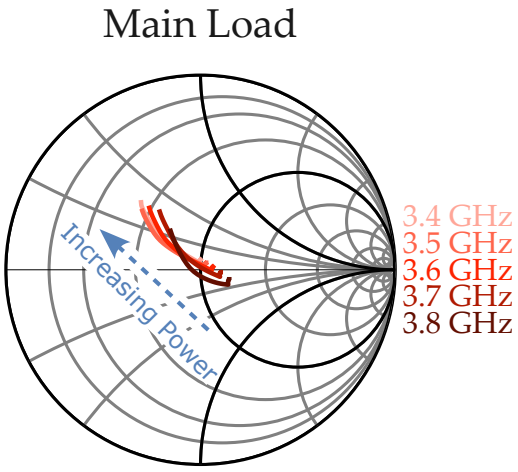


Figure 4.21: Load Impedance at the Main's Intrinsic Plane

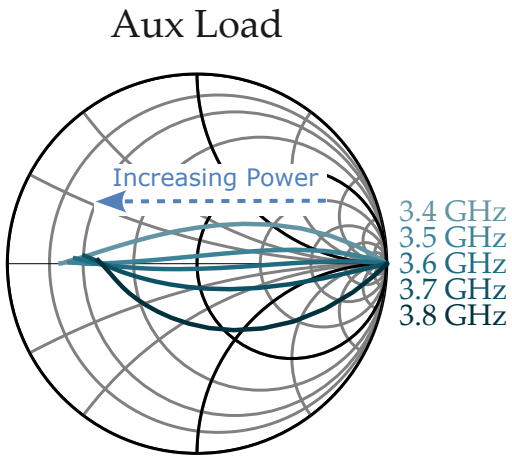


Figure 4.22: Load Impedance at the Auxiliary's Intrinsic Plane

Figures 4.23 and 4.24 show the current and voltage waveforms at the transistor intrinsic planes when driven by a 3.5 GHz tone at 35 dBm, mid-way between the Auxiliary turning on and peak power.

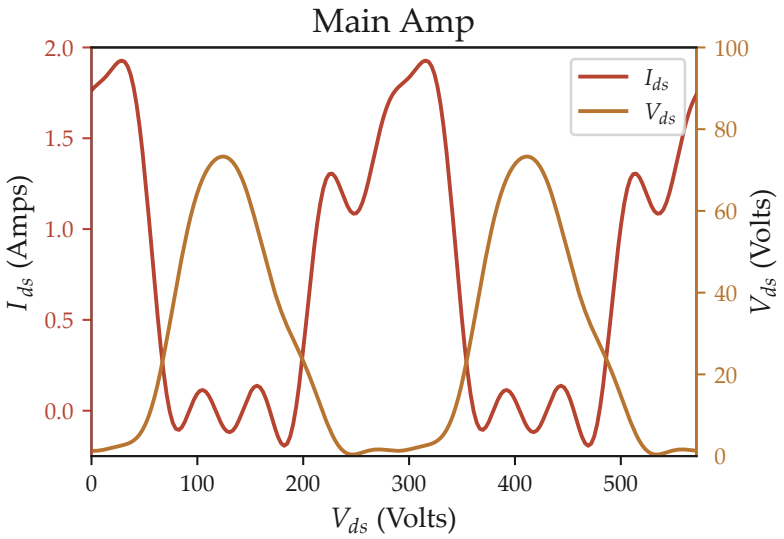


Figure 4.23: Intrinsic Waveforms of the Main Amplifier

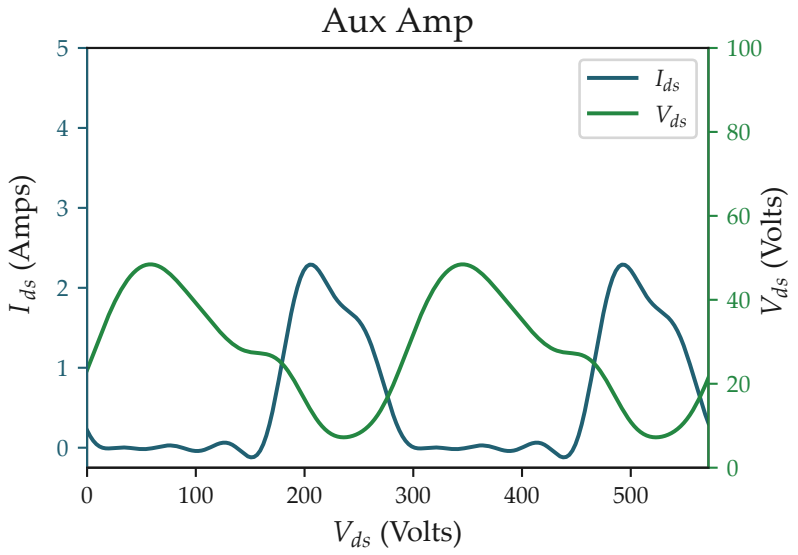


Figure 4.24: Intrinsic Waveforms of the Auxiliary Amplifier

The time-domain waveforms are useful for monitoring behaviors, such as the conduction angle of the amplifiers, as bias points are varied. However, viewing the dynamic loadlines provide a much clearer perspective on where some of the non-sinusoidal features of the waveform come from. Figures 4.25 and 4.26 show that the transistors are operating in class AB and class C. The Main amplifier shows evidence of being overdriven at this power level, with the voltage being clipped by the knee around 4 V. The Auxiliary clearly shows the effect of the load modulation, with its IV path traveling to almost exactly its $R_{\text{opt}}/2$, appropriate for being half-way through its useful power range. The IV path does not fully reach the knee so the efficiency will be somewhat lower than ideal.

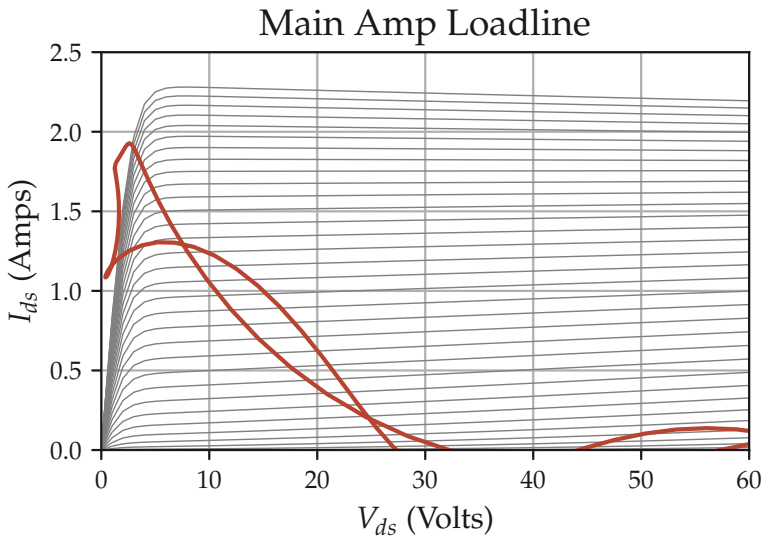


Figure 4.25: Intrinsic Loadline of the Main Amplifiers

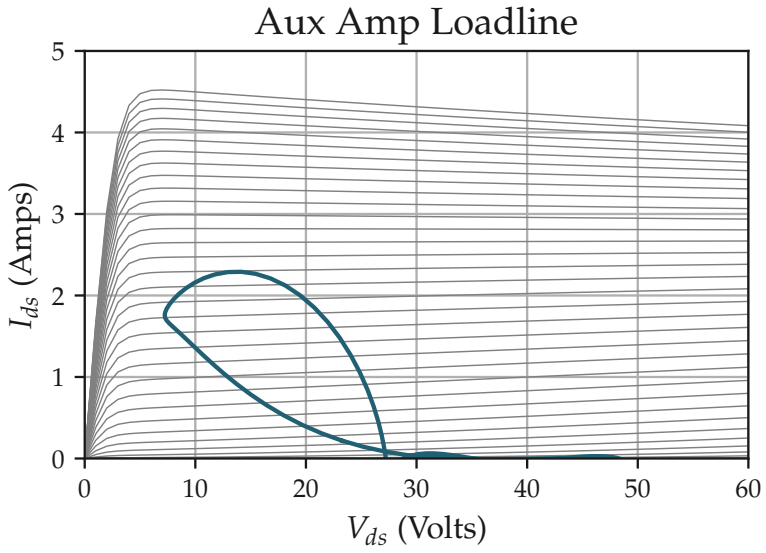


Figure 4.26: Intrinsic Loadline of the Auxiliary Amplifier

Focusing on the current and voltage magnitudes at the fundamental frequency, as seen in Figure 4.27, several key behaviors can be monitored. The left hand plot shows the Main supplying current immediately at small signal levels and the

Auxiliary beginning to supply current just as the Main starts saturating, around 7 volts V_{in}, equal to ~27.5dBm. The Auxiliary reaches a maximum of 2.5 A and the Main 1.25 A, a perfect 2:1 current ratio.

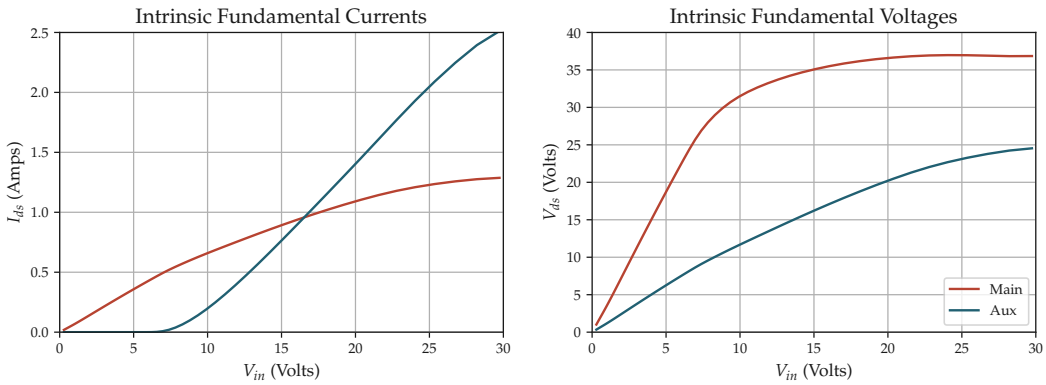


Figure 4.27: Intrinsic Fundamental Current and Voltage

The voltages show that the voltage on the Main rises quickly, as desired, until hitting a knee and saturating its voltage swing. The Auxiliary rises nearly linearly across the range.

4.5.2 *Amplifier Performance*

Having examined the load modulation behavior from multiple perspectives, it is appropriate to look at the higher level amplifier metrics to see if the design goals were met. As the selection of the Doherty architecture was primarily motivated by a need for efficiency, we examine this first. Figure 4.28 shows that significant success was achieved in obtaining the characteristic peak in efficiency at the OBO point

and in maintaining the efficiency through to $P_{\max}$. Additionally, the performance is very consistent across the full frequency band.

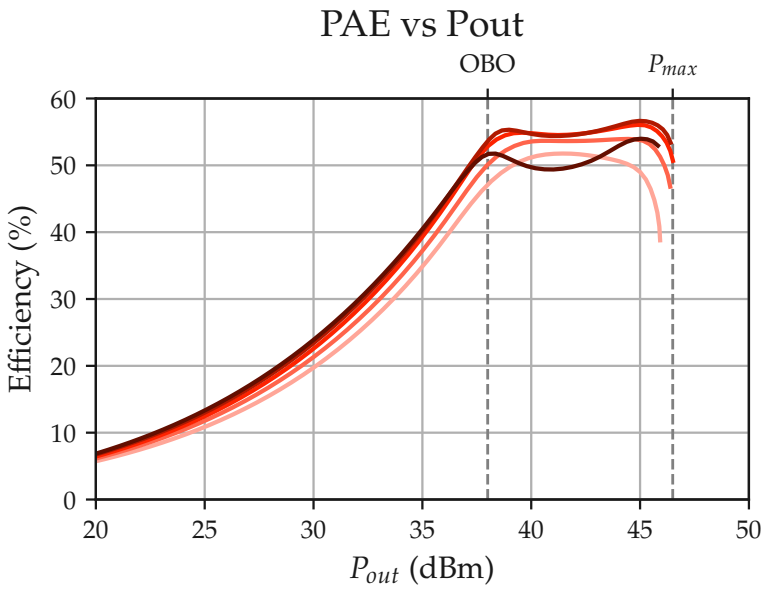


Figure 4.28: Power-Added Efficiency of the completed Doherty

The gain of the amplifier, Figure 4.29, is flat across frequency and power, with a small decrease as the Auxiliary amplifier turns on. This is expected as the Auxiliary is operating in deep class C in order to control its turn-on point and to maximize efficiency. The small signal gain has a variation of 1 dB across frequency and, with the exception of 3.8 GHz, maintains tight gain behavior across frequencies at all powers. The simulated power sweep extends until $\simeq$ 3.5dB of compression. The power sweep, Figure 4.29, unsurprisingly reflects the flatness and consistency of the gain results.

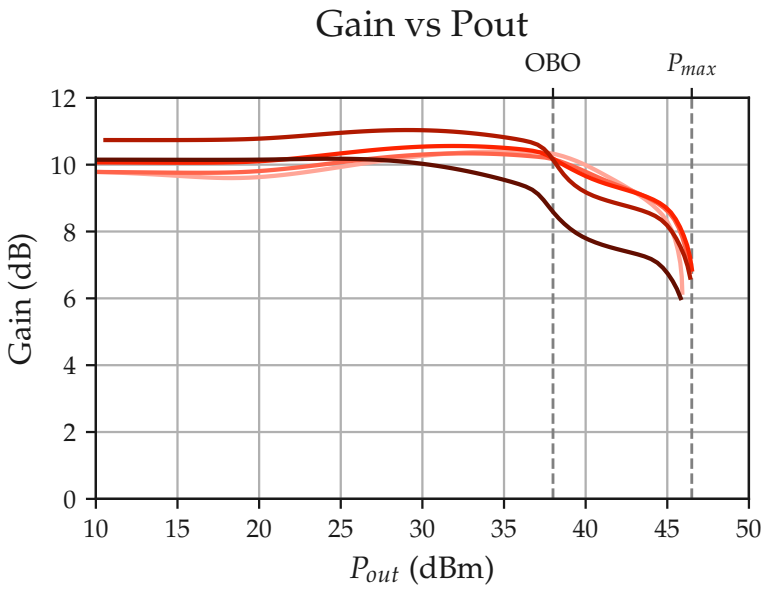


Figure 4.29: Power Gain versus Output Power

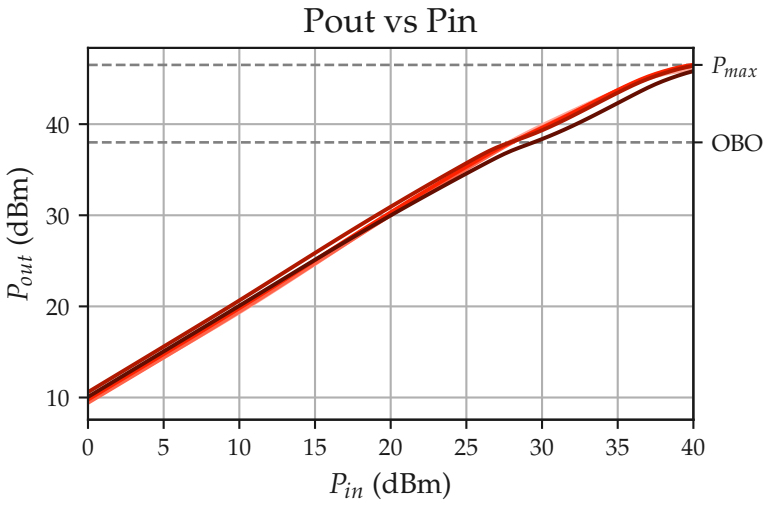


Figure 4.30: Output Power versus Input Power

Changing to focus on performance versus frequency, (4.31) shows that the amplifier reaches the full target power at the center of the band and falls only 0.5 dB on the edges. The maximum gain (4.32) varies 0.75 dB across the band of interest.

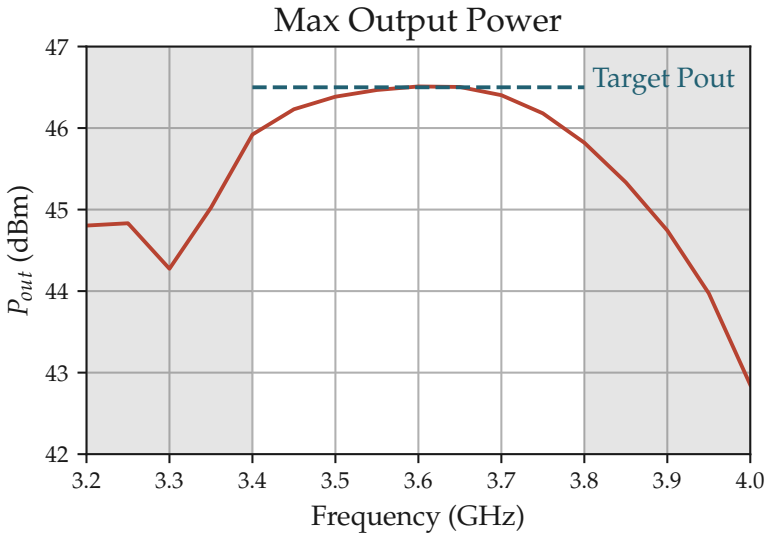


Figure 4.31: Saturated Output Power versus Frequency

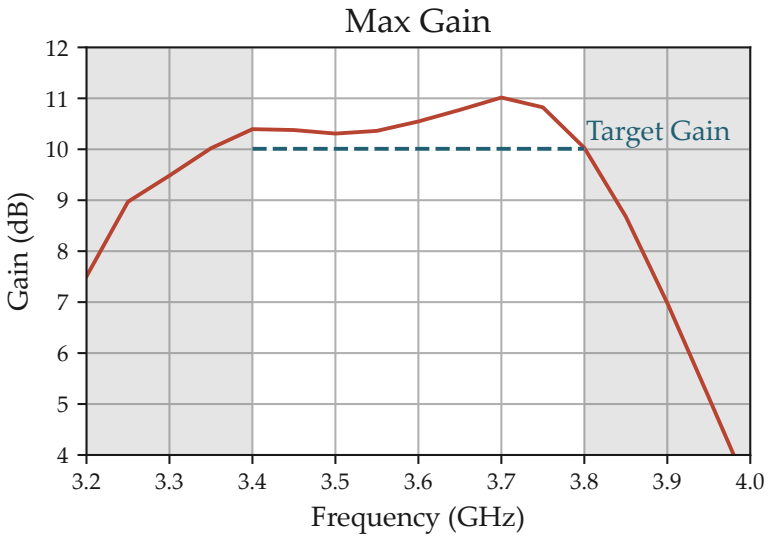


Figure 4.32: Maximum Gain versus Frequency

4.5.3 *Layout*

The final result of the design template process is a compact Doherty design. Figure 4.33 shows the circuit board layout with external connection pads labeled. This PCB was fabricated and Chapter 5 contains the measurements and analysis of the design's performance.

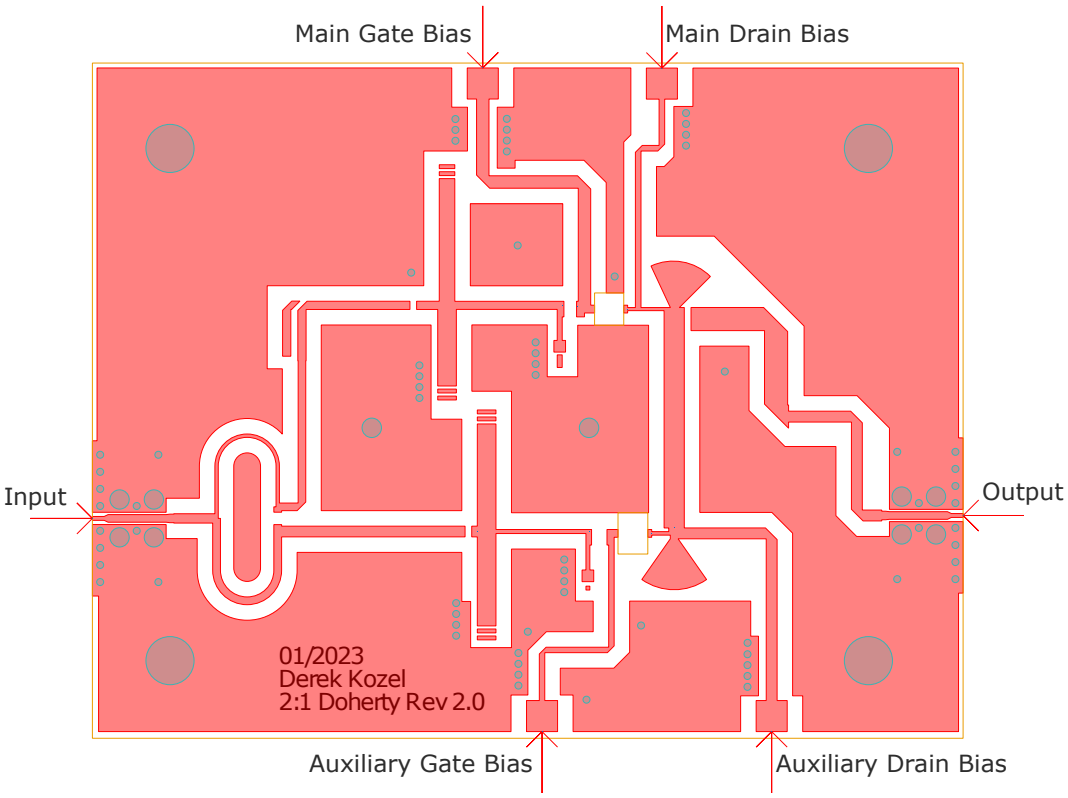


Figure 4.33: Single Input Doherty layout (56.1 x 43.5 mm)

4.6 CONCLUSION

This chapter has moved through the practical design of an RF power amplifier targeted at 5G cellular communications. The initial design exploration was performed using AC simulations and then moved to harmonic balance non-linear simulation of ideal and non-ideal versions of the design. A new Keysight ADS Schematic View was created for each stage of the design. These stages enable a systematic evaluation of the amplifier's performance, facilitating the identification and resolution of potential issues early in the development cycle.

The initial design utilizes ideal transmission lines and lumped elements to establish the basic functionality and performance targets of the Doherty power amplifier. The ideal transmission lines are replaced with microstrip lines, introducing a more realistic physical representation of the layout. This stage begins to account for the physical dimensions and characteristics of the transmission lines. The ideal lumped elements are subsequently replaced with accurate simulation models, provided by Modelithics for this research, of specific vendor components for passives. This step integrates commercially available components into the design.

Where applicable, microstrip inductors and capacitors replace the ideal passives. This further refines the design by incorporating components that closely mimic the physical layout and performance characteristics of the final product. At each stage, the schematic is adjusted to retain and optimize performance. This iterative

process ensures that the design evolves while maintaining or improving the key performance metrics.

EM simulation is used to refine the layout, especially in areas where multiple transmission lines converge or are in close proximity. Physical parasitics from the layout, which are not captured by the component models alone, are addressed in this stage. This step is critical for ensuring that the performance degradation introduced during physical layout is corrected where possible.

The approach of having a single, high-level testbench and data display used from initial concept to final PCB layout ensures a comprehensive understanding of the amplifier's behavior under various conditions, ultimately leading to a robust and optimized final design.

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5

MEASUREMENTS

As described in the preceding chapter, the Doherty Design Template was used to design an amplifier based on the requirements of a 5G small cell transmitter. This design used the Cree Wolfspeed CG2H die transistors to both focus on the non-linear behaviors of the transistor itself without packaging effects and to allow for a parallel experiment in minimizing the overall design size through beneficial use of the wire-bonds necessary to integrate the die with the PCB.

This chapter covers the fabrication and measuring of the amplifier including CW and modulated signals. The Design Template continued to be applicable in measuring the key performance indicators as the simulated design was converted into a manufacturable prototype layout. Several key metrics are directly compared, however many metrics simulated in the design template are infeasible to measure directly.

The Doherty Design template focused on the creation of a standard single-input Doherty design. This integrates a splitter to feed the input signal to the Main and Auxiliary and adjusts the relative transmission line lengths to optimize the phases of the amplified signals at the output combiner. This approach is useful as it allows the Doherty to function similar to other amplifier architectures with a single input

and output. However if the phasing is incorrect it is difficult to physically adjust the lengths on the PCB after fabrication. Additionally, a physical splitter provides a fixed ratio of power between the Main and Auxiliary.

It was decided to manufacture a variant of the design where the input splitter was removed to provide direct access to each amplifier. This dual input design would be used to characterize the Main in isolation and to examine the possible operating space for phase offsets and power splitter ratios. Once this operating space was measured, a set of points $\{P_{\text{in,main}}, P_{\text{in,aux}}, \theta\}$ were manually identified based on trade-offs between efficiency and output power. These points are maintained through the analysis and indicated on plots by emphasized markers. The single input design would also be fabricated and tested for overall system performance.

5.1 DUAL INPUT DOHERTY

5.1.1 *Fabrication*

The final dimensions of the amplifier, including bias networks and SMA connector footprints, is 56.1 x 43.5 mm. It is built on 10 mil (0.25 mm) thick Rogers 4350B substrate.

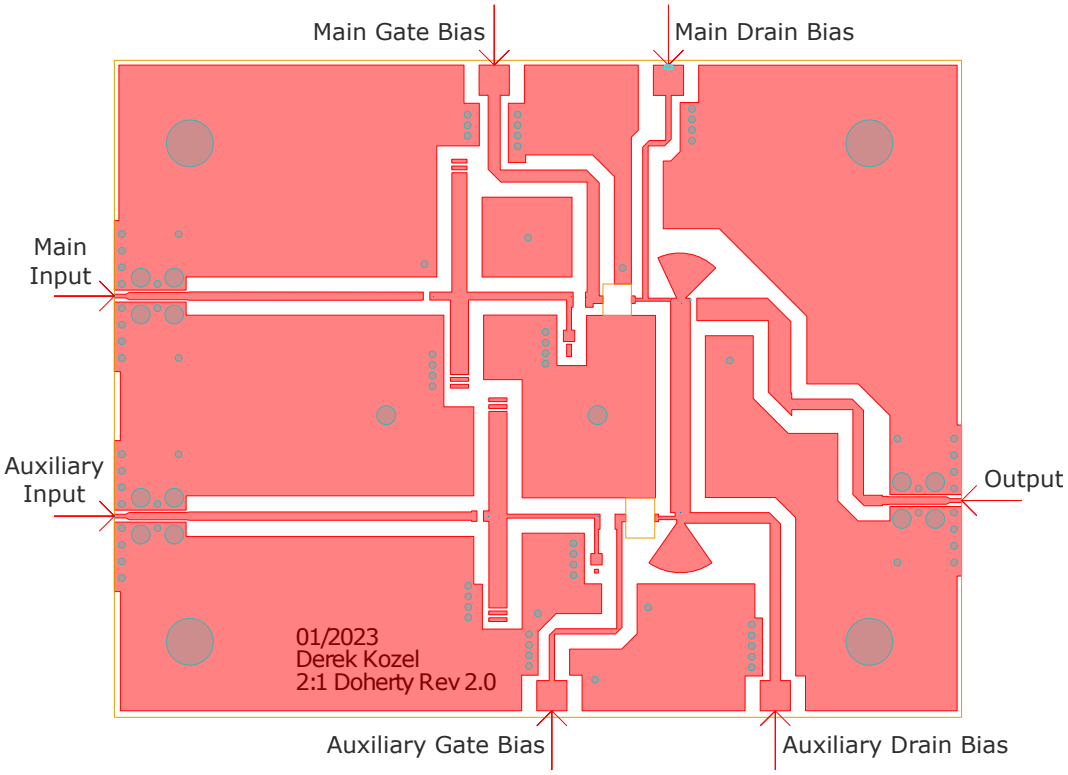

Figure 5.1: Dual Input Doherty layout (56.1 x 43.5 mm)

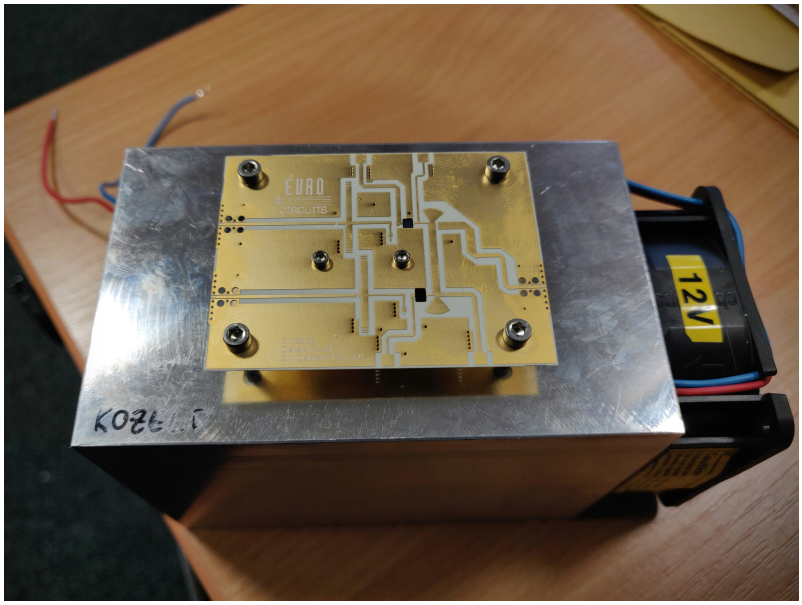

Figure 5.2: Dual Input Doherty test fit on heatsink

The PCB was bonded to a 4 mm thick copper plate using thermal epoxy and then mounted to a heatsink with a fan using thermal paste. The IconicRF team in Belfast supported this project by epoxying the transistor dies to the copper plate and wirebonding the dies to the PCB.

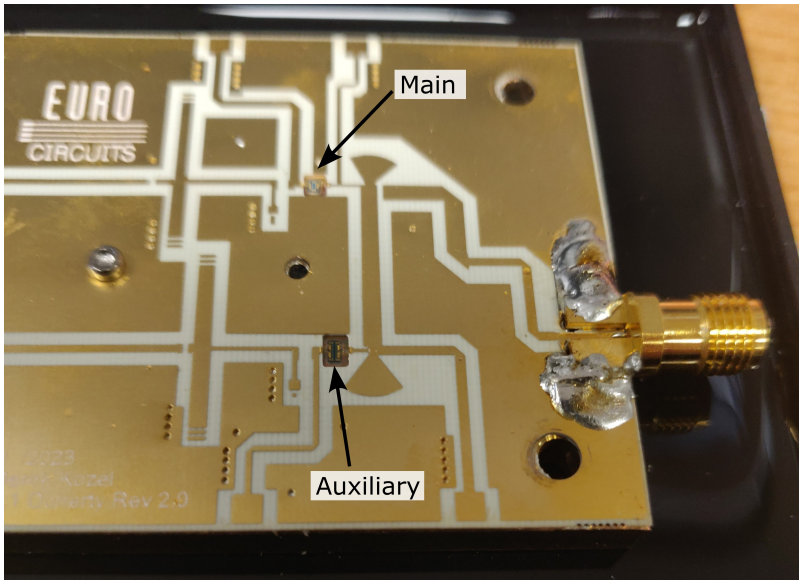

Figure 5.3: Cree Dies bonded to the PCB

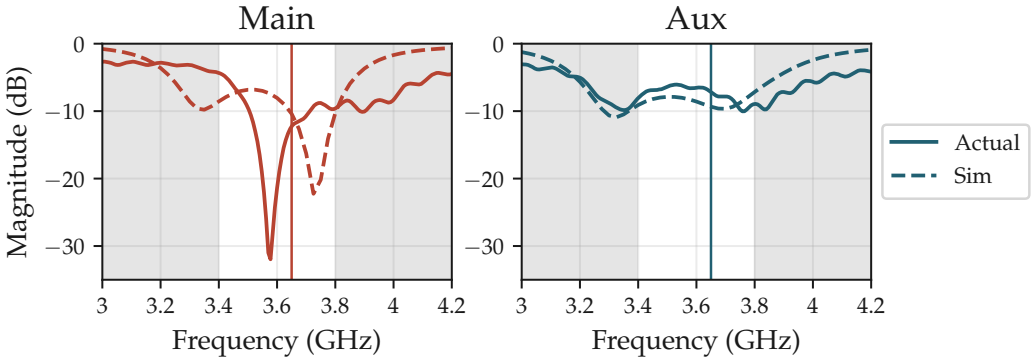

Figure 5.4: S_{11} Measurement versus Simulation

The biggest weakness of this design as manufactured is the input matching networks. As can be seen in Figure 5.4, the Auxiliary's input match performs nearly

identically to simulation, however the Main's input match has shifted higher in frequency by about 250 MHz, (a 7.5 % increase). Additionally the Main's input match was sensitive both in simulation and on hardware so attempts to retune the input match were unsuccessful. As a result, measurements were done at 3.65 GHz, indicated by the vertical line on each S11 plot.

5.1.2 *Measurement System*

System Overview

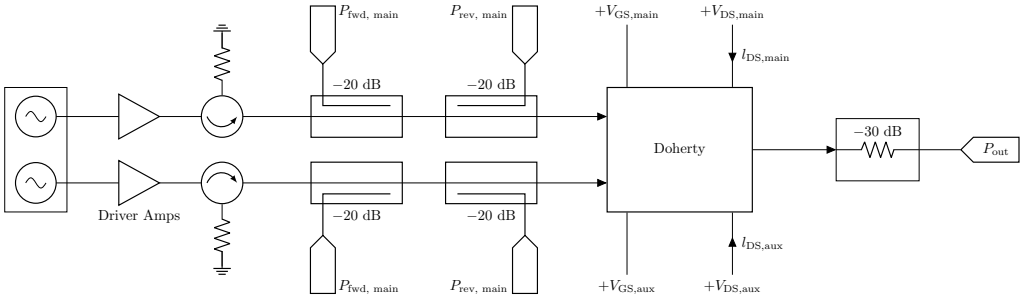

Figure 5.5: Dual input measurement system diagram

The measurement system is a two input, single output scalar network analyzer comprised of a two channel RF signal generator, directional couplers, and power meters. The high level diagram can be seen in Figure 5.5. It was developed by Bogusz [78] to support the characterization of Outphasing amplifiers and was built on by this work.

The system produces power readings of $P_{\text{fwd,main}}$, $P_{\text{rev,main}}$, $P_{\text{fwd,aux}}$, $P_{\text{rev,aux}}$, and P_{out}. In order to calculate efficiency, the system can read the voltage and current from a two channel power supply though in this design only one channel was used as both transistors used a common drain bias. The recorded values are $V_{\text{ds,dc}}$ and $I_{\text{ds,dc}}$.

The measurements were configured in three MATLAB source code files: InstrumentParametersCW.m, MeasurementParameters.m, and at the top of CW_meas.m.

The Anritsu MG3710A dual output signal generator is used as the source of input stimulus signals. It has several features which enable and simplify measurements of dual input amplifiers including the ability to share an internal local oscillator for both channels and to generate internal phase shifts on a per channel basis.

5.2 SOFTWARE ENHANCEMENTS

The system's control software is implemented in the MATLAB language and the source code was available to be modified. Several quality of life features were added as well as a series of modifications to the measurement process. The code was moved into Git version control and the version hash information was automatically embedded in each measurement results file. MATLAB's recommended code formatting was applied to all files and all warning messages were addressed.

The measurement results file already stored configuration data about the measurement system and was extended with additional metadata. The `author`, `bias_`

`main_gain`, and `bias_aux_gate` were added as static fields, set manually in the code as they did not change regularly. An addition was made to the code to prompt the user for a brief description of the measurement which was stored along with the current date and time in the results filename and as a property in the file.

The system's code initially displayed minimal information about the progress and status of an ongoing measurement. The existing log messages were reworked for clarity and detail and additional logging was added to provide information on the measurement configuration, current system behavior, and estimated time remaining.

More impactfully, the system allowed a variety of invalid configurations to be run, silently resulting in undesired behavior ranging from loss of phase offset repeatability to outputting the signal generator's maximum output power unexpectedly. This at best resulted in unusable data and at worst damaged or destroyed the attached DUT and potentially endangered components of the measurement system including the power meters measuring the forward direction power. `assert` is a MATLAB function which throws an error if the specified expression is not true. Listing 1 shows the addition of an assertion in the function used to set the generator's output power. While simple in its function, the check that the generator is actually set to the intended power level caught several instances when the generator power was set greater than 10 dB higher than expected. These errors most often occured due to limitations created by specific combinations of generator settings such as enabling the output attenuator hold feature.

```
function siggen_setpow(deviceObject, siggen_name, p0, siggen_t, varargin)
  switch siggen_name
  ...
  case {'MG3710A'}
    ...
    fprintf(deviceObject,...
      ['SOUR', num2str(varargin{end}), ':POW ', num2str(p0), ' DBM']);
    p_actual = str2double(query(deviceObject,...
      ['SOUR', num2str(varargin{end}), ':POW:CURR?']));

    assert(abs(p_actual - p0) < 0.1,...
      sprintf(['ERROR: Siggen channel %d could not be set to %.2f dBm.',
        'Actual power is %.2f. Exiting measurement.\n'],...
        varargin{end}, p0, p_actual));
  end
end
```

Listing 1: An assertion guarding against generating an unintended power level

The MG3710A signal generator can produce a repeatable phase offset between its two channels by sharing an internal local oscillator between the two channels. This ensures that the baseband signals are reliably created with a repeatable and constant offset, but the signal must then be amplified and attenuated internally to acheive the target output power. The generator uses a mechanical step attenuator as part of its power control path. When the step attenuator changes ranges it changes the physical length of the signal path which results in the phase offset between channels changing [79].

The measurement code already had the ability to configure the output attenuator to hold at a specific attenuation value. From this fixed point the output power could be varied by ± 10 dB without affecting the output phase offset. Three enhancements were made; checking that any power sweep covered ≤ 20 dB of range, automatic

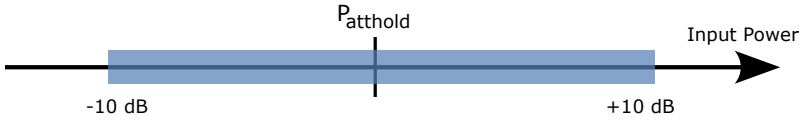

Figure 5.6: Valid input power range with Attenuator Hold active

calculation of the Attenuator Hold value based on the center of the range, and optionally, that the same Attenuator Hold value was used for all power sweeps falling within a 20 dB window. This third enhancement was necessary as the phase offset varies based on the attenuator hold value and not all measurements were done using the same power sweep ranges. By having the code preferentially use certain attenuator ranges, the phase was made repeatable whenever similar power levels were measured.

The signal generator has the internal capability to create a phase offset between the two channels. This capability builds upon the consistent initial phase offset which the previous modifications provide. A modification was made to use this programmatic phase shifting rather than pre-calculating and loading waveform files as it provides greater flexibility and reduces the initialization time of the system.

The original software had been limited to running nested parameter sweeps across frequency, power, and phase. While it was possible to generate datasets covering a large range of operating conditions, most of them are not useful and increase the measurement duration. The software was modified to allow specifying a consistent offset between the Main and Auxiliary input powers, simulating an unequal power splitter at the input. This was expanded to sweep a range of offset values at each Main input power point, allowing a time efficient exploration of

which splitter ratio was ideal for each power level. For measuring the low power behavior of the Main amplifier it is useful to sweep more than 20 dB of input powers so the Attenuator Hold feature was programmed to be automatically enabled only when the second channel is used.

Data Analysis

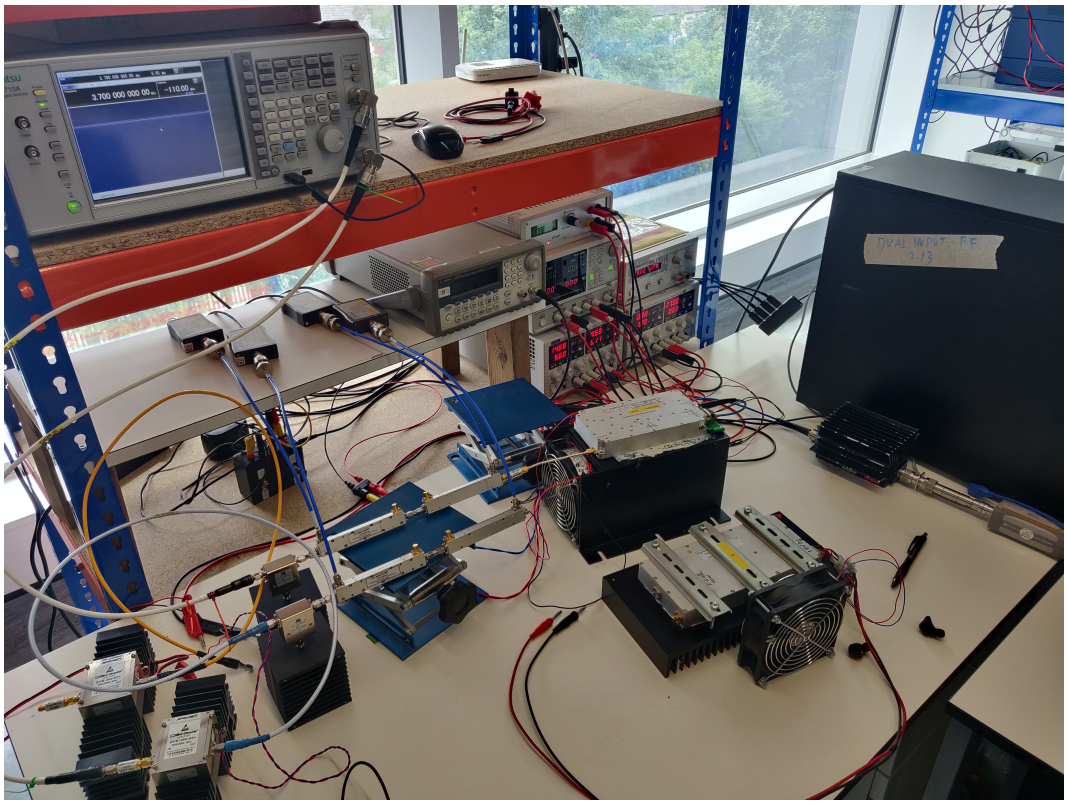

Figure 5.7: Measurement Setup for Driver Calibration

Another very important introduction to the controlling system has been a script to pre-characterize the drivers' response and create a look-up-table so the actual input power at the DUT can be set instead of the generator power. As the measurement system has the ability to measure actual input and output power, the driver

amplifiers can be inserted as the DUT and measured. When the code is put into driver calibration mode it directly uses the power sweep ranges as the raw values for the signal generator powers, and stores the measured gain values in a calibration table. These driver amp specific calibration files are stored and then recalled during normal measurements to allow accurate mapping of desired input power levels to signal generator settings. Having these files also allowed the code to be changed to reliably report to the user when signal levels beyond the calibrated range were requested, avoiding multiple occasions where long measurements would have contained data with systemic errors.

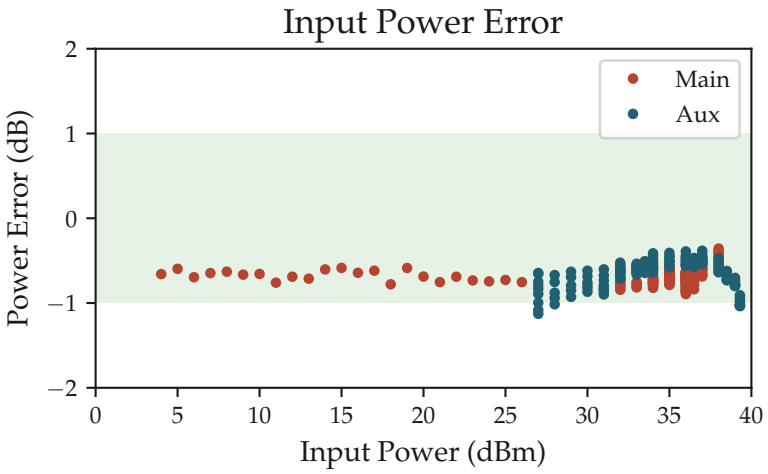

Figure 5.8: Measurement System Power Accuracy Check

As can be seen in Figure 5.8, the measured forward power at the Main and Auxiliary inputs are invariably slightly lower than the target power level by an average of -0.68 dB for the Main and -0.66 dB for the Auxiliary. It was decided to leave this input power error in-place as the true values will be available during

analysis and it was less risky for the input power level to be slightly lower than the target rather than unexpectedly higher than the target level.

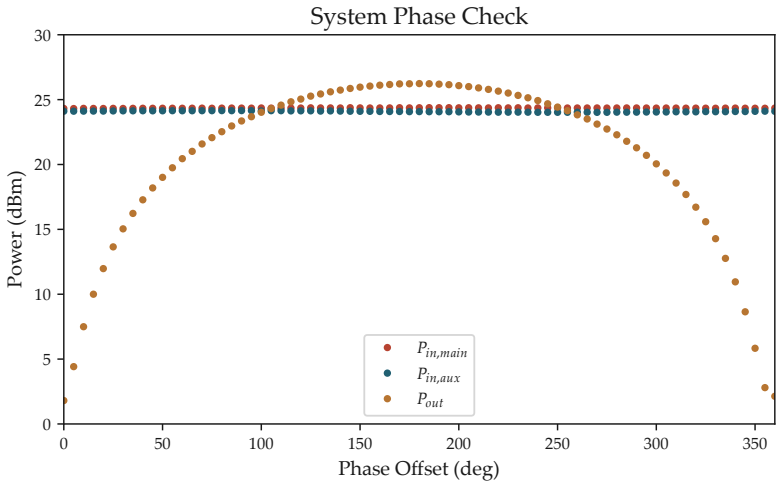

Figure 5.9: Measurement System Phase Check

In Figure 5.9, a hybrid coupler was inserted as the DUT with a 50 Ω power attenuator added to the second output port. A clean pattern of constructive and destructive combining can be seen. The plot shows two full phase sweeps performed with a full restart of the control computer and program between measurements, showing that the phase offset is highly repeatable between measurements. The test was done with identical low power driver amplifiers between the signal generator and the DUT inputs. The inability to measure the relative phases of the stimulus signals was initially considered not to be a problem after this verification as it showed that the phases were repeatable and the fixed offset could be found by using the hybrid coupler.

Figure 5.10 shows all 170 individual measurement points contained in the 19 sets of measurements used for this analysis. Measurements 1 to 28 examine the

behavior of the amplifier when only the Main is driven and the auxiliary has no input stimulus. The input source power was being increased in 1 dB steps. Measurements 24 and 25 showed an unexpected pause output power increasing, with measurements 26-28 matching expectations, so 24 and 25 were removed from the analysis as outliers. Measurements 29-170 examine the amplifier's behavior in the Doherty operating region. One point, 75, was removed as it spuriously showed a significant and non-repeatable increase in output power. The three removed measurements are marked with an 'x'. The remaining analysis in this chapter is based on the remaining 167 measurement points.

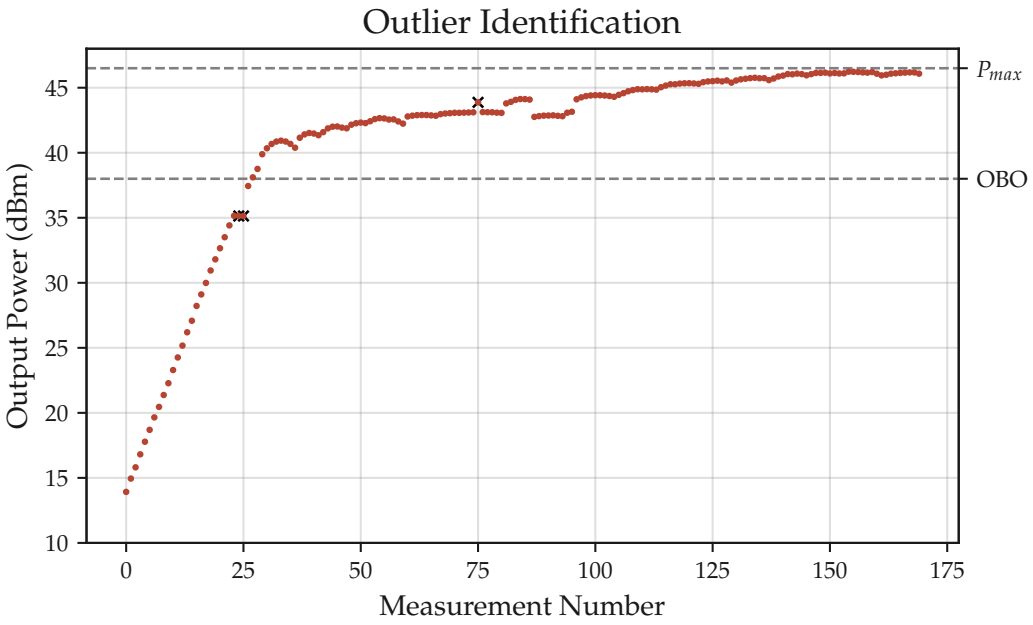

Figure 5.10: Input Power Outliers

5.3 DUAL-INPUT DOHERTY RESULTS

The initial measurement was a power sweep with only the Main channel active, between 5 dBm input power and 34 dBm. From there, the Auxiliary channel was enabled and a series of smaller measurements were done sweeping phase and incrementally increasing the Auxiliary and Main input powers to achieve target gain and efficiency values at various output power levels and sweeping the relative phasing of the input signals. Figure 5.11 shows the total available input power versus output power. The colors of the markers indicate groups of measurements where the input powers were kept fixed and the relative phase swept. The details of this approach and results will be shown in the following sections. This figure indicates that overall the measurements cover the targeted output power range.

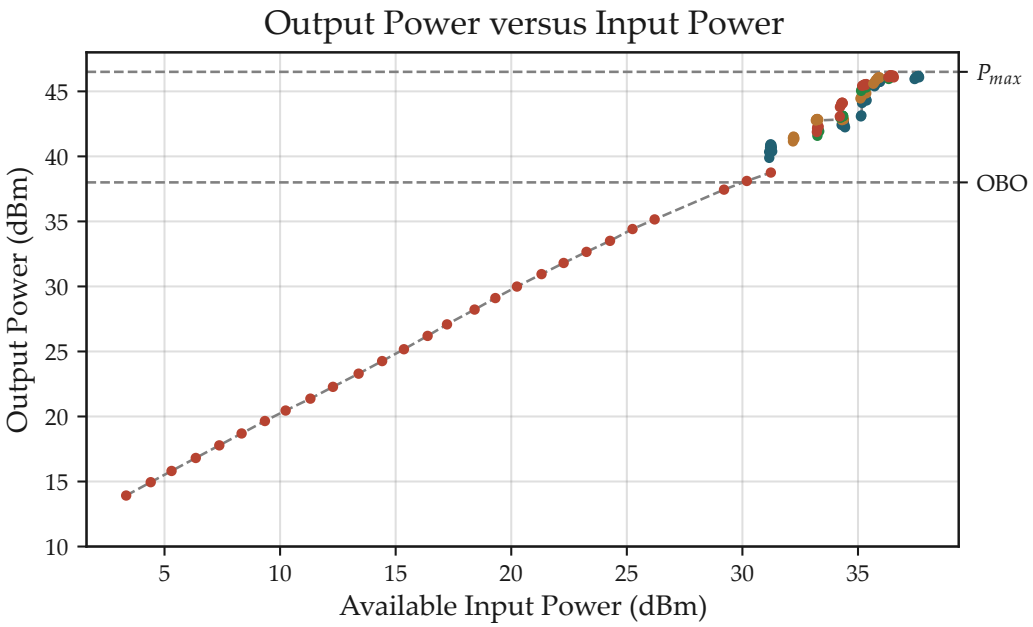

Figure 5.11: Total Input Power versus Output Power covering low power, Doherty region, and saturation

Figure 5.11 shows the measurement coverage of the output power. We can see that the gain remains linear all the way to P_{max}. There is a region around the OBO output power where the Main amplifier begins saturating and the addition of power from the Auxiliary would have likely improved gain linearity and provided a more complete dataset to draw conclusions from.

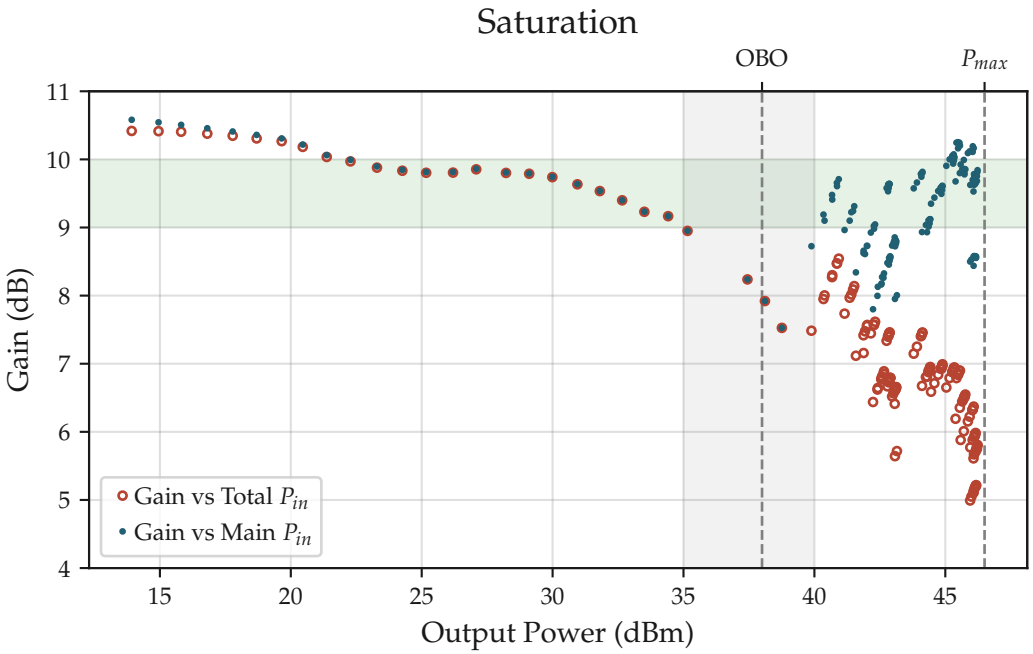

Figure 5.12: Gain relative to Main and Total Input Power

Figure 5.12 shows the amplifier's gain performance from two perspectives. First is the usual Power Gain where the output is referenced to the total input power. Second is Power Gain where only power to the Main input is considered, with Auxiliary input power being treated as a control signal.

$$\begin{aligned} \text{Gain} &= P_{\text{out}} - (P_{\text{in,main}} + P_{\text{in,aux}}) \\ \text{Gain}_{\text{main}} &= P_{\text{out}} - P_{\text{in,main}} \end{aligned} \tag{5.1}$$

From low power to the OBO breakpoint the Auxiliary amplifier has no input power so the calculated gain is equal for both cases. Above 40 dBm output power we can see the effect of the Auxiliary amplifier in boosting the output power. The behavior and control of the Auxiliary input power level and phase offset is explored

in the rest of the chapter. In Figure 5.12 it can be seen that the gain relative to the Main input signal can be restored in the load modulation region between the OBO breakpoint and $P_{\max}$ point such that the gain remains between 9 and 10 dB.

The overall system performance is summarized in Figures 5.13 to 5.16 show the effects of sweeping phase and the offset of input power levels between Main and Auxiliary. From the collected data a set of operating points where gain and efficiency are well balanced were manually selected and are shown as larger circles on each plot.

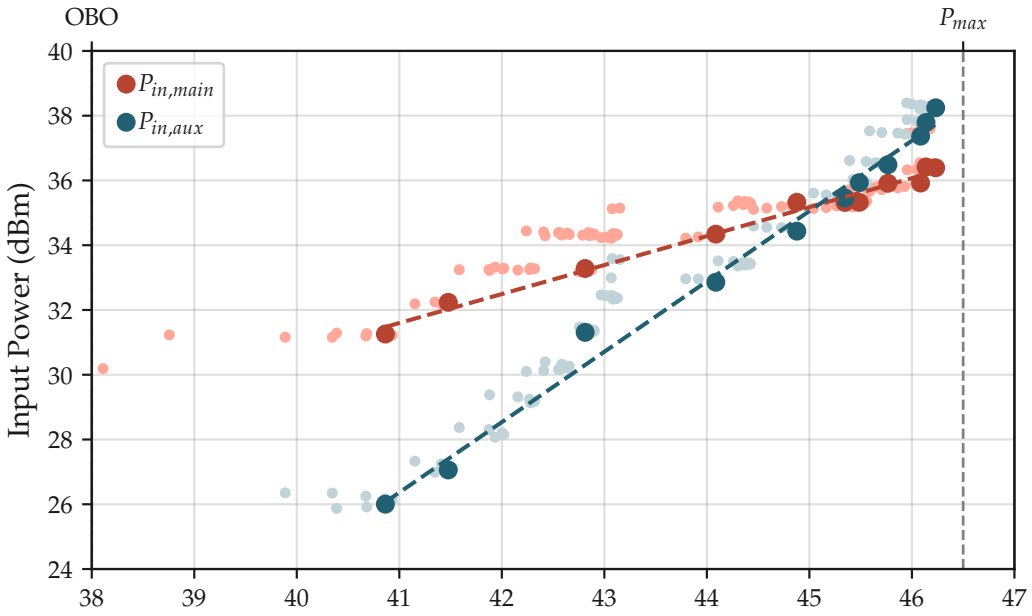

Figure 5.13: Input power at each port required for a given output power. Chosen operating points indicated by emphasized markers.

Figure 5.13 shows clear a linear trend (in decibel power) of the ideal power offset between Main and Auxiliary.

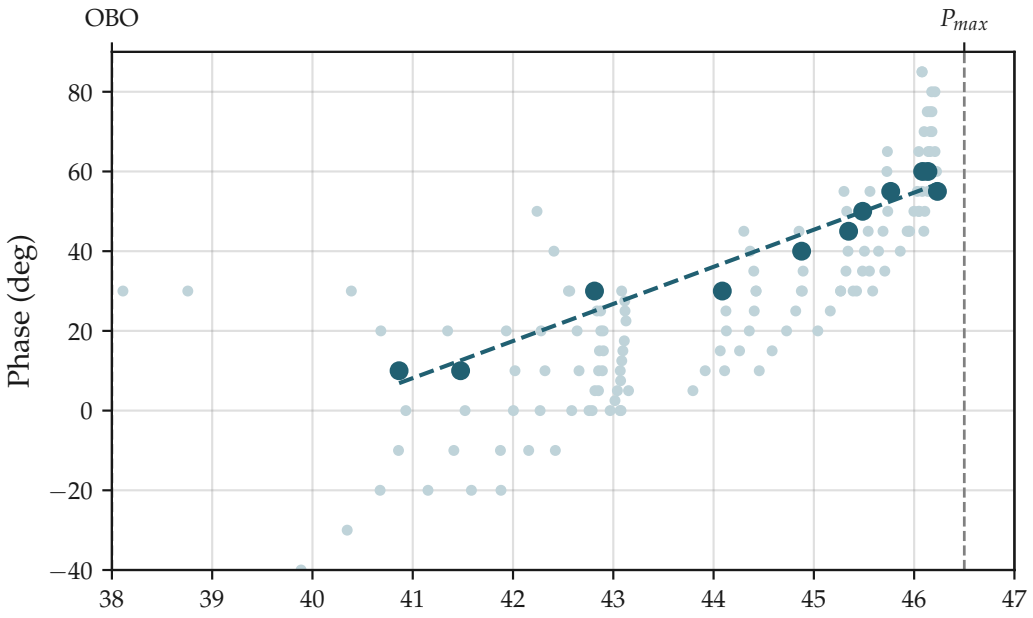

Figure 5.14: Effect of input phase offsets on output power. Chosen operating points indicated by emphasized markers.

In Figure 5.14 the selected operating points also show a linear shift in phase offset as achieved output power increases. The plotted trendline excludes the saturated power operating point as the heavy compression has introduced excessive AM-PM effects which are unsurprising and non-representative of the mid to high power operating behavior.

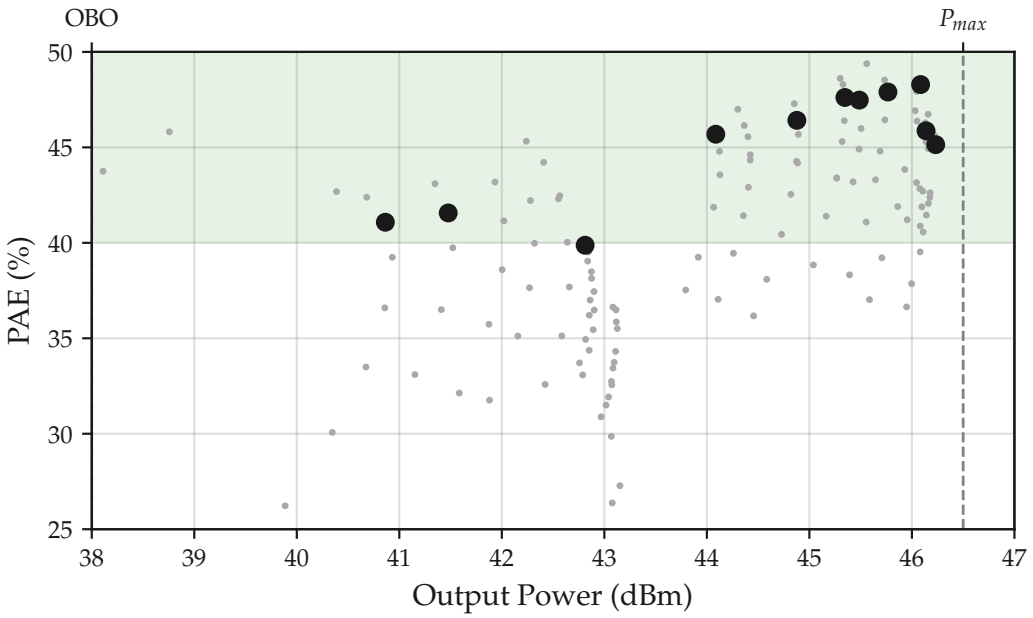

Figure 5.15: Achievable PAE values versus Output Power. Selected operating points indicated by emphasized markers.

Figure 5.15 shows how strongly efficiency varies as phase is swept. Each sweep forms an arc which includes a maximum output power and a decrease in power at both higher and lower phase offsets. The measurements were done with an emphasis on output power as there was significant concern that driving the amplifier into a state where the Auxiliary's current contribution was substantially out of phase with the Main's would not only decrease output power, but alter the desired load modulation in such a way that the devices could be damaged. As a result the optimal efficiency points were not captured for most power levels. However, for most sweeps the peak efficiency is above 40 % and show that efficiency improvements are slowing between the final measurement points so the dataset comes close to capturing the optimal efficiency points.

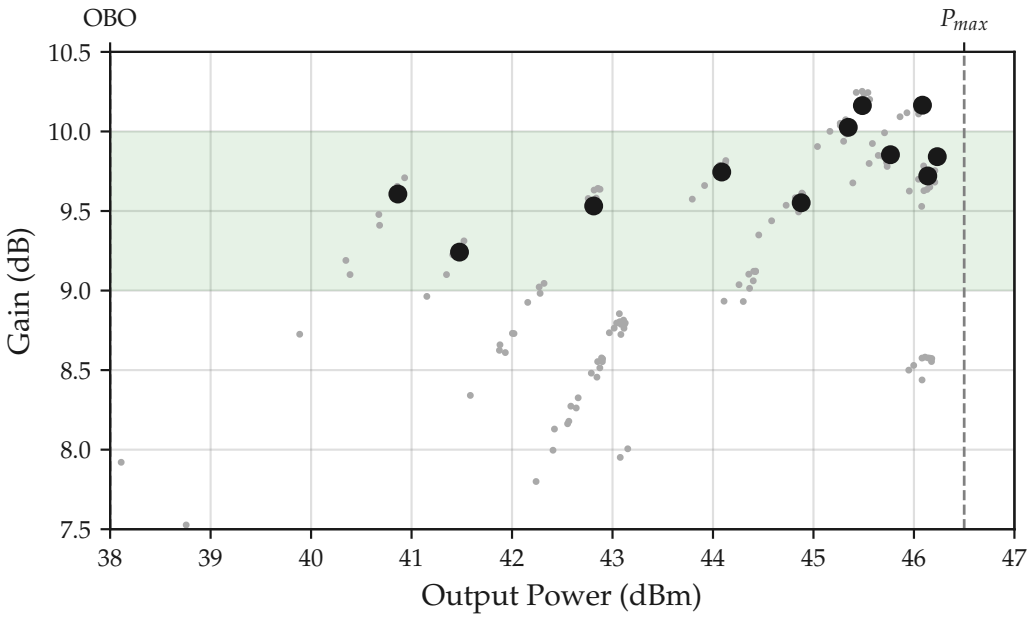

Figure 5.16: Gain relative to input power at the Main

Figure 5.12 has already shown that there were possible operating states where gain was level and remained in the target region around 9.5 dB. Figure 5.16 shows this same data zoomed to the Doherty region and with the selected operating states highlighted.

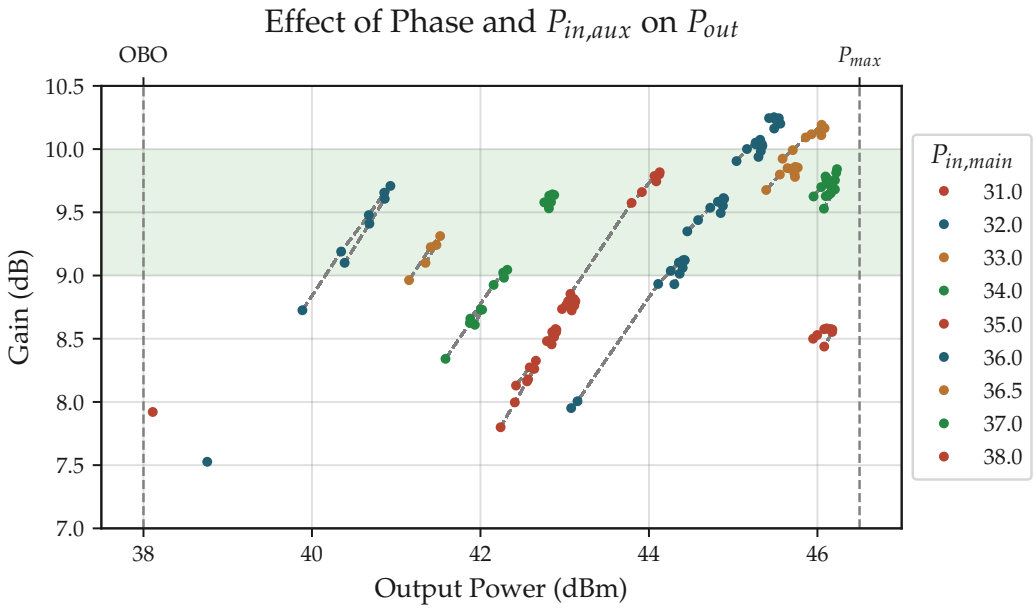

Figure 5.17: Effect of phase and input power offsets on gain

Looking more closely at the effective gain between the OBO and saturation points, several effects can be observed. Figure 5.17 shows multiple sweeps performed by fixing the Main and Auxiliary input powers and varying the phase around the maximum output power point. Each connected set of points represents one phase sweep. The Auxiliary input power is increased in steps until the amplifier gain relative to the input power at the Main rises to be within the target region of 9-10 dB. The colors of the points represent the $P_{\text{in,main}}$ and the effect of the increasing auxiliary power can clearly be seen, particularly in the red and blue sets of clusters between 42 and 45 dBm output power. The points connected by lines show efficiency as PAE. The larger green dots show the Drain Efficiency for the selected operating points.

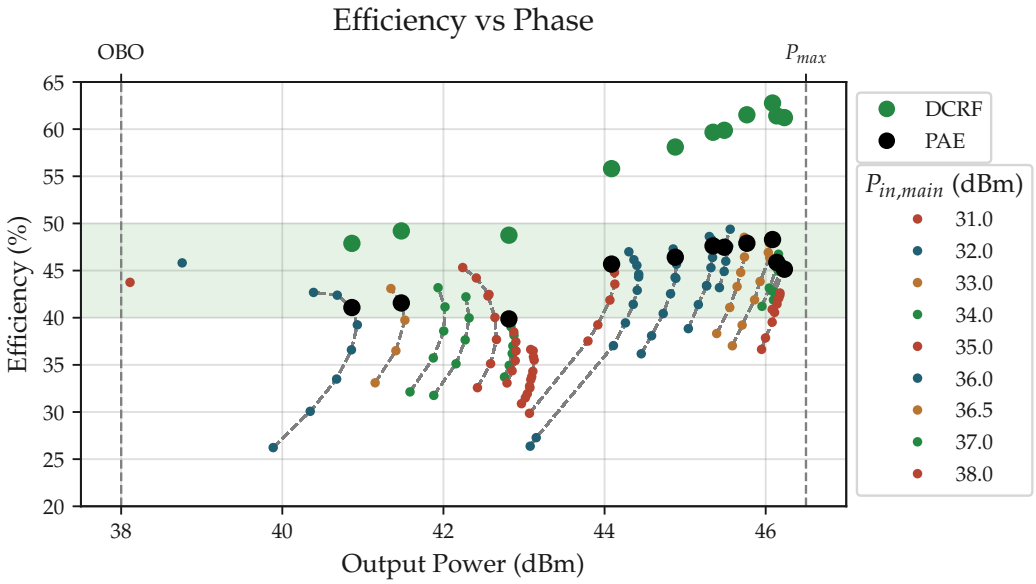

Figure 5.18: Effect of phase and input power offsets on Efficiency. Connected points show PAE for phase sweeps at a given $P_{\text{in,main}}$, $P_{\text{in,aux}}$. Emphasized markers show the PAE and DCRF for chosen operating points.

An alternative view of the same data focusing on PAE, shown by Figure 5.18, shows that the efficiency varies strongly with phase as indicated by the near vertical paths of the measurement arcs. Most phase sweeps have a change in output power of less than 1 dB but have a drop in efficiency of 10 % or more.

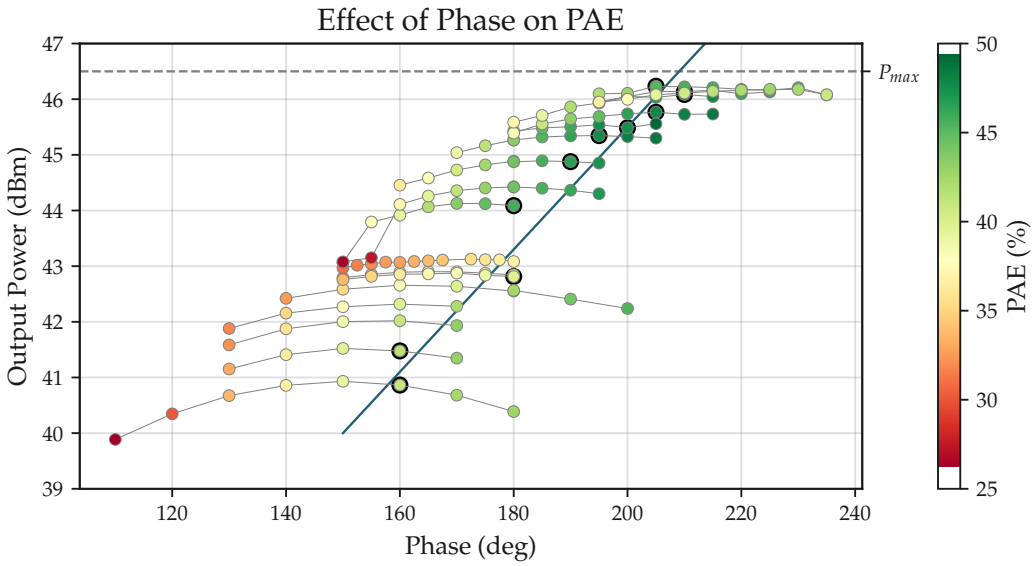

Figure 5.19: The optimal phase offset shifts as power increases. Selected operating points marked by a black outline.

Figure 5.19 shows the effect of phase on output power more directly with the PAE indicated by the marker colors. A clear trend can be seen with the maximum PAE located at the highest phase offset, farthest right, of each sweep. The sweep ranges were set to center on the maximum output power as linear gain was weighted most highly in the performance metrics.

The three preceding plots show the measurement coverage of the operating parameter space. The trendline on Figure 5.19 shows that the peak output power is shifting by 11 degrees of phase offset per dB of output power.

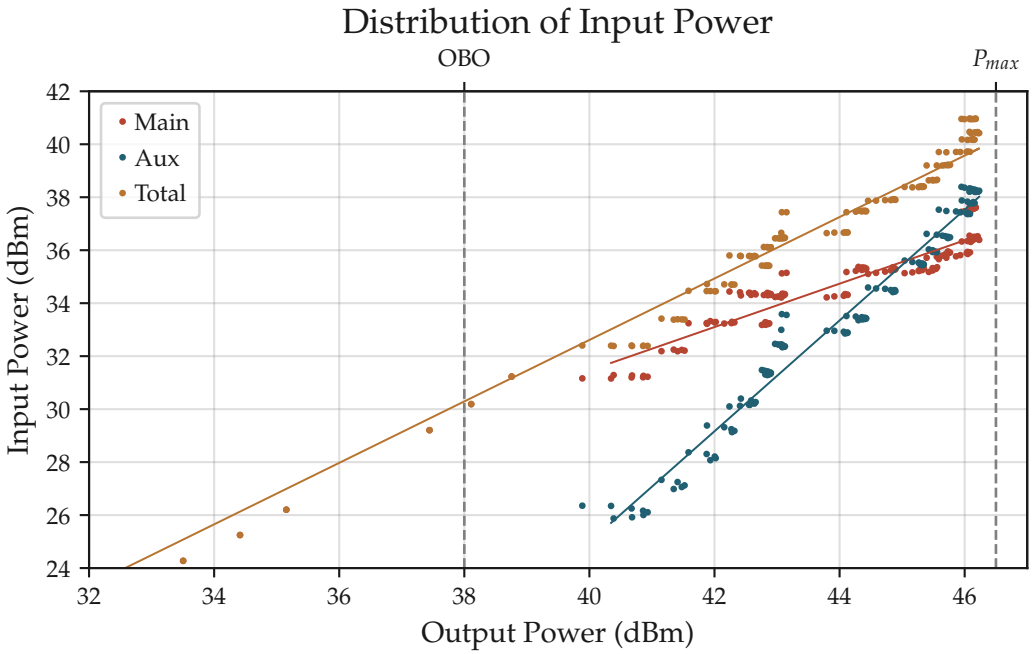

Figure 5.20: Measurements and trends for input power levels versus output power

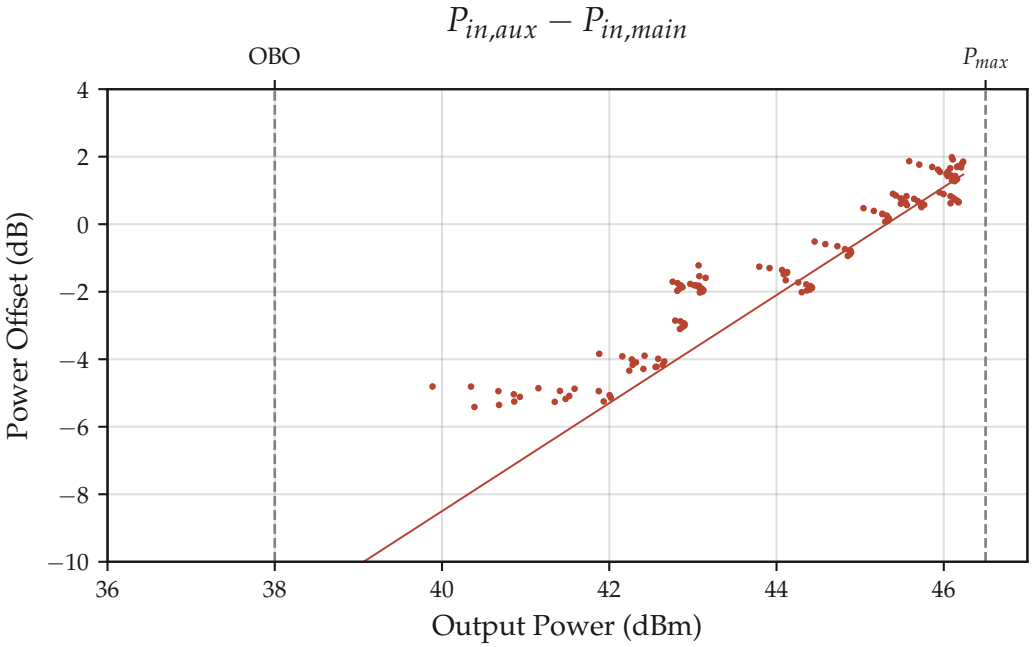

Figure 5.21: Offset between Main and Auxiliary Input Power versus Output Power

Figure 5.20 shows the contributions of Main and Auxiliary input power over output power. A clear trend in 5.20 (b) shows the Auxiliary input power starts at a −6 dB offset from the Main and rises to approximately +1.5 dB before the amplifier saturates. The slope of the offset is +1.6 dB/dB and is -11.7 dB at the breakpoint. Unfortunately, the measured points do not include the region just around the breakpoint.

5.4 SINGLE INPUT DOHERTY

The Single Input Doherty was fabricated at the same time as the Dual Input design and differs only in the addition of an unequal Wilkinson Splitter and a phasing section of microstrip at the input.

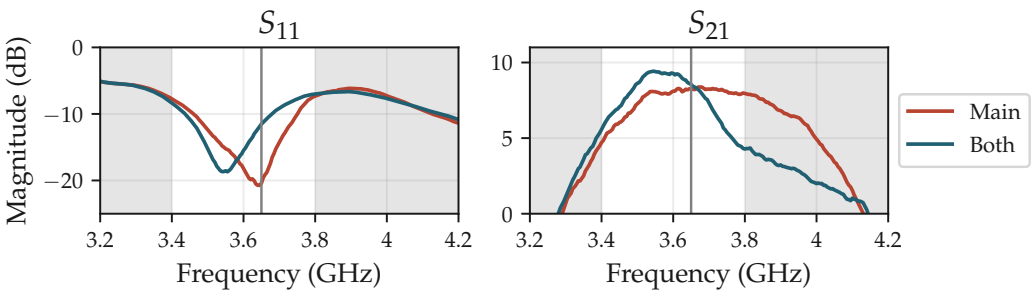

Figure 5.22: Single Input Measurements

The small signal behavior was measured in two states: the Main biased to 100 mA I_{ds} and Auxiliary pinched off, and both the Main and Auxiliary biased to 100 mA. The input match is fairly well centered in the band of interest though becomes marginal at the edges. Compared to the match of the Main and Auxiliary seen

in Figure 5.4, the input loss is slightly higher, as expected due to the addition of the splitter and additional line length. The match shifts down in frequency by ~100 MHz when the Auxiliary is biased into conduction, representative of the match in the load modulation region of operation.

With only the Main operating, the small signal gain is flat at ~8 dB from 3.5 to 3.9 GHz with a 3 dB bandwidth of 600 MHz centered on 3.7 GHz. When the Auxiliary is conducting the 3 dB bandwidth narrows to ~200 MHz centered on 3.55 GHz with a flat peak of 9.5 dB gain.

5.4.1 *Modulated Measurement*

Having extensively measured the dual input amplifier behavior and confirmed that the single input amplifier was active with small signal S-Parameter measurements, the next set of measurements focused on characterizing the performance with a modulated signal and examining the linearizability of the design.

The amplifier was brought to the Compound Semiconductor Applications Innovation Centre to make use of the measurement system [80]. The system is comprised of an SMW200A Vector Signal Generator and a FSW Signal & Spectrum Analyzer, both manufactured by Rohde & Schwarz, as shown in Figure 5.23. The FSW is capable of controlling the signal generator to perform coordinated operations including standard linearity measurements such as Adjacent Channel Leakage Ratio (ACLR) and EVM.

An EMPower 1131-BBM5K8CGM driver amplifier was used to produce the target input power. This model has a rated P_{1dB} of 40 dBm and a P_{sat} of 45.4 dBm. The small signal gain is 58 dB in the 3.4 to 3.8 GHz band and the gain at P_{sat} is 10 dB compressed, around 48 dB. The expected peak input power level required is 40 dBm, seen in 5.20, however with a modulated measurement the peak power will only be experienced for very short pulses which is expected to minimize the impact of the compression.

Figure 5.23: Modulated Measurement System

A 20 MHz wide OFDM 5G NR waveform with 8.5 dB PAPR was created in the signal generator. An initial test with the driver amplifier and power attenuator was performed to check the system performance. It was observed that the driver was capable of delivering at least 40 dBm at the target frequency, and that the

Direct Digital Pre-Distortion capability of the measurement system could improve it's ACLR to <-50 dBc which was considered more than sufficient to make its contribution to the measurement insignificant.

Table 5.1 lists the average output power and efficiency of each measurement point.

FREQUENCY GHZ	V_{GS} BIAS	I_D MA	P_{AVG} DBM	DCRF %
3.45	−4.0	400	35.5	31.7
3.50	−4.5	453	36.6	36.0
3.50	−5.0	373	36.0	38.1
3.50	−5.5	384	36.5	41.5
3.65	−5.5	429	35.9	32.4
3.65	−6.5	411	36.5	38.8

Table 5.1: Modulated Performance Data

The Dual Input Doherty amplifier was installed into the system and an initial measurement at 3.50 GHz with a $V_{gs,main}$ of -2.72 V ($I_{ds,main}$) and $V_{gs,aux}$ of -4.5 V was taken. The measured performance showed a low average output power, 36.6 dBm, and low efficiency of 36.0 %. Examining the AM–AM behavior of the amplifier showed that the Auxiliary was turning on too early, below the target P_{avg}.

The $V_{gs,aux}$ bias was then tested at two additional levels, -5.0 and -5.5 V, to shift the operating point further into class C and delay the turn on. This increased the efficiency to 38.1 % and 41.5 % respectively and the average power level remained at 36.5 dBm.

The Dual Input Doherty design showed a significant variation in performance given small changes in the phase offset between Main and Auxiliary amplifier input signals. As the true phase offset of the fabricated single input design is not known and the designed power levels were not being reached, the next step was to investigate the behavior at frequencies above and below 3.5 GHz.

At 3.65 GHz the performance was 35.9 dBm and 32.4 % efficient at -5.5 $V_{\text{gs,aux}}$, and 36.5 dBm and 38.8% efficient at -6.5 V. At the deeper bias point additional input power was required to reach the 36.5 dBm $P_{\text{out,avg}}$ level compared to at 3.5 GHz.

At 3.45 GHz and -4 V the performance was lower in both output power and efficiency, 35.5 dBm and 31.7 %. The gain was heavily compressed and using additional input power to try reaching the target output power risked damaging the amplifier.

FREQUENCY GHZ	V_{gs} BIAS	I_d MA	P_{avg} DBM	DCRF
3.50	−5.5	420	37.0	42.6
3.65	−6.0	420	36.5	38.0

Table 5.2: Performance with extended Main Input line

3.5 GHz gave the best performance overall for a given input power level, but neither the output power or efficiency met the design expectations. The PCB had been provisioned with a disconnected length of 50 Ω microstrip which could be used to lengthen the path to the Main transistor by ∼1.5 mm. Given the miniaturized nature of the design, that equates to increasing the nominal 90° phase offset from Main to Auxiliary by 30°. This is a large shift, relative to the nominal,

but fabrication tolerances and microstrip trace clearance requirements made it challenging to design a smaller shift. The existing trace was cut and the additional length soldered in.

At 3.65 GHz and -6 $V_{vg,aux}$ the performance stayed similar to before, 36.5 dBm and 38.0 %. At 3.5 GHz and -5.5 $V_{gs,aux}$ the performance improved to 37.0 dBm and 42.6 %. While small, this indicates that the phasing at 3.5 GHz was improved by increasing the relative length of the Main compared to the Auxiliary. The PCB layout did not have a straightforward way of further increasing the physical phase delay so an alternative was needed.

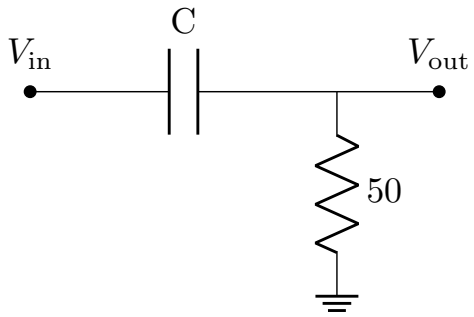

Figure 5.24: Capacitive Phase Shifter Circuit

Between the input splitter and each amplifier is a 100 pF DC blocking capacitor. As the matching networks have an input impedance of 50 Ω, these series capacitors can be analyzed using the equivalent circuit in Figure 5.24. Figure 5.25 shows the phase shift and power loss of a 3.5 GHz signal for capacitor values between 0.1 pF and 200 pF as calculated using Equation 5.2. For capacitance values of 100 pF or greater the signal experiences effectively no loss and a phase shift of less than

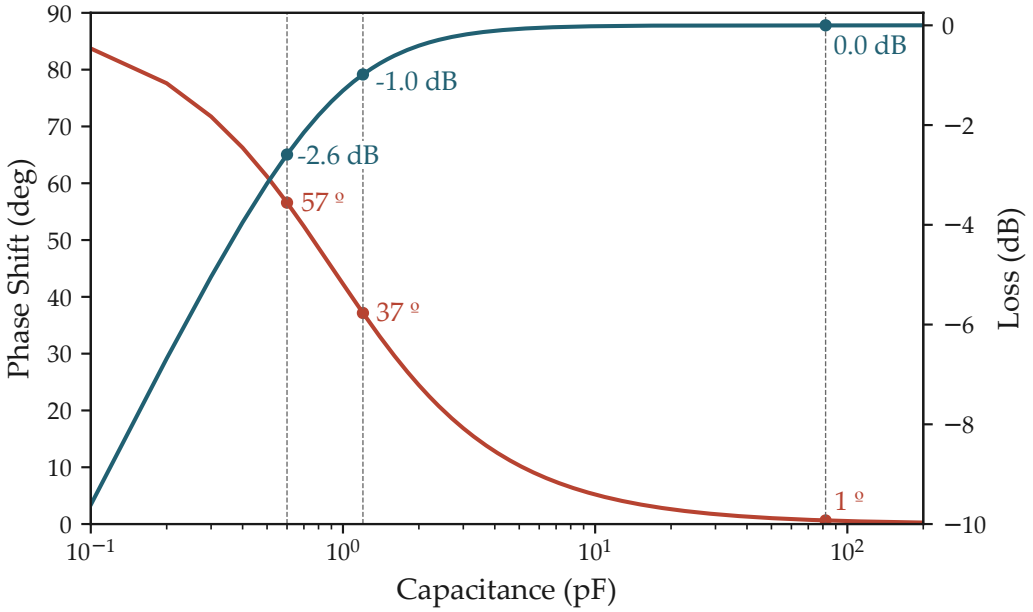

Figure 5.25: Capacitive Phase Shifter Performance

1 degree. The phase shift across the capacitor is such that the phase at node V_{out} leads node V_{in}, giving a negative phase shift.

$$\begin{aligned} \frac{V_{out}}{V_{in}} &= \frac{R}{R - \frac{j}{\omega C}} = \frac{1}{1 - \frac{j}{\omega CR}} \\ \angle\theta &= \tan^{-1}\left(\frac{1}{\omega CR}\right) = \tan^{-1}\left(\frac{X_c}{R}\right) \end{aligned} \tag{5.2}$$

Changing the DC blocking capacitor for the Auxiliary to 1.2 pF changed the phasing by 37° and reduced the drive to by 1 dB. The amplifier was remeasured at 3.5 GHz and -5.5 $V_{\text{gs,aux}}$ and the output power rose to 37.5 dBm and 45.6 % efficiency. In an effort to reach the design goal of 38 dBm P_{avg} the Auxiliary bias

was raised to -5V. This resulted in exactly reaching the 38.0 dBm goal with a small 1.9 percentage point reduction in efficiency to 43.7 %.

Two additional measurements were made to bracket the frequency as the large change in phase offset could have moved the optimal performance point. At 3.4 GHz it was possible to reach the 38.0 dBm power at a lower efficiency of 42.5 %. At 3.65 GHz the power and efficiency were nearly the same, though both lower than at 3.5 GHz.

FREQUENCY GHZ	V_{gs} BIAS	I_d MA	P_{avg} DBM	DCRF
3.40	−5.0	530	38.0	42.5
3.50	−5.0	516	**38.0**	43.7
3.50	−5.5	440	37.5	**45.6**
3.65	−5.5	515	37.9	42.8

Table 5.3: Performance data with 1.2 pF capacitor

Reaching the 38.0 dBm P_{avg} power level was a major milestone in the measurement process but the measured efficiency had not yet reached the value found in simulation. Given the 1 dB loss in the Auxiliary path some decrease in efficiency was expected but an additional phasing point was considered useful to test while the amplifier was in the measurement system. A 0.6 pF capacitor changes the phasing by an additional 20° but also adds 2.6 dB of total loss.

The series capacitor was changed from 1.2 pF to 0.6 pF and the amplifier retested. The approach at each new measurement condition was to begin at a low power state and progressively increase the drive strength until the output power was

compressing significantly, between 1 and 3 dB depending on the achieved output power and efficiency. Immediately upon powering the amplifier and supplying an RF signal it was noted that the efficiency had fallen significantly and compression began at a lower output power than in previous measurements. The measurement was stopped with an output power less than 35 dBm and with greater than 4 dB of compression, indicating that the change in phasing and additional loss was severely impacting performance. However, when the drive power was reduced below the turn-off point of the Auxiliary it was noted that the gain on the Main amplifier had fallen as well.

The isolation resistor of the input Wilkinson splitter was expected to prevent the mismatch of the Auxiliary changes from affecting the Main amplifier on the input side. On the output side a change in Auxiliary performance significantly alters the load modulation of the Main while also affecting the Auxiliary's own loading. Seeing a change in backoff led to concerns that the transistors themselves may have been degraded by the operating condition. This was checked by reverting to the 1.2 pF series capacitor which had produced the best amplifier performance. It was found that the amplifier was severely degraded both in output power and efficiency. A check of the passive components showed no evidence of damage. Replacing the transistors was considered infeasible as they are bare-die and local facilities were unavailable to rework them. Returning the amplifiers to the third-party organization which did the original mounting work would not be possible in the time remaining for the project. Additionally the existing design has been analyzed in both dual

and single input configurations, across a variety of frequencies, and with CW and modulated waveforms. Areas of improvement have been identified which would require alterations to the PCB and re-fabricating the amplifier. Time and funding limitations prevent this from being done during this work.

The modulated measurement system supports direct Digital Pre-Distortion (DPD) of the input waveform to offset the amplitude and phase non-idealities of the amplifier's transfer function. This makes use of the link between the vector signal analyzer and signal generator to drive the amplifier with a known stimulus signal and observe the output signal which has been modified both by ideal linear amplification and non-linear effects on both amplitude and phase. The system then modifies the input signal with the inverse of the observed error effects and re-measures the amplifier. Iteratively, this approach can derive an accurate model of the amplifier's behavior and cause the output waveform to be nearly ideal.

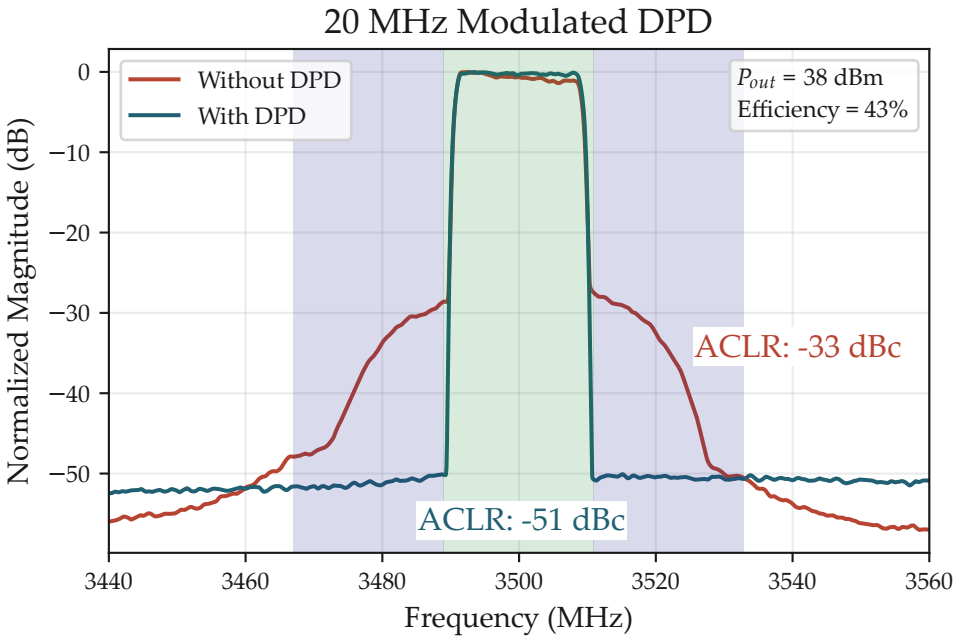

Figure 5.26: Single Input DPD Results

Figure 5.26 shows the output spectrum of the amplifier with 1.2 pF modification and a $V_{gs,aux}$ of −5.0 V. The amplifier's baseline performance has an ACLR of -33 dBc. The DPD corrected performance reduced the ACLR by 18 dBc to -51 dBc which meets the requirements and expectations of a 5G basestation amplifier.

5.5 COMPARISON

In this chapter the Doherty Design Template's efficacy was confirmed by CW and modulated measurements of a fabricated power amplifier. The simulated measurements closely match the final measurements. The final point of useful

comparison is with other published designs. Examining Table 5.5 shows that the fabricated design is highly competitive against similar amplifiers.

Measurement	*Unit*	*This*	[81]	[82]	[76]	[83]	[84]
Frequency Range	GHz	3.4-3.8	1.5-3.8	3.3-4.3	3-3.6	3.4-3.5	3.4-3.8
Center Frequency	GHz	3.6	2.65	3.8	3.3	3.45	3.6
Bandwidth	GHz	0.4	2.3	1	0.6	0.1	0.4
Fractional BW	%	11	87	26	18	2.9	11
OBO	dB	8.5	6	6	6	9	8
P_{sat}	dBm	46.25	43.4	44.5	44	49.5	38.5
DE_{OBO}	%	48	55	52	56	40	50
DE_{sat}	%	62.5	55	68.9	66	42.5	68
Gain	dB	10	13.8	11.1	11	8.5	28

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6

CONCLUSION

6.1 SUMMARY OF WORK

The Doherty architecture is as relevant as ever to provide highly efficient linear amplification over the powers, frequencies, and PAPRs needed by modern and future wireless communications systems. The work in this thesis aggregated the existing core theories of Doherty operation and synthesized them with leading non-linear circuit simulation and waveform engineering theories to create a design template with extensive analytics on internal circuit state.

The limitations of ideal theory were restated and key metrics defined. As Doherty and PA theory are well understood and extensively discussed, this thesis focuses on the use of increasingly powerful simulation tools in bridging theory and reality. The abilities of non-linear transistor models and circuit simulators to accurately determine and provide realistic behaviors was examined and demonstrated.

A demonstrator amplifier was designed, fabricated, and measured showing the efficacy of this approach. The amplifier achieved performance on-par with similar designs published in literature, with the addition of being physically compact.

A measurement system was modified and enhanced to provide insight into the behaviors of Main and Auxiliary amplifiers with a particular emphasis on the limitations of a static input splitter and the opportunities for dual input Doherty designs with digital control.

6.2 FUTURE WORK

6.2.1 *Hardware Demonstrations*

The design template could be further validated by designing additional amplifiers with different transistors, substrates, and performance specifications (frequency, power, bandwidth). Designing a MMIC would demonstrate additional simulation and system integration techniques. Working with packaged transistors where the models do not expose an intrinsic node would allow de-embedding approaches to be integrated with the template.

6.2.2 *In-system Measurements*

The design template strongly demonstrates the value of access to the voltage and current waveforms in-circuit. Ongoing research in the Cardiff University Centre for High Frequency Engineering is leading to the ability to make non-invasive current measurements at any point in the circuit including near the intrinsic plane [85].

6.2.3 *Algorithmic Optimization*

The CW measurements of the fabricated dual input RF PA demonstrator showed significant efficiency improvements and the ability to flatten the amplifier's gain behavior near saturation by controlling the input to the auxiliary amplifier. The measurement system could be extended to adaptively sweep the operating space to determine the best parameters and produce a better fit model. The measurement system could also be used to directly measure and compare models of different complexity such as linear power/phase lines, LUT based, and polynomial fit.

6.2.4 *Modulated Measurement System*

The dual input measurement system has the ability to use IQ baseband files. Only single tone CW stimulus was used in this thesis with phase shifts applied to the auxiliary channel. A modulated signal could be pre-calculated with true sub-sample time delays incorporated to allow nuanced analysis of Doherty behavior. Additionally further metrics such as Error Vector Magnitude for specific communications standards could be integrated to provide a more comprehensive analysis.

6.2.5 *Active Control System*

The step-wise dual input measurement system has been demonstrated to produce results, allowing for the determination of amplitude and phase functions to control the auxiliary input waveform and produce desirable performance improvements in the overall amplifier. These transfer functions could be built into a multi-channel streaming radio system to produce a complete digital Doherty system. Integrated current sensing and output signal observation could allow for the development and testing of real-time control systems which adaptively optimize system performance.

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"Perhaps the ending has not yet been written."

— Atrus

COLOPHON

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