Thermal Performance of 940 nm AlGaAs-Based VCSELs Grown on Germanium

J. Baker, C. P. Allford, S. Gillgrass, J. I. Davies, S. Shutts, and P. M. Smowton

Abstract—VCSEL thermal resistances are determined from power-current-voltage-wavelength measurements performed on nominally identical epitaxial structures grown on Ge and GaAs substrates. We show that the effective thermal conductivity of the VCSEL is increased when grown on Ge substrates.

Keywords—VCSEL, GaAs, Ge, thermal resistance

I. INTRODUCTION

The production of 800-1000 nm vertical-cavity surfaceemitting lasers (VCSELs) is a well-established industry built upon decades of advancements in epitaxy and fabrication in the GaAs-AlGaAs material system. However, in today's environmental and geopolitical context, question marks over GaAs have arisen relating to supply chain vulnerability and ecological impact. For these reasons, germanium, with its broader production, non-toxicity, and potential for recycling, presents itself as a viable alternative growth substrate in the future for the optoelectronics industry. In recent years, germanium has been described as an ideal drop-in replacement for gallium arsenide as the growth substrate of choice for high-volume production of AlGaAs-based VCSELs [1]. A driving motivation for using Ge is the lattice match with AlAs (and high Al-composition AlGaAs) which eliminates the strain-induced wafer bow suffered with growth on GaAs substrates. Other advantages include higher thermal conductivity, higher electron and hole mobility, higher fracture toughness, defect-free (zero EPD) crystal quality, and the potential to grow on thinner substrates. Subsequently, we have highlighted the benefits of growth on Ge for improving on-wafer uniformity of device performance resulting from a reduced oxidation variation [2], we have shown comparable performance of VCSELs grown on 200 mm (8-inch) Ge and

GaAs substrates [3], and investigated VCSELs grown on 450 and 225 µm thick Ge substrates [4]. Other research groups have focussed on the assessment of crystal quality and the transition layers between the Ge substrate and AlGaAs epitaxial structure [5], [6], leading to the successful production of 940 nm VCSELs [7], demonstration of 25 Gb/s NRZ transmission at elevated temperature [8], and the monolithic integration of AlGaAs DBRs on Si substrates via a Ge aspect ratio trapping layer [9]. Recently, a SWIR VCSEL emitting at 1380 nm was demonstrated using AlGaAs DBRs grown on Ge substrates and wafer-bonded to an AlGaInAs active region grown on InP [10]. It has also been alluded to in the literature, but not yet shown, that the thermal performance of Ge-substrate VCSELs should be improved due to the higher thermal conductivity of bulk Ge and we presented our initial findings relating to this at the 2024 IEEE International Semiconductor Laser Conference [11]. In this paper, we expand upon those results to robustly assess the thermal performance of Ge-substrate VCSELs against their GaAs counterparts through on-wafer electro-optical testing.

II. MATERIALS & METHODS

A. Epitaxial Structure & Device Fabrication

The epitaxial wafers used for this study are generic structures designed and grown by IQE plc for emission at 940 nm. This consists of a MQW active region in a λ -thick cavity, sandwiched between an upper p-doped AlGaAs DBR and lower n-doped AlAs-AlGaAs DBR. The inclusion of AlAs in the bottom DBR is used to improve heat dissipation due to improved thermal conductivity of binary AlAs [12]. A high Al composition layer is positioned in the top DBR which, after selective thermal oxidation, provides electrical and optical confinement. Nominally identical structures, within acceptable tolerances, are grown on n-type GaAs and n-type Ge substrates by MOVPE. For structures on Ge, a proprietary MOVPE-grown transition layer, developed by IQE, is included to ensure a smooth transition from Ge to AlGaAs. The devices characterised for this work are Quick VCSEL (QuickSEL) structures, the fabrication process of which is described in [13].

B. Experimental Method

To assess and compare the VCSEL thermal performance, the thermal resistance, R_{Th} , is measured for a range of oxide apertures for devices grown on both Ge and GaAs substrates. We employ the measurement technique described in [14] for the determination of R_{Th} , which we outline here. The thermal resistance can be defined as in equation (1) by the temperature change for a given heat flux:

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$$R_{Th} = \Delta T / \Delta P_{diss}, \tag{1}$$

where P_{diss} is the power dissipation:

$$P_{diss} = IV - P_{optical}.$$
 (2)

Here, *IV* is the total electrical power equal to the product of the bias current, *I*, and operating voltage, *V*, and $P_{optical}$ is the total optical power emitted from the VCSEL. The quantity ΔT in equation (1) is not directly measurable for a VCSEL, however, the shift of the emission wavelength can be used to indirectly measure the device internal temperature, due to the known refractive-index shift, as described in [15] and [16]. The resulting shift with temperature (in nm/°C) can be used to calibrate the wavelength shift with dissipated power (in nm/mW), the ratio of which gives the thermal resistance (in °C/mW), as in equation (3):

$$R_{Th} = \Delta T / \Delta P_{diss} = (\Delta \lambda / \Delta P_{diss}) / (\Delta \lambda / \Delta T).$$
(3)

By measuring thermal resistance for a range of oxide apertures, the equation

$$R_{Th} = 1/(2\xi D_a) \tag{4}$$

can be fit to the experimental data. This approximates the VCSEL as a disk heat source on a thick substrate, where ξ represents the thermal conductivity of the material separating the heat source from the heat sink, and D_a is the active region diameter [17]. In our case, ξ represents the thermal conductivity of the bottom DBR + substrate (including the transition layers for the Ge substrate devices). Hence, we use the measured thermal resistance to determine values of ξ for the Ge and GaAs substrate structures. The effect of interface resistances throughout the structure and between the substrate and heatsink are also included in the value of ξ . Often, the active region diameter is given by the oxide aperture diameter, which we measure via infrared microscopy in-situ during the thermal oxidation process. We find that our experimental data diverges from the model with this assumption, therefore, we include a correction to the oxide aperture diameter to allow for non-ideality, such that equation (4) becomes:

$$R_{Th} = 1/[2\xi(D_{ox} + b)].$$
 (5)

where D_{ox} is the oxide aperture diameter and *b* is a constant. We did not observe any differences in the oxidation behaviour (e.g. overall oxidation rate, crystallographic axis preference) between the Ge and GaAs substrate wafers.

III. RESULTS & DISCUSSION

Firstly, to verify that the epitaxial structures are equivalent, the electro-optical characteristics of devices ranging 30 to 49 μ m in mesa diameter are compared. This produces oxide aperture diameters ranging ~ 1 to 19 μ m. Onwafer testing was performed for Ge and GaAs substrate structures at the centre of a 150 mm (6-inch) wafer. Understanding the electrical performance of the devices is critical for determining the thermal resistance due to the impact on the calculated power dissipation values. This was assessed from current-voltage characteristics for a range of oxide apertures. The series resistance was found to be comparable for both Ge and GaAs structures, shown in Fig. 1. Circular transfer length method (CTLM) measurements were

carried out to assess the p-contact resistance for each sample. Specific contact resistances were found to be on the order of $10^{-7} \Omega \text{cm}^2$. Additionally, sheet resistances were extracted as 58 and 64 Ω_{\Box} for the Ge and GaAs wafer, respectively. This is representative of the conductivity of the uppermost layers of the top DBR but provides some indication of the doping concentrations throughout the epi-structure.

The threshold current, I_{th} , and current density, J_{th} , is compared for Ge and GaAs devices in Fig. 2. The GaAs substrate devices have a slightly higher threshold requirement, but values are comparable. Threshold currents are within a few hundred μ A for all devices tested and current densities are higher by ~ 0.2 kA/cm² for large aperture GaAs devices. This variation is within the tolerance of wafer-to-wafer and run-to-tun drift. There are some potential drivers of this which would have differing impacts on the thermal performance which we will consider, e.g., alignment of the gain peak and cavity mode wavelengths, overlap of the optical mode with the carrier density profile, mirror reflectivities, and absorption/scattering loss.



Fig. 1: Differential resistance between 2.2 and 2.4 V of \sim 2 to 18 μm oxide aperture diameter GaAs and Ge substrate devices.



Fig. 2: Threshold current and threshold current density of ~ 2 to 18 μm oxide aperture diameter GaAs and Ge substrate devices.



Fig. 3: Raw spectra at 25 °C from 0.5 to 6.5 mA for an \sim 3 µm VCSEL (top) and corresponding fundamental mode wavelengths versus current for the same device (bottom).

We observe the minima in J_{th} as a function of temperature to occur at approximately 50°C at the centres of all GaAs and Ge wafers measured, indicating that the detuning of the gain peak and cavity mode are equivalent. We do find that the emission wavelengths are 3-4 nm longer for the Ge wafers, which suggests a thicker inner cavity layer. If consistent throughout the layers, this would indicate that the Ge epi-stack is $\sim 0.5\%$ thicker than the GaAs, which would work to increase thermal resistance. However, this wavelength shift could also be indicative of a slight reduction in the Al composition in the cavity. It should be stated, then, that the low index layers in the bottom DBR pairs are composed of AlGaAs and AlAs. Therefore, if we assume that a reduction in Al composition is present throughout the stack, the thermal conductivity of the bottom DBR would decrease for the Ge wafer (due to a reduction in the Al composition in the high-index layers [12]). Furthermore, it may be that the threshold gain is higher for the Ge VSCELs which could be related to a reduced optical loss and/or increased reflectivity from the DBRs. The dominant contribution to internal optical loss is free carrier absorption in the p-doped layers in the top DBR of the structure, and, further, any effect of reflectivity on device performance is also originating in the top DBR, given that the bottom DBR (+ substrate) is close to 100% reflective. Therefore, these contributions to a difference in threshold requirement are

expected to have a negligible impact on the subsequent analysis. A difference in the overlap of the optical mode with the carrier density profile (transverse confinement factor) is more difficult to determine. However, from in-situ IRmicroscopy, we observe no distinct differences in the shape of the oxide apertures between the GaAs and Ge samples, hence we can assume that the mode shape and carrier density profiles are comparable. The VCSEL emission wavelength is extracted from spectral measurements at a range of pump currents (up to a maximum of 10 mA). Raw spectra are shown in Fig. 3 for a 3 µm aperture diameter device. The corresponding dissipated power at each current was determined from the power-current-voltage characteristics with $\Delta \lambda / \Delta P_{diss}$ then given by the slope of the curves. A plot showing the wavelength shift with dissipated power for ~ 8 um oxide aperture devices is shown in Fig. 4.



Fig. 4: VCSEL emission wavelength as a function of dissipated power at 25 $^{\circ}\mathrm{C}$ for an 8.2 and 8.6 $\mu\mathrm{m}$ GaAs and Ge VCSEL, respectively.



Fig. 5: VCSEL emission wavelength at zero dissipated power as a function of heatsink temperature for an 8.2 and 8.6 µm GaAs and Ge VCSEL, respectively.

This procedure is performed at increasing heatsink temperatures, from which we determine the temperature coefficient of the emission wavelength from the intercept of the curves, that is, the emission wavelength at zero dissipated power. This is done to exclude Joule heating (as detailed in [14]). The temperature dependence of the extracted wavelengths at zero dissipated power are shown in Fig. 5 for the same devices as Fig. 4. For both the GaAs and Ge substrate devices, $\Delta\lambda/\Delta T$ is 0.070 ± 0.001 nm/°C, with the error given by the numerical fit. This is in agreement with the expected shift given by the temperature coefficient of the refractive index of the stack [18]. Additionally, this approach also allows us to probe the temperature dependence of the thermal resistance. In our case, we find the increase in R_{Th} with temperature to be constant for both GaAs and Ge samples (with a temperature coefficient of ~ 0.006 (°C/mW)/°C) for the devices of Fig. 4 and 5), so we only consider and present data at 25°C in the subsequent discussion.

The resulting plot of thermal resistance as a function of oxide aperture is shown in Fig. 6 for both GaAs and Ge devices. From the fit of equation (5), we extract thermal conductivities of $\xi_{GaAs} = 0.3090 \pm 0.0003$ W/cm°C and $\xi_{Ge} = 0.3787 \pm 0.0011$ W/cm°C. The uncertainties are given by the standard error of the numerical fit. The correction to the active diameter, b, which was included as a term in the numerical fit and is given by 1.7 \pm 0.2 and 1.53 \pm 0.04 μ m for Ge and GaAs, respectively. The extracted thermal conductivity values are both reduced compared to the literature values of the thermal conductivity of bulk Ge (0.55 W/cm°C) and GaAs (0.44 W/cm°C) [19], which is expected given the presence of AlGaAs in the bottom DBR, as well as interface contributions, and potentially non-ideal thermal contact with the heat sink. We find the thermal conductivity of the Ge substrate VCSELs to be ~ 18% lower than that of GaAs, which is on the order of the difference of the bulk values. Therefore, we show that the higher thermal conductivity of Ge can indeed be leveraged to improve the thermal performance of AlGaAs-based VCSELs.



Fig. 6: Thermal resistance as a function of oxide aperture diameter for GaAs and Ge substrate VCSELs.

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