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PROPAGATION DELAY MATCHED CMOS 0.18 μm FREQUENCY DOUBLER FOR L-BAND APPLICATION

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ABSTRACT: *In this article, propagation delay matched CMOS frequency doubler for L-band application is proposed. Schmitt trigger and voltage controlled delay line compensates duty cycle error and propagation delay mismatching that are induced as the frequency of operation is increased. As a consequence, unwanted harmonic components suppression is greatly improved for higher frequency of operation. CMOS frequency doubler is designed at the input fundamental frequency (f_0) of 1.15 GHz and fabricated with TSMC 0.18 μm CMOS process. Measured output power at the doubled frequency ($2f_0$) is 2.67 dBm for the input power of 0 dBm. The amount of harmonic suppression for f_0, $3f_0$, and $4f_0$ are 43.65, 38.65, and 35.59 dB, respectively.*

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Key words: *frequency doubler; Schmitt trigger; voltage controlled delay line*

1. INTRODUCTION

Frequency multiplier is a good candidate for high frequency signal generation circuit due to the generic phase noise (PN) characteristic difference between frequency multiplier and generator. The stability of phase locked loop (PLL) with VCO is degraded as the operating frequency increases. Alternatively, high frequency signal can be obtained by multiplying the low frequency signal that has relatively high stability and low PN. Therefore, several studies have been done on the design of frequency multiplier circuit [1–6].

For example, a design technique using the *n*th harmonic component of a transistor is most widely used [2, 3]. Because of the periodic harmonic response of a transistor, the desired frequency components at integer multiple frequencies of the input fundamental signal can be obtained. By proper biasing and input/output matching network, we can obtain the desired output component with maximum amplitude. However, additional harmonic termination circuits or band pass filters are required since the amount of undesirable harmonics, including the fundamental, are considerable due to its low bias condition.

Time-delay technique, as shown in Figure 1, is another way of frequency multiplication and which is most likely used in the digital circuit design [4–6]. However, the operating frequency is fairly limited due to the uneven duty cycle and time-delay mismatching induced by the frequency limitation of the CMOS inverter.

In this article, we propose a group delay matched CMOS frequency doubler for L-band application to overcome those problems and increase the frequency of operation. Design theories and principles of operation of the proposed structure are presented with some simulation and experimental analysis in the following sections.

2. CIRCUIT DESIGN AND SIMULATION

At first, as shown in Figures 1 and 2, input continuous wave (CW) signal is converted into square wave through CMOS inverter (Inv) and Schmitt trigger (ST). An input square wave is delayed $T/4$ by the delay element, which consists of an integrator and comparator circuit, where T is the period of the input signal, and is fed into an XOR gate along with the intact input signal. Finally, we can obtain the output signal with half the input period T.

Figure 1 shows a block diagram of the conventional time-delay method frequency doubler. When we tried to increase the operating frequency of the conventional frequency doubler, we were confronted with two troublesome problems. First, we cannot obtain the square wave with 50% duty cycle from CW using a simple CMOS inverter structure at higher frequency. Because the rising

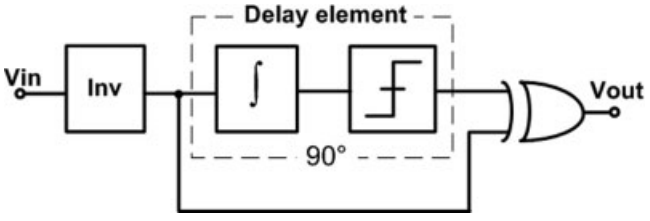

Figure 1 Conventional time-delay method frequency doubler

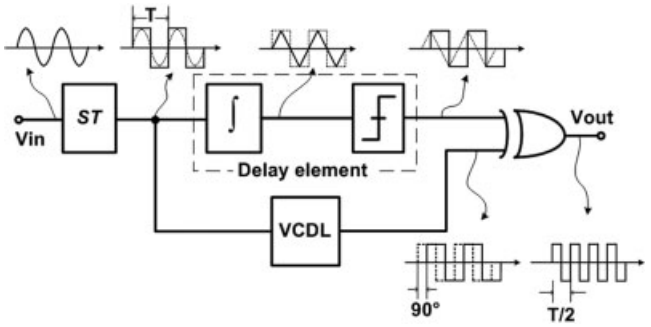

Figure 2 Proposed group delay time matched frequency doubler

and falling time are considerably large and different for one period at higher frequency, the logic performance of the XOR gate is fairly degraded. We define this phenomenon as an uneven duty cycle error. Second, even if we assume no duty cycle error, two inputs of the XOR gate may have a timing difference other than $T/4$ due to the propagation delay time of the delay element only at one side of a loop. This phenomenon is defined as a timing error, specifically propagation time mismatching. Timing error affects both the output power level of a desired multiplied signal and the unwanted harmonics suppression. Figure 2 is the block diagram of the proposed circuit. Schmitt trigger is adopted to give additional degree of freedom and compensate the duty cycle error of the CMOS inverter [7–9].

The output of the ST is split into the delay element path and the voltage controlled delay line (VCDL) path. The comparator in the delay element is implemented as a Schmitt trigger for the same purpose. VCDL compensate the propagation delay of the delay element to ensure the 90° phase difference at the input of an XOR gate. Finally, the XOR gate can generate the desired $2f_0$ with the exact 90° offset signals. When the amount of offset is deviated from 90°, output of the doubler circuit would have considerable amount of unwanted harmonics with lower $2f_0$ output power.

2.1. Schmitt Trigger (ST)

Circuit schematic of the ST adopted in the proposed structure is presented in Figure 3(a). The input and output voltages of a ST have hysteresis characteristics. That is, the output transitions from high to low when the input is higher than the higher threshold voltage, $V_{th,H}$, and the output goes to high when the input is lower than the lower threshold voltage, $V_{th,L}$. So the Schmitt trigger is a kind of a comparator with resistance to the noise of the amplitude between the two threshold voltages, $V_{th,H} - V_{th,L}$. Therefore, by adjusting the higher and lower threshold voltages through control voltage V_n, gate voltage of NMOS, and V_p, gate voltage of PMOS, independently, we can obtain the pure square wave with constant duty cycle. Figures 3(b) and 3(c) shows that the time of high to low transition can be delayed (increase in duty ratio) by increasing V_n, and low to high transition can be advanced (increase in duty ratio) by increasing V_p, and vice versa.

2.2. Voltage-Controlled Delay Line (VCDL)

Phase or propagation delay of a signal can be controlled by control voltage of the VCDL. Thus, the propagation delay mismatch between the reference input and the delayed signal can be optimized by VCDL [10]. The VCDL is a circuit that adjusts the propagation delay of input signal according to the charging/discharging time of the load capacitance of an inverter. The average propagation delay of the inverter is expressed as (1).

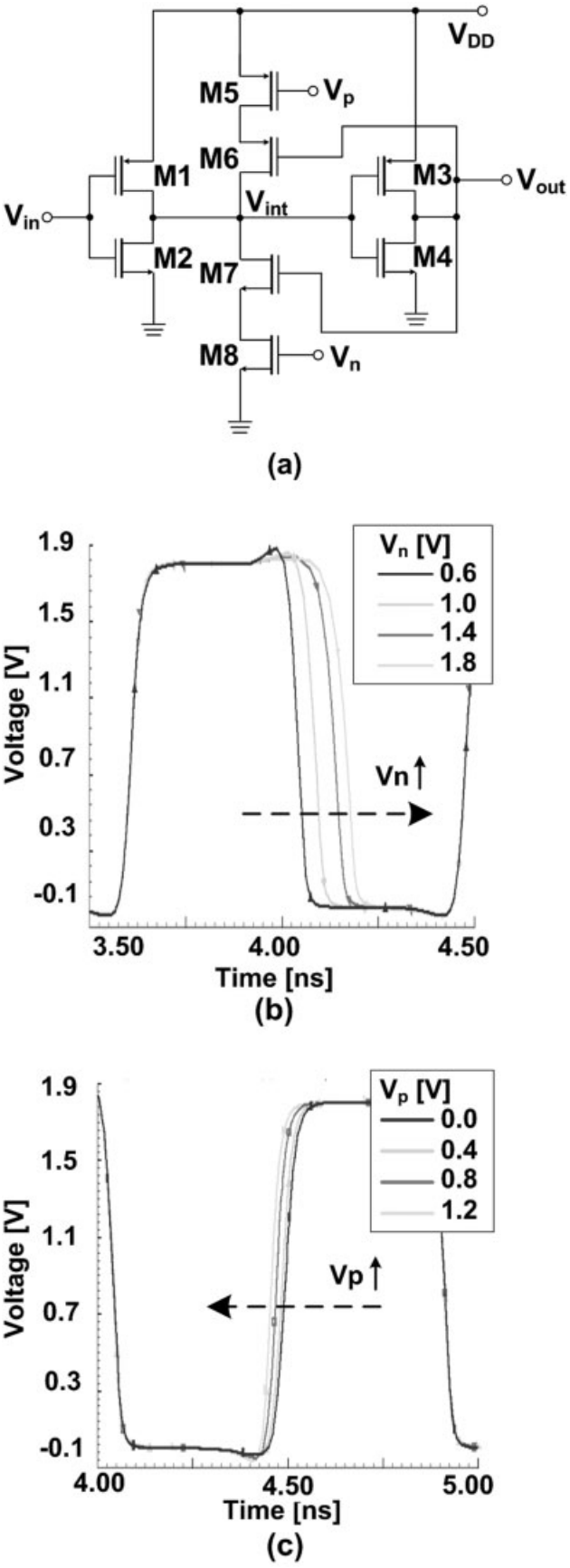

Figure 3 (a) Circuit schematic of Schmitt trigger, and hysterisis control of output waveform shaping for (b) V_n variation, and (c) V_p variation

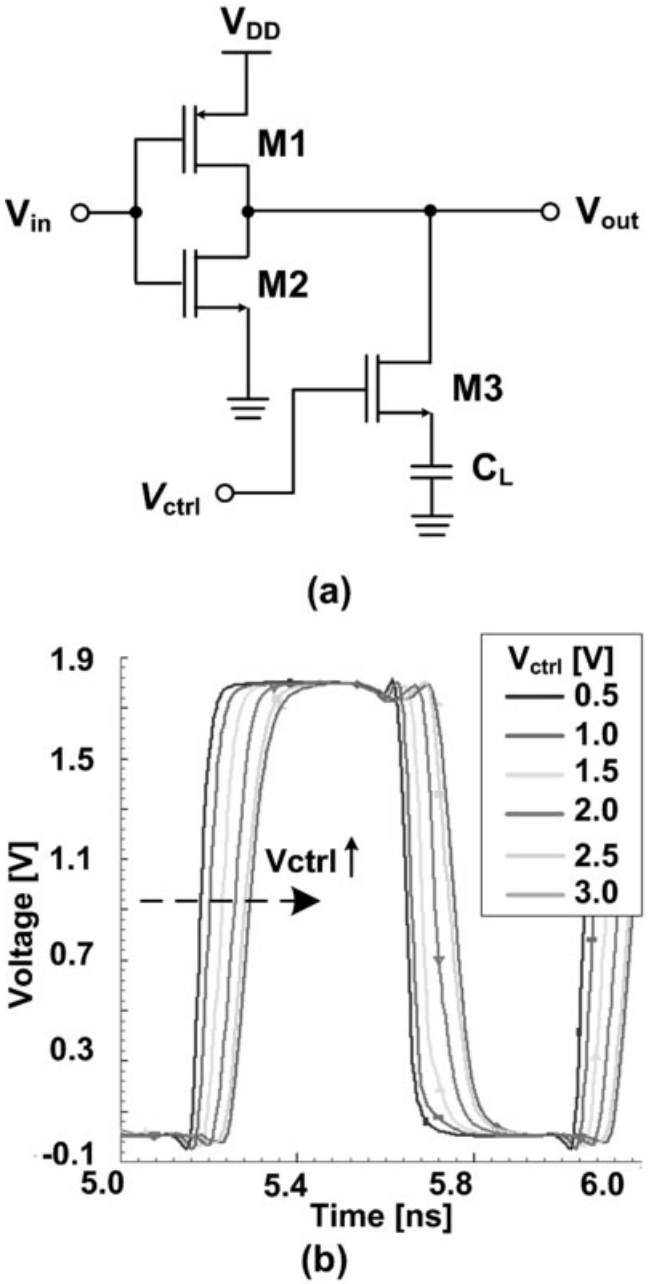

Figure 4 Voltage controlled delay line (a) unit cell, (b) 5-stage VCDL output waveform according to various control voltage (V_{ctrl})

$$t_d \approx \frac{2}{\mu C_{ox}(W/L)} \cdot \frac{C_L \cdot V_{DD}}{(V_{DD} - V_{th})^2} \quad (1)$$

where W and L is the width and length of the gate of an inverter, respectively.

Figure 4(a) is a schematic of the unit VCDL, and Figure 4(b) is a simulation result of 5-stage VCDL. The range of adjustable time is about 0.15 ns. Assuming f_0 of 1.15 GHz (one period $T = 0.87$ ns), this amount assures 17.2% adjustability for T. Available input frequency range of frequency doubling operation is 0.75–1.55 GHz for 0.15 ns propagation delay compensation, as presented in Figure 5. This graph shows just two periods of each waveform by truncating the data for clear presentation.

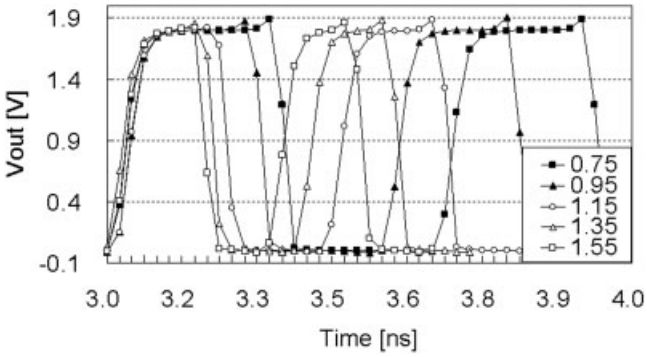

Figure 5 Output voltage waveforms according to various input frequency

3. EXPERIMENTAL RESULTS AND DISCUSSIONS

For the experimental verification of the proposed design, we have designed a frequency doubler that multiplies f_0 of 1.15 GHz to produce the output signal at 2.3 GHz. The proposed circuit is fabricated using CMOS TSMC 0.18 μm process. The core circuit layout area is $\sim 0.8 \times 0.5$ mm^2, and the total chip area is 1.1×0.7 mm^2 including bonding pads. The supply voltage (V_{DD}) is 1.8 V.

Figure 6 shows the measured output spectrum of the fabricated L-band frequency doubler. The measured output power at $2f_0$ is 2.67 dBm, when the input is fed with 0 dBm signal. The amount of harmonic suppression for f_0, $3f_0$, and $4f_0$ are 46.6, 38.65, and 35.59 dB, respectively. The measured PN characteristics of the output signal ($2f_0$) is -97.01 dBc/Hz (at 10 kHz offset) for -102.2 dBc/Hz of input signal (f_0). This is better than the theoretical PN degradation 10*log(2) = 6 dB, and the reason is thought to be the result of nearly perfect unwanted harmonic cancellation. Figure 7 shows the desired output power and unwanted harmonics.

Table 1 is the performance comparison of the proposed circuit with the conventional frequency doubler in [4]. The reference is selected based on the fact that it is the most recently published work on the frequency doubler using time delay technique, but without ST and VCDL. By introducing ST and VCDL, uneven duty cycle error and the time-delay mismatching of a conventional circuit can be overcome. Consequently, we achieved two times higher frequency of operation than the conventional circuit, showing excellent harmonic suppression performance. The amount of harmonic suppression improvement is 8.6–21.6 dB, and especially 4th harmonic suppression is improved as much as 21.6 dB.

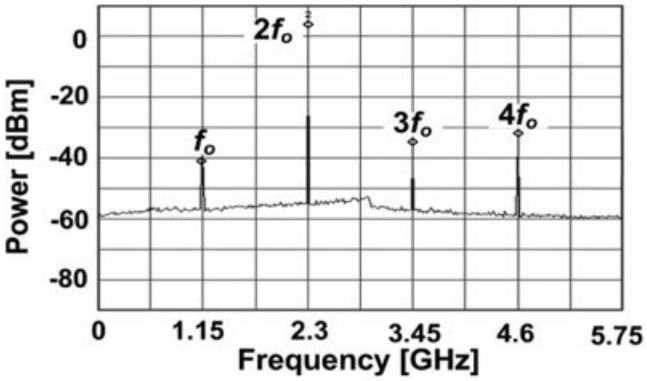

Figure 6 Output spectrum with 0 dBm input signal at 1.15 GHz

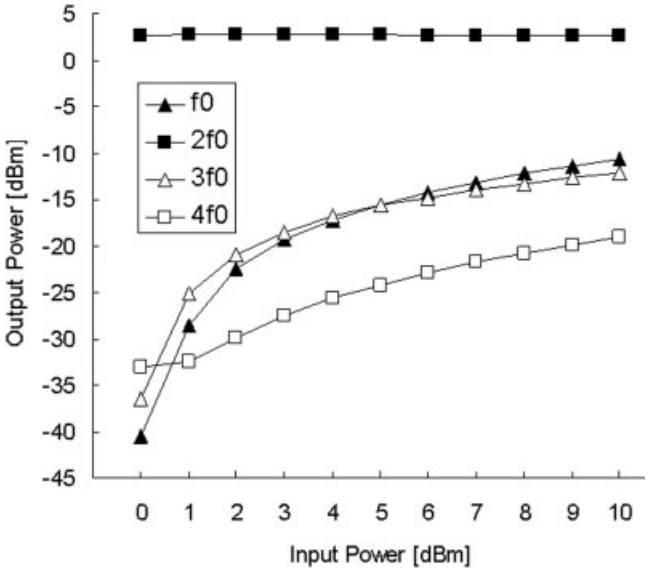

Figure 7 Desired output ($2f_0$) and unwanted harmonics for various input power

The total power consumption is 72 mW and this value is fairly higher than the previous work. This additional power consumption is attributable to the increased number of transistor by introducing ST and VCDL, being a cost for higher operating frequency and superior harmonic suppression. If we narrow down the range of input frequency or increase the frequency of operation, the required number of VCDL cells would be smaller, decreasing the total power consumption.

4. CONCLUSION

To achieve higher frequency generation and add additional degree of freedom, group delay time matched CMOS frequency doubler for L-band application is proposed. It is expected that the proposed frequency doubling topology would have a great contribution in increasing the operating frequency of various microwave and millimeter wave frequency multiplier circuit as a consequence of its wave shaping and delay mismatching compensation capability. We have a future work on the reduction of redundant power consumption, and the design of $2^{n\text{-th}}$ frequency multiplier.

ACKNOWLEDGMENTS

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TABLE 1 Performance Comparison

		[4]	This Work
f_0 [GHz]		0.6	1.15
2 f_0 [GHz]		1.2	2.3
P_{in} [dBm] at f_0		5	0
P_{out} [dBm] at f_0		4	2.67
V_{DD} [V]		1.8	1.8
Current [mA]		5	40
P_{diss} [mW]		9	72
Harmonic	f_0	30	46.6
Suppression	$3f_0$	30	38.6
Ratio [dB]	$4f_0$	14	35.6
Phase noise (at 100kHz offset)		−109	−109.7

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ENHANCED PATCH ANTENNA PERFORMANCES USING DENDRITIC STRUCTURE METAMATERIALS

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ABSTRACT: *The patch antenna with dendritic structure metamaterials is proposed and the performance of the antenna is investigated numerically and experimentally. Dendritic structure metamaterials can possess negative permeability due to the resonance of the magnetic polarizability within a band where the electromagnetic wave cannot propagate. The dendritic structure has the merit of fairly high-level of symmetry and can exhibit excellent isotropy. When the frequency of the antenna lies in the resonant bandgap, the performance of the antenna can be enhanced due to the fantastic electromagnetic characteristic of the dendritic structure. The study results show that compared with the conventional patch antenna without dendritic structure metamaterials, the half-power beamwidth (HPBW) of the proposed antenna becomes more convergent and the gain is higher.* © 2009 Wiley Periodicals, Inc.
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Key words: *dendritic structure; patch antenna; radiation patterns; gain*

1. INTRODUCTION

Patch antenna consists of a patch of metallization on a grounded substrate, which has the advantages of low-profile, lightweight, and leading to lots of applications. However, patch antenna also