# A Novel Approach for Wide Band High-Efficiency Power Amplifier Design

**A thesis submitted in partial fulfilment**
**of the requirement for the degree of Doctor of Philosophy**

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# Declaration

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**In the memory of my parents, Ali and Husa.**
**And for Haya, my beloved wife.**

# Abstract

Wireless communication systems require an efficient and broadband RF front-end. RF Power Amplifiers (PA) are the most critical component in the RF front-end and are considered the bottleneck in high efficient wideband transmitters. The research starts with an investigation of high efficient operation modes based on waveform engineering. The outcome of the research can be divided into two main parts: The first concerns an analysis of high efficient modes of operation. The second part builds on first part looking at the PA's efficiency-bandwidth perspective to design a wide band high efficient PA.

The first part of the thesis, introduces a novel linear high efficient PA mode termed Injection Power Amplifier (IPA) that exceeds drain efficiency of 90% without relying on the nonlinearity of a PA at the compression region. This is achieved by presenting appropriate negative harmonic impedances to a transistor to reduce the dissipated power, thus, increasing the efficiency of conversion of DC to fundamental RF power. The theoretical analysis of this mode is presented and a validation measurement has been carried out using an active load-pull system. The measured results confirmed the theoretical predictions of achieving high efficiency in a linear PA operation. Furthermore, a PA structure that is based on two parallel PAs (main PA and auxiliary PA) has been proposed along with the practical circuit realization of the IPA mode. In addition, a PA prototype has been designed following a methodology of nonlinear PA design based on waveform engineering. The PA prototype has been characterized and built operating at 0.9 GHz with an output power of 10 W showing a high linear efficient operation of 80% drain efficiency at only 1 dB compression level.

The second part of this work aims to tackle today's limitation of high efficient wideband PAs beyond octave bandwidth. A conceptual system based on multi-mode operation has been proposed to overcome the need for bandlimiting passive harmonic termination. This novel approach is based on combining passive termination with active harmonic injection to get around the theoretical limitation of one octave for high efficiency harmonically tuned power amplifiers. Furthermore, a proof of concept PA prototype has been designed and built for a two octave bandwidth (4:1 bandwidth) operating from 0.63-2.56 GHz and providing the rated output power of a 10 W GaN device with a PAE greater than 50% at only 1 dB compression point. This multi-mode approach shows a promising technique for future wideband high efficiency wireless transmitters.

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# Key Contributions

**First Contribution:** Study and analysis on a novel high efficiency mode termed Injection Power Amplifier (IPA). This mode is the focus of this thesis where the potential advantages of this mode in narrowband and wideband has been investigated.

**Second Contribution:** Utilization of RF current and voltage waveforms extracted from load-pull measurement for the development of the IPA mode.

**Third Contribution:** Design of a practical realization circuit for a narrow band IPA mode. The theoretical RF IPA mode has been compared to both the IPA mode validation measurement and the IPA prototype.

**Fourth Contribution:** Extending the IPA mode concept to be utilized in a multi-mode wide band PA design. A conceptual systems has been proposed based on a multi-mode PA approach.

**Fifth Contribution:** The proposed multi-mode wideband PA was designed and a prototype has been built. The achieved wide bandwidth and high efficiency operated at L band and the lower part of S band shows a promising technique for future wideband wireless transmitters.

# List of Publications

**First-Author Conference Papers:**

1. AlMuhaisen, A.; Wright, P.; Lees, J.; Tasker, P. J.; Cripps, S. C. & Benedikt, J. Novel wide band high-efficiency active harmonic injection power amplifier concept. Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International, 664-667.

2. AlMuhaisen, A.; Lees, J.; Cripps, S. C.; Tasker, P. J. & Benedikt, J. Wide band high-efficiency power amplifier design. Microwave Integrated Circuits Conference (EuMIC), 2011 European, 184-187.

**First-Author Transactions Papers:**

1. AlMuhaisen, A. ; Lees, J.; Tasker, P. J.; Cripps, S. C. & Benedikt, J. Novel Harmonic Load Injection Power Amplifier Concept. Microwave Theory and Techniques, IEEE Transactions [To be submitted].

2. AlMuhaisen, A. ; Lees, J.; Tasker, P. J.; Cripps, S. C. & Benedikt, J. Novel Wide Band High-Efficiency Power Amplifier Approach Beyond Octave Bandwidth. Microwave Theory and Techniques, IEEE Transactions [To be submitted].

**Other Papers:**

1. Carrubba, V.; Clarke, A. L.; Woodington, S. P.; McGenn, W.; Akmal, M.; AlMuhaisen, A.; Lees, J.; Cripps, S. C.; Tasker, P. J. & Benedikt, J. High-speed device characterization using an active load-pull system and waveform engineering postulator. Microwave Measurement Conference (ARFTG), 2011 77th ARFTG, 1-4.

2. Canning, T.; Almuhaisen, A.; Lees, J.; Benedikt, J.; Cripps, S. & Tasker, P. Utilization of RF I-V Waveform Load-Pull Information to Identify the Role FET Knee Profile has on Locating the Efficiency Maxima. Microwave Measurement Conference (ARFTG), 2011 78th ARFTG, 2011.

# Notation

| | |
|---|---|
| A | Amperes |
| ACP | Adjacent Channel Power |
| ACPR | Adjacent Channel Power Ratio |
| ADS | Advanced Design System |
| AM | Amplitude Modulation |
| AM-PM | Amplitude-Modulation-to-Phase-Modulation |
| BER | Bit Error Rate |
| BW | Bandwidth |
| C | Capacitance |
| CAD | Computer-Aided Design |
| CW | Continuous Wave |
| dB | Decibels |
| dBc | Decibels (reference to carrier power) |
| dBm | Decibels (reference to 1mW) |
| DC | Direct Current |
| DE | Drain Efficiency |
| DUT | Device Under Test |
| EER | Envelope Elimination and Restoration |
| EM | Electromagnetic |
| ESG | Electronic Signal Generator |
| ET | Envelope Tracking |
| EVM | Error Vector Magnitude |
| F | Farads |
| FET | Field Effect Transistor |
| GaAs | Gallium Arsenide |
| GaN | Gallium Nitride |
| Hz | Hertz |
| I | Current |
| $I_{dq}$ | Quiescent Drain Current |
| $I_{dss}$ | Saturation Drain-Source Current |
| IPA | Injection Power Amplifier |

| | |
|---|---|
| I-V | Current-Voltage |
| $I_{gen}$ Plane | Current-Generator Plane |
| IMD | Inter Modulation Distortion |
| j | Denotes the Imaginary Component of a Complex |
| L | Inductance |
| LDMOS | Laterally Diffused Metal Oxide Semi-Conductor |
| LSNA | Large-Signal Network Analyzer |
| m | Meter |
| MAG | Maximum Available Gain |
| NF | Noise Figure |
| NVNA | Nonlinear Vector Network Analyzer |
| OECD | Organization for Economic Co-operation and Development |
| P | Power |
| P1dB | Output Power at 1dB Gain Compression |
| PA | Power Amplifier |
| PAE | Power Added Efficiency |
| PAPR | Peak-to-Average Power Ratio |
| PEP | Peak Envelope Power |
| PUF | Power Utilisation Factor |
| R | Resistance |
| RF | Radio Frequency |
| RFPA | Radio Frequency Power Amplifier |
| SPA | Sequential Power Amplifier |
| S-parameters | Scattering Parameters |
| TDE | Total Drain Efficiecny |
| V | Voltage |
| VNA | Vector Network Analyser |
| W | Watts |
| WCDMA | Wideband Code Division Multiple Access |
| $\eta$ | Drain Efficiency |
| $\eta_{TDE}$ | Total Drain Efficiency |
| $\Gamma$ | Reflection Coefficient |
| $\Omega$ | Ohm |
| $X$ | Reactance |
| $Z$ | Impedance |

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# Chapter 1

# Introduction

In the past two decades, wireless communication systems have evolved dramatically and become a vital means of conducting daily life activities in modern societies for socializing and also in various sectors such as business, health and defence. In this thesis, research work has been carried out to investigate new methods of enhancing efficiency, bandwidth and output power of a Power Amplifier (PA). PAs are considered the bottleneck in wireless communication systems since PA defines bandwidth, efficiency and output power of RF transmitters.

This thesis begins with an introduction that sets the background essential for all the following chapters of the thesis and starts by introducing the research motivation in Section 1.1. Next, research perspective (Section 1.2) will be presented. In Section 1.3, an overview of wireless communication systems requirements for future generations are presented. Section 1.4 shows the effect of the RFPA (RF Power Amplifier) performance on the overall performance of RF transmitters in terms of energy efficiency. Next, a background on PA design, figure of merits and PA structures to enhance PA performance will be presented in Section 1.5. Finally in Section 1.6,

we will provide an overview of the next chapters in this thesis.

## 1.1 Research Motivation

This research is aimed to investigate novel PA design concepts for high efficient PAs. It also considers PA efficiency for future wireless applications with high transmission bandwidth as well.

## 1.2 Research Perspective

In modern times, wireless communication systems are the backbone of the modern world. According to recent estimates, the number of wireless subscribers is increasing by millions yearly and revenues of the market is hundreds of billions of dollars . For instance, in OECD (Organization for Economic Co-operation and Development) countries[1] the wireless broadband subscriptions have shown an annual increase since the beginning of the 1990s as shown in Fig. 1.1 [1].

The wireless market accordingly benefits massively from the increasing consumers demand for a wireless access point. Figure 1.2 shows that mobile networks has experienced annual growth more than any other communication technology in the period 2005-09. This clearly indicates that this is a mass-market industry [1].

These estimates highlight the importance of the industry and the huge demands for wireless access from consumers. However, the ra-

[1]OECD is an organizations of 34 member countries span the globe and include many of the world's most advanced countries and also emerging countries.

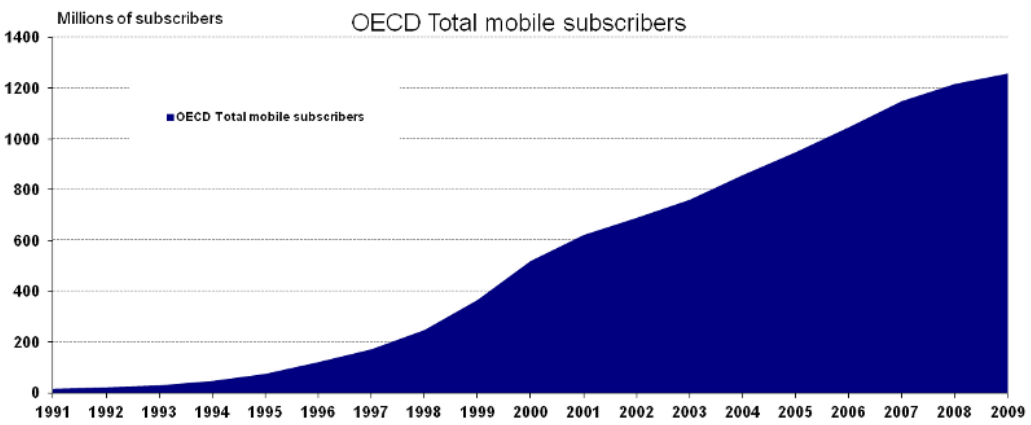



**Figure 1.1: OECD total mobile subscribers [1].**

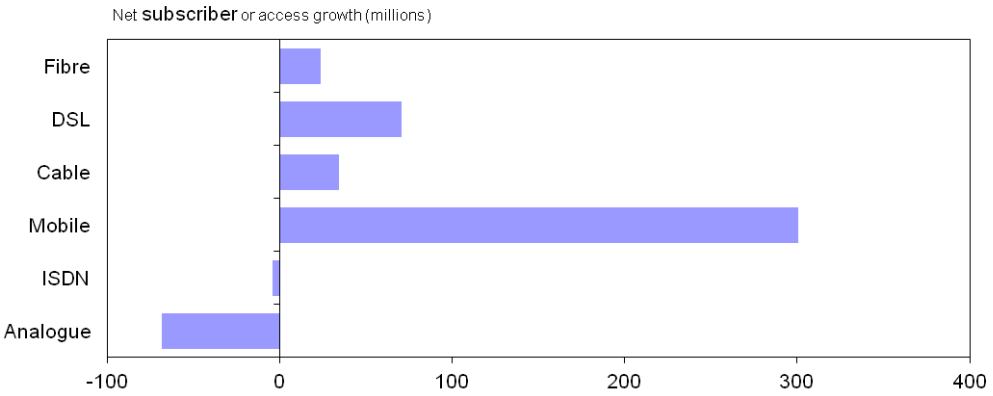



**Figure 1.2: Net access path growth of different communication technologies between 2005-09 [1].**

pid increase in the wireless global penetration are having severe effects on the environment. This is due to the the low energy efficiency exhibited by wireless communication systems coupled with a huge power consumption. This affects seriously the environment, for instance, an estimate of an equivalent of 11 tons of carbon dioxide is produced yearly by a typical 3G site [2]. In addition, as the expected rapid growth of wireless communication systems derived by

various applications and consumer demands continues, there is an urgent need for a dramatic improvement in the efficiency of these systems. Several projects have been initiated by the industry requirement to address energy efficiency of wireless communication networks. An example is the UK mobile Virtual Centre of Excellence (VCE) Green Radio project which is a major research program funded by industry and the Engineering and Physical Sciences Research Council (EPSRC) in UK. [3]

## 1.3 Wireless Communication - Evolution and Challenges

Since the beginning of history, societies communicate in traditional ways such as face to face contact, a message that can be sent physically or using very simple ways such as smoke signals over a line-of-sight distance. As the science progressed, societies used more developed means such as a telegraph which was invented by Samuel Morse in 1838 and then by telephony. Later in 1887, Hertz proved the existence of EM (electromagnetic) waves which had been predicted by Maxwell in 1867. In 1895, Marconi had successfully demonstrated the first wireless transmission across a distance of 18 miles from the Isle of Wight to a tugboat [4]. This new technology had opened a new era and wireless communication was born.

Nowadays, wireless communication is the fastest growing sector in communication systems driven by the consumer demands for wireless applications such as mobile devices, smart phones, portable

devices, internet access along with the required high data throughput. The increasing demand for high data rate drives the mobile technology to respond and offer improved services and standards. For instance, the first mobile generation (1G cellular) introduced in the early 80s was based on analog network operated at 900 MHz band. The second mobile generation system (2G cellular) was based on digital networks using TDMA, GSM TDMA, and CDMA modulation schemes and introduced a decade later in the early 90s. This 2G system offered much improved services relative to their predecessor 1G cellular systems. The 2G cellular system has evolved to the 2.5G and 3G cellular systems operated in higher frequency bands reaching up to 2.1 GHz. Nowadays 3G cellular systems are in operation around the world, offering more data throughput and enhanced functionality [5]. The currently emerging LTE systems are designed to offer even higher data throughput; this sets a requirement for broader bandwidth and higher linearity coupled with demands for lower cost and enhanced services.

This evolving wireless technology has serious effects on the energy systems; a typical GSM and WCDMA base station consumes 800W and 500W respectively [6] while a fully loaded 3G cell site consumes on average 3 kW of power [2]. Another way of defining the consumed energy in a wireless link is by using the energy consumption per information bit. For a typical cell size of radius 1000 m of a High-Speed Downlink Packet Access (HSDPA), the required energy per information bit is 8.2 $\mu$Joules/bit [3]. A direct result of this increasing energy consumption on the environment is the increase of the

greenhouse gas emission, which was pointed out in the beginning of this chapter. An estimated of 1% of the green house gases are the product of the cellular networks. Furthermore, the highly inefficient power consumption by wireless base stations translate directly into high operating expenses. For instance, the wireless access part of the cellular network contributes to most of the energy cost by 70% of the total energy bill in many mobile operators [7]. Figure 1.3 shows an example of the energy consumption of a typical wireless cellular network showing that most of the energy consumption is in the base stations. [8]

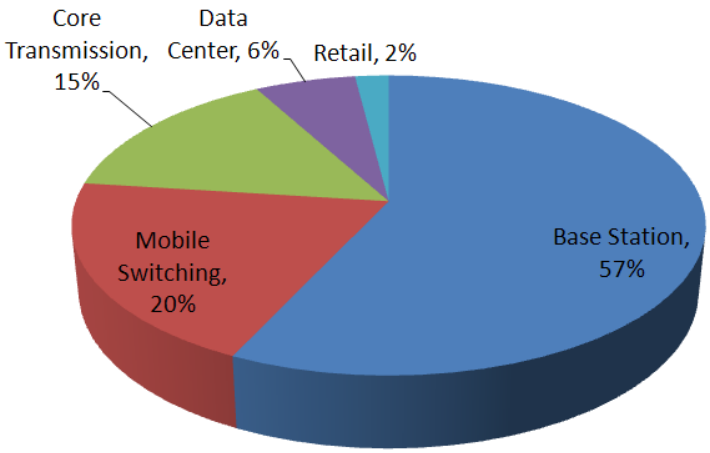



**Figure 1.3: Energy consumption in a typical wireless cellular network.**

In addition, since there has been a rapid deployment of wireless communication systems around the world in the past two decades, the importance of improving the performance of these systems has been a common understanding and a target for governments, industry and other international unions. This realization of the huge power consumption has driven the push towards more efficient "green"

communication systems. As a result, future wireless systems have a challenge of not only offering all the advantages of LTE systems such as the high data throughput demand but also to provide energy efficient systems. [4]

## 1.4 RFPA - Key Component in RF Transmitters

The wireless access points are a major energy drain where most of the energy is consumed by the RF front-end of the transmitters. For instance, 80% of the energy demands of base station are consumed by the radio part. The need for highly power efficient RF transmitters requires a design of efficient RF PAs, since PA accounts for more than 50% of the radio consumption power [9]. A detailed Pie chart concerning power consumption of a typical base station is displayed in Fig. 1.4. [10]

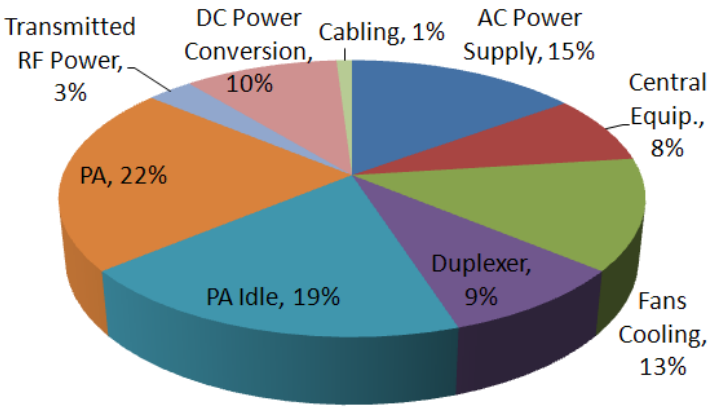



**Figure 1.4: Energy consumption in a typical base station.**

In addition, the efficiency of RFPAs also affects the other critical aspects of the wireless communication systems such as battery

cost, electrical power expenses, weight of power supplies and size of cooling systems, which on the other hand have also a significant impact on the environment. As a result, there is a large demand for improving RFPAs which is the focus of this research.

## 1.5 Power Amplifier Design

PAs amplify signals by converting DC power into a significant amount of RF power. PAs are categorized according to mode of operation, implementation and architecture. For a particular application, PAs are designed to specific requirements such as linearity, efficiency, gain, bandwidth, output power or a combination of those requirements. This also determines the chosen design method. Linearity and efficiency in modern wireless communication systems are the most significant factors. Linearity concerns the signal integrity, while the efficiency defines the energy consumption of the system.

The design of a highly linear and efficient PA is a challenge to be met simultaneously. This can be explained by looking at the input-output power characteristics of a PA as shown in Fig. 1.5. In the linear region, the output power ideally consists of only the fundamental frequency, the gain in the linear region is fixed (in this example, the linear gain is 10 dB). The theoretical efficiency at Peak Envelope Power (PEP) of class A and class B mode of operation is 50% and 78.5% respectively. However, if the power amplifier is allowed to operate in compression region, the efficiency is improved by generating more efficient current and voltage (I-V) waveforms at

the cost of a degraded linearity.

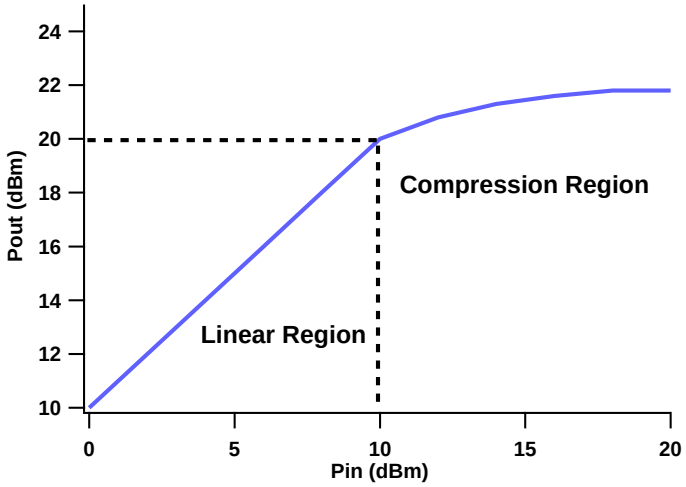



**Figure 1.5: Linear and compression region of power amplifiers .**

Usually, a trade-off between those two critical factors is considered in PA design. For instance, in constant envelope applications there is a very useful trade-off between efficiency enhancement and linearity. Applications using modulation techniques such as FSK (Frequency Shift Keying) and BPSK (Binary Phase Shift Keying) can tolerate significant amount of amplitude and phase distortion [11] and here the linearity can be traded for efficiency and RF output power. In those applications overdriven PAs are used to improve efficiency. This improvement is achieved by driving the active device into the compression region and also by appropriate harmonic terminations to attain high efficient current and voltage waveforms. For example, a class F amplifier achieved high efficiency by transforming the voltage waveform at the output of the active device from a sine wave to a square wave. [12]

On the other hand, for amplitude modulated applications such as Quadrature Amplitude Modulation (QAM) applications as in 16-QAM and 64-QAM, linearity is the critical aspect of the system. Most of the efficiency enhancement techniques in these applications are developed to improve efficiency at low power back-off levels as in Doherty Amplifier, the Outphasing Amplifier, Envelop Elimination and Restoration technique, and Envelop Tracking.

Research on linearity derived by the tight specs of the communication standards have pushed the industry to more linear systems. As a result, the high linearity specs are met while efficiency is still less of a concern in modern communication systems. Currently, in academia and industry there are an increasing concern about efficiency and future systems are required to address both linearity and efficiency simultaneously.

### 1.5.1 Linearity

Linearity is the most critical design requirement because non linear transmitters cause distortion in the amplification process of the input signal, hence data loss. The distorted signal is not only affecting the integrity of the transmitted signal but also generates signals at other frequency channels. These unwanted signals will be a potential source of distortion to the adjacent channels. Hence, there are two practical issues of concern in the context of wireless communication: PA nonlinearity, and adjacent channel interference. PA nonlinearity takes the form of amplitude distortion (AM-AM), and phase distortion (AM-PM). While the adjacent channel interference

comes in the form of unwanted signal generated in the out-of-band channels. Hence, linearity standards are specified to minimize the distortion generated by transmitters to a level where all channels can operate effectively. [11, 13]

In constant envelope applications, a highly non-linear PA can be used that operates in a saturation (compression) region to provide high efficient operation. An example is Global System for Mobile communication (GSM) where Gaussian Minimum Shift Keying (GMSK) modulation is used. In these modulation schemes, the amplitude is fixed and thus, avoids zero crossing which is the main cause of spectrum regrowth. As a result, a good linearity margin in adjacent channels is offered in these modulation schemes. For harmonics of the carrier, filtering processes can be used to eliminate out-of-band signals [14], hence, linearity requirement is met with an efficient use of the energy.

On the other hand, variable envelope modulation schemes can eliminate out of band signals but can not usually eliminate the Intermodulation Distortion (IMD); hence, a high linear transmitter is an essential requirement and usually PA is operated in back-off levels, i.e. lower than the PEP to minimize these effects.

Wireless communication standards specify the maximum acceptable power generated in these unwanted frequencies radiated by non-linear transmitters. Thus, various measures are considered for linearity characterization according to the application and the characteristics of the input signal.

A variety of methods are used to measure linearity. The traditional linearity measure is Carrier to Intermodulation (C/I) ratio. This is where a PA is driven by more than one carrier so the generated output signal is composed of fundamental, harmonics, sum and difference of the input signals. The harmonics are filtered out and the prime concern is the sum and difference of the input signal, called intermodulation products. The C/I ratio is measured by comparing the amplitude of the largest intermodulation product to the amplitude of the carriers. Typically, a linear PA will have a C/I greater than 30 dB. [15]

Most modern system's linearity requirements are defined by more complex measurement techniques; this includes Adjacent Channel Power Ratio (ACPR) and Error Vector Magnitude (EVM). ACPR measures the level where the signal power spread into the adjacent channels. ACPR is defined as the ratio of the power generated in a specified band outside the desired signal operating bandwidth to the power in the signal bandwidth. The minimum ACPR requirement of the 3rd Generation Partnership Project (3GPP) specification for a carrier spacing of 5 MHz is -35 dBc [16]. EVM is a measure for the linearity of both the transmitter and especially the receiver. EVM is defined as the ratio of the error vector magnitude (i.e., the magnitude difference between the actual demodulated vector location and the ideal vector location) to the magnitude of the ideal vector location. For most mobile communication systems, EVM is in the range of 5% to 10% [13]. For example, the minimum EVM requirement for a 16-QAM in the 3GPP specification is 12.5% [17] and is usually

implemented in a range of less than 5%. [18]

Often for linear PA design, the PA is operated at back off levels from the saturation condition to attain a satisfactory linear operation. In addition, there are a number of linearization techniques that can be employed in the transmitters to improve the linearity such as feedback, feed forward, and digital predistortion (DPD).

### 1.5.2 Efficiency

Efficiency is a critical factor, as mentioned earlier, in PA design. There are different definitions for efficiency that is preferable for different applications. Drain Efficiency $(\eta)$ is concerned only by the DC to RF fundamental power conversion and defined as:

$$\eta = P_{out}/P_{dc} \tag{1.1}$$

Power Added Efficiency (PAE) adds gain information to provide a suitable description of the PA performance. PAE is defined as the ratio of the difference between output and input power to the DC power, i.e.:

$$PAE = (P_{out} - P_{in})/P_{dc} \tag{1.2}$$

In addition, drain efficiency and PAE can be extended to include any DC power consumed by any circuit or system in the amplification process;

$$\eta_{total} = P_{out}/(P_{dc} + P_{dc\_system}) \tag{1.3}$$

Both equations provide an instantaneous drain efficiency at a specific drive (input power) level. This instantaneous efficiency defini-

tion is suitable for constant amplitude signals where PAs are operated at PEP. However, for a time variable amplitude signal, average efficiency provides an accurate measure. Average efficiency ($\eta_{AVG}$) is defined as the ratio of the average RF output power to the average DC power:

$$\eta_{AVG} = P_{outAVG}/P_{dcAVG} \tag{1.4}$$

Average efficiency calculation for a variable envelope signal requires the consideration of signal statistics such as Probability Density Function (PDF) and Cumulative Distribution Function (CDF). PDF measures the probability of specific magnitude of the envelope to occur while CDF considers the likelihood that a given magnitude would not be exceeded. For a multi-carrier signal, the PDF shows a Rayleigh distribution with a typical Peak-to-Average Power Ratio (PAPR) in the range of 6-13 dB which reduces significantly the efficiency. To put this in perspective, class A and class B have drain efficiencies at a PEP of 50% and 78.5%, which for a PAPR of 10 dB reduces to 5% and 28% respectively. [15]

In the past decades, however, many techniques for efficiency enhancement has been well researched and many old techniques, long forgotten, have re-emerged and been looking at again derived by the low average efficiency experienced by modern RF transmitters.

### 1.5.3 Basic PA Design Techniques

PAs amplify signals in different classic techniques such as class A, B and C according to the biasing of the quiescent current. Class A

operates in the active region of the transistor with a bias point midway between pinch-off and saturation. While class B is biased at pinch-off, and is only active for half the period of the input drive. Class C is biased at less than the pinch-off, and is active for less than half of the period. In Class B and Class C, the current waveform has a fundamental frequency and also harmonics of the fundamental frequency; those harmonics are shorted to prevent harmonics power generation. In these classes, there is trade-off between output power, drain efficiency and linearity.

The performance of PAs are usually analyzed as a function of a conduction angle. The conduction angle is the portion of the input signal cycle where the amplifier conducts. For example, a $360^{\circ}$ input signal conduction angle (i.e., Class A) indicates that the amplifier conducts during the full cycle of the input signal. To show PA's efficiency performance as a function of the conduction angle, DC and fundamental components of the Fourier serries[2] of the current waveforms are calculated [19] and plotted in Fig. 1.6.

At the full conduction angle (i.e., class A), both DC and fundamental amplitudes are equal, with drain efficiency of 50%. As the conduction angle is reduced, the fundamental component of the current waveform is slightly increased at class AB and then returns back to the same amplitude level at half of the conduction angle (i.e., class B). As the conduction angle is reduced from the class B condition towards deep class C, the fundamental component decreases

[2]This analysis is for $I_{max}$= 1A and $V_{dc}$= 1V. An ideal conditions are assumed where the maximum RF voltage swing is $2V_{dc}$ with no knee effect. Maximum RF current reaches up to $I_{max}$ and all harmonics are shorted.

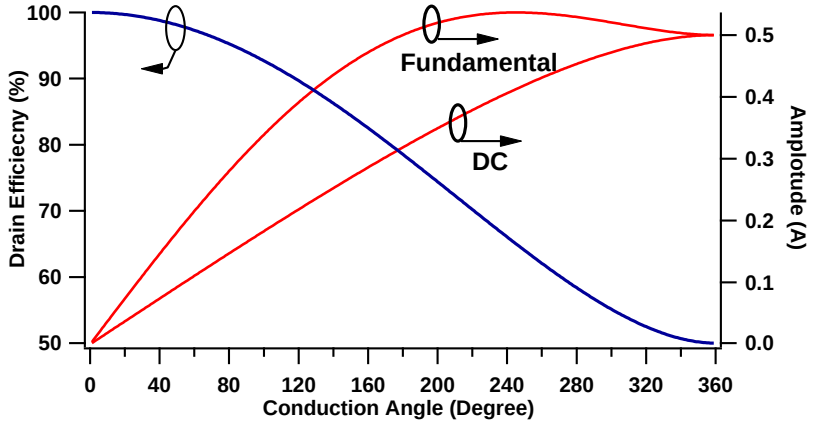



**Figure 1.6: Efficiency enhancement as a function of conduction angle.**

and reaches zero when PA is in a no conduction condition (i.e., conduction angle = zero). On the other hand, the DC component is reduced monotonically from class A towards class C. Accordingly, drain efficiency increases as the conduction angle is reduced from class A to class C.

### 1.5.4 Power Amplifier Architectures

In modern wireless communication, multi-carrier technologies are used to transmit many channels simultaneously for an efficient use of the primary resources, power and bandwidth. First, from a frequency spectrum perspective, the bandwidth is a limited resource which needs to be utilized efficiently. Second, from power efficiency perspective, a multi-carrier technology can reduce significantly the energy consumed by a PA, for example, in a 6-carrier technology the maximum energy consumption of a PA can be reduced by 30 % [9]; however, as multi-carrier technology evolved into utilizing more complex modulation schemes, the resulting variable envelope has a

high PAPR. Various techniques and architectures exist that address both efficiency and linearity for variable envelope signals. Some of these techniques were developed decades ago and have still generated a high research interest in the last decade such as Doherty Amplifier.

Each of those PA structures enhancement techniques is based on optimizing PA performance not only at PEP but also across a good dynamic range. Thus, a PA is required to perform well at high power region, and also at lower power region. High power amplifiers are usually optimized at or near compression region. Hence, in the low power region, they are far from the optimum case. That results in operating PAs not utilizing the full potential of the available drain's current and voltage power supply, accordingly that reduces the RF to DC conversion process.

Each of those PA structures improves PA performance by optimizing the set that defines PA operation. This can be in a form of presenting optimum loading, biasing control or combining two PAs or more that are optimized at different power levels. This can be further explained in the output power equation of a PA. Ideally, PAs are current source devices where the output drain current is a function of the gate biasing and input drive. The output voltage developed across the output load is a function of the output current; the output power thus can be written as [19]:

$$P_{out} = V_{rms} \cdot I_{rms} = \frac{V_f}{\sqrt{2}} \cdot \frac{I_f}{\sqrt{2}} = \frac{V_f^2}{2R} \tag{1.5}$$

where $V_f$ is the magnitude of the fundamental voltage, $I_f$ is the magnitude of the fundamental current, and $R$ is the output load. Equation 1.5 shows that the instantaneous output power is defined as function of the RF fundamental voltage and load presented to the PA. The input drive and gate bias controls indirectly the output RF voltage which can swing ideally up to $2V_{dc}$. To convert DC to RF power efficiently, the PA needs to utilize the full rail-to-rail voltage swing, i.e., the magnitude of the output RF fundamental voltage reaches the magnitude of the drain voltage supply. However, at back off power levels the RF voltage swing is reduced and that translates directly to a drop in the efficiency. This even gets worse in class A, where the transistor constantly draws a fixed quiescent current, thus, a fixed DC power is consumed regardless of the level of the input signal. While in other classes as in Class B, the DC power consumption is reduced as the driver level reduced.

Efficiency enhancement techniques, therefore, are required to maximize the RF fundamental voltage swing; this can be achieved by different techniques. One approach is to use a parallel PAs structure where each PA is optimally loaded and activated according to the drive level. The activation of these parallel PAs can be done by using the gate bias, which is called gate switching technique. Another approach is to utilise RF switches to activate different PAs at different drive levels as in the stage-bypassing technique.

Another approach is by controlling dynamically the voltage drain supply or the load. For instance, at a lower back off levels, where the transistor does not fully utilize the DC power, the load can be

increased to restore the RF voltage swing to its full potential. Another method is to reduce the voltage drain bias proportionally, as the drive signal decreases from the saturation condition, thus reducing the DC excess power. Therefore, PA enhancement architecture techniques can be categorized into three main categories: parallel linear power amplification, supply modulation techniques and load modulation techniques.

#### 1.5.4.1 Parallel Linear Power Amplification by Using Sequential PA, Stage-Bypassing and Gate Switching

To tackle the efficiency problem at power back off levels, the full RF voltage swing is required to be maintained. This can be achieved by using parallel transistors with different device peripheries such as in a Sequential Power Amplifier (SPA), stage switching and gate switching techniques. The output power can be directly coupled or by using conventional power combiners.

SPA uses multiple devices where at lower back off levels the main PA device is active until the saturation level is reached, then a peaking PA device with a larger device periphery starts operating at higher power levels and therefore maintains linear amplification with an improved efficiency at the lower power levels. This technique is more comparable to the Doherty PA where a peaking PA is inactive at lower back off levels, however, in SPA there is no load modulation occurring. In addition, the basic concept of SPA is not limited by a bandwidth restriction; this makes SPA suitable for broadband applications. A main consideration in the SPA structure is the design of

the combination process of the output power of those devices. The coupling ratio of the combiner is required to be designed in accordance to the PDF of the signal to optimize the average efficiency. [19, 20]

On the other hand, stage switching or stage-bypassing architectures use RF switches at the input and output of the main device (the larger device). At low power region, the main device is bypassed by the switches and thus prevented from consuming DC energy and only the low power device is active. At high power levels, the RF path switches to the high power stage; thus, the DC power of the large PA is used only when needed at the high power levels. However, the design needs to consider hysteresis effects and distortion due to switching transients. [21, 22]

Another approach is to activate the larger device at only the higher power levels by controlling the gate bias and generally termed the gate switching technique. The advantage is the absence of the losses in switches; and also considered as a candidate for broadband applications since there is no bandwidth restriction in this PA structure. However, due to the direct output coupling of the two devices, the input and output impedances vary as the higher device activated. [21, 23]

#### 1.5.4.2 Load Modulation

Load modulation changes the instantaneous load impedance presented to a PA and thereby the instantaneous amplitude. In regard to tackling the low efficiency exhibited by a PA in the low power region,

this technique improves drain efficiency at back offs by utilizing the fact that the optimum loading varies for different output powers. Basically, to maintain the full rail-to-rail RF voltage at the low power region, the impedance is increased to satisfy that condition. Therefore, in principle maintaining the high drain efficiency at PEP across the full dynamic range. The output power in this case is mainly a function of the output current.

The basic and intuitive approach is based on electronic tunable components such as pin-diode switches, Micro-Electro-Mechanical Systems (MEMS) switches and MEMS capacitors. MEMS switches have many advantages compared to pin-diode switches such as the very low power consumption, very low insertion loss, high linearity, high isolation and low cost. RF MEMS capacitive switches have inherent drawbacks such as the required high actuation voltage and low switching speed. In addition, the dielectric charging problems and temperature sensitivity of the movable membrane in MEMS capacitive devices lead to major limitations such as the power handling capability [24].

An example, which has been demonstrated at HF frequency is using electronically tunable inductors and capacitors. The measured average efficiency was doubled relative to class B for a Rayleigh-envelope signal with a 10 dB PAPR [25]. Furthermore, varactor-based tunable matching networks demonstrated at UHF frequency of a high power (7W) PA showed a significant increase of absolute 10% at 10 dB back off [26]. This approach has the advantage of being suitable for broad band application, however, it is still evol-

ving to overcome challenges in microwave frequencies such as linearity, reliability and tuning delay. [25, 27, 28]

Another approach uses the interaction between two PAs to actively perform load modulation. This is the case for the outphasing technique and the Doherty PA. The outphasing technique proposed by Chireix [29] in 1930s, often referred to as Linear Amplification using Nonlinear Components (LINC), describes a transmitter structure rather than a conventional PA. It consists of two parallel transistors which are driven by a phased-modulated signal at a constant amplitude. The output modulated amplitude is a vector sum of the two constant amplitudes with a varying phase difference. The effective outcome of the structure is performing load modulation which allows high efficiency at low power region. At PEP, the two carriers are in-phase and therefore achieving maximum theoretical efficiency. At back off, the two carrier PAs are almost phase-canceled, however, Chireix technique is able to perform well at this region due to the load modulation that is taking place which effectively reduces the DC power drawn form the supply. [30]

The most widely researched and implemented load modulation technique for the last decade is Doherty PA. In contrast to Chireix, it uses linear PAs and presents more of a PA function rather than a transmitter architecture. In the classic Doherty PA, two PAs of equal periphery size are coupled through an impedance-inverting network (typically a quarter wave transformer), where the main PA is biased in class B and the auxiliary (peaking) PA ia biased at class C [31]. The load presented to the main PA is actively loaded in the

high power region by the interaction of the peaking PA to maintain a constant voltage swing. The main PA is active in the lower power region with the peaking inactive and decoupled from the output network by an inverting impedance network, as the drive level increases, the output power reaches saturation where the RF drain voltage equals the DC drain supply voltage. The impedance presented to the main PA is R Ohm, here drain efficiency is 78.5% at 6 dB from PEP. As the input drive increases, the peaking PA kicks in and supplies current to the load, thus appearing as an increase in the effective load impedance. By using a quarter wave transformer, this increase in the impedance is transformed to a decrease in the effective impedance presented to the main PA. Thus, as the input signal increases, the effective impedance presented to the main PA is reduced to maintain a constant full RF voltage swing. At PEP, both PAs see half of the load impedance presented at 6-dB back-off (i.e., R/2 Ohm) and contribute to the final output power with efficiency equals to class B (78.5%). Doherty PA is often designed to a specific dynamic range where the signal statistics of a specific application are used to design for a specific back-off level. Doherty PA suffers from the bandwidth restriction of typically 10%; this is due to the quarter wavelength transformer used in the output network and the requirement of an accurate phase matching between the two paths [13, 19, 21]. The concept of Doherty PA might be looked at as a parallel linear amplification as in gate-switching or as a stage-bypassing technique but the essential difference lies in the active load modulation within the PA structure.

#### 1.5.4.3 Supply Modulation

Supply modulation controls the DC bias according to the drive level and consequently to the required output power. The control signal for the DC bias is generated by detecting the envelope of the input signal and then input into a step up DC-to-DC conversion process. Although this increases the system complexity and cost, it facilitates a significant improvement in drain efficiency at back-off provided that an efficient DC-to-DC conversion is maintained. This technique can be seen in Envelope Tracking (ET) and Envelope Elimination and Restoration (EER) architectures, in which the voltage drain bias is varied and also in adaptive bias technique when the gate bias is adapted. The advantages in these techniques are that they are suitable for broadband applications since there is no bandwidth restriction, which is a severe limitation for other techniques using load modulation, such as Doherty PAs.

EER systems proposed originally by Kahn [32] as an efficiency enhancement technique for Single-Sideband (SSB) transmitters. The technique basically splits the carrier and the envelope amplitude and feeds the phased-modulated carrier into a non-linear PA (such as class C, D, E, F) to be amplified efficiently to the desired level. The amplitude envelope is detected, amplified to remodulate the phased-modulated carrier by controlling the drain voltage supply, thus restoring the envelope amplitude into the output RF signal. EER transmitters are generally linear since the RFPA amplifies a constant carrier amplitude signal and therefore linearity in EER depends strongly on the modulator. The critical two factors that affect linearity are

the envelope bandwidth and the accurate alignment of the envelope and phase modulation. [21]

In ET, the drain voltage supply of a conventional linear PA is modulated directly by the level of the input drive. The envelope detector will reduce the unnecessary excess DC power and accordingly increases the efficiency. In principle, the efficiency enhancement can be maintained across all output power levels. One main advantage of the ET is that the output RF signal does not rely on the accuracy of the envelope detector and thus the requirement for the envelope detector is much simpler than other techniques such as EER. The ET technique as in EER, is based only on supply modulation and both are decoupled from RF matching; thus, there is no complexity in the design of the RF load at different drive levels. In addition, for more a simpler approach, a DC supply with switches can be used to output different voltage levels. The primary concern in such design is mainely linearity issues caused by the unwanted modulation from the supply voltage [19, 21, 33]. Current research on ET has reported good efficiency and linearity enhancement results, making it suitable for mobile handsets and transmitters of 3G and 4G mobile communication systems. [34, 35, 36, 37]

Another approach in supply modulation techniques is concerned with enhancing class A efficiency in the backoff region. Ideal DC drain bias current in class A is fixed at half of the maximum drain current and that is the main reason for the low efficiency exhibited in class A mode. In this technique, the DC bias current is forced to be proportional to the drive level and thus reduced at lower back-off

levels. Hence, efficiency is improved at back-off by adapting the gate bias rather than controlling the drain supply as in ET, hence, called the adaptive bias technique. The main advantage is that this technique is suitable for a linear PA that is operated well below the PEP. However, the designer should take care to design a fixed gain across the dynamic range. [13, 38]

## 1.6 Research Objective & Thesis Structure

This thesis seeks to address the design and development of high efficient RFPAs whilst broadening the operating bandwidth which is required for wide band applications. Therefore, the first objective is to investigate high efficient modes looking from a waveform engineering perspective. The second objective is an investigation for high efficiency broad band operation.

The structure of the thesis is written where each part starts with a background to cover the relevant literature. The thesis has been divided into two main parts, the first presents a novel concept for high efficiency PA design termed Injection Power Amplifier (IPA). The theoretical analysis of the new mode is first presented, followed by a validation measurement and PA demonstrator. The second part presents an investigation to extend the IPA concept to broadening the operating bandwidth of a complete functioning PA.

**Chapter 2** begins the first main part of this thesis and starts with a literature review on classic PA modes looking in detail at PA behavior from a current and voltage waveform perspective. Next, the

proposed novel PA mode will be presented along with supporting theoretical analysis.

**Chapter 3** draws on chapter two and examines the theoretical part by using a validation measurements. A brief overview on the active load-pull system used in the validation measurement will be presented. Next, the validation measurement will be compared to the theoretical part and followed by a discussion.

**Chapter 4** describes the design, synthesis, characterization, and evaluation of a PA demonstrator for the proposed concept. Starting with a quick background on PA design techniques for small signal, large signal technique and PA design based on waveform engineering. Next, PA demonstrator design will be presented along with the measurement results. This will conclude the first main part of this thesis for IPA theory, validation and prototype.

**Chapter 5** begins the second main part and starts with an overview of today's high efficiency wideband RFPA design. Then it looks at extending the IPA concept to wideband design. Next, a novel multi-mode approach that combines passive networks and active injection is presented.

**Chapter 6** will focus on the design and realization of the wide band PA demonstrator. It starts by showing a strategy for a circuit design to realize a double-octave bandwidth. Next, the proposed multi-mode is designed and the PA prototype is built and measured.

Finally, **Chapter 7** draws conclusions and summerises the thesis.

In addition, future work and suggested extensions to this research are also presented.

# *Chapter 2*

# High Efficiency Power Amplifier Design

## 2.1 Introduction

Power amplifiers can be generally categorized into two groups: current mode where the transistor behaves as a current source, and switched mode where the transistor operates as a switch. PAs that operate as switches are highly efficient and suitable for many applications. However, for applications that require linear amplitude amplification, PAs are operated as a current source. There are various RF Power amplifier classes in each mode of operation and each has its own advantages and disadvantages. According to the application and specific system needs, PAs can be designed to satisfy the application requirements.

In this chapter, first we will look at the essential parameters that describe PA performance. Next, we will present a vital theory in power amplifier design known as load line theory. Then, PA classes operated as a controlled-current-source will be presented looking in detail at the performance of each class. After that, we will discuss other possibilities of reaching other modes of operation by using wa-

veform engineering. Next, a novel theory will be introduced presenting a new mode of operation termed active harmonic load injection. Finally, we will summarize this chapter.

## 2.2 RF Power Amplifiers: Essential Performance Parameters

Power amplifier performance is defined using several parameters, some of the key design parameters are: output power, gain, linearity, efficiency, bandwidth, Power Utilization Factor (PUF). Other parameters are also important such as: return loss, stability, isolations, DC bias voltage and current, robustness, cost, reliability, size, weight, etc.

**RF Output Power (Pout)** is the RF output power converted from the supplied DC power.

**Gain** is a ratio of the output RF power relative to the input RF power and defined as:

$$Gain = Pout/Pin \tag{2.1}$$

**Linearity**, as previously indicated in Section 1.5.1, describes the integrity of the transmitted signal.

**Efficiency** as been also presented in Section 1.5.2, it shows how efficient the DC to RF output power conversion is. There are different efficiency equations such as Drain Efficiency in Eq.1.1 and PAE in Eq.1.2.

Another drain efficiency definition that will be used in this thesis, considers the DC power from the main PA and also any DC power from auxiliary PAs termed here as Total Drain Efficiency (TDE):

$$\eta_{TDE} = P_{out}/(P_{dc\_main} + P_{dc\_aux}) \tag{2.2}$$

**Bandwidth (BW)** is the operating bandwidth of the transistor. It is also called instantaneous BW if it describes the BW without any tuning. If there is any type of tuning it is termed tunable BW. Also, there are other definitions often used such as percentage BW and octave BW defined [39] as:

$$BW = F_H - F_L \tag{2.3}$$

$$Percentage\,BW = \frac{F_H - F_L}{F_C} \tag{2.4}$$

$$Octave\,BW = \frac{log\frac{F_H}{F_L}}{log\,2} \tag{2.5}$$

where $F_L$ is the lowest frequency, $F_H$ is the highest frequency and $F_C$ is the centre frequency.

**Power Utilization Factor (PUF)** is the ratio of the output power delivered in a specific mode to the power that would be delivered if operated in class A mode [19] as shown in Eq. 2.6. Hence, PUF is a parameter that can be used to compare different PA classes according to the maximum output power that can be delivered from that mode of operation.

$$PUF = 10\log(\frac{P_{out}}{P_{class\,A}}) \tag{2.6}$$

## 2.3 Real PAs: Main Constrains and Loss Mechanisms

The major limitations of practical real PAs is on-state resistance, parasitic output capacitance, voltage breakdown, and implementation losses. Those unavoidable losses affects the performance of PA in terms of output power, maximum operating frequency, gain, etc.

$\mathbf{R}_{on}$ is the on-state resistance that appears across the transistor. The voltage developed across it due to this resistance is usually a fraction of the DC voltage supply. However, the power dissipated across this small resistance accounts for part of the loss in a practical PA. This effect is termed knee effect which reduces the maximum allowable voltage swing and that translates directly to unavoidable degradation in drain efficiency typically by $10\%$.

$\mathbf{C}_{ds}$ is the most significant output parasitic capacitance. This shunt capacitance changes the RF load line trajectory where the RF voltage does not follow the RF current with a $180^{\circ}$ phase shift. Thus, some of the output power will be reduced according to this delay caused by the shunt capacitor, hence an additional inductive circuit is required to compensate this capacitive effect. However, this parasitic effect is frequency dependent for a fixed value which creates more of a challenge in the broadband design. Since the output matching network needs not only to transform the output load to the required optimum load, presented to the transistor at the current generator plane for a single frequency, but also should take account of the frequency dependency of the device's output impedance cau-

sed by the drain-to-source capacitance. Moreover, there are other parasitics but are much less significant and that includes bondwire inductance and the package parasitic. [19]

**Voltage Breakdown** is the maximum allowable voltage that a PA can stand without damage. The required breakdown voltage takes into account the operational requirement for robustness in a substantial mismatched condition. This also extends to include the package dielectric breakdown for the device (PA). [5]

**Implementation Losses** are unavoidable losses of a PA implementation for a specific structure or topology including transmission lines losses.

## 2.4 Load Line Theory

For maximum power transfer, it is known that the load impedance should be a conjugately matched to the source impedance. However, with the voltage knee effect present, the optimum impedance for real PAs is different and can be explained by load line theory. Load line theory [19] is based on simplified linear analysis which accounts for the knee effect. The output power, efficiency and gain for different modes of operation can be examined and analyzed. In addition, any parasitic effect can also be considered and can be compensated for in the output matching network.

Fig. 2.1 shows a class B dynamic RF load line trajectory for low impedance ($R_L$), high impedance ($R_H$) and optimum impedance

($R_{opt}$). For a power match, the ($R_{opt}$) equation is:

$$R_{opt} = (V_{dc} - V_{knee}) \cdot \frac{2}{I_{max}} = \frac{2\,(V_{dc} - V_{knee})}{I_{max}}\,. \tag{2.7}$$

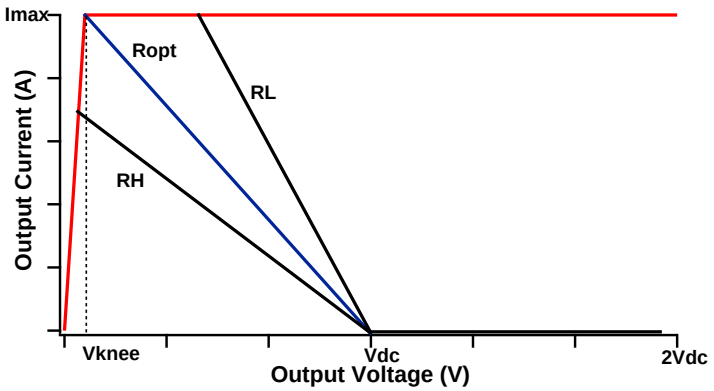



**Figure 2.1: Load line trajectories for different load conditions.**

For maximum power transfer, as can be seen in the $R_{opt}$ condition in Fig. 2.1, the current swings from zero to $I_{max}$. While the voltage swings from $V_{knee}$ to $(2V_{dc} - V_{knee})$. On the other hand, the other load conditions will limit the output power, and that can be seen in both the $R_H$ and $R_L$ conditions. In the $R_L$ condition, the voltage's swing is decreased which accordingly minimizes the output power and reduces efficiency. For the high load condition $R_H$, the voltage's swing is slightly increased relative to $V_{dc}$ and that translates to a higher drain efficiency, however, the output power is reduced due to the significant reduction in the current swing.

## 2.5 Power Amplifiers Classes

Power amplifiers can be classified into two main groups termed as current mode operation and switched mode operation [19, 40]. In current mode operation, a PA is operated as a controlled-current-source. While in switched mode operation, the PA is operated in saturation; thus, the amplifier behaves herein as a switch.

### 2.5.1 Current Mode Operation

PA operated in current mode operation is as class A, AB, B, C and F[1]. There are basic assumptions in this mode [5]:

- The input signal drive is a pure sinusoidal signal
- The PA is an ideal controlled-current-source, i.e., the output signal linearly follows the input drive.
- The RF current is allowed to swing between zero and saturation, however, not allowed to saturate.
- the RF voltage is allowed to swing between zero and $2V_{dc}$

The portion that the RF cycle operates in the active region is defined as the conduction angle and PAs accordingly classified based on the conduction angle as class A, AB, B and C. A simplified single-ended topology circuit is considered for the analysis of these classes as shown in Fig. 2.2.

Ideal assumptions have been considered for the analysis [41]:

[1]Class F with the first two odd harmonics: fundamental and third harmonic

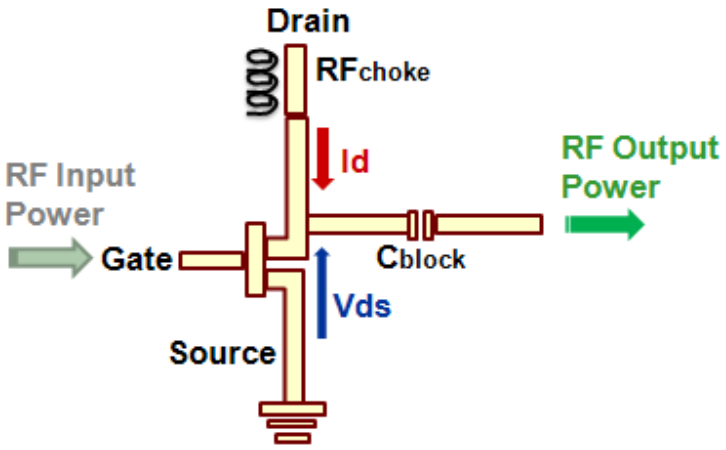



**Figure 2.2: Simplified single-ended PA circuit.**

- RF choke is ideal with no series resistance and its reactance at the operating frequency is infinite.
- RF choke allows DC current which is determined by the bias circuit.
- $C_{block}$ is a DC block capacitor and a short for AC signal.

#### 2.5.1.1 Class A

The transistor in class A is biased midway between the saturation and conduction pinch-off. Class A operates in the active region for the full input cycle, i.e., a $360^{\circ}$ conduction angle. The output waveform is a replica of the input waveform with a fixed gain and phase. [5]

The output current and voltage waveforms can be written as:

$$\mathrm{i}(\theta) = I_{dc} + I_1 \sin\theta \tag{2.8}$$

$$\mathrm{v}(\theta) = \mathrm{V_{dc}} - V_1 \sin\theta \tag{2.9}$$

where phase $\theta = \omega t$, $\omega$ is the angular frequency and $t$ is the unit time, $I_{dc} = \frac{I_{max}}{2}$ is the dc drain bias current, $I_1 = \frac{I_{max}}{2}$ is the fundamental component of the current waveform, $V_{dc}$ is the drain DC bias voltage, and $V_1 = V_{dc}$ is the fundamental component of the voltage waveform. The current and voltage waveforms are plotted in Fig. 2.3.

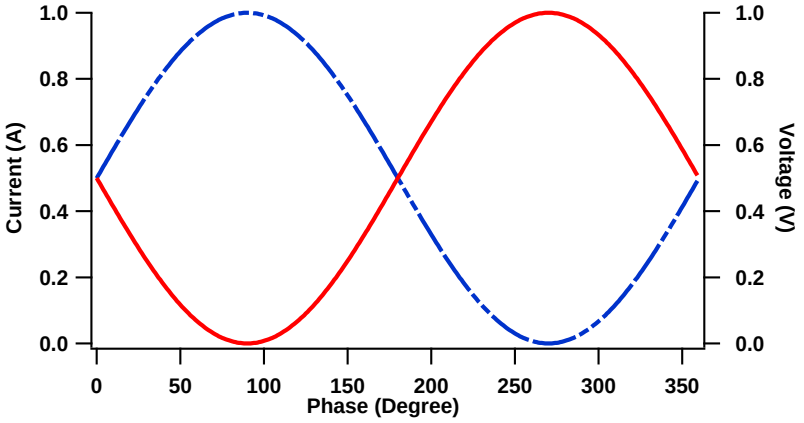



**Figure 2.3: Class A current (dashed line) and voltage (solid line) waveforms.**

The output power, DC power, drain efficiency and PUF are:

$$P_{out} = 0.5\, V_1\, I_1 = 0.5\, V_{dc}\, I_{dc} \tag{2.10}$$

$$P_{dc} = V_{dc}\, I_{dc} \tag{2.11}$$

$$\eta = \frac{P_{out}}{P_{dc}} = 50\,\% \tag{2.12}$$

$$PUF = 0\, dB \tag{2.13}$$

Class A has many advantages, above all it is inherently linear since no harmonics exists in the voltage and current signals. It has the highest gain since both positive and negative excursions drive the output power. In addition, it is a broadband class and that is due to

the absence of a highly reflective harmonic terminations. The only limiting factor is the $f_{max}$ of the transistor. However, drain efficiency at PEP is only 50% and that is the major drawback of this class. At lower back-off, drain efficiency is significantly affected compared to other classes and that is due to the fixed DC drain current. Therefore, class A is typically used in low power, high linearity, high gain and broadband applications.

#### 2.5.1.2 Class B

Class B is biased at pinch-off and conducts for only half of the input cycle i.e., conduction angle of $180^{\circ}$. The quiescent drain current is ideally zero. Class B can be used in a single ended or in push-pull topologies. The current waveform is a half sinusoidal signal and the voltage waveform is a purely sinusoidal signal. This requires the output network to short all even harmonics. The current and voltage waveforms are:

$$\mathrm{i}(\theta) = \mathrm{I_{max}}\left[\frac{1}{\pi} + \frac{\sin\theta}{2} + \sum_{\mathrm{n}=2,4,..}^{\infty} \frac{-2}{\pi\left[\mathrm{n}^2-1\right]}\cos\left(\mathrm{n}\theta\right)\right] \quad (2.14)$$

$$\mathrm{v}(\theta) = \mathrm{V_{dc}} - V_1 \sin\theta\,. \quad (2.15)$$

Current and voltage waveforms are shown in Fig. 2.4.

The performance of class B at PEP is:

$$P_{out} = 0.5\,V_1\,I_1 = 0.5\,V_{dc}\,\frac{I_{max}}{2} \quad (2.16)$$

$$P_{dc} = V_{dc}\,\frac{I_{max}}{\pi} \quad (2.17)$$

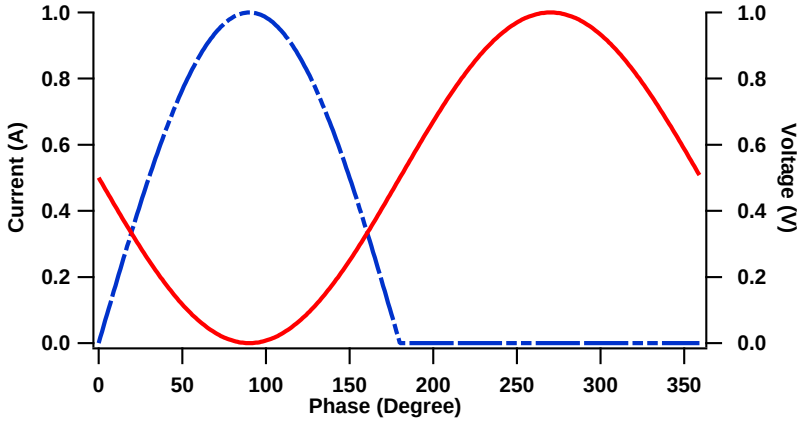



**Figure 2.4: Class B current (dashed line) and voltage (solid line) waveforms.**

$$\eta = \frac{P_{out}}{P_{dc}} = 78.5\,\% \tag{2.18}$$

$$PUF = 0\,dB \tag{2.19}$$

The drain efficiency is 78.5% at PEP. The DC drain current is proportional to the output RF power, hence, at low level signals the drain efficiency is significantly larger than that of class A. For instance, the average drain efficiency for a 10 dB PAPR is 5% and 28% for class A and class B respectively. The PUF is 0 dB, i.e., it provides the same power as class A.

Class B is considered to provide linear amplification since the amplitude of the drain current increases proportionally with a fixed half sinusoid signal to the amplitude of the input driver [15]. As biasing the transistor at pinch off provide higher efficiency than class A, however, the gain is reduce by 3 dB relative to class A. In class B, the amplitude driver needs to be twice that of class A so that the amplitude of the drain current can reach $I_{max}$ of the transistor.

Class B, as a single-ended topology, is required to terminate even harmonics into a short circuit and that minimize the operating bandwidth. A push-pull configuration is more complex, requires extra bias circuitry and uses lossy transformers but it offers broadband operation since even harmonics are canceled in this topology.

#### 2.5.1.3 Class C

Classical class C is biased in a portion less than the half of the RF cycle, i.e., less than $180^\circ$ but greater than $130^\circ$. Moving from class B to class C, the drain efficiency increases while linearity and gain are degraded. As the conduction angle decrease towards $0^\circ$, drain efficacy increases towards 100% while the output power decreases towards zero. Typically class C conduction angle is $150^\circ$ with an ideal efficiency of 85% for a compromise trade off between linearity, gain, output power and efficiency [42]. The output network is designed to pass the fundamental current and short all drain current harmonics to the ground so that the developed drain-source voltage is free of harmonics. Typical current and voltage waveforms of class C are shown in Fig. 2.5.

#### 2.5.1.4 Class F

Class F is evolved from class B where the voltage waveform is transformed into a square waveform [12, 43, 44, 45]. First introduced in the 1950s [46]; it is generally termed class F when only the third harmonic open termination is considered to maximally flatten the voltage waveform (Fig. 2.6) with drain efficiency 90.7% [19, 42].

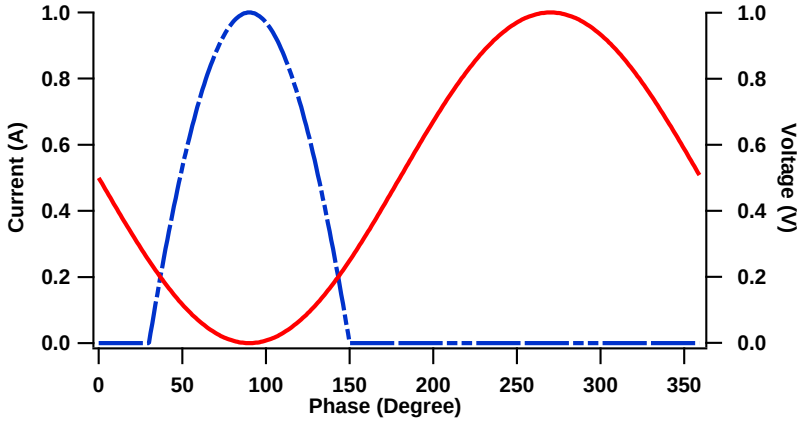



**Figure 2.5: Class C current (dashed line) and voltage (solid line) waveforms.**

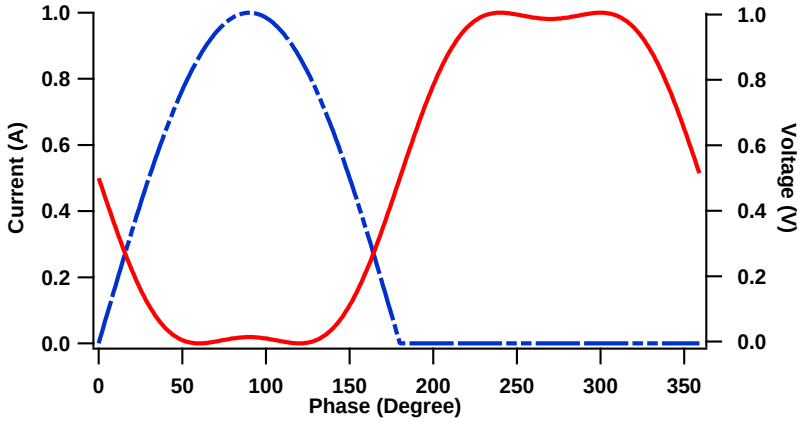



**Figure 2.6: Class F current (dashed line) and voltage (solid line) waveforms.**

Class F in principle is operated in a current mode operation [42], however, the generation mechanism of the clipped voltage waveform is not considered in the ideal class F operation. In practice, a portion of the RF cycle is driven into saturation to generate the required voltage waveform [19, 42, 43, 47]. The voltage waveform can be written as:

$$\mathrm{v}(\theta) = \mathrm{V_{dc}} - \mathrm{V_1}\sin(\theta) - \mathrm{V_3}\sin(3\theta) \tag{2.20}$$

where $V_3/V_1 = 1/6$ provides the maximum fundamental amplitude swing. The resulting drain efficiency is 90.7% and PUF is 0.6 dB.

#### 2.5.1.5 Class J

Class J is a derivative of class B providing the same output power and drain efficiency. The optimum fundamental and second harmonic impedances are:

$$Z_{f_0} = R_L + jR_L \tag{2.21}$$

$$Z_{2f_0} = 0 - j\frac{3\pi}{8}R_L. \tag{2.22}$$

The second harmonic load is capacitively terminated, while the fundamental load is required to provide a high reactive component (Fig. 2.7) to provide class B output power and drain efficiency.

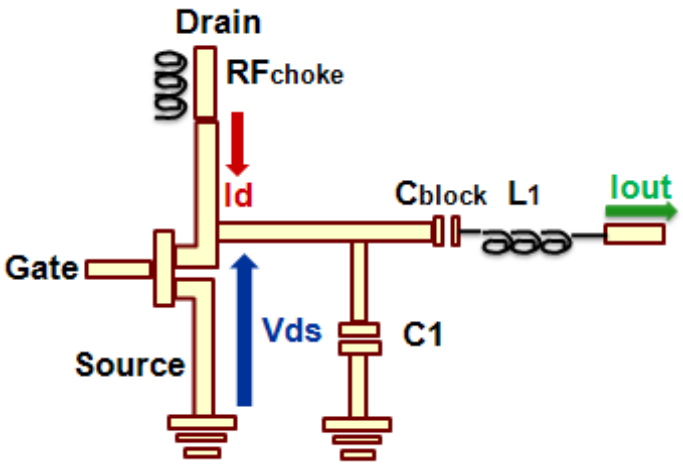



**Figure 2.7: Schematic of class J.**

This inductive fundamental load is the main difference between class B and class J [19, 48]. The main advantage of class J is that it

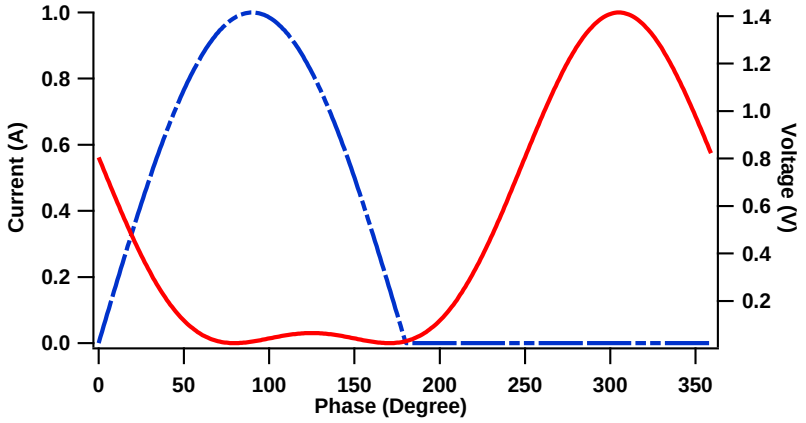



**Figure 2.8: Class J current (dashed line) and voltage (solid line) waveforms.**

requires a simple matching network, the second harmonic load termination can utilize the drain-to-source capacitance, with a simple inductive fundamental matching. Fig. 2.8 shows the current and voltage waveforms; one main drawback of class J is that it has a high even harmonic peaking in the voltage waveform.

### 2.5.2 Switched Mode Operation

Transistors in this mode are operated in saturation where the output network determines the voltage and current waveforms rather than the input drive. Switching mode amplifiers such as class D and class E amplifiers utilize the active device as a switch where either a voltage exists across the transistor or current exists passing through transistors's channel. As a result, since no overlap exists between current and voltage, and only the fundamental power reaches the load, the maximum efficiency reaches 100%. The ideal switching operation assumes zero on-resistance, infinite off-resistance and a zero switching time [13]. However, at microwave frequencies RF

power transistors cannot behave as a switch because the switching speed is slow. As a result, ideal class D operation is limited to lower frequency ranges. However, there are derivatives of the class E amplifier in which the slow switching can be allowed and used effectively at low microwave frequencies. [19]

## 2.6 Breaking 100% Barrier

The current waveform of class B is a half wave rectified sinusoidal signal which has a fundamental amplitude equal to half of the saturation current (i.e., $I_{max}/2$) while the DC component is only $I_{max}/\pi$. The key feature of the half rectified sinusoid is that over the same maximum current swing it provides for the same fundamental signal as the sinusoidal waveform but importantly it has a reduced $(2/\pi)$ DC component, hence providing for an increase of $(\pi/2)$ in drain efficiency. In addition, a short circuit at all higher harmonics is used to shape the voltage waveform to a simple sinusoid and therefore providing a maximum theoretical drain efficiency of 78.5%.

Considering class B current waveform with a half rectified sinusoidal voltage waveform would provide drain efficiency of $\pi^2/8 = 123\%$. However, the impedances required to generate those waveforms are negative at even harmonics and that means energy absorbtion which needs to be considered in the drain efficiency equation and that obviously will affect the total drain efficiency of the system. [19]

This leads to analysis and investigation on realizable waveforms

using waveform engineering. Basically the analysis starts from investigation of finding high efficient waveforms and then looking back on how those waveforms could be realized with passive networks. An investigation on these types of waveforms is in [19] where the analysis focused on the addition of a second harmonic voltage component and concludes that these kind of waveforms are unrealizable in practical PA design. The analysis shows that to obtain such a waveform, the phase of the second harmonic current component should be in quadrature phase with the second harmonic voltage. A simple $45^{\circ}$ phase shift between the fundamental current and voltage waveforms will achieve this condition, however, with a reduction in the output fundamental power and a power absorbtion at other even harmonic which is still theoretically unrealizable by passive networks.

## 2.7 Optimum Efficiency for Different Combinations of Harmonics

The aim is to obtain an optimum waveform that will improve drain efficiency by considering the following design options:

- To reduce the overlap between the voltage and current waveforms by deliberately enforcing those waveforms to have a faster switching time and as a result the overlap between waveforms will be minimum and power dissipated across the transistor will be reduced.
- To flatten the bottom of the voltage waveform and consequently

reducing power loss during on-state.

Snider [43] pioneered the work in the investigation of the effect of harmonic terminations and much research on harmonic termination strategies has been proposed in literature. Other authors have performed analysis on flattening the bottom of the voltage waveform [12, 19, 49]. Raab [45] came up with performance parameters to calculate the maximum efficiency and worked out waveform coefficients for odd and even harmonics.

Those performance parameters ($\gamma_V$ and $\gamma_I$) relate the dc component ($V_{\rm DD}$ and $I_{\rm dc}$) of the drain voltage and current to the amplitude of the fundamental frequency component ($V_1$ and $I_1$ ) as follows:

$$V_1 = \gamma_{V1} V_{\rm DD} \tag{2.23}$$

$$I_1 = \gamma_{I1} I_{\rm dc}. \tag{2.24}$$

Assuming a resistive load impedance at the fundamental frequency and an ideal FET (no on-state resistance, no distortion of the waveform). The dc power, output RF power and efficiency are:

$$P_o = \frac{V_1^2}{2R} = \frac{\gamma_{V1}^2 V_{DD}^2}{2R} \tag{2.25}$$

$$I_{dc} = \frac{I_1}{\gamma_{I1}} = \frac{V_1}{\gamma_{I1} R} = \frac{\gamma_{V1} V_{DD}}{\gamma_{I1} R} \tag{2.26}$$

$$\eta = \frac{P_o}{P_{dc}} = \frac{\gamma_{V1}\gamma_{I1}}{2}. \tag{2.27}$$

The waveform harmonic coefficients are calculated for maximum efficiency by adjusting the amplitude of harmonics to obtain a flat

waveform at the bottom of the voltage waveform. From [45] the second harmonic waveform coefficients for maximum efficiency are: $\gamma_{V1} = 1.4142, \gamma_{V2} = 0.354$, where $\gamma_{V1} = \frac{V_1}{V_{DD}}$ and $\gamma_{V2} = \frac{V_2}{V_1}$.

### 2.7.1 Performance Parameters

Now starting with a class B biasing condition and applying either odd or even waveform coefficients on the voltage waveform we have:

1. Odd harmonics case: provide square voltage waveforms and that is class F (considering first two odd harmonics) and class D (with infinite odd harmonic termination).

2. Even harmonics case: waveform peaking would create a half rectified voltage waveform.

Drain efficiency of odd and even harmonic peaking are shown in Fig. 2.9.

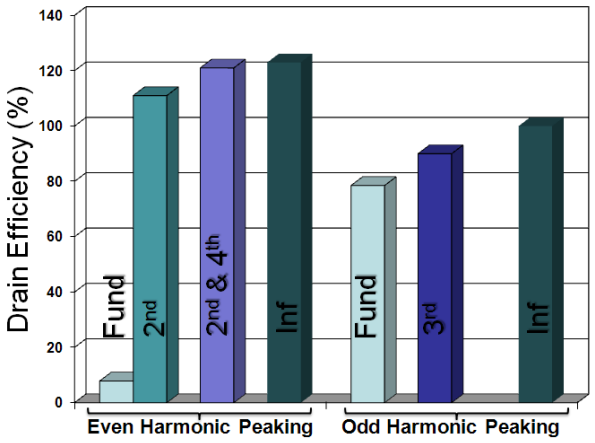



**Figure 2.9: Efficiency for even and odd harmonic peaking.**

As can be seen from Fig. 2.9 that odd harmonic peaking would provide class F and class D drain efficiencies. On the other hand,

even harmonic peaking could achieve a very high efficiency of $\pi^2/8$ = 123% when all even harmonics are properly terminated as discussed in Sec. 2.6. However, this drain efficiency shows that some power is not included in these equations which indicate that even harmonic peaking cannot be realized by passive networks. The reason is that the required impedances are negative which indicates an active realization is needed for such a system. In this case, the added power needs to be included in a new equation for the total system efficiency which we will be discussed in Sec. 2.9

From this graph, it can be seen that considering only the first second harmonic for even harmonic voltage peaking provide a significant drain efficiency of 111%. This high drain efficiency figure considering only second harmonic power absorbtion motivates to investigate a design where only one auxiliary PA can be used to generate the required power.

## 2.8 Operation Principle of Proposed Topology

As mentioned earlier, theoretical RFPA design has mainly constrained solutions via a focus on passive load-pull. The proposed power amplifier approach replaces the need for traditional passive band limiting harmonic terminations through active harmonic injection, to address the theoretical limitations on efficiency associated with passive harmonic injection. Active harmonic injection enables a new dimension to waveform shape the output voltage and current which has not yet been exploited in RFPA design. The initial investiga-

tion in Sec. 2.7.1 indicates potential advantages of such a mode of operation. A previously reported work on harmonic injection [50] at low frequency (HF band) showed high drain efficiency and demonstrated the principal idea in switched mode PA design, although it lacks analysis on the behavior of this mode of operation. Other works of second harmonic source injection at the input of the amplifier reported improvements in PA linearity. These works used a feedback technique based on feeding the intermodulation products back to the input of the PA, which showed significant reduction in the IMD. [51]

In the next section, second harmonic absorbtion by the transistor will be investigated and analyzed. The proposed system (Fig. 2.10) consists of two paths where the upper one generates the main fundamental RF signal and a lower path with a voltage source/ auxiliary PA to control the voltage/current waveforms of the main path. By injecting harmonics of the fundamental signal the voltage/current waveform can be shaped for better PA performance.

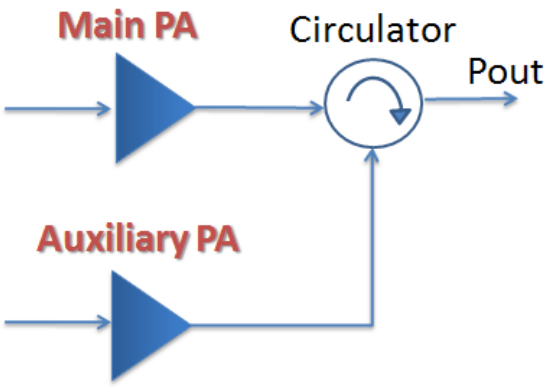



**Figure 2.10: Proposed PA structure.**

## 2.9 Theoretical Waveform Analysis

As a starting point, the current waveform is considered as a half-wave rectified sine wave that are utilized in class B. Now, considering only the first two harmonics of the voltage waveform, the voltage and current waveforms in the optimum case (Fig. 2.11) are given by the following equations [19, 45, 52]:

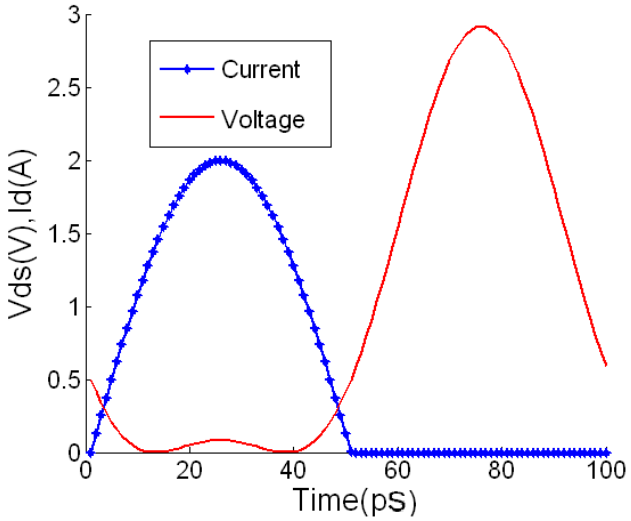



**Figure 2.11: Voltage and current waveforms for maximum efficiency condition.**

$$\mathrm{v}(\theta) = \mathrm{V_{dc}}\left[1 - \mathrm{x_1}\sin\theta - \mathrm{x_2}\cos(2\theta)\right] \tag{2.28}$$

$$\mathrm{i}(\theta) = \mathrm{I_{max}}\left[\frac{1}{\pi} + \frac{\sin\theta}{2} + \sum_{\mathrm{n}=2,4,..}^{\infty} \frac{-2}{\pi\left[\mathrm{n}^2 - 1\right]}\cos\left(\mathrm{n}\theta\right)\right] \tag{2.29}$$

where $\mathrm{V_{dc}}$ is drain DC bias voltage, $\mathrm{I_{max}}$ is the saturation current, $\mathrm{x_1} = \sqrt{2}$ and $\mathrm{x_2} = 0.5$ are the even harmonic coefficients for the maximum efficiency condition considering only fundamental and second harmonic components, phase $\theta = \omega\mathrm{t}$, $\omega$ is the angular fre-

quency and $t$ is the unit time. The magnitude of the fundamental voltage and current components respectively are: $\mathrm{V_1} = \sqrt{2}\mathrm{V_{dc}}$ and $\mathrm{I_1} = \mathrm{I_{max}}/2$. Thus, the required optimum fundamental load is given by;

$$\mathrm{R_f} = 2\sqrt{2}\mathrm{V_{dc}}/\mathrm{I_{max}}. \tag{2.30}$$

Analysis of these waveforms indicates the following DC power, output power and drain efficiency;

$$\mathrm{P_{dc1}} = \mathrm{V_{DC}I_{max}}/\pi = 2\mathrm{V_{DC}V_1}/\pi\mathrm{R_f} = 2\sqrt{2}\mathrm{V_{DC}^2}/\pi\mathrm{R_f} \tag{2.31}$$

where

$$\mathrm{V_1} = \mathrm{R_f I_1} = \mathrm{R_f I_{max}}/2 \tag{2.32}$$

$$\mathrm{P_{out}} = \mathrm{V_1^2}/2\mathrm{R_f} = \mathrm{V_{dc}^2}/\mathrm{R_f} \tag{2.33}$$

$$\eta_{\mathrm{Drain}} = \mathrm{P_{out}}/\mathrm{P_{dc}} = \pi/2\sqrt{2} = 111\%. \tag{2.34}$$

Obviously efficiency greater than 100% is not theoretically possible. Further analysis of the current and voltage waveforms indicates that the required load impedance at the second harmonic is negative and is given by;

$$\mathrm{R_{2f}} = -\frac{3\pi}{4}\mathrm{V_{dc}}/\mathrm{I_{max}} = -R_f \cdot \frac{3\pi}{8\sqrt{2}}. \tag{2.35}$$

While this is not possible with passive networks, it is achievable with active second harmonic injection. The required second harmonic power injected into the system is:

$$\mathrm{P_{rf2}} = \frac{\mathrm{V_2^2}}{2\mathrm{R_{2f}}} = \frac{1}{6\pi}\mathrm{V_{dc}} \cdot \mathrm{I_{max}} \tag{2.36}$$

Where $\mathrm{V}_2$ is the magnitude of the second harmonic voltage component. However, in this case the efficiency calculation must be modified to include the addition of the harmonic energy and TDE (Eq. 2.2) of the IPA is:

$$\eta_{TDE} = \mathrm{P_{out}}/\mathrm{P_{dc}} = \mathrm{P_{out}}/(\mathrm{P_{dc1}} + (\mathrm{P_{rf2}}/\eta_2)). \tag{2.37}$$

where $\eta_2$ are the drain efficiency of the generated harmonic power. $\mathrm{P_{dc1}}$ is the DC power supplied to the IPA structure for the generation of the RF fundamental power. The modified equation increases the amount of DC power to generate the required second harmonic power.

Figure 2.12 shows the proposed structure highlighting the impedances that are required to be presented to both the main and auxiliary devices.

The modified drain efficiency calculation shows that the efficiency of the second harmonic PA is important for achieving high total drain efficiency, which is shown in Fig. 2.13. As it can be seen, the resulting IPA drain efficiency is a nonlinear function of the efficiency of the second harmonic power and starts increasing significantly where only a 40% drain efficiency of the second harmonic power will provide class B drain efficiency.

Table 2.1 summarizes the predicted theoretical performance for the two cases when the efficiency of the second harmonic power is ideal 100% $(Ideal\ IPA)$ and a very modest 40% $(Modest\ IPA)$. The fundamental load ($\mathrm{R_{f0}}$), DC power accounting for total energy

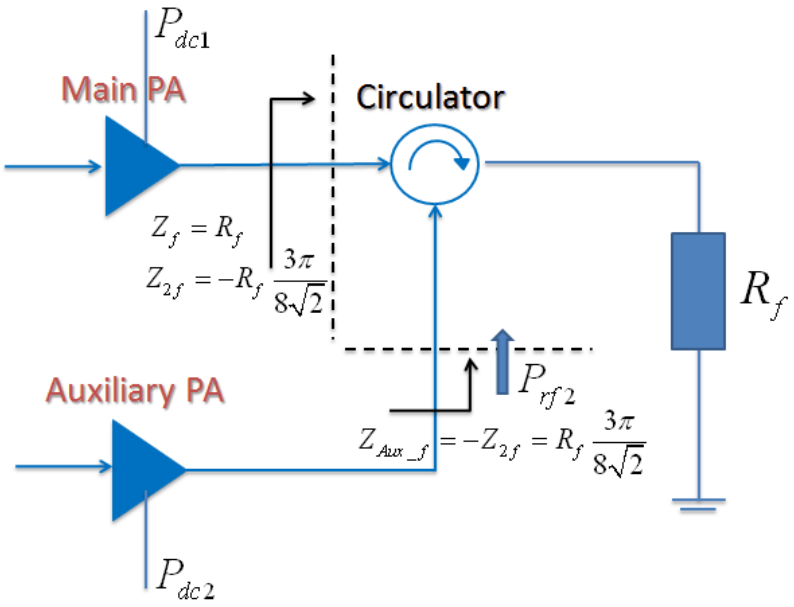



**Figure 2.12: Proposed IPA structure showing the required output impedance for both the main and auxiliary devices.**

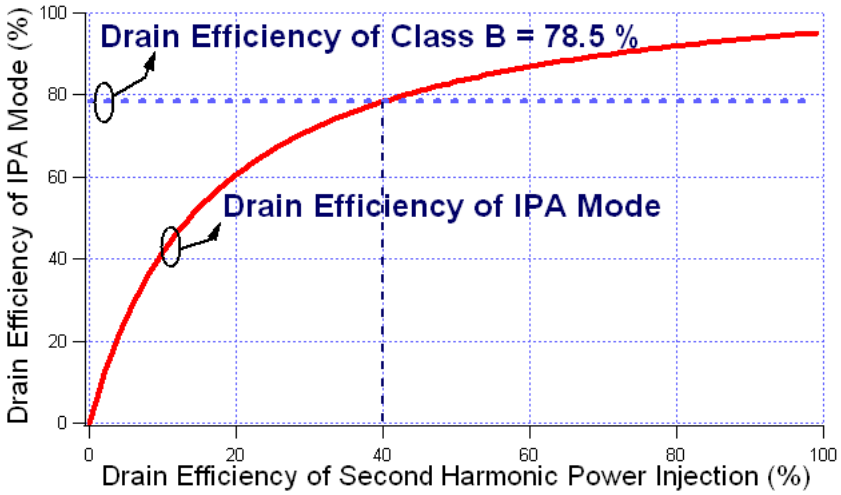



**Figure 2.13: The effect of the efficiency of the second harmonic injection power on the drain efficiency of IPA mode.**

into the system $(P_{dc})$, fundamental RF power $(P_{out})$, power utilization factor $(PUF)$, peaking value of voltage waveform $(V_{\max})$ and

total drain efficiency ($\eta_{TDE}$) shown in Table 2.1 are calculated assuming a normalized $\mathrm{V_{dc}}$= 1 V and saturation current $\mathrm{I_{max}}$ = 2 A.

**Table 2.1: PERFORMANCE PARAMETERS.**

| | $ClassB$ | $Ideal\ IPA$ | $Modest\ IPA$ |
|---|---|---|---|
| $R_{f0}(\Omega)$ | 1 | $\sqrt{2}$ | $\sqrt{2}$ |
| $P_{dc}(W)$ | $2/\pi$ | $\frac{2}{\pi}+\frac{2}{6\pi}$ | $\frac{2}{\pi}+\frac{4.96}{6\pi}$ |
| $P_{out}(W)$ | $1/2$ | $1/\sqrt{2}$ | $1/\sqrt{2}$ |
| $PUF(dB)$ | 0 | 1.5 | 1.5 |
| $V_{max}(V)$ | 2 | 2.9 | 2.9 |
| $\eta_{TDE}(\%)$ | 78.5 | 95.2 | 78.5 |

Table 2.1 reveals the performance of this new mode where the fundamental load and RF power are larger than class B by a factor of $\sqrt{2}$. Thus, with a very efficient second harmonic PA, the IPA mode can enable the design of very efficient PAs approaching 95.2%, a solution more applicable to narrowband design. Alternatively, even with modest second harmonic PA efficiency, the IPA mode has the potential to provide for efficiencies over 78.5%, a solution that is applicable to wideband PAs. One implication of the IPA mode is that it has a high voltage peaking effect. This can be seen also in other modes as in class E and class J; however, new emerging semiconductor technologies such GaN HEMT (High Electron Mobility Transistor) that have high voltage breakdown can be a preferable choice for such modes of operation.

The theoretical analysis has considered only the first two harmonics (fundamental and second) as the second harmonic is the most significant harmonic component and also because of the associated practical challenges of harmonic generation.

### 2.9.1 Output Power Analysis

Looking at Table 2.1, it can be seen that IPA total drain efficiency remains high despite the assumed inefficiency within the harmonic generation process as in the $Modest\ IPA$ case. Also, it shows that the output power has been increased by a factor of $\sqrt{2}$ from $class\ B$ to $Ideal\ IPA$ case while the DC power has increased by only a factor of $(1/6)$. Further analysis was carried out by comparing directly $class\ B$ performance with the one of the IPA to understand the occurring power conversion between the fundamental RF power on one hand and the DC and harmonic power levels on the other hand. The $class\ B$ output power, DC power and dissipated power are shown below:

$$\mathrm{P_{dc\_B}} = \mathrm{V_{dc}} \cdot \frac{\mathrm{I_{max}}}{\pi} \tag{2.38}$$

$$\mathrm{P_{rf\_B}} = 0.5 \cdot \mathrm{V_{dc}} \cdot \frac{\mathrm{I_{max}}}{2} = \frac{\pi}{4} \cdot \mathrm{P_{dc\_B}} \tag{2.39}$$

$$\mathrm{P_{diss\_B}} = \mathrm{P_{dc\_B}} - \mathrm{P_{rf\_B}} = \left(1 - \frac{\pi}{4}\right) \mathrm{P_{dc\_B}} \tag{2.40}$$

For comparison, the IPA mode's fundamental load $\mathrm{R_f}$, second harmonic load $\mathrm{R_{2f}}$, DC power $\mathrm{P_{dc\_I}}$, output power $\mathrm{P_{rf\_I}}$, DC power of injected harmonic $\mathrm{P_{dc_{2nd}}}$ and dissipated power $\mathrm{P_{diss\_I}}$ can be written as:

$$\mathrm{R_f} = 2 \cdot \mathrm{x_1} \cdot \mathrm{V_{dc}}/\mathrm{I_{max}} \tag{2.41}$$

$$\mathrm{R_{2f}} = -\frac{3\pi}{2} \cdot \mathrm{x_2} \cdot \mathrm{V_{dc}}/\mathrm{I_{max}} \tag{2.42}$$

$$\mathrm{P_{dc\_I}} = \mathrm{V_{dc}} \cdot \frac{\mathrm{I_{max}}}{\pi} \tag{2.43}$$

$$\begin{aligned} \mathrm{P_{rf\_I}} &= \frac{\mathrm{V_1^2}}{2\mathrm{R_f}} = \frac{(\mathrm{x1}\cdot \mathrm{V_{dc}})^2}{2\mathrm{R_f}} \\ &= \frac{\mathrm{V_{dc}}}{2}\cdot\frac{\mathrm{I_{max}}}{2}\cdot \mathrm{x_1} = \mathrm{P_{rf\_B}}\cdot \mathrm{x_1} \end{aligned} \tag{2.44}$$

Assuming 100% conversion efficiency the DC power that is required to generate the second harmonic signal is:

$$\begin{aligned} \mathrm{P_{dc_{2nd}}} &= \frac{\mathrm{V_2^2}}{2\mathrm{R_{2f}}} = \frac{(\mathrm{x_2}\cdot \mathrm{V_{dc}})^2}{2\mathrm{R_{2f}}} \\ &= \mathrm{V_{dc}}\cdot\frac{\mathrm{I_{max}}}{3\pi}\cdot \mathrm{x_2} = \mathrm{P_{dc\_B}}\cdot\frac{\mathrm{x_2}}{3} \end{aligned} \tag{2.45}$$

This is also the factor $(1/6)$ by which the DC of the IPA is increased due to the need for generating the second harmonic power. The above equation hence stipulates that the $2^{nd}$ harmonic power is generated externally and then injected into the transistor.

From the above equations it can be seen that the IPA output power is larger when compared to class B:

$$\Delta \mathrm{P_{rf}} = \mathrm{P_{rf\_I}} - \mathrm{P_{rf\_B}} = \mathrm{P_{rf\_B}}(\mathrm{x_1} - 1) \tag{2.46}$$

with the dissipated power $\mathrm{P_{diss\_I}}$ within the IPA being

$$\begin{aligned} \mathrm{P_{diss\_I}} &= \mathrm{P_{dc\_I}} + \mathrm{P_{dc_{2nd}}} - \mathrm{P_{rf\_I}} \\ &= \mathrm{P_{dc\_B}}\left(1 + \frac{\mathrm{x_2}}{3} - \frac{\pi\cdot \mathrm{x_1}}{4}\right) \end{aligned} \tag{2.47}$$

As a result, the dissipated power has been decreased by

$$\Delta \mathrm{P_{diss}} = \mathrm{P_{diss\_B}} - \mathrm{P_{diss\_I}}$$

$$
\begin{aligned}
&= \mathrm{P_{dc\_B}}\left(1-\frac{\pi}{4}-\left(1+\frac{\mathrm{x_2}}{3}-\frac{\pi\cdot\mathrm{x_1}}{4}\right)\right)\\
&= \mathrm{P_{dc\_B}}\left(\frac{\pi}{4}\left(\mathrm{x_1}-1\right)-\frac{\mathrm{x_2}}{3}\right)\\
&= \mathrm{P_{rf\_B}}\left(\mathrm{x_1}-1\right)-\mathrm{P_{dc\_B}}\cdot\frac{\mathrm{x_2}}{3}\\
&= \Delta\mathrm{P_{rf}}-\mathrm{P_{dc_{2nd}}}.
\end{aligned}
\tag{2.48}
$$

with the reduction of the dissipated power being directly proportional to the injected second harmonic power. The above equation can be also rearranged to

$$\Delta\mathrm{P_{rf}} = \Delta\mathrm{P_{diss}}+\mathrm{P_{dc_{2nd}}} \tag{2.49}$$

Thus, the increase of the fundamental output power is actually a function of the injected second harmonic power and the efficient utilization of DC power supplied to the transistor. This can be also seen when looking at the ideal RF load lines, which are shown in Fig. 2.14. As it can be seen the dissipated power of class B that is represented by the shaded area has been greatly reduced by the IPA mode through the use of only the $2^{nd}$ harmonic injection. In other words, the transistor is absorbing the second harmonic power and that allows the RF voltage swing developed across it to be increased which translates into an increase in the fundamental power.

Figure 2.15 shows a comparison between class B and IPA mode showing the DC power, dissipated power and output RF power. The injected second harmonic power in IPA mode allows an efficient utilization of the supplied DC power resulting in a significant reduction in the dissipated power in comparison to class B. Although the es-

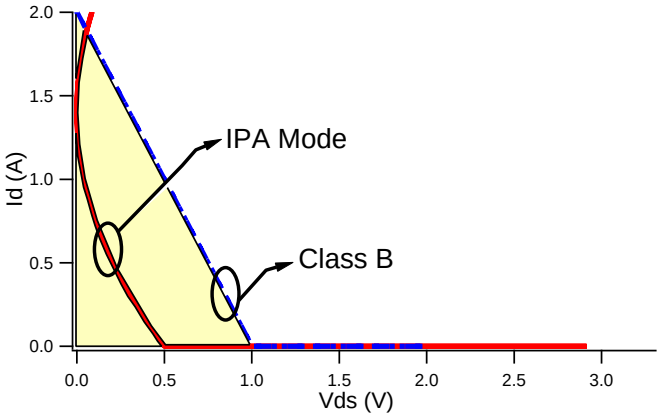
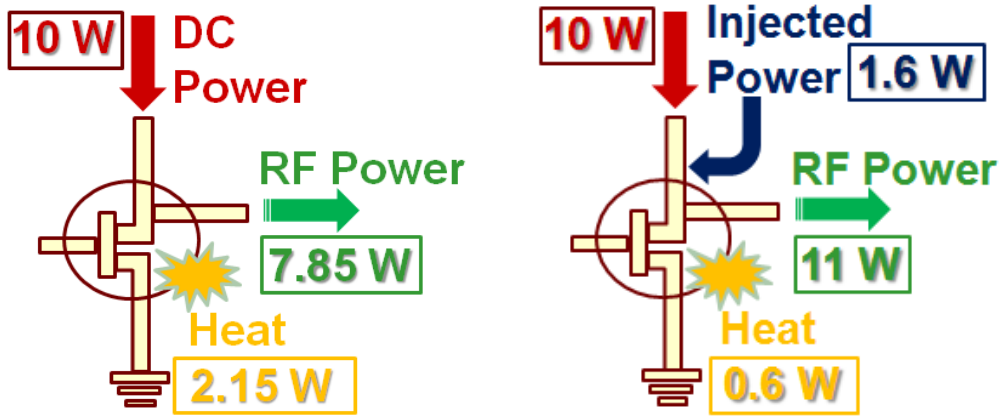



**Figure 2.14: RF load line.**

sential injected power is a second harmonic power but this injection allows an increase in the fundamental voltage component as been described previously resulting in an increase in the fundamental power which translates into an increase in the drain efficiency.




(a) Class B (b) IPA mode

**Figure 2.15: Comparison between Class B and IPA mode in a single-ended transistor showing DC power, dissipated power and output RF power.**

### 2.9.2 Drain Voltage Rail Condition

The IPA mode introduced also shows a high peaking effect on the voltage waveforms by a factor of $\sqrt{2}$ when compared to class B amplifier. Hence, a transistor technology is required with a high breakdown voltage when the same drain voltage rail (supply) is kept. This fits rather well with the increasing popularity of GaN technology with breakdown voltages significantly above 100 V thus allowing for a better utilization of its voltage range when employing common supply voltage values. The efficiency and output power values at PEP are shown in Table 2.1.

Alternatively, if the high peaking effect is not preferable and the drain rail voltage is a design parameter, it can be scaled down by a factor of $\sqrt{2}$ providing the same output power and maximum voltage swing as in class B. This can be beneficial for low power applications where the requirement is to reduce the DC power drawn from the batteries, as is the case in portable devices.

### 2.9.3 Second Harmonic Injection Analysis

#### 2.9.3.1 Sensitivity Analysis of the Drain Efficiency as a Function of the Magnitude and Phase of the Second Harmonic Voltage

The sensitivity of the drain efficiency of IPA mode as a function of the magnitude and phase of the second harmonic voltage needs to be studied due to its potential impact on design implementation. For this purpose, the magnitude and phase of the second harmonic voltage component has been varied where the magnitude and phase

of the fundamental has been fixed at the optimum condition as in Eq. 2.28 and 2.29, the sensitivity analysis is shown in Fig. 2.16 and Fig. 2.17.

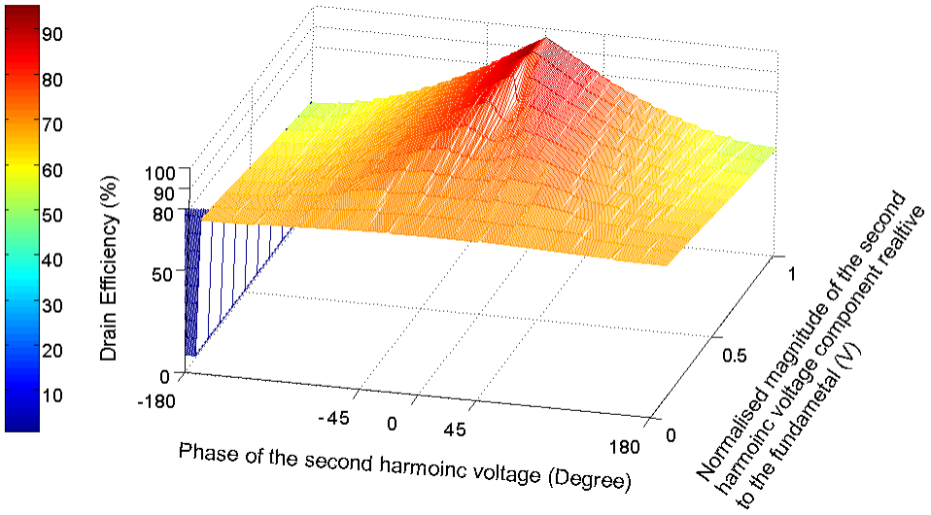



**Figure 2.16: Sensitivity analysis of the magnitude and phase of the second harmonic voltage component.**

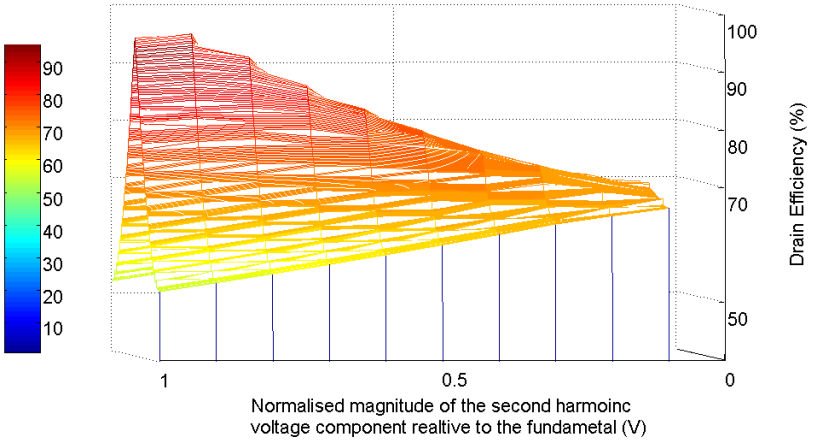



**Figure 2.17: Sensitivity analysis of the magnitude and phase of the second harmonic voltage component - cross section view.**

The graphs show that the magnitude and phase are not required

to be maintained at the optimum conditions. It can be seen that a drain efficiency above 79% can be maintained over a 90 degree range of the second harmonic voltage signal. The relaxed requirement for the second harmonic injection increases the chances of a successful first-pass PA design thus allowing for a cost-efficient design implementation and also minimizes the need for a dedicated phase control arrangement. This is also the case in broadband RFPA design which can take advantage of this flexibility where bandwidth-efficiency trade-off is a common practice.

#### 2.9.3.2 Optimum Second Harmonic Injection Considering Knee Voltage Effect

To consider the impact of the knee effect within the output I-V characteristic of a device, a knee voltage of 9 % of the DC supply $\mathrm{V_{dc}}$ is assumed that is shown in Fig. 2.18 along with the RF load-lines of class B and IPA mode.

It is apparent from Fig. 2.18 that the IPA RF load line (red circled line) is less limited by the knee voltage value at the maximum current swing as the momentary slope of the IPA load line advantageously aligns better with the knee region. The minimum voltage point of the IPA RF load line can be decreased by reducing the second harmonic voltage component and thus reducing the ripple within the composite waveform. The magnitude of the ripple is calculated by applying Eq. 2.28 at $\theta = \frac{\pi}{2}$ where the maximum value of

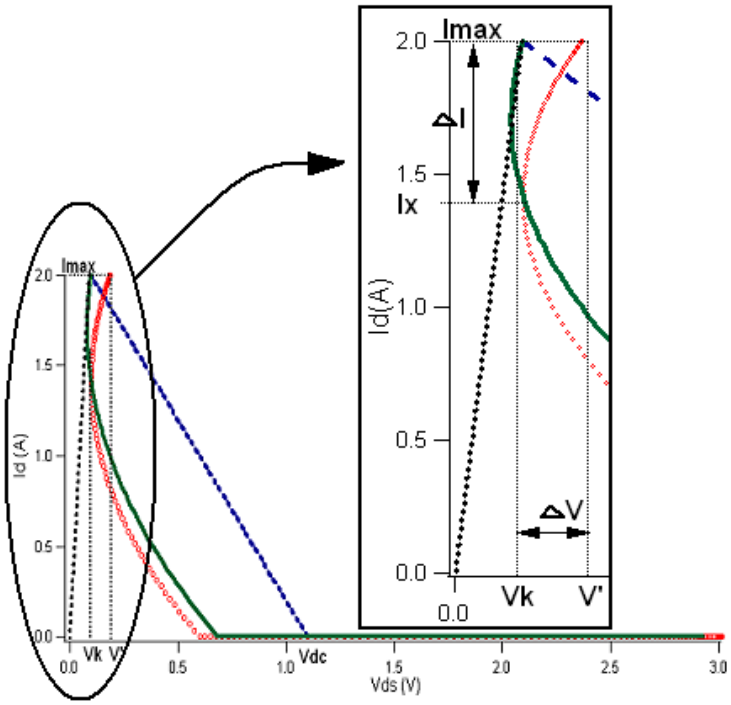



**Figure 2.18: More realistic knee effect, class B (blue dotted line), IPA mode (red circled line), optimized IPA (green solid line).**

the ripple exists:

$$\mathrm{Vds}\left(\frac{\pi}{2}\right) = \mathrm{V_{dc}}\left[1 - \mathrm{x_1} + \mathrm{x_2}\right] = 0.086 \cdot \mathrm{V_{dc}}. \tag{2.50}$$

With $\mathrm{x_1} = \sqrt{2}$ and $\mathrm{x_2} = 0.5$, as the first and second harmonic coefficients. Therefore, the second harmonic component will be reduced by this amount of ripple $(0.086 \cdot \mathrm{V_{dc}})$ indicated in Fig. 2.18 by $dV$:

$$\mathrm{V_2} = (0.5 - 0.086)\mathrm{V_{dc}} = 0.414 \cdot \mathrm{V_{dc}}. \tag{2.51}$$

However, in order to assure that no current clipping occurred, the slope of the ripple of the IPA RF load line $(\mathrm{m_{ripple}})$ is required to be

larger than the slope of the knee effect ($\mathrm{m_{knee}}$):

$$\mathrm{m_{ripple}} > \mathrm{m_{knee}}. \tag{2.52}$$

Assuming a straight line of the slope for a more simplified analysis, $\mathrm{m_{ripple}} = \Delta\mathrm{I}/\Delta\mathrm{V}$ and $\mathrm{m_{knee}} = \mathrm{I_{max}}/\mathrm{V_k}$ . The ripple of the RF load line is shown below:

$$\begin{aligned} \mathrm{m_{ripple}} &= \Delta\mathrm{I}/\Delta\mathrm{V} = \frac{\mathrm{I_{max}} - \mathrm{I_x}}{\mathrm{V'} - \mathrm{V_k}} \\ &= \left(\mathrm{I_{max}} - \mathrm{I_x}\right) / \left(\mathrm{V_{dc}} \cdot \delta\right). \end{aligned} \tag{2.53}$$

Where $\delta = (1 - x_1 + x_2)$.

$$\begin{aligned} \mathrm{m_{ripple}} &= \mathrm{I_{max}}\left(1 - \varepsilon\right) / \left(\mathrm{V_{dc}} \cdot \delta\right) \\ &= 2\left(1 - \varepsilon\right) / \left(\mathrm{R_L} \cdot \delta\right). \end{aligned} \tag{2.54}$$

Where $\varepsilon = I_x/I_{max}$ and $R_L = 2V_{dc}/I_{max}$.

Equation 2.54 shows that as $R_L$ gets larger, the ripple in the voltage waveforms increases leading to a reduction of the resulting slope. Therefore, reducing the second harmonic component will be more advantageous in high load conditions than lower load conditions. Since in lower load condition the slope of the ripple ($m_{ripple}$) increases, hence, will be more limited by the slope of the knee effect and accordingly will not get full advantage of the knee region. This also suggests that high power applications with high rail voltage can benefit more from the knee effect shape. The voltage waveform for the reduced second harmonic voltage component is shown in Fig.

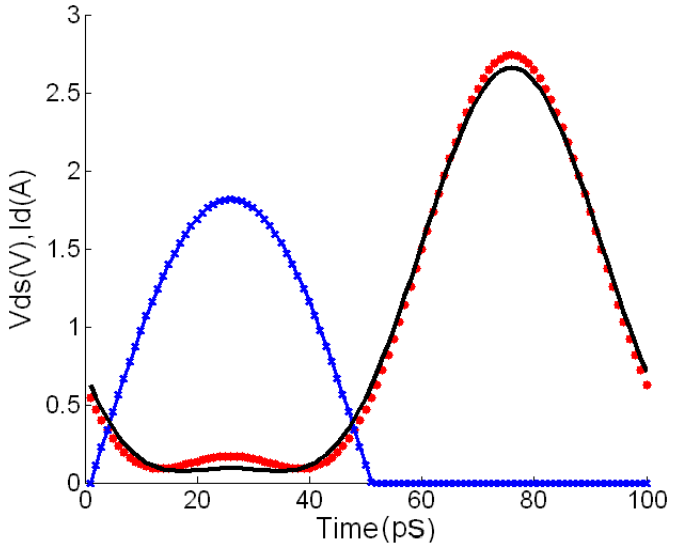



**Figure 2.19: Voltage and current waveforms for IPA (dotted red line) and optimized IPA mode (black solid line).**

2.19 while the corresponding RF load line is shown in Fig. 2.18 and the magnitude of the fundamental and second harmonic voltages are shown in Table 2.2.

Considering the knee effect on class B, IPA mode and optimized IPA mode the drain efficiency, $PUF$ and the required DC power for the injected second harmonic power (Eq. 2.45) relative to fundamental DC power (Eq. 2.43) are tabulated in Table 2.2. The knee effect has clearly affected the output power and drain efficiency of class B and IPA mode as shown in Table 2.2. As can be seen PUF of both class B and the IPA mode has dropped by 0.83 dB. This results in a PUF for the IPA mode of 0.68 dB. Furthermore, the drain efficiency in the Optimized IPA mode has increased by 2% due to the reduction of the 2nd harmonic power.

**Table 2.2: PERFORMANCE PARAMETERS FOR A MORE REALISTIC KNEE EFFECT.**

| | $V_1$ (V) | $V_2$ (V) | $\eta_{Drain}$ (%) | $PUF$ (dB) | Percent of DC Power of $2^{nd}$ harmonic to fundamental (%) |
|---|---|---|---|---|---|
| $Class\ B$ | 1 | 0 | 71.4 | -0.83 | 0 |
| $IPA$ | $\sqrt{2}$ | 0.5 | 87.7 | 0.68 | 0.15 |
| $OptimizedIPA$ | $\sqrt{2}$ | 0.414 | 89.7 | 0.68 | 0.12 |

This analysis demonstrates the potential of reducing the second harmonic injection to improve the IPA performance in terms of efficiency without any reduction of output power. The required second harmonic power decreased up to 12% of the main DC power and this also reduces the dependency on the efficiency of the second harmonic power.

## 2.10 Summary

In this chapter, we have examined the essential background for conventional high efficiency PA classes operating as current source and switched modes. After presenting the essential background for PAs operation, a new mode of operation that does not rely on passive termination but active harmonic injection has been introduced. This new dimension in PA design termed IPA has been studied, analyzed and compared to conventional PA classes. The potential advantages of such mode has been presented along with the performance parameters that defines the second harmonic load power injection.

The injection mode advantages includes a highly linear efficiency mode where the waveforms can be realizable without relying on

compression mechanisms. This linear efficiency has been achieved by the efficient utilization of the device by presenting a negative impedance essential for a high efficient voltage waveform. The requirement for this mode is an additional auxiliary PA. Also, this mode as in class E and class J has a high voltage peaking. However, new FET technologies as in GaN HEMT can be utilized to support the high voltage operation.

In addition, a sensitivity analysis has been carried out on the required injected second harmonic signal relative to the fundamental signal. The sensitivity analysis of the injected second harmonic phase shows that a good PA performance can be achieved in a phase range of $90^{\circ}$. This shows that wideband PA application can take advantage of this phase tolerance. This potential advantage will be investigated for a design of a prototype broadband PA in the subsequent chapters.

# *Chapter 3*

# Injection Power Amplifier Mode Validation

## 3.1 Introduction

The introduced IPA mode detailed in **Chapter 2** is based so far on only theoretical analysis. To verify the new mode of operation, a transistor set to operate in a real condition will be tested. The performance of the real PA will be then compared to the theoretical part to verify that a transistor can support such a mode of operation. Since this mode cannot be achieved by only a passive measurement system, an active load-pull measurement system developed by Cardiff University will be used.

This active load-pull system has the ability not only to characterize PAs working in real conditions but also to capture the terminal voltage and current waveforms; thus allowing a link direct to the theory. Also active load-pull measurement system places reflection coefficient on the Device Under Test (DUT) port at any spot on the Smith chart including reflection coefficients greater than unity. This is an important aspect of the measurement systems since the active injection mode can only be verified by an active measurement sys-

tem. Its ability to capture the incident and reflected waves allows the measurement and calculation of the injected RF second harmonic power.

In this chapter, the essential background on transmission line theory, linear and nonlinear characterization will be briefly described. Next, an overview of the active load-pull measurement system developed by Cardiff University will be introduced. Then, validation measurements of the IPA mode using the active load-pull measurement system will be presented. Following the validation measurement, the theoretical part and measurement results will be compared; the captured waveforms will also be compared to the ideal IPA waveforms. Finally, a summary of this chapter will be presented.

## 3.2 Transmission Line Background

The current, voltage and power transmitted from a source impedance ($Z_S$) to be delivered to a load ($Z_L$) can be represented by travelling waves across a transmission line (Fig. 3.1) with a characteristic impedance ($Z_0$). Travelling waves are either incident waves travelling in a positive direction (from the source to the load) or a reflected wave travelling in the negative direction (from load back to the source). The reflected waves are a function of the quality of the matching between the source and load. If the load and source are perfectly matched then the reflected travelling wave does not exist. [53, 54]

The reflection coefficient ($\Gamma$) is the ratio between the reflected

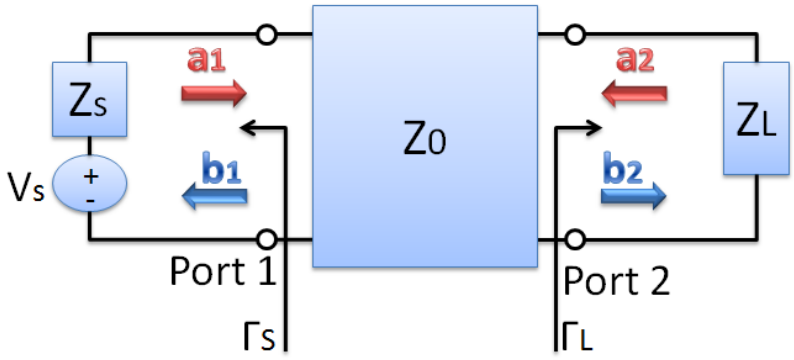



**Figure 3.1: Transmission line.**

and incident waves and that shows the quality of match between a source and a load.

$$\Gamma = \frac{V_{refelected}}{V_{incedent}} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{3.1}$$

In addition, the reflection coefficient can also be expressed in dB and termed return loss ($L_{loss}$) [5, 55]:

$$L_{loss} = -20log(\Gamma) \tag{3.2}$$

## 3.3 Linear Characterization Systems

The most widely used technique for characterizing RF components and networks are based on S-parameters (Scattering Parameters). This provides a fast and more accurate approach for network characterization at high frequency more than any other kinds of parameters. For instance, for other measurement parameters such y-parameters, the device terminals (ports) are required to be shorted or opened. This can be measured at low frequency but at high frequency this is

hard to be measured. This is due to the fact that at high frequency, the lead inductance and capacitance makes it hard to obtain an open or short at the device terminals. Typically tuning stubs are required which are also adjusted at each frequency measurement to obtain a short or open measurement which is hard and tedious. In addition, it is imposable to measure active devices such as transistors in a highly reflective termination; a short or open could cause oscillation or damage to the DUT.

S-parameter technique is measured where the DUT ports are terminated at the characteristic impedance of the measuring system and usually at a $50\,\Omega$ load and source impedance. This technique measures the traveling incident and reflected waves at the network ports instead of direct measure of terminal voltage and currents. The incident $a_i$ and reflected $b_i$ waves at the $i^{th}$ port are complex normalized voltage waves. These incident and reflected waves are defined in terms of the terminal voltage $V_i$, terminal current $I_i$, and arbitrary reference impedance $Z_i$ where an asterisk denotes the complex conjugate [55, 56]:

$$a_i = \frac{\text{voltage wave incident on the i}^{\text{th}}\text{ port}}{\sqrt{Z_i}} = \frac{Vi + Z_i I_i}{2\sqrt{Z_i}} \quad (3.3)$$

$$b_i = \frac{\text{voltage wave reflected on the i}^{\text{th}}\text{ port}}{\sqrt{Z_i}} = \frac{Vi - Z_i^* I_i}{2\sqrt{Z_i}} \quad (3.4)$$

For a two port network, S-parameters $S_{11}, S_{12}, S_{21}, S_{22}$ are defined by:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} = \text{Input reflection coefficient} \quad (3.5)$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} = \text{Output reflection coefficient} \quad (3.6)$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} = \text{Forward transmission coefficient} \quad (3.7)$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} = \text{Reverse transmission coefficient} \quad (3.8)$$

One key advantage of S-parameters is that they can be converted directly into impedances and power; for instance, $S_{11}$ can be written as:

$$S_{11} = \frac{b_1}{a_1} = \frac{Z_1 - Z_0}{Z_1 + Z_0} \quad (3.9)$$

where $Z_1$ is the input impedance at port 1. While $S_{21}$ can be expressed as:

$$|S_{21}|^2 = \text{Transducer power gain with } \mathrm{Z_0} \text{ load and source.}$$

Also, simple relationships relate travelling waves to power waves; $a_i$ and $b_i$ can be expressed as:

$$|a_i|^2 = \text{Power incident on the } \mathrm{i^{th}} \text{ port}$$
$$|b_i|^2 = \text{Power reflected from the } \mathrm{i^{th}} \text{ port}$$

Those expressions can be used in signal flow graph to calculate performance parameters such as power and gain of a connected networks [57]. In a two port signal flow graph, the gain (as in S21) and the port mismatch loss (as in S11) can be combined for a simple power calculation as shown in Fig. 3.2:

For instance, $b_1$ can be calculated from the signal flow graph as a function of the incident wave $a_1$ and the load matching quality $\Gamma_L$.

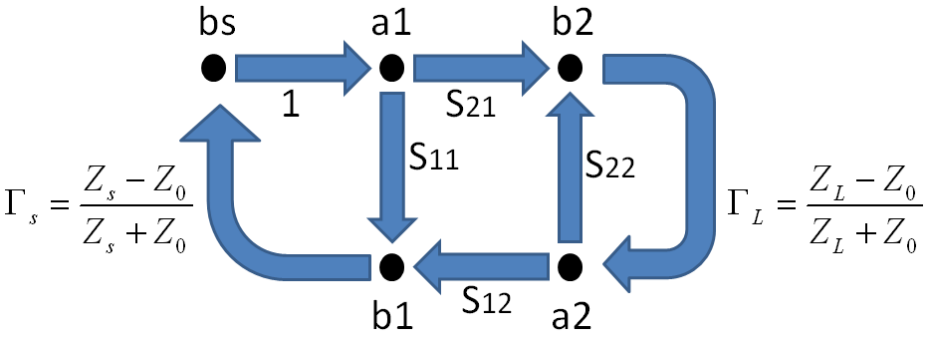



**Figure 3.2: Signal flow graph.**

This can be expressed as:

$$b_1 = a_1 S_{11} + a_2 S_{12} = a_1 S_{11} + b_2 \Gamma_L S_{12} \tag{3.10}$$

If the load is perfectly matched (i.e., $\Gamma_L = 0$) then $b_1$ becomes:

$$b_1 = a_1 S_{11} \tag{3.11}$$

This flow graph technique will be helpful in the calculation of the second harmonic power injected into the system in the subsequent section.

## 3.4 Non-linear Characterization Systems Capable of Waveform Engineering

Standard measurement systems are based on frequency domain systems such as small signal VNAs where S-parameters are measured. In these systems, the DUT is characterized by the magnitude and phase of a small signal and limited to its linear region. Active de-

vices like PAs are typically characterized using load-pull measurement systems, where the captured data and performance of the PA are mapped onto a smith chart, thus, a trade-off design can be established.

However, linear measurements lacks the critical information required to analyse the nonlinearity characteristic exhibited by most RF components. For example, a PA is designed and optimized by understanding the nonlinear behavior of the PA under test. In addition, the key standard requirements for PAs such as the level of harmonic distortion, gain compression performance and intermodulation distortion caused by multi-tone stimuli cannot be characterized by small signal VNAs.

A nonlinear scalar characterization that measures the magnitude transfer characteristics provides information as to the AM-AM characteristic of the device under large signal conditions. However, it is insufficient to perform deep analysis on the DUT and does not provide much information about the device behavior. For example, the device limiting physical phenomena like dispersion (as in trapping and thermal effect) cannot be understood and analyzed by this measurement technique.

The only data that provides a deep insight to the active device under test are the terminal RF I-V waveforms. The terminal RF I-V waveforms are the key that defines transistor performance. The ability to measure those waveforms provides critical information required to analyze the DUT; such as the performance of the RF relative

to the DC boundary condition.

In addition, the ability to interact with a DUT at different biasing and loading conditions provides the PA designer a tool to explore, modify and analyse different modes of operation under RF excitation. This experimental control is termed waveform engineering which is generally accepted in RF PA theory where the biasing level, circuit and device technology are deduced from these terminal I-V waveforms. Essentially, the key concept that waveform engineering offers is a unifying link between the basic RF theory and practical PA design [58].

Nonlinear measurement systems based on time domain systems like Nonlinear Vector Network Analyzer (NVNA) termed also Large-Signal Network Analyzer (LSNA) measures the terminal voltage and current under real conditions. These measurement systems introduced in the late 1980s are based on a network analyzer where the waveform measurement is carried by either a sampling down-converter or by a mixer down-converter. These waveforms are then constructed by measuring samples over many cycles of the repeating waveform. Applications of nonlinear measurement systems based on time domain systems includes [5, 58]:

1. Semiconductor device development: for instance, the observation of the limiting physical boundaries of the transistor allows to understand the transistor technology's limiting conditions, which then can be fed back to enhance transistor processing techniques.

2. Device model extraction, evaluation: the measurement carried out on a DUT can be directly compared to the device model in CAD simulation and thus provides a verification tool. Also, the measured linear and nonlinear data allows the modeling of small and large signal behavior of a transistor.

3. Amplifier circuit design and characterization: the ability to measure the DUT performance at a matched and mismatch condition allows the designer to target specific design goals such as gain, efficiency, power,..etc. Also, PAs nonlinearity can be measured such as AM-AM distortion, AM-PM distortion and IM distortion. In addition, transistors can be evaluated at a specific frequency, power or impedance environment. The ability to provide the desired impedance environment allows for the design and development of high efficient PAs at lower back off, for instance, the Doherty PA structure is operated under variable mismatch environments in several dBs of back off levels.

Load-pull measurement systems based on waveform engineering use either passive tuners as in a NVNA or active injection to present the required loads to the DUT. In the passive load-pull systems, the losses in the measurement system limit the range of load terminations while active load-pull systems overcome this problem by utilizing active sources to emulate the desirable load termination.

### 3.4.1 Active Load-Pull Measurement System

The validation measurements for the IPA mode have been carried out by using an active load-pull measurement system (Fig. 3.3) developed by Cardiff University [59]. The time-varying incident and reflected waves were measured using a four-channel digital sampling oscilloscope. The port under test is pulled to the desired impedances by three source generators operated at the fundamental, second and third harmonics. The measurement system is vector calibrated to obtain error corrected waveform measurement [58]. The measurements are carried on a transistor that is operated in real conditions but without considering the variations in temperature and the stress on PA's that might exist in practical wireless applications.

## 3.5 IPA Transistor Level Validation

The validation measurements presented in this chapter are for two cases. The first is for a fixed fundamental load measurement where class B and IPA mode sees the same fundamental load impedance. The second measurement will provide direct comparisons with the theory, where the load of the IPA mode is larger than class B load by $\sqrt{2}$ as been previously described in Sec. 2.9.

In this section, first the power flow calculation into the DUT will be described. Next, the first validation measurement will be presented and followed by discussion and analysis. Then, second measurement will be presented, which will provide more of a comparison to the theory part.

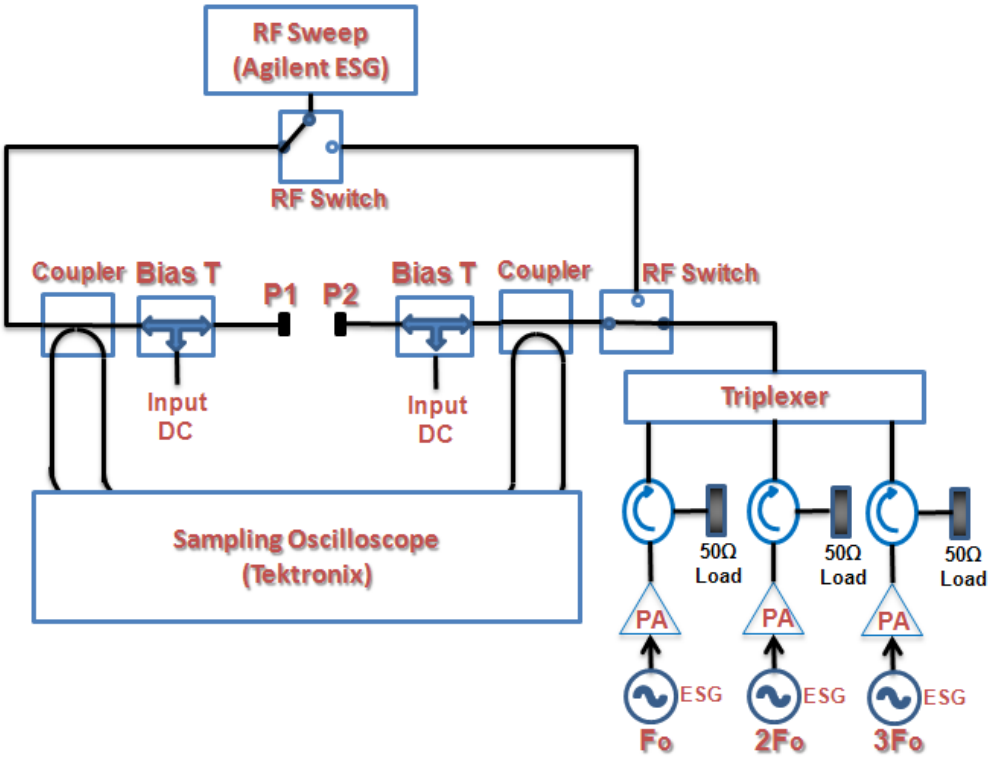



**Figure 3.3: Active load-pull measurement system.**

### 3.5.1 Power Flow into the DUT

From Network Theory, assuming peak values the power going into the DUT (Fig. 3.4) is calculated as follows [55]:

$$P_{in} = \frac{1}{2}\left[|a_2|^2 - |b_2|^2\right] \tag{3.12}$$

where $a = V_{incident}/\sqrt{Z}$ and $b = V_{reflected}/\sqrt{Z}$

From power flow graph Fig. 3.4:

$$b_2 = a_2\Gamma_{in} \tag{3.13}$$

$$a_2 = b_2 L^2 \Gamma_s + L a_s \tag{3.14}$$

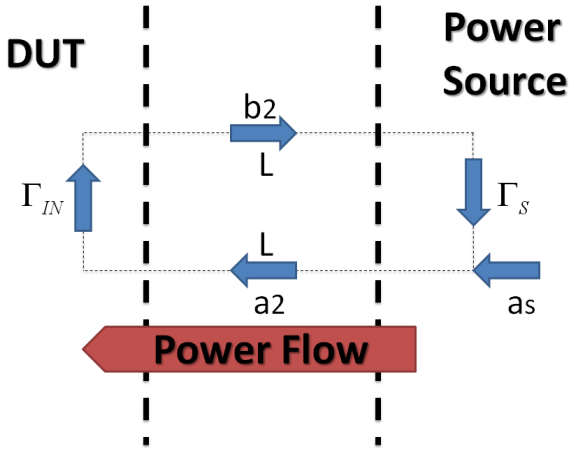



**Figure 3.4: Power flow.**

where $L$ is the link loss,

$$a_2 = a_2\Gamma_{in}L^2\Gamma_s + La_s \tag{3.15}$$

$$a_2[1 - L^2\Gamma_{in}\Gamma_s] = La_s \tag{3.16}$$

Assuming no loss in the link and both are matched,

$$a_s = a_2[1 - \left|\Gamma_{in}{}^2\right|] \tag{3.17}$$

If $\Gamma_{in} = 0$ , that is the whole power delivered to the DUT is fully absorbed,

$$a_s = a_2 \tag{3.18}$$

Therefore,

$$P_{in} = \frac{1}{2}\left|a_2\right|^2 \tag{3.19}$$

This analysis shows that the expected injected power will be affected by any mismatch and any loss in the link. Therefore, the expected injected power will be more than the ideal case and that will affect

the overall efficiency of the system.

### 3.5.2 Validation Measurement for a Fixed Load Impedance

To validate the IPA mode, experimental transistor investigations were undertaken at 0.9 GHz using the previously described waveform measurement and engineering system developed at Cardiff University. Since this measurement systems utilizes active harmonic load-pull, it can provide the negative impedances necessary to experimentally demonstrate the IPA mode of operation on a selected 10 W packaged GaN HEMT Cree Inc device (part number CGH40010F, see data sheet in **Appendix A**). For the appropriate comparison with theory the I-V waveforms at the current generator plane of the packaged device are required, hence a package parasitic de-embedding process [60] was used.

#### 3.5.2.1 IPA Measurement

In order to achieve the required half rectified class B current waveform, the 10 W GaN device was biased around pinch-off at a 28V drain voltage.

The active load pull measurement started from an inverted class F optimum fundamental loading condition; this initial point had a high loading condition [61] with an appropriate inductive reactance that compensated for the device's output capacitance at 0.9 GHz. The inverted class F condition was chosen because of the IPA and inverted class F both have the same approach with respect to the voltage waveform. Thus, in this measurement we will present the IPA mode

of that loading condition and then we will show the corresponding mode when no injection occurred. However, for a direct comparison with theory, a starting fundamental loading condition should be at class B which is the case in the second measurement that will be presented in Sec. 3.5.3.

After setting the fundamental loading condition, the active second harmonic loop was then used to inject energy at the second harmonic to appropriately shape the voltage waveform; targeting a half rectified waveform offset by 180 from the current waveform. Table 3.1 shows the measurement set up for IPA mode.

**Table 3.1: IPA MEASUREMENT BIASING AND LOADING CONDITION.**

| | $V_{gs}\ (V)$ | $I_q\ (mA)$ | $V_{ds}\ (V)$ | $\Gamma_{L(f_0)}$ | $\Gamma_{L(2f_0)}$ | $\Gamma_{L(3f_0)}$ |
|---|---|---|---|---|---|---|
| Package Plane | $-2.5$ | 180 | 28 | $0.26\angle 82°$ | $4\angle -94°$ | $1\angle -145°$ |
| $I_{gen.}$ plane | - | 180 | 28 | $0.13\angle 0°$ | $4\angle 178°$ | $1\angle 180°$ |

The measured load reflection coefficient of the second harmonic at the package plane is 4 with a phase of $-94°$ and that corresponds to a $178°$ relative to the fundamental at the current generator ($I_{gen.}$) plane. The de-embedding model for this device is shown in Appendix E. The measured I-V waveforms achieved at the $I_{gen.}$ plane are shown in Fig. 3.5. The even harmonic peaking I-V waveforms clearly demonstrate that the transistor can support this mode of operation.

### A. Second Harmonic Power Calculation

To calculate the injected second harmonic power to the DUT, first the load reflection coefficient seen by the DUT is measured as shown

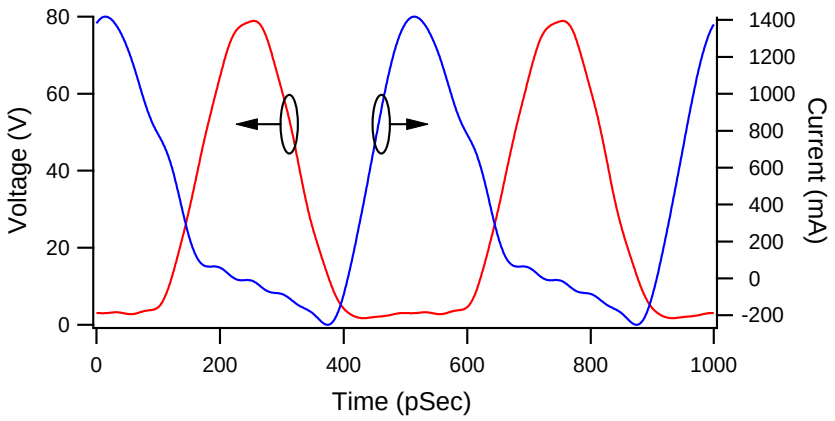



**Figure 3.5: IPA mode Voltage/Current waveforms de-embedded to the current generator plane for a fixed fundamental load impedance.**

in Fig. 3.6.

$$\Gamma_L = \frac{a_2}{b_2} \tag{3.20}$$

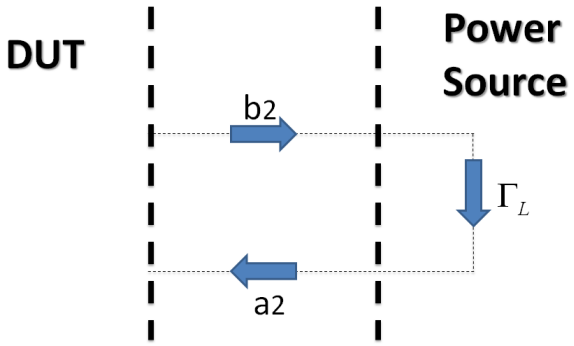



**Figure 3.6: Load reflection coefficient of DUT before injection.**

Then the required second harmonic impedance is presented to the DUT as shown in Fig. 3.7.

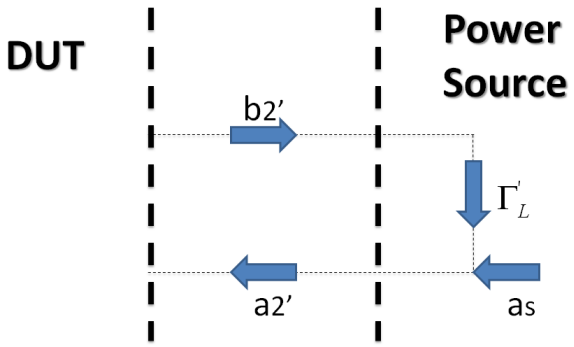



**Figure 3.7: Load reflection coefficient of DUT after injection.**

The new load reflection coefficient:

$$\Gamma'_L = \frac{a_2{}' + a_s}{b_2{}'} = \frac{b'_2\Gamma_L + a_s}{b_2{}'} \tag{3.21}$$

Therefore,

$$a_s = \Gamma'_L b'_2 - b'_2\Gamma_L \tag{3.22}$$

$$a_s = b'_2[\Gamma'_L - \Gamma_L] \tag{3.23}$$

Therefore, the output power from the source amplifier will be:

$$P_{inj} = \frac{1}{2}|a_s|^2 \tag{3.24}$$

An example for second harmonic power calculation is as follows; for the following measured output power: $P_{out} = 11.56$ W, $P_{dc} = 11.42$ W, $\Gamma_L = 0.01$, $\Gamma'_L = 5.9$ and $b'_2 = 0.26$. Using Eq. 3.23:

$$\begin{aligned} a_s &= b'_2\,[\Gamma'_L - \Gamma_L] \\ &= 0.26\,[5.9 - 0.01] = 1.5314 \end{aligned}$$

$\Gamma_L$ is very small compared to $\Gamma'_L$ and could be canceled from the equation. Using Eq. 3.24: $P_{inj} = 1.17$ W. Thus, TDE (Eq. 2.2) is 92 %.

Measuring the injected second harmonic power as been described, the efficiency of the IPA mode is calculated accordingly over a power sweep of 16 dB. Figure 3.8 shows that the maximum drain efficiency (Eq. 1.1) is 105% and total drain efficiency (Eq. 2.2) is 91.6 %.

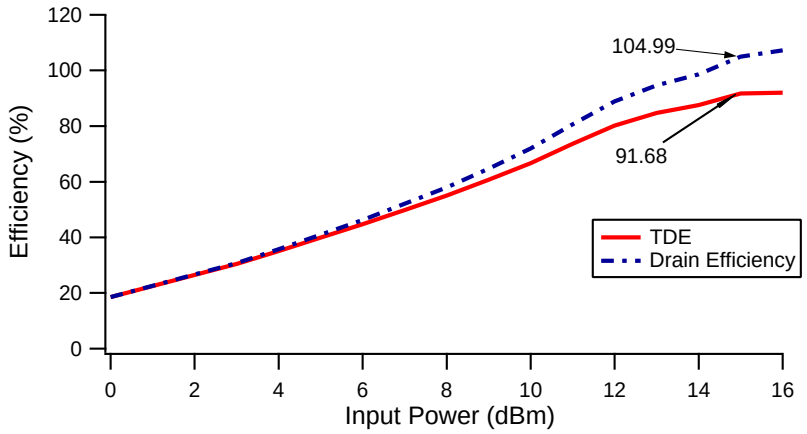



**Figure 3.8: IPA drain efficiency .**

The next section will show the performance of the transistor with and without injection mode. Those modes will be compared for output power, drain efficiency and DC power.

#### 3.5.2.2 PA Without Injection

The harmonic injection mode is set to be in off mode, i.e, no second harmonic injection. This mode, as will be seen, is as class B where all harmonic terminations are shorted. It has been measured at the

biasing and fundamental loading condition as in IPA mode and that resulted in a compressed class B as will be seen in this section. Table 3.2 details the measurement set up for compressed class B.

**Table 3.2: Compressed Class B MEASUREMENT BIASING AND LOADING CONDITION.**

| | $V_{gs}\ (V)$ | $I_q\ (mA)$ | $V_{ds}\ (V)$ | $\Gamma_{L(f_0)}$ | $\Gamma_{L(2f_0)}$ | $\Gamma_{L(3f_0)}$ |
|---|---|---|---|---|---|---|
| Package Plane | $-2.5$ | 180 | 28 | $0.26\angle 82°$ | $1\angle -94°$ | $1\angle -145°$ |
| $I_{gen.}$ plane | - | 180 | 28 | $0.13\angle 0°$ | $1\angle 178°$ | $1\angle 180°$ |

The voltage and current waveforms are shown in Fig. 3.9. As can be seen, once the class B condition applied at the same drive level as in IPA mode, the resulted current waveform is clipped since the loading is fixed as in the IPA condition; which resulted in a mode that is driven into the knee region. This confirms the IPA theory where the fundamental impedance of class B is reduced from IPA mode by a factor of $\sqrt{2}$. However, we will return to this issue later on in Sec. 3.5.3 where the fundamental impedance of class B will be reduced from IPA mode by a factor of $\sqrt{2}$, i.e., $R_{class\ B} = R_{IPA}/\sqrt{2}$.

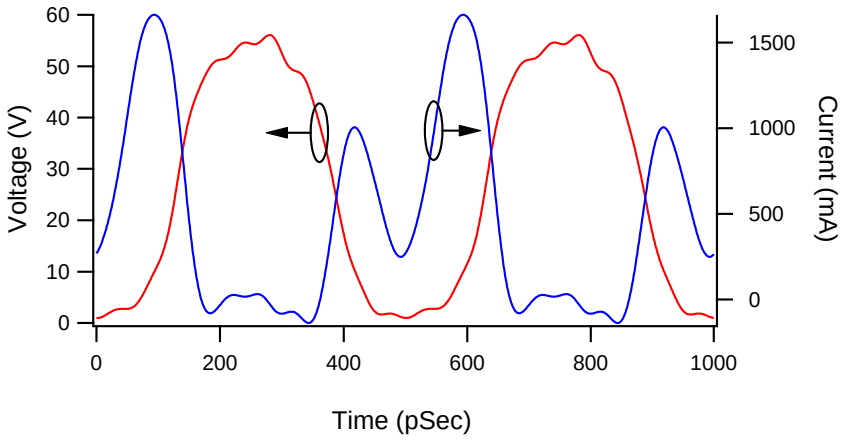



**Figure 3.9: Compressed Class B voltage & current waveforms.**

#### 3.5.2.3 Discussion

By Looking at the voltage and current waveforms, the first observation one can make is that in the compressed class B case the transistor is clearly overdriven in contrast to the IPA mode. In IPA mode, the active injected second harmonic voltage component contributed to an increase in the fundamental voltage component without forcing the current into a clipping regime (i.e., without hitting the voltage knee effect) and consequently, in accord with the theory, both the RF output power and efficiency increased.

The performance parameters of the compressed class B and IPA (at a fixed drive for a PEP of IPA mode) are tabulated below:

**Table 3.3: PERFORMANCE PARAMETERS COMPARISON.**

| | $\eta_{TDE}\%$ | $P_{out}$(dBm) | $P_{dc}$(dBm) | $V_{\max}$(V) | $I_{max}@V_{ds}$ |
|---|---|---|---|---|---|
| Compressed Class B | 57 | 38.8 | 41.3 | 56 | $1.66A@10.2V$ |
| IPA | 91.6 | 40.8 | 40.5 | 78 | $1.414A@3.0V$ |

In the following sections, the output power, DC power, maximum voltage, efficiency and linearity of compressed class B and IPA mode will be compared at the same fundamental load for the same device.

**A. Maximum Voltage**

The measured maximum voltage for IPA is 78 V and this is expected with IPA's high even peaking effect since:

$$V_{\max} = V_{dc}+V_1+V_2 = V_{dc}+\sqrt{2}\,(V_{dc}-V_k)+0.5\,(V_{dc}-V_k) = 78.3\ V$$

where $V_{knee} = 1.74$ V. While for compressed class B the maximum voltage is 56 V which is close to the expected maximum voltage:

$$V_{\max} = V_{dc} + V_1 = V_{dc} + (V_{dc} - V_k) = 28 + 26.3 = 54.3 \ V$$

This shows that the even harmonic of the IPA allows the fundamental component to be increased resulting in a voltage waveform with a high peaking.

**B. Output Power**

Ideally, the load of class B ( Table 2.1) should be lower than the one of the IPA by $\sqrt{2}$, i.e.;

$$R_B = \frac{R_{IPA}}{\sqrt{2}} \tag{3.25}$$

and that results with output power of class B being less than IPA case by 1.5 dB (Eq. 2.44).

$$P_B = \frac{V_{dc}^2}{2R_B} = \frac{V_{dc}^2 \cdot \sqrt{2}}{2R_{IPA}} \tag{3.26}$$

For the same load condition, the output power of class B is less than IPA mode by 3 dB. This is because the fundamental impedance is kept the same as IPA load impedance, i.e., $R_B = R_{IPA}$, thus;

$$P_{compress\ class\ B} = \frac{V_{dc}^2}{2R_{IPA}} \tag{3.27}$$

Therefore, using Eq. 2.33 the output power of this mode will be less than IPA mode by;

$$P = 10 \cdot \log(\frac{P_{compress\ class\ B}}{P_{IPA}}) = 10 \cdot \log(\frac{1}{2}) = -3\,dB \tag{3.28}$$

The measured output power versus input power performance is as shown in Fig. 3.10 and as can be seen, the peaking power of the IPA has increased by 2 dB when compared to compressed class B.

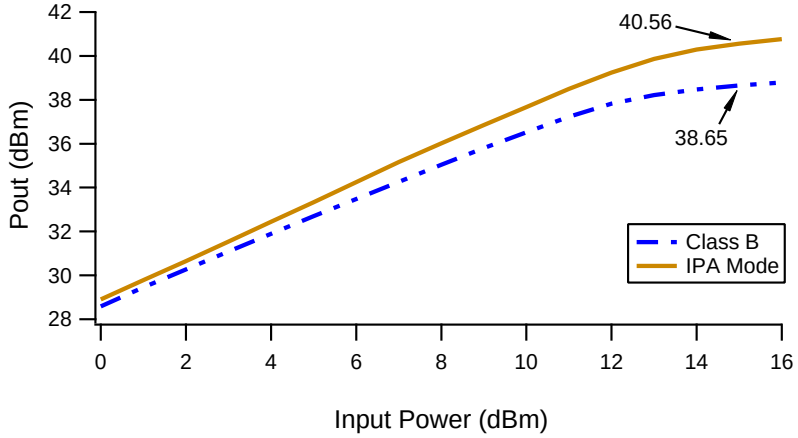



**Figure 3.10: Output power comparison .**

This is less than expected and is most probably due to the knee effect which also impacts the output power of the transistor. The theoretical output power including the knee effect will be:

$$P_{compress\ class\ B} = \frac{V_{dc}^2}{2R_{IPA}} \cdot (1 - \frac{1.74}{28})^2 = \frac{V_{dc}^2}{2R_{IPA}} \cdot 0.88\ W$$

The resulting output power in comparison to the IPA case will be;

$$P = 10\log(P_{compress\ class\ B}/P_{IPA}) = 10\log(0.88/0.5) = -2.4\ dB$$

Thus, the expected theoretical increase of IPA mode should be 2.4 dB, which compares well with the obtained measurement results in Fig. 3.10.

### C. Efficiency

To compare compressed class B and IPA efficiencies for the same

device, a plot of drain and total drain efficiency is shown in Fig. 3.11. As can be seen the drain efficiency of the IPA mode (91.6%) has increased by 35% compared to compressed class B (57%).

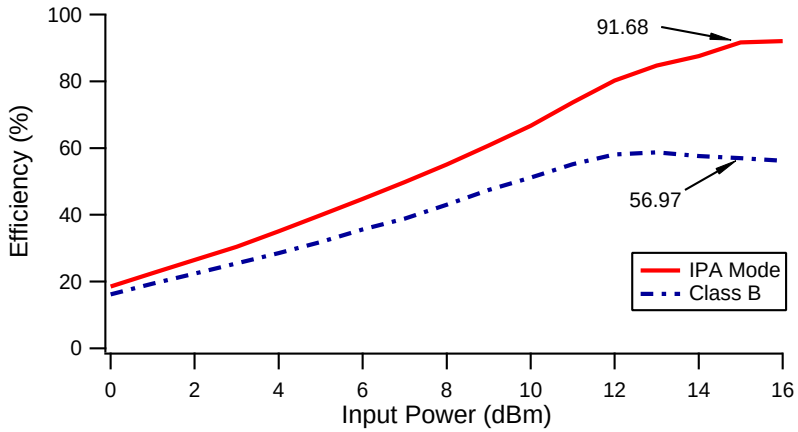



**Figure 3.11: Efficiency comparison .**

The displayed TDE efficiency of the IPA mode takes into account the RF energy injected at the second harmonic. The measured 91.6% is relatively close to the predicted value of 95.2% (corresponding to that for a 100% efficient second harmonic generator). The small difference can be associated with the knee effect which will limit the maximum voltage swing. Considering the knee effect in drain efficiency calculation, and assuming a 100% efficient conversion of the RF second harmonic injected power, the predicted TDE efficiency is:

$$\eta_{IPATDE} = \frac{P_{RF}}{P_{dc}(1+\frac{V_k}{V_{dc}}) + (\frac{P_{rf_{2f0}}}{\eta_{2f0}})} = 90.4\%$$

where $V_k = 1.74V$ is the measured minimum voltage value. This adjusted efficiency is in good agreement with the measurements. In fact, the measured efficiency is slightly higher than the theoretical

value and possibly this is partially due to the advantageous effect of the higher harmonic voltage components produced by the system impedance. In addition, the theoretical result is calculated at PEP (i.e., at the maximum linear output power), however, in practical PA devices specifying the maximum linear point is difficult due to the variation in the gain of the PA. As a result, measuring TDE with a tenth of a dB compression could also contribute to this slight increase of efficiency. Also, the loading of compressed class B is not optimal and therefore delivered lower performance; the comparison between class B and IPA mode will be presented in the following section.

### 3.5.3 Validation Measurement Where the Load Impedance of the IPA Mode is at the Optimum Load Condition

This measurement shows a direct comparison between class B and IPA mode. Class B is measured first. Next, IPA mode will be measured at a fundamental load that equals $\sqrt{2}\ Z_{L_{class\,B}}$ as been discussed in Sec. 2.9 (Table 2.1).

The class B mode is measured for a 10 W GaN device and biased around pinch-off at a 28 V drain voltage. The resulting class B loads at the current generator plane are tabulated in Table 3.4 along with the measured performance.

#### 3.5.3.1 Measurement and Results

To establish IPA mode for even second harmonic injection, the fundamental load is determined according to Eq. 2.30 relative to class B

(the loading condition is presented in Table 3.4). The voltage and current waveforms of class B and IPA mode are shown in Fig. 3.12 and 3.13 respectively. The dynamic RF load lines for both class B

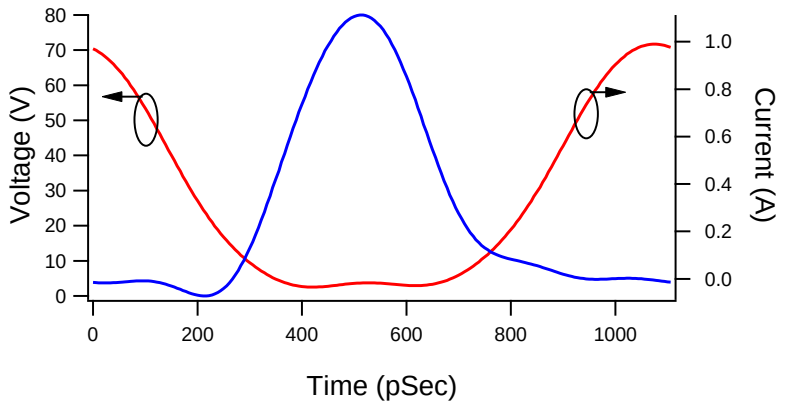



**Figure 3.12: Class B voltage/current waveforms de-embedded to the current generator plane for an optimum fundamental load impedance.**

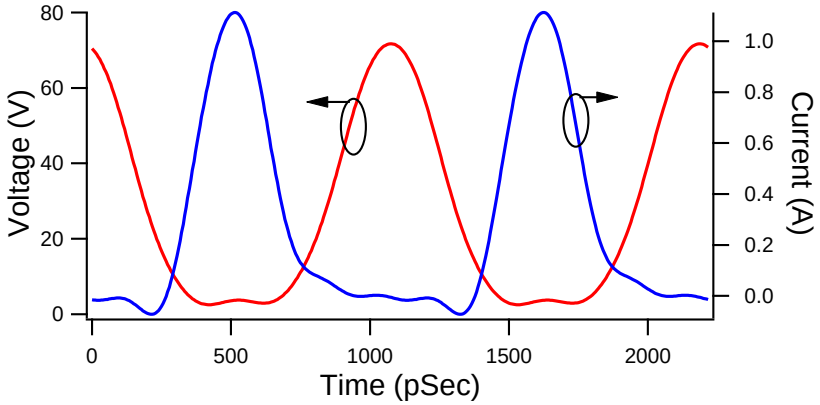



**Figure 3.13: IPA Voltage/Current waveforms de-embedded to the current generator plane for an optimum fundamental load impedance.**

and IPA mode are shown in Fig. 3.14. In the IPA mode the active injected second harmonic voltage component allows the fundamental voltage component to be increased without clipping the current

waveform. This confirms the analysis presented in Sec. 2.9 where the IPA mode shows a more efficient dynamic load line compared to class B, previously shown in Fig. 2.14 and in Fig. 2.18. The IPA mode shows a load line that looks like an L shape which indicates that when the transistor is in the on state (i.e., conducting), the voltage waveform has a flat waveform compared to class B. This implies that the dissipated power in the IPA mode is less than that of class B which translates to an increase in drain efficiency. Also, the RF voltage waveform is allowed to swing to larger than twice of the DC drain voltage supply and that indicates an increase in the fundamental voltage component. This increase in the fundamental voltage component implies an increase in the RF output power compared to class B. Therefore, the drain efficiency of the IPA mode is expected to be much higher than that of class B.

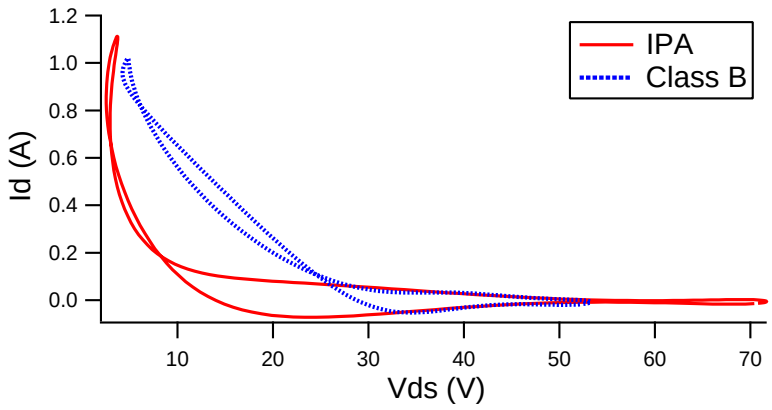



**Figure 3.14: RF load line of class B and IPA de-embedded to the current generator plane.**

For drain efficiency calculation the second harmonic injected power is considered in the drain efficiency equation as in Eq. 2.2 as-

suming a 100% efficient conversion of the RF second harmonic injected power. The measurement results are tabulated in Table 3.4 where a high drain efficiency mode has been measured and verified the expected theoretical high drain efficiency.

**Table 3.4: MEASUREMENT PERFORMANCE PARAMETERS FOR CLASS B AND IPA MODE.**

| | Class B | IPA mode |
|---|---|---|
| $\Gamma_{f_0}$ | $0\angle 0°$ | $0.17\angle 0°$ |
| $\Gamma_{2f_0}$ | $1\angle 180°$ | $4\angle 140°$ |
| $\Gamma_{3f_0}$ | $1\angle 180°$ | $1\angle 180°$ |
| $P_{f_0}$ (dBm) | 37.8 | 39.14 |
| $P_{2f_0}$(dBm) | 0 | 31.1 |
| $P_{dc}$(dBm) | 38.9 | 39.0 |
| $\eta_{TDE}$ (%) | 73.2 | 89.6 |
| $V_{max}(V)$ | 53.2 | 71.7 |

#### 3.5.3.2 Discussion of Device Measurements

**A. Fundamental and Harmonic Load Reflection Coefficients**

This section will compare and relate the output impedances of the measurement to the theory. The output impedance of the device is relatively large and for simplicity a fundamental load of $50\,\Omega$ has been chosen for class B. For output load of $Z_0 = 50\,\Omega$ (Fig. 3.15), the fundamental and second harmonic load reflection coefficients (Eq. 3.1) of class B for the following output impedances presented to the DUT $Z(f)_{Class\ B} = 50\,\Omega$ and $Z(2f)_{Class\ B} = 0$ are:

$$\Gamma(f)_{L\ Class\ B} = \frac{Z_L - Z_0}{Z_L + Z_0} = 0\angle 0 \tag{3.29}$$

$$\Gamma(2f)_{L\ Class\ B} = 1\angle 180 \tag{3.30}$$

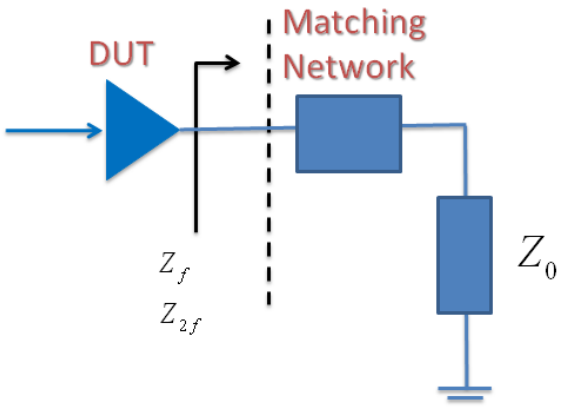



**Figure 3.15: Schematic of a DUT showing the output load reflection coefficient.**

The corresponding fundamental and second harmonic load impedances of IPA mode (Eq. 2.30, 2.35) are:

$$Z(f)_{IPA} = \sqrt{2}Z_f = \sqrt{2}Z_0 \tag{3.31}$$

$$Z(2f)_{IPA} = \frac{-3\pi}{8\sqrt{2}} \cdot Z_f = \frac{-3\pi}{8} \cdot Z_0 \tag{3.32}$$

Hence, load reflection coefficients of IPA mode will be:

$$\Gamma(f)_{L\,IPA} = \frac{\sqrt{2}Z_0 - Z_0}{\sqrt{2}Z_0 + Z_0} = 0.17\angle 0 \tag{3.33}$$

$$\Gamma(2f)_{L\,IPA} = 12.23\angle 180 \tag{3.34}$$

The measured result for the fundamental load reflection coefficient is close to the theoretical value, however, the measured second harmonic load reflection coefficient of $4\angle 140$ is lower than predicted theoretical value of $12.23\angle 180$ (Eq. 3.34). This can be due to the discussed knee effect of real devices (Sec. 2.9.3.2) where the second harmonic voltage component can be reduced from the $0.5 \cdot V_{dc}$ value,

which also decreases the required $\Gamma(2f)_L$ while the TDE is maintained high. In addition, the phase difference can be partially due to the fact that the current in practical transistors has not a perfect half rectified waveform. Also, the sensitivity of the phase of the second harmonic voltage component can tolerate some phase differences as discuss in Sec. 2.9.3.1.

**B. Maximum Voltage**

The measured maximum voltage for IPA is 71.7 V; the maximum voltage can be calculated as:

$$V_{\max} = V_{dc}+V_1+V_2 = V_{dc}+\sqrt{2}\,(V_{dc}-V_k)+0.5\,(V_{dc}-V_k) = 75.8\ V$$

where $V_{knee} = 2.9V$. While for class B the maximum voltage is 53.2 V which is close to the expected maximum voltage:

$$V_{\max} = V_{dc} + V_1 = V_{dc} + (V_{dc} - V_k) = 28 + 23.8 = 51.8\ V$$

This shows that the even harmonic of the IPA allows the fundamental component to be increased resulting in a voltage waveform with a high peaking.

**C. Output Power**

The measured output power has increased by 1.34 dB and this is comparable to the theoretical value of 1.5 dB. This increase in power is in part due to the injected second harmonic power contributing to around 1 dB of the change and the efficient utilization of the transistor as well. This outcome highlights an alternative interpretation of how this amplifier works. The resulting waveform shaping allow for

the conversion of RF power injected at the second harmonic to RF power at the fundamental frequency [50].

This result confirms the output power analysis presented in Sec. 2.9.1 . Moreover, the required injected second harmonic power is, as expected, only 16% of the fundamental output power.

#### D. Efficiency

The measured efficiency, taking into account the RF energy injected at the second harmonic is 89.6% at P1dB assuming a 100% conversion efficiency. However, the predicted theoretical IPA TDE is 95.2% (corresponding to a 100% efficient second harmonic generator). Considering a more realistic knee effect, as in Table 2.2, reduces ideal TDE from 95.2% to 89.7% (optimized IPA) and 87.7% (IPA) at PEP. The measured TDE of the IPA mode is relatively close to the theoretical results taking into account the knee effect and gain compression. Thus, validation measurement confirms that a transistor can support this mode with a highly linear efficient operation.

## 3.6 Summary

This chapter presented a validation measurements for an injection power amplifier mode. The validation measurement chapter started with an overview on linear and nonlinear characterization in microwave frequencies. Next, the waveform measurement system that was used for the validation measurement was briefly described. Following the brief description of the waveform measurement system used for the validation measurement, the Injection Power Amplifier

(IPA) was established by injecting appropriate second harmonic power at the output port of the device.

This chapter shows that a transistor operated under real conditions can indeed support IPA mode. The measurement results are in agreement with theoretical analysis. The TDE efficiency of the measured IPA mode reached high linear efficiency of 90%, and that in accord to theory considering the knee effect of the device. The output power of the measured IPA mode was also in agrement with the theoretical part (1.5 dB) with an increase of 1.31 dB; the analysis concluded that the difference of 0.19 dB between the theory and measured data is due to the knee effect of the real device.

# *Chapter 4*

# Injection Power Amplifier Design

## 4.1 Introduction

In chapter 3, the validation measurement proved that IPA mode can be supported by a transistor in a real operating condition. In this chapter, IPA design based on the active load-pull measurements (Chapter 3) will be presented.

This chapter, starts with a background on PA design for small signal and large signal design. Next, PA design based on waveform engineering will be briefly described. A proposed IPA design is described and then realised as a proof-of-concept. Finally, the chapter concludes with a summary.

## 4.2 Power Amplifier Design Techniques

### 4.2.1 Small Signal Transistor Amplifier Design Technique

Linear power amplifiers are typically designed around small signal S-parameters. These measurement are carried out in a 50 $\Omega$ system where the incident and reflected waves are measured. These basic linear measurement usually performed by VNAs to characte-

rize passive structures and linear active devices. Several equations can be calculated from S-parameter measurements that defines gain, minimum Noise Figure (NF), stability, bandwidth, or power.

For instance, Fig. 4.1 illustrates the reflection coefficient of a microwave amplifier [57]. The input and output reflection coefficients of the transistor are calculated as:

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{4.1}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{4.2}$$

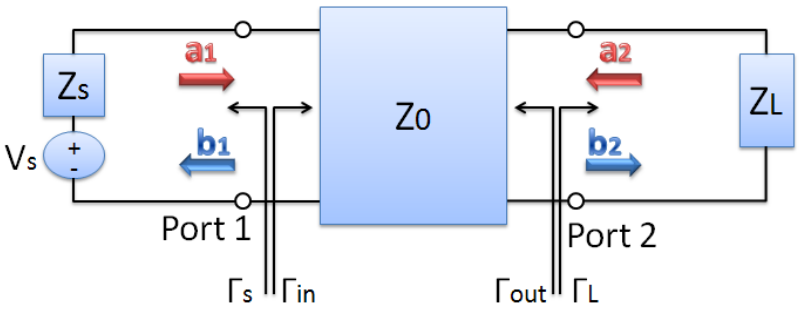



**Figure 4.1: Schematic of input and output reflection coefficient of a DUT .**

An input matching network needs to transform the source impedance $Z_S$ (usually 50 Ω) into the input impedance of the transistor $Z_{in}$. Also an output matching network is required to transform the load impedance $Z_L$ (usually 50 Ω) to the output impedance of the transistor $Z_{out}$. Therefore, for a maximum power transfer the source and load reflection coefficient are required to be conjugately mat-

ched i.e.;

$$\Gamma_S = \Gamma_{in}^* \tag{4.3}$$

$$\Gamma_L = \Gamma_{out}^* \tag{4.4}$$

where the asterisk denotes the complex conjugate.

In addition, S-parameters are used to determine the stability consideration of a transistor. Stability determines the transistor's resistance to oscillation and this is a very important factor in amplifier design. For instance, amplifier design with stability factor (K) greater than unity assures an unconditional stability condition, i.e., no oscillation will occur under any passive termination. Stability factor is calculated as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{4.5}$$

and

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{4.6}$$

Often, amplifier design parameters such as gain and power are mapped into contours on a Smith chart; this allows a PA to be designed according to design specifications. Once the targeted design goals are specified, the output and input matching networks are designed accordingly along with a stabilizing circuit. [53, 57]

Small signal design is appropriate for low power applications such as Low Noise Amplifier (LNA) designs with output power levels well below the compression region. A driver stage operated in

class A in the linear region can also be designed using the small signal design technique. However, small signal S-parameters lack the accuracy at high power levels where an RF amplifier is optimized and designed for high power high efficiency applications.

### 4.2.2 Large Signal Power Amplifier Design Technique

For high power amplifier design, small signal S-parameters are not valid as described in the previous section. Therefore, a large signal measurement is required to characterize the behavior of high power amplifiers.

High power Load-pull measurement systems allow high power PA characterizations and typically measure output power and the incident and reflected waves under small and large signal condition. The measured data set from load-pull measurements is a function of reflection coefficient which can then be mapped onto a Smith chart as output power contours.

High power RF PA design is usually based on the provided load-pull contours in the transistor's data sheet. From these load-pull contours, the input and output matching networks are designed accordingly to present the required reflection coefficient for a particular design specification.

CAD software is also used in high power amplifier design, however, it is not always available. Large signal models are hard to find and take time to develop. Issues of the accuracy of the large

signal model are always a problematic in PA design, hence, PA prototyping is used and usually requires several iterations to achieve the desired high efficiency operation. This is due to the lack of the relative phase information of the harmonics. In addition, the mode of operation cannot be determined when the RF current and voltage waveforms at the current generator plane are not available; accordingly the performance cannot be further optimized.

### 4.2.3 PA Design Based on Waveform Engineering

Since the terminal I-V waveforms are the key to high efficiency PA design, the observation of the waveforms along with employing waveform engineering concept is a key enabler for the design of highly efficient and linear PA modes of operation. This section will describe IPA design based on waveform engineering.

PA design based on waveform engineering [58] has shown state-of-the-art performance over a narrowband as in the high power high-efficiency inverse class F design [62] achieving drain efficiencies above 81%. This approach was also utilized in wideband design as in broadband class J [48] and broadband class F [63]. The performance of these PA prototypes is approaching the theoretical maximum with the first design iteration.

The approach is based on first measuring a transistor in a large signal waveform measurement system. The captured terminal waves and data set are mapped onto a smith chart. Using a de-embedding technique allows the waveforms at the current generator plane to be

computed. These data sets are also exported into CAD software; the input and output matching networks are designed accordingly. In addition, coupling the captured waveform measurement data with a large signal model allows further analysis on the transistor. Also, optimization techniques can be used to achieve the desired design goals.

## 4.3 IPA Prototype Design Based on Waveform Engineering

The proposed IPA consists of two RF paths where the upper one Fig. 4.2 generates the main fundamental radio frequency signal and a lower path with a smaller second harmonic auxiliary PA to control the I-V waveforms of the main PA. The injected even harmonic signal from the auxiliary PA establishes the IPA mode at the main PA. The fundamental RF path consists of a coupler to provide a fraction of the fundamental signal that can be up converted to second harmonic. Here, an off-the-shelf frequency doubler is employed to drive the small signal PA followed by the auxiliary PA. This proposed IPA structure will be tested with a CW signal, however, future designs should consider the effect of the doubler on modulated signals. The particular configuration has been chosen as all required components were at hand, however, other configurations are possible.

This IPA structure is more complex relative to other typical RFPA design. However, as been presented in the first chapter, RFPA design reaching complex design structure to address efficiency design for a

good dynamic range as in the Doherty and Chireix PA design. IPA mode, is also a complex structure which have the potential to address challenges in RFPA design such as high linear efficiency design or wideband design. In addition, IPA design is less complex than ET PA where in ET PA a step up efficient DC to DC conversion process is required.

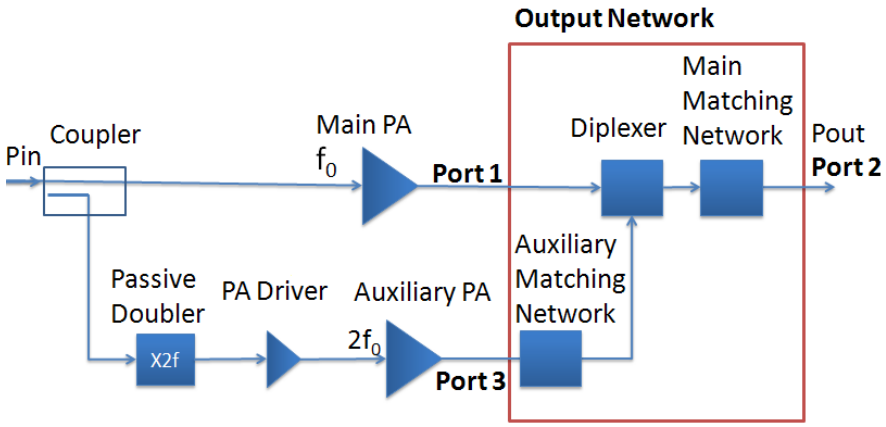



**Figure 4.2: Proposed topology.**

The IPA design starts with active load pull measurements on the device (PA) that are presented in Sec. 3.5.3. The emulated fundamental and harmonic impedances are measured. Next, the output matching network is designed accordingly using ADS (Advanced Design System). The output network design starts with the multiplexer network followed by the matching network. The multiplexer network is designed in such a way to allow the harmonic injection. In addition, a large signal model has been used for optimizing the output matching network with the diplexer design.

### 4.3.1 PA Demonstrator Design

For the proof of concept, the actual realized PA consists of two 10 W GaN (CGH40010F) HEMT (High Electron Mobility Transistor) devices biased at class B, the drain voltage is biased at 28V for the main device while the auxiliary device is biased at a much lower level at 8 V, since the required injected second harmonic power is much lower than the fundamental RF power. The PA demonstrator also includes an output matching network which consists of a simple multiplexer and impedance transformers. The devices have been chosen since they are commercially available; a nonlinear model exists and provides relatively high output power levels. For the circuit board a high frequency laminate board (TMM3) from Rogers Corporation is used. The board parameters are shown in Table 4.1. The input drive is achieved using two ESGs (Electronic Signal Generators); hence one is used to generate the second harmonic signal instead of a doubler and thus feeds the auxiliary PA directly.

**Table 4.1: Parameters Of The High Frequency Laminate Board (TMM3).**

| Parameter | Value |
|---|---|
| Substrate thickness | 0.762 mm |
| Relative dielectric constant | 3.27 |
| Relative permeability | 1 |
| Conductor conductivity | $5.961 \times 10^7$ Siemens/meter |
| Dielectric loss tangent | 0.002 |

#### 4.3.1.1 Multiplexer Design

The design starts with a multiplexer (Fig. 4.3) that allows the main PA (Port1) fundamental signal to see only a constant load while the

auxiliary PA (Port2) sees only the main PA. This way the RF fundamental signal finds its way to the load and the auxiliary PA performs the required waveform shaping.

The S-parameters for the multiplexer network (using ideal transmission lines) are shown in Fig. 4.4 with the network designed for a fundamental frequency signal at 0.9 GHz.

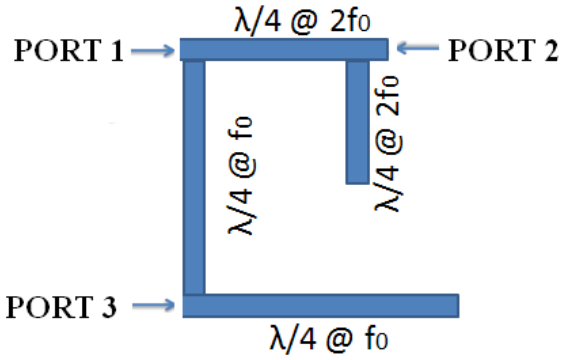



**Figure 4.3: Multiplexer.**

The resulting diplexer[1] network shifts the input impedance of port 1, and this shift is required to be considered in the design of the fundamental matching network; i.e., to transform the input impedance of port 1 ($\Gamma = 0.45\angle 153°$) into the desired load reflection coefficient of the DUT (Table 3.4).

The multiplexer network as can be seen from S(3,1) allows Port 1 to input a signal at $2f_0$ to Port 3, and sees an open circuit at the fundamental $f_0$ frequency, i.e., there is no power transferred between Port 1 and Port 3 at the fundamental $f_0$ frequency.

[1]The Diplexer is used as a general term to show that the network at Port 2 passes the low fundamental frequency and blocks the high second harmonic frequency, Port 3 passes the second harmonic frequency while blocking the fundamental frequency and Port 1 is the common port. However, this networks doesn't perform as the exact definition of a Diplexer.

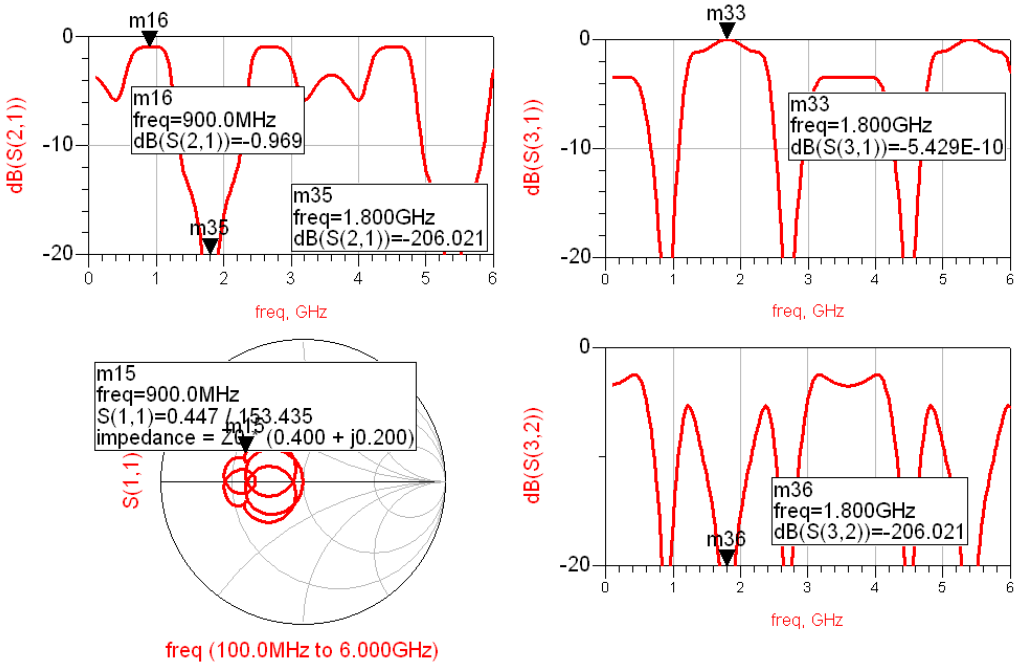



**Figure 4.4: S-parameters for the multiplexer network.**

#### 4.3.1.2 Output Matching Network

The output matching network was designed for optimum performance according to the load pull measurements while the auxiliary PA's matching network was designed based on the provided data sheet of the device (Appendix B). The design of the output matching network was challenging since the output network needs to present the required optimum fundamental and harmonic loads while allowing the frequency multiplexing at the same time. So a compromise in the design was considered. Next, an optimization process in ADS was used, the load reflection coefficient of the output network is displayed in Fig. 4.5.

The output matching network is required to present the desired

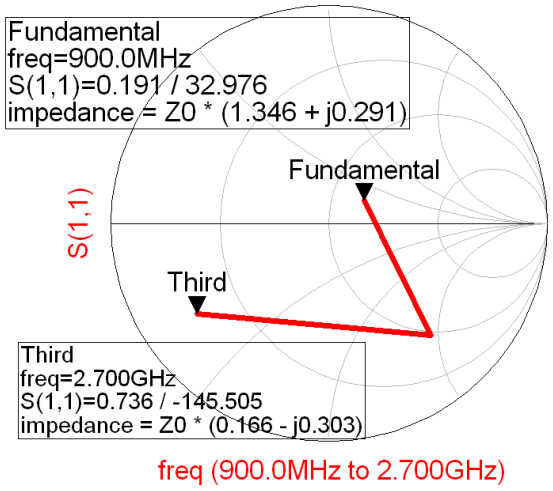



**Figure 4.5: Load reflection coefficient of the output matching network.**

fundamental load reflection coefficient of $\Gamma_L = 0.17\angle 0°$ (Table 3.4). The output network (Fig. 4.5) is designed accordingly with an optimization process for both the multiplexer and the matching networks. Looking at Fig. 4.5, the fundamental load reflection coefficient presented to the current generator plane of the device is $0.19\angle 33°$ which is not precisely the desired fundamental reflection coefficient presented in Table 3.4. In addition, the third harmonic reflection coefficient is $0.74\angle -145°$ which is not a perfect short circuit. Accordingly the performance of the realised PA is expected to be lower than the performance displayed in the validation measurement results.

To quantify the loss of the output network, the S-parameter of the output network is measured in ADS software, where the source impedance is defined as 58.5 $\Omega$ for port 1 (i.e., corresponds to the matched case of $\Gamma = 0.17\angle 0°$) and a 50 $\Omega$ load at port 2. The insertion loss S(2,1) of the output network is 0.21 dB (Fig. 4.6). This link

loss will reduce the output power and as a result reduces the theoretical TDE (95.2%). The output power of IPA mode (Table 2.1) will be reduced to;

$$\begin{aligned} Pout &= P_{IPA} - P_{loss} \\ &= ([10 \cdot \log(0.707)] + 30\,dBm) - 0.21\,dB \\ &= 28.5 - 0.21 = 28.29\,dBm = 0.675\,W \end{aligned}$$

Therefore, the new theoretical TDE accounting for the insertion loss will be;

$$TDE = 0.675/0.743 = 90.8\%$$

.

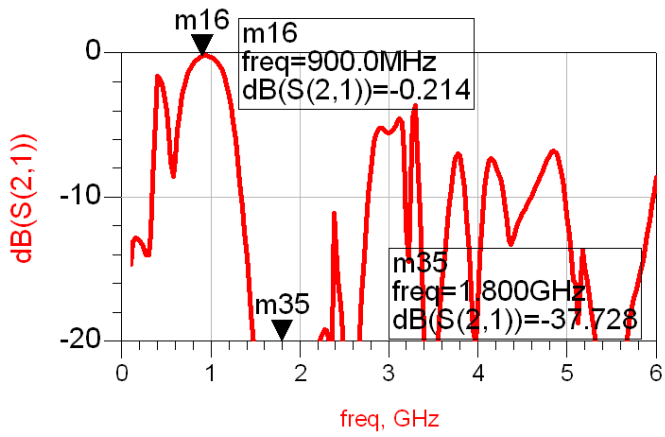



**Figure 4.6: Insertion loss S(2,1) of the output network.**

For more comparable results, the measurement results presented in Table 3.4 show TDE of 89.6% with output power of 39.14 dBm which will be reduced by the insertion loss of 0.21 dB to 38.93 dBm. Accordingly, the TDE will be reduced to 85.3%

### 4.3.2 PA Simulation Results

The schematic of the PA demonstrator is shown in Appendix C. The simulated results (Fig. 4.7) shows TDE of 78.6% at P1dB and 88% at the saturated output power level.

The difference in drain efficiency at P1dB between the simulated results ($\eta_{TDE} = 78.6\%$) and the validation measurement results ($\eta_{TDE} = 89.6\%$) is partially due to the output matching network where the fundamental and harmonic loads are not the desired optimum loads as been pointed out earlier. In addition, the DC power of the injected second harmonic power in the validation measurement is calculated from the measured RF power assuming a unity drain efficiency of the auxiliary source. However, despite the fact that this circuit is the first design version of IPA mode, the expected drain efficiency at only a modest drain compression of 1 dB is 78.6%.

Figure 4.7 shows that with a further investigation and optimization, the efficiency can be further increased by using an optimised drive strategy. As the plot shows that optimizing the phase of the second harmonic signal can increase the TDE up to 80% at P1dB; this will be carried out in the realized IPA power amplifier to optimize the efficiency at the maximum linear operation. Moreover, this topology has interesting drain efficiency behavior. It does not decrease but continues to increase as the PA is driven hard into saturation, a result that can be utilized in some applications. This drain efficiency behavior is likely to be due to the discussed positive slope of the knee effect which the IPA mode utilized efficiently. The predicted

efficiency at the saturated output power of 11 W is 88%.

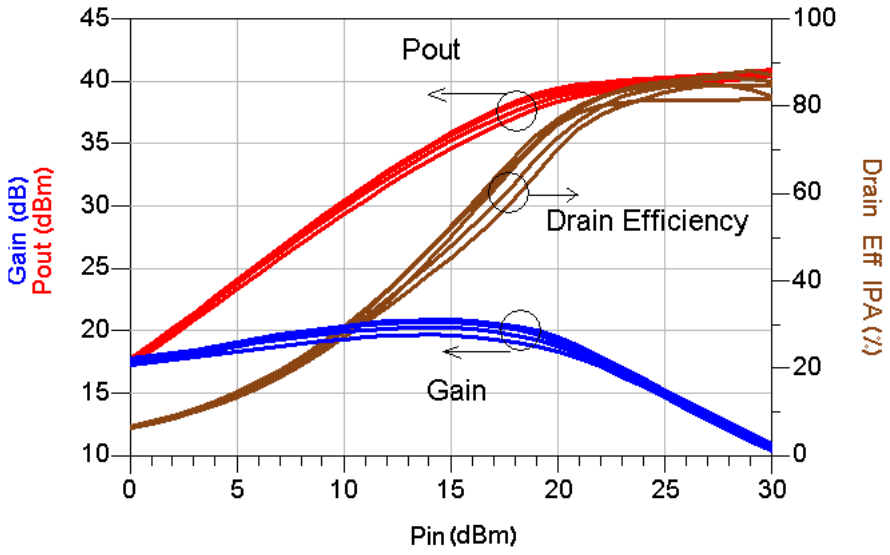



**Figure 4.7: IPA simulation results for an increasing phase offset between the two input signals.**

### 4.3.3 Realized PA Demonstrator

This is the first stage in the design, the IPA demonstrator is designed to be driven by two Electronic Signal Generators (ESGs) for both the fundamental and second harmonic input power as previously depicted in Fig. 4.3. The PA demonstrator (Fig. 4.8) was successfully fabricated and characterized. It achieved a drain efficiency of 74.3% at 900 MHz at P1dB for a non-optimal drive strategy. The highest drain efficiency was 85.7% at the saturated output power of 10 W. (Fig. 4.9)

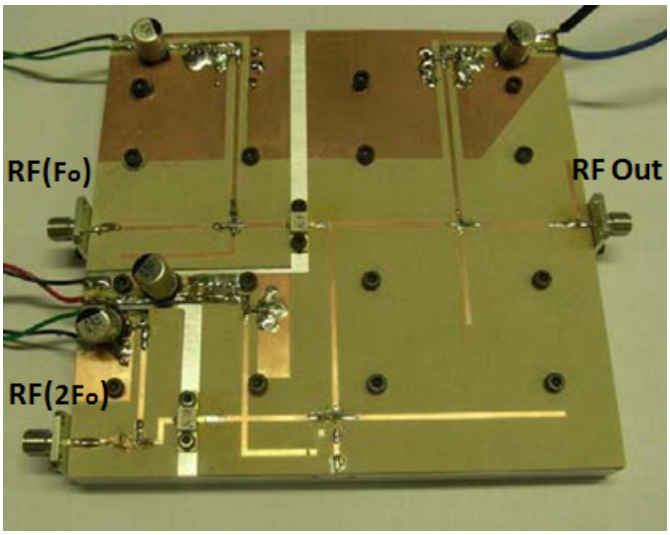



**Figure 4.8: Realized IPA.**

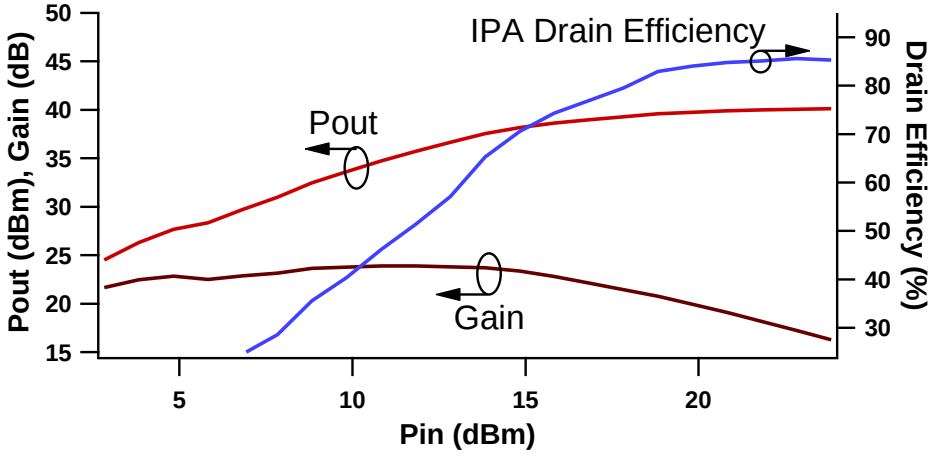



**Figure 4.9: IPA measurement results for a constant (and hence not yet optimized) magnitude and phase offset between the two drive signals.**

### 4.3.4 IPA Power Amplifier

A complete functioning IPA power amplifier with a single input (Fig. 4.2) has been designed using a coupler, doubler and PA driver. The PA driver is an off the shelf PA used at the low power side.

Therefore, the DC power of the driver has not been considered in the drain efficiency equation.

Considering the knee effect, the second harmonic power has been optimized at the P1dB compression point where the injected second harmonic power is reduced. The optimized driving condition has shown enhanced results (Fig. 4.10) with a drain efficiency of 80% at P1dB and this result is more comparable to the analysis presented in the theory part. Although the IPA power amplifier presented here is only a proof of concept where a multiplexer utilized $\lambda/4$ transmission lines, which limited the utilized bandwidth, the measured relative bandwidth is 22% for drain efficiencies of 60-80% at P1dB.

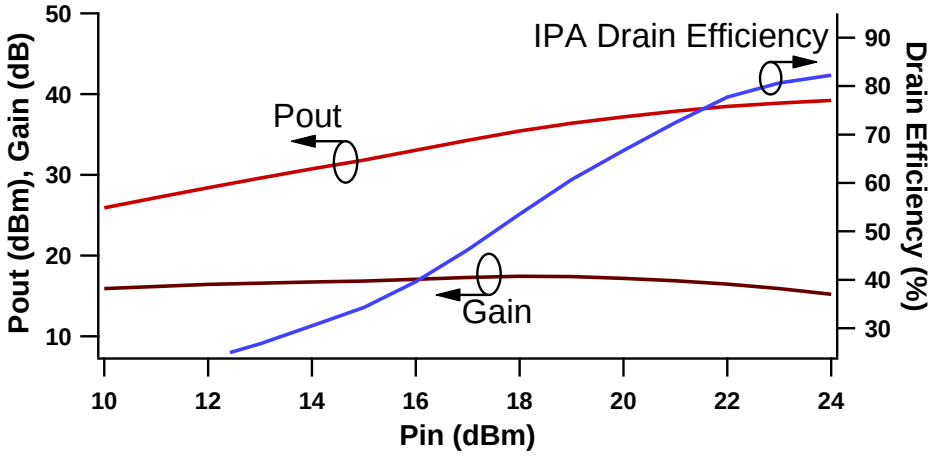



**Figure 4.10: IPA power amplifier measurement results.**

Linearity was not the intention of this research and the aim of the PA prototype is to demonstrate the IPA mode. However, many applications have a standard linearity specs; thus, a two-tone signal has been measured and the output spectrum at the P1dB compression

point is shown in Fig. 4.11. The third-order intermodulation distortion IM3 is -24 dBc and the fifth-order intermodulation distortion IM5 is -22 dBc.

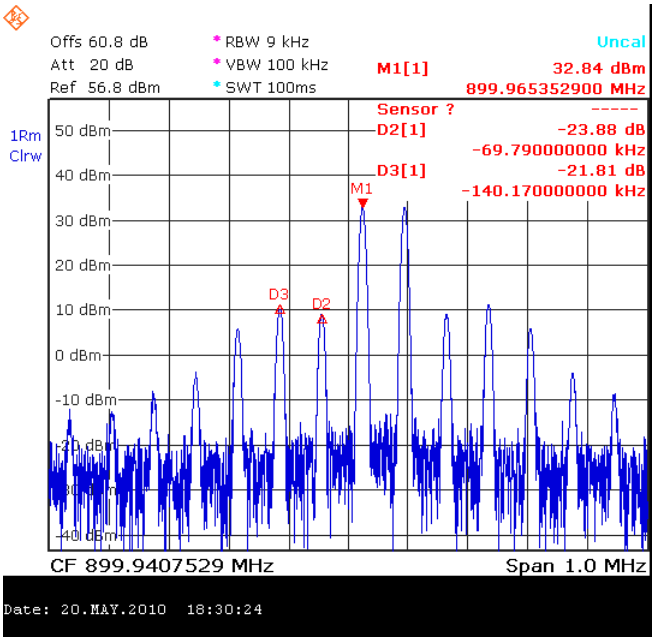



**Figure 4.11: IPA power amplifier linearity measurement.**

## 4.4 Summary

This chapter has provided a proof of concept in the detailed PA prototype. The IPA is designed according to the validation measurements in Chapter 3. The output network is designed to perform two crucial tasks: first to function as a diplexer network to allow second harmonic power injection into the main device and also passes the fundamental signal into the load; second, to present the required fundamental and harmonic impedances extracted from the load-pull measurements. The design of the output network was satisfactory

but did not present exactly the required fundamental and harmonic load impedances. Hence, the simulated and measured results of the IPA prototype was less than the validation measurement of the device.

The IPA prototype is designed, built, and characterized; the measured results of the IPA prototype at 0.9 GHz shows a high linear efficiency of 80% at P1dB compression point and 86% at 4 dB compression point delivering the rated output power of 10W. Despite, the deviation of the realized matching network from the desired fundamental and harmonic impedances, the IPA prototype shows a high linear efficiency mode; hence, this proof of concept IPA prototype validates the injection power amplifier concept and its potential.

# *Chapter 5*

# Extending IPA mode Towards Wide Band Power Amplifier Applications

## 5.1 Introduction

Creating a wide bandwidth high efficient PA is the ultimate design goal for the next generation of mobile communication. A single wideband PA reduces the cost and size of a multiple narrowband PAs. In addition, wideband PAs can be employed in multi-standard and multi-band applications.

In this chapter, a state-of-the-art wideband PA designs in the current literature will be presented. Next, a novel approach for wideband PA design will be described employing a multi-mode approach. Each mode of the proposed wideband design will be discussed. In addition, a combining network, which is a key design part in the multi-mode approach will be described. Finally, a summary of the chapter will be presented.

## 5.2 Wide Band High-Efficiency Power Amplifier Design

Typically, power amplifiers require fundamental and harmonic matching circuits to achieve high efficiency figures. Class B, for example, has a high drain efficiency of 78.5% while class F is 91.7% and both require a high Q-factor network which typically limits the operating bandwidth into 10%.

For wideband applications, RFPAs are traditionally designed in class A operation where the theoretical peak efficiency is 50% and in real devices the peak efficiencies are typically in the range of 40%. For high efficiency operation, RFPAs require a high reflective harmonic termination, which limits the operating bandwidth to less than an octave since the second harmonic frequency will be part of the fundamental operating bandwidth. For instance, the recently introduced wideband class J [48] and continuous class F [63] design show a high efficiency operation across a wide frequency band, however, still limited to less than one octave.

The published state-of-the-art highly efficient PAs $\eta > 55$ % and wideband BW >50 % are shown in Table 5.1.

**Table 5.1: STATE-OF-THE ART WIDEBAND RFPA.**

| Reference | Class | Frequency (GHz) | Freq. Ratio | Power (W) | Gain (dB) | Drain Eff. (%) |
|---|---|---|---|---|---|---|
| [48] | J | 1.4-2.6 | 1.9 | >11 | >9 | 60-70 |
| [64] | E [1] | 1.9-4.3 | 2.4 | >10 | >9 | 57-72 |
| [63] | F | 0.55-1.1 | 2 | >8.5 | >9.5 | 65-80 |

[1] It did not mention in that paper which class but was based on a switch mode model for the device with second harmonic phase tuning which is more likely to be a variant of class E operation.

Table 5.1 shows that only recently has the research community attempted to mitigate the bandwidth limitation of high efficiency operation. The maximum achieved bandwidth as shown in the table is not far from the theoretical limitation of an octave bandwidth. Also, it is worth mentioning that most of the published work operated in a harmonically tuned PA modes across most of the bandwidth. In cases in which the frequency band extends beyond an octave, most of the designs are operated in class B mode with resistive harmonic loading or a variant of restively harmonic loaded class E/F/J in the lower band; since by definition the harmonic loads of the harmonically tuned PAs (class J/F/E) require a high reflection network. This is not the case for those designs, the resistive harmonic loads from the lower frequency range become then the fundamental impedance at the upper band, hence, allowing for operation beyond the octave limitation. This is not stated in those published works and there was not any analysis on the mode of operation at the lower band.

## 5.3 Wideband IPA Design

Ideal wide band IPA operation can be implemented with an ideal circulator as previously shown in Fig. 2.10. However, due to the lack of an ideal broadband circulator, another design approach can be implemented by using filters and a diplexer. A diplexer based on a quarter wavelength transmission line can provide the required function of passing the fundamental signal from DUT to the load, and allows simultaneously the second harmonic signal to pass to the DUT port; however, this approach has a limited bandwidth of

operation. As a result, due to the lack of circuits that behave as an ideal circulator, a new approach is proposed based on multi-mode approach, which will be discussed in the next section.

### 5.3.1 A Novel Multi-Mode Approach

A novel approach, based on combining passive and active harmonic terminations would theoretically allow the designer to maintain the required harmonic terminations across a multi-octave band. In this design, second harmonic injection will be utilized to present a variant of different modes [65]: class B, class J and IPA mode that are located at neighboring frequency bands. Hence, active and passive harmonic injection architectures would be a significant improvement to such systems to push further the limitations of today's PAs' efficiency and bandwidth.

### 5.3.2 Modes of Operation

The following section will briefly summarise three proposed PA modes of operation in the multi-mode approach.

#### 5.3.2.1 Resistive Loaded Class B

Considering class B with a second harmonic resistively loaded, the current waveform is a half rectified sine wave:

$$\mathrm{i}\left(\theta\right) = \mathrm{I}_{\max}\left[\frac{1}{\pi} + \frac{\sin\theta}{2} + \sum_{\mathrm{n}=2,4,..}^{\infty} \frac{-2}{\pi\left[\mathrm{n}^2-1\right]}\cos\left(\mathrm{n}\theta\right)\right] \tag{5.1}$$

and the voltage waveform is defined as:

$$\mathrm{v}(\theta) = V_{dc}[1 - 0.5 \cdot Z(f_0) \cdot sin\theta + Z(2f_0) \cdot \frac{2}{3\pi} cos2\theta] \qquad (5.2)$$

where $V_{dc}$ is drain DC bias voltage and $I_{max}$ is the saturation current. The resistively loaded class B impedances are defined as:

$$Z(nf_0) = \begin{cases} R_n + j \cdot 0 & for\ n = 1\ or\ 2 \\ 0 + j \cdot 0 & for\ n > 2 \end{cases} \qquad (5.3)$$

Using Eq. 5.1-5.3, the performance of a transistor as a function of the ratio of the second harmonic impedance to the fundamental impedance $(Z_{2f_0}/Z_{f_0})$, drain efficiency $(\eta_{Drain})$, power utilization factor (PUF) and harmonic distortion of the second harmonic power referenced to fundamental $(HD_{2f_0})$ of the resistively loaded class B are shown in Table 5.2.

**Table 5.2: RESISTIVE LOADED CLASS B PERFORMANCE ACCORDING TO RATIO OF THE SECOND HARMONIC TO THE FUNDAMENTAL IMPEDANCE.**

| $Z_{2f_0}/Z_{f_0}$ | $\eta_{Drain}$ (%) | $PUF$ $(dB)$ | $HD_{2f_0}$ $(dBc)$ |
|---|---|---|---|
| 1 | 55 | -1.5 | - 7 |
| 0.5 | 65 | -0.9 | -10 |
| 0 | 78.5 | 0 | -inf |

Table 5.2 shows that according to the ratio of the second harmonic to the fundamental load, a compromise between efficiency, PUF and linearity can be achieved in wideband PA design. For instance, as the second harmonic impedance reaches half of the fundamental impedance, the drain efficiency increases up to 65% with a compromised linearity and output power. That is, drain efficiency of class B

(78.5%) will be reduced to (65%) when the second harmonic is in midway between a short and the fundamental load $Z_{f_0}$. The second harmonic distortion is -10 dBc; and the power utilization factor is -0.9 dB which indicates that the RF output power in this mode will be less than ideal class B by 0.9 dB. These output power and linearity results has been observed for wideband design reaching an octave [64] where the lower band sees the resistive impedance of the upper band.

Class B with a reduced second harmonic load relative to the fundamental load allows wideband design with a compromise between efficiency, power and linearity. This approach will be exploited in the lower band where harmonics still lie in the operating band.

This analysis considered only a second harmonic resistive load since all higher harmonics will be much lower than the second harmonic load due to the fact that the output capacitance of the device will present a lower reactive impedance to the higher harmonics. In addition, the output passive network can also be used to present a high reflection network at out of band frequencies.

#### 5.3.2.2 Class J

Class J offers class B performance with drain efficiency of 78.5%. Class J [48] has shown high efficiency operation over broadband bandwidth reaching up to 60% of percent bandwidth. Class J will be used at the upper band where the harmonics required for class J operation will be out of the operating bandwidth and thus the passive

network will be designed to present the highly reflective network required for class J operation. The optimum fundamental and second harmonic loads are:

$$Z_{f_0} = R_0 + j \cdot R_0 \tag{5.4}$$

$$Z_{2f_0} = 0 - j \cdot \frac{3\pi}{8} \cdot R_0 \tag{5.5}$$

#### 5.3.2.3 IPA mode

IPA mode will be used in the mid band to support the transition between the two modes operated in the lower and upper band and so extend the operating bandwidth. The fundamental and second harmonic loads of IPA mode [52] are:

$$Z_{f_0} = \sqrt{2}R_0 + j \cdot 0 \tag{5.6}$$

$$Z_{2f_0} = \frac{-3\pi}{8} \cdot R_0 + j \cdot 0 \tag{5.7}$$

### 5.3.3 Proposed Multi-Mode Operation

The design is based on presenting appropriate harmonic load impedances that can be actively modified over a range of frequencies to improve the power and efficiency performance of a wideband power amplifier. The PA topology will be based on the IPA structure as depicted in Fig. 5.1.

The key novel aspect of the design concept proposed is that in the mid band the IPA mode will be utilized to provide a transition between the two modes of operation and thus extending the operating bandwidth.

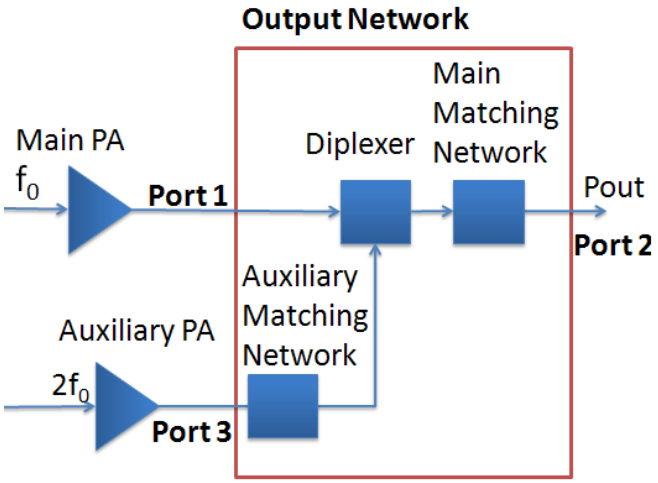
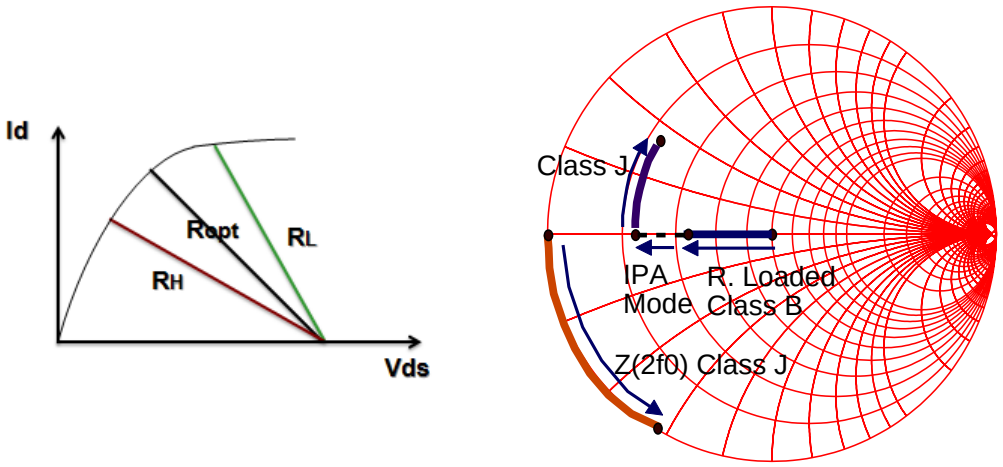



**Figure 5.1: Injection power amplifier.**

The impedance requirements of the proposed multi-mode is shown in Fig. 5.2, where a resistively loaded class B is operated in the range of $f_0$ to $3f_0/2$ therefore, the second harmonic load will span from $2f_0$ to $3f_0$, hence in-band. Class J operation will span from $3f_0$ to $4f_0$ therefore, the second harmonic load will span from $6f_0$ to $8f_0$, hence above band, and thus will be highly reflective as shown on the smith chart. IPA mode will be utilized to link those two modes of operation where it spans from $3f_0/2$ to $3f_0$, thus provide for active second harmonic impedance control from $3f_0$ to $6f_0$.

The load line in Fig. 5.2 shows that a compromise between those modes will have to be considered to achieve a drain efficiency greater than 60% for a double-octave bandwidth. The gain and output power will not be flat across the operating bandwidth due to the different modes employed in each band. However, to have more flatter gain and power across the band, a possible solution is to design the




(a) Load line (b) Smith chart

**Figure 5.2: Multi-mode operation.**

PA around a 1.5 dB contour of the optimum power ($P_{opt}$) by choosing the impedance of the upper band to be half of the impedance at the lower band i.e., $R_L = R_H/2$. Choosing $R_H = \sqrt{2}R_{opt}$, where $R_{opt}$ is the optimum impedance of the device for maximum output power. The output power [19] for those impedances at the high and low load conditions will be;

$$P_{out} = \frac{P_{opt}}{\sqrt{2}} \tag{5.8}$$

Therefore, the output power at the upper and lower bands relative to the $P_{opt}$ are;

$$P_{out} = 10 \cdot \log\left(\frac{P_{out}}{P_{opt}}\right) = 10 \cdot \log\left(\frac{1}{sqrt2}\right) = -1.48\,dB \tag{5.9}$$

Figure 5.3 shows the fundamental impedances versus frequency for a double-octave bandwidth design where the impedance of the upper

band is half of that at the lower band.

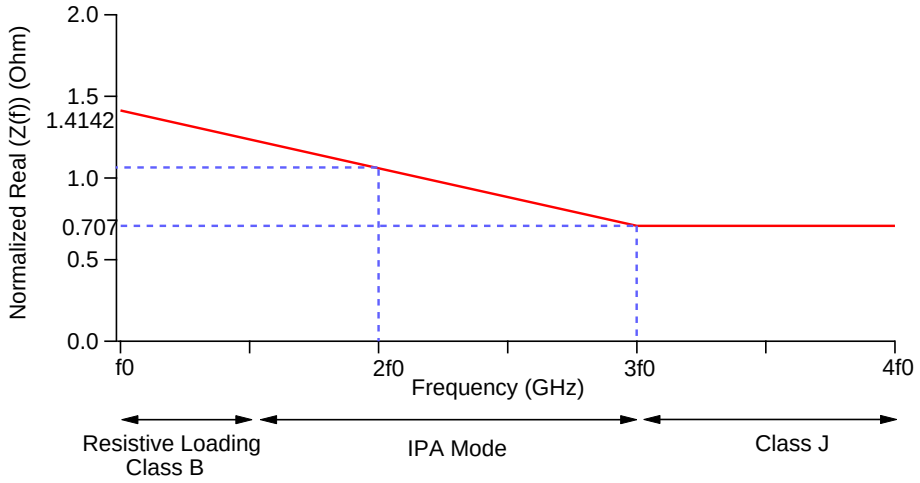



**Figure 5.3: Fundamental impedance of a multi-mode design where the impedance at the upper band is half of the impedance at the lower band.**

### 5.3.4 Combining Network

A key aspect in this design is the development of a suitable combining network that allows injection of the second harmonic signal, which is generated by the auxiliary PA, without interfering with the signal transmission of the fundamental signal path between the main PA and the load. As a result, the main device can be designed in such a way that it sees an optimum fundamental load across a multi-octave band while the second harmonic impedance is generated by both the passive network and active injection. The ideal function of the combining network is depicted in Fig. 5.4. Such functionality can be approximated by a diplexing network or a power combining network.

The complete PA of the IPA structure was shown in Fig. 4.2 and

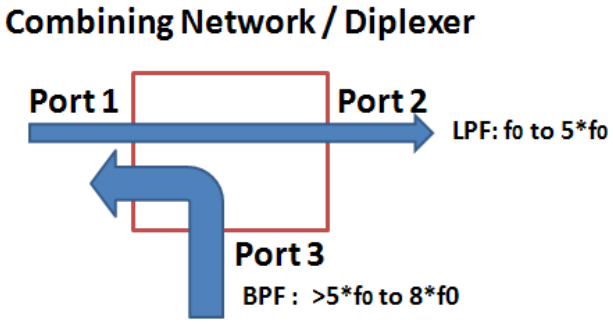



**Figure 5.4: Combing network/ Diplexer.**

that will be adopted in **Chapter 6** for a wideband PA design. As been previously described, a coupler has been utilized to extract a fraction of the input signal which is then fed into a passive doubler to generate the second harmonic signal. After that the second harmonic signal is input into a low power driver and then into the input of the auxiliary PA. Thus, IPA mode can be used in the designated mid band. On the other hand, the output network consisted of the combining network, main matching network and auxiliary network should be designed for fundamental matching and also to provide the necessary passive harmonic terminations for the lower and upper bands.

## 5.4 Summary

A proposed extension of IPA mode to wideband design has been presented. Due to the technical design challenges of designing an ideal broadband circulator required for broadband IPA mode, a novel approach based on multi-mode operation that combines both passive and active harmonic injection is proposed. A key circuit combining

network design has been described to allow multi-mode operation of passive and active harmonic injection. In this multi-mode design, a compromise between efficiency, linearity and output power has been considered for wideband operation. The proposed PA can be designed for bandwidth exceeding a double-octave. In the lower band, a resistive class B is proposed where harmonics lie in the operating bandwidth, the proposed design considered a lower load at the harmonics of class B; in this mode the efficiency is traded for output power, gain and linearity. In the mid band, the IPA mode is employed to extend the operating bandwidth. In the upper band, class J is designed where the harmonics lie outside the operating bandwidth.

# *Chapter 6*

# A Novel Multi-Mode Power Amplifier Design

## 6.1 Introduction

The proposed multi-mode PA in **Chapter 5** will be designed, built and characterized. This chapter starts with introducing a conceptual system for a double-octave bandwidth; the response of the output network will be defined for each mode of operation.

Since the design is for broadband operation (double-octave), the fundamental matching and harmonic terminations across this bandwidth will be hard to achieve at the exact required impedances, especially with a complex output network that consists of a combining network and the main and auxiliary matching networks. Thus, the design will be based on a non-linear model of the devices; and an optimization process for the output network will be used in ADS software.

A conceptual system of the output network response will be first defined to provide the required fundamental matching, passive termination and harmonic injection across the relevant frequencies at

each band. Next, the large signal model will be investigated for DC analysis, stability and then a load-pull simulation across the desired bandwidth will be carried out. Finally, a multi-mode wide band PA prototype will be designed, built and measured.

## 6.2 Multi-Mode PA Design

### 6.2.1 PA Design Strategy

For a 4:1 bandwidth (double-octave) design [65], the design will utilize three modes of operation across 0.7-2.8 GHz as shown in Table 6.1. In this design, the targeted efficiencies are PAE >50% and the resistive loading class B will be extended to cover larger band from $f_s$ to $2f_s$, so that the IPA mode will cover a band from $2f_s$ to $3f_s$ and that is more practical for the complex design of IPA mode, while class J covers the band from $3f_s$ to $4f_s$. The IPA mode will be active only in the desired bandwidth by using band pass filters at the input side of the auxiliary PA. Alternatively, the limited bandwidth of passive doublers can also be utilized at the input of the auxiliary PA to output only the desired second harmonic frequency.

**Table 6.1: MODES OF OPERATION.**

| | Fundamental Load | Second Harmonic Load |
|---|---|---|
| Resistively Loaded Class B | $f_s$ to $2f_s$ 0.7 to 1.4 GHz | Passively Loaded |
| IPA mode | >$2f_s$ to $3f_s$ >1.4 to 2.1 GHz | Actively loaded |
| Class J | >$3f_s$ to $4f_s$ >2.1 to 2.8 GHz | Passively Loaded |

### 6.2.2 Conceptual System for Double-Octave BW

#### 6.2.2.1 Lower Band

In the lower band, as has been proposed in **Chapter 5**, a resistively loaded class B will be designed. The output network of the multi-mode PA will be designed as shown in Fig. 6.1

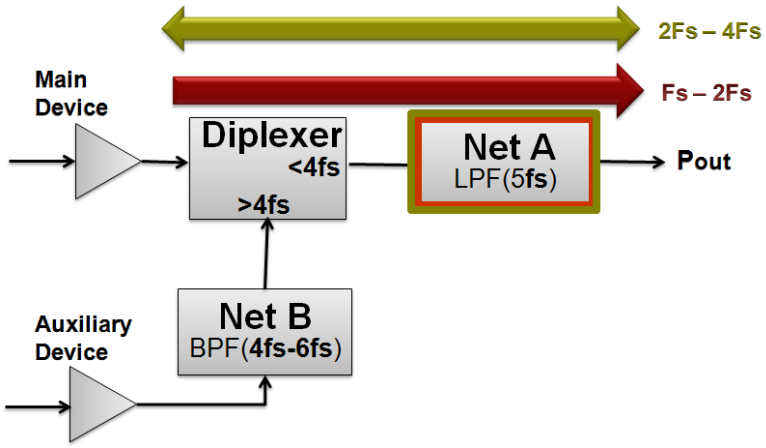



**Figure 6.1: Conceptual system design showing restively loaded class B output network.**

The Diplexer network will pass the fundamental signal from $f_s$ to $4f_s$. Thus, *Network A* will present the fundamental and second harmonic loads.

#### 6.2.2.2 Middle Band

IPA operation is shown in Fig. 6.2 in the band ($2f_s$ to $3f_s$). The fundamental signal will pass through the lower port ($< 4f_s$) of the Diplexer where *Network A* will present the fundamental matching. The second harmonic load will be actively controlled by the auxiliary device. *Network B* will be designed for a fundamental matching of the

auxiliary device.

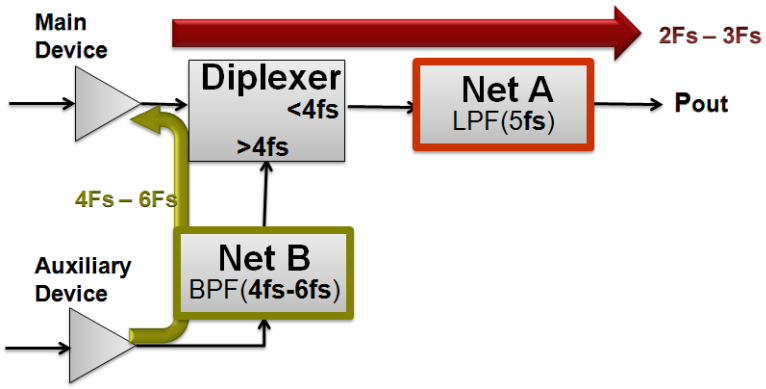



**Figure 6.2: Conceptual system design showing IPA output network.**

#### 6.2.2.3 Upper Band

In the upper band, class J will be designed for the band ($3f_s$ to $4f_s$) as shown in Fig. 6.3. *Network A* is designed to presents matching network for the fundamental signal. While *Network B* is designed to present the second harmonic load required for class J operation.

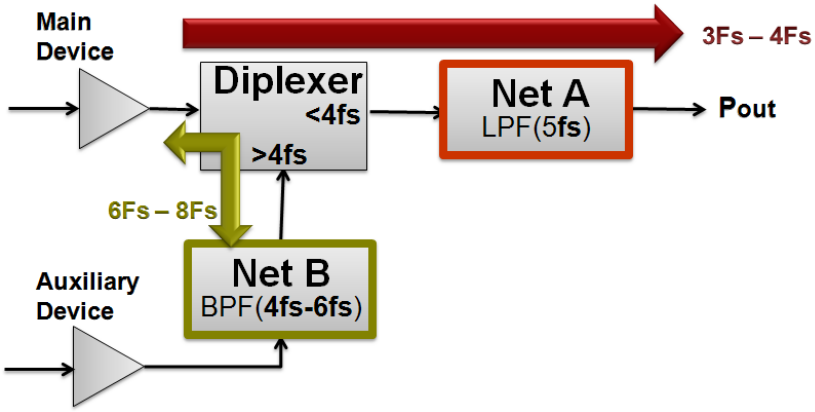



**Figure 6.3: Conceptual system design showing class J output network.**

### 6.2.3 Device of choice for Broadband Applications

For broadband operation, the selection of the device is critical. The bandwidth is limited in high power devices by the high capacitance and small optimum load. A small optimum load will require multi-section matching networks which is suitable at a fixed frequency. However, with a high capacitance, the matching for broadband operation is hard to achieve. Therefore, for high efficiency high power applications a device technology with a small capacitance and high output optimum load will be preferable over other technologies.

A wide bandgap semiconductor as a GaN HEMT devices have high power density which is more than 10 times that of GaAs technology. This means GaN devices have a smaller periphery which makes the device capacitance much lower than other technologies for the same operating power. In addition, GaN HEMT devices have a high breakdown voltage and that results in a high output impedance. Therefore, the low output capacitance coupled with a high output impedance allows for simple input and output matching networks to be designed for broadband applications. [66, 67]

### 6.2.4 Device Characteristics

In this section, we will look at the characteristics of the 10 W Cree device (CGH40010F) which will be used in this wideband PA design. First we will perform DC Analysis followed by S-parameter simulation and then the design of a stabilizing circuit.

#### 6.2.4.1 DC Analysis

Performing a DC analysis (Fig. 6.4) on the 10 W Cree device shows that the gate pinch off is around -2.4 V and more than 10 W can be achieved from this device. The knee voltage is around 3 V and has a high breakdown voltage which is suitable for a mode of operation that requires high voltage peaking.

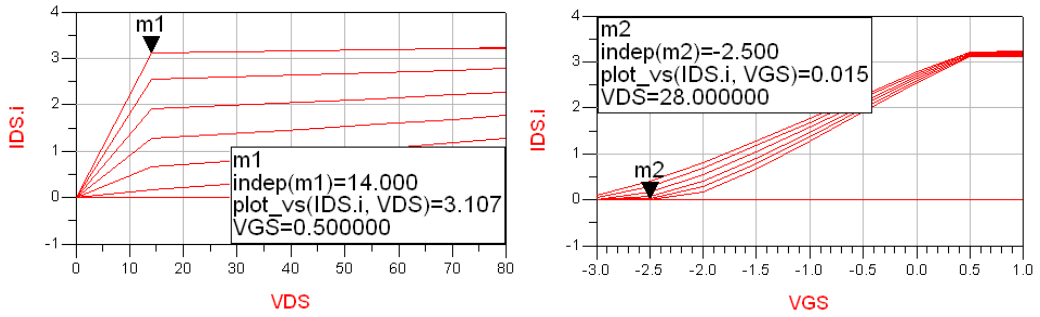



**Figure 6.4: DC analysis.**

#### 6.2.4.2 S-Parameter Simulation

In this section, S-parameter simulation will be performed (Fig. 6.5) to look at the 10 W Cree device behavior. Figure 6.6 shows that at class B bias condition the usable operating bandwidth for a maximum available gain greater than 10 dB is roughly from DC - 5 GHz.

#### 6.2.4.3 Stability

A stabilising circuit with a series resistive loading of 10 Ω and a shunt resistance of 47 Ω with a bank of shorting capacitance (Fig. 6.7) was used to attain unconditional stability (i.e., k-factor >1) across

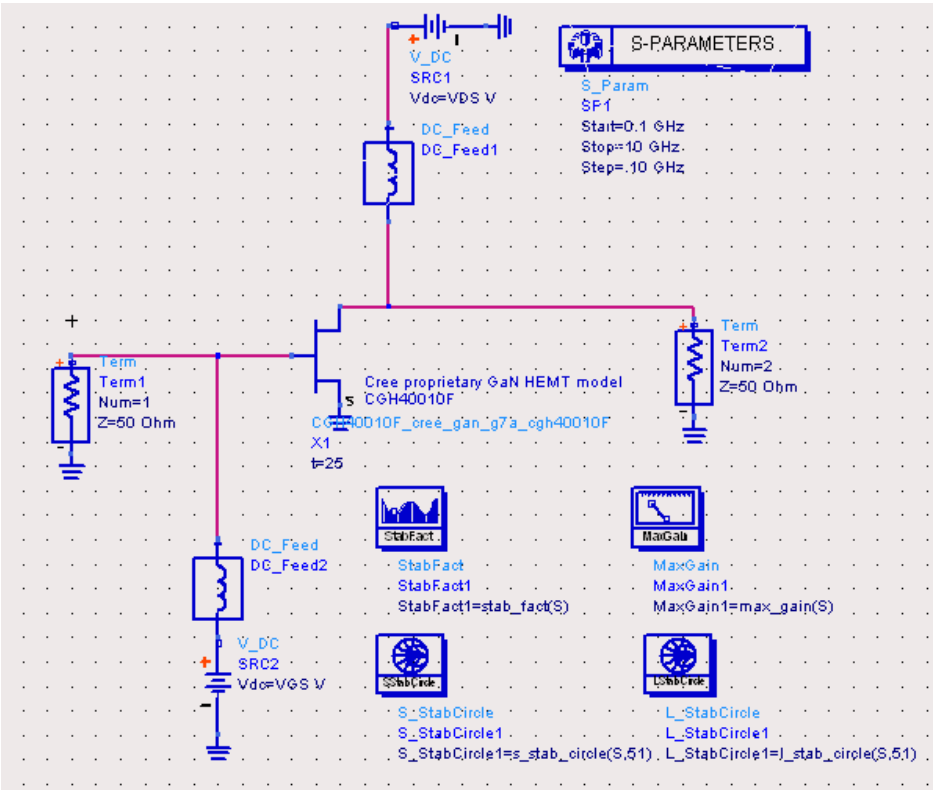



**Figure 6.5: Schematic of s-parameter simulation.**

in band and out of band frequencies. The steps of improving the gain at the higher band is described in (Appendix D).

S-parameter simulation for the PA device with the stabilizing circuit is shown in Fig. 6.8. It can be seen that the transistor is unconditionally stable and has a maximum available gain of greater than 10 dB for the required operating bandwidth (0.7-2.8 GHz)

#### 6.2.4.4 Load-Pull Simulation

Load-Pull simulation has been performed to identify the optimum fundamental impedance for a maximum efficiency across the operating bandwidth. The resulting optimum fundamental and harmo-

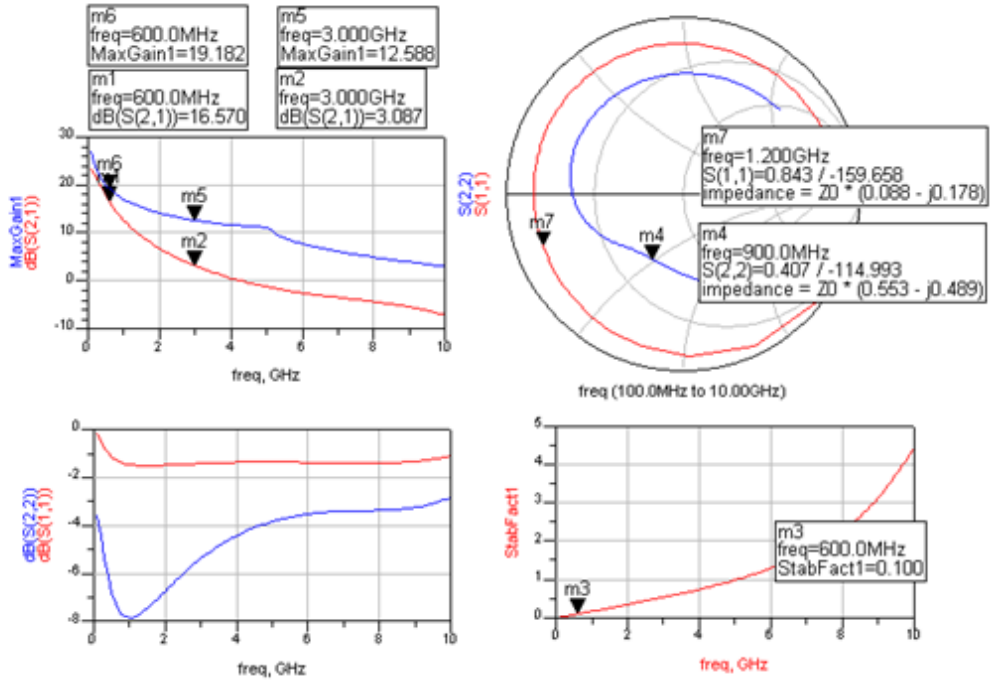



**Figure 6.6: S-parameter simulation.**

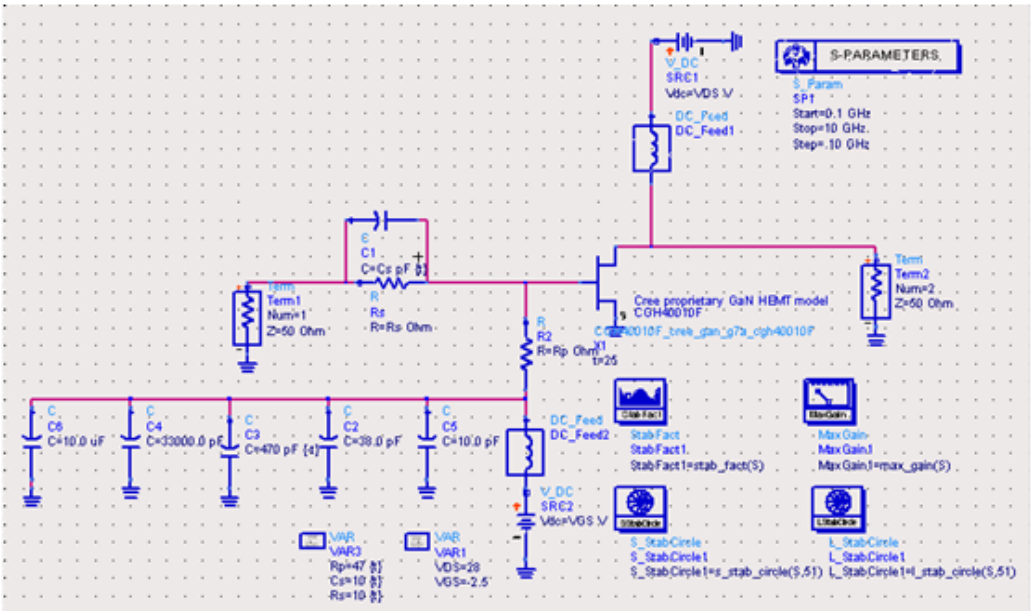



**Figure 6.7: Schematic of the stabilising circuit.**

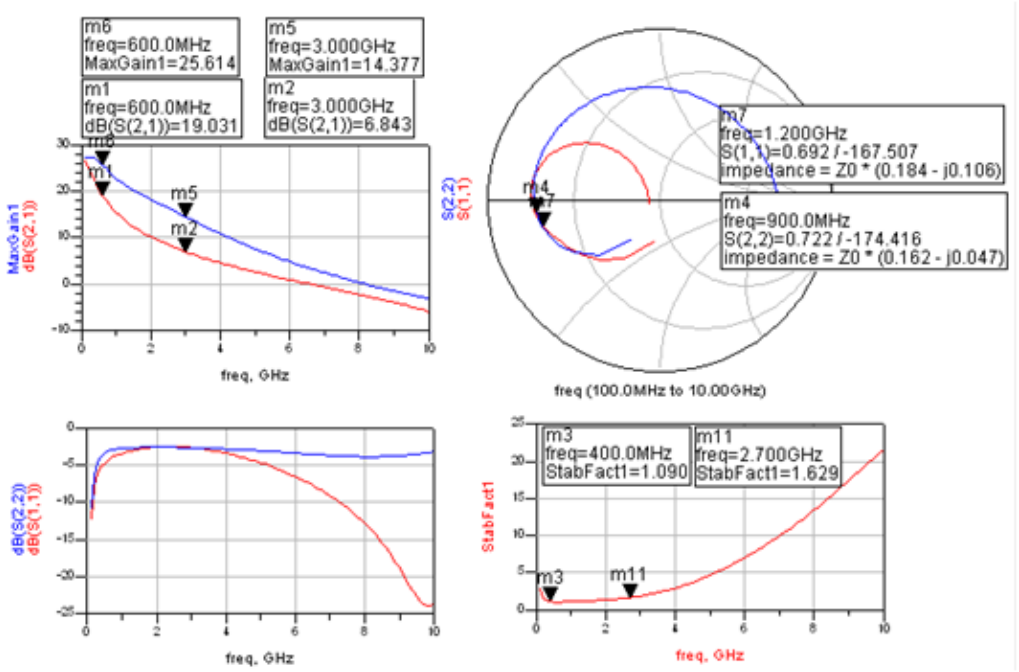



**Figure 6.8: S-parameter simulation for the stabilising circuit.**

nic loads for the three required PA modes of operation are shown in Table 6.2 for different modes of operation. The load-pull simulation has been performed for a class B biasing condition with a gate-source voltage of -2.4 V and drain-source voltage of 28 V.

**Table 6.2: OPTIMUM LOADS USING LOAD-PULL SIMULATION.**

| Freq (GHz) | 0.7 | 1.4 | 1.5 | 2.1 | 2.2 | 2.8 |
|---|---|---|---|---|---|---|
| $Z(f_s)$ ($\Omega$) Resistive loading class B | 39.4+ J21.4 | 23.8+ J17.0 | - | - | - | - |
| $Z(f_s)$ ($\Omega$) IPA mode | - | - | 26.5 + J44.0 | 23.5+ j18.3 | - | - |
| $Z(f_s)$ ($\Omega$) Class J | - | - | - | - | 13.65 + j12.2 | 14.35+ j2.65 |
| $Z(2f_s)$ ($\Omega$) | 50 - j0 | 50 + j0 | -10 + j10 | -10 + j10 | 0 + j60 | 0 + j150 |
| $Z(3f_s)$ ($\Omega$) | 50 - j0 | 50 + j0 | 0 - j10 | 0 - j30 | 0 + j0 | 0 - j0 |
| $Z(nf_s)$ ($\Omega$) | Shorted | Shorted | Shorted | Shorted | Shorted | Shorted |

## 6.3 PA Prototype Design

The PA prototype consists of two devices, a 10 W Cree (CGH40010F) device (main device) and a 6 W Cree (CGH40006PE) device (auxiliary device) where both were biased at pinch-off. Both devices will be designed to operate in a high efficiency mode according to the load-pull simulations. The design will start with the output network that connects both main and auxiliary PAs. After that, input matching will be designed for both devises.

### 6.3.1 Output Network Design

In this section we will show the design of the output network (highlighted in a box in Fig. 5.1) and consists of the combining network (Diplexer) and the matching circuitry for both the main and auxiliary devices.

#### 6.3.1.1 Combining Network Design

The combing network (diplexer) design is required to present an open circuit to the main device at the fundamental frequency when looking into the auxiliary device. The centre frequency for the combining network chosen is 1.8 GHz since it is in the mid-band of the targeted operating bandwidth (0.7-2.8 GHz). A high frequency laminate board from Roger corp. (TMM3) has been used in this design.

The design starts first with using a radial stub of length 18 mm to present a short at 1.8 GHz (Fig. 6.9). Next, a quarter-wavelength

line (25.8 mm) at 1.8 GHz has been employed to transform this short created by the radial stub into an open circuit at port 1 and 2. Also, the drain DC biasing circuit for the main device has been considered.

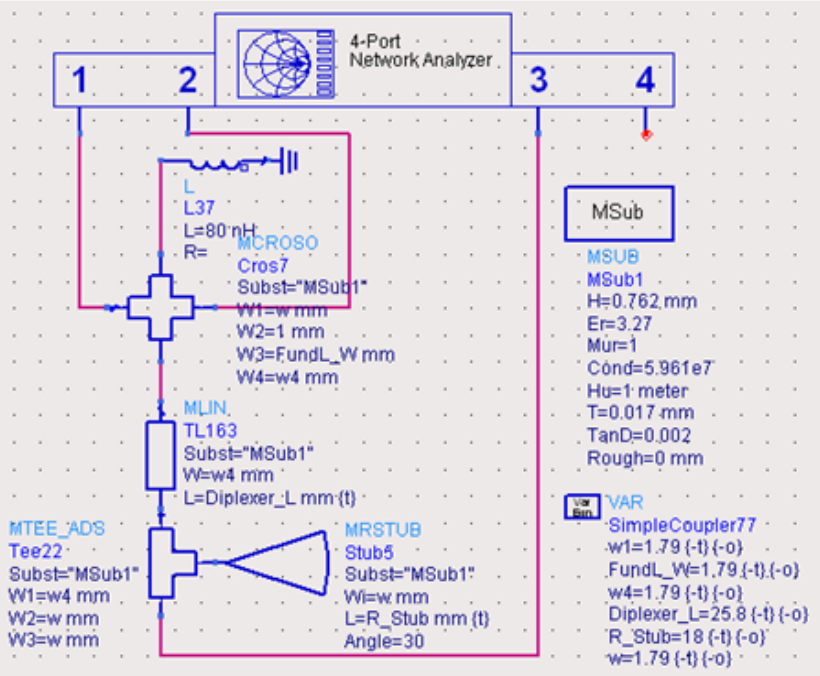



**Figure 6.9: Schematic of the diplexer network.**

Figure 6.10 shows the diplexer network performance where the input impedance of port 1 S(1,1) sees a 50 Ω load at 1.8 GHz. Consequently the forward transmission coefficient S(2,1) has its best results at 1.8 GHz and performance is degraded as the frequency deviates from the centre frequency of the design. The injection port S(1,3), sees high impedance for the frequency range of 1.2 GHz to 2.5 GHz and sees low impedance from 3.0 GHz to 5.5 GHz which is appropriate for the frequency range of the injection mode (3.0-4.2 GHz).

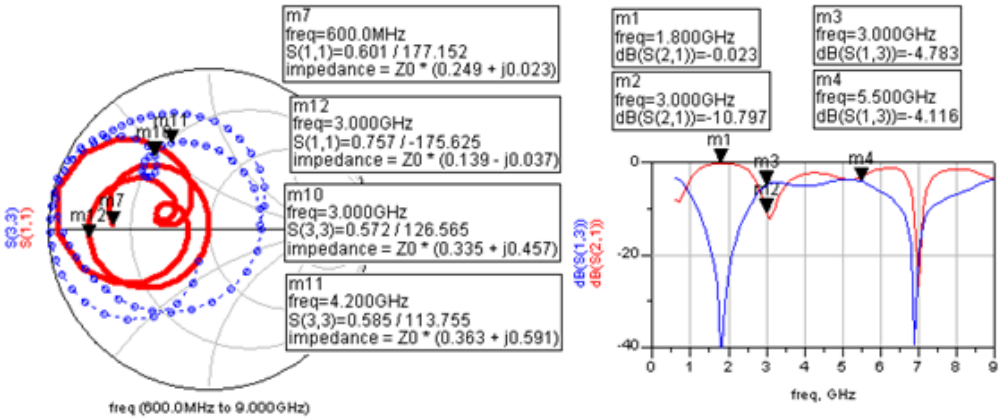



**Figure 6.10: S-parameter simulation for the diplexer network .**

#### 6.3.1.2 Output Matching Network

**A. Main Matching Network**

After the diplexer network design, the output matching network for the main device has been designed (Fig. 6.11) to present the required broadband fundamental impedance identified by load-pull simulation. However, with a complex design including a diplexer network, the matching was targeting a zone on the Smith chart around the optimum fundamental load rather than matching to the exact predefined loads. This is reasonable since the aim of the design is a high-efficiency wideband PA where a trade-off between bandwidth and efficiency must be considered.

Figure 6.12 shows the simulation results of the output network and it can be seen that the input impedance of port 1 is plotted on smith chart as S(1,1) indicated by dotted squared and the injection port (Port3) as S(3,3). S(1,1) presents a fundamental load impedance close to the load-pull simulation at the lower band and upper band

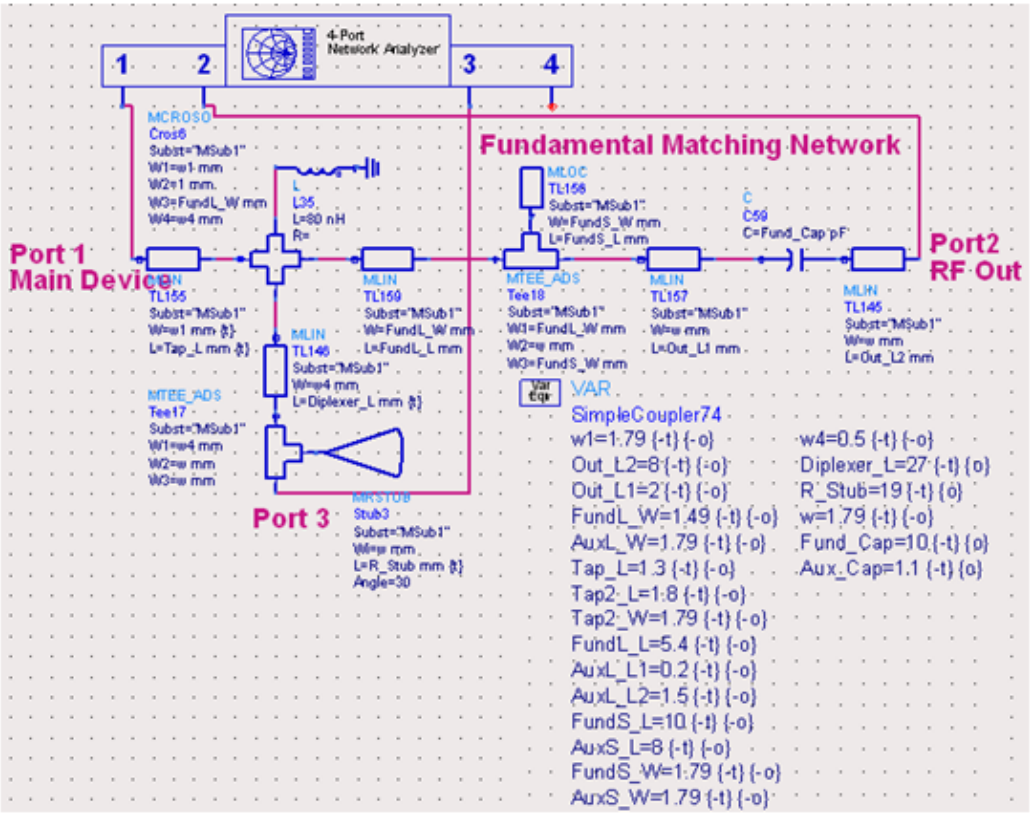



**Figure 6.11: Schematic of the output network with the fundamental matching network.**

but not at the mid band where IPA mode will be utilized to link the two modes of operation. Also, the forward transmission coefficients S(2,1) and S(1,3) shows a good broadband performance across 0.9-2.2 GHz and as the frequency reaches the edges of the operating bandwidth the performance is degraded.

### B. Auxiliary Matching Network

The input impedance looking from port 3 S(3,3) clearly presents a challenge for broadband matching the auxiliary device across 3.0-4.2 GHz where the impedance spans a relatively big circle (from 6 Ω to 65 Ω) around a 50 Ω Smith chart. This is mainly due to

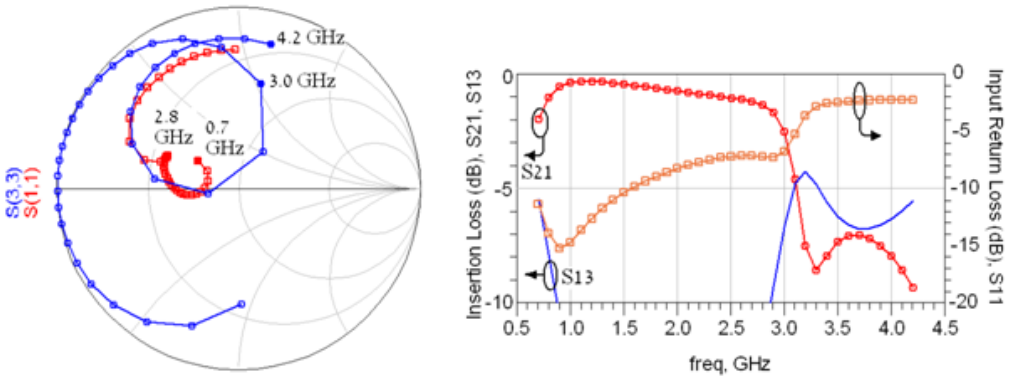



**Figure 6.12: S-parameter simulation for the output network including the fundamental matching network.**

the complex nature of the quarter wave transformer used in this design. Those impedances need to be matched to a fundamental load impedance spans from $Z_L = 12.57 + j23.1\ \Omega$ at 3 GHz to $Z_L = 9.44 + j11.68\ \Omega$ at 4 GHz (Appendix B).

A biasing circuit for the auxiliary PA and a tuning circuit (Fig. 6.13) have been added to match the input impedance S(3,3) of port 3 into an area closer to the centre of the smith chart across 3.0-4.0 GHz bandwidth as shown in Fig. 6.14.

The output network with output matching for both devices is shown in Fig. 6.15. Port 1 represents the port connected to the main device, port 2 is the RF out and port 3 is connected to the auxiliary device.

The simulation results of the output network are shown in Fig. 6.16. It can be seen, the fundamental impedance presented to the main device S(1,1) has fallen close to the required optimum loads, tabulated in Table 6.2, across the lower and upper band of the opera-

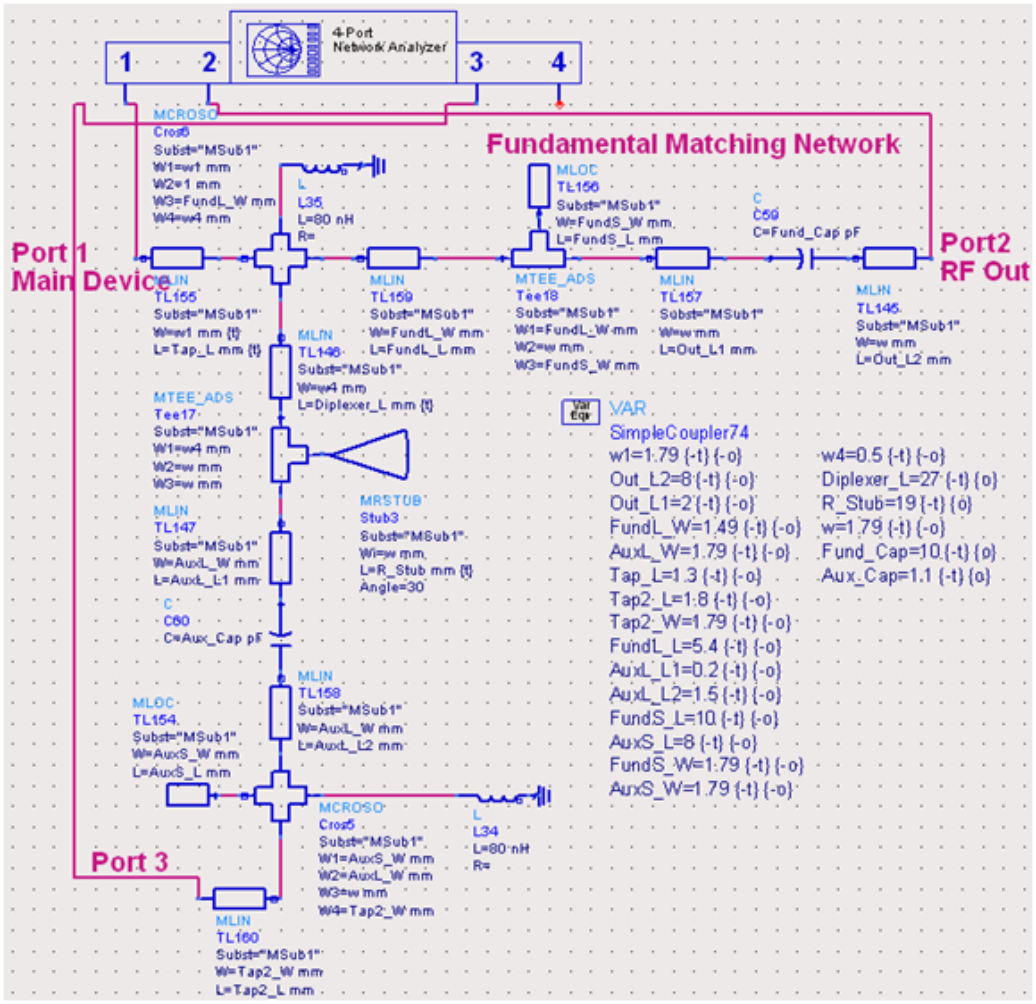



**Figure 6.13: Schematic of output network with matching networks.**

ting bandwidth. Though, in the mid band the imaginary part of the fundamental impedance does not stay in the inductive part of Smith chart, which will affect the PA performance in this band.

The input impedance S(3,3) looking from port 3, clearly presents a challenge for broad band matching for the auxiliary device across 3.0-4.2 GHz, especially in the upper band. Therefore, the injection mode window is not expected to operate perfectly across the desi-

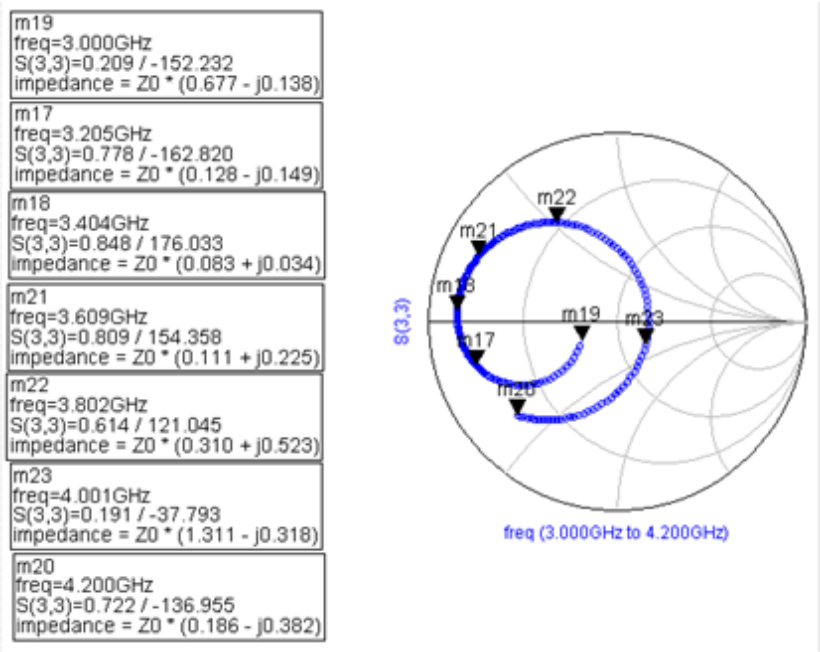



**Figure 6.14: S-parameter simulation of the input impedance of port 3.**

gned window (3.0-4.2 GHz).

### 6.3.2 Input Matching network

The input matching network for both PAs (Fig. 6.17, Fig. 6.18) has been conjugately matched at the maximum operating frequency to improve the gain at the upper band.

### 6.3.3 PA Simulation Results

#### 6.3.3.1 Simulation Results

A complete structure as proposed in Fig. 4.2 including a coupler, doubler and band pass filter (Appendix E) has been simulated and the expected stability of the PA is shown in Fig. 6.19.

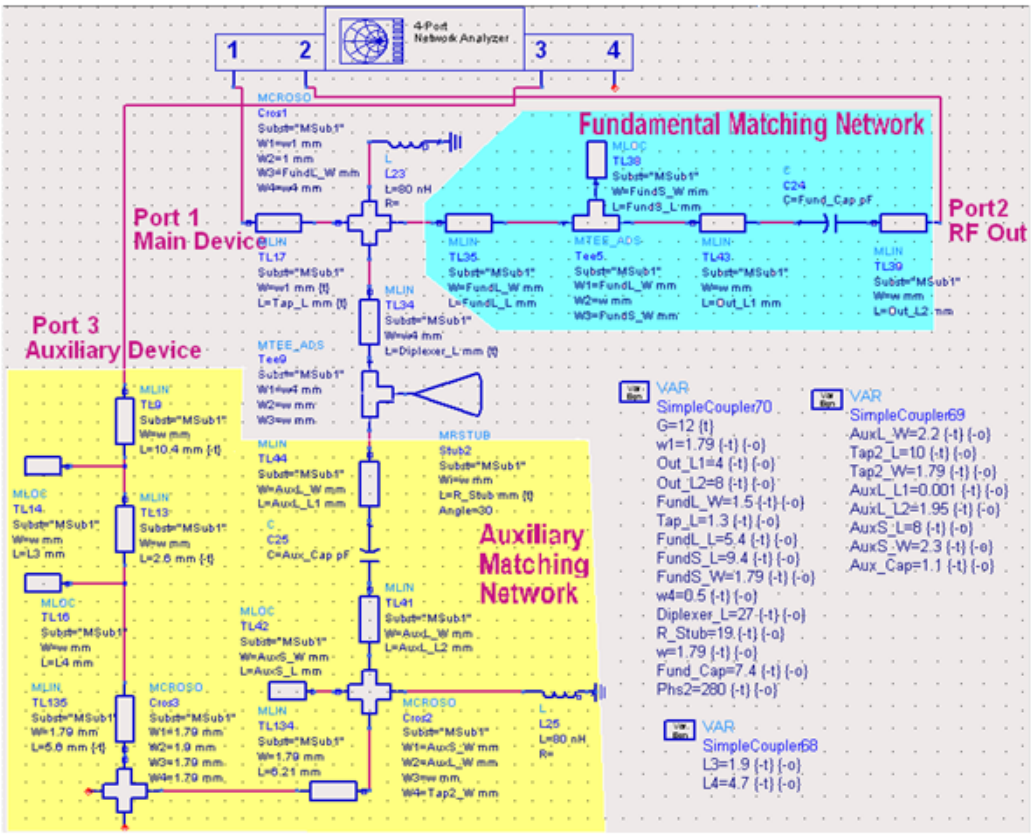



**Figure 6.15: Schematic of the output network.**

The stability spec. of this project is a k-factor greater than 1.1 to insure the unconditional stability of the PA (Fig. 6.19).

#### 6.3.3.2 Momentum Simulation

The design then has been simulated by momentum simulation and optimized. The simulation results are shown in Fig. 6.25 where a PAE > 50% is calculated across 4:1 bandwidth (0.68 - 2.72 GHz) with an output power is equal to or greater than the rated power of a 10 W device.

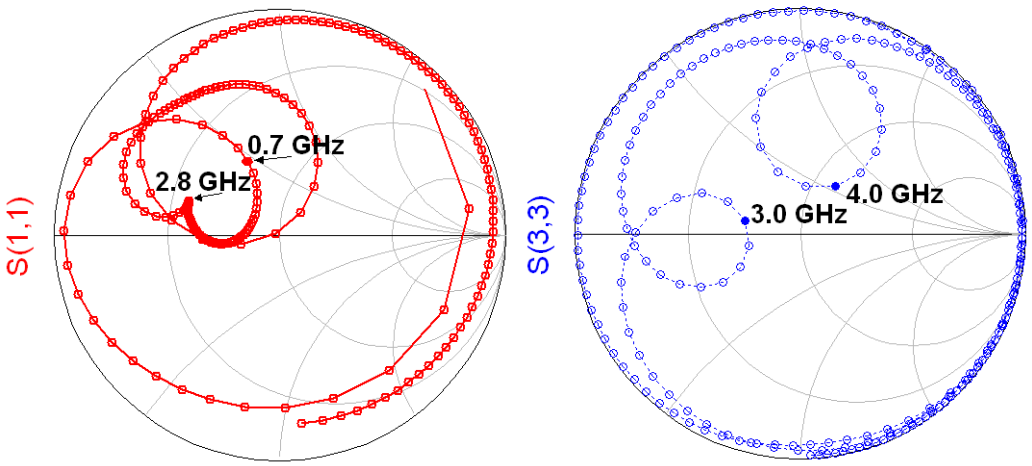



**Figure 6.16: S-parameter simulation of the output network.**

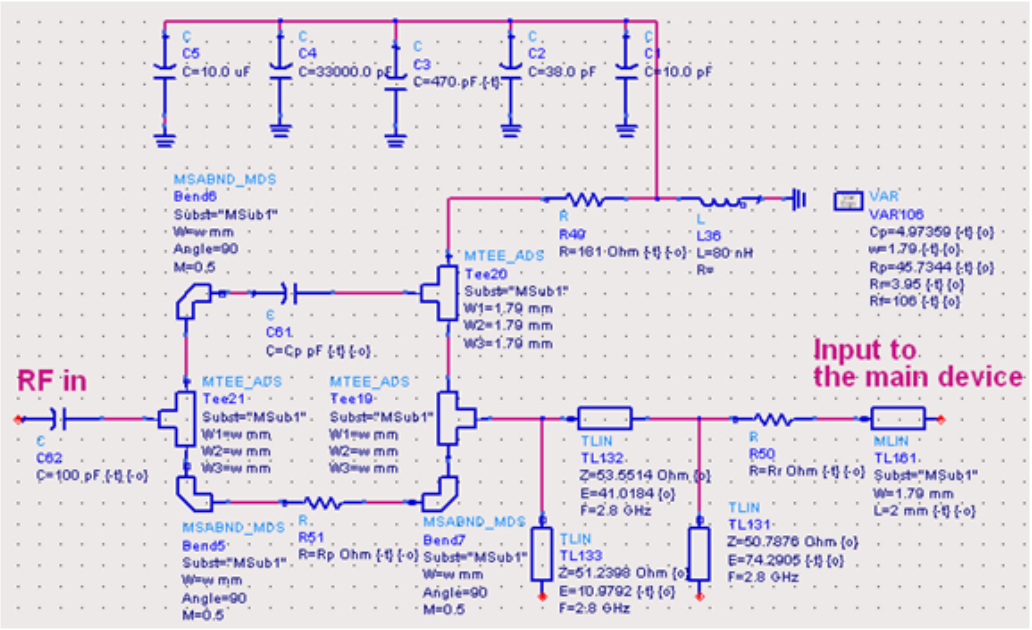



**Figure 6.17: Schematic of input match for the main device.**

## 6.3.4 PA Prototype Measurement

### 6.3.4.1 PA Structure

The power amplifier prototype is a hybrid design where commercially available components will be used for a proof of design concept.

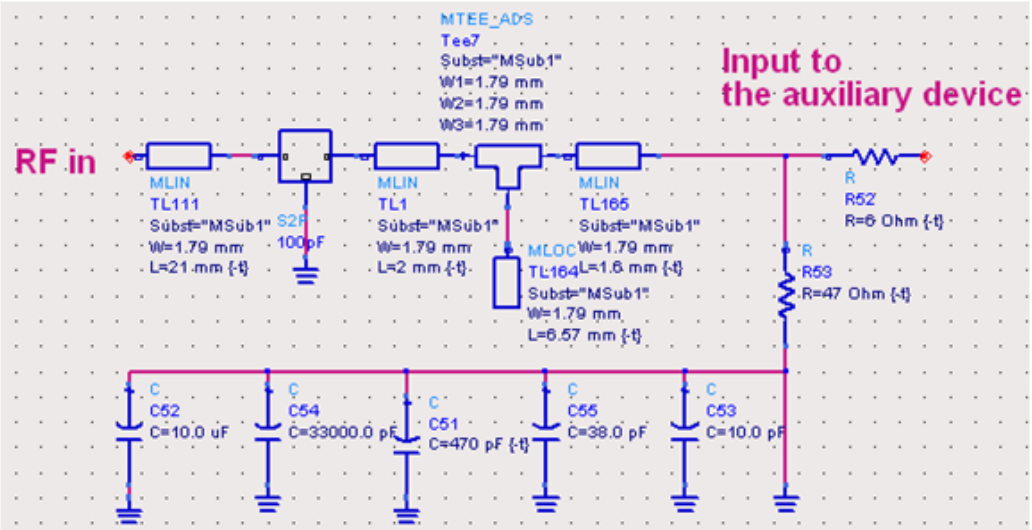



**Figure 6.18: Schematic of input match for the auxiliary device.**

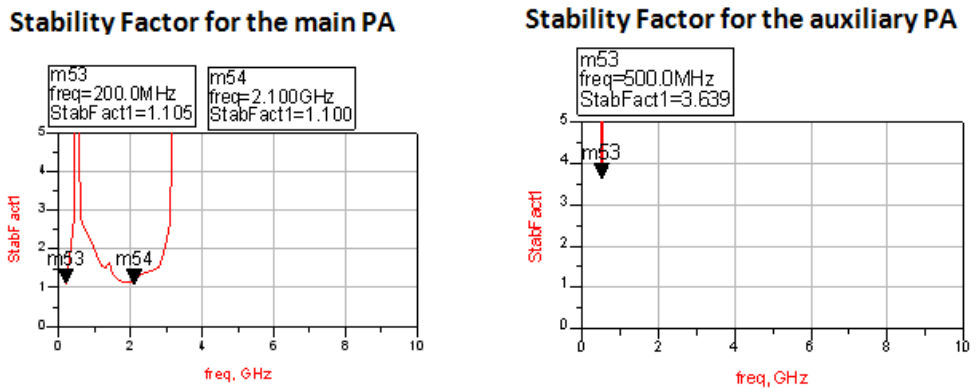



**Figure 6.19: Simulation of stability factor of complete structure.**

The PA prototype is shown in Fig. 6.20 where the main and auxiliary devices with their matching networks are mounted on one board. While the other components will be a set alone off-the-shelf components commercially available like couplers, filters and frequency doublers. In Fig. 6.20, the main device (10 W) is in the middle of the PA and the auxiliary device (6 W) is in the lower side of the PA. The board used is a high frequency laminate board (TMM3) from Ro-

gers Corp. mounted on an Aluminium base metal with dimensions of 61.5x76.5 mm.

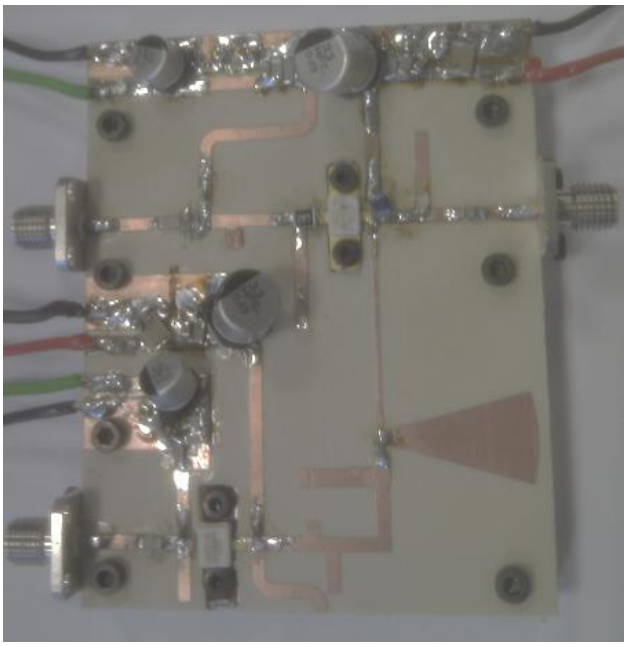


**Figure 6.20: Realised PA prototype.**

#### 6.3.4.2 PA Measurement

The first test was a stability test, and the realised PA has successfully passes the test that was performed using a spectrum analyzer. Secondly, the PA performance was measured across the bandwidth (0.6-2.8 GHz) where the output power is measured by spectrum analyzer (Agilent N1996A).

The measured results for a complete structure (Fig. 6.21) are shown in Fig. 6.25. The passive doubler used is from Marki Microwave (D99210) and the PA driver is an off-the-shelf component.

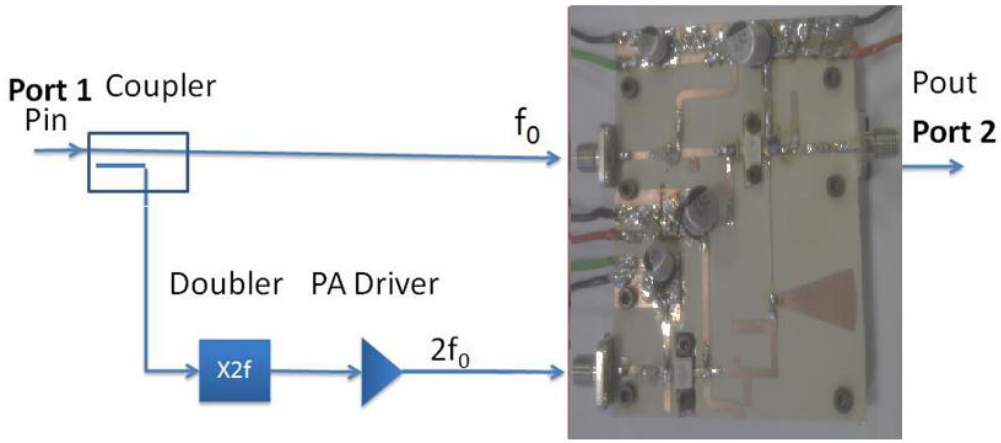



**Figure 6.21: Full structure PA prototype.**

The PA performance at each band is measured; Fig. 6.22 shows the input, output power, Drain Efficiency (DE), TDE and PAE at 0.7 GHz. Where PAE includes all the DC power of the structure, i.e.;

$$PAE = \frac{P_{rf} - P_{in}}{P_{dc\ Main} + P_{dc\ Aux}}$$

The measured PAE at P1dB is in the mid 50s% and output power is

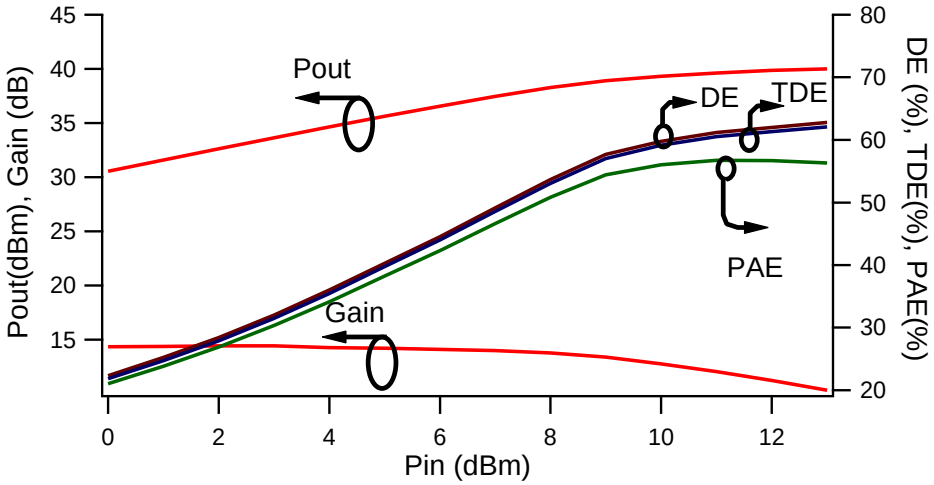



**Figure 6.22: Measured results of the PA prototype at 0.7 GHz.**

around the rated output power 40 dBm.

Figure 6.23 shows the performance at 1.6 GHz (mid band); this is the window where IPA mode is active. The drain efficiency at P1dB is in the mid 80s%, while the TDE (i.e., DE including DC power of the auxiliary device) is above 80% and PAE is in mid 70%. The output power in this mode has increased up to 42.9 dBm; this is a difference of almost 2.9 dB from the lower band. The reason is that in the lower band, a resistive class B mode is utilized and that reduces the output power by 0.9 dB (as been discussed in Chapter 5); while in the mid band, the output power of the IPA mode is ideally expected to be increased by 1.5 dB. However, this gain difference between these modes was described in Chapter 5, thus, this PA design did not consider a flat gain design.

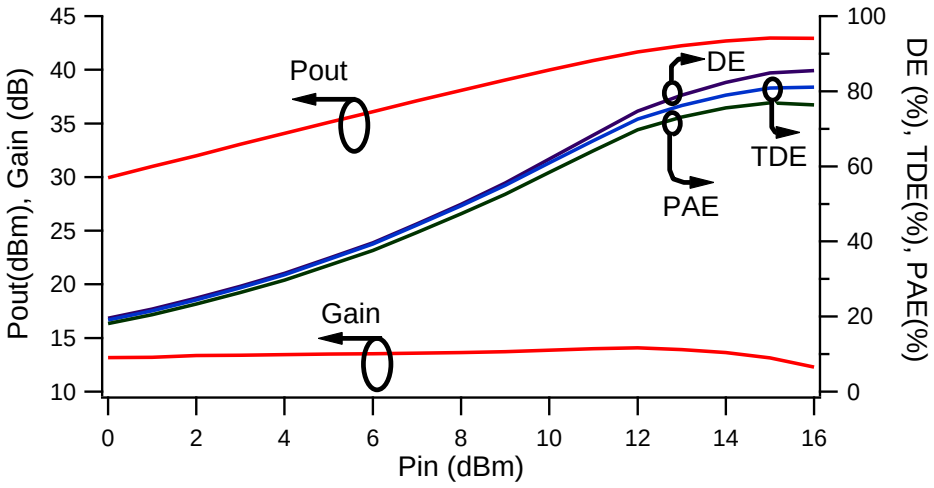



**Figure 6.23: Measured results of the PA prototype at 1.6 GHz.**

At 2.4 GHz (upper band), the performance of the PA is shown in Fig. 6.24. The PAE is above the 50s% and output power is 41.9 dB.

It is worth mentioning that there is a very small measured DC power of the auxiliary device at the upper band and that reduces DE by 2%.

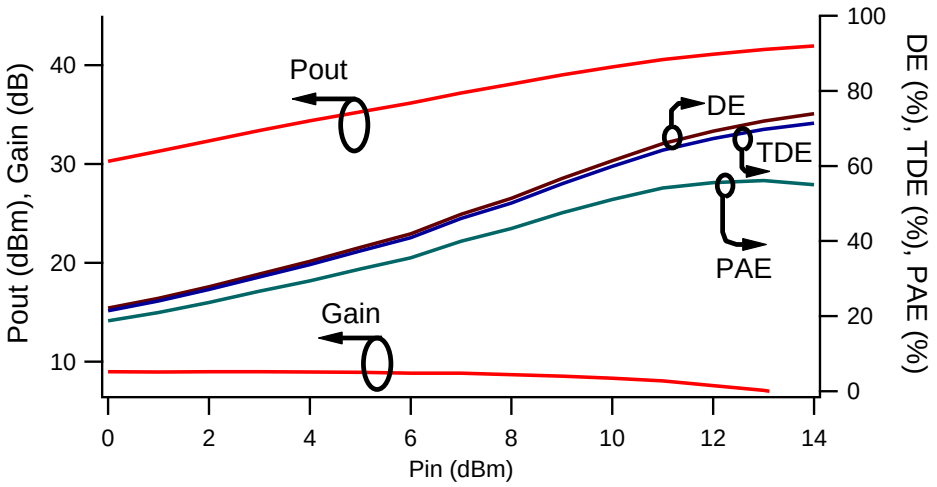



**Figure 6.24: Measured results of the PA prototype at 2.4 GHz.**

Figure 6.25 shows that the PA achieved a performance of PAE > 50% measured at 1 dB compression point for a bandwidth of greater than 4:1. The measured results are relatively close to the simulation results but with a shifted frequency window from the original design of (0.68 -2.72 GHz) to (0.63-2.56 GHz). In addition, the measured performance improved at the mid band while at the upper band degraded. Also, the gain differs from the simulation and that is most likely due the input matching network.

Figure 6.26 compares the performance of the PA in the injection mode to the case when no injection is applied. The PAE has improved in most of the injection window, the highest is at 1.6 GHz with 19% enhancement and the worst case is at 1.7 GHz where there was not any improvement. As been discussed earlier, this is due to the

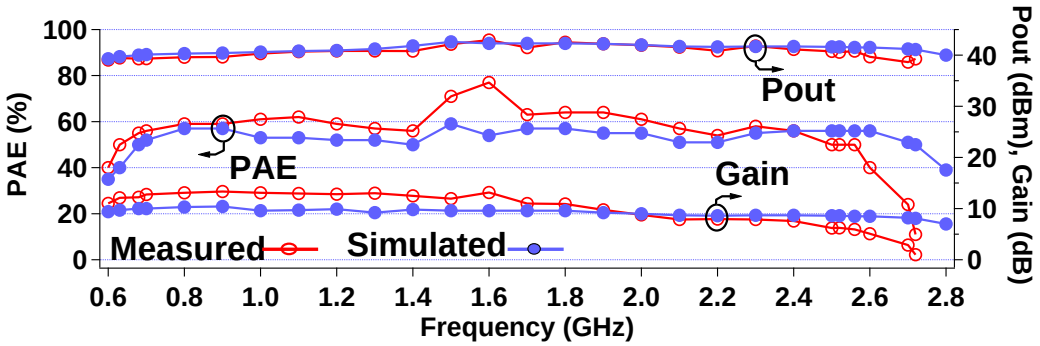



**Figure 6.25: Simulated and measured results of the PA prototype showing PAE, Pout and gain.**

nature of the combining network which makes the matching for the auxiliary device difficult across the whole bandwidth in the injection window.

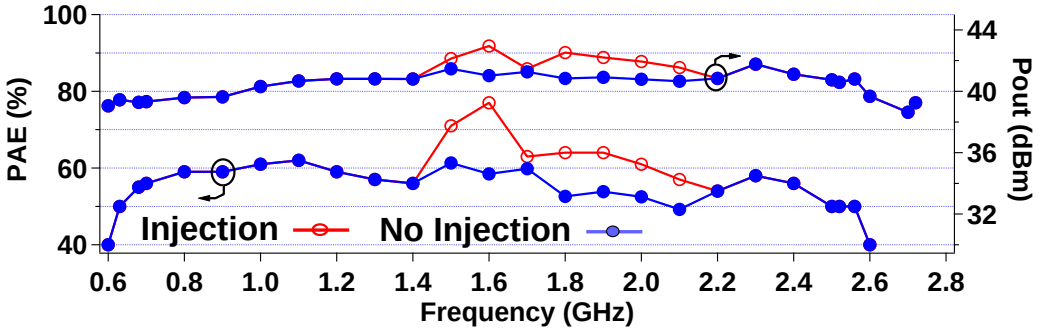



**Figure 6.26: The measured results of applying injection and no injection mode of the PA prototype showing PAE and Pout.**

The measured harmonic powers relative to the fundamental are shown in Table 6.3. The performance ranges from high harmonic power levels at the lower band to the low harmonic power levels in the upper band. The relatively high harmonic power levels at the lower band are a direct consequence of the resistive harmonic terminations. The measured performance at the resistively loaded

class B is comparable to the analysis presented in Sec. 5.2. The harmonic levels in the injection window (1.6 GHz) are less than 22 dBc and at Class J (2.4 GHz) the power levels are less than 48 dBc due to the reflective network presented to the harmonics of the upper band.

**Table 6.3: Measured Harmonic Power Relative to Fundamental Power.**

| Freq (GHz) | 0.7 | 1.0 | 1.6 | 2.4 |
|---|---|---|---|---|
| 2nd Harmonic (dBc) | -11 | -15 | -22 | -48 |
| 3rd Harmonic (dBc) | -13 | -25 | -30 | -50 |

A two-tone linearity measurement at 1.6 GHz is shown in Fig. 6.27. It can be seen that the IMD3 and IMD5 at P1dB point are smaller than -20 dBc for 1.6 GHz. However, the worst case is at 0.7 GHz (resistively loaded class B) where the IMD3 is -12 dBc; this is expected since the second and third harmonic impedances lie in the operating fundamental bandwidth of the PA (Fig. 6.28).

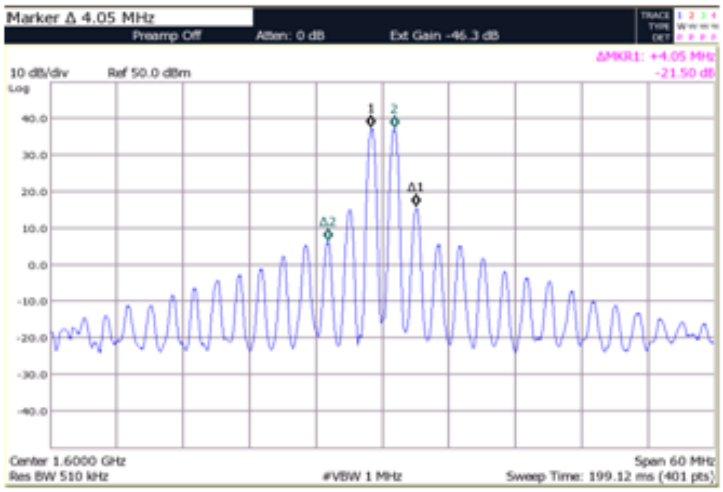



**Figure 6.27: Linearity measurement at 1.6 GHz.**

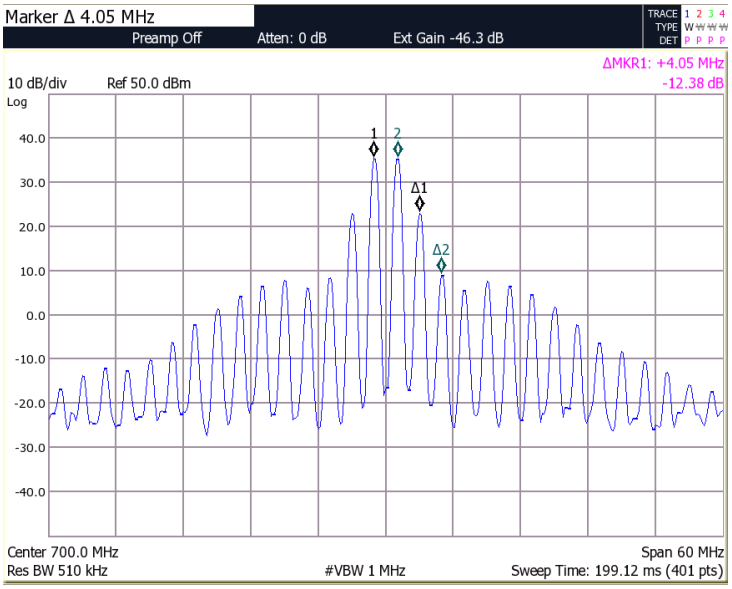



**Figure 6.28: Linearity measurement at 0.7 GHz.**

## 6.4 Summary

A high efficiency (PAE >50%) broad band (double-octave) PA prototype is designed according to the proposed multi-mode operation in **Chapter 5**. A conceptual system for the output network has been described to allow the multi-mode operation. The trade-off between linearity, efficiency, gain and power was established to achieve high efficiency over a broad bandwidth. The PA prototype is designed considering a practical realization of the proposed multi-mode PA. First, to reduce the challenges associated with the design of the multiplexer and fundamental matching of the auxiliary device, the bandwidth of the injection mode is reduced. Second, an optimization process of the output network was considered to achieve a double octave bandwidth of PAE >50%.

# *Chapter 7*

# Conclusions and Future Work

## 7.1 Conclusions

This research was undertaken to investigate the low efficient energy consumption aspect of communication systems. In particular, RF PAs which consume a large amount of energy that is supplied to RF transmitters. In this investigation, both narrowband and wideband PA design was considered for high efficient operation.

A novel power amplifier mode was introduced based on finding efficient voltage and current waveforms. The outcome shows that these waveforms require negative harmonic impedances at even harmonics. The research suggested an active harmonic injection for this mode. Investigation on this new mode showed that the drain efficiency of this mode was 95.2%.

The wideband operation of the IPA mode was investigated. Due to the limitation of technical circuit technology where broadband circulators are not available, a multi-mode wideband design was proposed that integrates IPA mode with class B/J to extend the operating bandwidth.

Following the introductory chapter, **Chapter 2** presented the essential background for PA classes and introduced a novel power amplifier mode termed IPA. IPA was based on presenting a negative harmonic impedance to realize highly efficient waveforms; this required an auxiliary PA to inject harmonic power to the main PA. The injected harmonic power was low relative to the main PA. The analysis on this mode showed that this IPA mode has a potential for high efficiency operation. Further analysis on optimizing IPA mode for real devices showed that this mode has a curvy RF load line shape which allows a designer to take advantage of the knee effect shape; this resulted in higher efficiency figures.

**Chapter 3** concerned about validating the theoretical part of IPA mode. An active load-pull measurement system was used to emulate a negative harmonic impedance to a PA operating under real conditions. The captured terminal I-V waveforms were in agreement with IPA theory. In this chapter, measurement results were compared to the theoretical expectation. The outcome of the analysis on output power, efficiency considering knee effect calculation validated the theoretical part of IPA mode presented in **Chapter 2**. The extracted RF current and voltage waveforms from the load-pull measurement were utilized in the development of the IPA mode in **Chapter 4**.

An IPA prototype design is initiated in **Chapter 4** based on the captured waveform measurement. A practical realization circuit of the IPA structure is proposed. The structure uses a coupler and passive doubler to input the second harmonic signal into an auxiliary PA to perform the required waveform shaping at the output of the

main PA. The diplexer circuit is based on quarter wavelength transmission lines. The output matching network and the diplexer were designed to present the harmonic impedance collated from active load-pull waveform measurements. ADS software was used to design an IPA prototype and perform optimization on the output network. The measured results of the IPA prototype showed a PA with a high linear efficiency reaching up to 80% of total drain efficiency at a modest compression point of only 1 dB. This work did not consider the efficiency of the driver stage as it acted as a proof of concept for IPA design. In addition, the RF power of the driver stage is an off-the-shelf PA and its power is very low; its output power is only a very small fraction of the RF output power of the PA. The measured results in terms of output power and efficiency are comparable with the theory and validation measurement taking into account the losses of the output network.

**Chapter 5** starts the second part of the thesis concerned about wideband design. A novel multi-mode PA design was proposed to design a highly efficient PA for a double-octave bandwidth. This chapter started by explaining the reason behind the limitation of high efficient operation across a broad bandwidth. As described, the highly reflective output network of a PA will prevent high efficiency operation beyond an octave bandwidth. The proposed approach considers passive and active harmonic injection that integrates IPA mode with class B/J modes.

In **Chapter 6**, a multi-mode high efficient PA for a double-octave bandwidth was designed and built. The chapter started with a concep-

tual system model for the required response of the output matching network to allow multi-mode operation. The objective of the wideband design was to show a proof of concept to a multi-mode PA for a multi-octave bandwidth with $PAE > 50\%$ at the P1dB compression point. The measured results showed that a wideband high efficiency PA can be designed to go beyond an octave bandwidth. The measured results have achieved a double-octave bandwidth for $PAE$ >50%. The linearity measurement at the resistive harmonic environment adopted in the lower band of the multi-mode PA are comparable to published work for the same harmonic conditions.

In conclusion, the power amplifier injection mode has been studied, analyzed, validated, designed and built. The circuits that allows such mode was designed for narrowband operation. However, due to the lack of enabling technology for broadband combining network, a compromise of multi-mode operation is considered. The novel multi-mode PA shows a promising candidate for wideband high efficient PAs.

## 7.2 Future Work

This research has shown the proof of concept of IPA mode; both the narrowband PA prototype and the IPA mode integration into a multi-mode PA design have been designed and built. This work can be further investigated for scalability in both power and frequency. The PA prototype presented in this thesis is mainely designed around a 10 W GaN device, scalability for higher power would be important

to see how IPA mode can improve efficiency in high power devices with higher device capacitance and compare class B operation to IPA mode.

In future investigations it might be possible to design a full IPA structure on a Monolithic Microwave Integrated Circuit (MMIC) level where all components are integrated in one unit. This allows for more optimization of the input transmission lines for broadband operation. The design could also considers either a passive or active doubler. If an active doubler design is being considered then that will reduce the need for the additional PA driver; however, an efficient active doubler is required. Also, the use of a band limiting doubler would cancel the need for a band pass filter.

Additionally, the diplexer network itself needs to be investigated and redesigned particularly for broader bandwidth. This is an important issue for future research.

Furthermore, the linearity aspect of the IPA mode has not been discussed in the design of both narrow and wide band design. This can be further analyzed considering modulated signals for communication applications.

Moreover, a flat gain for a multi-mode wideband design can be studied and improved by adapting new design strategies to achieve this target including trade-off between gain and bandwidth.

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# Appendices

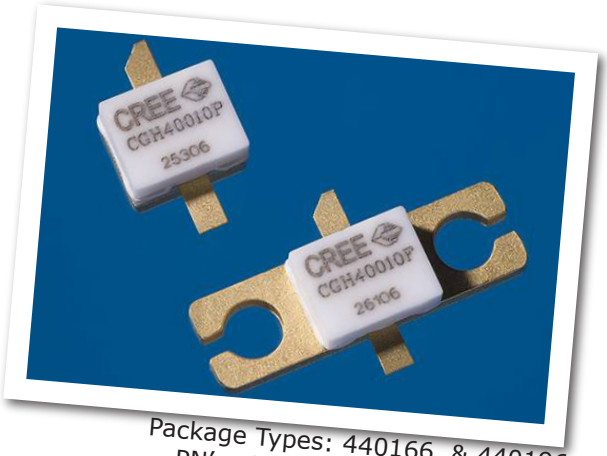
# *Appendix A*

# Cree GaN HEMT (CGH40010F) Device Data Sheet

# CGH40010

## 10 W, RF Power GaN HEMT

Cree's CGH40010 is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). The CGH40010, operating from a 28 volt rail, offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making the CGH40010 ideal for linear and compressed amplifier circuits. The transistor is available in both screw-down, flange and solder-down, pill packages.




Package Types: 440166, & 440196
PN's: CGH40010F & CGH40010P

### FEATURES

- Up to 6 GHz Operation
- 16 dB Small Signal Gain at 2.0 GHz
- 14 dB Small Signal Gain at 4.0 GHz
- 13 W typical $P_{SAT}$
- 65 % Efficiency at $P_{SAT}$
- 28 V Operation

### APPLICATIONS

- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, Linear amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA waveforms

RoHS COMPLIANT

PRELIMINARY
Rev 2.0 – December 2008

Large Signal Models Available for SiC & GaN

## Absolute Maximum Ratings (not simultaneous) at 25˚C Case Temperature

| Parameter | Symbol | Rating | Units |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | 84 | Volts |
| Gate-to-Source Voltage | $V_{GS}$ | -10, +2 | Volts |
| Storage Temperature | $T_{STG}$ | -55, +150 | ˚C |
| Operating Junction Temperature | $T_J$ | 175 | ˚C |
| Maximum Forward Gate Current | $I_{GMAX}$ | 4.0 | mA |
| Soldering Temperature[1] | $T_S$ | 245 | ˚C |
| Screw Torque | $\tau$ | 60 | in-oz |
| Thermal Resistance, Junction to Case[2] | $R_{\theta JC}$ | 5.0 | ˚C/W |
| Case Operating Temperature[2,3] | $T_C$ | -10, +105 | ˚C |

Note:
[1] Refer to the Application Note on soldering at www.cree.com/products/wireless_appnotes.asp
[2] Measured for the CGH40010F at $P_{DISS}$ = 14 W.
[3] See also, the Power Dissipation De-rating Curve on Page 6.

## Electrical Characteristics ($T_C$ = 25˚C)

| Characteristics | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **DC Characteristics[1]** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | -3.8 | -3.3 | -2.3 | VDC | $V_{DS}$ = 10 V, $I_D$ = 3.6 mA |
| Gate Quiescent Voltage | $V_{GS(Q)}$ | – | -3.0 | – | VDC | $V_{DS}$ = 28 V, $I_D$ = 200 mA |
| Saturated Drain Current | $I_{DS}$ | 2.9 | 3.5 | – | A | $V_{DS}$ = 6.0 V, $V_{GS}$ = 2.0 V |
| Drain-Source Breakdown Voltage | $V_{BR}$ | 84 | 100 | – | VDC | $V_{GS}$ = -8 V, $I_D$ = 3.6 mA |
| **RF Characteristics[2] ($T_C$ = 25˚C, $F_0$ = 3.7 GHz unless otherwise noted)** | | | | | | |
| Small Signal Gain | $G_{SS}$ | 12.5 | 14.5 | – | dB | $V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA |
| Power Output[3] | $P_{SAT}$ | 10 | 12.5 | – | W | $V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA |
| Drain Efficiency[4] | $\eta$ | 55 | 65 | – | % | $V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA, $P_{SAT}$ |
| Output Mismatch Stress | VSWR | – | 10 : 1 | – | Ψ | No damage at all phase angles, $V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA, $P_{OUT}$ = 10 W CW |
| **Dynamic Characteristics** | | | | | | |
| Input Capacitance | $C_{GS}$ | – | 5.00 | – | pF | $V_{DS}$ = 28 V, $V_{gs}$ = -8 V, f = 1 MHz |
| Output Capacitance | $C_{DS}$ | – | 1.32 | – | pF | $V_{DS}$ = 28 V, $V_{gs}$ = -8 V, f = 1 MHz |
| Feedback Capacitance | $C_{GD}$ | – | 0.43 | – | pF | $V_{DS}$ = 28 V, $V_{gs}$ = -8 V, f = 1 MHz |

Notes:
[1] Measured on wafer prior to packaging.
[2] Measured in CGH40010-TB.
[3] $P_{SAT}$ is defined as $I_G$ = 0.36 mA.
[4] Drain Efficiency = $P_{OUT}$ / $P_{DC}$





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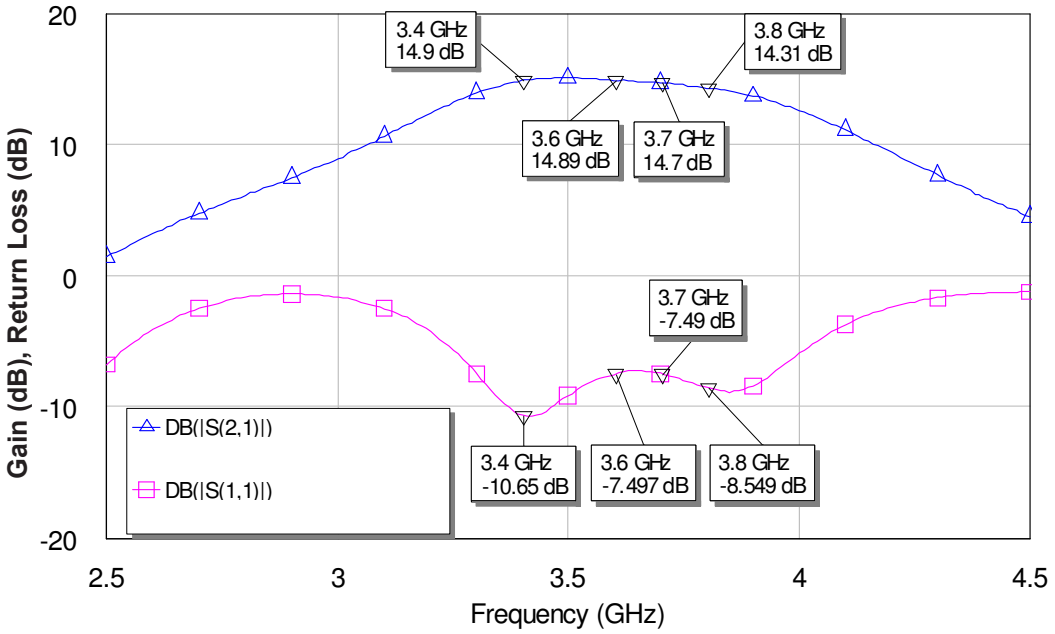
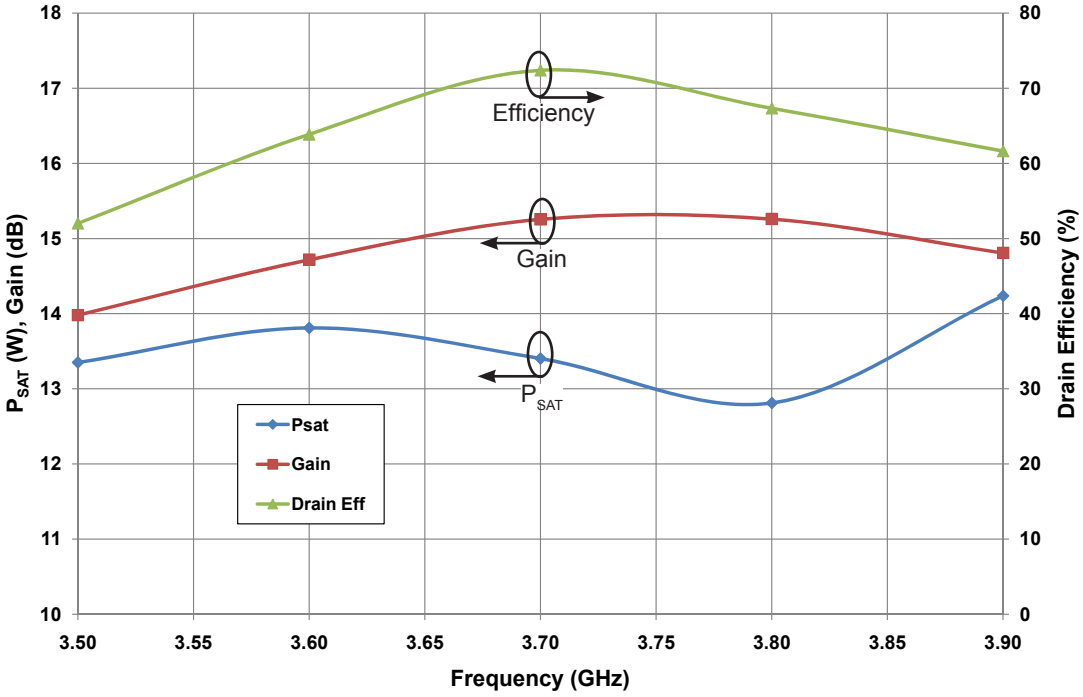
## Typical Performance

**Small Signal Gain and Return Loss vs Frequency of the CGH40010 in the CGH40010-TB**




**$P_{SAT}$, Gain, and Drain Efficiency vs Frequency of the CGH40010F in the CGH40010-TB**
**$V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA**



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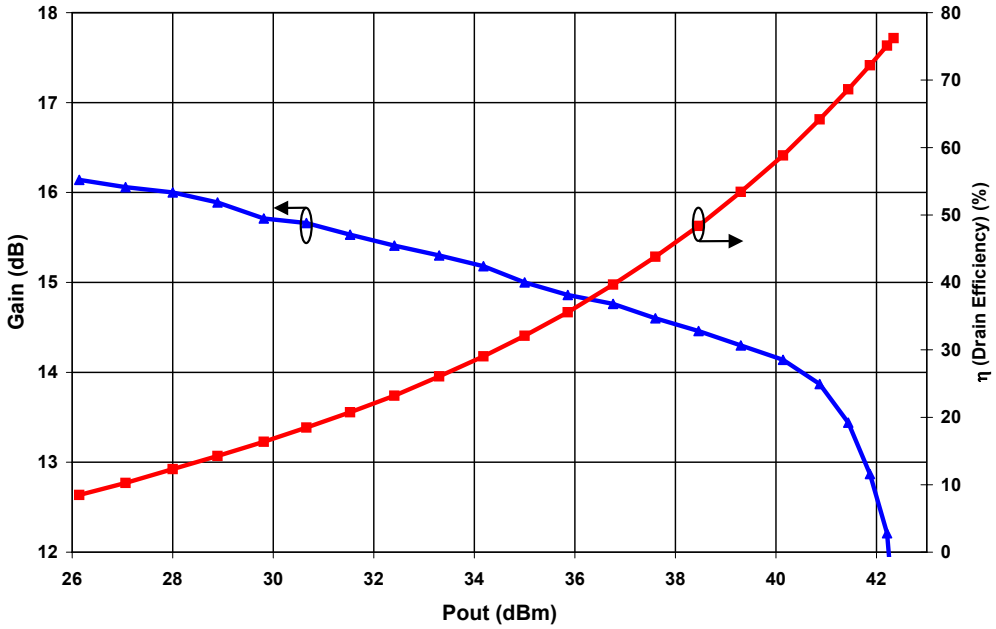
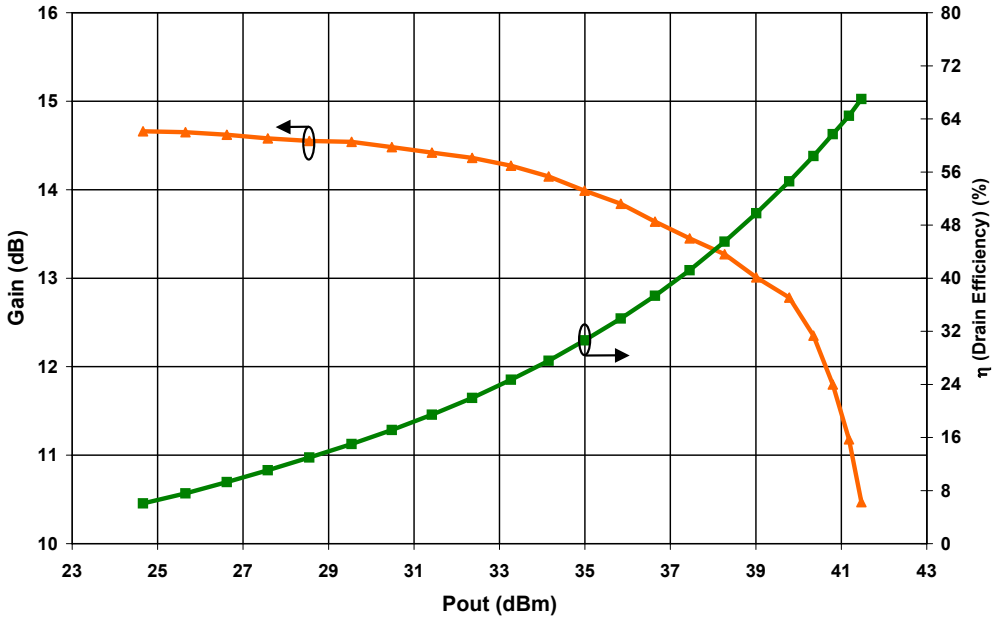
## Typical Performance

**Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for Drain Efficiency at 2.0 GHz**
**$V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA, Freq = 2.0 GHz**




**Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for Drain Efficiency at 3.6 GHz**
**$V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA, Freq = 3.6 GHz**



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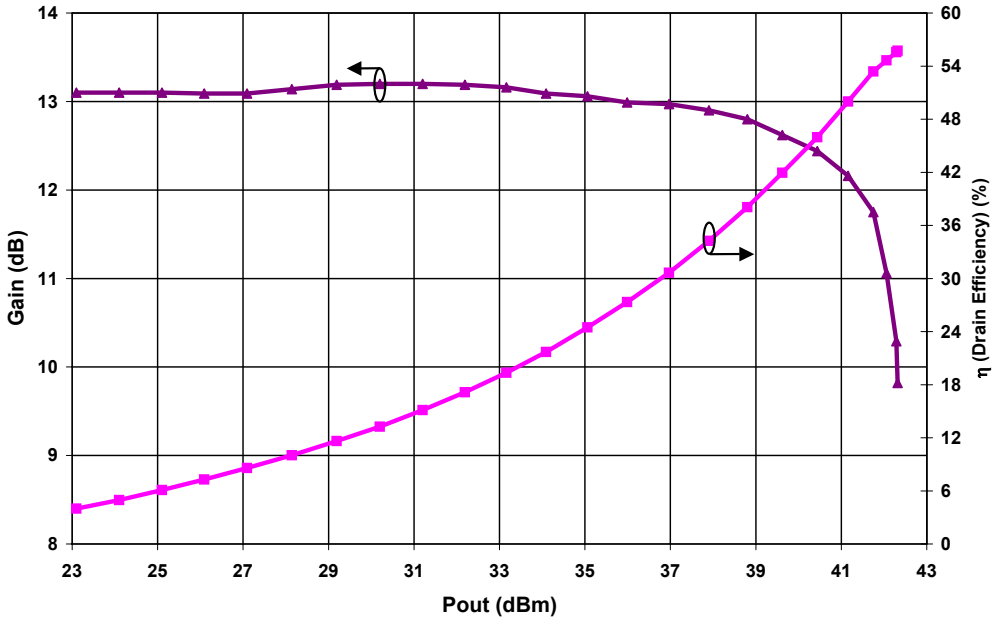
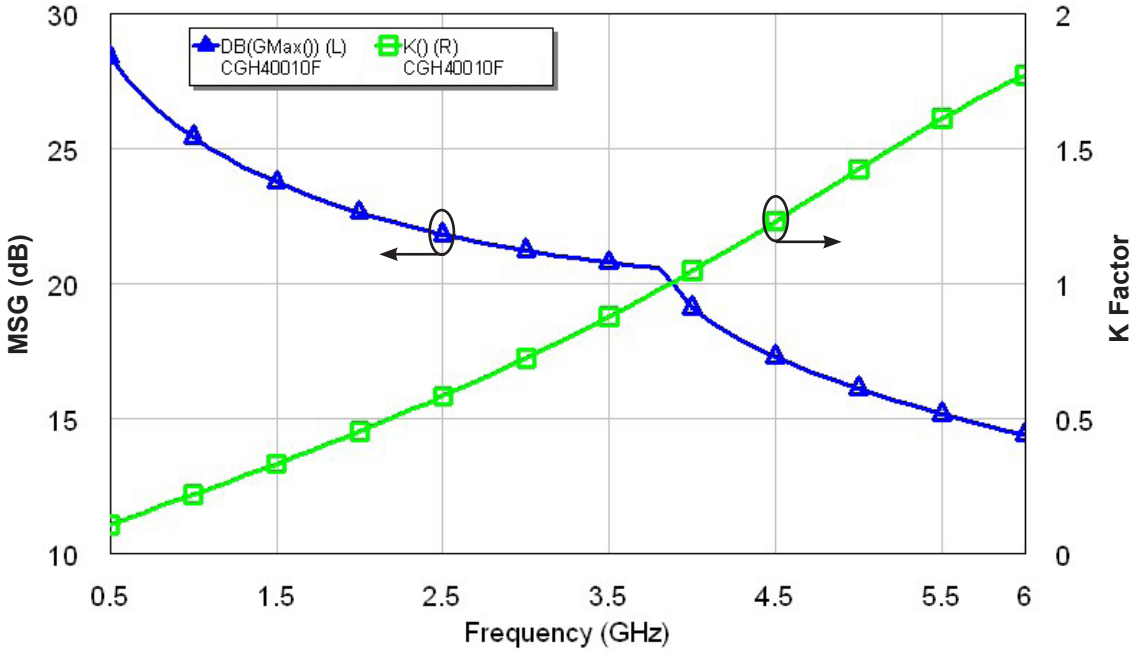
## Typical Performance

**Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for P1 Power at 3.6 GHz**
**$V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA, Freq = 3.6 GHz**




**Simulated Maximum Stable Gain, Maximum Available Gain and K Factor of the CGH40010F**
**$V_{DD}$ = 28 V, $I_{DQ}$ = 200 mA**



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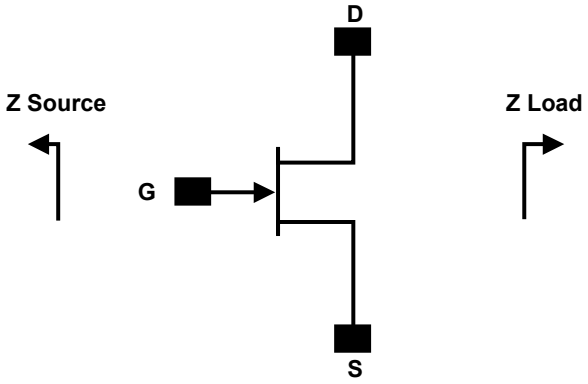
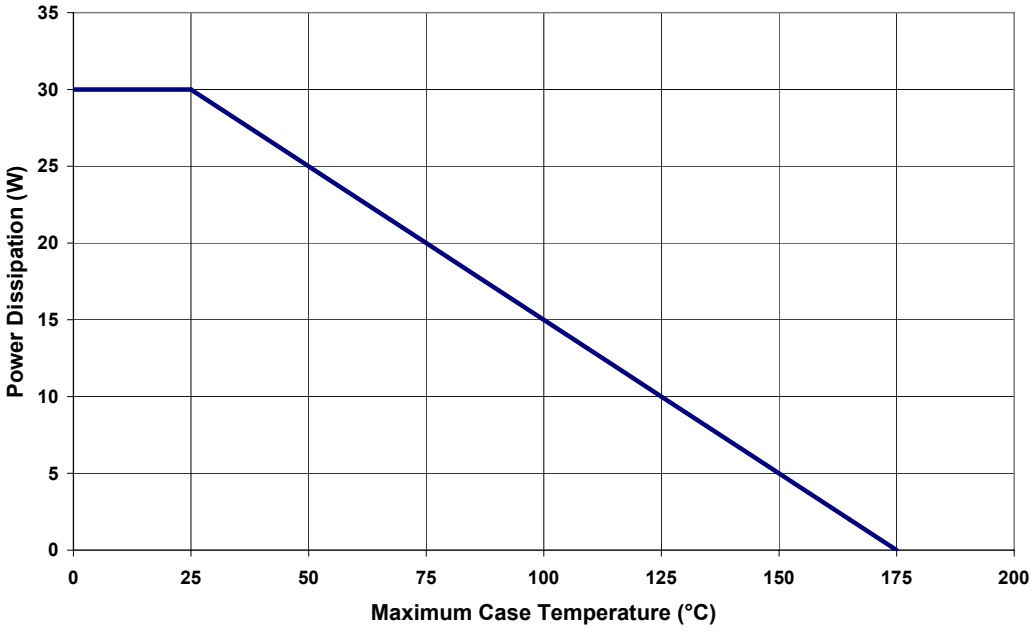
## Source and Load Impedances




| Frequency (MHz) | Z Source | Z Load |
|---|---|---|
| 500 | 13.1 + j17 | 15.6 + j13.4 |
| 1000 | 9.2 + j10.7 | 12.96 + j8.25 |
| 1500 | 6.4 + j3.9 | 8.78 + j3.9 |
| 2500 | 4.0 – j4.0 | 6.37 – j0.1 |
| 3500 | 3.8 – j10.4 | 5.45 – j5.1 |

Note 1. $V_{DD}$ = 28V, $I_{DQ}$ = 200mA in the 440166 package.
Note 2. Optimized for $P_{SAT}$ and PAE.
Note 3. When using this device at low frequency, series resistors should be used to maintain amplifier stability.

## CGH40010 Power Dissipation De-rating Curve



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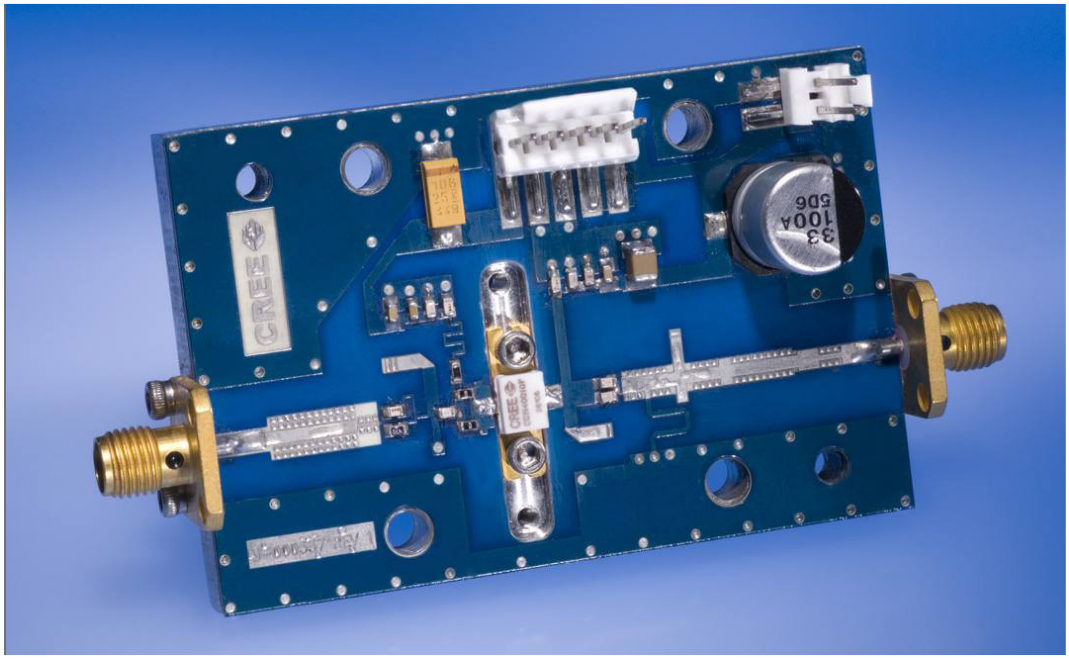
## CGH40010-TB Demonstration Amplifier Circuit Bill of Materials

| Designator | Description | Qty |
|---|---|---|
| R1,R2 | RES,1/16W,0603,1%,0 OHMS | 1 |
| R3 | RES,1/16W,0603,1%,47 OHMS | 1 |
| R4 | RES,1/16W,0603,1%,100 OHMS | 1 |
| C6 | CAP, 470PF, 5%,100V, 0603 | 1 |
| C17 | CAP, 33 UF, 20%, G CASE | 1 |
| C16 | CAP, 1.0UF, 100V, 10%, X7R, 1210 | 1 |
| C8 | CAP 10UF 16V TANTALUM | 1 |
| C14 | CAP, 100.0pF, +/-5%, 0603 | 1 |
| C1 | CAP, 0.5pF, +/-0.05pF, 0603 | 1 |
| C2 | CAP, 0.7pF, +/-0.1pF, 0603 | 1 |
| C10,C11 | CAP, 1.0pF, +/-0.1pF, 0603 | 2 |
| C4,C12 | CAP, 10.0pF,+/-5%, 0603 | 2 |
| C5,C13 | CAP, 39pF, +/-5%, 0603 | 2 |
| C7,C15 | CAP,33000PF, 0805,100V, X7R | 2 |
| J3,J4 | CONN SMA STR PANEL JACK RECP | 1 |
| J2 | HEADER RT>PLZ.1CEN LK 2 POS | 1 |
| J1 | HEADER RT>PLZ .1CEN LK 5POS | 1 |
| - | PCB, RO4350B, Er = 3.48, h = 20 mil | 1 |
| Q1 | CGH40010F or CGH40010P | 1 |

## CGH40010-TB Demonstration Amplifier Circuit



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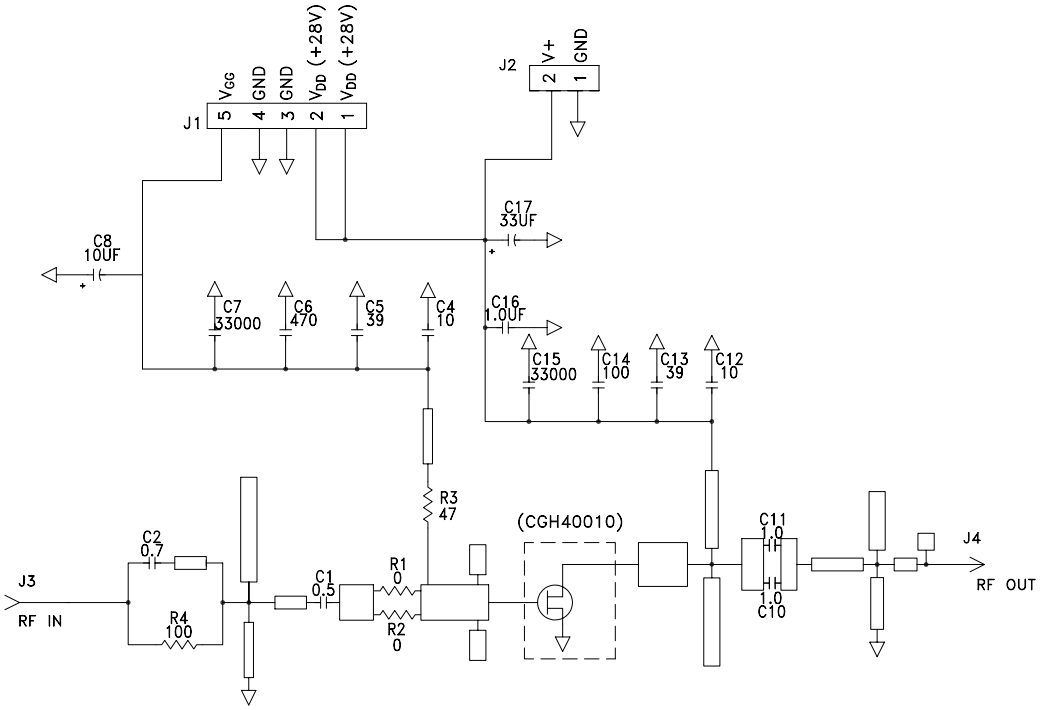
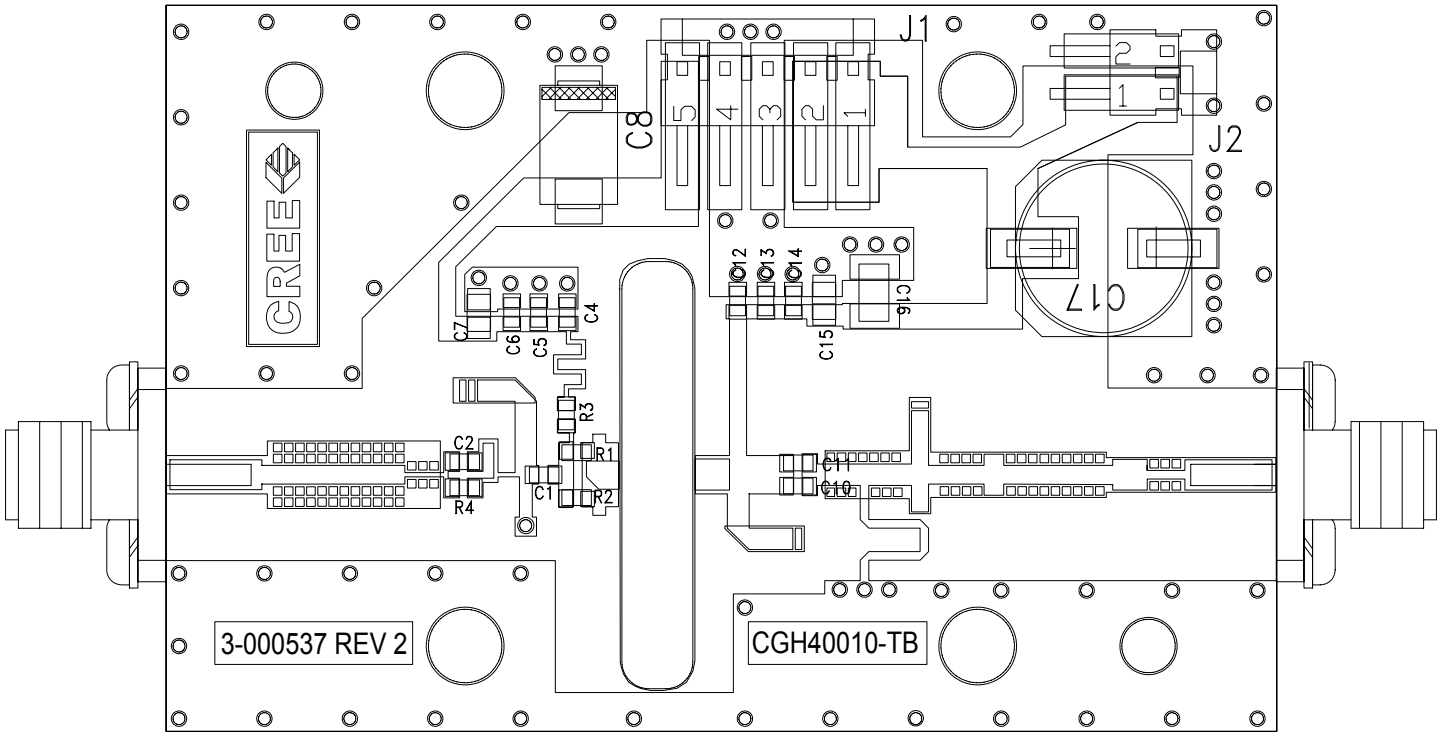
## CGH40010-TB Demonstration Amplifier Circuit Schematic




## CGH40010-TB Demonstration Amplifier Circuit Outline



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## Typical Package S-Parameters for CGH40010
## (Small Signal, $V_{DS}$ = 28 V, $I_{DQ}$ = 100 mA, angle in degrees)

| Frequency | Mag S11 | Ang S11 | Mag S21 | Ang S21 | Mag S12 | Ang S12 | Mag S22 | Ang S22 |
|---|---|---|---|---|---|---|---|---|
| 500 MHz | 0.8934 | -132.64 | 17.56 | 104.52 | 0.0321 | 17.50 | 0.387 | -108.94 |
| 600 MHz | 0.8873 | -141.26 | 15.03 | 98.88 | 0.0329 | 12.46 | 0.372 | -117.00 |
| 700 MHz | 0.8834 | -147.95 | 13.09 | 94.17 | 0.0334 | 8.36 | 0.362 | -123.20 |
| 800 MHz | 0.8807 | -153.33 | 11.58 | 90.10 | 0.0337 | 4.89 | 0.357 | -128.07 |
| 900 MHz | 0.8789 | -157.80 | 10.37 | 86.47 | 0.0338 | 1.87 | 0.355 | -131.99 |
| 1.0 GHz | 0.8777 | -161.61 | 9.38 | 83.16 | 0.0339 | -0.83 | 0.354 | -135.19 |
| 1.1 GHz | 0.8768 | -164.92 | 8.56 | 80.08 | 0.0339 | -3.28 | 0.355 | -137.86 |
| 1.2 GHz | 0.8762 | -167.85 | 7.87 | 77.19 | 0.0339 | -5.55 | 0.357 | -140.14 |
| 1.3 GHz | 0.8758 | -170.49 | 7.28 | 74.45 | 0.0338 | -7.67 | 0.360 | -142.12 |
| 1.4 GHz | 0.8756 | -172.90 | 6.77 | 71.82 | 0.0337 | -9.66 | 0.364 | -143.86 |
| 1.5 GHz | 0.8755 | -175.13 | 6.33 | 69.28 | 0.0336 | -11.56 | 0.368 | -145.43 |
| 1.6 GHz | 0.8754 | -177.21 | 5.94 | 66.82 | 0.0335 | -13.38 | 0.372 | -146.86 |
| 1.7 GHz | 0.8755 | -179.16 | 5.59 | 64.42 | 0.0333 | -15.12 | 0.377 | -148.19 |
| 1.8 GHz | 0.8756 | 178.98 | 5.28 | 62.08 | 0.0331 | -16.81 | 0.382 | -149.44 |
| 1.9 GHz | 0.8757 | 177.21 | 5.01 | 59.79 | 0.0329 | -18.43 | 0.387 | -150.63 |
| 2.0 GHz | 0.8759 | 175.50 | 4.76 | 57.53 | 0.0327 | -20.01 | 0.393 | -151.78 |
| 2.1 GHz | 0.8761 | 173.86 | 4.53 | 55.31 | 0.0325 | -21.55 | 0.398 | -152.90 |
| 2.2 GHz | 0.8763 | 172.26 | 4.33 | 53.12 | 0.0323 | -23.04 | 0.404 | -154.00 |
| 2.3 GHz | 0.8766 | 170.70 | 4.14 | 50.95 | 0.0321 | -24.50 | 0.410 | -155.08 |
| 2.4 GHz | 0.8768 | 169.17 | 3.97 | 48.82 | 0.0318 | -25.92 | 0.416 | -156.15 |
| 2.5 GHz | 0.8771 | 167.67 | 3.81 | 46.70 | 0.0316 | -27.31 | 0.421 | -157.22 |
| 2.6 GHz | 0.8774 | 166.19 | 3.67 | 44.60 | 0.0313 | -28.67 | 0.427 | -158.29 |
| 2.7 GHz | 0.8777 | 164.73 | 3.53 | 42.52 | 0.0310 | -29.99 | 0.433 | -159.36 |
| 2.8 GHz | 0.8780 | 163.28 | 3.41 | 40.45 | 0.0308 | -31.29 | 0.439 | -160.44 |
| 2.9 GHz | 0.8782 | 161.85 | 3.29 | 38.39 | 0.0305 | -32.56 | 0.444 | -161.52 |
| 3.0 GHz | 0.8785 | 160.41 | 3.18 | 36.35 | 0.0302 | -33.80 | 0.450 | -162.61 |
| 3.2 GHz | 0.8790 | 157.56 | 2.99 | 32.29 | 0.0296 | -36.19 | 0.461 | -164.83 |
| 3.4 GHz | 0.8795 | 154.71 | 2.82 | 28.27 | 0.0290 | -38.48 | 0.471 | -167.09 |
| 3.6 GHz | 0.8799 | 151.84 | 2.67 | 24.27 | 0.0284 | -40.66 | 0.481 | -169.40 |
| 3.8 GHz | 0.8803 | 148.94 | 2.54 | 20.28 | 0.0278 | -42.72 | 0.490 | -171.76 |
| 4.0 GHz | 0.8806 | 146.00 | 2.42 | 16.29 | 0.0271 | -44.66 | 0.499 | -174.19 |
| 4.2 GHz | 0.8808 | 143.00 | 2.31 | 12.31 | 0.0265 | -46.48 | 0.507 | -176.67 |
| 4.4 GHz | 0.8809 | 139.93 | 2.22 | 8.32 | 0.0259 | -48.17 | 0.514 | -179.22 |
| 4.6 GHz | 0.8810 | 136.79 | 2.13 | 4.30 | 0.0253 | -49.73 | 0.521 | 178.16 |
| 4.8 GHz | 0.8809 | 133.56 | 2.06 | 0.27 | 0.0246 | -51.13 | 0.527 | 175.47 |
| 5.0 GHz | 0.8808 | 130.23 | 1.99 | -3.80 | 0.0240 | -52.38 | 0.533 | 172.70 |
| 5.2 GHz | 0.8806 | 126.80 | 1.93 | -7.91 | 0.0235 | -53.47 | 0.537 | 169.85 |
| 5.4 GHz | 0.8804 | 123.26 | 1.87 | -12.07 | 0.0229 | -54.37 | 0.542 | 166.90 |
| 5.6 GHz | 0.8801 | 119.60 | 1.82 | -16.28 | 0.0224 | -55.09 | 0.545 | 163.86 |
| 5.8 GHz | 0.8797 | 115.81 | 1.77 | -20.56 | 0.0220 | -55.62 | 0.548 | 160.71 |
| 6.0 GHz | 0.8793 | 111.87 | 1.73 | -24.91 | 0.0216 | -55.96 | 0.550 | 157.44 |

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## Typical Package S-Parameters for CGH40010
## (Small Signal, $V_{DS}$ = 28 V, $I_{DQ}$ = 200 mA, angle in degrees)

| Frequency | Mag S11 | Ang S11 | Mag S21 | Ang S21 | Mag S12 | Ang S12 | Mag S22 | Ang S22 |
|---|---|---|---|---|---|---|---|---|
| 500 MHz | 0.8989 | -139.91 | 18.41 | 101.60 | 0.0267 | 15.28 | 0.368 | -124.81 |
| 600 MHz | 0.8945 | -147.69 | 15.65 | 96.44 | 0.0272 | 10.86 | 0.361 | -132.08 |
| 700 MHz | 0.8917 | -153.69 | 13.58 | 92.13 | 0.0275 | 7.30 | 0.358 | -137.49 |
| 800 MHz | 0.8899 | -158.52 | 11.98 | 88.39 | 0.0277 | 4.31 | 0.356 | -141.64 |
| 900 MHz | 0.8886 | -162.54 | 10.71 | 85.04 | 0.0278 | 1.72 | 0.356 | -144.91 |
| 1.0 GHz | 0.8877 | -165.97 | 9.68 | 81.98 | 0.0278 | -0.58 | 0.358 | -147.56 |
| 1.1 GHz | 0.8871 | -168.97 | 8.83 | 79.12 | 0.0278 | -2.67 | 0.359 | -149.74 |
| 1.2 GHz | 0.8867 | -171.64 | 8.11 | 76.42 | 0.0277 | -4.60 | 0.362 | -151.58 |
| 1.3 GHz | 0.8864 | -174.06 | 7.50 | 73.84 | 0.0277 | -6.40 | 0.365 | -153.16 |
| 1.4 GHz | 0.8862 | -176.28 | 6.98 | 71.37 | 0.0276 | -8.08 | 0.368 | -154.56 |
| 1.5 GHz | 0.8860 | -178.34 | 6.52 | 68.97 | 0.0275 | -9.69 | 0.371 | -155.80 |
| 1.6 GHz | 0.8859 | 179.73 | 6.12 | 66.64 | 0.0274 | -11.21 | 0.375 | -156.94 |
| 1.7 GHz | 0.8859 | 177.90 | 5.76 | 64.36 | 0.0273 | -12.68 | 0.379 | -157.99 |
| 1.8 GHz | 0.8859 | 176.15 | 5.45 | 62.13 | 0.0271 | -14.08 | 0.383 | -158.98 |
| 1.9 GHz | 0.8859 | 174.48 | 5.17 | 59.93 | 0.0270 | -15.44 | 0.387 | -159.93 |
| 2.0 GHz | 0.8860 | 172.86 | 4.91 | 57.77 | 0.0268 | -16.75 | 0.392 | -160.84 |
| 2.1 GHz | 0.8861 | 171.29 | 4.68 | 55.64 | 0.0267 | -18.02 | 0.396 | -161.73 |
| 2.2 GHz | 0.8861 | 169.76 | 4.47 | 53.53 | 0.0265 | -19.25 | 0.401 | -162.60 |
| 2.3 GHz | 0.8862 | 168.27 | 4.28 | 51.45 | 0.0263 | -20.44 | 0.406 | -163.47 |
| 2.4 GHz | 0.8863 | 166.80 | 4.11 | 49.38 | 0.0261 | -21.60 | 0.410 | -164.34 |
| 2.5 GHz | 0.8864 | 165.35 | 3.94 | 47.33 | 0.0260 | -22.73 | 0.415 | -165.20 |
| 2.6 GHz | 0.8865 | 163.92 | 3.80 | 45.30 | 0.0258 | -23.82 | 0.420 | -166.08 |
| 2.7 GHz | 0.8866 | 162.50 | 3.66 | 43.27 | 0.0256 | -24.88 | 0.424 | -166.96 |
| 2.8 GHz | 0.8867 | 161.09 | 3.53 | 41.26 | 0.0254 | -25.91 | 0.429 | -167.85 |
| 2.9 GHz | 0.8868 | 159.69 | 3.41 | 39.26 | 0.0252 | -26.91 | 0.434 | -168.76 |
| 3.0 GHz | 0.8869 | 158.29 | 3.31 | 37.27 | 0.0250 | -27.88 | 0.438 | -169.67 |
| 3.2 GHz | 0.8870 | 155.50 | 3.11 | 33.30 | 0.0245 | -29.73 | 0.447 | -171.55 |
| 3.4 GHz | 0.8871 | 152.69 | 2.93 | 29.35 | 0.0241 | -31.45 | 0.456 | -173.50 |
| 3.6 GHz | 0.8872 | 149.87 | 2.78 | 25.41 | 0.0237 | -33.04 | 0.464 | -175.51 |
| 3.8 GHz | 0.8871 | 147.00 | 2.65 | 21.48 | 0.0233 | -34.50 | 0.472 | -177.60 |
| 4.0 GHz | 0.8871 | 144.09 | 2.53 | 17.55 | 0.0228 | -35.82 | 0.479 | -179.76 |
| 4.2 GHz | 0.8869 | 141.12 | 2.42 | 13.61 | 0.0224 | -37.00 | 0.486 | 178.00 |
| 4.4 GHz | 0.8867 | 138.08 | 2.32 | 9.64 | 0.0223 | -38.03 | 0.492 | 175.68 |
| 4.6 GHz | 0.8865 | 134.95 | 2.24 | 5.66 | 0.0217 | -38.91 | 0.498 | 173.27 |
| 4.8 GHz | 0.8861 | 131.75 | 2.16 | 1.64 | 0.0213 | -39.63 | 0.503 | 170.78 |
| 5.0 GHz | 0.8857 | 128.44 | 2.09 | -2.41 | 0.0210 | -40.20 | 0.507 | 168.19 |
| 5.2 GHz | 0.8853 | 125.03 | 2.03 | -6.51 | 0.0208 | -40.61 | 0.511 | 165.50 |
| 5.4 GHz | 0.8848 | 121.50 | 1.97 | -10.66 | 0.0206 | -40.88 | 0.514 | 162.70 |
| 5.6 GHz | 0.8842 | 117.85 | 1.92 | -14.87 | 0.0205 | -41.03 | 0.517 | 159.80 |
| 5.8 GHz | 0.8837 | 114.07 | 1.87 | -19.15 | 0.0204 | -41.06 | 0.519 | 156.77 |
| 6.0 GHz | 0.8831 | 110.15 | 1.83 | -23.51 | 0.0205 | -41.02 | 0.521 | 153.61 |

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## Typical Package S-Parameters for CGH40010
## (Small Signal, $V_{DS}$ = 28 V, $I_{DQ}$ = 500 mA, angle in degrees)

| Frequency | Mag S11 | Ang S11 | Mag S21 | Ang S21 | Mag S12 | Ang S12 | Mag S22 | Ang S22 |
|---|---|---|---|---|---|---|---|---|
| 500 MHz | 0.9045 | -145.34 | 18.40 | 99.37 | 0.0233 | 13.69 | 0.369 | -136.87 |
| 600 MHz | 0.9013 | -152.43 | 15.58 | 94.58 | 0.0237 | 9.77 | 0.367 | -143.11 |
| 700 MHz | 0.8993 | -157.90 | 13.49 | 90.58 | 0.0239 | 6.65 | 0.367 | -147.68 |
| 800 MHz | 0.8979 | -162.30 | 11.88 | 87.09 | 0.0240 | 4.04 | 0.368 | -151.16 |
| 900 MHz | 0.8970 | -165.97 | 10.61 | 83.95 | 0.0240 | 1.79 | 0.369 | -153.88 |
| 1.0 GHz | 0.8963 | -169.12 | 9.58 | 81.06 | 0.0240 | -0.20 | 0.370 | -156.08 |
| 1.1 GHz | 0.8958 | -171.88 | 8.73 | 78.35 | 0.0240 | -2.00 | 0.372 | -157.90 |
| 1.2 GHz | 0.8955 | -174.36 | 8.02 | 75.78 | 0.0240 | -3.65 | 0.375 | -159.44 |
| 1.3 GHz | 0.8952 | -176.61 | 7.42 | 73.33 | 0.0239 | -5.19 | 0.377 | -160.78 |
| 1.4 GHz | 0.8950 | -178.69 | 6.90 | 70.96 | 0.0238 | -6.63 | 0.380 | -161.95 |
| 1.5 GHz | 0.8949 | 179.37 | 6.44 | 68.66 | 0.0238 | -7.99 | 0.383 | -163.01 |
| 1.6 GHz | 0.8948 | 177.54 | 6.05 | 66.42 | 0.0237 | -9.28 | 0.386 | -163.97 |
| 1.7 GHz | 0.8947 | 175.80 | 5.70 | 64.22 | 0.0236 | -10.51 | 0.389 | -164.87 |
| 1.8 GHz | 0.8947 | 174.14 | 5.39 | 62.07 | 0.0235 | -11.69 | 0.393 | -165.72 |
| 1.9 GHz | 0.8946 | 172.53 | 5.11 | 59.94 | 0.0234 | -12.82 | 0.396 | -166.54 |
| 2.0 GHz | 0.8946 | 170.98 | 4.86 | 57.85 | 0.0233 | -13.91 | 0.400 | -167.33 |
| 2.1 GHz | 0.8946 | 169.47 | 4.63 | 55.78 | 0.0231 | -14.96 | 0.404 | -168.10 |
| 2.2 GHz | 0.8946 | 167.98 | 4.43 | 53.73 | 0.0230 | -15.97 | 0.407 | -168.86 |
| 2.3 GHz | 0.8946 | 166.53 | 4.24 | 51.69 | 0.0229 | -16.95 | 0.411 | -169.62 |
| 2.4 GHz | 0.8946 | 165.10 | 4.07 | 49.68 | 0.0227 | -17.89 | 0.415 | -170.38 |
| 2.5 GHz | 0.8945 | 163.69 | 3.91 | 47.67 | 0.0226 | -18.80 | 0.419 | -171.14 |
| 2.6 GHz | 0.8945 | 162.29 | 3.77 | 45.68 | 0.0225 | -19.67 | 0.423 | -171.91 |
| 2.7 GHz | 0.8945 | 160.90 | 3.64 | 43.70 | 0.0223 | -20.51 | 0.426 | -172.70 |
| 2.8 GHz | 0.8945 | 159.52 | 3.51 | 41.73 | 0.0222 | -21.32 | 0.430 | -173.49 |
| 2.9 GHz | 0.8945 | 158.14 | 3.39 | 39.76 | 0.0220 | -22.10 | 0.434 | -174.30 |
| 3.0 GHz | 0.8944 | 156.76 | 3.28 | 37.80 | 0.0219 | -22.84 | 0.438 | -175.12 |
| 3.2 GHz | 0.8943 | 154.01 | 3.09 | 33.89 | 0.0216 | -24.24 | 0.445 | -176.82 |
| 3.4 GHz | 0.8942 | 151.24 | 2.92 | 30.00 | 0.0213 | -25.50 | 0.452 | -178.58 |
| 3.6 GHz | 0.8940 | 148.44 | 2.77 | 26.11 | 0.0210 | -26.64 | 0.459 | 179.57 |
| 3.8 GHz | 0.8938 | 145.60 | 2.64 | 22.22 | 0.0207 | -27.63 | 0.465 | 177.65 |
| 4.0 GHz | 0.8935 | 142.71 | 2.52 | 18.32 | 0.0205 | -28.49 | 0.471 | 175.64 |
| 4.2 GHz | 0.8931 | 139.75 | 2.42 | 14.40 | 0.0203 | -29.22 | 0.477 | 173.54 |
| 4.4 GHz | 0.8927 | 136.72 | 2.32 | 10.46 | 0.0201 | -29.81 | 0.482 | 171.36 |
| 4.6 GHz | 0.8922 | 133.61 | 2.24 | 6.49 | 0.0199 | -30.26 | 0.487 | 169.08 |
| 4.8 GHz | 0.8917 | 130.41 | 2.16 | 2.49 | 0.0198 | -30.59 | 0.491 | 166.70 |
| 5.0 GHz | 0.8911 | 127.11 | 2.09 | -1.56 | 0.0198 | -30.82 | 0.494 | 164.23 |
| 5.2 GHz | 0.8904 | 123.71 | 2.03 | -5.65 | 0.0198 | -30.95 | 0.498 | 161.64 |
| 5.4 GHz | 0.8898 | 120.19 | 1.97 | -9.80 | 0.0198 | -31.01 | 0.500 | 158.94 |
| 5.6 GHz | 0.8891 | 116.54 | 1.92 | -14.02 | 0.0200 | -31.04 | 0.502 | 156.12 |
| 5.8 GHz | 0.8884 | 112.77 | 1.88 | -18.30 | 0.0203 | -31.06 | 0.504 | 153.17 |
| 6.0 GHz | 0.8877 | 108.85 | 1.83 | -22.66 | 0.0206 | -31.12 | 0.505 | 150.08 |

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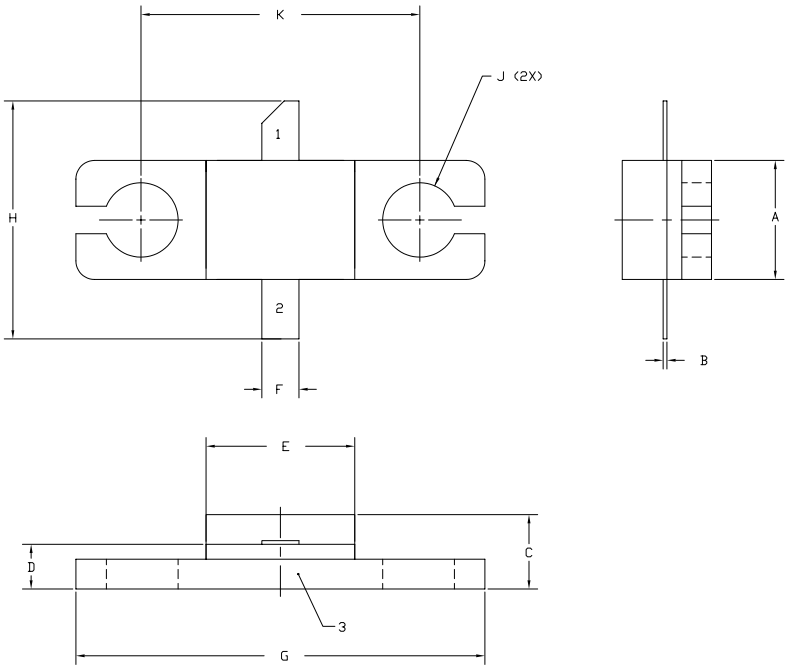
## Product Dimensions CGH40010F (Package Type — 440166)



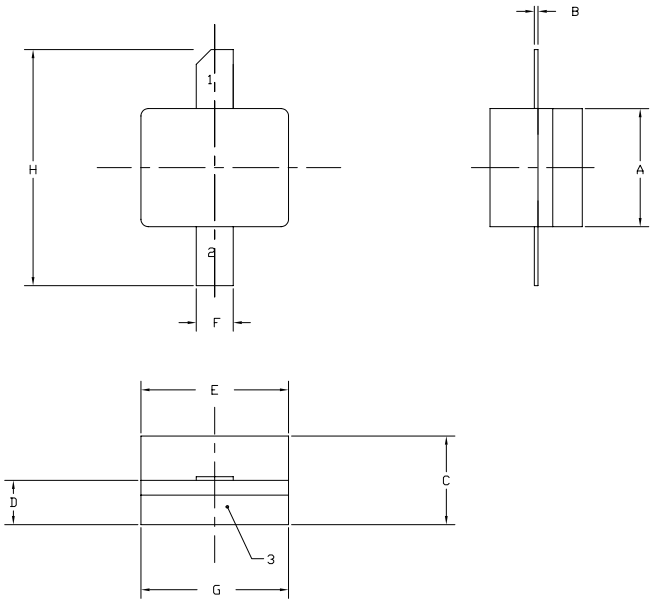

NOTES:

1. DIMENSIONING AND TOLERANICING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.
5. ALL PLATED SURFACES ARE NI/AU

| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.155 | 0.165 | 3.94 | 4.19 |
| B | 0.004 | 0.006 | 0.10 | 0.15 |
| C | 0.115 | 0.135 | 2.92 | 3.43 |
| D | 0.057 | 0.067 | 1.45 | 1.70 |
| E | 0.195 | 0.205 | 4.95 | 5.21 |
| F | 0.045 | 0.055 | 1.14 | 1.40 |
| G | 0.545 | 0.555 | 13.84 | 14.09 |
| H | 0.280 | 0.360 | 7.87 | 8.38 |
| J | ø .100 | | 2.54 | |
| K | 0.375 | | 9.53 | |

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE

## Product Dimensions CGH40010P (Package Type — 440196)




NOTES:

1. DIMENSIONING AND TOLERANICING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.
5. ALL PLATED SURFACES ARE NI/AU

| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.155 | 0.165 | 3.94 | 4.19 |
| B | 0.003 | 0.006 | 0.10 | 0.15 |
| C | 0.115 | 0.135 | 2.92 | 3.17 |
| D | 0.057 | 0.067 | 1.45 | 1.70 |
| E | 0.195 | 0.205 | 4.95 | 5.21 |
| F | 0.045 | 0.055 | 1.14 | 1.40 |
| G | 0.195 | 0.205 | 4.95 | 5.21 |
| H | 0.280 | 0.360 | 7.112 | 9.114 |

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE





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# *Appendix B*

# Cree GaN HEMT (CGH40006P) Device Data Sheet

# CGH40006P

## 6 W, RF Power GaN HEMT

Cree's CGH40006P is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). The CGH40006P, operating from a 28 volt rail, offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making the CGH40006P ideal for linear and compressed amplifier circuits. The transistor is available in a solder-down, pill package.


Package Types: 440109
PN's: CGH40006P

### FEATURES

- Up to 6 GHz Operation
- 13 dB Small Signal Gain at 2.0 GHz
- 11 dB Small Signal Gain at 6.0 GHz
- 8 W typical at $P_{IN}$ = 32 dBm
- 65 % Efficiency at $P_{IN}$ = 32 dBm
- 28 V Operation

### APPLICATIONS

- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, Linear amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA waveforms

RoHS COMPLIANT

PRELIMINARY
Rev 2.0 – March 2011

Large Signal Models Available for SiC & GaN

## Absolute Maximum Ratings (not simultaneous) at 25˚C Case Temperature

| Parameter | Symbol | Rating | Units |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | 84 | Volts |
| Gate-to-Source Voltage | $V_{GS}$ | -10, +2 | Volts |
| Storage Temperature | $T_{STG}$ | -65, +150 | ˚C |
| Operating Junction Temperature | $T_J$ | 225 | ˚C |
| Maximum Forward Gate Current | $I_{GMAX}$ | 2.1 | mA |
| Soldering Temperature[1] | $T_S$ | 245 | ˚C |
| Thermal Resistance, Junction to Case[2] | $R_{\theta JC}$ | 9.5 | ˚C/W |
| Case Operating Temperature[2] | $T_C$ | -40, +150 | ˚C |

Note:
[1] Refer to the Application Note on soldering at www.cree.com/products/wireless_appnotes.asp
[2] Measured for the CGH40006P at $P_{DISS}$ = 8 W.

## Electrical Characteristics ($T_C$ = 25˚C)

| Characteristics | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **DC Characteristics[1]** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | -3.8 | -3.3 | -2.3 | $V_{DC}$ | $V_{DS}$ = 10 V, $I_D$ = 2.1 mA |
| Gate Quiescent Voltage | $V_{GS(Q)}$ | – | -3.0 | – | $V_{DC}$ | $V_{DS}$ = 28 V, $I_D$ = 100 mA |
| Saturated Drain Current | $I_{DS}$ | 1.7 | 2.1 | – | A | $V_{DS}$ = 6.0 V, $V_{GS}$ = 2.0 V |
| Drain-Source Breakdown Voltage | $V_{BR}$ | 120 | – | – | $V_{DC}$ | $V_{GS}$ = -8 V, $I_D$ = 2.1 mA |
| **RF Characteristics[2] ($T_C$ = 25˚C, $F_0$ = 2.0 GHz unless otherwise noted)** | | | | | | |
| Small Signal Gain | $G_{SS}$ | 11.5 | 13 | – | dB | $V_{DD}$ = 28 V, $I_{DQ}$ = 100 mA |
| Power Output at $P_{IN}$ = 32 dBm | $P_{OUT}$ | 7.0 | 9 | – | W | $V_{DD}$ = 28 V, $I_{DQ}$ = 100 mA |
| Drain Efficiency[3] | η | 53 | 65 | – | % | $V_{DD}$ = 28 V, $I_{DQ}$ = 100 mA, $P_{IN}$ = 32 dBm |
| Output Mismatch Stress | VSWR | – | – | 10 : 1 | Ψ | No damage at all phase angles, $V_{DD}$ = 28 V, $I_{DQ}$ = 100 mA, $P_{IN}$ = 32 dBm |
| **Dynamic Characteristics** | | | | | | |
| Input Capacitance | $C_{GS}$ | – | 3.0 | – | pF | $V_{DS}$ = 28 V, $V_{gs}$ = -8 V, f = 1 MHz |
| Output Capacitance | $C_{DS}$ | – | 1.1 | – | pF | $V_{DS}$ = 28 V, $V_{gs}$ = -8 V, f = 1 MHz |
| Feedback Capacitance | $C_{GD}$ | – | 0.1 | – | pF | $V_{DS}$ = 28 V, $V_{gs}$ = -8 V, f = 1 MHz |

Notes:
[1] Measured on wafer prior to packaging.
[2] Measured in CGH40006P-TB.
[3] Drain Efficiency = $P_{OUT}$ / $P_{DC}$



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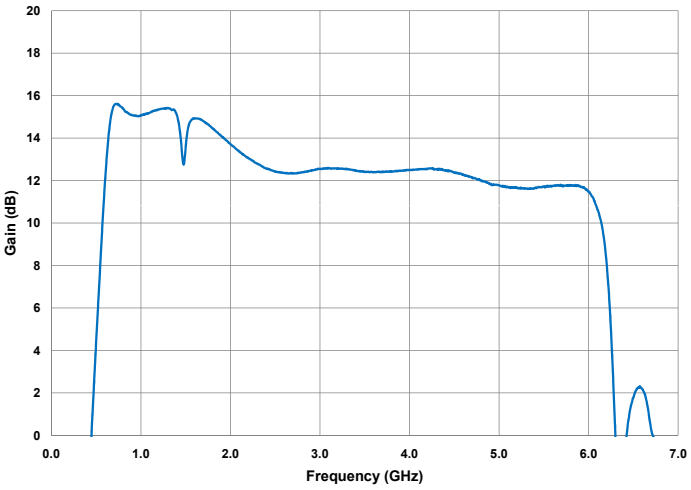
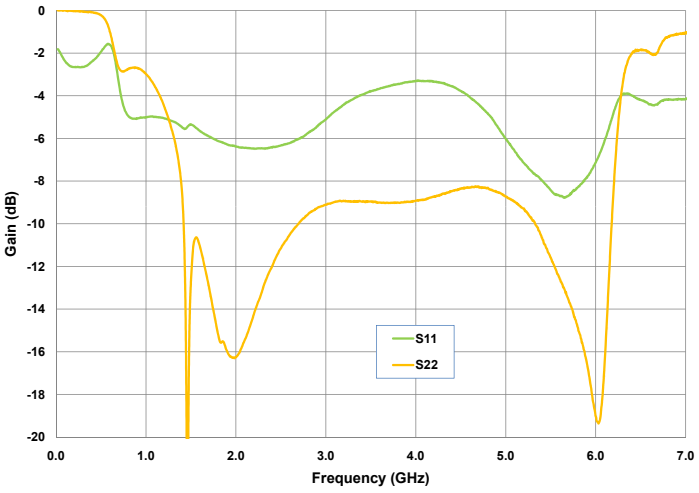
## Typical Performance

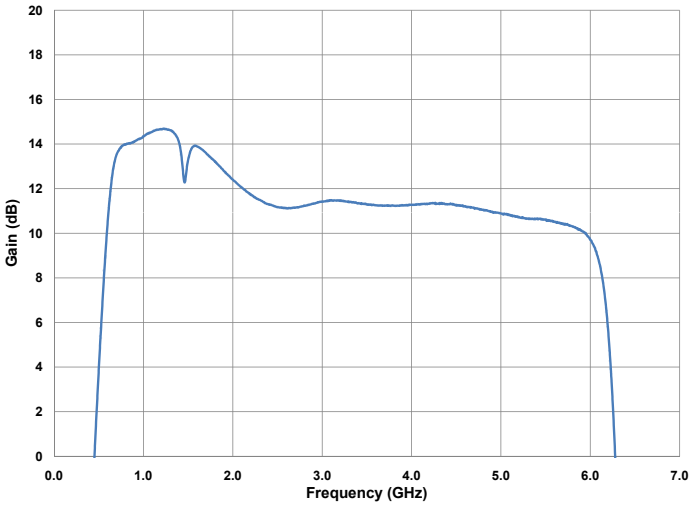
### Small Signal Gain vs Frequency at 28 V of the CGH40006P in the CGH40006P-TB



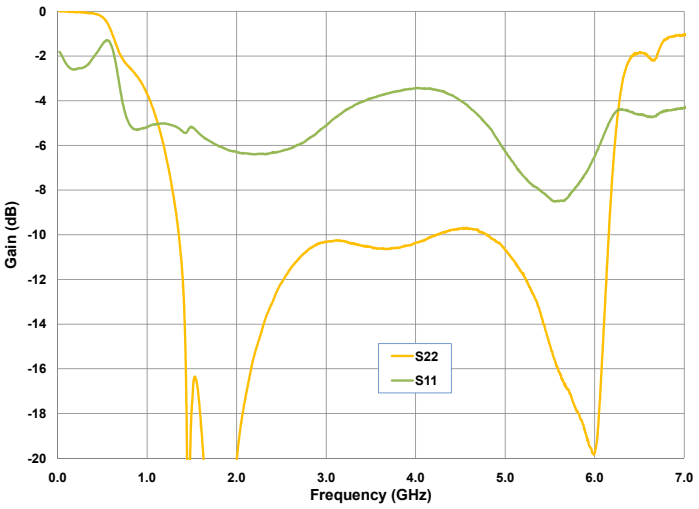

### Input & Output Return Losses vs Frequency at 28 V of the CGH40006P in the CGH40006P-TB




### Small Signal Gain vs Frequency at 20 V of the CGH40006P in the CGH40006P-TB




### Input & Output Return Losses vs Frequency at 20 V of the CGH40006P in the CGH40006P-TB





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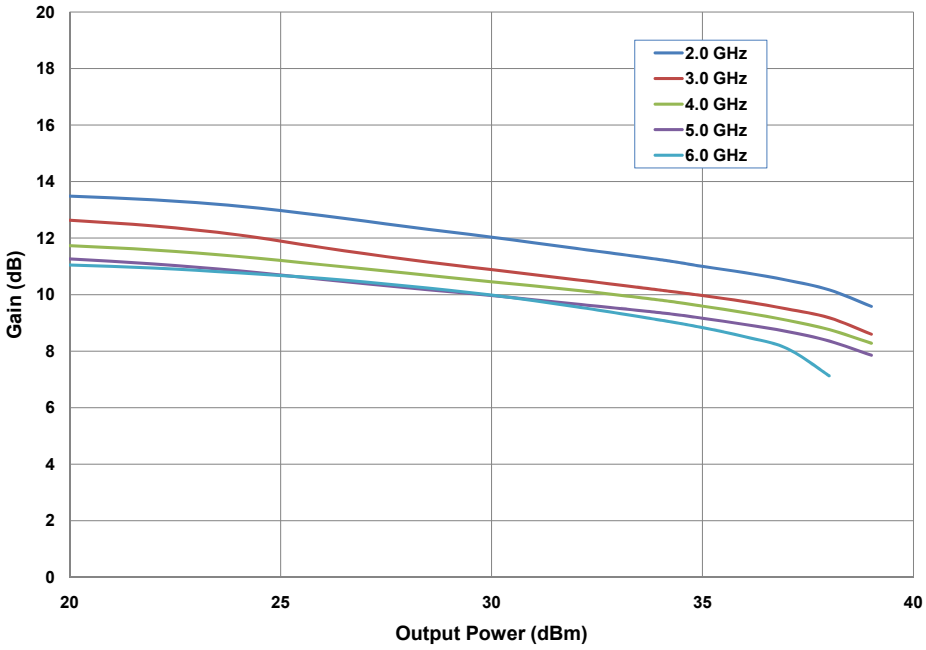
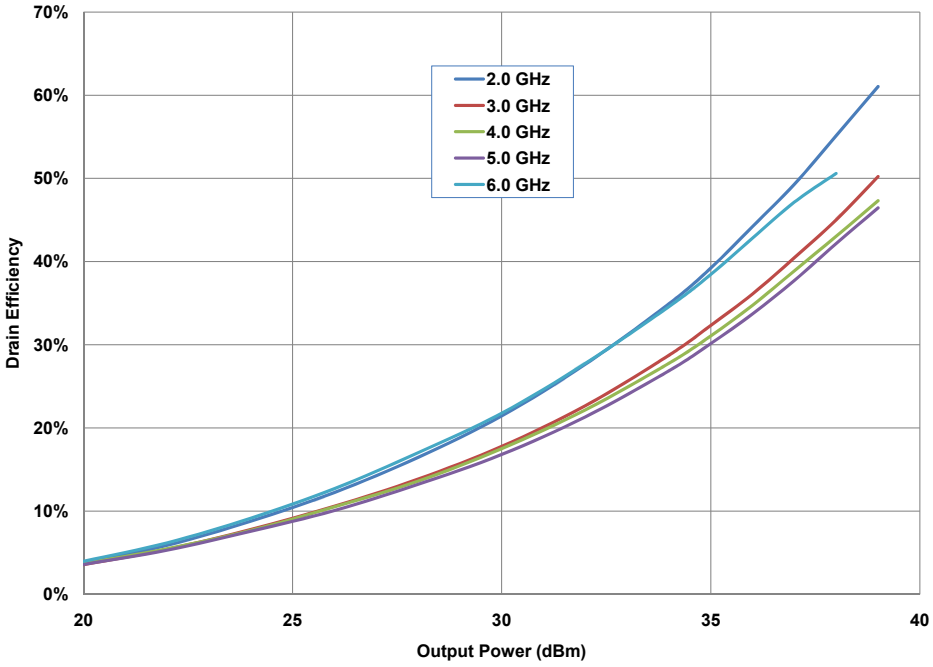
## Typical Performance

**Power Gain vs Output Power as a Function of Frequency of the CGH40006P in the CGH40006P-TB**
**$V_{DD}$ = 28 V, $I_{DQ}$ = 100 mA**




**Drain Efficiency vs Output Power as a Function of Frequency of the CGH40006P in the CGH40006P-TB**
**$V_{DD}$ = 28 V, $I_{DQ}$ = 100 mA**



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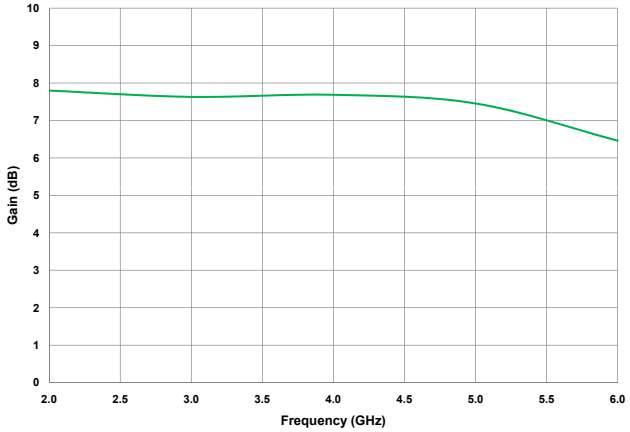
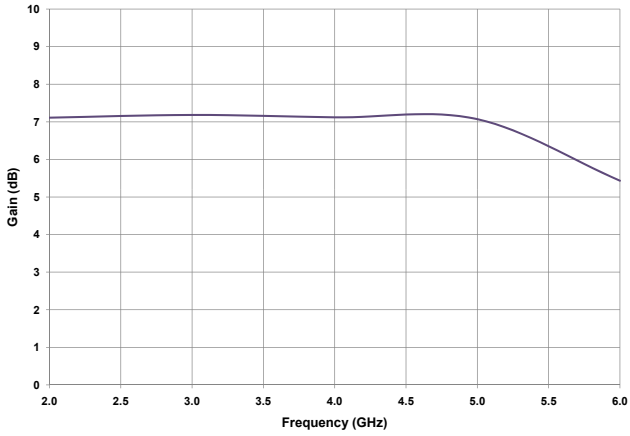
## Typical Performance

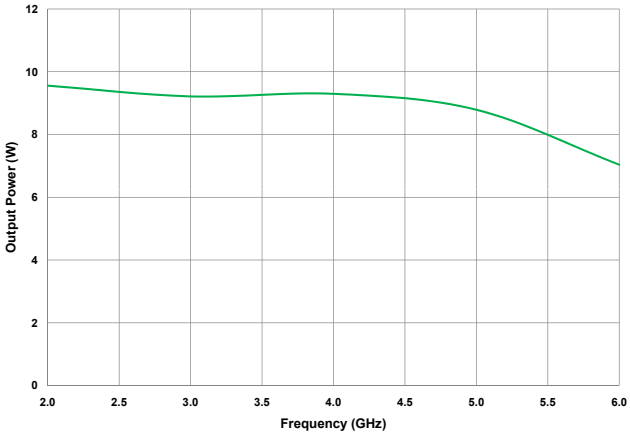
### Power Gain vs Frequency of the CGH40006P in the CGH40006P-TB at $P_{IN}$ = 32 dBm, $V_{DD}$ = 28 V



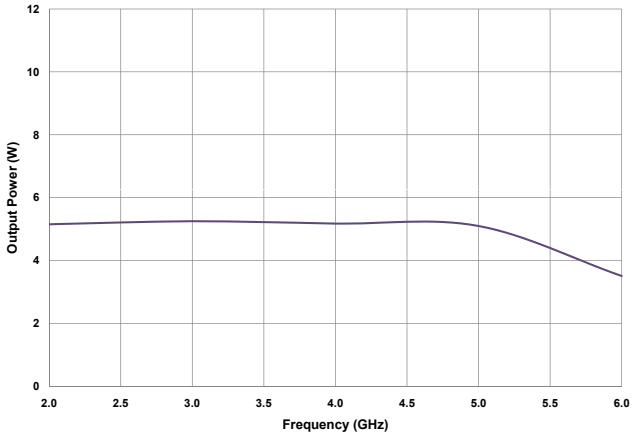

### Power Gain vs Frequency of the CGH40006P in the CGH40006P-TB at $P_{IN}$ = 30 dBm, $V_{DD}$ = 20 V



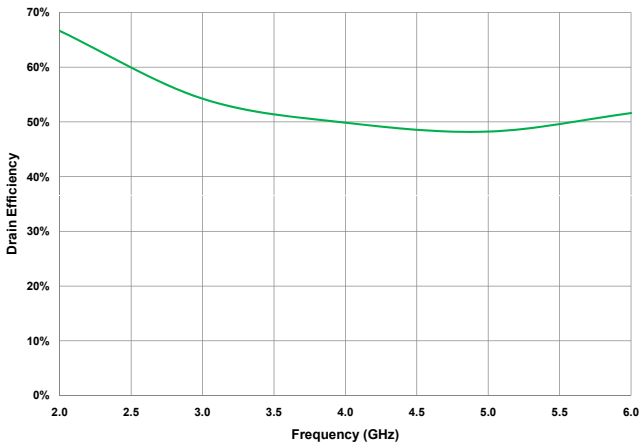

### Output Power vs Frequency of the CGH40006P in the CGH40006P-TB at $P_{IN}$ = 32 dBm, $V_{DD}$ = 28 V



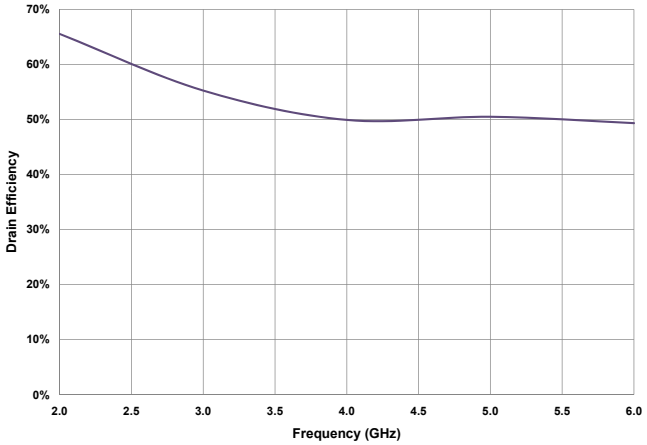

### Output Power vs Frequency of the CGH40006P in the CGH40006P-TB at $P_{IN}$ = 30 dBm, $V_{DD}$ = 20 V




### Drain Efficiency vs Frequency of the CGH40006P in the CGH40006P-TB at $P_{IN}$ = 32 dBm, $V_{DD}$ = 28 V




### Drain Efficiency vs Frequency of the CGH40006P in the CGH40006P-TB at $P_{IN}$ = 30 dBm, $V_{DD}$ = 20 V



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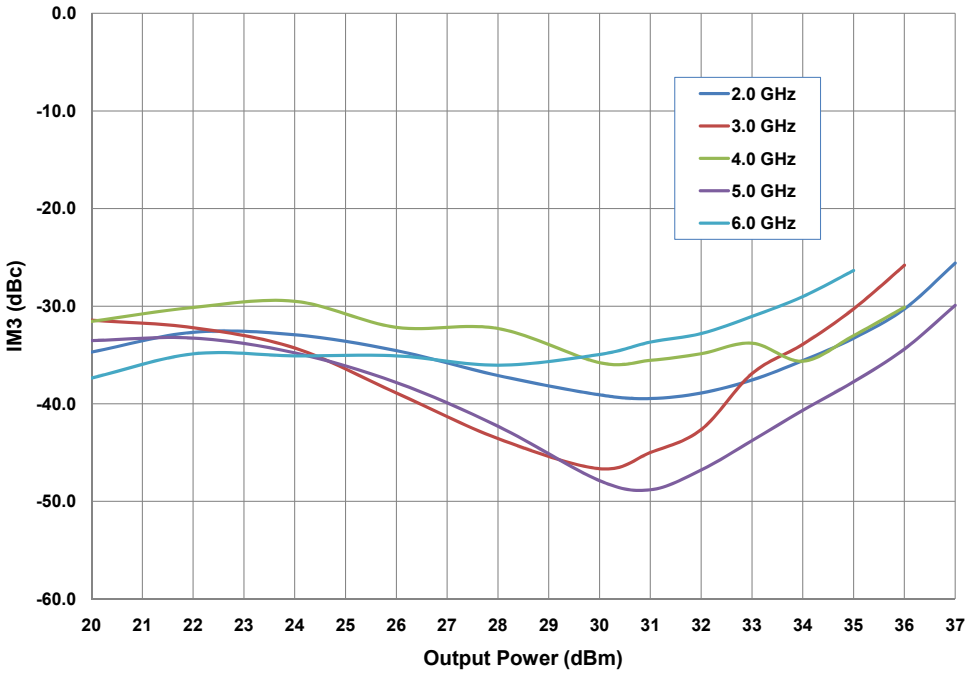
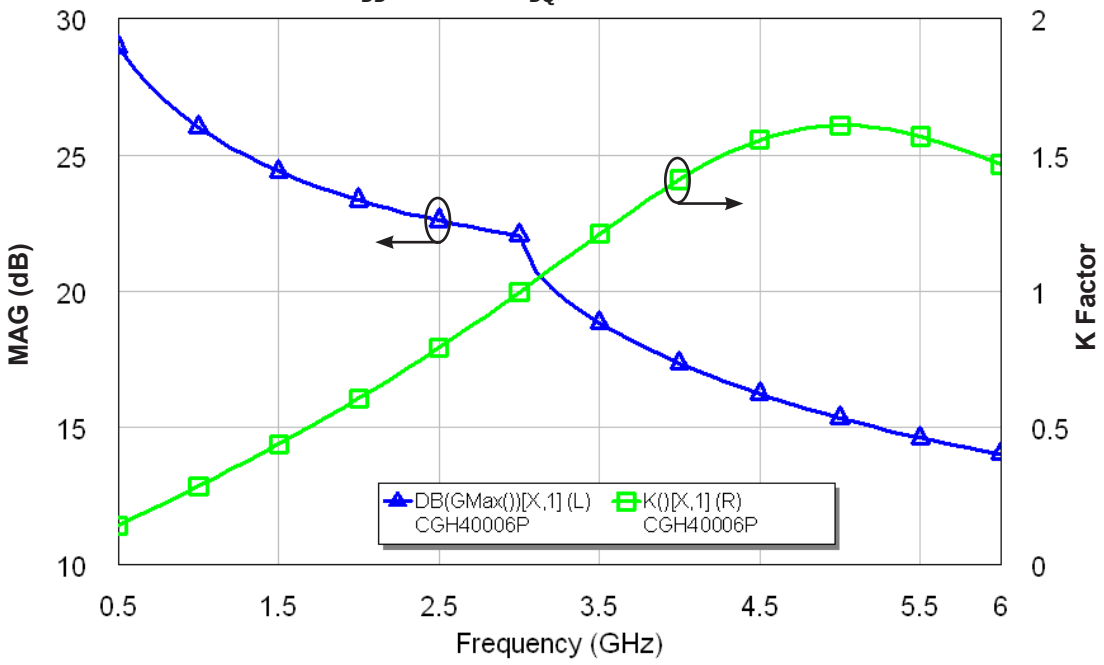
## Typical Performance

**Third Order Intermodulation Distortion vs Average Output Power as a Function of Frequency of the CGH40006P in the CGH40006P-TB**
**$V_{DD}$ = 28 V, $I_{DQ}$ = 60 mA**




**Simulated Maximum Available Gain and K Factor of the CGH40006P**
**$V_{DD}$ = 28 V, $I_{DQ}$ = 100 mA**



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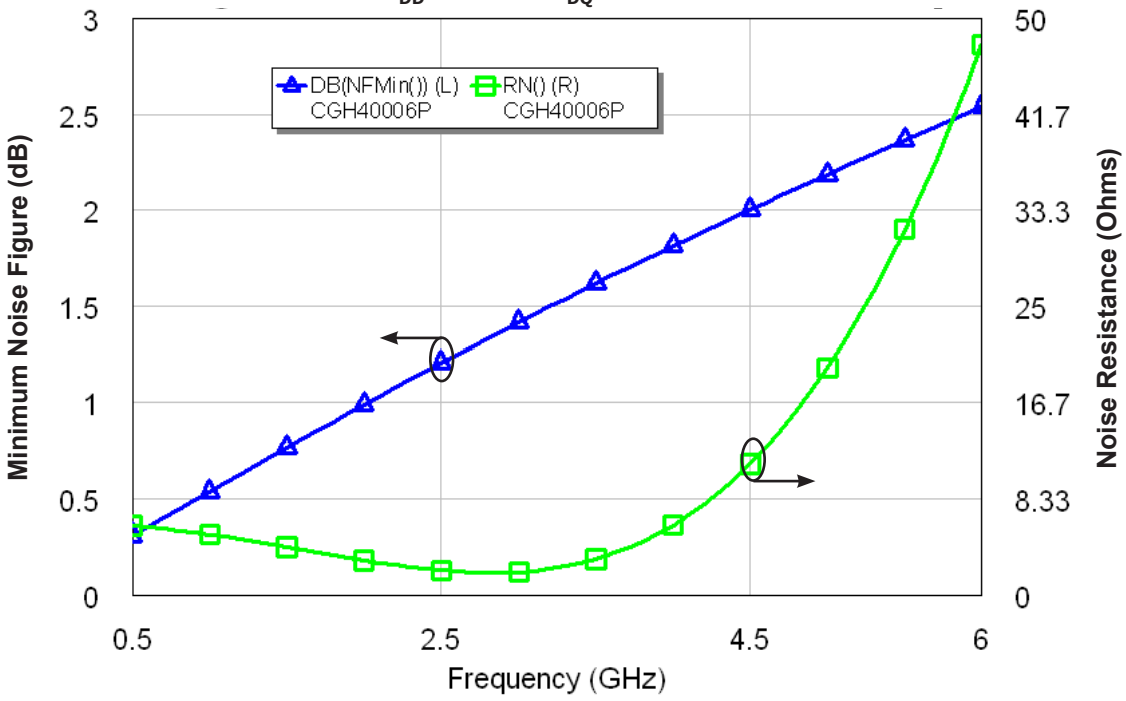
## Typical Noise Performance

**Simulated Minimum Noise Figure and Noise Resistance vs Frequency of the CGH40006P**
**$V_{DD}$ = 28 V, $I_{DQ}$ = 100 mA**




## Electrostatic Discharge (ESD) Classifications

| Parameter | Symbol | Class | Test Methodology |
|---|---|---|---|
| Human Body Model | HBM | 1A > 250 V | JEDEC JESD22 A114-D |
| Charge Device Model | CDM | 1 < 200 V | JEDEC JESD22 C101-C |



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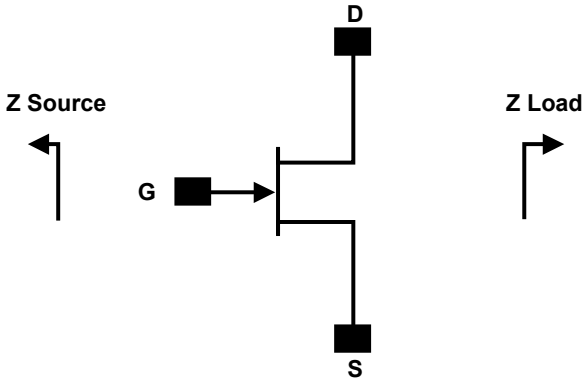
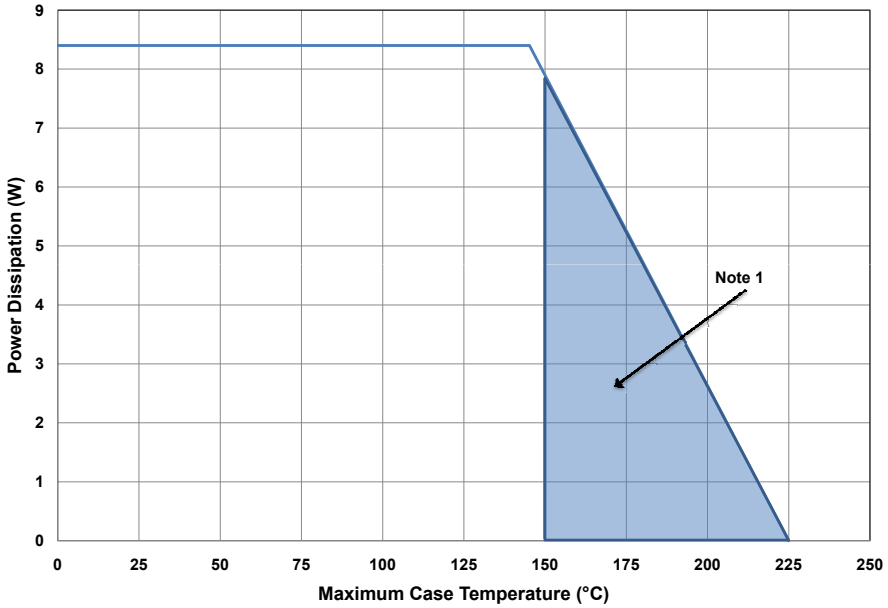
## Source and Load Impedances




| Frequency (MHz) | Z Source | Z Load |
|---|---|---|
| 1000 | 13.78 + j6.9 | 61.5 + j47.4 |
| 2000 | 4.78 + j1.78 | 19.4 + j39.9 |
| 3000 | 2.57 - j6.94 | 12.57 + j23.1 |
| 4000 | 3.54 - j14.86 | 9.44 + j11.68 |
| 5000 | 4.42 - j25.8 | 9.78 + j4.85 |
| 6000 | 7.1 - j42.7 | 9.96 - j4.38 |

Note 1. $V_{DD}$ = 28V, $I_{DQ}$ = 100mA in the 440109 package.
Note 2. Optimized for power gain, $P_{SAT}$ and PAE.
Note 3. When using this device at low frequency, series resistors should be used to maintain amplifier stability.

## CGH40006P Power Dissipation De-rating Curve




Note 1. Area exceeds Maximum Case Operating Temperature (See Page 2).



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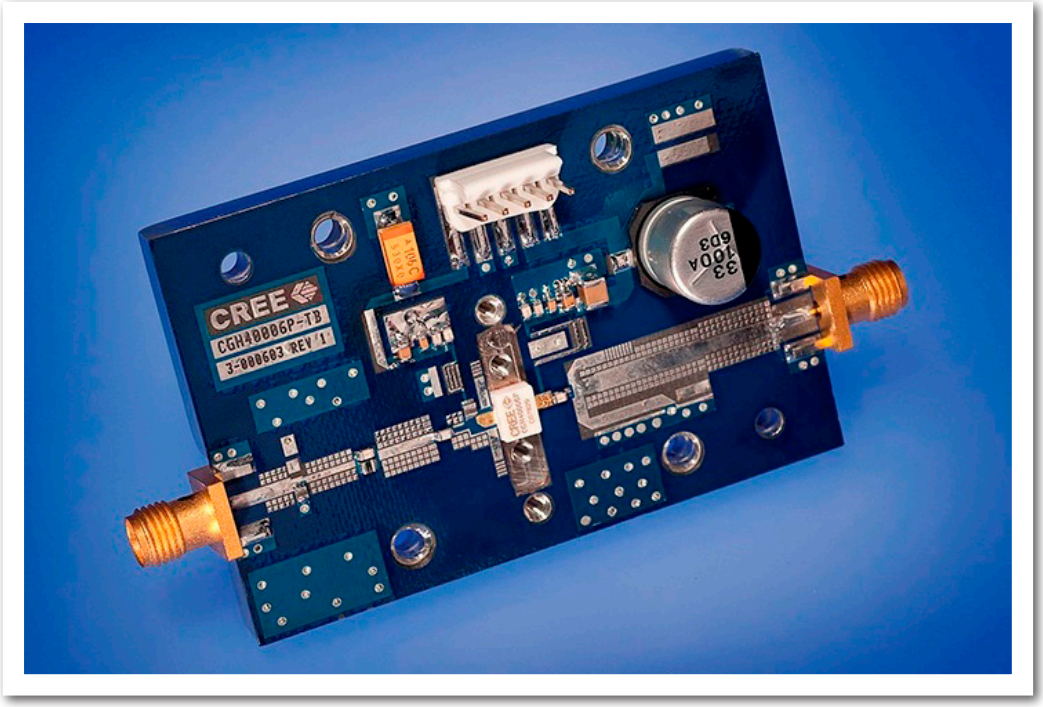
## CGH40006P-TB Demonstration Amplifier Circuit Bill of Materials

| Designator | Description | Qty |
|---|---|---|
| R1 | RES, AIN, 0505, 470 Ohms (≤5% tolerance) | 1 |
| R2 | RES, AIN, 0505, 10 Ohms (≤5% tolerance) | 1 |
| R3 | RES, AIN, 0505, 150 Ohms (≤5% tolerance) | 1 |
| C1 | CAP, 2.0 pF +/-0.1 pF, 0603, ATC 600S | 1 |
| C2 | CAP, 4.7 pF +/-0.1 pF, 0603, ATC 600S | 1 |
| C10 | CAP, 3.6 pF +/-0.1 pF, 0603, ATC 600S | 1 |
| C4,C11 | CAP, 8.2 pF +/-0.25, 0603, ATC 600S | 2 |
| C6,C13 | CAP, 470 pF +/-5%, 0603, 100 V | 2 |
| C7,C14 | CAP, 33000 pF, CER, 100V, X7R, 0805 | 2 |
| C8 | CAP, 10 uf, 16V, SMT, TANTALUM | 1 |
| C15 | CAP, 1.0 uF +/-10%, CER, 100V, X7R, 1210 | 1 |
| C16 | CAP, 33 uF, 100V, ELECT, FK, SMD | 1 |
| J3,J4 | CONN, SMA, STR, PANEL, JACK, RECP | 2 |
| J1 | HEADER RT>PLZ .1CEN LK 5POS | 1 |
| - | PCB, RO5880, 20 MIL | 1 |
| Q1 | CGH40006P | 1 |

## CGH40006P-TB Demonstration Amplifier Circuit



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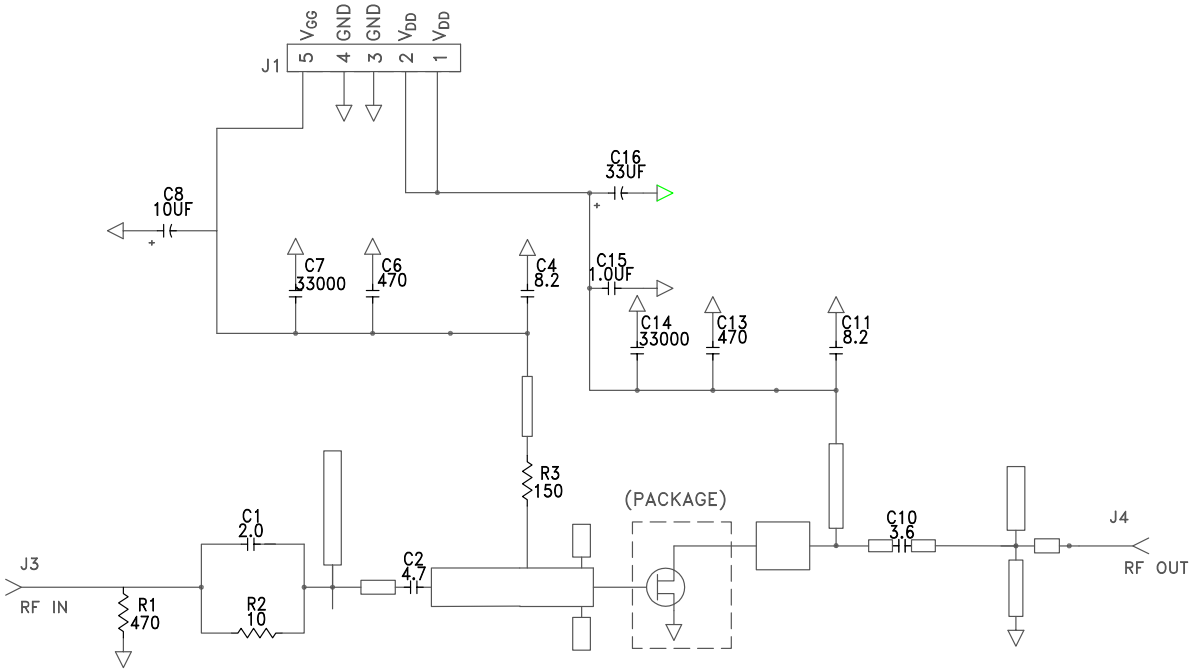
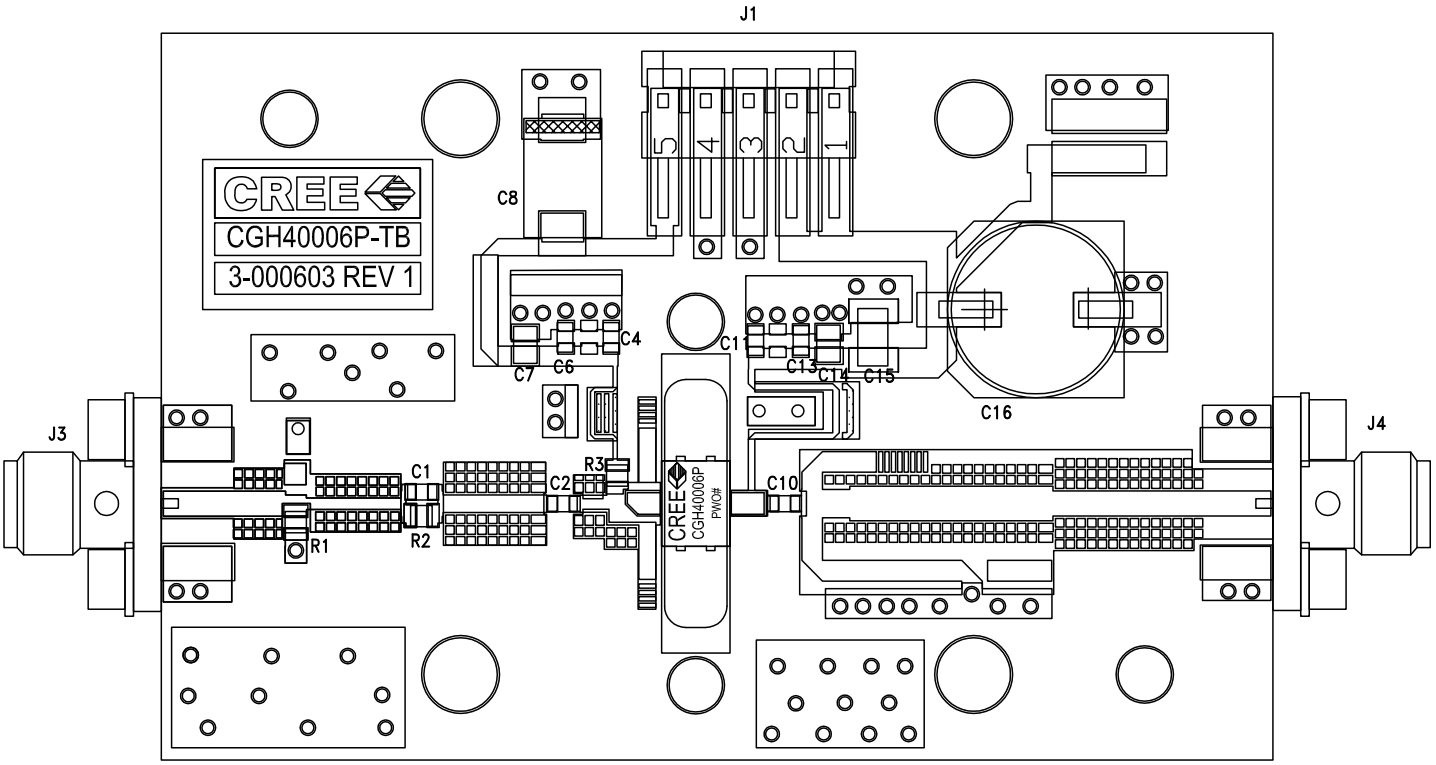
## CGH40006P-TB Demonstration Amplifier Circuit Schematic




## CGH40006P-TB Demonstration Amplifier Circuit Outline





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## Typical Package S-Parameters for CGH40006P
## (Small Signal, $V_{DS}$ = 28 V, $I_{DQ}$ = 100 mA, angle in degrees)

| Frequency | Mag S11 | Ang S11 | Mag S21 | Ang S21 | Mag S12 | Ang S12 | Mag S22 | Ang S22 |
|---|---|---|---|---|---|---|---|---|
| 500 MHz | 0.905 | -96.56 | 18.30 | 120.62 | 0.023 | 35.87 | 0.456 | -52.76 |
| 600 MHz | 0.889 | -107.98 | 16.39 | 113.31 | 0.025 | 29.63 | 0.429 | -58.98 |
| 700 MHz | 0.877 | -117.55 | 14.76 | 106.99 | 0.026 | 24.39 | 0.408 | -64.31 |
| 800 MHz | 0.867 | -125.66 | 13.37 | 101.43 | 0.027 | 19.92 | 0.393 | -68.96 |
| 900 MHz | 0.860 | -132.61 | 12.19 | 96.46 | 0.028 | 16.05 | 0.381 | -73.11 |
| 1.0 GHz | 0.854 | -138.66 | 11.18 | 91.94 | 0.028 | 12.66 | 0.374 | -76.87 |
| 1.1 GHz | 0.849 | -143.98 | 10.31 | 87.79 | 0.028 | 9.64 | 0.368 | -80.34 |
| 1.2 GHz | 0.845 | -148.73 | 9.56 | 83.92 | 0.028 | 6.92 | 0.366 | -83.57 |
| 1.3 GHz | 0.842 | -153.01 | 8.90 | 80.29 | 0.028 | 4.46 | 0.365 | -86.61 |
| 1.4 GHz | 0.839 | -156.90 | 8.33 | 76.84 | 0.028 | 2.22 | 0.365 | -89.49 |
| 1.5 GHz | 0.837 | -160.49 | 7.82 | 73.56 | 0.028 | 0.15 | 0.367 | -92.24 |
| 1.6 GHz | 0.835 | -163.81 | 7.37 | 70.40 | 0.028 | -1.75 | 0.369 | -94.88 |
| 1.7 GHz | 0.833 | -166.92 | 6.96 | 67.36 | 0.028 | -3.51 | 0.373 | -97.43 |
| 1.8 GHz | 0.832 | -169.85 | 6.60 | 64.41 | 0.028 | -5.15 | 0.376 | -99.88 |
| 1.9 GHz | 0.830 | -172.62 | 6.27 | 61.54 | 0.028 | -6.67 | 0.381 | -102.27 |
| 2.0 GHz | 0.829 | -175.27 | 5.98 | 58.74 | 0.028 | -8.08 | 0.386 | -104.58 |
| 2.1 GHz | 0.828 | -177.81 | 5.71 | 56.00 | 0.028 | -9.40 | 0.391 | -106.84 |
| 2.2 GHz | 0.827 | 179.75 | 5.46 | 53.32 | 0.027 | -10.61 | 0.396 | -109.04 |
| 2.3 GHz | 0.826 | 177.38 | 5.24 | 50.68 | 0.027 | -11.73 | 0.401 | -111.19 |
| 2.4 GHz | 0.825 | 175.07 | 5.03 | 48.09 | 0.027 | -12.77 | 0.407 | -113.29 |
| 2.5 GHz | 0.824 | 172.82 | 4.84 | 45.53 | 0.027 | -13.71 | 0.412 | -115.36 |
| 2.6 GHz | 0.823 | 170.61 | 4.67 | 43.00 | 0.026 | -14.57 | 0.418 | -117.38 |
| 2.7 GHz | 0.821 | 168.44 | 4.51 | 40.50 | 0.026 | -15.34 | 0.423 | -119.36 |
| 2.8 GHz | 0.820 | 166.30 | 4.36 | 38.02 | 0.026 | -16.02 | 0.428 | -121.32 |
| 2.9 GHz | 0.819 | 164.18 | 4.22 | 35.57 | 0.026 | -16.62 | 0.434 | -123.24 |
| 3.0 GHz | 0.818 | 162.08 | 4.09 | 33.13 | 0.026 | -17.13 | 0.439 | -125.13 |
| 3.2 GHz | 0.816 | 157.91 | 3.85 | 28.31 | 0.025 | -17.89 | 0.449 | -128.84 |
| 3.4 GHz | 0.813 | 153.76 | 3.65 | 23.53 | 0.025 | -18.30 | 0.458 | -132.46 |
| 3.6 GHz | 0.810 | 149.58 | 3.47 | 18.78 | 0.025 | -18.38 | 0.467 | -136.00 |
| 3.8 GHz | 0.807 | 145.35 | 3.31 | 14.05 | 0.024 | -18.13 | 0.474 | -139.48 |
| 4.0 GHz | 0.804 | 141.05 | 3.18 | 9.32 | 0.024 | -17.60 | 0.481 | -142.91 |
| 4.2 GHz | 0.801 | 136.66 | 3.05 | 4.57 | 0.024 | -16.82 | 0.488 | -146.30 |
| 4.4 GHz | 0.797 | 132.15 | 2.94 | -0.20 | 0.025 | -15.89 | 0.493 | -149.67 |
| 4.6 GHz | 0.793 | 127.50 | 2.85 | -5.01 | 0.025 | -14.87 | 0.497 | -153.02 |
| 4.8 GHz | 0.789 | 122.70 | 2.76 | -9.86 | 0.026 | -13.89 | 0.500 | -156.37 |
| 5.0 GHz | 0.785 | 117.72 | 2.68 | -14.79 | 0.027 | -13.04 | 0.503 | -159.74 |
| 5.2 GHz | 0.780 | 112.55 | 2.62 | -19.78 | 0.029 | -12.42 | 0.504 | -163.14 |
| 5.4 GHz | 0.776 | 107.17 | 2.55 | -24.86 | 0.030 | -12.13 | 0.505 | -166.59 |
| 5.6 GHz | 0.772 | 101.58 | 2.50 | -30.03 | 0.032 | -12.22 | 0.504 | -170.10 |
| 5.8 GHz | 0.768 | 95.76 | 2.44 | -35.30 | 0.035 | -12.75 | 0.503 | -173.70 |
| 6.0 GHz | 0.764 | 89.70 | 2.40 | -40.69 | 0.037 | -13.73 | 0.501 | -177.41 |

Download this s-parameter file in ".s2p" format at http://www.cree.com/products/wireless_s-parameters.asp



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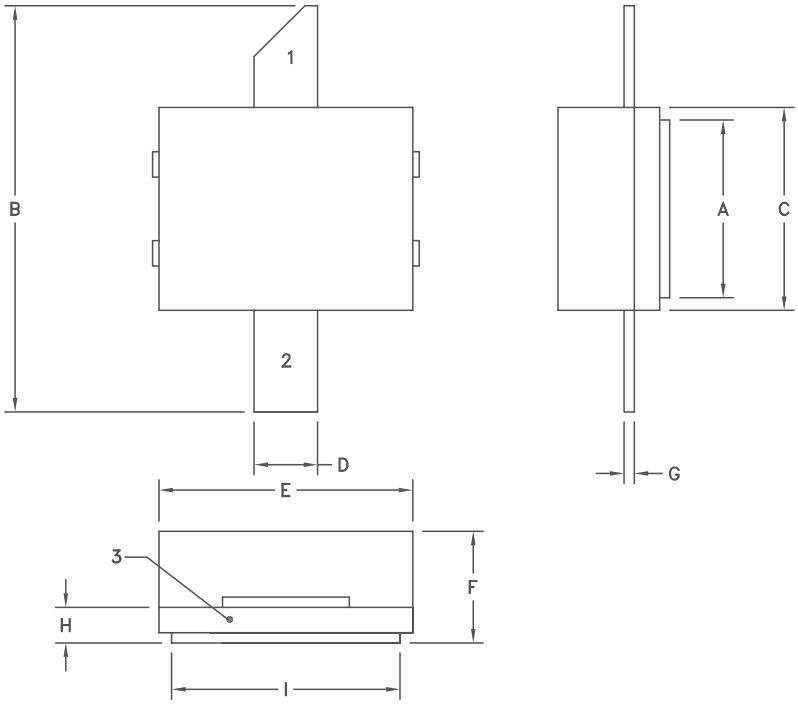
## Product Dimensions CGH40006P (Package Type — 440109)




NOTES: (UNLESS OTHERWISE SPECIFIED)

1. INTERPRET DRAWING IN ACCORDANCE WITH ANSI Y14.5M–1982 DIMENSIONING AND TOLERANCING.
2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | .135 | .145 | 3.43 | 3.68 |
| B | .315 | .325 | 8.00 | 8.26 |
| C | .155 | .165 | 3.94 | 4.19 |
| D | .045 | .055 | 1.14 | 1.40 |
| E | .195 | .205 | 4.95 | 5.21 |
| F | .090 | .110 | 2.29 | 2.79 |
| G | .007 | .009 | .178 | 0.23 |
| H | .026 | .030 | .660 | .762 |
| I | .175 | .185 | 4.45 | 4.70 |

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE





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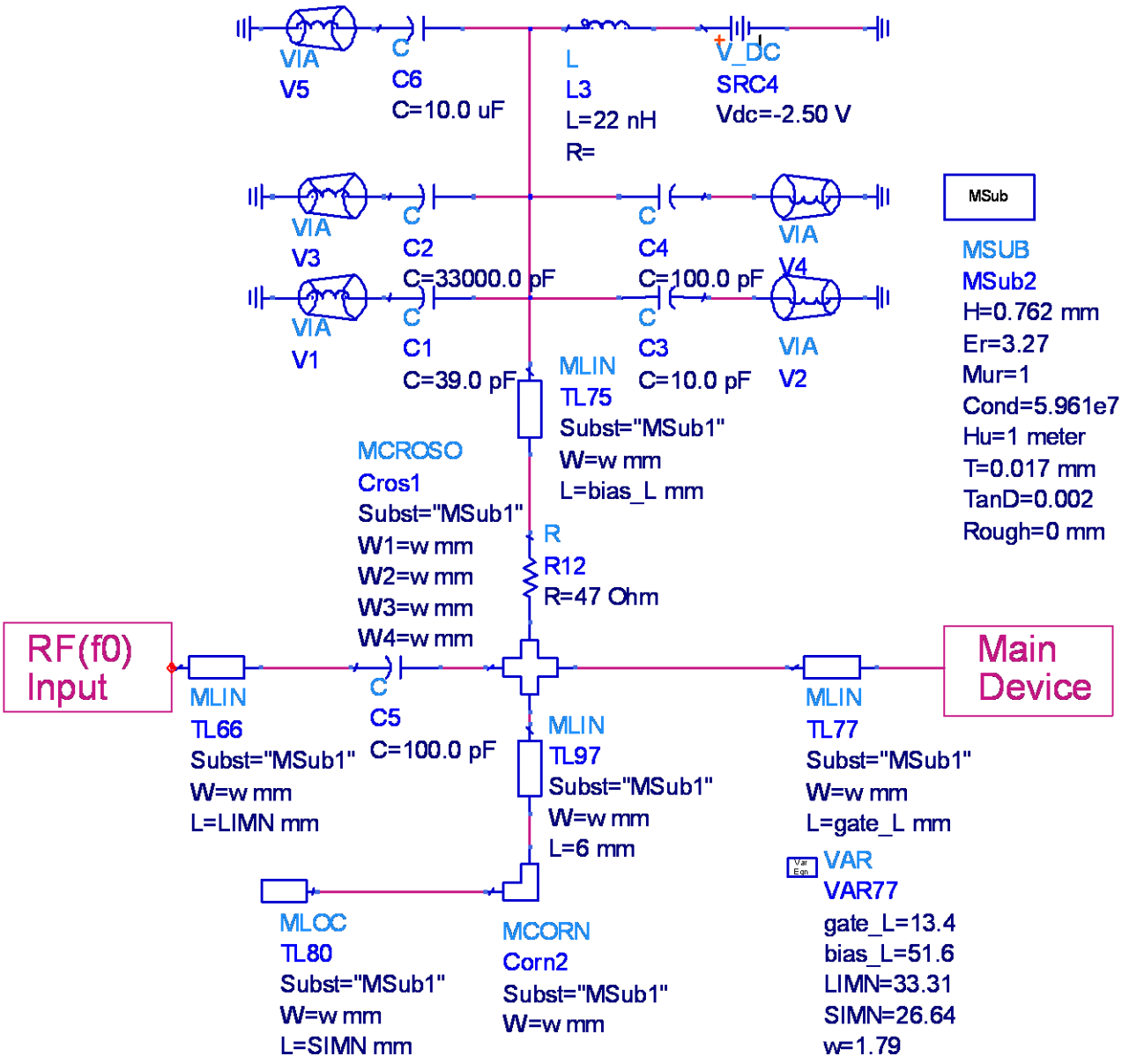
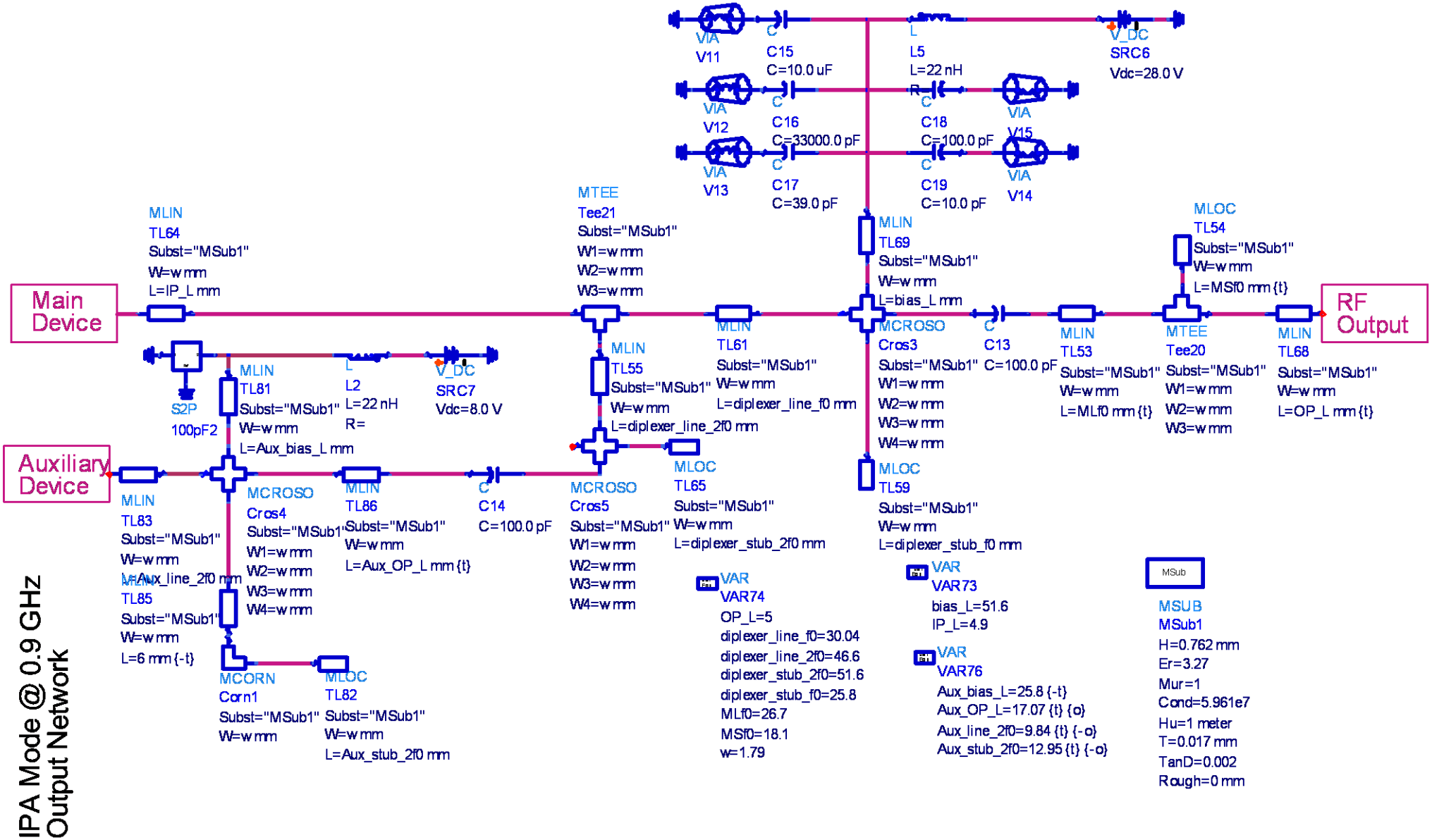
# *Appendix C*

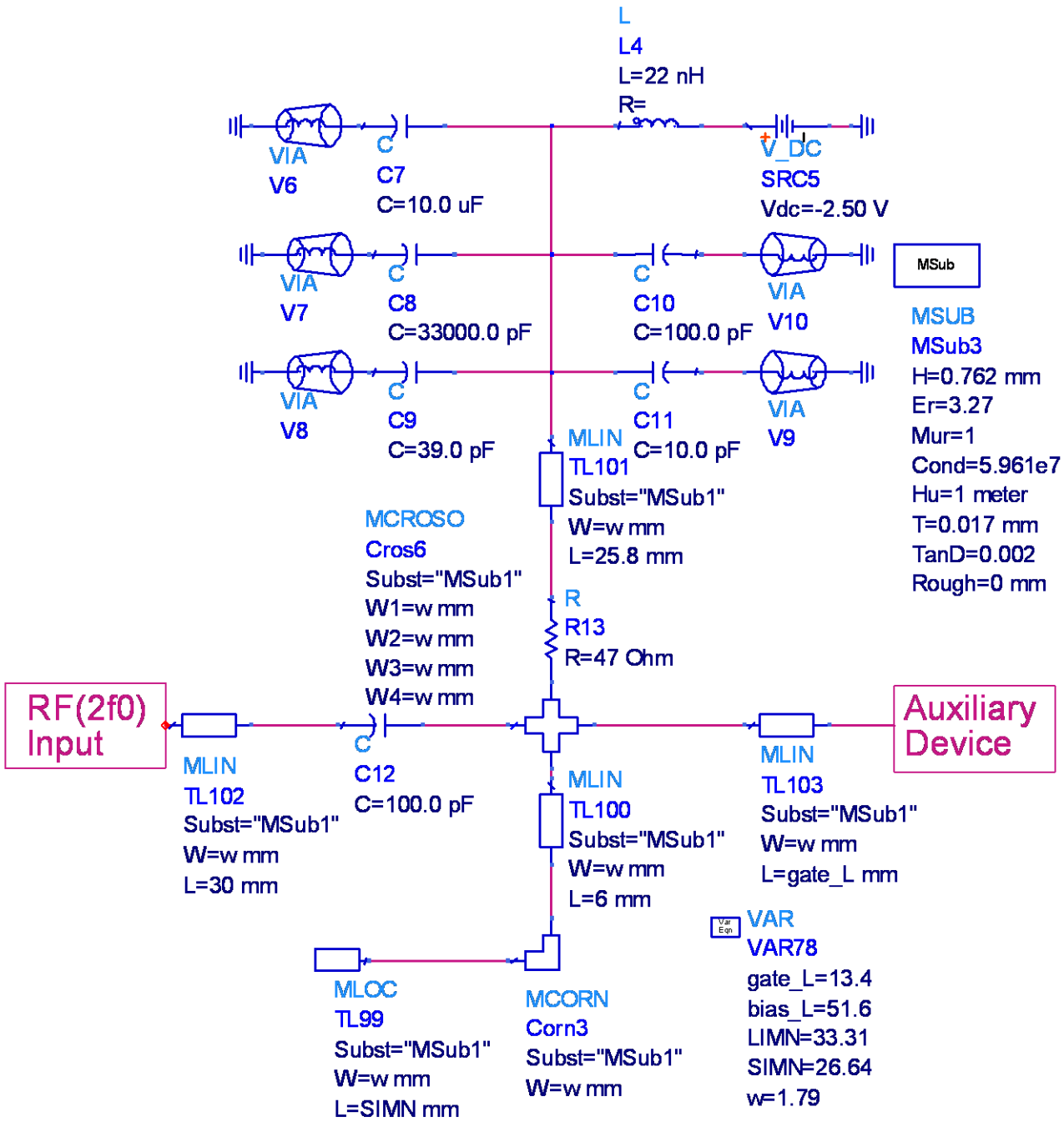
# Narrowband IPA Design Schematic

# IPA Mode @ 0.9 GHz
# Input Network (Main Device)




IPA Mode @ 0.9 GHz
Output Network
Main Device
Auxiliary Device
RF Output
VIA V11
C C15 C=10.0 uF
L L5 L=22 nH
V_DC SRC6 Vdc=28.0 V
VIA V12
C C16 C=33000.0 pF
C C18 C=100.0 pF
VIA V15
VIA V13
C C17 C=39.0 pF
C C19 C=10.0 pF
VIA V14
MLIN TL64 Subst="MSub1" W=w mm L=IP_L mm
MTEE Tee21 Subst="MSub1" W1=w mm W2=w mm W3=w mm
MLIN TL69 Subst="MSub1" W=w mm L=bias_L mm
MLOC TL54 Subst="MSub1" W=w mm L=MSf0 mm {t}
S2P 100pF2
MLIN TL81 Subst="MSub1" W=w mm L=Aux_bias_L mm
L L2 L=22 nH R=
V_DC SRC7 Vdc=8.0 V
MLIN TL55 Subst="MSub1" W=w mm L=diplexer_line_2f0 mm
MLIN TL61 Subst="MSub1" W=w mm L=diplexer_line_f0 mm
MCROSO Cros3 Subst="MSub1" W1=w mm W2=w mm W3=w mm W4=w mm
C C13 C=100.0 pF
MLIN TL53 Subst="MSub1" W=w mm L=MLf0 mm {t}
MTEE Tee20 Subst="MSub1" W1=w mm W2=w mm W3=w mm
MLIN TL68 Subst="MSub1" W=w mm L=OP_L mm {t}
MLIN TL83 Subst="MSub1" W=w mm L=Aux_line_2f0 mm
MCROSO Cros4 Subst="MSub1" W1=w mm W2=w mm W3=w mm W4=w mm
MLIN TL86 Subst="MSub1" W=w mm L=Aux_OP_L mm {t}
C C14 C=100.0 pF
MCROSO Cros5 Subst="MSub1" W1=w mm W2=w mm W3=w mm W4=w mm
MLOC TL65 Subst="MSub1" W=w mm L=diplexer_stub_2f0 mm
MLOC TL59 Subst="MSub1" W=w mm L=diplexer_stub_f0 mm
MLIN TL85 Subst="MSub1" W=w mm L=6 mm {-t}
MCORN Corn1 Subst="MSub1" W=w mm
MLOC TL82 Subst="MSub1" W=w mm L=Aux_stub_2f0 mm
VAR VAR74 OP_L=5 diplexer_line_f0=30.04 diplexer_line_2f0=46.6 diplexer_stub_2f0=51.6 diplexer_stub_f0=25.8 MLf0=26.7 MSf0=18.1 w=1.79
VAR VAR73 bias_L=51.6 IP_L=4.9
VAR VAR76 Aux_bias_L=25.8 {-t} Aux_OP_L=17.07 {t} {o} Aux_line_2f0=9.84 {t} {-o} Aux_stub_2f0=12.95 {t} {-o}
MSub MSUB MSub1 H=0.762 mm Er=3.27 Mur=1 Cond=5.961e7 Hu=1 meter T=0.017 mm TanD=0.002 Rough=0 mm

# IPA Mode @ 0.9 GHz
# Input Network (Auxiliary Device)



# *Appendix D*

# Stabilising Circuit for Wideband Design

A stabilising circuit with a series resistive loading of 10 $\Omega$ and a shunt resistance of 47 $\Omega$ with a bank of shorting capacitance was used to attain unconditional stability (i.e., k-factor >1 in Eq. 4.5) across in band and out of band frequencies. The gain at the high frequency range can be improved by adding a capacitor parallel to the series resistive loading (Fig. 6.7). The impedance of the capacitance needed to be lower than $R_s = 10\,\Omega$ at frequency greater than 2 GHz:

$$X_c = \frac{1}{w \cdot C} < 10$$

therefore

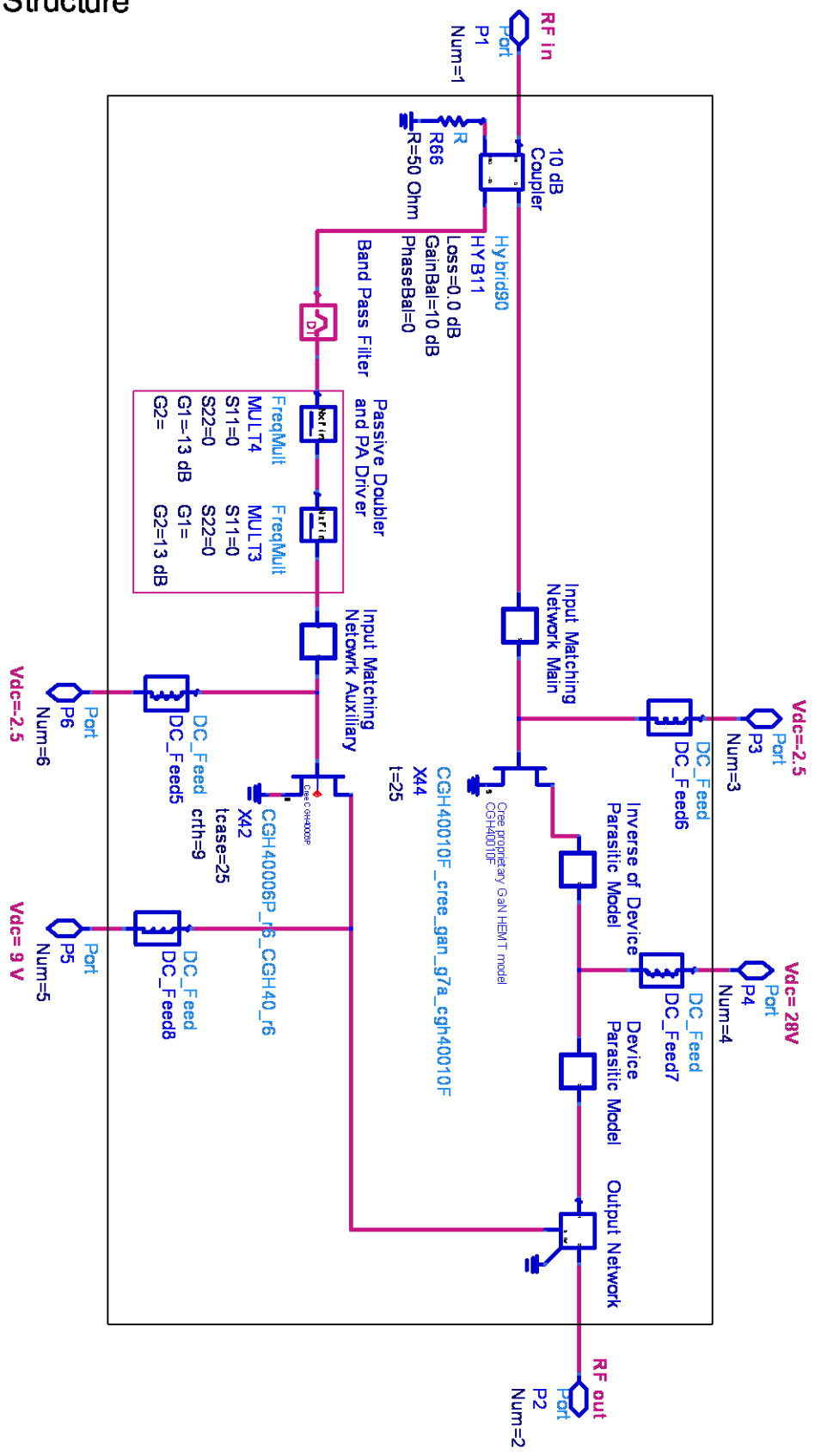
$$C > \frac{a}{2 \cdot pi \cdot (2GHz) \cdot 10} = 8pf$$

Therefore, any value greater than $C = 10pF$ can be chosen.

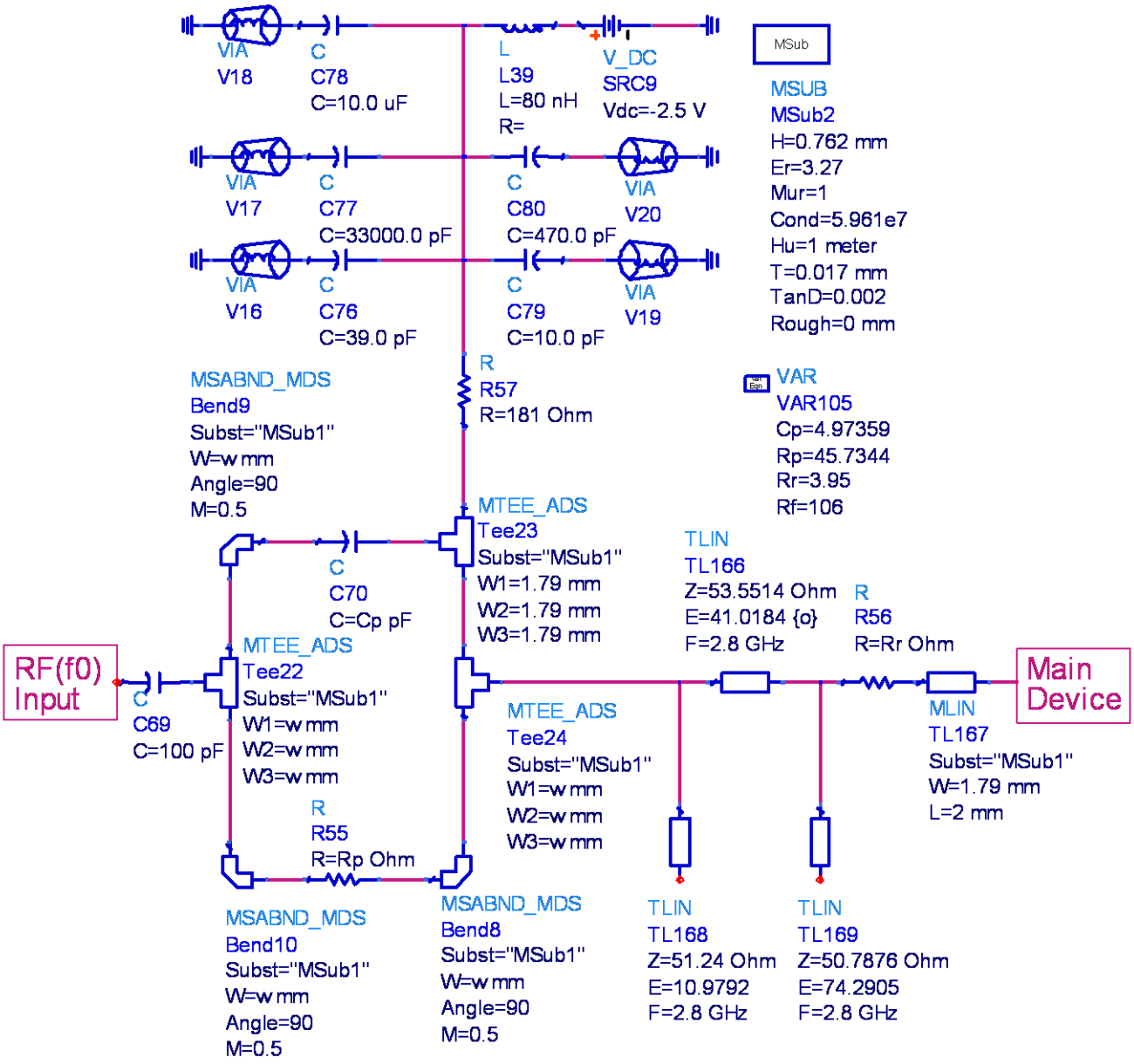
# *Appendix E*

# Wideband Multi-Mode Design Schematic

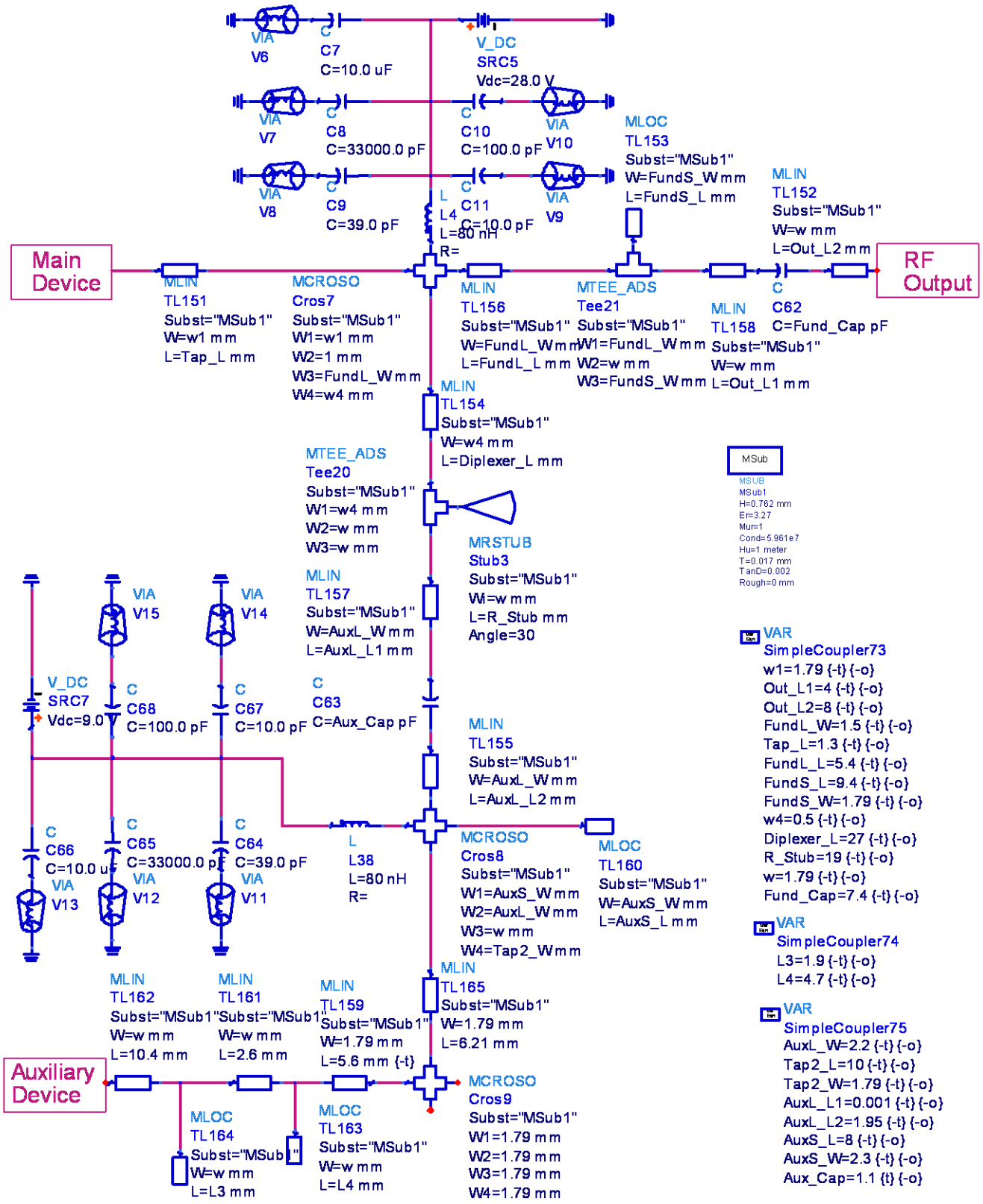
IPA Mode
Wideband Design
Full Structure



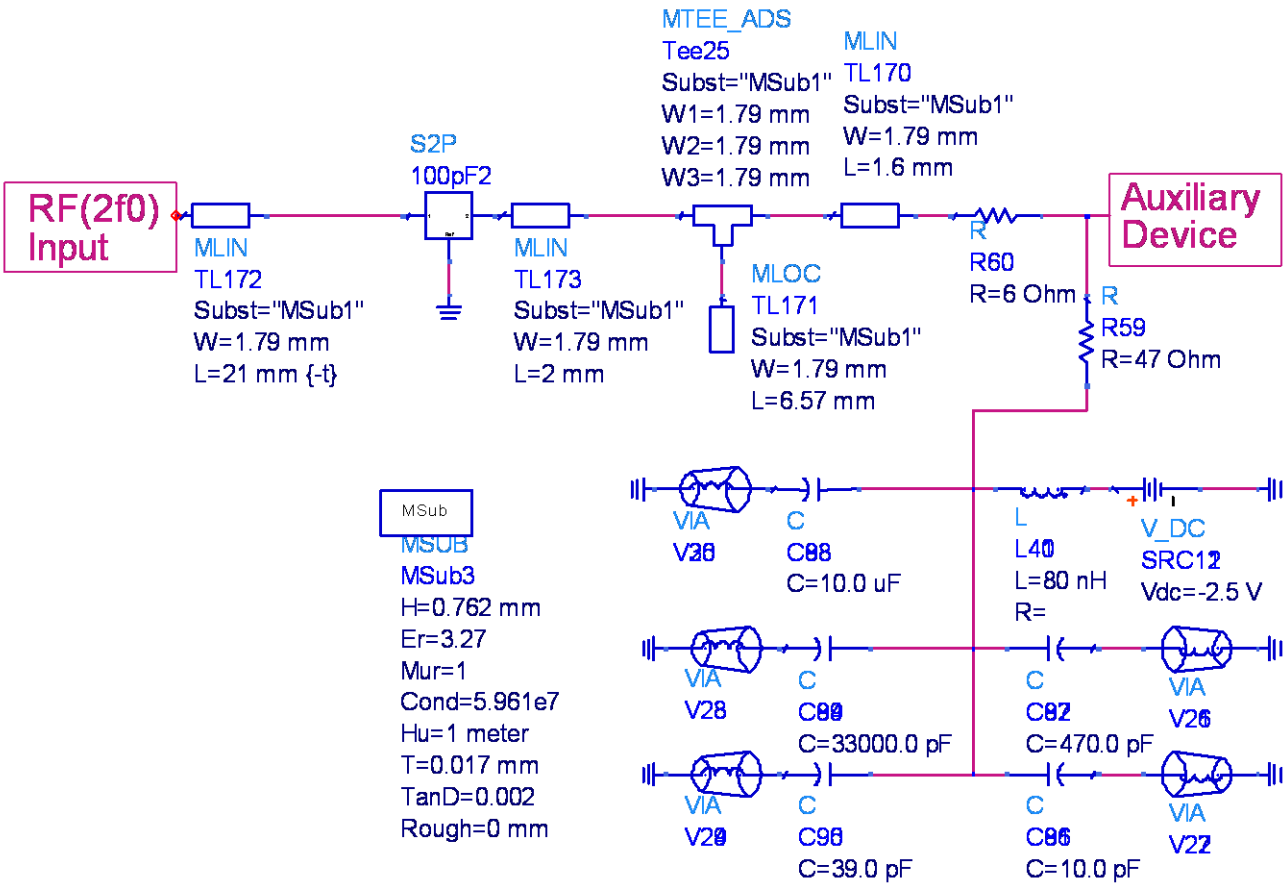
# IPA Mode
# Wideband Design
# Input Network (Main Device)



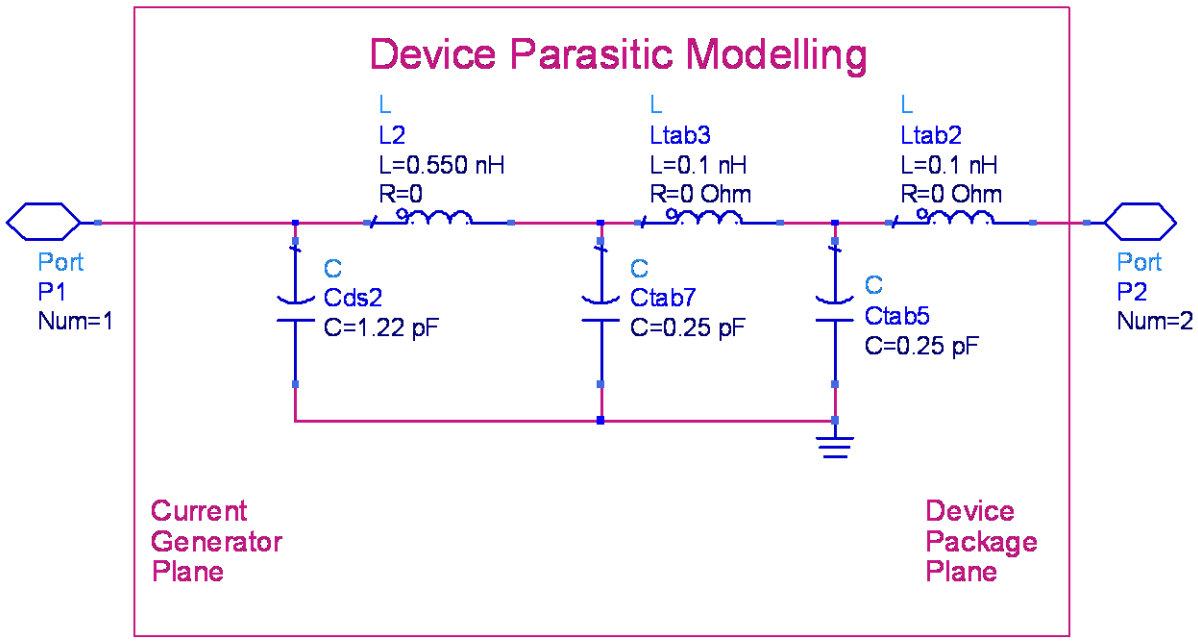
IPA Mode
Wideband Design
Output Network



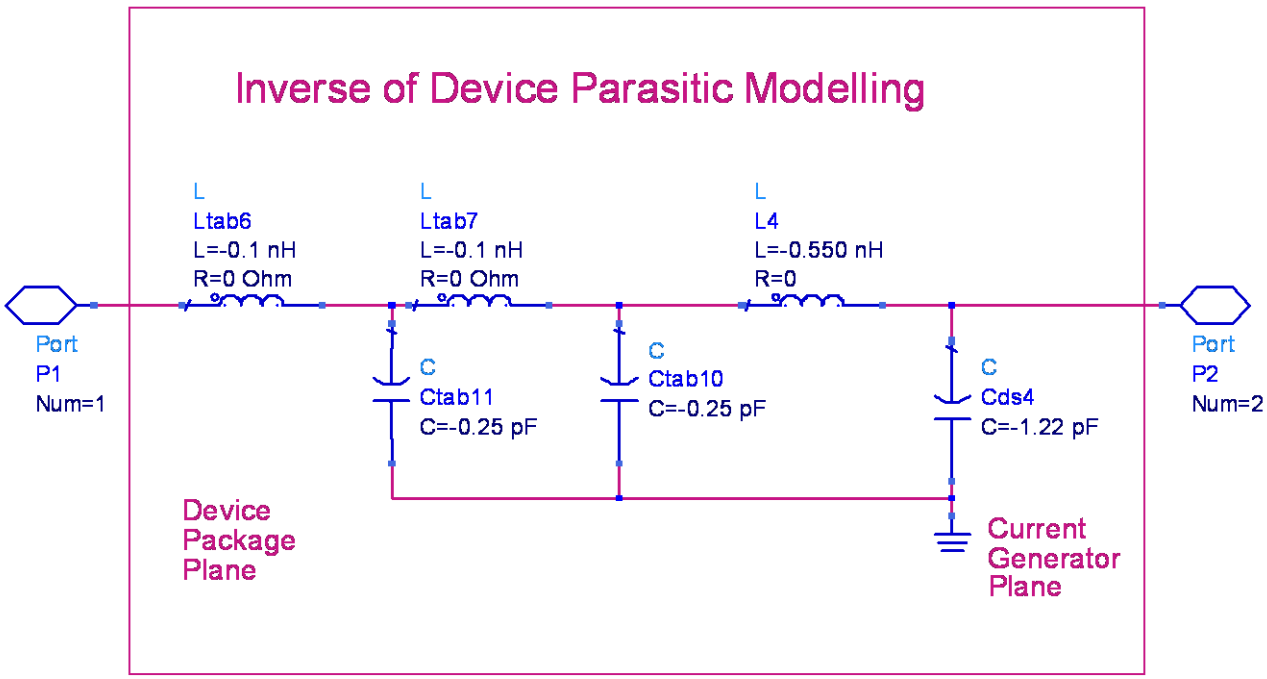
# IPA Mode
# Wideband Design
# Input Network (Auxiliary Device)



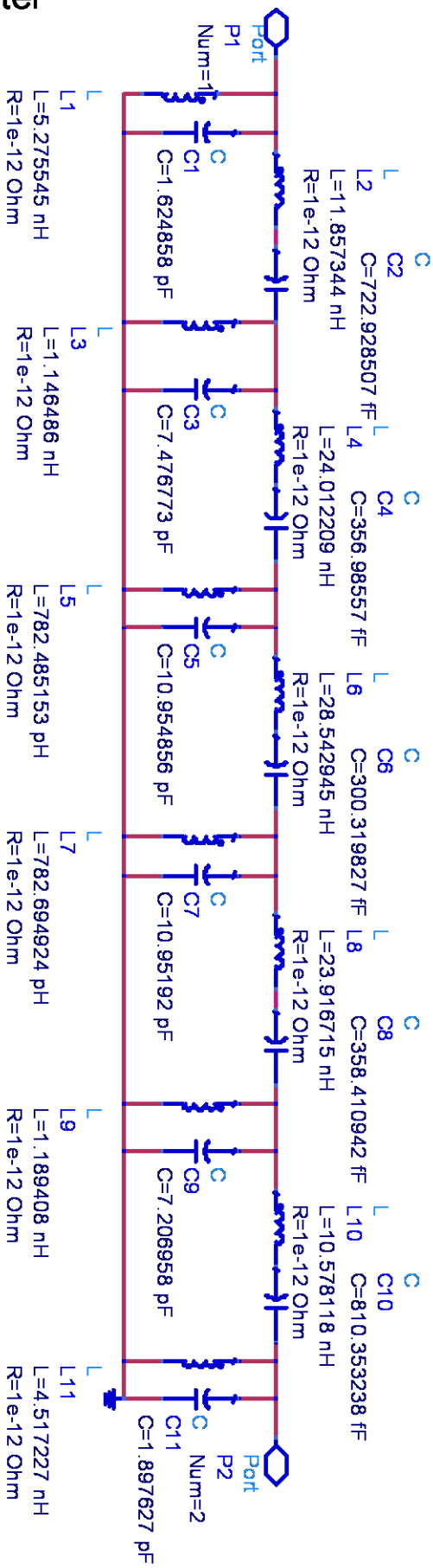
# Device Parasitic Modelling



# Inverse of Device Parasitic Modelling



# Band Pass Filter



# Publications

**1-**
**"Novel wide band high-efficiency active harmonic injection power amplifier concept**
**AlMuhaisen, A.; Wright, P.; Lees, J.; Tasker, P. J.; Cripps, S. C. & Benedikt, J.**
**2010 IEEE MTT-S International"**

# Novel Wide Band High-Efficiency Active Harmonic Injection Power Amplifier Concept

Abdullah AlMuhaisen, Peter Wright, J. Lees, P. J. Tasker, Steve C. Cripps and J. Benedikt

Centre for High Frequency Engineering, Cardiff School of Engineering, Cardiff University, Cardiff, UK

***Abstract* — This paper introduces a novel approach for the realization of wide band (>octave) high-efficiency (>95%) high Power Amplifiers (PAs). The proposed concept utilizes active harmonic injection to achieve the appropriate waveform shaping of the voltage/current waveforms necessary to deliver simultaneously both high power and high efficiency operation. The new PA structure thus consists of two parallel PAs where the main PA generates fundamental power and an auxiliary PA injects a harmonic signal at the output of the main PA to perform waveform shaping. An active harmonic injection PA circuit designed around the 10 W GaN transistor is demonstrated, along with the basic mathematical analysis and computer simulation of this new mode of operation. The measured performance of the PA demonstrator realized at 0.9 GHz provided a drain efficiency of 74.3% at P1dB, validating the concept and its potential.**

***Index Terms* — Broadband amplifiers, high efficiency, injection amplifiers, microwave amplifiers, power amplifiers.**

## I. Introduction

In many communication and radar systems there is an increasing need to improve the functionality of the Power Amplifier (PA) to meet new system specifications; definitely in terms of output power, bandwidth, efficiency and often also linearity. For example, wireless communication systems consume significant electric power with the component consuming the largest amount of power being the Power Amplifier (PA), thus the importance of improving their efficiency.

Fundamentally the only way to improve the efficiency of a Power Amplifier is to use harmonic injection to provide for wave shaping of the RF output voltage/current waveforms. This harmonic injection is typically achieved by presenting appropriate passive reactive output load terminations at the harmonics. Power Amplifiers operating in the traditional class B (78.5%) and F (100%) modes are all examples of this approach. Generally these modes, since they require high Q-factor short and/or open circuit terminations, provide solutions that are inherently narrow band.

More recently and alternative mode of operation, class J (78.5%), was introduced that requires only reactive second harmonic terminations [1]. Additionally by exploiting the newly highlighted design continuum combining both the Class B and J modes this bandwidth limitation can be partially overcome. Recently a PA demonstrating high efficiency (>60%) over a 60% bandwidth has been demonstrated [2]. However, the maximum theoretical efficiency of this approach is only 78.5% and it cannot address systems requiring over an octave bandwidth.

This paper introduces a novel power amplifier approach, which utilizes active rather than passive second harmonic injection, to address these theoretical limitations on efficiency and bandwidth associated with passive second harmonic injection. The paper starts with an investigation of optimum waveforms that would deliver best performance in terms of efficiency and power. Next, the active load pull system developed by Cardiff University [3] was used to experimentally investigate whether the 10 W GaN transistor can support these optimum waveforms. Finally, a prototype amplifier test structure based on this new topology is designed, simulated, built and measured to demonstrate its feasibility.

## II. Theoretical Analysis

### *1. Passive Second Harmonic Injection*

In Class B and J amplifiers the transistor is initially biased so that, ideally, the resulting current waveform is shaped to provide a half rectified sinusoid. The key feature of the half rectified sinusoid is that over the same maximum current swing it provides for same fundamental signal as the sinusoidal waveform but importantly it has a reduced $(2/\pi)$ DC component, hence providing for an increase of $(\pi/2)$ efficiency. In Class B a short circuit at the second harmonic is used to shape the voltage waveform to a simple sinusoid. While in class J an appropriate fundamental and second harmonic reactive termination is used to shape the voltage waveform into a band limited half rectified sinusoid. In both these cases it is assumed that all higher harmonics are passively terminated into low impedance, in which case they both have a maximum theoretical efficiency of 78.5%.

### *2. Active Second Harmonic Injection*

On close inspection it is observed that the performance potential of the Class J current and voltage waveforms is limited by the constraint of requiring passive harmonic injection. The two half rectified waveforms are offset by 135 rather than the optimum 180 case; the value required for a real only fundamental load (maximum output power) and to minimize current and voltage waveforms overlap (maximum efficiency).

The voltage and current waveforms in the optimum case are given by the following equations:

$$v(\theta) = V_{dc}\left[1 - \sqrt{2}\cos(\theta) + 0.5\cos(2\theta)\right] \quad (1)$$

$$i(\theta) = I_{max}\left[\frac{1}{\pi} + \frac{\cos(\theta)}{2} + \frac{2}{3\pi}\cos(2\theta) + \cdots\right] \quad (2)$$

Indicated that the required optimum fundamental load is given by;

$$R_f = 2\sqrt{2}V_{dc}/I_{max} \quad (3)$$

Analysis of these waveforms indicates the following output power and efficiency performance.

$$P_{dc} = 2V_{DC}\,I_{max}/\pi = 2V_1/\pi R_f = 2\sqrt{2}V_{DC}^2/\pi R_f \quad (4)$$

$$P_{out} = V_1^2/2R_f = V_{dc}^2/R_f \quad (5)$$

$$\eta_{Drain} = P_{out}/P_{dc} = \pi/2\sqrt{2} = 111\ \% \quad (6)$$

Obviously efficiency greater than 100% is not theoretically possible. Further analysis of the current and voltage waveforms indicates that the required load impedance at the second harmonic is negative and is given by;

$$R_{2f} = -\frac{3\pi}{4}V_{dc}/I_{max} \quad (7)$$

While this is not possible with passive second harmonic injection it is achievable if active second harmonic injection is utilized. However, in this case the efficiency calculation must be modified, as follows, to include the addition of this energy input.

$$\eta_{IPA\ Drain} = P_{out}/(P_{dc} + (P_{dc0}/\eta_0)) \quad (8)$$

where $P_{dc0}$ and $\eta_0$ are the DC power and efficiency of the generated harmonic power. The modified drain efficiency calculation shows that the efficiency of the second harmonic PA is important for achieving high overall efficiency. Table (1) shows the predicted theoretical performance when the efficiency of the second harmonic PA is 100% and 50% respectively.

For $V_{dc} = 1$ V and $I_{max} = 2$ A;

TABLE 1
PERFORMANCE PARAMETERS

| | $P_{dc}(W)$ | $P_{out}(W)$ | $PUF^1(dB)$ | $V_{max}(V)$ | $\eta_{Drain}(\%)$ |
|---|---|---|---|---|---|
| $ClassB$ | $2/\pi$ | $1/2$ | 0 | 2 | 78.5 |
| $IPA^{2nd}$ 100% | $\frac{2}{\pi}+\frac{2}{6\pi}$ | $1/\sqrt{2}$ | 1.5 | 2.9 | 95.2 |
| $IPA^{2nd}$ 50% | $\frac{2}{\pi}+\frac{4}{6\pi}$ | $1/\sqrt{2}$ | 1.5 | 2.9 | 83.3 |

The results show that even when the second harmonic power is fully accounted for and with realistic efficiency values for the second harmonic power generator that the active injection second harmonic Power Amplifier (IPA) has the potential to provide for efficiencies over 80%. The bandwidth advantage expected is inherently associated with such mode of operation since the fundamental matching can be broadband covering multiple octaves and harmonic impedances can be actively adjusted using broadband PAs such as multi octave class-A PA design. Moreover, the expected power of IPA will be around 50% enhanced relative to class-B equivalent.

## III. TRANSISTOR VALIDATION

To validate these theoretical results experimental transistor investigations were undertaken using the previously developed waveform measurement and engineering system at Cardiff University. Since these measurements system utilized active harmonic load-pull they can provide the negative impedances necessary to experimentally demonstrate the IPA mode of operation on the selected 10W packaged GaN device. For the appropriate comparison with theory the V/I waveforms at the current generator plane of the packaged device are required, hence a package parasitic de-embedding process [4] was used.

### *A. Measurement and Results*

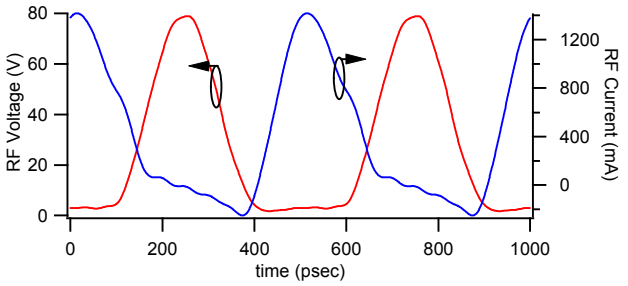



Fig. 1 Voltage/Current waveforms de-embedded to the current generator plane

In order to achieve the required half rectified class-B current waveform the 10 W GaN device was biased around pinch-off at a 28V drain voltage. The active load pull measurement started from inverted class-F optimum fundamental loading condition [5]. The active second harmonic loop was then used to inject energy at the second harmonic to appropriately shape the voltage waveform; targeting a band-limited half rectified waveform offset by 180 from the current waveform. The measured V/I waveforms achieved at the current generator plane are shown in Fig.1. It clearly demonstrates that transistor can support this mode of operation. The required optimum load reflection coefficient of the second harmonic measured is 4 with a phase of 178° relative to the fundamental load reflection coefficient.

The dynamic RF load line for this IPA mode is shown in Fig. 2 and is compared to that achieved for class-B operation; passive harmonic injection into the same fundamental load at the same drive level. In the Class-B case the transistor is clearly overdriven in contrast to the IPA mode. In the IPA the active injected second harmonic voltage component allowing the fundamental voltage component to be increased without

[1] This is Power Utilization Factor [1] which shows the power capability of a device referenced to class-B output power

forcing the current into a clipping regime and consequently as theoretically predicted both the RF output power and efficiency increases.

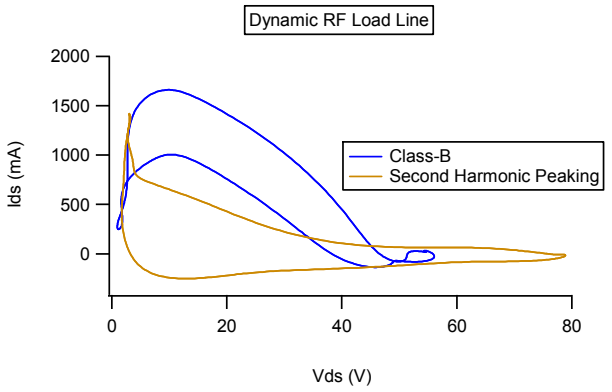



Fig. 2 RF load line of class-B and IPA de-embedded to the current generator plane

*B. Discussion*

The measured efficiency, taking into account the RF energy injected at the second harmonic is 92%. This is very close to that predicted theoretically which is 95.2% (correspond to that predicted for a 100% efficient second harmonic generator). The reduction of efficiency can be associated with the knee effect which will limit the minimum voltage value. Considering knee effect in drain efficiency calculation predicts an efficiency of 90.4%:

$$\eta_{\text{IPA Drain}} = P_{RF}/\left(P_{dc}(1 + V_k/V_{dc}) + (P_{dc0}/\eta_0)\right) \quad (9)$$

$$= 90.4\%$$

where $V_k = 1.74$ V is the measured minimum voltage value. The measured efficiency is slightly higher than the theoretical value and possibly this is the advantageous effect of the higher harmonic voltage components produced by the system impedance.

Also as theoretically predicted the measured output power in this IPA mode has increased by 2 dB. This is in part due to the injected second harmonic power contributing around 1 dB of the change. This outcome highlights an alternative interpretation of how this amplifier works. The resulting waveform shaping allow for the conversion of RF power injected at the second harmonic to a RF power at the fundamental frequency [6]. These results show that significant advantages can be gained from second harmonic injection in terms of efficiency, power and possibly bandwidth.

## IV. PA Demonstrator

A. *Proposed Topology*

The proposed Injection Power Amplifier (IPA) consists of two paths where the upper one (Fig. 3) generates the main fundamental radio frequency (RF) signal and a lower path with a voltage source/auxiliary PA to control the V/I waveforms of the main PA by injecting the even harmonics of the fundamental signal, resulting in the V/I waveforms being shaped for better PA performance in terms of power, efficiency and bandwidth. The baseband information (BB) are up converted by Local Oscillator (LO) through this constant LO power and the fundamental signal is up converted to second harmonic by a doubler. This solution of generating the second harmonic is just a suggestion and could be realised by other circuit topologies.

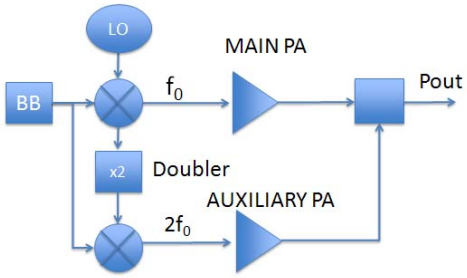



Fig. 3 Proposed topology

*B. PA Demonstrator Design*

For the purpose of proof of concept and simplicity, the actual realized PA demonstrator consists of two 10 W GaN HEMT (High Electron Mobility Transistor) devices (CGH40010F) biased at class-B and an output matching network consisting of a simple multiplexer and impedance transformers. The devices have been chosen since they are commercially available; nonlinear model exist and provide relatively high output power levels. The board used is a high frequency laminate board (TMM3) from Rogers Corporation. Input drive is achieved using two ESGs (Electronic Signal Generators); hence one is used to generate the second harmonic signal instead of a doubler and thus feeds the auxiliary PA directly.

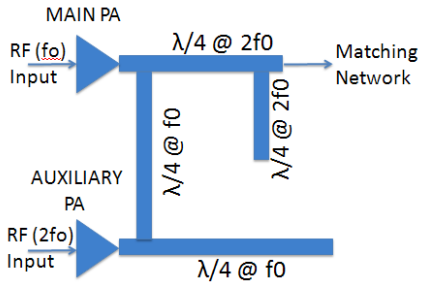



Fig. 4 Multiplexer

The design starts with a multiplexer (Fig.4) where the main PA fundamental signal sees only constant load while the auxiliary PA, active second harmonic injection, sees only the main PA. Therefore, the RF fundamental signal finds its way to the load and the auxiliary PA performs the required waveform shaping.

The output matching network was designed for optimum performance according to load pull measurement while the

auxiliary PA's matching network was designed based on ADS simulation for maximum efficiency. Next, an optimization process in ADS has been used and the simulated results showing a drain efficiency of around 75 % at P1dB.

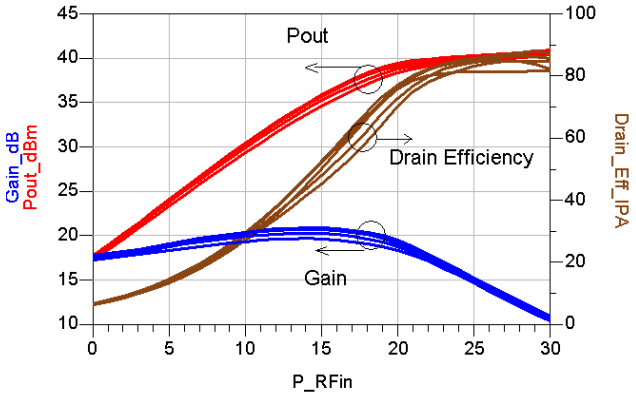



Fig. 5 IPA Simulation results for an increasing phase offset between the two input signals

It is believed that with further investigations/optimization that this value can be further increased using an optimised drive strategy as can be seen in Fig.5. However, it was felt that this design performance was sufficient to demonstrate the potential of the IPA mode of operation, hence demonstrate the feasibility of using this concept in PA design for high efficiency wide band applications. Moreover, this topology has interesting drain efficiency behaviour. It does not decrease but continues to increase as the PA is driven hard into saturation, a result that can be utilized in some applications. The predicted efficiency is 88% at 11W.

### *C. Realized PA Demonstrator*

The demonstrator PA (Fig.6) has successfully fabricated and characterized. It achieved the expected efficiency at P1dB with IPA drain efficiency of 74.3 % at 900 MHz for a yet not optimised drive strategy. The highest drain efficiency was 85.7% at the saturated output power of 10W. (Fig.7)

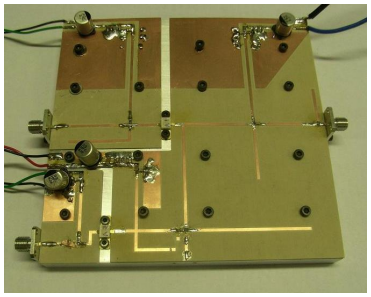


Fig. 6 Realized IPA

## V. Conclusion

A novel approach for wide band high efficiency high power amplifier has been introduced. The approach is based on the concept of using active second harmonic injection to wave shape the transistor output V/I waveforms. Theoretical analysis indicated that this concept is capable of delivering very high, >95%, efficiencies.

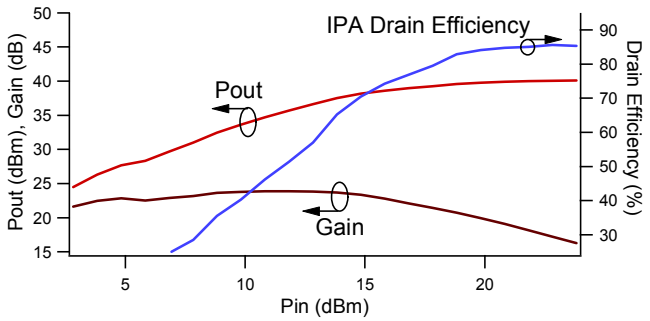



Fig. 7 IPA measurement results for a constant (and hence not yet optimized) magnitude and phase offset between the two drive signals.

This analysis fully takes into account the input energy component at the second harmonic and was confirmed by initial experimental measurements. These measurements involved both active load-pull measurements on the transistor and on a proof of concept PA structure.

## Acknowledgement

The authors would like to thank the support from Aamir Sheikh, Simon Woodington and Cree Inc. for providing the GaN device. We would also thank Saudi Government for the scholarship grant under king Abdullah scholarship program.

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# Publications

**2-**
**"Wide band high-efficiency power amplifier design**
**AlMuhaisen, A.; Lees, J.; Cripps, Steve C.; Tasker, P. J.; Benedikt, J.**
**IEEE Microwave Integrated Circuits Conference (EuMIC), 2011 European, Manchester, UK. "**

# Wide Band High-Efficiency Power Amplifier Design

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*Abstract*—**This paper presents a hybrid (passive & active) power amplifier concept for a wideband high drain efficiency power amplifier design. The proposed design integrates for the first time a dual-band PA with an active second harmonic injection to achieve high efficiency across a continuous wideband frequency range of two octaves. The design utilizes a resistively loaded class B at the lower frequencies and a class J mode of operation at the upper frequency band. To maintain high efficiency during the transition between the two PA modes an active second harmonic injection at the output of the main transistor is employed through an addition of an auxiliary low power amplifier. To demonstrate the validity of the novel concept a demonstrator is realized around a 10 W GaN transistor with an average efficiency of 63% across 0.6-2.4 GHz at only modest gain compression of 1dB.**

***Keywords-component; broadband amplifier; high efficiency; injection amplifier; microwave amplifier; power amplifiers***

## I. INTRODUCTION

In radar and communication systems there is an increasing need for a wideband and highly efficient RF transmitters. Their efficiency affects critical aspects of communication systems such as battery cost, electrical power expenses, weight of power supplies, operational time, size of cooling systems and consequently have a significant impact on the environment. The critical system in the design is the RF front-end where the Power Amplifier (PA) exhibits low power efficiencies over larger bandwidths.

The PA design for high efficiency operation requires waveform shaping of the voltage/current waveforms to achieve simultaneously high power and high efficiency PA. Basically, such operation is performed by presenting harmonic termination at the output of the transistor such as class B and class F [1]. However, designing an output matching network to present highly reflective harmonic termination for a transistor requires a high Q-factor which limits the operating bandwidth.

The newly highlighted design continuum that combines class B and class J modes achieves high efficiency (> 60%) over 60% bandwidth [2]. However, this design approach is still limited to less than an octave bandwidth after which the harmonic impedances become part of the fundamental matching network.

The dual-band PAs design represents another approach for maintaining high-efficiency operation across a larger band of frequencies. However, it does provide the required fundamental and harmonic load impedances only at selected and disjoined frequency bands with each having relatively narrow bandwidths [3]. Recently, a novel wide band high efficiency PA design has been proposed that utilized active harmonic injection [4] reducing the reliance on passive networks for the generation of suitable harmonic impedances. This PA concept therefore establishes a new design trade-off between efficiency and the operational bandwidth.

The PA design in this paper builds on the dual-band PA concept, however, it utilizes a resistively loaded class B [1] at the lower band and a class J design at the upper frequency range to increase the bandwidth of the two bands. To maintain the PA efficiency in the mid-band, during which the transition between the two modes occurs, the IPA mode is employed to overcome the limitation of the passive output matching network. Initial proof-of-concept demonstrates that this new approach for a PA design can achieve average efficiencies of 63% across two octaves.

## II. POWER AMPLIFIER DESIGN

The aim of the design is to achieve a two-octave (0.6-2.5 GHz) high efficiency design targeting mobile communication bands from 0.8-2.5 GHz. The design is based on combining different modes of operation to maximize the operating bandwidth by utilizing a hybrid design structure of passive and active injection. The resulting principle PA topology is showing in Fig.1.

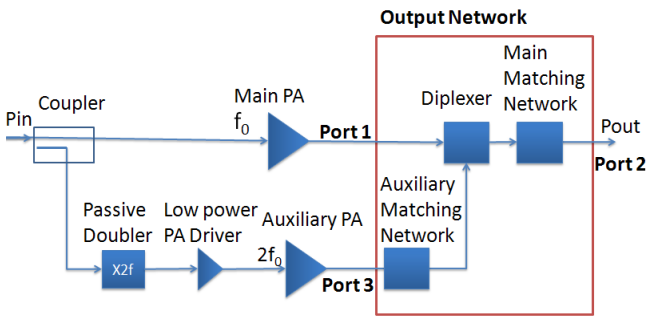


Figure 1 PA output topology

Within this structure the diplexer is an essential component as it must i) allow active injection from the auxiliary port at out of band frequencies (3.0-4.0 GHz) which present the second harmonic load termination for the mid band (1.5-2.0 GHz) while ii) also allowing the RF

fundamental signal to be transmitted from the main PA to the load with minimum losses in the operating bandwidth (0.6-2.5 GHz). The initial diplexer design [4] employed an open stub with a length of quarter wavelength line at the fundamental frequency generating a low impedance. A quarter wavelength line is then used to transform the low impedance into a higher value and connected in parallel to the main PA. The initial design, as shown in Fig. 2a, ensures a low loss transmission between the main PA and the output load at the fundamental frequency. At the second harmonic frequency a low loss connection is established between the two output of the main and auxiliary PA. Due to the use of multiple quarter wavelength lines the structure exhibits a relatively narrow bandwidth. To mitigate this quarter wavelength open stub was replaced by a radial stub in this work (Fig. 2b). The diplexer design was optimized for the fundamental frequency of 1.5-2.0 GHz.

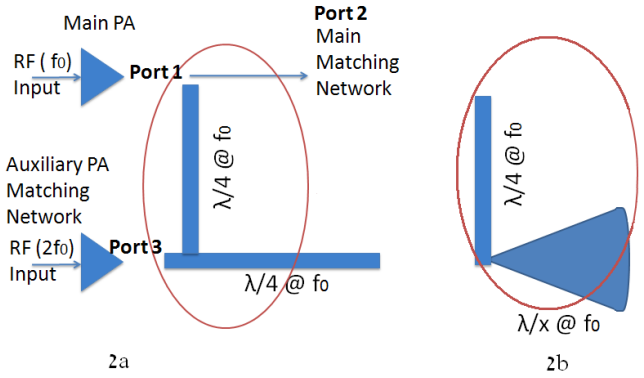


Figure 2 Diplexer design, initial (2a) and broadband design (2b).

The main matching network, as shown in Fig 1, is used to create an appropriate fundamental load condition at the main PA across the frequency range 0.6-2.5 GHz and a high reflection coefficient over the second harmonic injection bandwidth between 3.0 and 4.0 GHz. Its location after the diplexer therefore ensures the effectiveness of the second harmonic injection from the auxiliary power amplifier.

The role of the auxiliary matching network is to provide a match between the low-impedance that is established by the radial stub and the optimum impedance of the auxiliary PA stage. The auxiliary matching network also provides the second harmonic impedances to establish the class J mode of the main PA over the fundamental frequency 2.1-2.5GHz.

## III. PA Output Network Design

For the main PA a 10 W GaN HEMT (High Electron Mobility Transistor) device (CGH40010F) is utilized with drain-source bias voltage of Vds=28V. The device has been chosen for its capability of producing relatively high output powers over a large bandwidth in comparison to other technologies [5]. For the design a large signal model (supplied by Cree) is employed that has shown in previous investigations a good agreement with large-signal measurements [2]. To allow the application of fundamental power amplifier theory during the design stage, the device and package parasitics [6] were utilized to move the reference plane of the simulations and measurements towards the output current generator plane ($I_{gn}$).

### A. *Identification of target impedance*

Initial power, load-pull simulations were performed (Fig.3) identifying the required fundamental load at $I_{gn}$ (current generator plane) for each mode of operation at 0.8, 1.5 and 2.1 GHz with the second harmonic reflection coefficients for each frequency being fixed in accordance to the fundamental power amplifier theory at $0\angle 0^\circ$ (since no harmonic tuning at the lower band), $1\angle 180^\circ$ [4] and $1\angle -55^\circ$ [1] respectively. The third, fourth and fifth harmonics are shorted in all these modes.

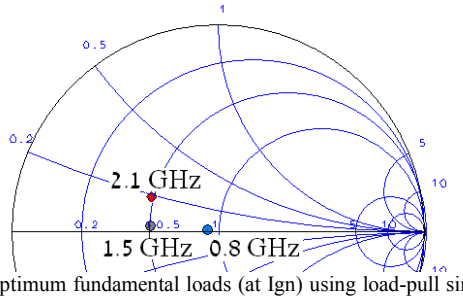


Figure 3 Optimum fundamental loads (at Ign) using load-pull simulation for a wideband high efficiency design for different mode of operations at 0.8, 1.5 and 2.1 GHz..

### B. *PA Output Matching Network Design*

The design of the main matching network (highlighted in Fig.1) consists of 50 ohm line with an open-ended stub in parallel. During the design the impact of the diplexer that is connected between the main matching network and the main device was taken into account. The simulated and measured impedances of the realized output network highlighted in Fig.1 are shown in Fig. 4. Again, to facilitate a better relationship with the fundamental power amplifier theory the reference plane of the measurements were moved towards the output current generator $I_{gn}$ using a device and package parasitics model.

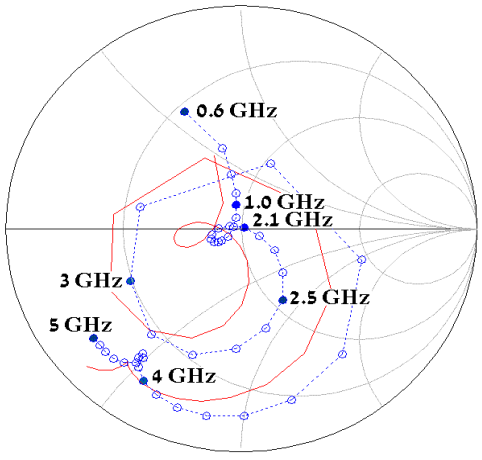


Figure 4 Simulated (solid line) and measured (dotted circle) of the input impedance (S11) of the output network as indicated in Fig.1 and then moved to the Ign plane.

The input return loss (S11) and insertion loss (S21) for the output network (Fig.1) show a good performance across 0.8-2.3 GHz band while at the edges of the operating bandwidth (0.6 and 2.5 GHz) the performance is degraded. (Fig.5)

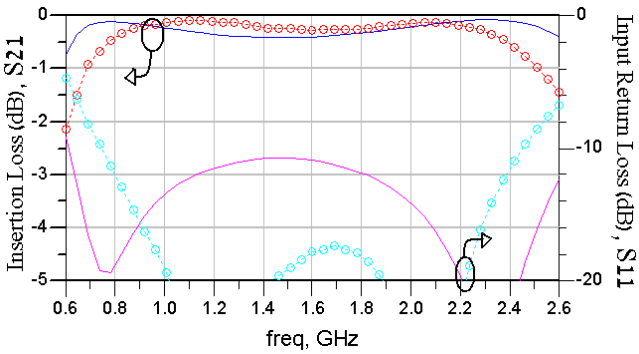


Figure 5 Simulation (dotted circle) and measurement (solid line) of insertion loss (S21) and input return loss (S11) of the output network as indicated in Fig.1.

As can be seen, the realized output matching network is only slightly offset from the real impedance within the 1.0-2.1 GHz band. At the frequencies below 1GHz the matching network present to the main device a fundamental load with an increasing reactive component towards the lower frequencies. It is therefore expected the efficiency and performance of the main PA will gradually decrease towards lower frequencies.

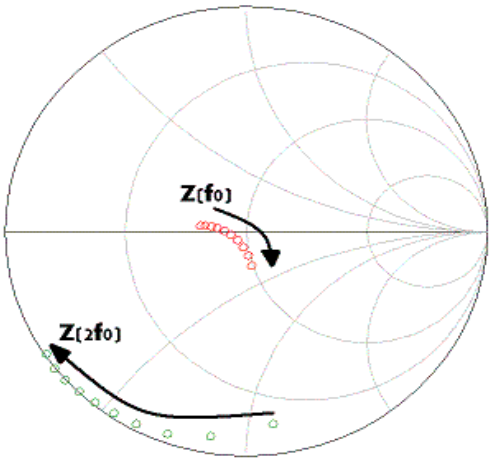


Figure 6 Simulated of the impedance (S11 as indicated in Fig.1) presented to the transistor (at Ign) for varient class J at 2.1-2.4 GHz.

Within the upper band (2.1-2.5GHz) the passive network is fully utilized to present appropriate harmonic loads to the transistor since the related harmonics are outside the operating fundamental frequency band and therefore will not limit the achievable bandwidth. Therefore, the design is optimized to operate the transistor in a variant of class J. The fundamental and second harmonic loads presented to the current generator plane of the main transistor are highlighted in Fig. 6. Because of the complexity of the realized circuit the resulting fundamental and harmonic matching in this band represents a compromise and consequently only variant of class J is created within the design rather than the ideal impedances for this mode.

## IV. Proof of Concept

The complete PA architecture, as depicted in Fig. 1, was first design and simulated to validate the initial idea. To demonstrate the performance of the design a circuit consisting of the main PA device, the designed diplexer and output matching network were realized. For the fabrication of the microstrip elements a high frequency laminate board (TMM3) from Rogers Corp was utilized.

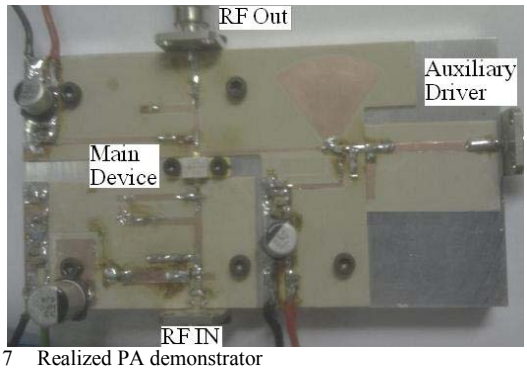


Figure 7 Realized PA demonstrator

The suggested output topology as depicted in Fig. 7 uses a signal generator source for the second harmonic injection to allow for direct observations of the second harmonic injection process. To facilitate a match between the auxiliary driver with the 50 output and the input of the diplexer a temporary matching network was created that was optimized for a frequency of 1.6 GHz.

To obtain realistic results for the efficiency the measured RF output power was divided by the DC power that was supplied to the main device and the RF second harmonic injected power (Eq.1).

$$\eta_{Drain} = P_{out} / \left( P_{DC\_Main} + P_{RF\_Auxilairy} \right) \quad (1)$$

The measured performance shows a drain efficiency of 57-75% with average efficiency of 63% across a bandwidth of 0.6-2.4 GHz at P1dB as shown in Fig. 8. It should be noted that the chosen compression at which the PA performance is measured is lower in comparison to single-stage PA designs that were reported for the same device [2]. The measured results are compared against the simulation results of the complete PA design as shown in Fig 1.

As can be seen the measurements and simulation results are in good agreement for the frequency range 0.6-1.4GHz over which the class B mode with resistively loaded harmonics was implemented.

The measurements across the 1.5-2.0 GHz frequency window demonstrate clearly the effectiveness of the IPA mode with a high drain efficiency (>70%) at 1.6 GHz for

which the temporary auxiliary matching network was optimized. This is also in good agreement with simulation results. The measured efficiency drop towards 2.0 GHz can be attributed by the need to inject high powers, which is required to maintain an appropriate magnitude ratio between the fundamental and second harmonic load [4]. For instance, at the fundamental frequency of 2.0 GHz the auxiliary driver has to inject more RF power (up to 4 W) at the second harmonic to improve the efficiency of the main device. Once this RF power is taken into account as in (1) the resulted drain efficiency is degraded. Therefore, it is expected that a complete PA design, as it is planned for the next design iteration, will result in efficiency values above 70% across 1.5-2.0 GHz as predicted by the simulations.

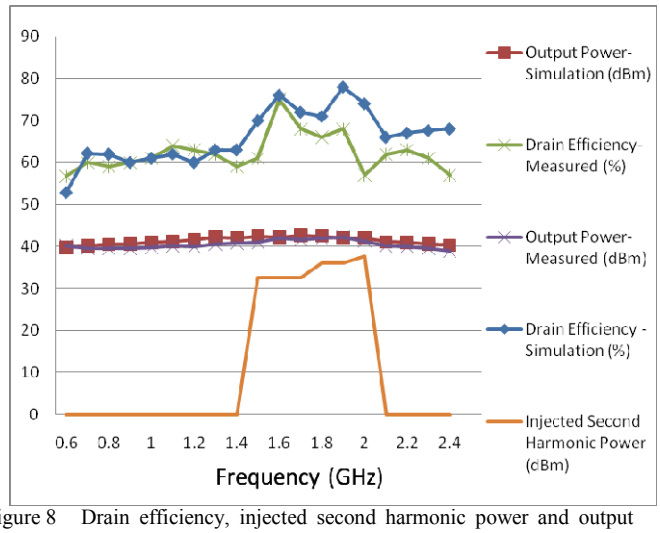


Figure 8 Drain efficiency, injected second harmonic power and output power of the PA demonstrator at P1dB for 0.6-2.4 GHz.

Table I
Measured Harmonic Power Relative to Fundamental Power

| Freq (GHz) | 0.6 | 1.0 | 1.5 | 1.9 | 2.4 |
|---|---|---|---|---|---|
| 2nd Harmonic (dBc) | -10 | -20 | -24 | -56 | -60 |
| 3rd Harmonic (dBc) | -11 | -18 | -60 | -60 | -60 |

The measured harmonic powers relative to the fundamental are shown in Table I where performance ranges from -10 dBc at the lower band and smaller than -20 dBc for 1-2.4 GHz. The relatively high harmonic power levels at the lower frequency band are a direct consequence of the resistive harmonic terminations, the highest level is at 0.6 GHz.

## V. FUTURE WORK

In the next design iteration it is planned to realise the complete PA structure as depicted in Fig.1. The presented results have highlighted the sensitivity of the PA concept to the accurate matching between the auxiliary PA stage and the diplexer design. Consequently, the focus of this design activity will be the auxiliary PA design stage and its integration over the injection frequency window of 3.0-4.0 GHz.

## VI. CONCLUSION

A novel PA concept has been proposed, designed and built that utilizes both passive and active harmonic impedance generation. The novel topology merges a dual-band PA design with an injection PA mode to obtain a continuous bandwidth over a two-octave bandwidth. The realized PA demonstrator validates this concept achieving drain efficiencies between 57% and 75% from 0.6 to 2.4 GHz at relatively small gain compression level of 1dB.

## ACKNOWLEDGMENT

The authors would like to thank Cree Inc. for providing the GaN device. We would also thank Saudi Government for the scholarship grant under king Abdullah scholarship program.

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# Publications

**3-**
**"High-speed device characterization using an active load-pull system and waveform engineering postulator**
**Carrubba, V.; Clarke, A. L.; Woodington, S. P.; McGenn, W.; Akmal, M.; AlMuhaisen, A.; Lees, J.; Cripps, S. C.; Tasker, P. J. & Benedikt, J.**
**Microwave Measurement Conference (ARFTG), 2011 77th ARFTG, 1-4. "**

# High-Speed Device Characterization Using an Active Load-Pull System and Waveform Engineering Postulator

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***ABSTRACT* — This paper presents a methodology that provides rapid estimation of the parameters necessary for the high-speed characterization of transistor devices used in modern microwave power amplifiers. The key in achieving this significant measurement speed improvement is the use of a systematic waveform postulation methodology in combination with an active harmonic load-pull measurement system. The methodology is based on a rapid and systematic procedure that initially requires only a few DC measurement parameters to approximate the device's transfer characteristic and boundary conditions. Using these parameters, it is then possible to accurately estimate or 'postulate' the idealized output current and voltage waveforms, in this case for a three harmonic Class-F mode. These waveforms are rich in information and provide harmonic load impedances as well as other key postulated parameters that can then be used to 'guide' the harmonic active load-pull measurement system resulting in a very time-efficient characterization process.**

***Index Terms* — Microwave devices, microwave measurements, parameter estimation, power amplifiers, predictive models.**

## I. INTRODUCTION

The importance of minimizing the time required for the characterization of modern microwave devices, such as those used in the RF Power Amplifier (RFPA) has become critical as it allows manufacturers to gain competitive advantage.

An established and preferred approach in designing RFPAs is based on non-linear device modeling, where CAD and a well defined device model is used to reduce and ideally eliminate measurement complexity, reducing to a minimum the number of measurements needed to achieve a required or 'target' performance. In reality however, sufficiently accurate device models tend not to be available for the emerging and highly promising device technologies that may be of interest to future PA designers. The alternative design approach is based on direct device measurement and specifically conducting exhaustive fundamental and harmonic load-pull measurements, possibly at different drive and bias levels and with the design targets usually being drain efficiency and output power. As can be imagined, this approach demands significant microwave measurement hardware and involves a high degree of human interaction over a significant time frame. This paper describes an intermediate design and optimization process that lies somewhere between simple modeling and measurements world, where by combining the two approaches, it is possible to benefit from the advantages of both. Obviously, the device cannot be perfectly described using such a simple model, but using simple information of the device itself it is shown how measurement and characterization time can be substantially reduced. The advantage of using an analytical procedure, in this case IGOR software from WaveMetrics, is to achieve quick results (without any further simulation) which can directly guide and control the load-pull system, indicating the first guess toward the measured optimum output performance. The approach described in this paper is divided into two stages. The first stage involves the extrapolation of simple DC parameters from DCIV measurement data, from which a linear or 'modified' hyperbolic tangent approximation of the device's transfer characteristic is derived. From here the voltage and current PA waveform postulator, firstly presented by Cripps [3], has been developed and used to apply waveform engineering concepts in order to identify high power and high efficiency modes of operation. The resulting, postulated, achievable current waveforms are initially used to identify optimum bias conditions and then the required harmonic impedances. In the second stage, waveform device characterization is 'guided' using the postulated target waveforms that have been identified, and these are then used as the basis for the load-pull measurement activity. It will be shown that for well behaved devices, and using postulated data generated from first step, satisfactory measurement results can be achieved very quickly. In fact, for both well-behaved and unpredictable devices, this procedure can give a quick 'first-guess' information for bias voltages and impedances, allowing focused load-pull activity to be quickly conducted. A comparison of output performance achieved using a typical manual measurement procedure, where the optimum target performance has been achieved using accurate but long load-pull measurements, and this high-speed approach using linear and modified tanh approximations of the device's transfer characteristic have been conducted in order to demonstrate the validity of the approach. For this investigation, QinetiQ GaN transistors operating at 0.9GHz of frequency, 15V of drain voltage and delivering 23dBm of output power are used. Measurements have been carried out using the active envelope load-pull (ELP) measurement system [4] developed at Cardiff University.

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## II. Automated Approach

The first stage of the developed automated approach is based on DCIV measurement data, from which the two approximations of the device's transfer characteristic are derived. Firstly, for the linear approximation, five parameters are extracted to adequately describe the DC boundaries and the device transfer characteristic. Specifically, these are drain voltage ($V_{DC}$), pinch-off voltage ($V_t$), saturation drain current ($I_{DSS}$), knee voltage ($V_{knee}$) and the transconductance ($g_m$). For the modified tanh approximation, the addition of empirical parameters termed A, B and C are used, as shown in (3). Once achieved the quick DCIV measured data, these are then utilized by the postulator to predict the required drive, bias voltage and harmonic impedances, as well as the expected time-domain voltage and current waveforms, output power and efficiency for a specific mode of operation.

Drive level and input bias along with the device's boundary conditions play a significant role in shaping the current waveform. In this analysis, input bias is typically swept over a range around the theoretical class-F bias setting, which will be in the region of the device's pinch-off voltage. The relationship between the postulated output current and voltage waveforms dictate the achievable output power and drain efficiency. The link between the input bias and output current waveform is provided by an appropriate choice of the transfer characteristic as shown later in (2) and (3).

For a successful optimization, it is important to accurately specify and weight the targeted output power level. As an example, for a given bias range the predictor may converge towards a class C bias point thus optimizing for very high efficiency at the expense of output power. Once the optimum waveforms are identified by the postulator, the resulting device conditions are uploaded into the time-domain measurement system software, which then replicates in reality the bias, drive, and harmonic loading conditions identified by the postulator. To facilitate accurate comparison with the waveforms measured at the output reference plane established by the measurement system, the predicted waveforms (which are postulated in the absence of extrinsic and intrinsic parasitic effects) are embedded with the effects of the device output parasitic capacitance. For these measurements, a value of $C_{DS}$=0.04pF was used. It should be noted that the embedding of the parasitic output capacitance is necessary to verify the device performance in terms of output waveforms, as well as to identify the harmonic loads that need to be presented at the device measurement plane.

## III. Implementation Of Automated Approach

### A. Extraction of DCIV Parameters

For these measurements, the DC drain voltage was fixed at $V_{DS}$=15V. The knee voltage ($V_{knee}$) is the point that divides the saturation and the linear region of the device and in terms of time domain waveforms, can be defined as the minimum value of the achievable RF drain voltage. As it can be seen from Fig. 1, $V_{knee}$ can assume any value between 0 and 4V. A correct value can be established by knowing the output RF power ($P_{OUT}$) which is delivered by the device according to the following equation:

$$P_{OUT} = \frac{1}{2}\frac{(V_{DC} - V_{knee})\cdot I_D}{2} \quad (1)$$

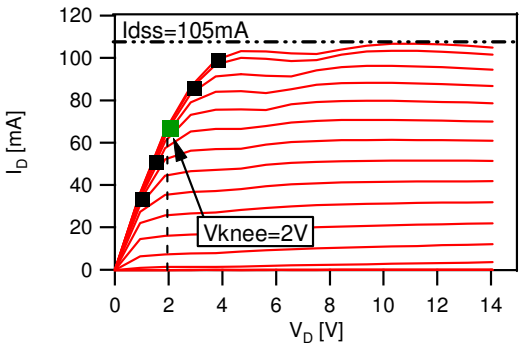


Fig. 1. Measured DCIV.

With reference to equation (1) and Fig. 1, if operating with a knee voltage of 2V, the corresponding maximum drain current is approximately 65mA and achievable output power is approximately 23.2dBm, which in this case is the closest to the datasheet value of 23dBm. The saturation current ($I_{DSS}$) is the maximum current which the device can deliver, and this parameter can again be easily found from DCIV characteristic shown in Fig. 1. The pinch-off voltage ($V_t$) is the gate bias voltage where the device starts to conduct current. This value can be obtained from the extracted transfer characteristic. $G_m$ is the transconductance of the device which is identified by the slope of the transfer characteristic. A, B and C are empirical values used to fit as close as possible the modify tanh approximation of the transfer characteristic to the measured one. Table 1 summarizes the DC extracted parameters which are common to both transfer characteristics.

TABLE I
EXTRACTED DC PARAMETERS

| $V_{DC}$ [V] | $V_t$ [V] | $I_{DSS}$ [mA] | $V_{knee}$ [V] |
|---|---|---|---|
| 15 | -5.5 | 105 | 2 |

### B. Waveform Engineering Prediction

When using both the linear and hyperbolic tangent approximations of the transfer characteristic, additional DC parameters need to be extracted; example is shown in Table II.

TABLE II
EXTRACTED PARAMETERS FOR DIFFERENT TRANSFER CHARACTERISTIC

| Linear | Tanh | | |
|---|---|---|---|
| $g_m$ [A/V] | A | B | C |
| 0.43 | 2.25 | 0.4 | 0.316 |

Using these two simple functions to model the transfer characteristics as shown in (2) and (3), it is possible to generate an idealized three-harmonic class-F voltage waveform (3rd harmonic square waveform) that achieves good postulated results in terms of bias voltage ($V_G$) and harmonic impedances.

$$I_{D\_linear} = v_g \cdot g_m \cdot I_{DSS}\left[1 - e^{\frac{V_{DS}}{V_{knee}}}\right], \quad (2)$$

$$I_{D\_\tanh} = [(1 + A \cdot \tanh(v_g \cdot B - V_t \cdot C))/2] \cdot 2I_{DSS}\left[1 - e^{\frac{V_{DS}}{V_{knee}}}\right], \quad (3)$$

where $v_g$ is the input voltage.

Fig. 2 shows that the linear function and especially the tanh function in this case offer good approximations to the measured transfer characteristic.

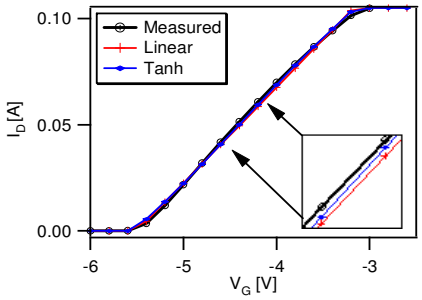


Fig. 2. Measured linear and hyperbolic tangent characteristics.

Using the DC parameters established for the tanh characteristic, the postulator identifies the optimum bias point and harmonic impedances for, in this case a class-F mode of operation. As this mode relies on a half rectified sinusoidal current waveform, the third harmonic current component is significantly suppressed.

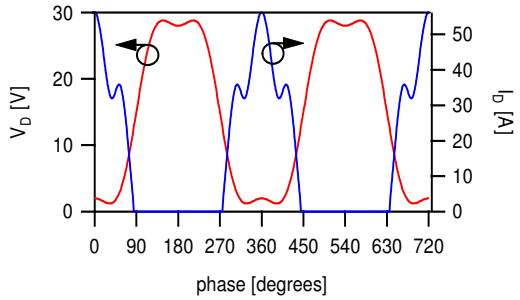


Fig. 3. Predicted class-F voltage and current waveforms at the current-generator plane using the modified tanh characteristic.

The predictor will also develop waveforms such as those in Fig. 3, as well as the expected output power and drain efficiency, shown later in Table VI. Fig. 4 shows the behavior of the third harmonic current as a function of gate bias voltage ($V_G$) for the two modeled transfer characteristics as well as from direct measurements. It can be seen here that to minimize the third harmonic current (to achieve the half rectified sinusoidal current waveform), the hyperbolic tangent function offers a closer fit to the measured device behavior.

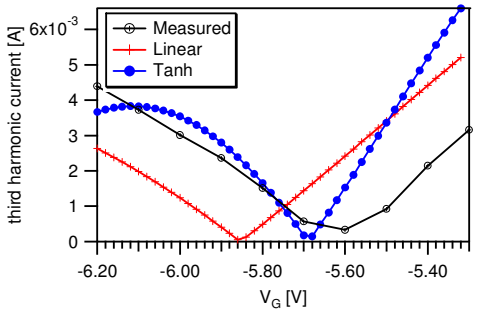


Fig. 4. Third harmonic current amplitude for measured, linear and hyperbolic tangent functions.

In the manually measured case in Fig. 4, the class-F bias point ($V_G$=-5.6V) is slightly lower than pinch-off (Vt=-5.5V) resulting in a higher value of efficiency still maintaining the expected output power. For both linear and tanh functions, the optimum choice of bias voltage is not the one that exactly minimize the third harmonic current. This is because the aim is to achieve the best trade-off between efficiency and output power. Considering for example the tanh approximation, a bias point of $V_G$=-5.68 V offers the best postulated efficiency ($\eta$=83%), but this is at the expense of lower output power $P_{OUT}$=22.7dBm. Changing the bias voltage to $V_G$=-5.64V (shown in Table III) results in a better compromise between efficiency $\eta$=82% and higher output power $P_{OUT}$=23dBm.

TABLE III
IDENTIFIED BIAS VOLTAGE FOR MINIMUM 3RD HARMONIC CURRENT FOR DIFFERENT TRANSFER CHARACTERISTICS

| | ***Measured*** | ***Linear*** | ***Tanh*** |
|---|---|---|---|
| ***Bias Points*** | *-5.6 V* | *-5.78 V* | *-5.64 V* |

*B. Measurements using predicted parameters*

Once the required bias voltage and harmonic impedances have been identified as shown in Tables III and IV, the next stage was to use these emulated values directly in the measurement system in order to identify the resulting measured waveforms, output power and efficiency on real devices. Fig. 5 shows the measured and predicted (inset) load-line for both device plane (green line) and output measurement plane (red line). The predicted load-line has been identified using the hyperbolic tangent characteristic approximation. It can be seen that the measured results agree quite well with those predicted. Besides it can be seen that the knee voltage is approximately 2V, as expected.

TABLE IV
FUNDAMENTAL AND HARMONIC IMPEDANCES AT OUTPUT MEASUREMENT PLANE

| | ***Z(f0) [Ω ]*** | ***Z(2f0) [Ω ]*** | ***Z(3f0) [Ω ]*** |
|---|---|---|---|
| ***Manual*** | 616+j2.96 | 0+j0.43 | 0+j954 |
| ***Linear*** | 630+j91 | 0+j0 | 2209+j2131 |
| ***Tanh*** | 626+j90 | 0+j0 | 2152+j1708 |

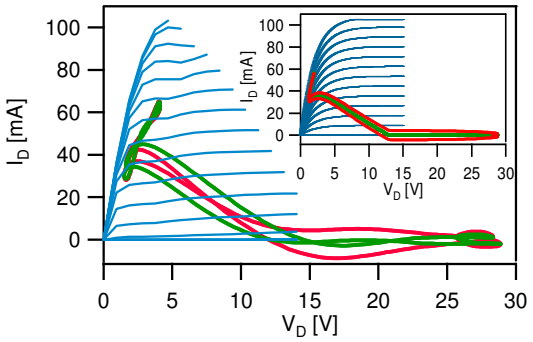


Fig. 5. Measured RF load-line at device current-generator plane (green line) and output measurement plane (red line) with the predicted RF load-line inset.

Similarly, as it can be seen from the measured time domain voltage and current waveform in Fig. 6, there is a good agreement with predicted waveforms of Fig. 3.

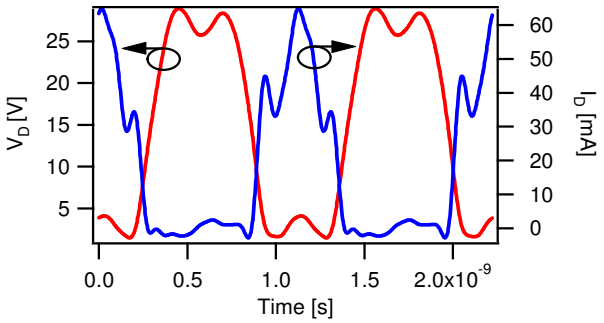


Fig. 6. Measured voltage and current waveforms at the device current-generator plane.

## IV. Results And Comparison

Table V shows measurement results achieved using the manual procedure [2], where all target parameters have been obtained using long sweeps directly from the measurement activity without any prediction. Table VI shows predicted results, and measurement results when using the predicted linear and modified tanh approximations. As it can be seen, the new procedure yields device performances that are close to that achieved when using the manually driven approach. Obviously the predicted values will be closer to the measured equivalents for well behaved devices. In any case, an important first guess can be achieved, greatly reducing the time taken to locate these optimums values.

Interestingly, both linear and hyperbolic tangent functions are able to predict bias point and harmonic impedances that show a very good agreement with those identified using the manual approach, thus demonstrating the validity of the approach. For unpredictable devices or higher frequencies, starting from this first guess which gives a zoomed window, load-pull can be conducted for the achievement of the optimum condition.

TABLE V
MANUAL MEASUREMENT RESULTS

| | ***Measurements*** |
|---|---|
| ***Manual*** | Pout=23.57dBm<br>$\eta$ = 81.024 |

TABLE VI
PREDICTED AND MEASURED RESULTS USING PREDICTION

| | ***Prediction*** | ***Measurements*** |
|---|---|---|
| ***Linear*** | Pout=22.93dBm<br>$\eta$= 82.71% | Pout= 23.3dBm<br>$\eta$ = 79.6% |
| ***Tanh*** | Pout=22.96dB<br>$\eta$ = 82 % | Pout= 23.34dBm<br>$\eta$ = 80.35 % |

## V. Conclusion

This paper has demonstrated that armed only with simple DC information describing a real device, it is possible to significantly speed up load-pull measurement activity. The paper emphasizes how the incorporation of simple waveform data, derived from basic set of DC measurements, can have a significant impact in supplying important first-guess measurement data including drive, bias and load condition, improving dramatically the time utilization of the load-pull measurement systems. This work is therefore of high significance to the load-pull measurement community where combining the measurement activity with modeling (albeit simple modeling) knowledge, it is possible to avoid very time consuming, exhaustive measurement activities. Results based upon postulated waveforms show a good agreement with those obtained using a conventional manual search procedure for well behaved devices. Predictions and measurements have been conducted using different geometries of QinetiQ GaN transistors, and TriQuint and RFMD GaAS transistors all giving satisfactory results.

## Acknowledgement

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# Publications

**4-**
**"Utilization of RF I-V Waveform Load-Pull Information to Identify the Role FET Knee Profile has on Locating the Efficiency Maxima.**
**Canning, T.; Almuhaisen, A.; Lees, J.; Benedikt, J.; Cripps, S. & Tasker, P.**
**Microwave Measurement Conference (ARFTG), 2011 78th ARFTG, 2011. "**

# Utilization of RF I-V waveform load-pull information to identify the role FET Knee Profile has on locating the efficiency maxima

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**Abstract — Typically performance maxima in terms of output power, efficiency, etc. are determined from analyzing, effectively "data mining", load-pull measurements. This approach while identifying relevant design information provides no insight into the origin or location of the relevant maxima. However, if during load-pull measurements the RF I-V waveforms are also measured this insight is available. Measured RF I-V waveform load-pull information from a 10x75um Gallium Arsenide transistor operating in class-B at 8GHz is used to correctly identify the effect of the knee region of the transistor I-V characteristic on power and efficiency. As a consequence the location of the drain efficiency contours on the Smith Chart are explained in terms of $V_{min}$ and current waveform compression.**

***Index Terms* – Amplifier Knee, class-B, high efficiency, waveform engineering, power amplifier**

## I. Introduction

RF Power Amplifiers (RFPAs) are a key component in modern communications systems. A large proportion of system power is usually devoted to amplification of the RF signal to overcome losses in the transmission medium. These large powers mean that the efficiency of the RFPA can have a large effect on overall system efficiencies. Much work has gone into improving the efficiencies of RFPAs in recent years [1]-[5].

Cardiff University has been at the forefront of investigations into RF I-V waveform engineering or shaping for efficiency improvement of High Power Amplifiers (HPA's). The ability to view measured waveforms of the device in operation and compare these to the theoretical waveforms have yielded extremely high efficiency amplifiers and new modes of operation [3]. It has also been observed that not all devices perform optimally in each mode of operation [6].

This work attempts to utilize the ability to view waveforms to explain the impact of the knee effect on drain efficiency.

## II. Waveform Engineering

RF I-V Waveform measurements when combined with active load pull systems, the waveform engineering element, are generating a wealth of information that has the ability to give great insight into the operation of high frequency transistors. In the past, amplifier design methodologies utilizing load pull measurements concentrated on plotting figures of merit, power, efficiency, etc., versus impedance on a smith chart. By definition these figures of merit were a form of data mining from the waveforms present at the device terminals showing some relevant key performance indicators. Using legacy instrumentation this focus on key performance indicators was unavoidable due to measurement constraints. The ability to analyze voltage and current waveforms directly however, poses the question as to whether these figures of merit are necessarily now the best information to use for data mining when targeting design objectives.

## III. Simple Knee Effect in Theory

Simple high efficiency amplifier theory does not consider the knee effect in calculating efficiency and output power. A perfect device model with no knee assumes the device is able to operate, at a point in the cycle with absolutely no drain source voltage and saturated current. This oversimplified condition does not apply to real devices, especially in power devices which, even at moderate powers, operate at hundreds of milliamperes.

Using a hard limiting IV model offers a way to, at a very basic level, quantify the effect of the knee on amplifier performance.

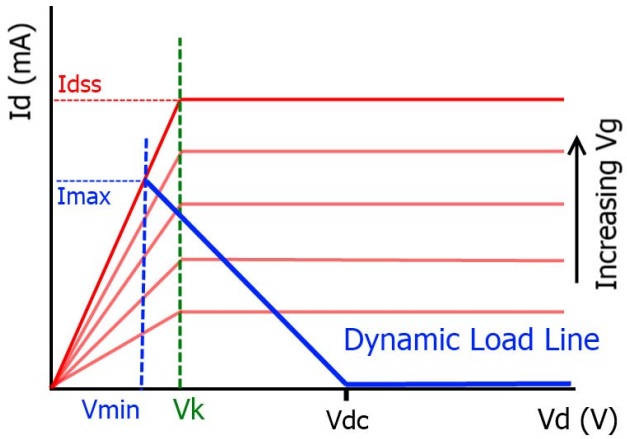


Fig 1. Definition of Idss, Imax, Vk, Vmin and Vdc.

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TABLE I

EFFECT OF KNEE VOLTAGE ON AN IDEAL DEVICE IN CLASS B

| $V_{min}/V_{dc}$ (V) | $\frac{P_{1F0}}{P_{DC}}$ (%) | Power Loss (dB) |
|---|---|---|
| 0 | 78.5 | 0 |
| 0.04 | 75.07 | -0.2 |
| 0.09 | 71.58 | -0.4 |
| 0.13 | 68.1 | -0.62 |
| 0.18 | 64.6 | -0.85 |
| 0.22 | 61.1 | -1.1 |

Table I states how this minimum voltage limit can affect drain efficiency and output power. An increase in knee voltage will also require a reduced drive level to prevent overdriving and clipping the waveform, resulting in a reduced efficiency [7].

If we define drain efficiency ( $\eta$ ) as

$$\eta = \frac{P_{1F0}}{P_{DC}} \qquad (1)$$

Then $\eta$ for the class B case with a $V_{min}$ condition imposed becomes

$$\eta = \frac{\pi}{4} \cdot \frac{(V_{DC} - V_{MIN})}{V_{DC}} \qquad (2)$$

The decrease in efficiency associated with increased $V_{min}$ comes from the $V_{DC} - V_{MIN}$ term in the equation for fundamental current. Table 1 assumes the class B current waveform is unaltered and that the voltage waveform alone is limiting the efficiency, as shown in (2).

The presence of drain efficiency optima clearly is inconsistent with this simple theory which would seem to suggest, looking at Fig 1, maximum efficiency at high loads. If we perform load pull at a constant Pin we must also consider the effect of the knee region on the current waveform.

## IV. WAVEFORM MEASUREMENTS

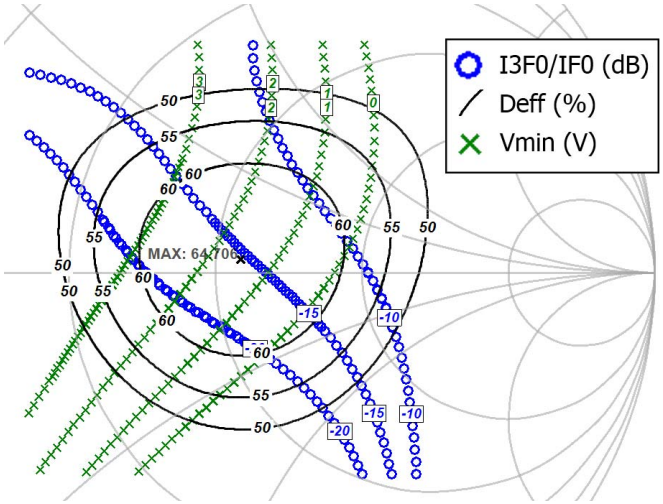


Fig 2: Measured drain efficiency contours vs. Vmin (V) and compression (ratio of third harmonic to fundamental current) contours for a deembedded device in class B. Drive level held constant.

Fig 2 shows an example of contours that could not be plotted without waveform data. They show the relationship between $\eta$, $V_{min}$ and a third figure, third harmonic current over fundamental current.

In a half rectified current waveform the third harmonic current should be zero, so any third harmonic current shows the presence of compression in the current waveform.

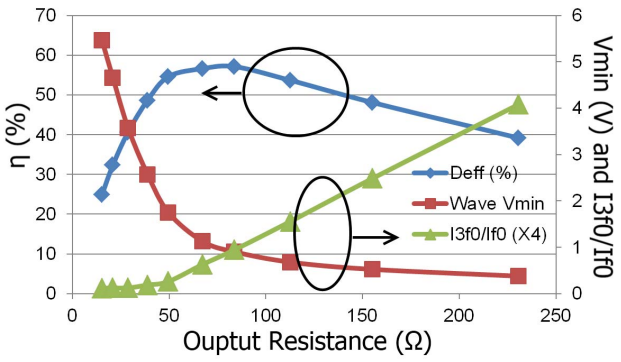


Fig 3: Measured waveforms from test device demonstrating the Vmin compression tradeoff

Fig 3 summarizes the effect shown in Fig 2 by constraining the analysis to the real impedance plane. Here it appears there is a tradeoff between $V_{min}$ and current wave compression. The surprising aspect of this figure is the amount of third harmonic current present at the optimum drain efficiency point. This suggests there exists a set of waveforms which contain significant third harmonic current while maintaining high efficiency.

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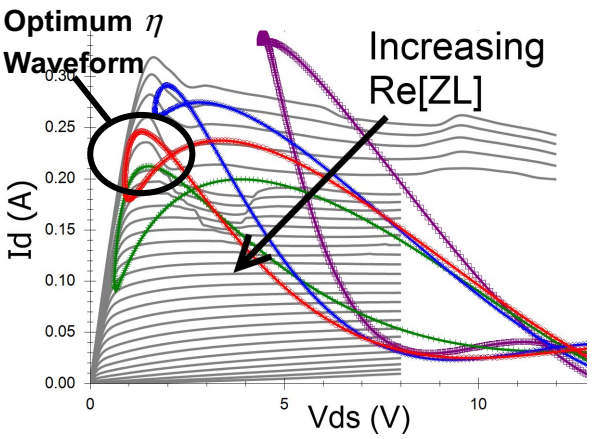


Fig 4. Load lines deembedded to the Igen plane of a device where the output resistance is being swept with constant Pin.

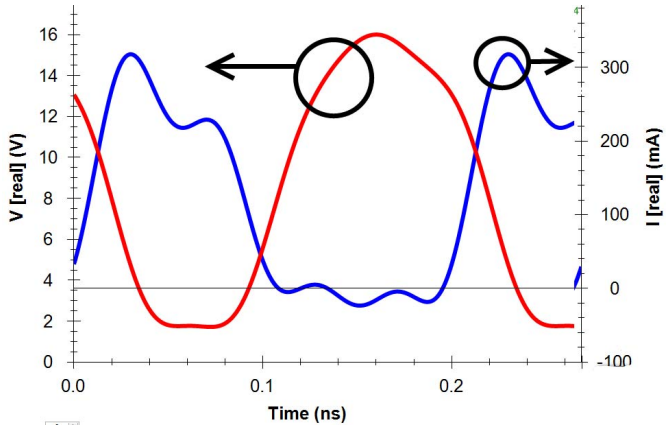


Fig 5: Waveforms of the optimum η load line shown in Fig 4.

Fig 4 shows measured load lines, where output load is swept along the real part of the smith chart with a constant input power. The shape of the load line close to the knee of the higher impedance states shows the flattening of the top of the waveform as the waveforms begins to impact the knee region. Fig 5 shows the IV waveforms of the load line with the highest η. It becomes apparent by looking at the waveform data here that the conventional half rectified current waveform does not hold the optimum solution for η in this case.

## V. Analytical Compression Analysis

Seeing that current waveform compression is occurring in measured device waveforms, we could now consider if this observation can be supported by folding a simple analytical analysis of current waveform compression into (2).

Fig 6 defines α, a measure of the conduction angle of the normalised input voltage waveform (and thus the output current waveform) in a simple hard limiting case.

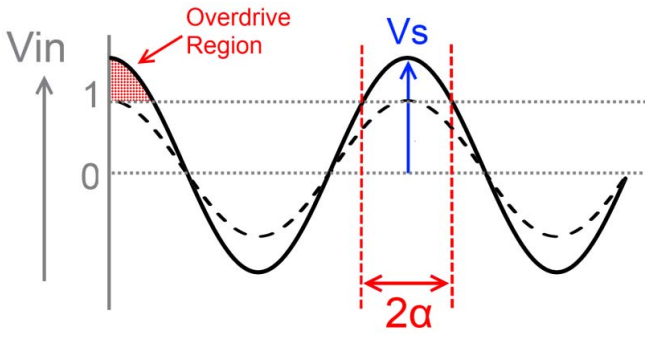


Fig 6: Defining the compression angle α in terms of input voltage. Vin is normalized so zero is pinch off and one would give Idss at the output.

Fig 6 and equations (3)-(6) are taken from [7] but have been simplified to the class-B case. $\alpha$ is defined as

$$\cos(\alpha) = \frac{1}{V_S} \tag{3}$$

$$I_{DC} = \frac{I_{MAX}}{\pi}\left[\alpha + \frac{1}{\cos\alpha}(1-\sin(\alpha)\right] \tag{4}$$

$$I_{1F0} = \frac{2I_{MAX}}{\pi}\left[\sin\alpha + \frac{1}{4\cos\alpha}(\pi - 2\alpha - \sin(2\alpha))\right] \tag{5}$$

Using (2) now but substituting in the new values for $I_{DC}$ and $I_{1F0}$ gives a new equation for efficiency which incorporates the effect of $V_{min}$ and compression.

$$\eta = \frac{(V_{DC} - V_{MIN})}{V_{DC}} \cdot \frac{I_{1F0}}{I_{DC}} \tag{6}$$

Using (6) we can now attempt to support the $V_{min}$ versus compression hypothesis for the shape of drain efficiency contours by comparing measured data from Fig 3 and predicted efficiency.

While analytically possible to incorporate compression into drain efficiency predictions, an alternative approach would be to perform load pull, not under constant drive, but under constant current waveform compression. This would eliminate α and demonstrate for a particular compression level the optimum load impedance. The compression level could initially be determined by amplifier gain or power requirements.

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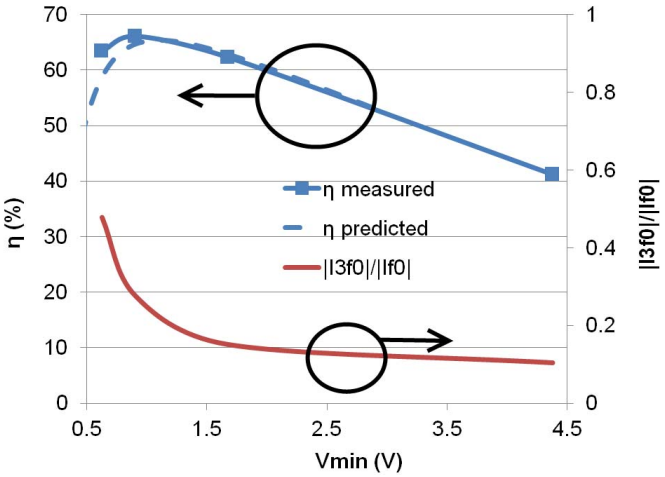


Fig 7: Predicted vs. Measured drain efficiency for device A with decreasing output resistance at a constant input drive. Here $\alpha = \frac{1}{V_{MIN}}$

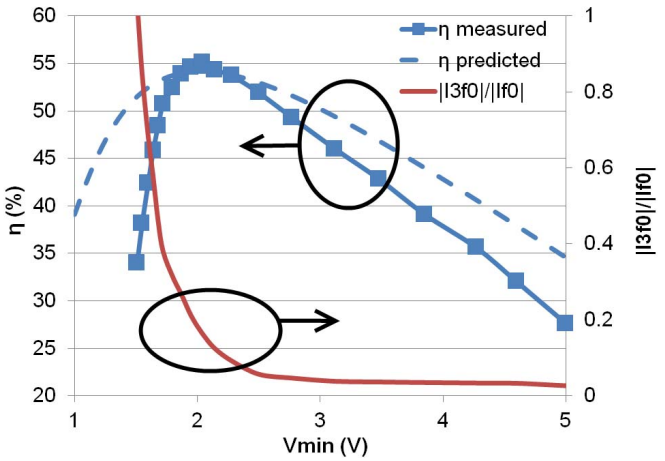


Fig 8. Predicted vs. Measured drain efficiency for device B with decreasing output resistance at a constant input drive. Here $\alpha = \frac{2.5}{V_{MIN}}$.

Fig 7 and Fig 8 show measured and predicted values of $\eta$ for two GaAs HEMT 10x75um devices. It can be observed that the measured and simulated values for $\eta$ are highly correlated. $\alpha$ has been chosen here as inversely proportional to $V_{min}$ to simulate the measured data shown in Fig 3. The compression characteristics of devices will vary depending on their knee profiles and their small signal gain characteristics. This simple $\eta$ analysis demonstrates how Waveform measurements and theory can come together to provide a greater understanding of device operation.

## VI. Conclusion

Waveform measurements have been used to demonstrate how both $V_{min}$ and compression against the knee region contribute to $\eta$ variation in a constant drive load sweep. A simple equation linking $\eta$, $V_{min}$ and device compression has been presented and used to demonstrate consistency between waveform based theory and measured data.

Waveform investigations on two sets of measured data from 10x75µm Gallium Arsenide FETs showing good correlation between predicted and measured drain efficiency variations.

Optimal drain efficiency was shown to occur under quite considerable compression.


## Acknowledgement

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