Low temperature impact ionization in indium antimonide high performance quantum well field effect transistors

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The observation of a kink effect in the output characteristic of an InSb/AlInSb quantum well field effect transistor structure at low temperature (1.6 K) is reported. The effect is strongly temperature dependent, and while just discernible at room temperature, it is greatly enhanced below ~120 K. At 1.6 K strong hysteresis is observed in the (output) forward characteristic of the device when sweeping the drain bias up and down. Corresponding instability is also observed in the gate leakage current as a function of gate voltage. We explain the effect by comparing with Monte Carlo simulations, observing strong hole accumulation under the gate region of the device as a result of significant impact ionization in the drain region. This accumulation is enhanced compared to the more common InAs/AlSb type II system, due to the fact that InSb/AlInSb has a type I band alignment. This inhibits the loss of holes to the gate contact, a significant leakage mechanism in type II systems. We show that the extent of the hysteresis is a good measure of the charge accumulation under the gate region and estimate accumulation by examination of the hysteresis compared with the results of the Monte Carlo simulation. © *2006 American Institute of Physics.*
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I. INTRODUCTION

Narrow band gap high electron mobility transistors (HEMTs) are currently of great interest due to their desirable material qualities, which lend themselves to low-power high-speed applications. Among such materials InSb shows considerable promise because of its extremely high electron mobility and saturation velocity.[1–3] The low effective mass and narrow band gap of these materials, however, also introduce a susceptibility to impact ionization-related effects that manifest themselves as an increased output conductance, often referred to as the "kink effect," due to the increase in drain current observable in the output characteristic[4–6] giving rise to a conductance kink. Such an effect has been observed in a number of heterostructure systems, with a level of severity that can limit the usefulness of the device.[4,5] Further work on AlSb/InAs systems has sought, with some success, to minimize this effect so that it is almost negligible at 293 K.[7,8] A related issue for the InAs/AlSb material system is an enhanced gate leakage due to increased charge, created by impact ionization in the drain, drifting back to the gate contact. This is strongly enhanced as a result of the type II band alignment in such systems, whereby the holes in the valence band are not confined and so are not inhibited from drifting back to the gate contact. This results in a strong "bell" shaped characteristic in the gate current, even at room temperature.[9,10]

We report that a kink effect has been observed in InSb/AlInSb quantum well field effect transistors (QW FETs) at low temperatures, with accompanying gate leakage enhancement. A strong temperature dependence is identified such that the kink effect is negligible at temperatures approaching 293 K. The enhancement in drain current develops with increasing gate bias until hysteresis is observed. We propose that the accumulation of impact ionization generated holes precipitates a positive feedback mechanism that can drive the drain current of a pinched-off device into the on-state. However, this mechanism is self-limiting and the device is not necessarily driven into breakdown. We use a combination of a two-dimensional (2D) self-consistent Schrödinger-Poisson band modeling and a 2D Monte Carlo simulation to demonstrate this effect theoretically, and compare with experimentally observed behavior.

II. MATERIAL GROWTH AND DEVICE FABRICATION

The InSb/AlInSb quantum well material was grown by solid-source molecular beam epitaxy (MBE) on a semi-insulating GaAs substrate. In growth order, the structure consists of an accommodation layer, a 3 μm $Al_xIn_{1-x}Sb$ buffer ($x=0.15$), a 20 nm InSb quantum well channel layer, fol-

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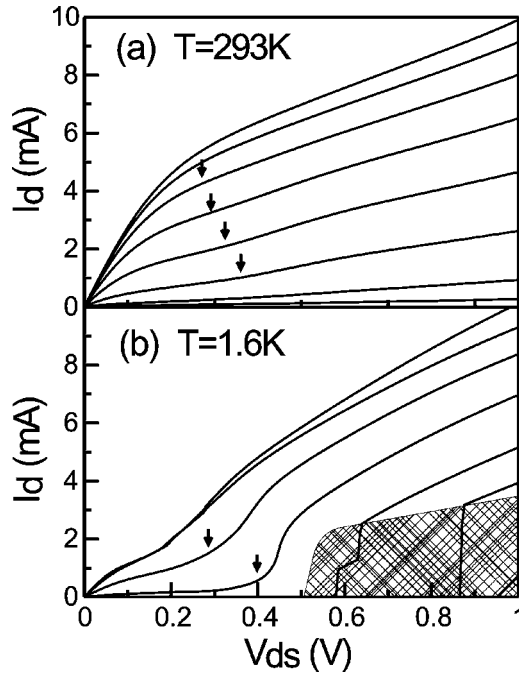[a]Electronic mail: p.buckle@qinetiq.com

FIG. 1. The output characteristics for a nominal 100 nm gate length device taken at temperatures of (a) 293 K and (b) 1.6 K for a range of gate voltages [(a) V_g=0–0.8 V, (b) V_g=0–0.8 V]. The hatched area indicates the extent of the region of instability in the device drain current.

FIG. 2. Output characteristics for gate biases of −500 and −600 mV, showing the strong hysteresis observed in the drain current (I_d). The inset shows the dependence of the width of this hysteresis (ΔV_{ds}) vs gate bias (V_g).

lowed by a 50 nm $Al_xIn_{1-x}Sb$ (x=0.15) cap with Te δ doping ($\sim 1 \times 10^{12}$ cm^{-2}) located 5 nm above the quantum well. This forms a type I heterostructure alignment, providing confinement for both electrons and holes in the channel. Hall measurements have determined the mobility to be 2.4 $\times 10^4$ cm^{-2} V^{-1} s^{-1} (RT)/4.5 $\times 10^4$ cm^2 V^{-1} s^{-1} (77 K) with a carrier concentration of 6.2×10^{11} cm^{-2} (RT)/4.1 $\times 10^{11}$ cm^{-2} (77 K).

QW FET devices were fabricated using optical lithography to define the source and drain with Ti/Au layers deposited by e-beam evaporation and lift-off providing Ohmic contacts. E-beam lithography was used to define Ti/Au Schottky gate structures with nominal lengths of 100, 200, or 400 nm onto mesas of width 20 or 40 μm. These devices were then isolated by wet chemical etching. The gates are air bridged between the mesa edge and the gate feed metal to minimize gate leakage. Full details of similar devices with room temperature ac and dc performances can be found in Ref. 2.

III. EXPERIMENTAL RESULTS

The InSb/AlInSb QW FETs were characterized over a number of temperatures between 1.6 and 293 K using a liquid helium bath cryostat. With a typical 100 nm gate length device, output characteristics were taken in the depletion mode by sweeping the drain bias with respect to the source contact (V_{ds}) between 0 and +1 V and measuring the drain current (I_d), with the gate voltage (V_g) varying between 0 and −0.8 V. Commonly observed transconductance compression for low V_g (Ref. 11) is observed in Fig. 1, where the onset of channel modulation is at finite V_g (in this case
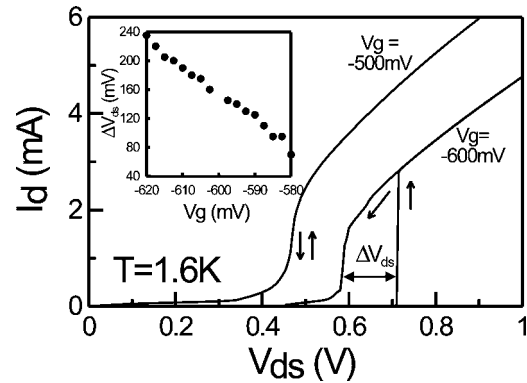
around −250 mV). This is usually ascribed to the screening effect of trapped surface charge under the gate region.[5,11]

At 293 K the presence of an inflection in the drain current can be seen to develop in some structures at source-drain voltages above ∼200 mV [indicated by an arrow in Fig. 1(a)]. It is clear even at these temperatures that this effect emerges as a function of applied gate bias. This "kink" progresses to higher V_{ds} as V_g becomes more negative and the device is pinched off. Similar features have been observed elsewhere in InAs/AlSb (Refs. 7, 10, and 11) and InAs/InGaAs (Refs. 4 and 5) devices at room temperature. For the InSb/AlInSb devices reported here this effect is minimal at room temperature; indeed in some devices the conductance kink is extremely difficult to discern. Decreasing the sample temperature has a strong impact on this kink when below ∼150 K, resulting in dramatic jumps in output conductance at high negative gate biases at sample temperatures approaching 1.6 K. This is demonstrated clearly in the output characteristic shown in Fig. 1(b). At this temperature the effect has increased to the extent that I_d becomes larger by many orders of magnitude over a very small increase in V_{ds}. Beyond this, I_d appears to vary in a more stable way. It is apparent from these curves that the jump between low and high output conductivities is the result of some process that effectively opens or enlarges the channel by some means. As V_g is increased in magnitude (in this case, beyond −500 mV) the kink becomes more dramatic, leading to a region of instability illustrated in Fig. 1(b) by the hatched area. The onset of this instability coincides exactly with the gate voltage required to fully pinch off the device. The output characteristics shown in Fig. 2 were obtained by sequentially sweeping V_{ds} from 0 to +1 V and returning to 0 V for two specific values of V_g in the unstable region (−500 and −600 mV). The direction of the voltage sweep is indicated on the figure by directional arrows. These data reveal that in its extremity (within the unstable region) the conductance kinks seen in Fig. 1(b) represent one direction of a hysteresis cycle. As V_g becomes more negative the magnitude of this hysteresis becomes greater. Taking the V_g=−600 mV sweep in Fig. 2 as an example, the initial increase in V_{ds} from 0 to 700 mV indicates that the channel is entirely pinched off, then over a further increase in V_{ds} of only a few mV the channel is rapidly opened and a high current is received by the drain. This
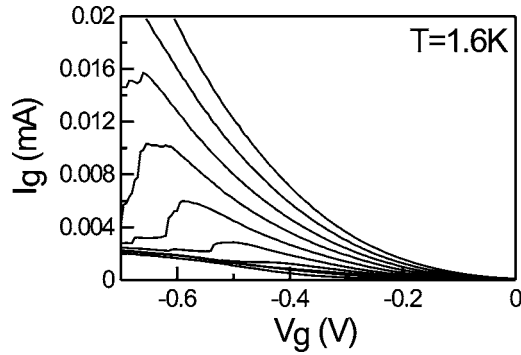
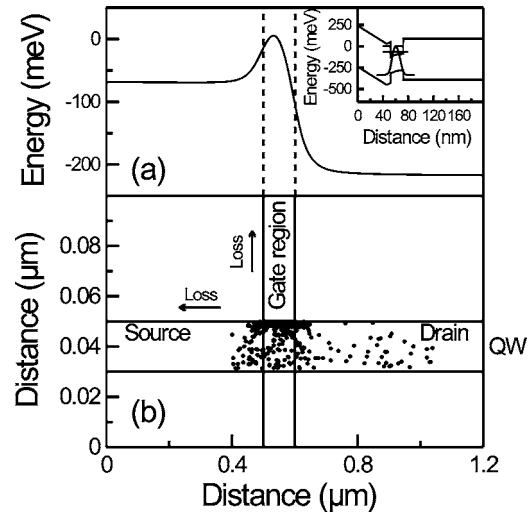FIG. 3. Gate leakage (I_g) at 1.6 K for a 100 nm gate device. Drain voltages range from 0 through to 1 V.

FIG. 4. (a) The conduction band profile along the conducting channel of the device, calculated from a 2D Schrödinger-Poisson model, for a device just pinched off. (b) The filled circles represent position data for 2D Monte Carlo hole superparticles at $V_{ds}=0.5$ V and $V_g=-0.6$ V (at time $t=3$ ns), where the simulation is seen to stabilize. Each of these hole superparticles represents a finite amount of charge (one superparticle represents a hole density of 2.3 $\times 10^{16}$ cm^{-3}).

process sees that the current switches to some steady high conductance state after which I_d varies stably with V_{ds}. On the negative going return V_{ds} sweep (from +1 to 0 V) the device remains in this high conductance state until a much lower V_{ds} is reached. This immediate switching is equipment limited and is suggestive of a strong positive feedback mechanism rapidly turning the device on to some saturation conductance. The enforced high conductance state of the return sweep is indicative that the device is not able to switch between states as before and is being "held" at high conductance. The extent of the hysteresis can be characterized by the quantity ΔV_{ds}, indicated in Fig. 2. This value describes the difference in V_{ds} between points where pinch off is achieved in the two conductance states. The inset of Fig. 2 shows ΔV_{ds} as a function of V_g. The mechanism controlling the extent of the hysteresis is clearly linearly proportional to the applied gate voltage.

Figure 3 shows the gate leakage current I_g as a function of V_g and V_{ds}, where V_g was swept from 0 to −0.8 V for values of V_{ds} between 0 and +1 V. At low V_{ds} the gate current is consistent with leakage across a Schottky barrier gate; however, beyond $V_{ds}\sim 400$ mV the gate current becomes enhanced over a finite range of V_g. For higher V_{ds} bell curves begin to develop from this excess current, increasing in magnitude as a function of V_{ds} and peaking at higher V_g. There is an abrupt change in this excess current, however, at $\sim V_g=-0.5$ V, where it rapidly reverts back to the background leakage trend.

IV. DISCUSSION AND DEVICE MODELING

We consider the role of impact ionization in the drain region of the device and the subsequent effect of the transport of holes. In particular, we consider the consequence of hole charge accumulation within the gate region, which is often cited as the cause for the kink effect at room temperature in transistors made from other material. To gain insight into the nature of this effect we have used a combination of a self-consistent 2D Schrödinger-Poisson model and a 2D Monte Carlo simulation. Figure 4(a) shows a conduction band profile along the conducting channel of the device. This profile is for the quantized state within the QW region shown in the band diagram of the layer structure of the device [Fig. 4(a) inset]. It is worth noting at this point that the InSb/AlInSb material system has a type I band alignment[12]

rather than the type II of more widely reported InAs/AlSb HEMTs.[7–11] Holes within the channel are more strongly confined [Fig. 4(a) inset] than in a type II system, especially at low temperatures where thermal excitation out of the QW is greatly reduced. It can therefore be expected that charge accumulation will be more significant than in type II structures and a good candidate mechanism for the observed instability, whereby the two stable states have different charge configurations for the same potentials applied to the gate and drain contacts (giving rise to differing potential profiles across the active region of the device). These charge states are accessed by appropriate initial conditions (i.e., positive and negative sweeps of the source-drain potential) leading to different conductance states.

Monte Carlo transport simulations have been performed with the 2D ensemble simulator SLURPS (Ref. 13) in which Poisson's equation is solved self-consistently alongside the particle dynamics. Impact ionization, using a Keldysh form for the ionization scattering rate, was included.[13,14] Additional scattering mechanisms considered were those due to acoustic phonons, optic phonons (both polar and nonpolar), ionized impurities, and alloy scattering (for AlInSb). The calculations included Γ and L electron valleys and heavy hole (HH) and light hole (LH) valence bands. Figure 4(b) shows the typical results for the Monte Carlo simulation at $V_{ds}=0.5$ V with $V_g=-0.6$ V, at some finite time where the simulation has been observed to stabilize. There is a strong accumulation of hole charge under the gate region by this time. The effect of this accumulation on the gate is significant in that it lowers the effective gate potential. This will have the effect of opening up the channel under the gate, injecting more high energy electrons into the drain region. This subsequently creates more holes from impact ionization, and so a positive feedback mechanism is established rapidly opening up the device channel. This behavior is exactly what is
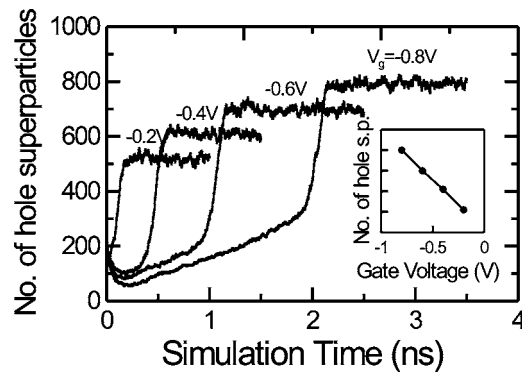
FIG. 5. The number of hole superparticles within the 2D Monte Carlo device simulation, as a function of simulation time, is shown for four different values of gate bias at $V_{ds}=0.5$ V. The inset shows the number of hole superparticles predicted after stabilization of the simulation at finite time.
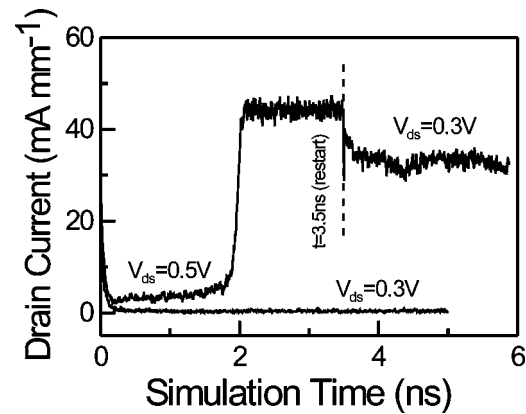

FIG. 6. Time evolution of two 2D Monte Carlo simulations of drain current vs simulation time, for $V_g=-0.8$ V. The drain bias for the two simulations differs at initiation (0.5 and 0.3 V labeled). However, at $t=3.5$ ns simulation time, after the drain current has stabilized, the higher drain voltage (0.5 V) is dropped to 0.3 V. Between $t=4$ and $t=5$ ns the simulations are running with identical parameters, the resultant difference originating from the initial conditions at the $t=3.5$ ns restart point.

observed in the output characteristic of the device [Fig. 1(b)] with strong positive feedback forcing the device on, at sufficiently large drain bias to allow impact ionization. It has been proposed elsewhere that this mechanism will cause catastrophic device failure, as the positive feedback drives the device into breakdown.[3] However, there are two limiting factors for this mechanism. Firstly, the reduction in the gate potential means that there is a corresponding increase in hole current that drifts back to the source region. It is assumed in the Monte Carlo simulation that holes, when reaching the electron rich source contact, are lost to the system (either in radiative or nonradiative recombination). Indeed the Monte Carlo simulation only stabilizes if this loss mechanism is included, since otherwise holes will simply increase towards infinity within the source region since in this model they are not extracted by the contact. Secondly, the effect of perturbing the gate potential due to the accumulated holes is that the barrier for hole transport out to the gate contact is reduced, therefore enhancing the hole gate current. Evidence for the increase in hole leakage to the gate is seen in Fig. 3, where there is a clear enhancement to the gate leakage over a certain V_{ds} threshold. These two loss mechanisms are indicated in Fig. 4(b) by arrows. As holes accumulate under the gate, these loss mechanisms will increase and will ultimately act as a limiting process to the feedback mechanism that opens up the channel. The hole density reaches equilibrium with a balance of the injection of holes from the drain (from impact ionization), and the loss of holes to the gate and source contacts. This is observed in the Monte Carlo simulation provided it is allowed to stabilize at sufficiently long time scales. The number of holes in the system is plotted as a function of simulation time in Fig. 5 for four separate gate voltages. In each case the system stabilizes at an increasing number of holes with increasing negative gate bias. Furthermore, there is a linear relationship between the number of holes in the system after stabilization and gate bias (shown as the inset to Fig. 5). This supports the experimentally observed behavior of the width in bistability which we ascribe to a measure of the charge accumulation. Figure 6 shows the time evolution of two Monte Carlo simulations, plotting the drain current for different drain biases (at the same gate voltage). These biases are effectively above and just below the

threshold for the positive feedback mechanism. The simulations start from the same initial arbitrary charge conditions and, after some induction time whereby the initial hole distribution is rearranged, both simulations settle into a steady state charge distribution and therefore steady drain bias. The lower drain voltage simulation ($V_{ds}=0.3$ V) settling into a low drain current state (low hole accumulation), and the high drain voltage ($V_{ds}=0.5$ V), as in Fig. 5, settling into a high drain current (high hole accumulation). However, if the high charge state simulation is stopped, and then restarted with the lower drain bias ($V_{ds}=0.3$ V) using the $V_{ds}=0.5$ V charge distribution as restart conditions, the system settles into a different charge state with a much higher number of holes for the same source-drain and gate potentials. This is shown in Fig. 6 after $t=3.5$ ns (dotted line). The difference between these two curves is simply the differing charge states resulting in the bistability presented in Figs. 1 and 2.

The feedback and subsequent bistability are seen strongly in the gate leakage (Fig. 3). The origin of the excess current and the bell curve is often cited as evidence of impact ionization generated hole leakage in type II systems such as InAs/AlSb (Refs. 9 and 10) where no barrier exists to inhibit the loss of carriers. Generally in these type II systems, the enhancement of gate current can be orders of magnitude greater than the background Schottky leakage and is a major problem for the gate leakage in this materials system.[10] However, in our type I system, holes are inhibited by the valence band barrier, and so our gate current enhancement (bell curve) is substantially smaller. The sharp positive feedback effect seen in our output characteristic manifests itself in the gate leakage curves as the abrupt turning off of the gate leakage attributed to holes. For sufficiently negative V_g, the leakage of holes to the gate causes the impact ionization/hole accumulation process to shut down. At sufficiently high V_{ds} the gate will acquire an accumulation of holes that holds the gate potential low (the origin of the high conductance state). However, as V_g becomes negative the channel becomes pinched off, this leads to a reduction in the impact ionization

rate, and consequently fewer holes drifting back to the gate region so there is no longer a steady state of hole accumulation and leakage. As a result the potential barrier created by V_g will be raised, and the positive feedback mechanism in this instance rapidly turns the device off. The rapid shutting off of the impact ionization process is reflected in the sudden collapse of the excess gate leakage; this is demonstrated in Fig. 3 at the left hand edge of the bell curves.

V. CONCLUSION

We have observed a conductance kink in the output characteristic of an InSb/AlInSb QW FET that is extremely temperature dependent, such that at 1.6 K the kink becomes significantly pronounced. At sufficient gate bias the drain current becomes unstable, showing strong hysteresis for different voltage sweep directions. We attribute this behavior to the accumulation of charge under the gate region of the device. This has a positive feedback on the device output current related to the decrease in the potential under the gate, which in turn opens the gate further. This is consistent with the behavior observed using a 2D Monte Carlo simulation, showing hole accumulation and charge induced bistability and associated hysteresis.

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