Novel Highly Efficient Broadband Continuous Power Amplifier Modes

A thesis submitted to Cardiff University
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Doctor of Philosophy

By

Vincenzo Carrubba, M.Sc.

Division of Electronic Engineering
School of Engineering
Cardiff University
United Kingdom

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Broadband Continuous
Power Amplifier Modes

.... To my wife Mari,

with all my love ....

If someone feels that they had never made
a mistake in their life, then it means they
had never tried a new thing in their life.
"Albert Einstein"

- VRNGU -

Declaration of Originality

This work has not previously been accepted in substance for any degree and is not concurrently submitted in candidature for any degree.

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Abstract

The power amplifier is one of the most important and crucial component of the wireless networks due to its high power consumption. For this reason, in the last 20-30 years many scientists from all around the world have addressed the issue of how minimising such power consumption, which means maximising the PA efficiency as well as gain while delivering the expected power and the appropriate linearity for the specified frequency. Nowadays due to the continuous demand of wireless services, PAs with high power-efficiency for the specified narrow band frequency are not enough. Such PAs have to be capable to deliver satisfactory output performance for the wide spectrum frequency. For this reason, the work presented in this thesis is focused around the PA stage and describes a new way to design broadband power amplifiers used in the wireless communication systems. For the first time this work presents what have been termed "*Continuous Modes*". It is known that for delivering high efficiency states, output high harmonic impedances must be taken into account. However, the knowledge of where such harmonic terminations should be once found the singular optimum fundamental load would deliver the high efficiency condition but will not reveal information in terms of bandwidth. In this work it is demonstrated that if varying the reactive part of the fundamental impedance from the optimum condition and adjusting reactively the high harmonic terminations in accordance with the Continuous theory applied to the different PA classes, a new "*Design Space*" where the output performance remains theoretically constant can be achieved. Furthermore, varying both reactively and resistively the fundamental load and again adjusting the magnitude and phase of the high harmonic terminations a yet wider design space would be revealed with the output performance slightly degraded from the optimum condition but still giving satisfactory performance. The degradation of such performance is balanced to the fact that now new alternative solutions are revealed allowing more flexibility in the PA design. Now the PA designer can decide which new impedances to target if designing narrow band PAs or he can decide to target more solutions for which broadband PAs can be realised.

The research presented in this thesis shows the theoretical Continuous Mode theory applied to the various PA classes supported by experimental measurement results using the *Waveform Engineering Time Domain Active Envelope Load-Pull* system developed at Cardiff University applied to different transistors technology and sizes. Besides, a Continuous Class-FV PA delivering around 10.5 W of average power, 11 dB of average gain and 65-80% of drain efficiency for an octave bandwidth between 0.55 GHz and 1.1 GHz has been designed and realised.

List of Publications

First Author:

1. V. Carrubba, S. Maroldt, M. Mußer, H. Walcher, M. Schlechtweg, R. Quay, O. Ambacher, "Dual-Band Class-ABJ AlGaN/GaN High Power Amplifier," *42nd IEEE European Microwave Conference (EuMC)*, pp. 635-638, October 2012.

2. V. Carrubba, R. Quay, M. Schlechtweg, O. Ambacher, M. Akmal, J. Lees, J. Benedikt, P. J. Tasker, S. C. Cripps "Continuous-ClassF3 Power Amplifier Mode Varying Simultaneously First 3 Harmonic Impedances," *IEEE MTT-S Microwave Symposium Digest*, pp. 1-3, June 2012.

3. V. Carrubba, M. Akmal, R. Quay, J. Lees, J. Benedikt, S. C. Cripps, P. J. Tasker "The Continuous Inverse Class-F Mode With Resistive Second Harmonic Impedance," *IEEE Transaction on Microwave Theory and Techniques*, Vol. 60, Issue 6, pp. 1928-1936, June 2012.

4. V. Carrubba, J. J. Bell, R. M. Smith, Z. Yusoff, J. Less, J. Benedikt, P. J. Tasker, S. C. Cripps, "Inverse Class-FJ: Experimental Validation of a New PA Voltage Waveform Family," *IEEE Asia Pacific Microwave Conference (APMC)*, pp. 1254-1257, December 2011.

5. V. Carrubba, A. L. Clarke, M. Akmal, Z. Yusoff, J. Lees, J. Benedikt, S. C. Cripps, P. J. Tasker "Exploring the Design Space for broadband PAs Using the Novel "Continuous Inverse Class-F Mode," *IEEE European Microwave Conference (EuMC)*, pp. 333-336, October 2011.

6. V. Carrubba, J. Lees, J. Benedikt, P. J. Tasker, S. C. Cripps, "A Novel Highly Efficient Broadband Continuous Class-F RFPA Delivering 74% Average Efficiency for an Octave Bandwidth," *IEEE MTT-S Microwave Symposium Digest*, pp. 1-1, June 2011.

7. V. Carrubba, A. L. Clarke, S. P. Woodington, W. McGenn, M. Akmal, A. Almuhaisen, J. Lees, S. C. Cripps, P. J. Tasker, J. Benedikt "High-Speed Device Characterization Using an Active Load-Pull System and Waveform Engineering Postulator," *IEEE Microwave Measurement Conference (ARFTG)*, pp. 1-4, June 2011.

8. V. Carrubba, A. L. Clarke, M. Akmal, J. Lees, J. Benedikt, P. J. Tasker, S. C. Cripps "On the Extension of the Continuous Class-F Mode Power Amplifier," *IEEE Transaction on Microwave Theory and Techniques*, Vol. 59, Issue 5, pp. 1294-1303, May 2011.

9. V. Carrubba, A. L. Clarke, M. Akmal, J. Lees, J. Benedikt, P. J. Tasker, S. C. Cripps "The Continuous Class-F Mode Power Amplifier," *IEEE European Microwave Conference (EuMC)*, pp. 432-435, September 2010.

Co-Author:

10. P. J Tasker, V. Carrubba, P. Wright, J. Lees, J. Benedikt, S. Cripps, "Wideband PA Design: The "Continuous" Mode of operation," *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, pp. 1-4, October 2012.

11. M. Akmal, L. Lees, H. Choi, S. Bensmida, V. Carrubba, J. Benedikt K. Morris, M. Beach, J. McGeehan, P. J. Tasker, "Characterization of memory Effects for Complex Multi-tone Excitations using Broadband Active Baseband Load-pull," *42nd IEEE European Microwave Conference (EuMC)*, pp. 1265-1268. October 2012.

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14. M. Akmal, J. Lees, V. Carrubba, Z. Yusoff, J. Benedikt, P. J. Tasker "Multi-tone Measurement Infrastructure for Microwave Power Transistor Characterization under Wideband Multi-tone Stimuli," *International Journal of Remote Sensing Applications (IJRSA)*, April 2012.

15. M. Akmal, J. Lees, V. Carrubba, Y. Zubaida, S. Woodington, J. Benedikt, P. J. Tasker, S. Bensmida, K. Morris, M. Beach, J. McGeehan "An Enhanced Modulated Waveform Measurement System for the Robust Characterization of Microwave Devices Under Modulated Excitation," *IEEE European Microwave Integrated Conference (EuMIC)*, pp. 180-183, October 2011.

16. M. Akmal, V. Carrubba, J. Lees, S. Bensmida, J. Benedikt, K. Morris, M. Beach, J. McGeehan, P. J. Tasker "Linearity Enhancement of GaN HEMTs Under Complex Modulated Excitations by Optimizing the Baseband Impedance Environment," *IEEE MTT-S Microwave Symposium Digest*, pp. 1, June 2011.

17. Z. Yusoff, M. Akmal, V. Carrubba, J. Lees, J. Benedikt, P. J. Tasker, S. C. Cripps "The Benefit of GaN Characteristic over LDMOS for Linearity

Improvement Using Drain Modulation in Power Amplifier System," *IEEE Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC),* pp. 1-4, April 2011.

18. M. Akmal, J. Lees, V. Carrubba, S. Bensmida, S. Woodington, J. Benedikt, K. Morris, M. Beach, J. McGeehan, P. J. Tasker "Minimization of Baseband Electrical Memory Effects in GaN HEMTs Using Active IF Load-Pull," *IEEE Asia Pacific Microwave Conference (APMC)*, pp. 7-10, December 2010.

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Achievements During the PhD Course

- **Recipient** of the ***"EuMC Microwave Prize"***, at the European Microwave Conference (EuMC), Amsterdam, 2012, for the paper entitled "*Dual-Band Class-ABJ AlGaN/GaN High Power Amplifier*".

- **Recipient of** the **"Honourable Mention"** at the Student Paper Competition, IMS 2011, Baltimore, for the paper entitled: *"A Novel Highly Efficient Broadband Continuous Class-F RFPA Delivering 74% Average Efficiency for an Octave Bandwidth"*.

- **Finalist** in the *"**EuMIC Young Engineers Prize**"* at the European Microwave Integrated Conference (EuMIC), Paris, 2010, for the paper entitled: *"The Continuous Class-F Mode Power Amplifier"*.

- **Won** with Cardiff University and Freescale Semiconductor et. al. the "***Silver Excellent Award 2012***" with the OPERA-Net project – a Celtic Eureka funded R&D European project.

List of Abbreviations

WLAN – Wireless Local Area Network

RF – Radio Frequency

1G – First Generation

AMPS – Advanced Mobile Phone Service

NMT – Nordic Mobile Telephone

TACS – Total Access Communications System

FDMA – Frequency Division Multiple Access

2G – Second Generation

GSM – Global System for Mobile Communications

TDMA – Time Division Multiple Access

3G –Third Generation

UMTS – Universal Mobile Telecommunication Systems

CDMA – Code Division Multiple Access

WCDMA – Wideband CDMA

4G – Fourth Generation

WPAN – Wireless Personal Area Network

QoS – Quality of Service

WiMAX – Worlwide Interoperability

LTE – Long Term Evolution

LTE Advanced – Long Term Evolution Advanced

OFDM – Orthogonal Frequency Division Multiplexing

MIMO – Multiple Input Multiple Output

2.5G – Second and half Generation

ELF – Extremely Low Frequency

SLF – Super Low Frequency

ULF – Ultra Low Frequency

VLF – Very Low Frequency

MF – Medium Frequency

HF – High Frequency

GaAs – Gallium Arsenide

GaN – Gallium Nitride

AlGaN – Aluminum Gallium Nitride

HBT – Heterojunction Bipolar Transistor

MESFET – Field Effect Transistor

PHEMT – Pseudomorphic High Electron Mobility Transistor

MMIC – Monolithic Microwave Integrated Circuits

OPERA-Net – Optimising Power Efficiency in mobile Radio Network

CO_2 – Carbon Dioxide

EU – European

PA – Power Amplifier

ELP – Envelope Load Pull

DUT – Device Under Test

VNA – Vector Network Analyser

FFT – Fast Fourier Transformation

IFFT – Inverse Fast Fourier Transformation

$I_{GEN\text{-}PLANE}$ – Current Generator Plane

ADC – Analogue to Digital Converter

MTA – Microwave Transition Analyzer

CW – Continuous Wave

HT – Harmonically Tuned

IMD – Intermodulation Distorsion

PUF – Power Utilization Factor

ZVS – Zero Voltage Switching

ADS – Advanced Design System

PAR – Peak to Average Ratio

HFET – Heterostructure Field Effect Transistor

RFMD – Radio Frequency Microwave Devices

MLIN – Microstrip Line

BO – Back Off

ACP – Adjacent Channel Power

ACPR – Adjacent Channel Power ratio

Table of Contents

Chapter 1

Introduction

1.1 Introduction

In the past 10-15 years the development of wireless communication has proceeded rapidly and could arguably, nowadays, be described as indispensable. Consumer electronics such as cellular telephones and wireless computer peripherals such as Bluetooth, Wireless Local Area Network (WLAN) devices and satellite communication systems are just a few examples of the wireless devices and technologies that have become part of everyday life.

In this Chapter the history of wireless communication is presented, from Morse Code to the latest wireless technologies. Here a more detailed presentation of the different mobile phone generations are presented starting from the first generation (1G), where only voice data was transmitted, to the fourth generation (4G) where mobile phones have become interactive devices capable of managing several aspects of peoples' lives.

1.2 The History of Wireless Communication

Wireless communication involves the transfer of information between two points without connection. The first wireless communication system was the telegraph invented by Samuel Morse in 1838. Later in 1870, Alexander Graham Bell invented the telephone [1-2].

The concept of transmitting signals without cables at high frequencies over large distances was developed at the time where radar was under intensive development as was the first major application of microwave communications during World War II. Even if the theory was developed and applied many years ago, significant developments have kept the field of wireless communications active and vibrant for high frequency devices, microwave integrated circuits and broadband applications of modern Microsystems [3]. The foundation of electromagnetic theory was formulated in 1873 by James Clerk Maxwell [4] who hypothesized through mathematical considerations that electricity, magnetism and even light are all the manifestations of the same phenomena: the electromagnetic field. After the discovery of this theory many important scientists have built upon Maxwell's theory from Heaviside to Hertz.

However, the first person to develop a wireless communication technology using electromagnetic propagation was Guglielmo Marconi in 1894. Numerous investigators had been exploring Maxwell's theory in the previous years, but Marconi was the first to be commercially successful. Initially such a system was used to provide communications with ships at sea [2], and from this basic principle additional developments had been made for military applications during the Second World War. Later this theory was used for the development of radar, radio and satellite communications which are now widely used for both military and commercial applications. The invention of the transistor, coupled with the concepts explained so far, opened the way for the *wireless communication for cellular systems*. This had a very strong impact on our way of life; statistics show that in United States more than 28 thousand people join the cellular phone system every day, motivating competitive manufacturers to provide handsets with higher performance at a lower cost.

The increased number of services offered by mobile phones has resulted in a rapid growth of demand, particularly in terms of both services and reduction of weight and sizes of the mobile phone unit. In fact the present goals are to improve quality of mobile phones services, reducing the size and weight, whilst still maintaining low costs. The reduction in size is, in practice, accompanied with the reduction in the size of the battery which must be achieved without compromising the final performance. In each mobile handset, the power amplifier is required to transform the DC battery power into RF energy. This results in the need to design high performance amplifiers that operate efficiently with the aim of reducing the DC power consumption as well as maintaining the linearity requirement. The achievement of the high efficiency state is a very complex process especially when targeting it for multiple frequencies. For this reason the research presented in this thesis will show the possibility to extend the high power-efficiency state over bandwidth.

1.3 Mobile Phone Generations

Communication is at the heart of human activity and the advent of wireless technology has allowed communication to and from anywhere around the world [7]. In particular, the last decade has witnessed a rapid growth in the mobile cellular communications market. Mobile phone technology has been diffused around the world faster than any other communication technology. The first generation (1G) of cellular phones was born with the aim of carrying only voice data. Nowadays mobile phones have become multi-functional and interactive devices capable of various and advanced services: video call, text and video messages as well as internet with all its services. As shown in Fig. 1.1, in 1995 less than 2% of the global population used mobile phones while in 2010 subscriber numbers increased to almost 50%, and therefore following this trend nowadays (2012-2013) such number has definitely increased to more than 50%.

(a) Global mobile phone subscribers 1995 **(b) Global mobile phone subscribers 2010**

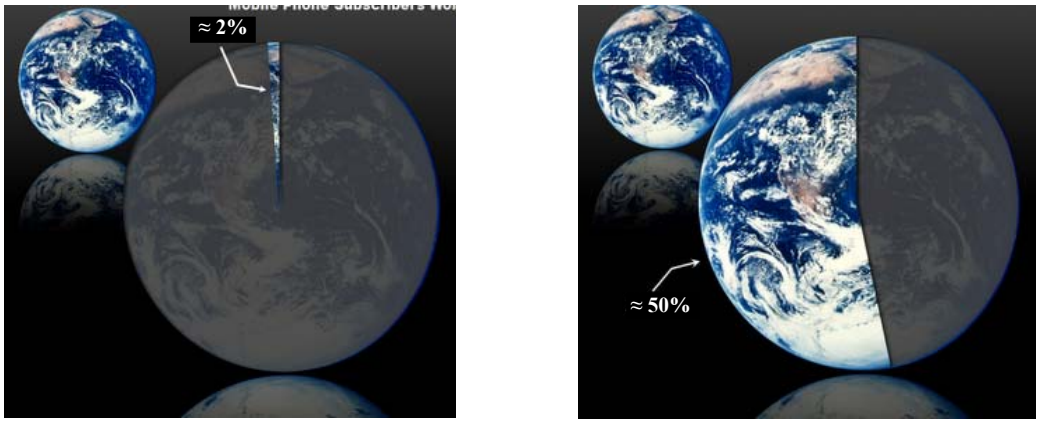

Fig. 1.1 – Global mobile phone subscribers in (a) 1995 and (b) 2010.

1.3.1 First Generation Networks – 1G

First generation (1G) mobile phone networks were the earliest cellular systems to be developed. The first cellular network was born in Chicago (USA) in 1978. This system used a technology called AMPS (*Advanced Mobile Phone Service*) working at a frequency of 800 MHz [8].

In 1981 the Nordic Mobile Telephone System (NMT 450) from Scandinavia, using the 450 MHz band (and later even working at 900 MHz), was the first one to introduce first generation mobile phones in Europe. Later, in 1985 the United Kingdom introduced a new technology similar to the AMPS called TACS (*Total Access Communications System*) working at 900 MHz [9-10].

This First Generation phones were analogue, used for voice calls only, and their signals were transmitted by the method of frequency modulation (FM) [10]. These systems typically allocated one 25 MHz frequency band for the signals to be sent from the cell base station to the handset, and a second different 25 MHz band for signals being returned from the handset to the base station. These bands were then split into a number of communications channels, each of which would be used by a particular user. Each channel was separated from the adjacent channels by a spacing of 30 KHz, which was not particularly efficient in terms of the available radio spectrum. This therefore placed a limitation on the number of calls that could be made at any one time.

However, the system was a multiple access one, since a second caller could use the same channel once the first caller had hung up. Such a system is called "frequency division multiple access" (FDMA) [9, 11]. In addition, because the output power of the transmitter's cell is restricted and designed to cover a specific area, it was possible to use the same frequencies in other cells that were far enough away to avoid interferences. This system is called frequency re-use, and enables the network capacity to be increased. When the user passes from one cell area to another it is important that the call is not interrupted, this is prevented by a process called handover.

Although First Generation systems had a very important impact, they showed some problems both in terms of privacy and user capability.

1.3.2 Second Generation Networks – 2G

Due to the rapidly increase of users, the Second Generation (2G) mobile telephone networks were the logical next stage in the development of wireless systems after 1G. Such increase of users, particularly in the areas with higher population density, meant that increasingly sophisticated methods had to be employed to handle the large number of calls, and so avoid the risks of interference and dropped calls [8].

Although many of the principles involved in the 1G system also apply to 2G there were differences in the way that the signals were handled. The 1G networks were not capable of providing the more advanced features of the 2G systems, such as caller identity and text messaging.

One of the successful 2G digital systems is GSM (*Global System for Mobile Communications*), a mobile phone standard that was developed during the 1980s. The GSM system is able to utilise any of the three frequency bands at 900, 1800 and 1900 MHz, and many GSM phones can operate as dual-band or tri-band phones, whereby they adapt to the local frequency system in the region the user travels through [11]. In GSM 900, for example, two frequency bands of 25 MHz bandwidth are used. The band 890-915 MHz is dedicated to uplink communications from the mobile station to the base station, and the band 935-960 MHz is used for the downlink communications from the base station to the mobile

station. Each band is divided into 124 carrier frequencies, spaced 200 KHz apart, in a similar fashion to the FDMA method used in 1G systems. Then, each carrier frequency is further divided using the TDMA (*Time Division Multiple Access*) technology into eight 577 μS long "time slots", every one of which represents one communication channel. The total number of possible channels available is therefore 124 x 8, producing a theoretical maximum of 992 simultaneous conversations [8-10].

1.3.3 Third Generation Networks – 3G

The data rates supported by the basic 2G networks were only 9.6 kbps, which was inadequate to provide any sophisticated digital services [8-12].

The next step forward was the third generation (3G). Many countries, before having 3G networks, had the intermediate stage of 2.5G [10]. The significant features of 3G systems are that they support much higher data transmission rates and offer increased capacity, which makes them suitable for high-speed data applications as well as for traditional voice calls. In fact, 3G systems are designed to process data and since voice signals are converted to digital data, this could be easily handled, in the same way as any other form of data. [12].

The benefits of higher data rates and greater bandwidth mean that 3G mobile phones can offer subscribers a wide range of data services, such as mobile internet access and multimedia applications. Compared with earlier mobile phones, a 3G handset provides many new features and the possibilities for new services are almost limitless. This includes many popular applications such as TV streaming, multimedia, video-conferencing, web browsing, e-mail, paging, fax, and navigational maps.

The main 3G technologies include UMTS *(Universal Mobile Telecommunication Systems*) CDMA (*Code Division Multiple Access*) and later WCDMA (Wideband CDMA) technology [6, 10]. It is generally accepted that CDMA and WCDMA are a more advanced superior transmission technology compared to the old techniques used in GSM/TDMA.

The Third Generation of mobile phones is also designed for global roaming throughout most parts of the world. However, in some parts of the world there are

problems due to different standards where there exists only a 2G or 2.5G network, with the 3G service not available.

The operating frequencies of many 3G systems will typically use parts of the radio spectrum in the region of approximately 2 GHz, which were not available to operators of 2G systems. UMTS systems are designed to provide a range of data rates, depending on the user's circumstances, providing up to 144 kbps for moving vehicles, up to 384 kbps for pedestrians and up to 2 Mbps for indoor or stationary users.

1.3.4 Fourth Generation Networks – 4G

The worldwide ongoing development of 3G standards has driven research into what will be the fourth generation (4G) of mobile communication technologies. Here, one of the aims is to provide higher transmission rates, around 100 Mb/s for high mobility communication such as from cars and trains and 1 Gb/s for low mobility communication such as pedestrians or when stationary [12]. The 4G standard is not only characterised by higher data rates but it is also characterised in terms of user capacity, data convergence and in general more services with better quality. Here the call is not interrupted in the case when a terminal moves from one cell to another one thanks to the handover concept [13]. This basically means that any user can move in freedom anywhere and anytime while using the same services according to their specific requirements. In addition, 4G provides flexible interoperability of the various kinds of existing wireless networks, such as satellite, cellular wireless, WLAN (Wireless Local Area Network), WPAN (Wireless Personal Area Network) [13] and systems for accessing fixed wireless networks. In a few words, the main goal is to unify the different wireless communication system networks such as computers, mobile phones and personal devices in order to overcome the heterogeneity of the existing networks, which is meant to become a major part of future mobile communication networks [14]. A 4G system is expected to provide high Quality of Service (QoS), high security and reliability and low power consumption in broadband applications. Wide bands of frequency are necessary in 4G systems in order to transfer the high amount of data with the high data-rates previously mentioned.

Pre-4G technologies such as mobile WiMAX (Worldwide Interoperability for Microwave Access) and first-release of long term evolution (LTE) have been on the market since 2006 and 2009 respectively, and are often branded as 4G in marketing materials. The current versions of these technologies provide downstream peak bit-rates of 144 Mbit/s and 100 Mbit/s respectively, therefore they consequently do not fulfill the original requirements of data rates approximately up to 1 Gbit/s for 4G systems. Advanced versions of the above two standards are under development and called "LTE Advanced" and "WirelessMAN-Advanced" respectively. These two standards and other evolved 3G technologies that do not completely fulfil the proper requirements, could be considered "4G", as they provide a substantial level of improvement in performance and capabilities with respect to the initial third generation systems now deployed [15].

In all 4G standards, the CDMA spread spectrum radio technology used in 3G systems and IS-95 is abandoned and replaced by OFDM (Orthogonal Frequency Division Multiplexing) and MIMO (Multiple Input Multiple Output) [15]. Fig. 1.2 shows the global mobile phone subscriptions increase (left Fig.) and base stations by technology (right Fig.) from 2009 to 2013 (estimated). It can be seen that in 2009 the subscribers using the 2G, 2.5G and 3G with mainly the GSM and W-CDMA standards were around 4.5 billion, whilst nowadays (2011-2012) the people who use mobile phones with the previous and/or new standards are more than 5 billion resulting in more than 50% of all the global population, accounting for a population of over 7 billion people.

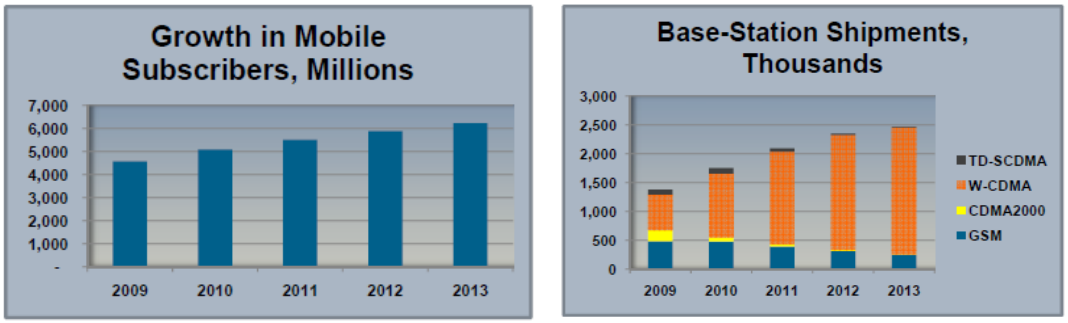

Fig. 1.2 – Global growth on cellular subscribers (left) and base station.

Fig. 1.3 shows the progress tree of communication technology summarizing the different mobile phone generations [16]. The first generation (1G) is on the bottom

of the tree, and by moving towards the top of the tree, it can be seen the second and third generations (2G and 3G) and then the latest generation 4G straight on the top. Here, it can be noted that 4G is shown as an integration of systems interworking with each other as explained previously.

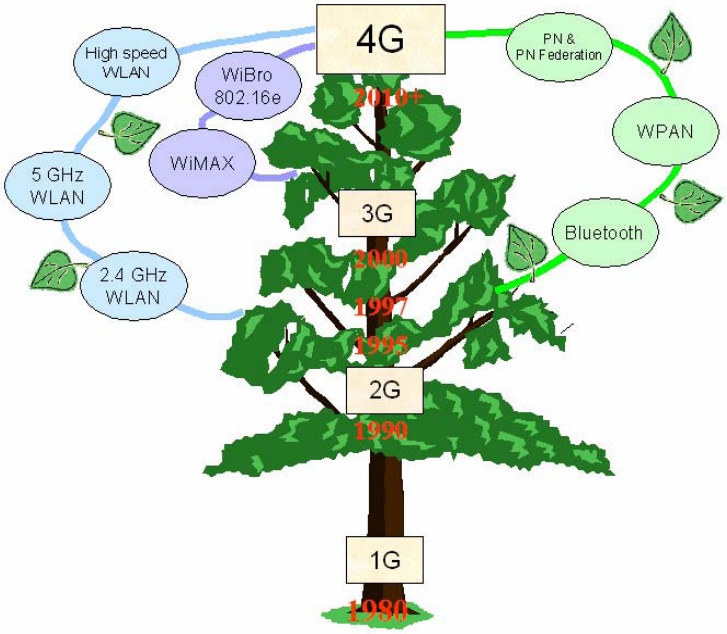

Fig. 1.3 – The progress tree of communication technology [16].

1.4 Introduction to RF/Microwave Engineering

Microwave and radio frequency (RF) engineering is an exciting and dynamic field. Initially it was exclusively used in the military industries, but the dramatic explosion for communication systems with such applications as wireless computer networks, broadcast video and especially mobile telephony with the continued demand for voice, data, and video communication has revolutionised the industry. The high frequencies permit both large numbers of independent channels for a wide variety of uses envisioned as well as significant available bandwidth per channel for high speed communication. Besides, they have the added advantage of being able to penetrate fog, dust, foliage and even buildings.

Electromagnetic energy is transmitted into different frequencies, and the properties of the signal and the energy depend on those frequencies [1]. The

amount of spectrum allocated to these different uses differs by frequency band as well as country. In the low frequency spectrum there are the Extremely Low Frequency (ELF) in the range of 3-30 Hz, the Super Low Frequency (SLF) from 30 Hz to 300 Hz, the Ultra Low Frequency (ULF) from 300 Hz to 3 KHz, the Very Low Frequency (VLF) ranking between 3 KHz to 30 KHz and the Medium Frequency (MF) from 300 KHz to 3 MHz. Fig. 1.4 shows the location of the frequency band in the electromagnetic spectrum starting from the high frequency (HF) up to the X-Rays, while Table 1.I [17] shows some typical application used at the different frequencies.

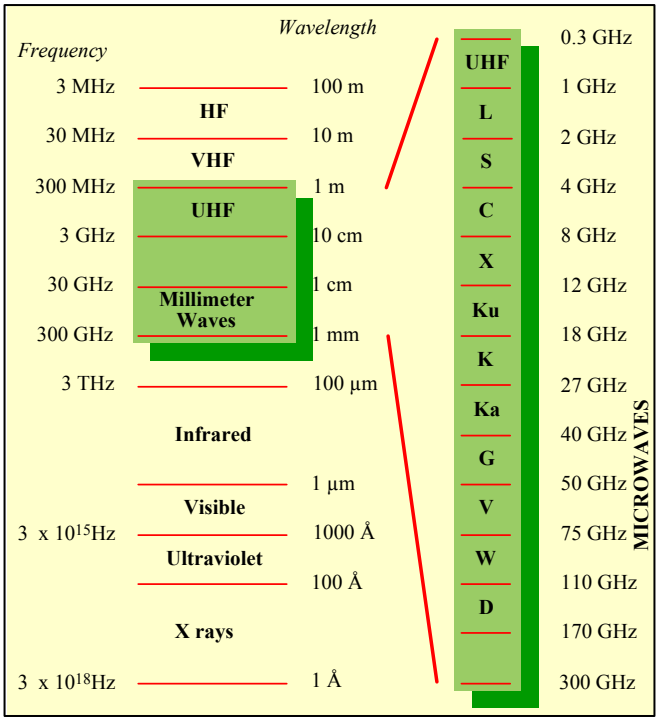

Fig. 1.4 – The electromagnetic spectrum.

The most fundamental characteristic that distinguishes RF engineering from microwave engineering is directly related to the frequency, and thus the wavelength of the electronic signals being processed. For low frequency and RF circuits the signal wavelength is much larger than the size of the electronic system and circuit components. In contrast, for microwave systems the size of typical electronic components is often comparable to the signal wavelength. This concept introduces the two areas used in RF/microwave designs. Since in conventional RF

design, the circuit components and interconnections are generally small compared to a wavelength, with good approximation they can be modelled as lumped elements.

TABLE 1.I
TYPICAL APPLICATIONS FOR DIFFERENT FREQUENCIES

Application	*Frequency*	*Application*	*Frequency*
Military Communications	ELF	US cellular	824-849MHz 869-894MHz
AC – electric power transmission	SLF	European GSM cellular	880-915MHz 925-960MHz
Earthquakes monitoring	ULF	GPS	1575.42MHz 1227.6MHz
AM broadcast band	535-1605KHz	Microwave ovens	2.45GHz
Short wave radio band	3-30MHz	US DBS	11.7-12.5GHz
VHF TV	54-88MHz	US ISM bands	902-928MHz 2.4-2.484GHz 5.725-5.85GHz
UHF TV	174-890MHz	US UWB radio	3.1-10.6GHz

For microwave frequencies however, the time delay associated with signal propagation between two components is a big fraction of the signal period, and thus lumped element descriptions are no longer adequate to describe the electrical behaviour. In this case a distributed-element model is required to accurately capture the electrical behaviour.

Although the utilisation of lumped-element components were not advisable at microwave frequencies due at the time delay propagation, the miniaturisation of active and passive components often increases the frequencies at which lumped element circuit models are sufficiently accurate. Reducing the component dimensions proportionally reduces the time delay for propagation through a component. As a consequence, lumped element components at microwave frequencies are becoming increasingly common in systems previously based only on distributed elements, even if the operational frequencies remain unchanged. The negative side of component and circuit miniaturisation is the introduction of potentially new parasitic distributed-element effects that could previously be treated using lumped-element RF models.

Traditional microwave engineering, starting with its historically military applications, has been focused for long time on delivering performance at any cost. As a consequence, only special-purpose devices have been developed and used at microwave frequencies, often obtaining narrow ranges of applicability.

With continuing advances in silicon microelectronics, new high performance materials using III-V semiconductor compound such as gallium arsenide (GaAs) or gallium nitride (GaN) have been developed in 1980. The high performance of these materials allowed the development of heterojunction-bipolar-transistors (HBTs), field-effect transistors (MESFETs) and pseudomorphic high electron mobility transistors (pHEMTs) [18]. These electronic devices made with the advanced quality of the semiconductors that can operate at higher current density and lower rail voltages, provide very high frequencies capability, up to 100 GHz, with greater output powers [6].

This development, with silicon microelectronics moved from low-frequencies into the microwave spectrum, is accompanied by a shift from physically large devices, low-integration-level hybrid implementations to very small devices, highly integrated solutions based on monolithic-microwave-integrated-circuits (MMICs). Here, the small size of components and the advanced processing techniques using the silicon substrate enables the integration of both active and passive components. As a result the smaller circuit design operating at reduced supply voltages introduced the possibility to use them in the development of wireless communication for mobile phone systems.

One interesting aspect of raising the frequencies is that a lot of physical effects that are negligible at lower frequencies become increasingly important. In the microwave world these aspects are studied everyday, where for a given device a completely different behaviour can be observed with changing frequencies.

1.5 OPERA-NET - Optimising Power Efficiency in mobile RAdio NETworks

The research presented in this thesis has been carried out as part of the OPERA-Net (Optimising Power Efficiency in mobile RAdio NETworks). The OPERA-Net is a European project that aims to constitute a task force through a holistic approach considering a complete end-to-end system [11], identifying all relevant network elements and their interdependencies [19].

According to publicly available data, base station power consumption account for approximately 200 to 500 GW per year per operator in some European countries.

In the UK, the mobile industry accounts for around 0.7% of CO_2 emissions and each mobile subscriber is responsible for around 55 kg of CO_2 per year.

Europe has embarked on an ambitious plan to cut its energy consumption by around 20% by 2020. This is in order to fight climate change due to the millions of tonnes of CO_2 emitted into the atmosphere, as well as reducing the overall costs by more than €100 billion annually [20].

In particular, the main focus of the OPERA-NET project is to address the power and energy efficiency technology barrier to implement next generation mobile broadband systems encompassing terminal, infrastructure and end-to-end systems, trying to allow the EU industry to take a leadership role in environmentally sustainable mobile networks.

Power and energy efficiency within the wireless technology industry is not a new phenomenon. In an RF end-to-end system a lot of energy is dissipated between each block, but the block that dissipates the most is the power amplifier (PA) [3]. For this reason it is very important to achieve and maintain higher efficiency over bandwidth as it will be demonstrated in this thesis. Saving power in the order of single-digit watts in a single PA means saving many kilowatts at base station level, which means saving gigawatts or terawatts at national level [19].

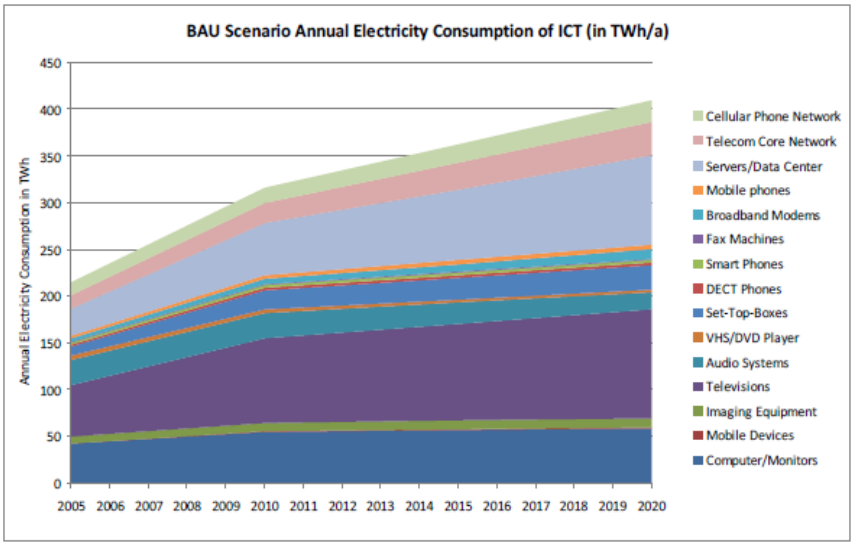

Fig. 1.5 – Annual Electricity Consumption [19].

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Chapter 2

Measurement Systems, Load-Pull and Power Amplifier Modes

2.1 Introduction

This Chapter 2 will introduce some of the waveform measurement system concepts with different passive and active load-pull configurations. Here the meaning of linear and especially non-linear concepts typical of power transistor behaviour will be explored. As most of the various measurements conducted within this research, and presented in this thesis, have been conducted using the active envelope load-pull (ELP) system architecture developed at Cardiff University, a more detailed analysis of this measurement system will be given. Furthermore, because most of the research described in this thesis is based on power amplifier modes through waveform engineering, a detailed analysis of the different conventional power amplifier classes will be shown. In addition, the broadband multi-solution Class-J mode, which has been the starting point of the new broadband PA classes described in the next Chapters of this thesis, will be described.

2.2 RF Waveform Engineering Measurement Systems

The achievement of valid measurements with high accuracy is not due only to the device itself, but more particularly to the correct setup of the measurement system in which the device is tested. In order to measure the device-under-test (DUT) correctly, all components of the measurement setup must be accurately modelled and calibrated.

Nowadays RF/microwave measurement systems offer constant characteristic impedance of 50 Ω at both input and output ports of a DUT. The use of a standard characteristic impedance is necessary for all microwave equipment as at high frequencies interconnection wires will have a significant electrical length in comparison to the wavelength at the application frequency, resulting in a different voltage at each end of the connection. The 50 Ω value for standard impedance (characteristic impedance Z0) was selected from the trade-off between the lowest loss and maximum power transfer for a line of coaxial cable. In order to provide the minimum attenuation in a coaxial structure with air as dielectric, the optimum ratio between the outer and inner conductor is 3.6, which corresponds to an impedance of 77 Ω. This value of impedance presents the best performance in terms of loss but does not provide for maximum peak power transfer. The best power performance is achieved when the ratio between outer and inner conductor is 1.65, which corresponds to an impedance of 30 Ω. Therefore, the value of standard 50 Ω is achieved from a compromise between 77 and 30 Ω in accordance with the formula [1]

$$50 \cong \sqrt{77 * 30}$$

The 50 Ω impedance is the standard impedance which ensures that all RF/microwave connectors and instruments present the same impedance in order to avoid reflection.

2.2.1 Linear (Small Signal) Measurement System

Simple measurements for low frequency, where measurements of voltages and currents are based on the use of open and short circuits, cannot be used at RF/microwave frequencies. The use of low frequency measurement techniques into

the high frequency world, would not be able to maintain the high and low impedances over the wide bandwidth, becoming unstable within the test environment.

To overcome this problem measurements based on incident (termed *a* wave) and reflected (termed *b* wave) travelling waves, which are related to a constant measurement impedance environment of 50 Ω, are presented. These travelling waves are related to the measurements of the scattering parameters (S-parameters) [2], which describe the linear electrical behaviour of the DUT when under various stimuli of small signals, as shown in Fig. 2.1.

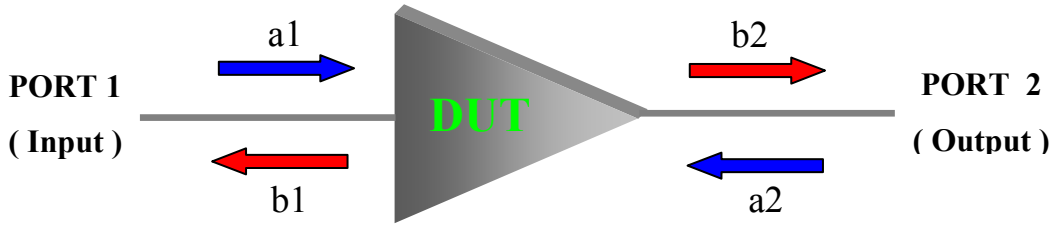

Fig. 2.1 – Travelling waves for a two port network.

The parameters a1 and b1 are the input incident and reflected travelling waves respectively at port 1, whilst a2 and b2 are the corresponding incident and reflected waves at port 2.

The linear S-parameters are the ratio between the reflected and the incident travelling waves as shown in Table 2.I.

TABLE 2.I
S-PARAMETERS FOR A TWO PORT NETWORK

	Reflection	**Transmission**
PORT 1	S11 = b1 / a1 (a2=0)	S21 = b2 / a1 (a2=0)
PORT 2	S22 = b2 / a2 (a1=0)	S12 = b1 / a2 (a1=0)

The S11 parameter gives the input port reflection coefficient (port1) while the parameter S22 gives the reflection coefficient for the output port (port2). S21 and S12 are the transmission signal from port 1 to port 2 and the transmission signal from port 2 to port 1 respectively.

The relationship between voltage and current with the travelling waves a and b are:

$$a1 = \frac{V1^{+}}{\sqrt{Z0}}; \quad b1 = \frac{V1^{-}}{\sqrt{Z0}} \ , \tag{2.1}$$

where

$$V1 = V1^{+} + V1^{-} = \left(a1 + b1\right) \cdot \sqrt{Z0}; \tag{2.2}$$

while

$$I1 = I1^{+} - I1^{-} = \frac{V1^{+} - V1^{-}}{Z0} = \frac{\left(a1 - b1\right)}{\sqrt{Z0}} \ . \tag{2.3}$$

$V1^{+}$ and $V1^{-}$ as well as $I1^{+}$ and $I1^{-}$ are the incident and reflective voltages and currents respectively [2].

The instrument used for the S-parameters measurement is known as a Vector Network Analyser (VNA) [3]. Although the VNA can capture important information, such as magnitude and phase in the frequency domain of the small signal quantities, with frequencies up to 110 GHz, it is limited to linear analysis. This means that it can capture the information using one frequency at a time and it can be only applied when the superposition principle holds true [4]. For the characterisation of power devices, where the harmonic contents are directly related to the fundamental stimulus, the superposition principle cannot be applied. Therefore, such analysis cannot be used when dealing with non-linear devices, ignoring the important effect of the higher harmonic frequencies which can cause distortion.

2.2.2 Non-linear (Large Signal) Measurement System

If the power of the input incident travelling waveform is kept within the linear region, the DUT can be characterised using S-parameters, as only a fundamental frequency component is generated by the device, and the VNA explained previously can be used. When the input drive is increased for enhanced performance, the devices are much closer to the compression region, meaning that input and output are not related to each other with a linear behaviour. In this case,

the higher frequency components generated by the non-linear nature of the device itself have to be captured for the full characterisation of the DUT behaviour.

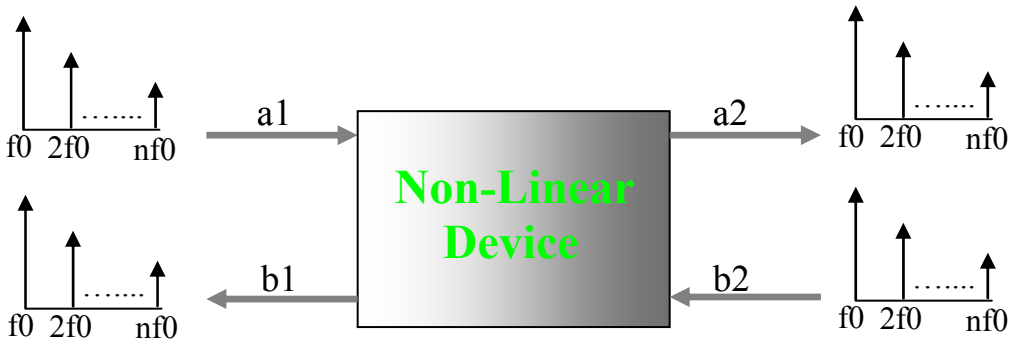

Fig. 2.2 – Non-linear stimulus for a two port network.

To overcome this problem, and to capture higher harmonics rather than fundamental only, a spectrum analyzer can be used. The spectrum analyzer is a scalar instrument capable of measuring a broad spectrum in real time for a wide dynamic range. It allows the measurement in terms of magnitude of fundamental and higher harmonics. However, it does not allow phase measurements, limiting its use for the characterisation of devices in modern measurement systems.

Different methods for the measurements of large signals for the non-linear device behaviour have been used in the past 25 years [5-6].

One method for large signal measurements is based around sampling oscilloscope technology. The first measurement system based on this concept was presented in 1989 by Sipila [7]. In this case, by using a Tektronix oscilloscope, the measured signals are converted into the frequency domain using a Fast Fourier Transformation (FFT) providing magnitude and phase information for all frequencies. After the correction of errors due to any losses or mismatches in the measurement system, the oscilloscope provides voltage and current waveforms in the time domain through the Inverse Fast Fourier Transformation (IFFT). Measurements in the time domain are of high importance to the RF design process as it enables different classes of operation to be determined by the observation of the waveforms. It will be demonstrated in Chapter 3 that when dealing for example with the Class-F mode, which requires a square voltage waveform at the intrinsic current-generator plane $I_{GEN\text{-}PLANE}$ [8-9], the same output performance in terms of

drain efficiency and power can be achieved with different shapes of the voltage waveform. This principal demonstrates that similar results can be obtained than expected from a reference waveform for different waveform shapes.

Problems with non-linear measurement systems based on the oscilloscope are introduced by limited sampling rates of the oscilloscope itself. This is because the Analogue to Digital Converter (ADC) is required to sample the full period of the measured waveforms at smaller time intervals. At higher frequencies this can result in a reduced bit resolution and reduced dynamic range [7, 10-11].

Later in 1990 a combined architecture between the VNA and the oscilloscope was presented by Kompa [12]. Thanks to the use of both instruments, this combined the high dynamic range and frequency domain capability of the VNA with the time domain waveform capture of the sampling oscilloscope. In fact, the VNA measures the complex ratio of two signals at their fundamental frequency, while the sampling oscilloscope then measures the time domain waveform components composing the ratio. The problem of this architecture (as the only VNA architecture) is that it does not capture the high harmonics behaviour, thus limiting its use to single tone device characterisation.

Nowadays there are several instruments and measurement techniques to try to understand the non-linear behaviour of the networks. One example is the PNA-X (Phase Network Analyzer-X Parameter) from Agilent where the high harmonics and thus the device non-linear behaviour can be captured and studied. Another example is the ZVA (Z Vector Analyzer) from R&S (Rhode and Schwartz). However, many scientists from all over the world are working with the aim of developing and improving the high frequency instruments in order to speed up the devices and systems (i.e. transistors and PAs) characterisation with higher accuracy. Very often these techniques offer valuable information, but never the complete answer. This is more due to the limitations of the instruments, which give only partial information, or due to the level of accuracy of the system or the calibration techniques used, giving only qualitative information.

The measurements undertaken in this research and presented in this thesis have been conducted using a measurement system based on the Microwave Transition Analyzer (MTA) previously realized and presented in [13-15]. The MTA is a 2

channel sampling scope capable to give accurate information about all the harmonic components in terms of magnitude and phase of the incident and reflected travelling waves at the input and output device ports, from DC to 40GHz.

The measurement system based on the MTA will be presented in a more detailed analysis in section 2.3.3.C.

2.3 Load-Pull Systems

The optimum performance for a power transistor is achieved by presenting the proper fundamental and harmonic load and source impedances which depend on the device-under-test (DUT). These techniques demonstrated by D. M. Snider [16] are called load-pull and source-pull respectively [17].

Source-pull is the technique for which the optimum input impedance can be presented in order to properly match the input side presenting the appropriate sinusoidal voltage for which the device power gain can be optimised. Once the power gain is optimised, the load-pull technique is used in order to identify the optimum fundamental and harmonic impedances for each design goal. In the last years many load-pull systems have been developed and used as shown in Fig. 2.3. As noted from such Fig. 2.3, the overall load-pull systems can be divided into passive and active.

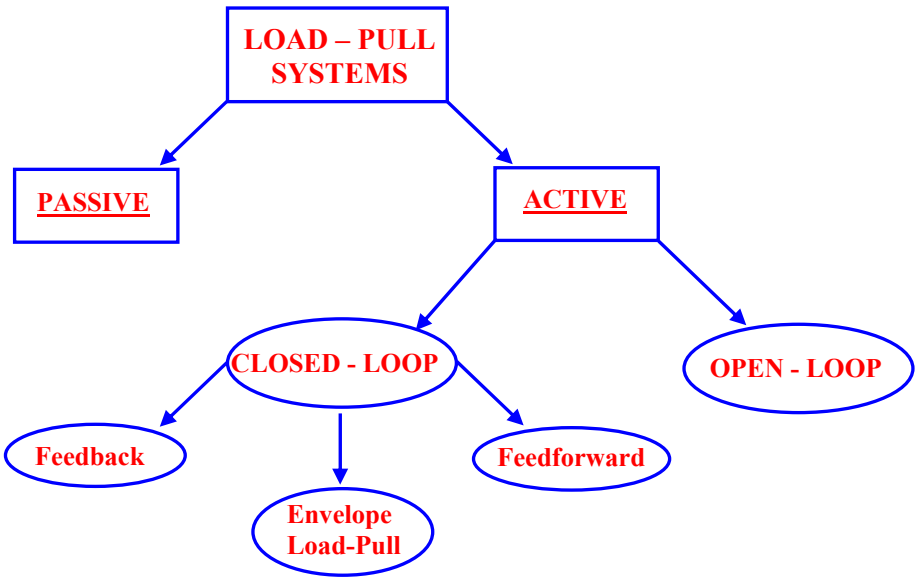

Fig. 2.3 - Load-pull systems classification.

Here the active systems are divided in open-loop and closed-loop where the open-loop are again grouped in feedback, feedforward and envelope load-pull (ELP). The details of the various systems are presented in sections 2.3.1, 2.3.2 and 2.3.3.

2.3.1 Passive load-pull system

Traditionally the emulation of load impedances has been achieved by using passive techniques, where mechanical tuners or phase shifters were used to tune the output reflection coefficient [18-20].

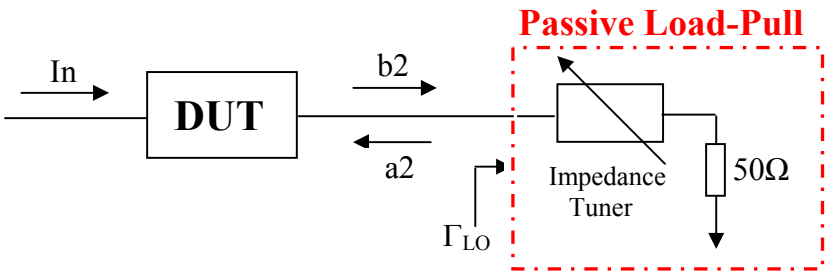

Fig. 2.4 - Passive load-pull system.

Once the DUT is stimulated by an input signal (In), the output signal b2 generated by the device flows straight into the load-pull system and by varying the impedance tuner a variation in the reflected wave a2 in terms of magnitude and phase can be achieved. The modified signal a2 is then inserted back to the output of the device, thus a reflection coefficient Γ_{LOAD} (Γ_{LO}) can be presented by dividing the signal going back into the device (a2) and the signal that flows inside the passive load-pull (b2), as shown in (2.4)

$$\Gamma_{LOAD} = \frac{a2}{b2} \tag{2.4}$$

From the load reflection coefficient it is possible to calculate the load impedance Z_{LOAD}:

$$Z_{LOAD} = Z_0 \left(\frac{1+\Gamma_{LOAD}}{1-\Gamma_{LOAD}} \right), \tag{2.5}$$

where Z_0=50 Ω is the characteristic impedance.

Despite the simplicity of passive load-pull, it cannot always be used for the characterisation of advanced power devices. This is primarily due to the fact that any losses introduced between the device itself and the load-pull system (tuners) will reduce the maximum magnitude of the modified signal a2, limiting the range of load impedances that can be presented. This means that impedances with very high reflection coefficients (i.e. Γ=1) cannot be presented due to the losses between the tuners and the device itself. For this reasons, it is very important that the tuners are placed as close as possible to the DUT. However recent works have demonstrated passive source-and-load systems with Γ near to unity [21-22].

Another disadvantage of this technique is that when tuning the single frequency of interest, it results in a variation of all the remaining higher spectral components. Therefore, the devices are constantly exposed at different harmonic impedances when tuning for the optimum fundamental one. This clearly degrades the performance of the device characterisation, especially for the high efficiency modes, where specific points (short and/or open circuits) must be presented at the higher harmonics. In this case a triplexer could be used in order to split the different harmonic contents, but it would introduces more losses resulting in reflection coefficients far from the short and open circuit conditions Γ=1 (required for the high harmonic terminations) in order to obtain the high power-efficiency condition.

2.3.2 Active Open-loop load-pull system

The first active open-loop load-pull system was developed and presented by Takayama [23] in 1976. The active systems avoid some of the limitations of passive load-pull by actively compensating for any losses introduced between the

DUT and the load-pull system/test-set itself. This allows any value of impedance to be presented to the DUT. In this case triplexers are still needed, but here injecting fundamental and higher harmonics it is possible to present the desired harmonic impedances with reflection coefficient equal to unity for both fundamental and harmonic impedances.

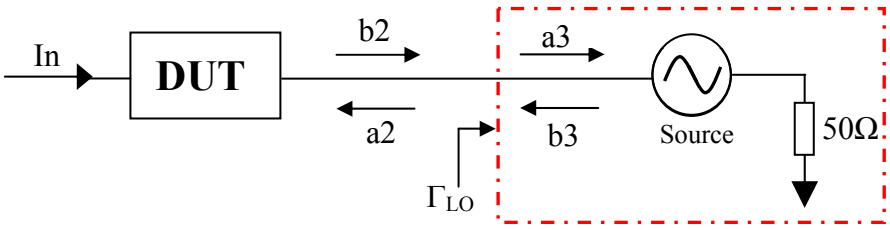

Fig. 2.5 - Generic active open-loop load-pull system configuration.

As it can be seen from Fig. 2.5, in this case the signal that goes back towards the device port 2 (b3) is directly generated by an RF signal generator. The load reflection coefficient is achieved by dividing the signal generated by the source b3 (with a2=b3) and the output signal generated from the device b2 (with a3=b2).

$$\Gamma_{LOAD} = \frac{b3}{a3} = \frac{1}{\left(s_{21} \frac{a1}{b3} + s_{22} \right)} \tag{2.6}$$

As it can be noted from Fig. 2.5 and from equation (2.6), by varying b3 it is possible to present different load impedances to the DUT.

Another advantage of open-loop load-pull is the stability. Here, it is possible to avoid oscillations in the iteration of the load impedances, which makes it suitable for the characterisation of high power devices.

However, these types of architecture are slow due to the numerous iterations required, especially when taking into account multiple harmonics, hence new advanced fast multiharmonic systems have been recently developed as presented here [24].

2.3.3 Active Closed-loop load-pull systems

Comparing passive and active open-loop load-pull systems, it appears clear that the best solution would be the combination of both. This means that a load-pull system should be robust and flexible as well as fast and able to synthesize reflection coefficients as near as possible to the edge of the Smith chart (Γ=1) .

For this purpose the active closed-loop load-pull system is presented [25]. There are two basic techniques employed for the realisation of active closed-loop load-pull configurations: *feedback load-pull* and *feedforward load-pull* [10]. A third alternative technique for achieving closed-loop load-pull has been realised at Cardiff University by Williams [26] and it has been called active "*envelope load-pull"* (ELP).

a) Feedback load-pull

The feedback load-pull shown in Fig. 2.6 is a closed-loop active technique for which high reflection coefficients can be presented.

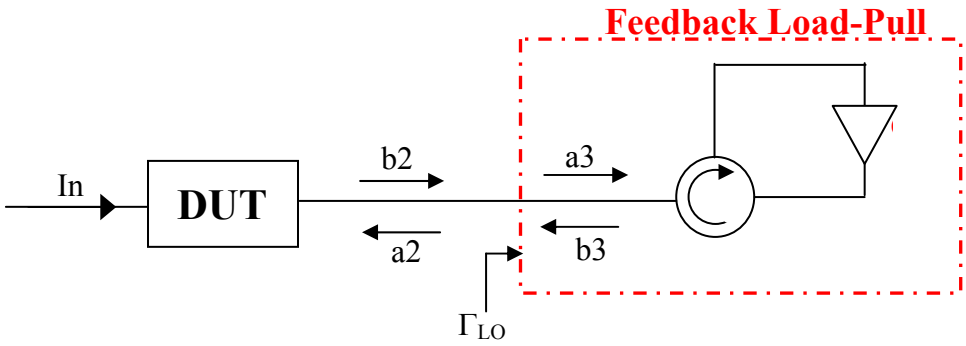

Fig. 2.6 - Feedback load-pull architecture.

Once the DUT is stimulated by an input signal, the output signal b2=a3 flows inside the circulator thus into a certain power amplifier, creating a loop varying the magnitude and the phase of that signal b3=a2 which then goes back again through the circulator toward the output of the device. In this case

$$b3 = G \cdot a3 \,, \tag{2.7}$$

and the load reflection coefficient is achieved as

$$\Gamma_{LOAD} = \frac{b3}{a3} = G \,, \tag{2.8}$$

where G causes the load variation in terms of magnitude and phase. Any value of impedance can be obtained by choosing appropriate vales of G. Fig. 2.6 represents the basic architecture for only fundamental frequency, the same concept is applied when extended it for multiple harmonic frequencies [10].

The disadvantage of this technique is that if the device becomes unstable, the feedback configuration does not control the power, with the danger of damaging the DUT and the instruments as well. For this reason, this technique is more suitable for low power devices, where thanks to the low power levels it is easier to protect the equipment from damage.

b) Feedforward load-pull

In the second active closed-loop technique, the variation of the load reflection coefficient is achieved directly by a variation of the input signal. Over the years, numerous feedforward load-pull systems have been extended and presented for load-pull characterisation at high frequencies as presented here [27-28].

Fig. 2.7 shows the basic feedforward load-pull configuration for one frequency (again, as with feedback load-pull, it can be extended for multiple frequencies).

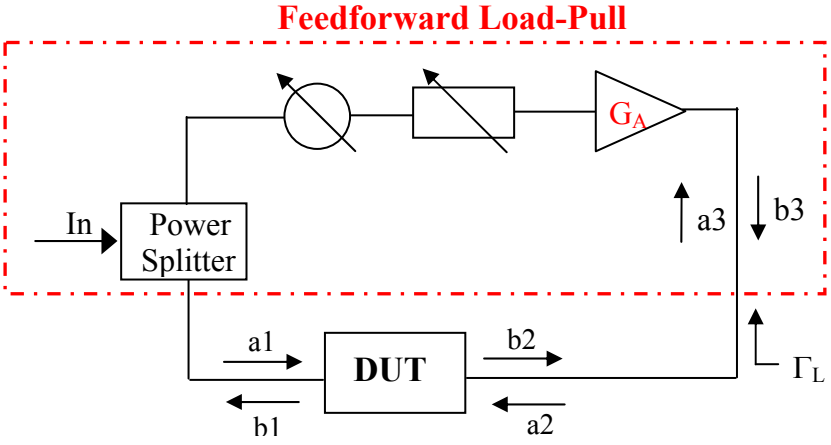

Fig. 2.7 - Feedforward load-pull architecture.

Here the input signal is divided in two parts by a power splitter, one part (a1) is forwarded to the input of the DUT and the other one is modulated by a mechanical

tuner. The signal is then amplified and the resulting signal b3 is sent to the output of the device, where:

$$b3 = G \cdot a1 \,. \tag{2.9}$$

Therefore the load reflection coefficient is achieved by:

$$\Gamma_{LOAD} = \frac{b3}{a3} = \frac{1}{\frac{s_{21}}{G} + s_{22}} \tag{2.10}$$

As it can been noted from (2.10), the signal generated from the output of the device a3 is function of the input signal a1 and the signal generated within the load-pull.

To ensure the stability condition the load reflection coefficient Γ_{LOAD} must always be smaller than $1/s_{22}$. Again, from equation (2.10) it can be noted that the condition $\Gamma_{LOAD} < 1/s_{22}$ is valid for any value of G smaller than infinite.

Conclusively, it can be said that this technique has been widely used at both low and high power levels due to its stability property.

c) Measurement System in the Envelope load-pull (ELP) configuration

A large number of measurements based on CW (continuous waves) stimuli have been taken in this thesis. These measurements were taken using an active load-pull measurement system based around the *envelope load-pull* (ELP) configuration which has been realized and in detailed explained somewhere else as well as in a subsequent Chapter [Appendix A].

The measurement system with the active load-pull configuration is shown in Fig. 2.8 and first presented by Tudor Williams [26].

The measurement system configuration using the ELP architecture is based on the Microwave Transition Analyzer (MTA) sampling scope demonstrated by Demmler et. al [29] and already presented briefly in section 2.2.2. The MTA 70820A from Hewlett Packard/Agilent is a dual channel sampling scope capable of measuring the absolute values of magnitude and phase of signals between DC and 40 GHz. The two signals of the 2-channel MTA are down converted using a local oscillator to an intermediate frequency (IF) between 10 MHz and 20 MHz [11],

after that the low frequency signals can be digitized using different techniques, for example by measuring the repetition of the signals or capturing non-repetitive single shot pulsed signals [30].

The input signal is provided by a Synthesised Sweeper (83640A), delivering power up to 25 dBm. Here a linear broadband power amplifier (PA) is necessary in order to have higher power delivered to the input of the DUT. As it can be seen, the input signal a1 is coupled using a broadband directional coupler where additional attenuators can be used in order to reduce the overall power sent to the MTA ports to less than the maximum safe power allowed (in the order of zero dBm). A test set of switches is used allowing the two channel MTA to operate as a four channel receiver measuring the overall incident and reflected travelling waveforms. Channel 1 is used to measure both the incident waves at the input a1 and output a2 of the DUT while channel 2 is used to measure the reflective waves b1 and b2 determined by the direction of the switches. The DC biasing of the device is achieved by using two bias tees, one at the input and one at the output of the DUT, with a current capability of 0.5 A at an RF bandwidth from 45 MHz to 40 GHz. For higher power (current) capability hybrid couplers can be used. Here the DC signal can still go through the bias tee joining then the RF signal which can go through the hybrid coupler. The fundamental and harmonic impedances can be achieved by using the ELP technique [31]. In this technique, the device transmitted signal b2 flows through the isolator (which isolates the transmitted wave b2 with the injected signal a2), after that the transmitted signal b2, which is rich in harmonic content is divided into the three harmonics F0, 2F0 and 3F0. The 3 signals can therefore flow into the ELP module. The single ELP module configuration is shown in more detail in Fig. 2.9.

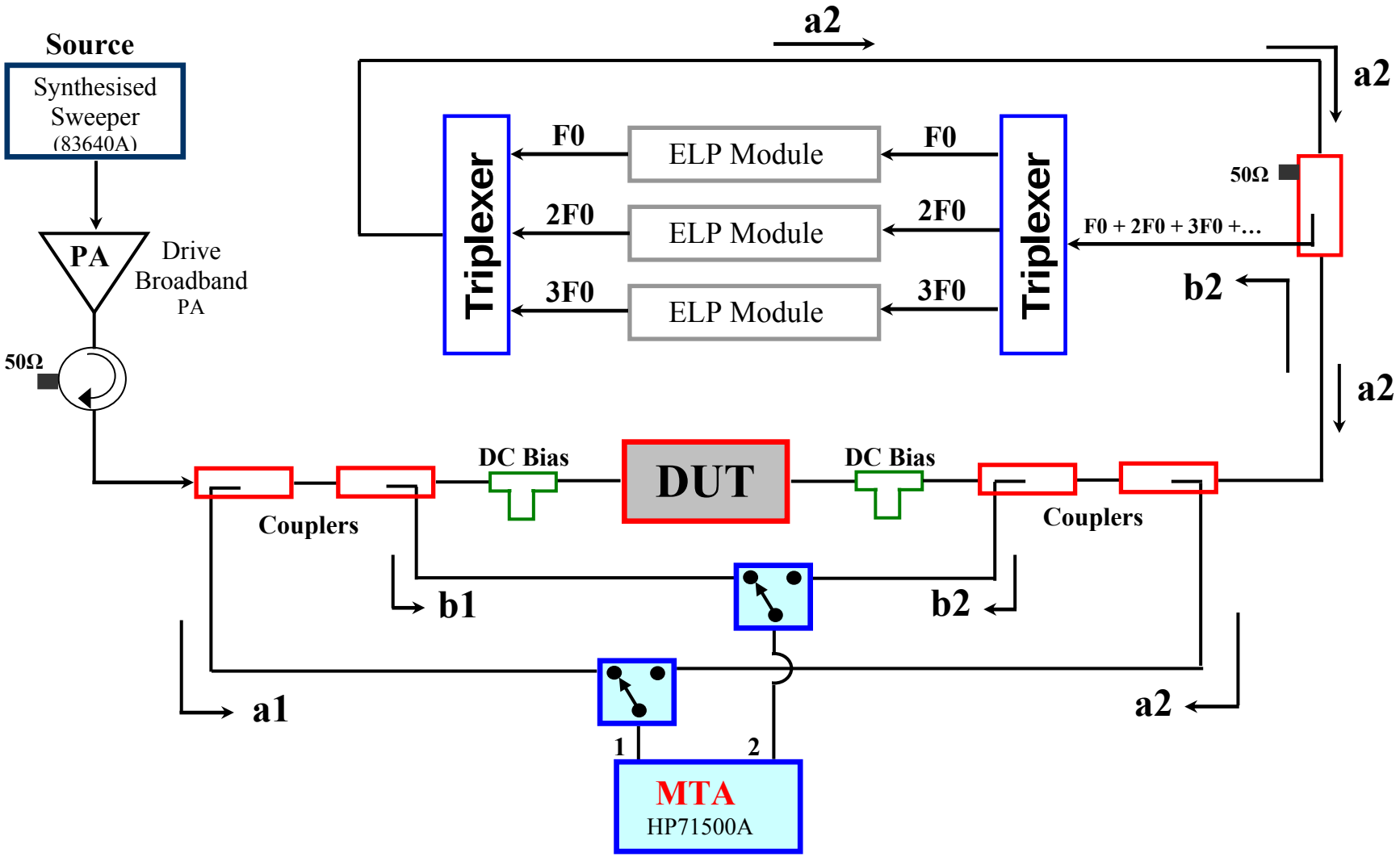

Fig. 2.8 - Cardiff University measurement system with active envelope load-pull (ELP) configuration.

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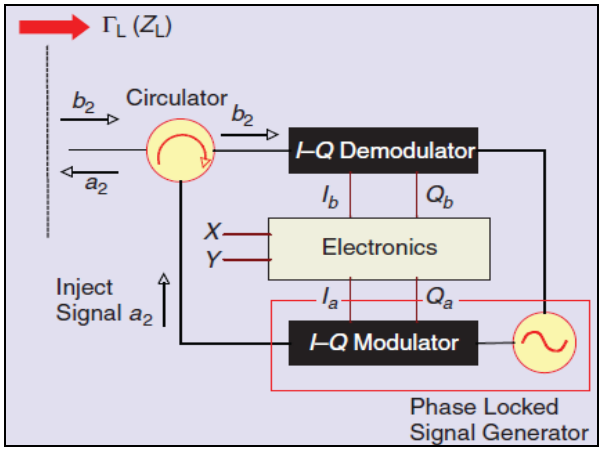

Fig. 2.9 – ELP Module architecture.

Here the signal is down converted to the baseband frequency using an I/Q demodulator. The down converted I_b and Q_b signals are then injected into an electronic control-unit box and by setting the correct values of the external variables X and Y the required signals I_a and Q_a are obtained by using a measurement software environment called Igor (available from WaveMetrics) developed at Cardiff University [32]. These signals can then be up converted to the RF frequency by a quadrature modulator, and the wave a2 will feed back into the output of the DUT. The emulated load reflection coefficient (Γ) is therefore given by the ratio of the reflected a2 and transmitted b2 waves, as shown in (2.11).

$$\Gamma(t) = a2/b2 = X(t) + jY(t) \tag{2.11}$$

The measurement system allows voltage and current waveforms to be measured at the external (package) device plane and then shifted to the device output generator plane $I_{GEN\text{-}PLANE}$ by de-embedding the parasitic components [33] again through an Igor software program developed at Cardiff University.

The full detailed analysis of the ELP measurement system can be found here [13, 26, 32].

2.4 Conventional Power Amplifier Modes of Operation

2.4.1 Concepts and Definitions

In this section a classification of the different power amplifier (PA) modes of operation will be detailed as well as several RF concepts and definitions mostly used in RFPA (Radio Frequency Power Amplifier) characterisation and designs [34-35].

Thanks to the continuous demand of advanced wireless communication technologies, the last decades have been focused on improving the overall PA performance in terms of efficiency, output power, gain and linearity. PAs represent an important element in wireless communication technologies. They are non-linear circuits with the aim of amplifying the given signal at a given frequency or for a narrow band of frequencies, typically around 5% or lower. However, it will be shown and demonstrated in the coming Chapters of this thesis that by manipulating the fundamental and higher harmonic impedances it is possible to maintain constant the output performance over larger bandwidths.

The main goal of PAs is to have a satisfactory trade-off between the output parameters previously mentioned. Low power efficiency degrades the overall performance which is translated in reduced life and increased size of the batteries for mobile phones, higher CO_2 environment emissions that impact global warming, as well as larger demand of space for cooling requirements in base stations with overall increased costs. High gain reduces the number of stages required to amplifier the overall signal, again minimizing manufacturing costs, while high linearity is required for the standard communication signal transmission and depends on the modulation requirements [36]. The design of power amplifiers can be divided into different amplifier classes/modes depending on their bias point and output matching network topology. The different modes rely on the use of waveform engineering. This means that each PA mode can be recognized from the proper voltage and current waveforms presented to the device output intrinsic plane. As a power transistor is ideally an input voltage controlled current source, the choice of the input bias voltage affects the output drain current waveform in terms of conduction angle. If the device is biased at half the maximum current

swing, a conduction angle of 360° is presented on the current waveform. If the bias point is lower than half the maximum swing but greater than zero the conduction angle is between 180° and 360° while in the case of bias point lower than zero the conduction angle is between 0° and 180°, as shown in Table 2.II and in the transfer characteristic of Fig. 2.10 where the drain current I_D is function of the gate bias voltage V_{GS}. A more detailed analysis will be presented in the next Sections of this Chapter when presenting in details each PA mode.

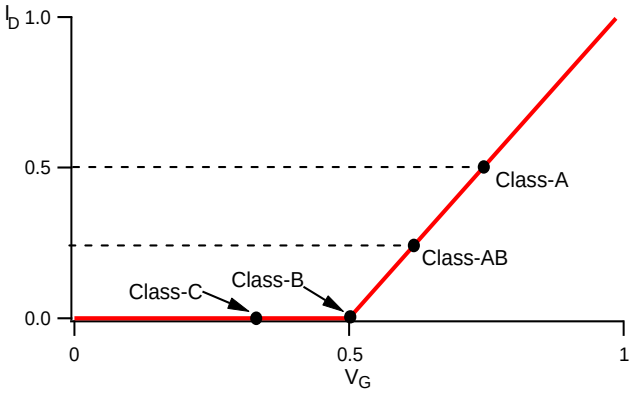

Fig. 2.10 – Transistor classes bias points considering a linear transfer characteristic.

Once the required drain current is achieved, by presenting the appropriate output circuit topology it is possible to present different fundamental and harmonic components in order to shape the voltage waveform. The shape of voltage and current waveforms define the overall output performance in terms of power, efficiency and gain as well as linearity. Efficiency and linearity are two conflicting parameters in PA designs; this means that the high linearity requirement is often accompanied in a reduction in power-efficiency and vice versa.

Table 2.II shows an overview of the different modes with the different output performance information. It can be noted that the Class-A [34-35] presented later in Section 2.4.3, is a linear mode as sinusoidal shapes are present on both voltage and current waveforms. Class-B, Class-AB and Class-C [34-36] can still present satisfactory linearity requirements, which depends on the bias point value. The more the bias point is decreased the more the linearity is degraded. In this case, the linearity performance is worse than the Class-A mode as higher harmonics are present on the current waveform. Class-D and Class-E are known as switched

modes as they behave as a switch [34, 37-38]. The Class-F and Inverse Class-F (Class-F^{-1}) are the high harmonically tuned (HT) modes [34, 35-38]. In the switched modes and harmonically tuned modes, very high drain efficiency (DE) can be reached at the expense of the overall linearity, which can however be regained through different enhancement linearization techniques [34, 39-43]. As already said, unfortunately linearity and efficiency are the inversely proportional, this means that high linearity leads to low efficiency and vice-versa. Therefore, depending on the application, PA designers need to trade-off in the best way these two parameters for a satisfactory overall performance.

TABLE 2.II
RFPA CLASSES PERFORMANCE

	RFPA Classes						
	Current Modes				**Switch Modes**		**HT**
Performance	**A**	**AB**	**B**	**C**	**D**	**E**	**F / F^{-1}**
Max DE (%)	50	50÷78.5	78.5	100	100	100	100
Linearity	Excellent	Good	Good	Bad	Bad	Bad	Bad
Gain (dB)	VeryHigh	High	Low	VeryLow	VeryLow	VeryLow	Low

2.4.1.1 Output Power and Efficiency

Before the different classes can be described, some parameters mostly used in RF characterisation and PA designs will be presented. As already mentioned in the previous section, two of the most important parameters used in PA designs are output power and efficiency. It is important to highlight that the high efficiency state is required at the same time as delivering the expected output power, which depends on the device size. Fig. 2.11 shows the PA schematic with the DC power component, the fundamental input power at the fundamental frequency ($P_{IN}(F0)$) and the output power components at both fundamental $P_{OUT}(F0)$ and higher frequency $P_{OUT}(F \neq F0)$.

The DC power is partly converted into useful RF output signal and partly into harmonic or spurious frequencies while the rest is dissipated inside the amplifier defined as P_{diss}. [38, 44]. This means that the overall power balance [44] is:

$$P_{DC} + P_{IN}(F0) = P_{OUT}(F0) + P_{OUT}(nF0) + P_{diss} \tag{2.12}$$

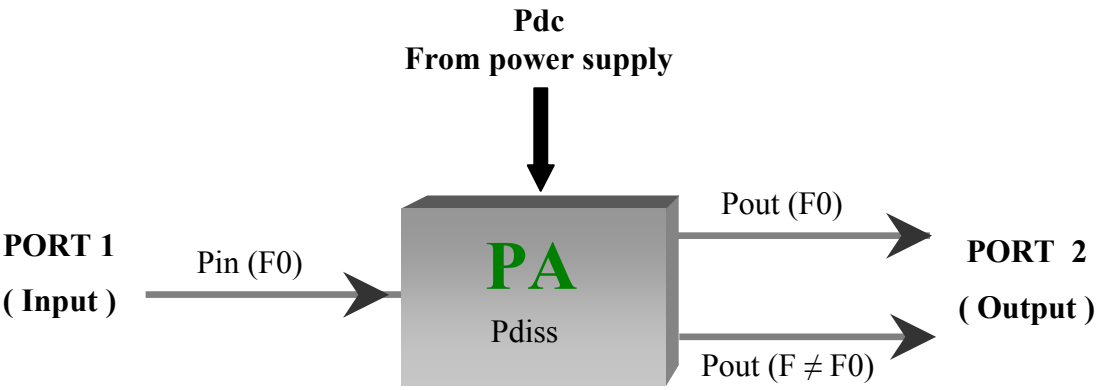

Fig. 2.11 – Power balance in PA.

The RF output power is half the product between the real part of the fundamental voltage component and the fundamental current component as shown in (2.13).

$$P_{OUT}(F0) = \frac{1}{2} \cdot \mathrm{Re}(V_1 \cdot I_1). \tag{2.13}$$

While the DC power can be calculated as:

$$P_{DC} = V_{DC} \cdot I_{DC}. \tag{2.14}$$

The quality factor of the DC power consumption is the efficiency. This is basically the quantity of DC power that is converted into useful RF output power. There are two common definitions for the efficiency: drain efficiency (η or DE) and power-added efficiency (PAE).

The drain efficiency is the ratio between the fundamental output power ($P_{OUT}(F0)$) and the DC power (P_{DC}):

$$\eta = \frac{P_{OUT}(F0)}{P_{DC}} \tag{2.15}$$

The PAE incorporates the input RF drive performance by subtracting it from the output power:

$$PAE = \frac{P_{OUT}(F0) - P_{IN}(F0)}{P_{DC}} \tag{2.16}$$

The PAE formulation is very important when considering devices with low gain, often due to the high fundamental frequency of operation. If the RF power gain is less than 10 dB, then the drive power requirements will start to make a serious impact on the overall efficiency, and the higher the efficiency is, the more significant the effect is [34]. It can be noted that if dealing with high gain devices, the input power does not affect substantially the overall efficiency, thus the input power can be ignored, leading to equation (2.15).

2.4.1.2 Gain

The gain (G) is the parameter that relates the input power with the output power. High gain reduces the number of stages required to amplify the overall signal thus minimising manufacturing costs. The main gain parameters used when considering a two-port network connected are: *power gain*, *available gain* and *transducer power gain* [2]. These three definitions of the gain can all be considered and applied when the device is in compression (as described later), called large signal gain, or when in back off (BO), called linear gain.

The *power gain (G)* is the ratio between the power dissipated in the load Z_L to the power delivered to the input of the two-port network (both expressed in watts).

$$G = \frac{P_L}{P_{in}} \tag{2.17}$$

The *available gain (G_A)* is the ratio of the power from the two-port network to the power available from the source. This assumes conjugate matching [34] of both the source and the load, and depends on Z_S but not Z_L.

$$G_A = \frac{P_{AVN}}{P_{AVS}} \tag{2.18}$$

The *transducer power gain (G_T)* is the ratio of the power delivered to the load to the power available from the source and depends from both Z_S and Z_L.

$$G_T = \frac{P_L}{P_{AVS}} \tag{2.19}$$

The main difference between these gain expressions is primarily due to the input and output matching condition. If input and output are both conjugately matched to

the source and load impedances then the gain is maximized and they are equal: $G=G_A=G_T$, otherwise they will be different.

2.4.1.3 Linearity Concepts

As mentioned in section 2.2.2, RF power transistors and RFPAs are non-linear devices where the non-linear effects significantly contribute to the overall distortion. The typical reason for the non-linear effects are mainly due to the harmonic distortion also called out-of-band distortion, and gain compression also called in-band distortion [45-46], as well as memory effects which will not be discussed in this thesis and are discussed elsewhere [47-49].

The out-of-band distortion is due to the presence of the higher frequency harmonics multiple of the fundamental one. The presence of the higher harmonics degrade the overall signal linearity, but as it will be shown and demonstrated in the next chapters, they allow the achievement of very high efficiency states.

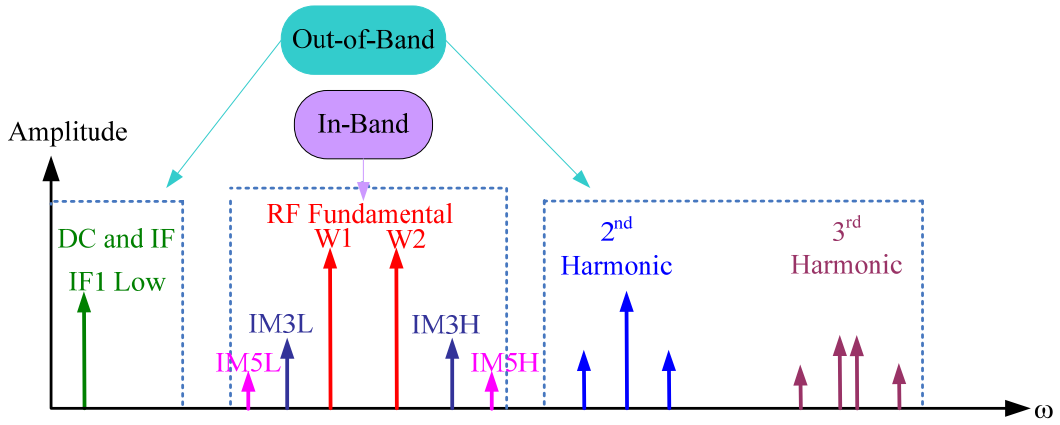

Fig. 2.12 – Spectrum of a two-tone signal.

The in-band distortion is mainly due to the device compression. The compression point of a power transistor can be found by plotting the output power vs the input power as shown in Fig. 2.13. In this case the simulation of a 10 W power transistor is presented [Appendix B].

As it can be noted, the device behaves linearly between 7 dBm and 17 dBm, where the gain is nearly constant around 22-23 dB. When the transistor reaches its maximum linear power, the output power increases with lower slope; this leads to a decrease in gain from its ideal constant value. Therefore, the decrease of gain from its constant linear value is referred to as gain compression. For example, the device will be in 3 dB of gain compression (usually written as P3 dB) when the gain is reduced by 3 dB from its linear value, in this case 20 dB where the saturated output power is around 40.5 dBm. The more the device is compressed, the more the third and fifth intermodulation distortion IMD3 and IMD5 (shown in Fig. 2.12) (as well as the higher intermodulation distorsion degree orders) products will be present, which degrades the overall linearity [34, 49].

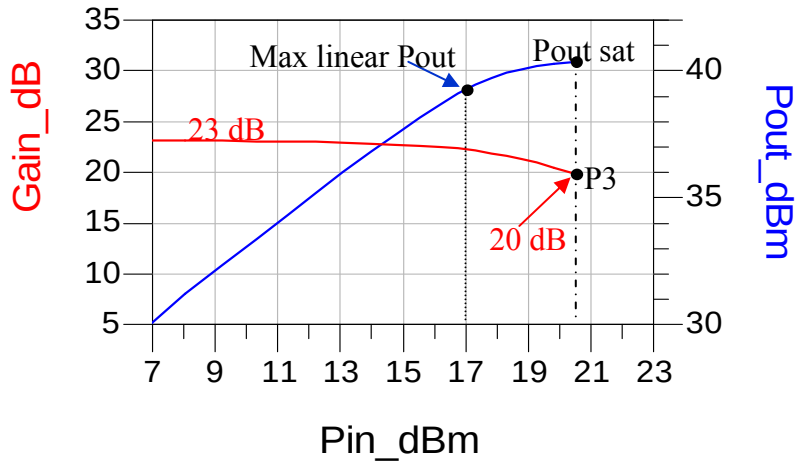

Fig. 2.13 – Gain and Pout vs Pin showing the P3dB of G compression.

2.4.2 Analytical Analysis of Conduction Angle for PA modes

Through the use of "*waveform engineering*" [50] and by knowing the different target voltage *v(θ)* and current *i(θ)* waveforms, it is possible to define the transistor operation modes. Therefore, by shaping drain voltage and current waveforms, mainly due to the bias condition, input voltage condition and the harmonic terminations, output power, gain, efficiency and linearity can be optimized.

The basic process of varying the conduction angle is shown in Fig. 2.14. Modeling the transistor as an input voltage controlled current source, by varying the input voltage, and with the appropriate bias component V_q, it possible to obtain the desired output drain current waveform. It can be noted that when the input

voltage V_g is greater than the pinch-off V_t the drain current is active and assumes the sinusoidal shape with its maximum normalized value up to I_{max}=1, when V_g goes below V_t the drain current goes to zero. The parameter α represents the portion of the RF cycle for which the current is above zero [34].

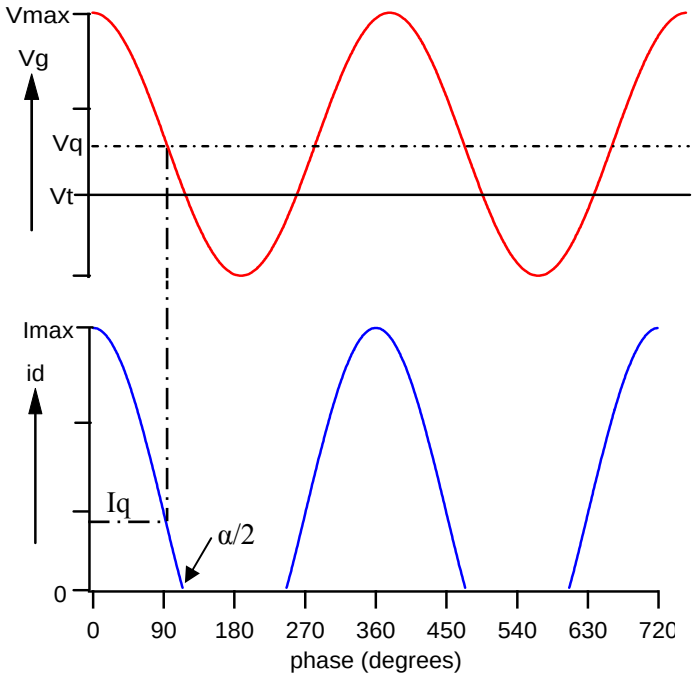

Fig. 2.14 – Input voltage and output current waveforms.

The drain current waveform can be analytically described as:

$$i_d(\vartheta) = I_q + I_{pk}\cdot\cos(\vartheta) \qquad -\alpha/2 < \vartheta < \alpha/2$$
$$= 0 \qquad -\pi < \vartheta < -\alpha/2\,;\ -\alpha/2 < \vartheta < \pi\,, \qquad (2.20)$$

where

$$\cos(\alpha/2) = -I_q / I_{pk}\,, \quad \text{and} \quad I_{pk} = I_{\max} - I_q\,. \qquad (2.21)$$

Therefore substituting (2.21) in (2.20) the drain current is

$$i_d(\vartheta) = \frac{I_{\max}}{1-\cos(\alpha/2)}\cdot(\cos\vartheta - \cos(\alpha/2))\,. \qquad (2.22)$$

The magnitude of the *n* harmonics is

$$I_n = \frac{1}{\pi}\cdot\int_{-\alpha/2}^{\alpha/2}\frac{I_{\max}}{1-\cos(\alpha/2)}\cdot(\cos\vartheta - \cos(\alpha/2))\cdot\cos n\vartheta d\vartheta\,, \qquad (2.23)$$

where n=0,1,2,3 etc, leads to the DC, fundamental, second, third, etc current components [34].

Table 2.III shows voltage and current quiescent values normalized to unity with the appropriate conduction angle for the classes: A, B, AB, and C, which will be presented in a detailed analysis in sections 2.4.3 and 2.4.4.

TABLE 2.III
PA CLASSES BIAS POINT AND CONDUCTION ANGLE

Mode	bias point (Vq)	quiescent current (Iq)	conduction angle
Class A	0.5	0.5	2π
Class AB	0 - 0.5	0 - 0.5	π - 2π
Class B	0	0	π
Class C	< 0	0	0 - π

2.4.3 Class-A Mode

Power amplifiers can be divided into two categories, one in which the device acts as a current source and the other one in which the device acts as a switch.

The Class-A is the simplest PA mode, it belongs to the first group and as mentioned in section 2.3.1 it is also known as the linear mode [34].

The quiescent current is ideally half the saturation current I_{DSS} (maximum current I_{max}); this means that the device is all the time in the active region with a conduction angle of 360°.

Only the fundamental component is presented in both voltage and current waveforms while the harmonic terminations are considered short-circuited. The fundamental contents are presented by using the circuit shown in Fig. 2.15 with in this case R_{F0} = 50 Ω. This leads to a sinusoidal shape in both waveforms as shown in Fig. 2.16 [34-38] which can also be derived from the voltage and current general formulations of (2.24) and (2.25) [38],

$$v(\vartheta) = V_{dc} - \sum_{n=1}^{\infty} \left(V_{nr} \cos n\vartheta - V_{ni} \sin n\vartheta \right), \tag{2.24}$$

$$i(\vartheta) = I_{dc} + \sum_{n=1}^{\infty} \left(I_{nr} \cos n\vartheta - I_{ni} \sin n\vartheta \right), \tag{2.25}$$

where $\theta=\omega t$ is the conduction angle and the coefficients V_{nr}, V_{ni}, I_{nr} *and* I_{ni} are the real and imaginary parts of the voltage and current components respectively, and n is the number of harmonics considered, where in this case n=1.

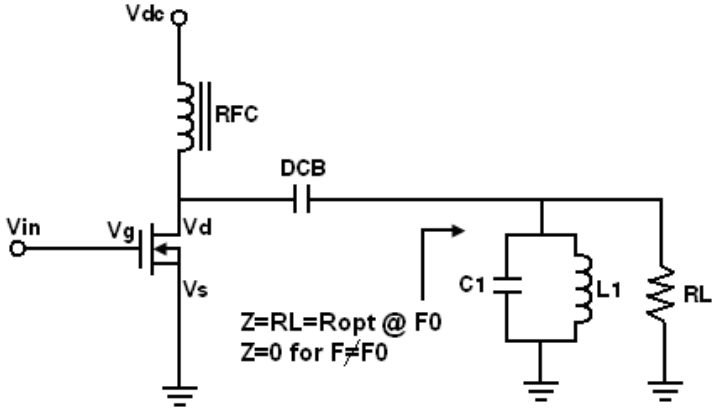

Fig. 2.15 – Class-A power amplifier schematic.

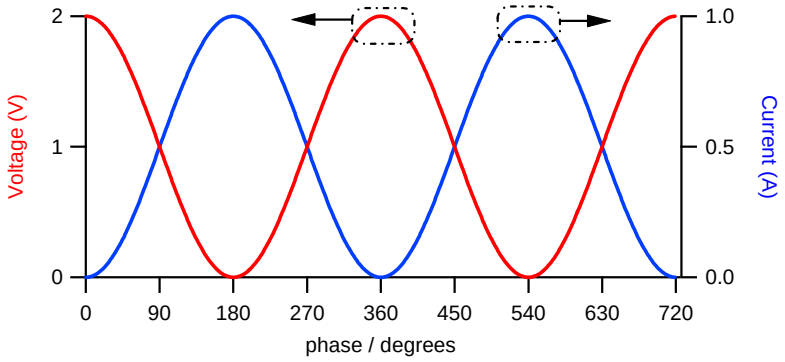

Fig. 2.16 – Class-A voltage and current waveforms.

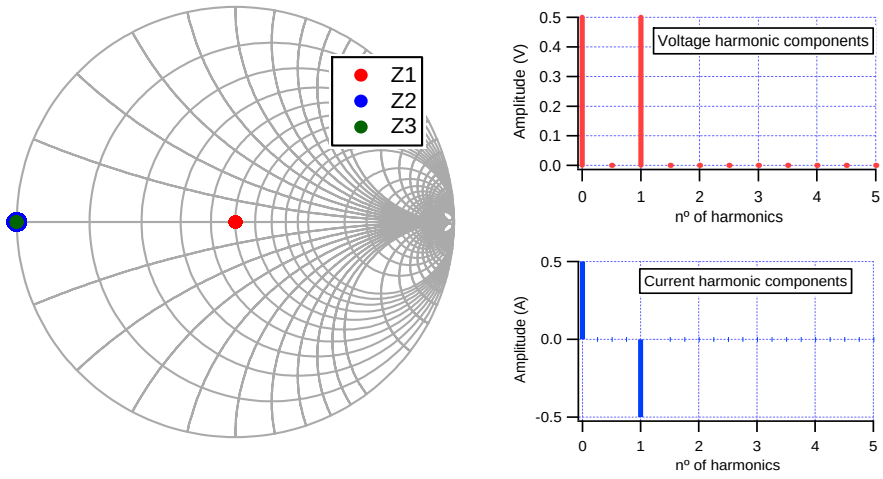

Fig. 2.17 – Class-A impedances and voltage and current spectral components.

As can be noted from the harmonic content of Fig. 2.17 fundamental voltage and current components are 180° phase shifted due to the negative current flowing into the load.

Fig. 2.18 shows a transistor's generalised DCIV characteristic with the Class-A load-line as well as current and voltage waveforms for which it is possible to understand and derive the output performance in terms of power and drain efficiency. V_{min} represents the knee voltage V_{knee} (or V_k) defined as the minimum value of the achievable RF drain voltage [34]. V_{max} is the maximum voltage while V_{dc} is the quiescent voltage. The same concept is applied to the current parameters I_{max}, I_{min} and I_{dc}, where I_{min} is assumed to be zero.

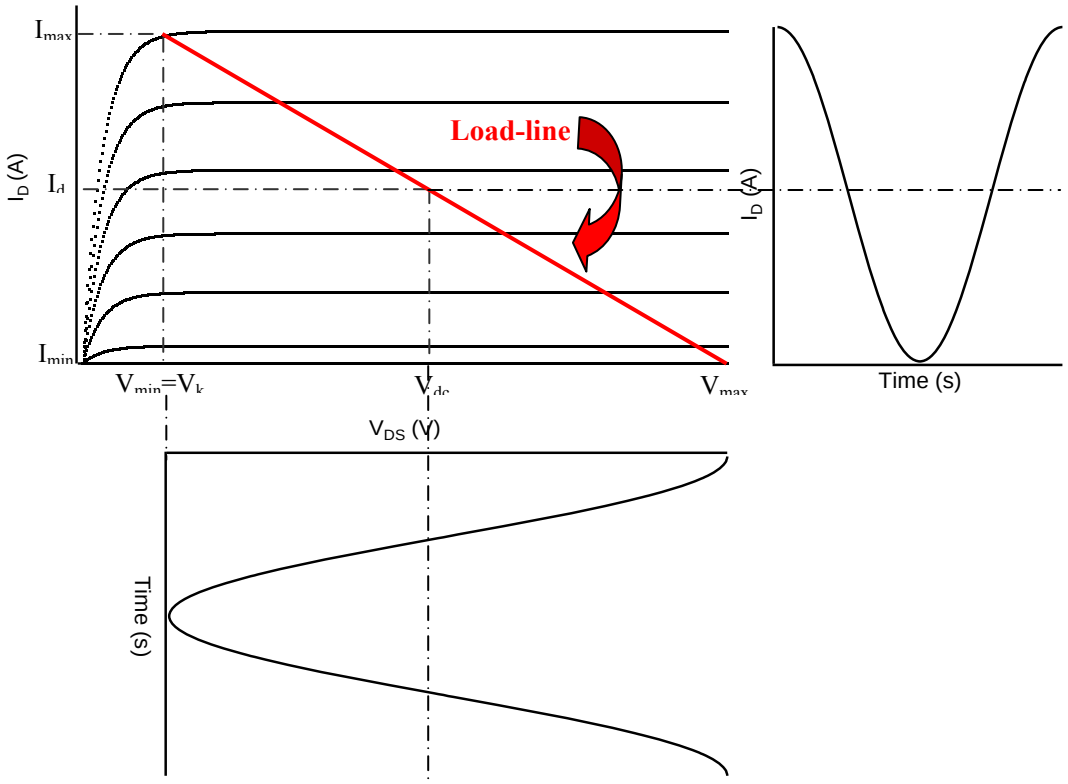

Fig. 2.18 – Class-A load-line and waveforms.

The RF output power is the product between the fundamental voltage and current components divided by 2:

$$P_{out} = \frac{V_1 \cdot I_1}{2} \tag{2.26}$$

Where:

$$V_1 = \frac{\Delta V}{2} = \frac{V_{\max} - V_{\min}}{2}, \tag{2.27}$$

$$I_1 = \frac{\Delta I}{2} = \frac{I_{\max} - I_{\min}}{2}. \tag{2.28}$$

Therefore:

$$P_{out} = \frac{\Delta V \cdot \Delta I}{8}. \tag{2.29}$$

Being the DC power:

$$P_{dc} = V_{dc} \cdot I_{dc}, \tag{2.30}$$

where:

$$V_{dc} = \frac{V_{\max} + V_{\min}}{2}, \tag{2.31}$$

$$I_{dc} = \frac{I_{\max} + I_{\min}}{2}, \tag{2.32}$$

therefore:

$$P_{dc} = \left(\frac{V_{\max} + V_{\min}}{2}\right) \cdot \left(\frac{I_{\max} + I_{\min}}{2}\right). \tag{2.33}$$

Being the drain efficiency:

$$\eta = \frac{P_{out}}{P_{dc}}, \tag{2.34}$$

in the ideal case where $V_{min} = I_{min} = 0$, the output power Pout will be equal to

$$P_{out} = \frac{V_{\max} \cdot I_{\max}}{8} \tag{2.35}$$

while the DC power P_{dc} is

$$P_{dc} = \frac{V_{\max} \cdot I_{\max}}{4} \tag{2.36}$$

leading to a drain efficiency of 50% as shown in (2.37):

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{V_{\max} \cdot I_{\max}}{8} \cdot \frac{4}{V_{\max} \cdot I_{\max}} = 0.5 \tag{2.37}$$

2.4.4 Class AB, B and C Modes

Just as in the Class A case, Classes AB, B and C model the transistor as a current source and can be represented by the same circuit topology of Fig. 2.15 [34-38, 51]. The main difference between these three classes is due to the different conduction angles explained analytically in paragraph 2.4.2 and shown in Table 2.III. However, in all the three classes the conduction angle is lower than 360° and depends on the bias voltage presented.

For the ***Class-B*** mode the gate-bias voltage is theoretically set at the device pinch-off where the conduction angle is θ=180°. This means that the device will be for half of the time in the active region and the other half of the time will be OFF leading to an ideal half-wave rectified sinusoidal current waveform with 50% duty cycle and a sinusoidal voltage waveform as shown in Fig. 2.19 and 2.21. The harmonic impedances greater than the fundamental one will all be short-circuited (Fig. 2.20) leading to the sinusoidal voltage waveform. It can be seen on the current and voltage spectra that while the voltage waveform has only the DC and fundamental components present, the current waveform introduces higher harmonic contents due to its truncated shape. The fundamental current component will be 180° phase shifted with the voltage fundamental component due to the current flowing towards the load (I_D=-gm·V_{GS}).

The truncated shape on the bottom part of the current waveform reduces the overlap between the voltage and current waveforms resulting in decrease of DC power, leading to an increase in efficiency.

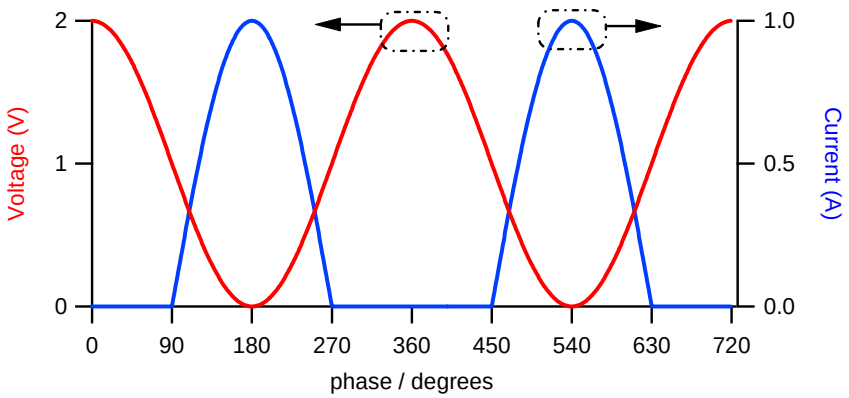

Fig. 2.19 – Class-B voltage and current waveforms

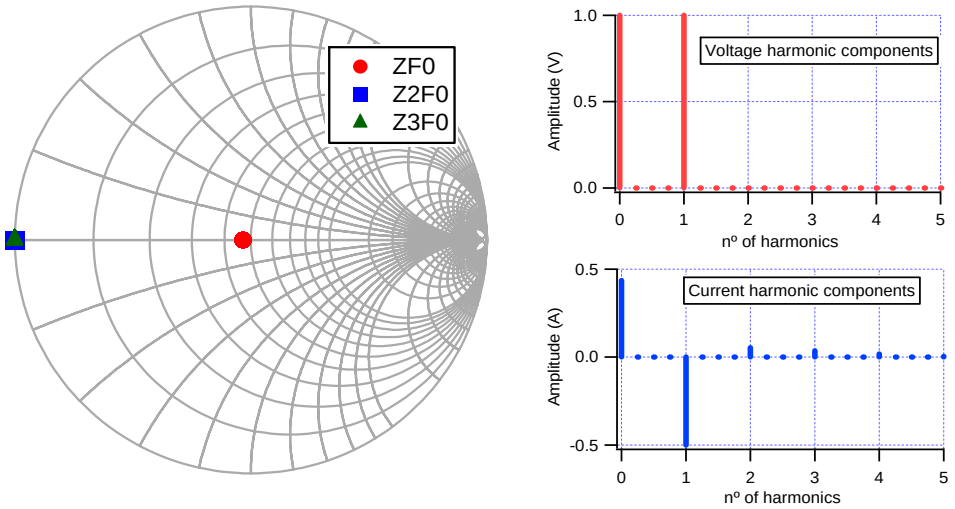

Fig. 2.20 – Class-B impedances and voltage and current spectral components.

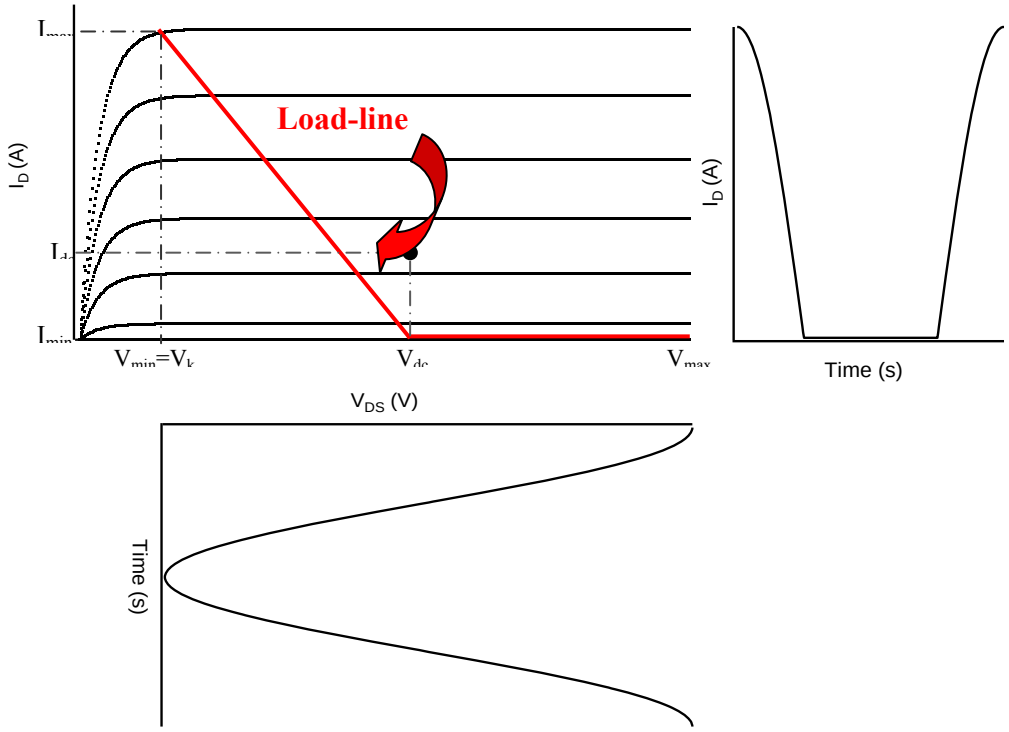

Fig. 2.21 – Class-B load-line and waveforms.

In the load-line of Fig. 2.21, it can be noted the current will be active when the drain voltage V_{ds} is $V_{min} < V_{ds} < V_{dc}$ while it will be zero in the range $V_{dc} < V_{ds} < V_{max}$. By applying the same concepts and formulations from (2.24) to (2.37) the Class-B output power and drain efficiency can be obtained, where in this case the DC current is

$$I_{dc} = \frac{\Delta I}{\pi} + I_{\min} = \frac{I_{\max} - I_{\min}}{\pi} + I_{\min} . \qquad (2.38)$$

Therefore, by biasing the device at its pinch-off, the DC supply is reduced by a factor of 2/π compared with the Class-A condition resulting in an increase of efficiency of π/4, better known as 78.5%.

An important parameter to introduce is the power utilization factor (PUF) [34] which is defined as the ratio between the RF power delivered by a particular mode under consideration to the power delivered from the Class-A mode. Here, a PUF=1 can be reached with the higher efficiency (78.5%) accompanied in a reduction of 6 dB in gain, as higher drive power is needed in order to reach the maximum voltage swing.

For the ***Class-AB*** mode the gate-bias voltage is theoretically set between the pinch-off and half the maximum current, which leads to a conduction angle between $180° < \theta < 360°$. This leads to a wave rectified sinusoidal current waveform with duty cycle between 50% and 100%, thus the device will be in the active region for more than half the time.

In this Class-AB condition, a PUF ≥ 1 can be achieved with efficiencies greater than 50% but lower than 78.5%, again accompanied by a reduction in gain. The increase in efficiency with the respective decrease in gain depends on the conduction angle presented between 180° and 360°.

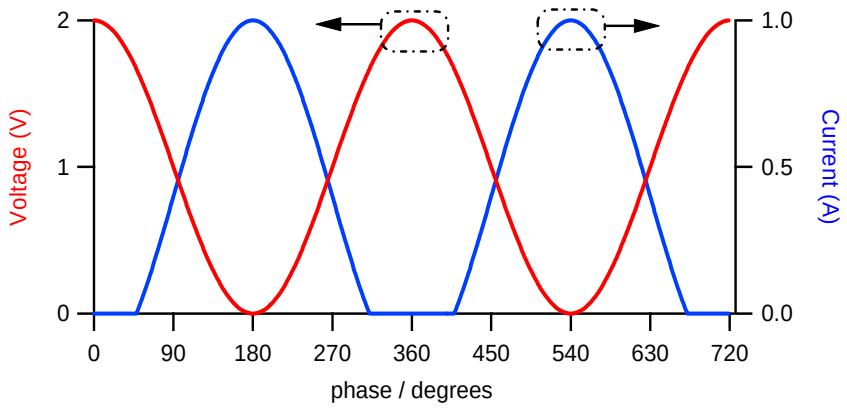

Fig. 2.22 – Class-AB voltage and current waveforms.

Fig. 2.22 shows the Class-AB voltage and current waveforms, also shown in Fig. 2.23 with the load-line. Such load-line shows clearly that for a certain voltage value $V_{DS} > V_{AB}$ the current is equal to zero ($360° < \theta < 180°$) for which a smaller overlap between current and voltage would lead to an increase in efficiency when compared with the Class-A case.

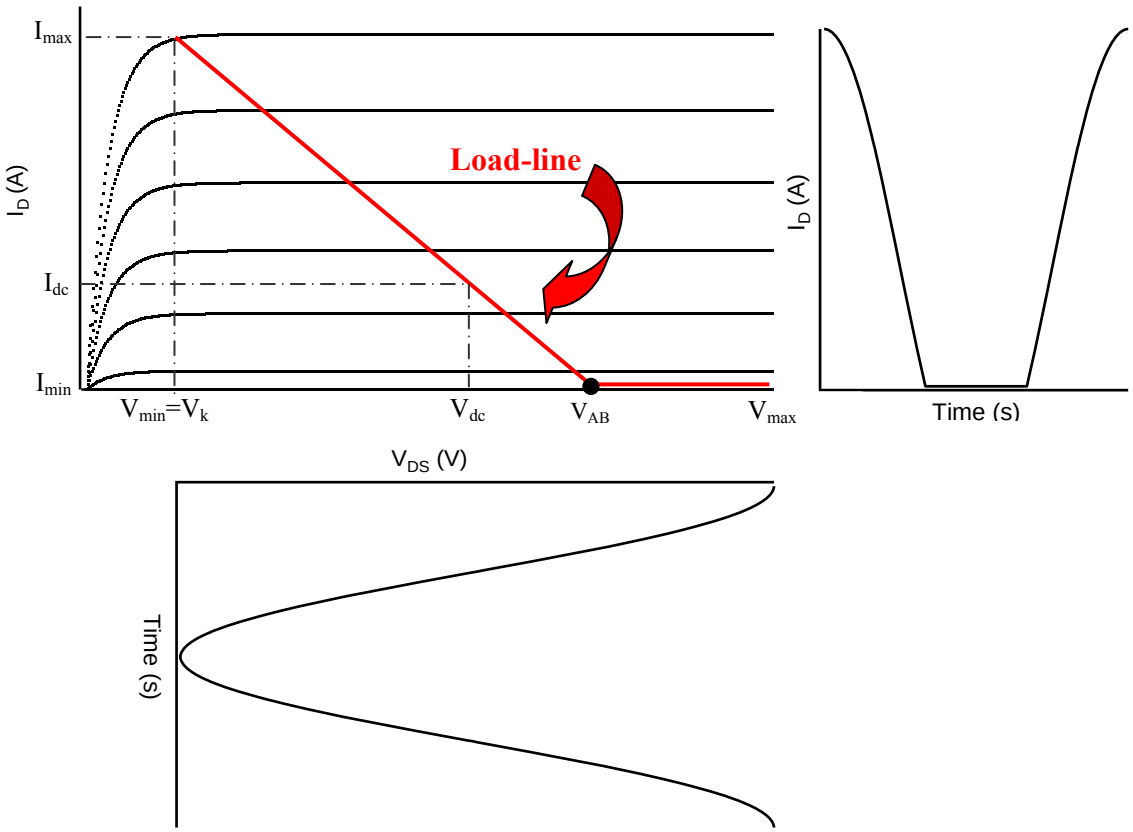

Fig. 2.23 – Class-AB load-line and waveforms.

In the ***Class-C*** mode the gate-bias voltage is set below the pinch-off voltage $V_{GS}<V_{TH}$, so the transistor is active for less than half of the RF cycle, which means that the current waveform will have a conduction angle between 0 and 180° while presenting a sinusoidal voltage waveform shown in Fig. 2.24.

Here the drain efficiency ideally reaches 100% by decreasing the conduction angle towards zero. Unfortunately the linearity decreases, and the output power decreases towards zero with drive power increasing towards infinity. A typical trade-off is a conduction angle of 150° with an efficiency of 85%.

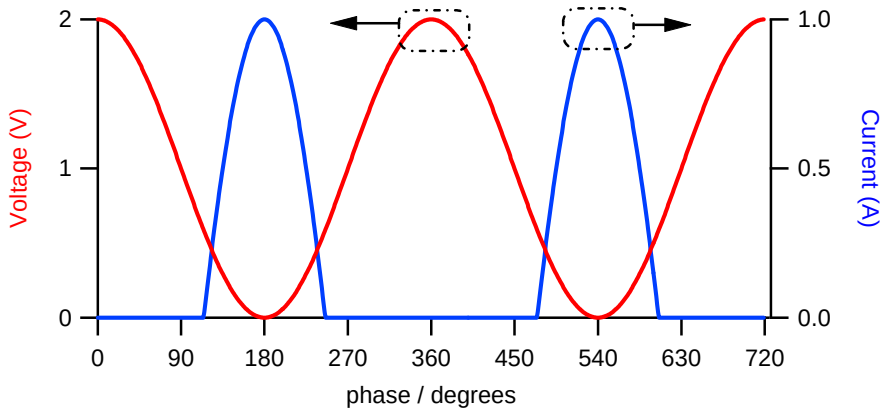

Fig. 2.24 – Class-C voltage and current waveforms.

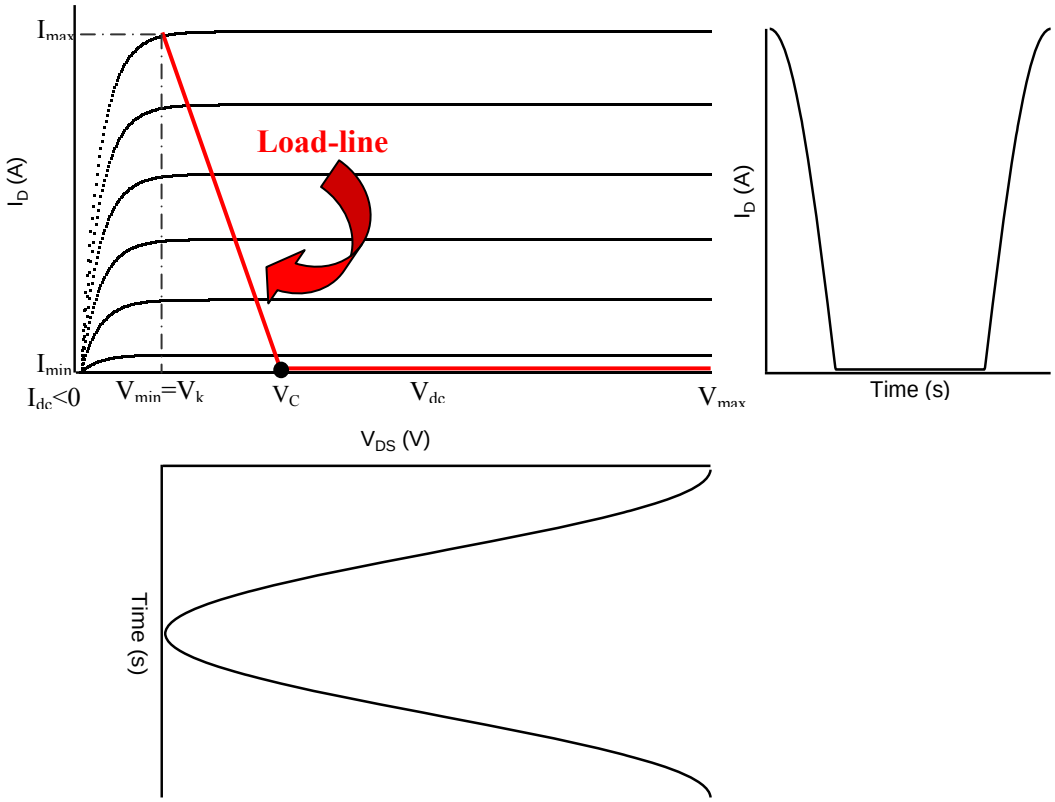

Fig. 2.25 – Class-C load-line and waveforms.

2.4.5 Class-D Mode

The Class-D is defined as a switch mode since the device is meant to act as a switch [34, 37, 51]. Fig. 2.26 shows a schematic implementation of the Class-D using an LCR branch while Fig. 2.27 shows the voltage and current waveforms resulting from that circuit.

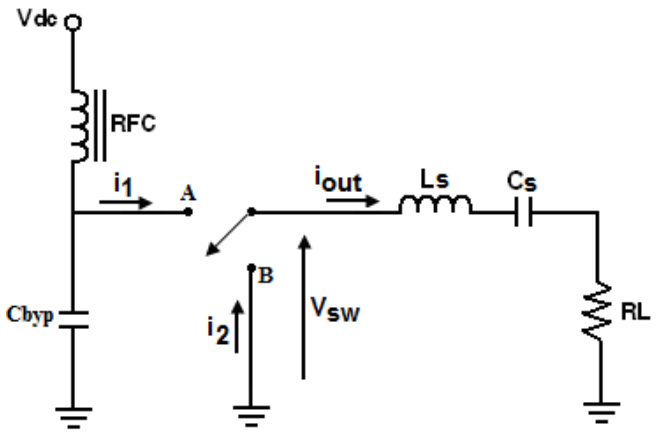

Fig. 2.26 – Class-D power amplifier schematic.

It can be seen that when the switch A is ON the output current i_{out} will be equal to the current i_1 which flows towards the load conducting a positive sinewave while the current i_2 is equal to zero. Vice-versa, when the switch A is OFF and the switch B is ON the current i_1 will be equal to zero and the output current will be i_{out}=- i_2 leading to a negative half sine wave [34].

Therefore, supposing a duty cycle of 50% as shown in Fig. 2.27, where for half of the time the switch is ON and half of the time is OFF, the maximum current I_{pk} will be:

$$I_{pk} = I_{dc} \cdot \pi \,. \tag{2.39}$$

The fundamental current I_1 flowing towards the branch LCR is

$$I_1 = \frac{I_{pk}}{2} \,, \tag{2.40}$$

and the fundamental voltage across the LRC branch is

$$V_1 = V_{dc} \cdot \frac{4}{\pi} \,. \tag{2.41}$$

Being the RF output power the product between the fundamental voltage and the current components:

$$P_1 = \frac{V_1 \cdot I_1}{2} = \frac{1}{2} \cdot \frac{V_{dc} \cdot 4}{\pi} \cdot \frac{I_{pk}}{2} = \frac{V_{dc} \cdot I_{dc}}{\pi} \,, \tag{2.42}$$

and being the DC power

$$P_{DC} = V_{dc} \cdot I_{dc} = \frac{V_{dc} \cdot I_{pk}}{\pi} \,, \tag{2.43}$$

the overall efficiency is

$$\eta = \frac{P_1}{P_{dc}} = 100\,\% \,. \tag{2.44}$$

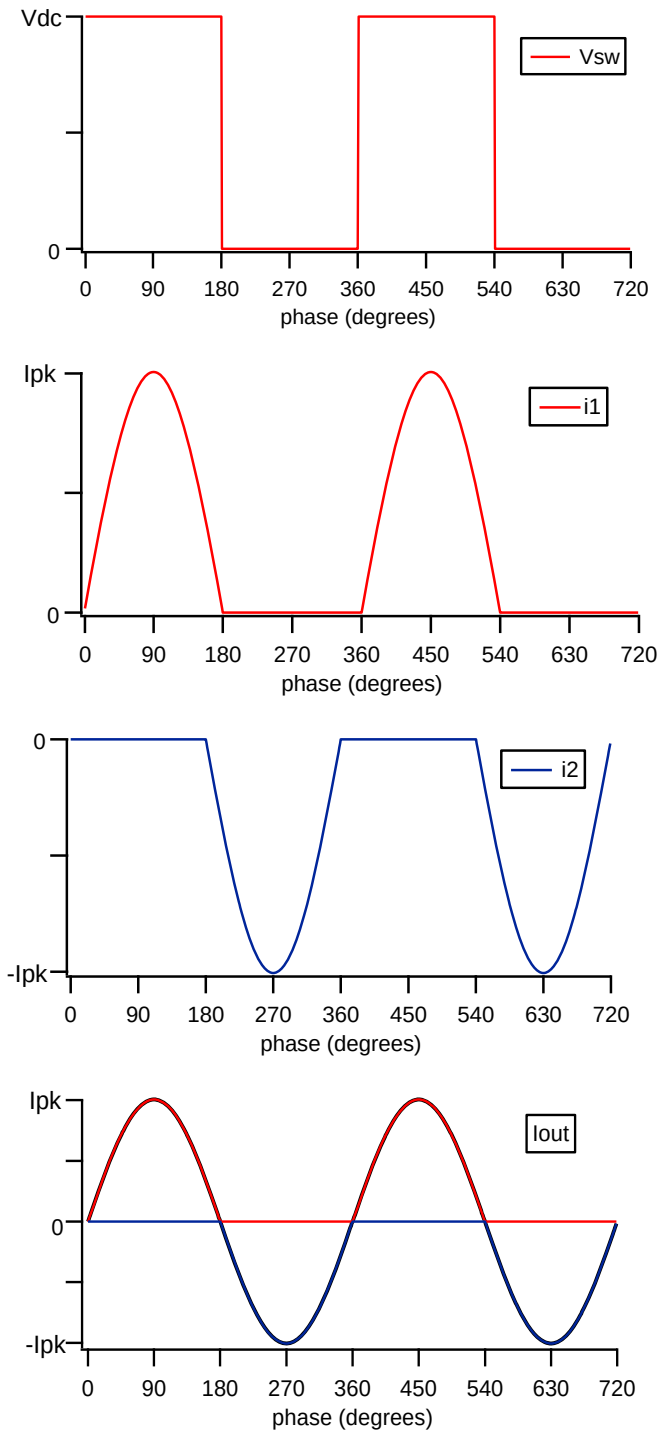

Fig. 2.27 – Class-D switching waveforms.

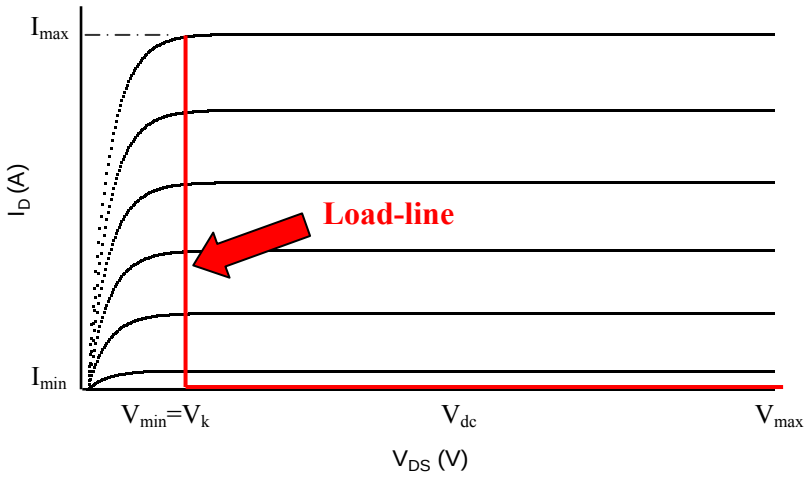

Fig. 2.28 – Class-D load-line.

Assuming an ideal transistor, where switching time is zero and there is no on-state resistance or voltage drop across the active device, an ideal square voltage waveform can be achieved, shown in Fig. 2.27, with 100% efficiency as no power is dissipated as heat in the transistor. Note from the load-line of Fig. 2.28 that the device behaves as a perfect switch.

However, a finite transition time will occur in practical implementations resulting in the overlap of non-zero output voltage and current which significantly degrades the efficiency [52]. Different analysis can be presented in order to present more realistic class-D switching behaviour, as shown elsewhere [37].

This problem can be partially solved by using the Class-E approach as shown in section 2.4.6, where the idea of soft switching can minimise the issues presented in the Class-D.

2.4.6 Class-E Mode

As with Class-D, the Class-E mode is a switch mode PA and the waveforms can be achieved with a slower switching characteristic, from here on termed 'soft switching'.

In this section the main concept of the Class-E mode will be presented, without detailed mathematical analysis, which can be found elsewhere [34-38, 53-55].

Fig. 2.29 shows the basic schematic implementation of a Class-E PA. The series LC is tuned to the fundamental frequency which means that the only fundamental component will flow towards R_{LOAD} while the higher harmonics will be open-circuited.

The overall current that flows into the switch-capacitor combination is

$$i(\vartheta) = I_{rf} \cdot \cos(\vartheta) + I_{dc} \tag{2.45}$$

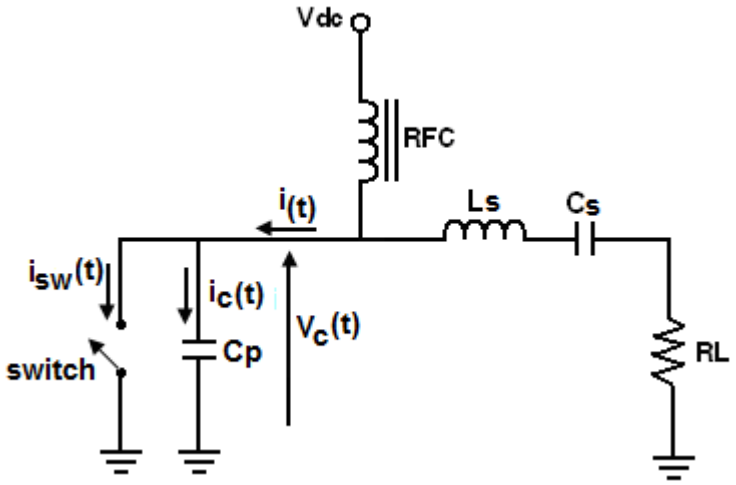

Fig. 2.29 – Class-E power amplifier schematic.

It is clear that when the device is switched ON, for example from 0 to $\alpha 1$ (Fig. 2.30), where $\alpha 1$ is an arbitrary angle value, the overall current *i(θ)* will flow into the device. When the device is OFF the overall current *i(θ)* will flow into the capacitor. As should be noted, the key concept of this Class-E mode is that when the switch passes from ON to OFF the current will instantaneously flow into the capacitor with no power dissipation, but during its turn-on mode (from OFF to ON) any charge stored into the parasitic capacitor Cp will be discharged through the device with a slow rise time, resulting in a power loss. In order to avoid this, the Class-E PA should be designed such that the voltage across the switch reaches zero at exactly the turn-on instant. This condition is called zero-voltage switching (ZVS) [59]. Besides, as can be seen from Fig. 2.30 (c), the voltage Vc reaches the zero value exactly when the switch starts to conduct current. In this case there is no overlap between voltage and current resulting in an ideal 100% efficiency.

An important observation is that Class-E is a non-linear mode and suffers in terms of PUF (which must be traded-off with gain) and peak voltages, which can however be marginal since new wide bandgap technologies such as GaN (gallium nitride) [56-57] allow very high peak values to be reached thanks to the high breakdown voltage characteristic.

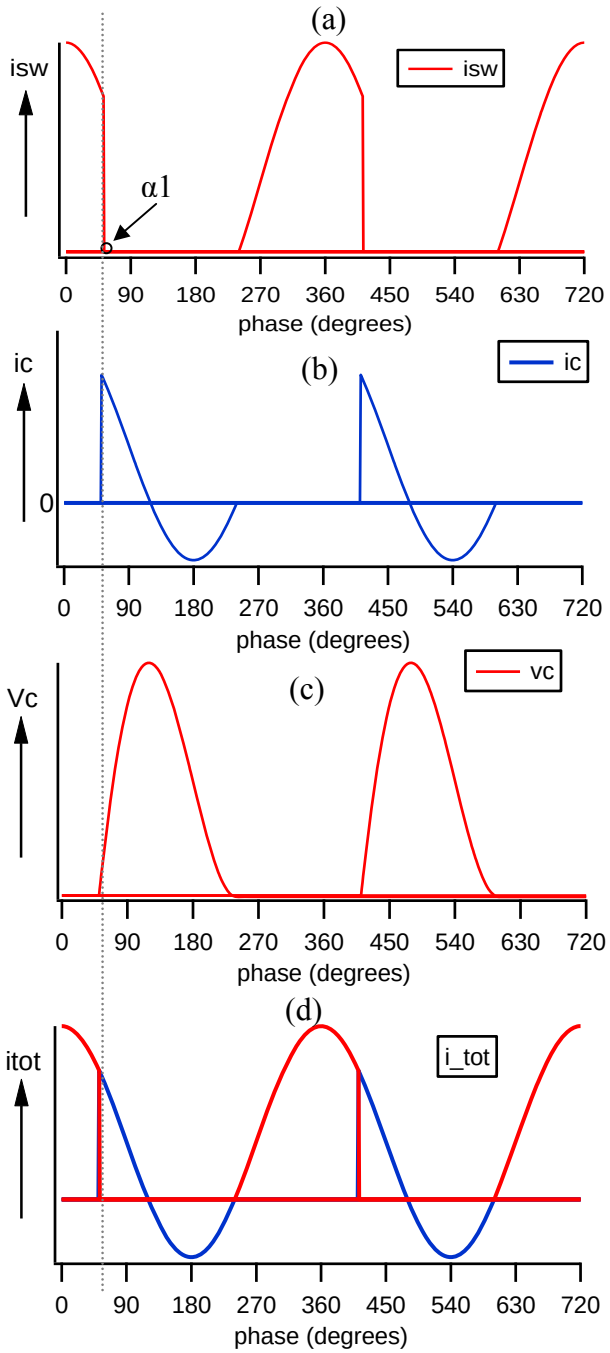

Fig. 2.30 – Class-E voltage and current waveforms: (a) switch current, (b) shunt capacitor current, (c) shunt capacitor voltage and (d) total current.

However, even if the ideal efficiency of 100% can theoretically be achieved, in practical implementations the switch has a finite on-state resistance and the turn-off switching still suffers from finite transition time [58-60]. At low frequency, in the order of hundreds of MHz, this mode can certainly have benefits [34]. But at GHz frequencies, as mentioned, there is this central issue that the RF power transistor cannot realistically be modelled as a simple switching element as it will not switch fast enough to avoid the linear region resulting in power dissipation and efficiency reduction.

However, it is important to highlight that in the last years thanks to the new and improved device technologies mentioned earlier, the Class-E mode has been used for the realisation of high efficiency power amplifiers at high frequency resulting in interesting output performance results [62].

2.4.7 Class-F Mode

In the linear modes presented in section 2.4.3 and 2.4.4, the efficiency states have been achieved by presenting the appropriate bias condition and optimum fundamental impedance whilst short-circuiting all the higher harmonics. The Class-F mode is obtained by using harmonic resonators in the output network, as shown in Fig. 2.31, in order to shape the voltage waveform through appropriate choice of harmonic content [34-38, 63-68]. The current waveform is a half wave rectified sinusoid achieved by biasing the device at its pinch-off. The voltage waveform is presented with an optimum fundamental impedance, short-circuit even harmonic and open-circuit odd harmonic loads at the intrinsic $I_{GEN\text{-}PLANE}$, as shown in the schematic. The branch L1C1 is tuned to the fundamental frequency (F0), which means that at frequency F0 it behaves as an open-circuit while the branch LnCn, where n=3,5,7…etc, behaves as a short-circuit. Therefore, at the transistor plane, optimum impedance Z_{LOAD} (with imaginary part equal to zero) will be presented. At even harmonic frequencies, the branch LnCn will be short circuited as well as L1C1 leading to short-circuit even harmonic impedances. At odd frequencies, the network LnCn behaviours as an open-circuit (as it is tuned to odd frequencies) leading to open-circuited odd harmonic impedances.

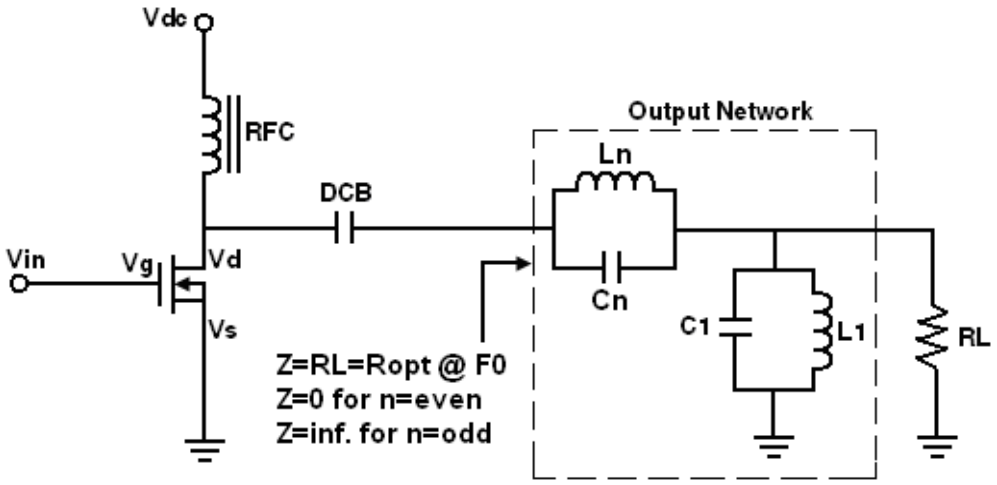

Fig. 2.31 – Class-F PA schematic.

The benefit of the Class-F condition is the possibility to increase the fundamental voltage component due to the introduction of third harmonic voltage content (when considering first three harmonic contents as they are usually sufficient to exploit the transistor´s optimum performance) while maintaining the condition that the voltage never reaches zero during the RF cycle. Equations (2.46) and (2.47) describe the general representation of the current and voltage waveforms:

$$\begin{aligned} i_d(\vartheta) &= I_{pk} \cdot \cos(\vartheta) \quad -\pi/2 < \vartheta < \pi/2 \\ &= 0 \qquad -\pi < \vartheta < -\pi/2\,; \quad \pi/2 < \vartheta < \pi\,, \end{aligned} \tag{2.46}$$

where I_{pk} is the peak voltage and θ is the conduction angle.

$$v(\vartheta) = V_{dc} - \sum_{n=1}^{\infty} \left(V_{nr} \cos n\vartheta - V_{ni} \sin n\vartheta\right), \tag{2.47}$$

where V_{dc} is the DC voltage, V_{nr} and V_{ni} are real and imaginary parts of the voltage components where n is the number of harmonic components.

In this case, taking into account infinite harmonic content in both the voltage and current waveforms, the ideal half-wave rectified sinusoidal current waveform and the perfect square voltage waveform are achieved as shown in Fig. 2.32 leading to the ideal 100% drain efficiency.

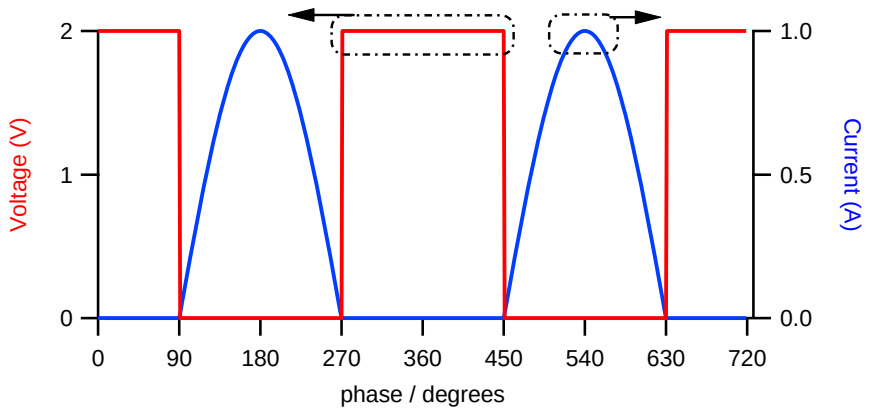

Fig. 2.32 – Class-F voltage and current waveforms when considering for both waveforms infinite harmonic content.

When reducing the number of utilized voltage harmonics to three, the generalised case of (2.47) can be expressed as

$$v(\vartheta) = V_{dc} - V_1 \cos(\vartheta) - V_2 \cos(2\vartheta) - V_3 \cos(3\vartheta)\,. \tag{2.48}$$

Here the maximum drain efficiency is reduced to 90.7% with the waveforms shown in Fig. 2.33. As shown in the spectral contents of Fig. 2.34, DC, fundamental and third harmonic components are presented in the voltage waveform while DC, fundamental and all the higher even harmonic contents are presented in the current waveform.

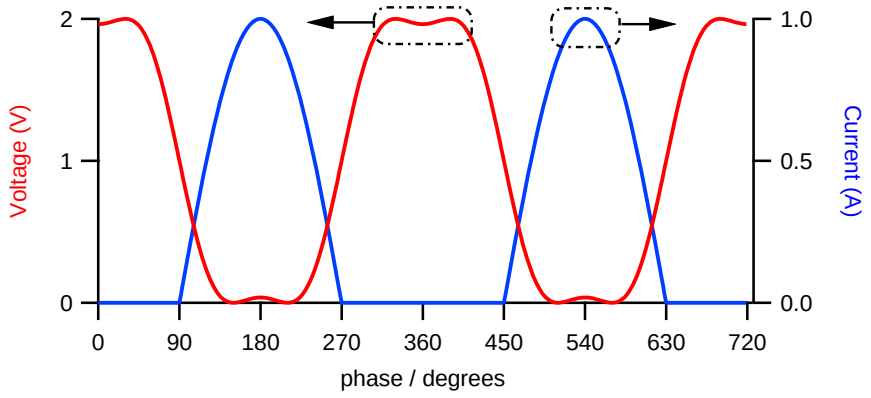

Fig. 2.33 – Class-F voltage and current waveforms when considering infinite harmonic contents in the current waveform and three harmonic contents in the voltage waveforms.

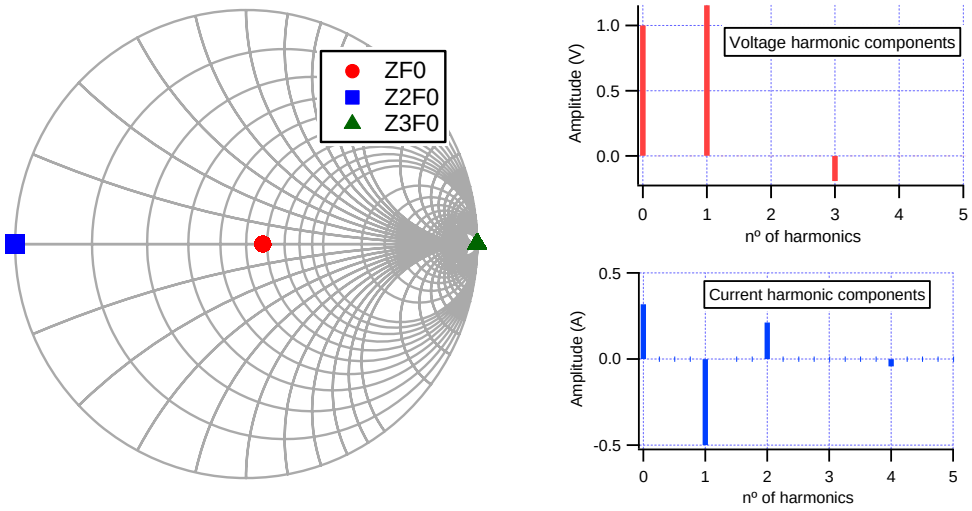

Fig. 2.34 – Class-F impedances and voltage and current spectral components.

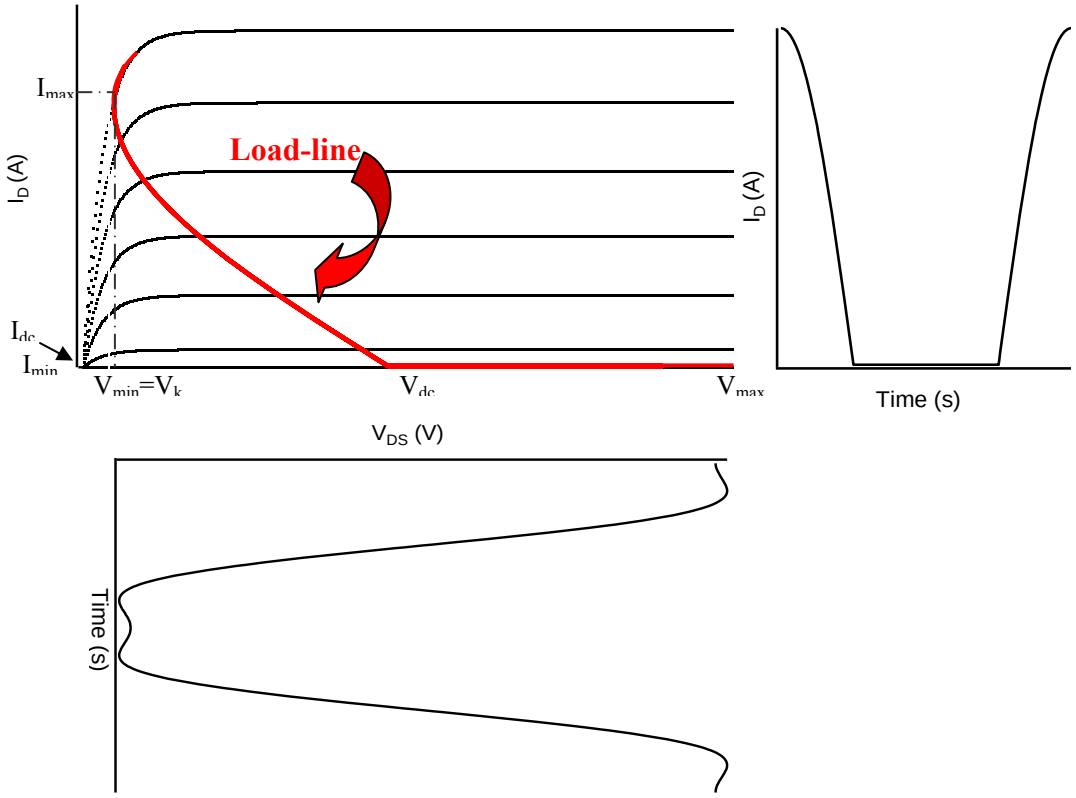

Fig. 2.35 – Class-F load-line and waveforms.

Tables 2.IV and 2.V show the voltage and current component values (normalised to unity DC component) [34, 64] as a function of the utilised number of harmonics in order to maximise the drain efficiency, shown in Table 2.VI. When accounting for only the fundamental component, the Class-B condition is revealed

to have drain efficiency of 78.5%. When introducing the third harmonic voltage content with value of $1/3\sqrt{3}$ (approx. 0.1925) the voltage waveform squares-up but a smaller swing is presented. Therefore, increasing the fundamental voltage by V_1=0.1925*6, the voltage waveform reaches its maximum value with the benefit of the higher efficiency of 90.7%.

The improvement in power efficiency is obviously accompanied with degradation in linearity due to the introduction of the higher harmonics. However, this linearity requirement can effectively be traded off with power and efficiency. Besides, it can be satisfied by utilising standard or advanced linearization techniques [39-43].

TABLE 2.IV
CLASS-F OPTIMUM VOLTAGE VALUES AS A FUNCTION OF UTILIZED HARMONICS

	Class-F Voltage Harmonic Values		
M	**Using 1 harmonic**	**Using 2 harmonics**	**Using 3 harmonics**
V1	1	1.155	1.207
V3	0	0.1925	0.28
V5	0	0	0.073

TABLE 2.V
CLASS-F OPTIMUM CURRENT VALUES AS A FUNCTION OF UTILIZED HARMONICS

	Class-F Current Harmonic Values		
N	**Using 1 harmonic**	**Using 2 harmonics**	**Using 3 harmonics**
I1	1	1.41	1.5
I2	0	0.5	0.5835
I4	0	0	0.0834

TABLE 2.VI
CLASS-F OPTIMUM DRAIN EFFICIENCY AS A FUNCTION OF UTILIZED HARMONICS

	Class-F Efficiency (%)			
N	**M=1**	**M=3**	**M=5**	**M=∞**
1	50	57.7	60.35	63.66
2	70.71	81.6	85.35	90.03
4	75	86.54	90.52	95.48
∞	78.54	90.63	94.8	100

Where: M = number of voltage components
N = number of current components

2.4.8 Inverse Class-F Mode (Class-F^{-1})

The inverse Class-F mode is similar to the Class-F mode, where by presenting the appropriate output network, as shown in Fig. 2.31 (similar to Class-F), the Class-F mode inverted waveforms can be revealed [35-37].

Here, differently from the Class-F case, the even harmonics are open-circuited as the resonator LnCn with n=2,4,6…etc is presented. At the fundamental frequency, the resonator will behave as a low impedance (ideally short-circuit) as well as the branch L1C1 and, as the Class-F mode, the optimum fundamental impedance can be presented by choosing $R_{LOAD}=R_{opt}$ (at the $I_{GEN-PLANE}$). At the odd frequencies both resonators LnCn and L1C1 behave ideally as low impedance resulting in short-circuit odd harmonic impedances [68-72].

When presenting infinite harmonic contents in both voltage and current waveforms the ideal half-wave rectified with second harmonic peaking $V_{max}=\pi \cdot Vdc$ voltage waveform and the perfect square current waveform are presented resulting in efficiency of η=100%. The input bias voltage condition of this mode is half the maximum current (as for the Class-A mode), where by hitting the boundaries, odd components are generated allowing the waveform to become squared.

Few research works have shown that the half-wave rectified waveform can be achieved by starting from the pinch-off bias voltage as shown here [73]. In this case only the top part of the waveform needs to be squared, but higher input power are required resulting in a decrease of gain.

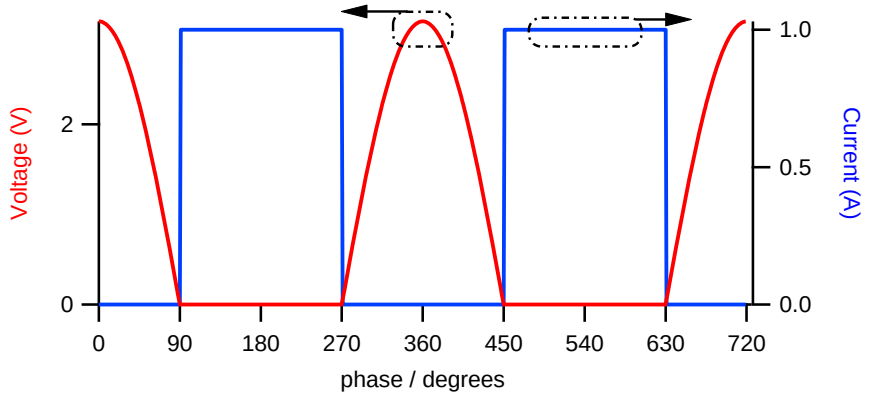

Fig. 2.36 – Class-F^{-1} voltage and current waveforms when considering for both waveforms infinite harmonic contents.

When reducing the number of voltage harmonics down to three on both waveforms (shown in Fig. 2.37), the drain efficiency is reduced to 81.6%. Table 2.VII and 2.VIII show the Class-F^{-1} values of voltage and current components function of the number of harmonics utilized in order to maximize the drain efficiency shown in Table 2.IX.

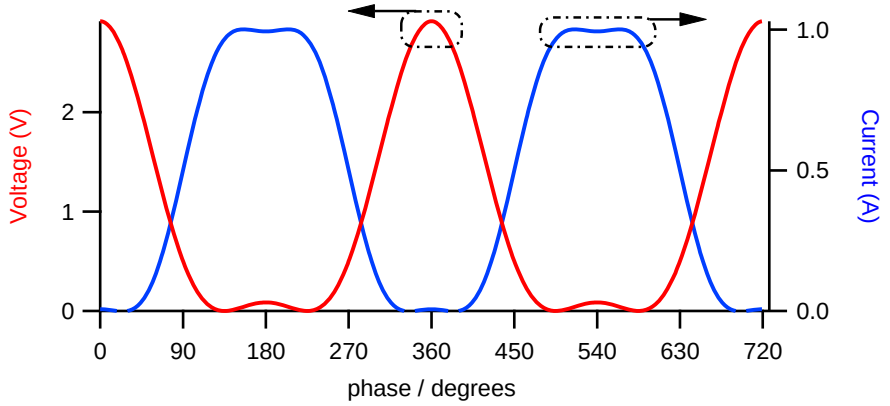

Fig. 2.37 – Class-F^{-1} voltage and current waveforms when considering for both waveforms three harmonic contents.

TABLE 2.VII
CLASS-F^{-1} OPTIMUM VOLTAGE VALUES AS A FUNCTION OF UTILIZED HARMONICS

	Inverse Class-F Voltage Harmonic Values		
M	**Using 1 harmonics**	**Using 2 harmonics**	**Using 3 harmonics**
V1	1	1.4142	1.5
V2	0	0.5	0.55
V4	0	0	0.0786

TABLE 2.VIII
CLASS-F^{-1} OPTIMUM CURRENT VALUES AS A FUNCTION OF UTILIZED HARMONICS

	Inverse Class-F Current Harmonic Values		
N	**Using 1 harmonics**	**Using 2 harmonics**	**Using 3 harmonics**
I1	0.5	0.577	0.6035
I3	0	0.083	0.1161
I5	0	0	0.0303

TABLE 2.IX
CLASS-F^{-1} OPTIMUM DRAIN EFFICIENCY AS A FUNCTION OF UTILIZED HARMONICS

	Inverse Class-F Efficiency (%)			
N	**M=1**	**M=2**	**M=4**	**M=∞**
1	50	70.71	75	78.54
3	57.7	81.6	86.55	90.63
5	60.35	85.35	90.53	94.8
∞	63.66	90.02	95.49	100

Where: M = number of voltage components
N = number of current components

Fig. 2.38 and 2.39 show the Class-F^{-1} load line with the appropriate waveforms and first three harmonic impedances with the appropriate voltage and current spectral components. It should be noted that the Class-F mode presents DC, fundamental and odd harmonic content on the voltage waveform while presenting DC, fundamental and even harmonic content on the current waveform. Here, the Class-F^{-1} presents the opposite components: DC, fundamental and even content for the voltage waveform while DC, fundamental and odd content for the current waveform.

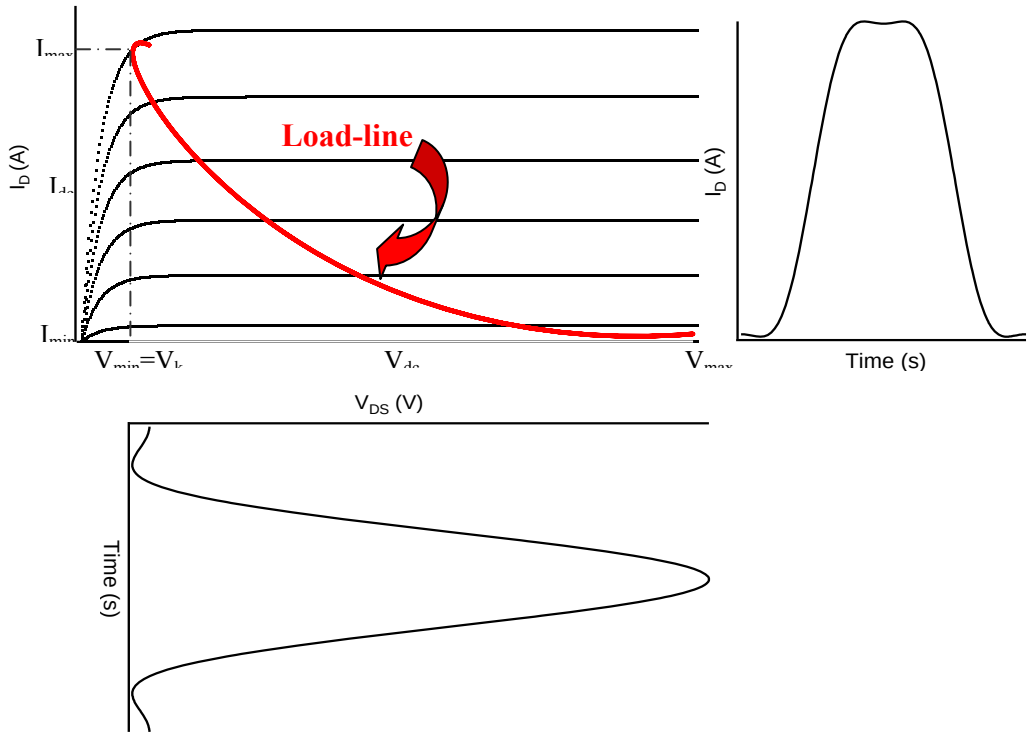

Fig. 2.38 – Inverse Class-F load-line and waveforms.

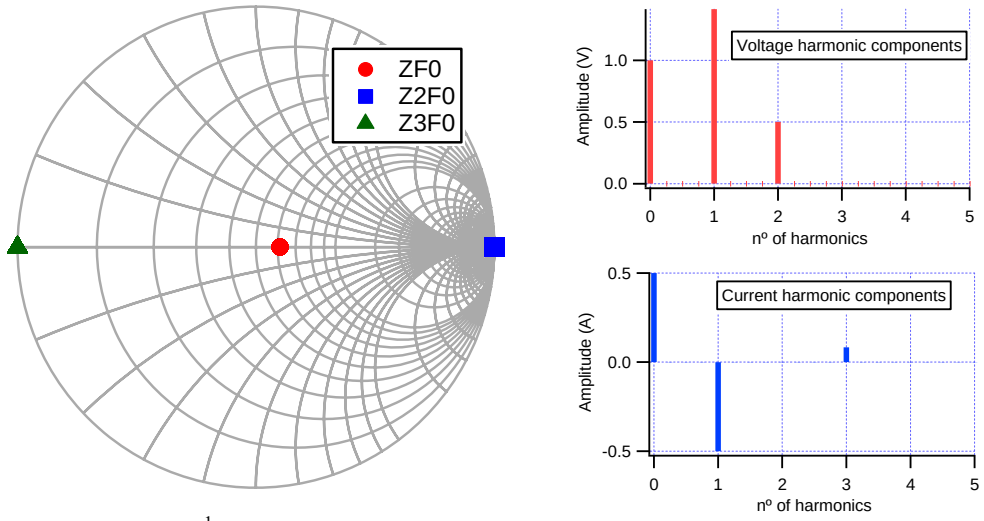

Fig. 2.39 – Class-F^{-1} impedances and voltage and current spectral components.

In the inverse Class-F case the output power is ideally higher than Class-F mode thanks to the higher voltage peak due to the introduction of second harmonic content. The drain efficiency is ideally the same, as shown in Tables 2.VI and 2.IX. However, when considering real devices, the efficiency is higher in the Class-F mode when dealing with high fundamental impedances (small device sizes for which the output power is typically smaller than 10W) while the efficiency will be higher in inverse mode if dealing with small fundamental impedances (big device sizes for which the output power is typically greater than 10W). This is demonstrated in the following work [74], and shows that the efficiency is function of the ratio between second harmonic and fundamental load. The greater is this ratio, the smaller is the efficiency and vice-versa.

2.4.9 Class-J Mode (the father of the Continuous Modes)

The understanding of the various standard classes explained in the previous sections is important in order to understand the new broadband modes shown for the first time in the research presented in this thesis.

The Class-J class, presented recently by Cripps [34], was the first new mode using the combination of fundamental and harmonic impedances in order to support a wider bandwidth in wireless communication. The Class-J is a more

practical mode which takes into account the use of intrinsic parasitics such as the drain-source capacitors C_{DS} as part of the loading criteria. In the standard modes such as the Class-B case, the short-circuit second harmonic impedance must be presented at the $I_{GEN\text{-}PLANE}$ in order to reach the high efficiency state while presenting the optimum fundamental impedance. Although in real devices, due to the non-idealities of the parasitic elements, the optimum device behaviour is very often found to be away from the perfect short and/or open circuit terminations.

However, in this case it will be assumed that the optimum performance is obtained when presenting an optimum fundamental impedance and short-circuit second harmonic load. This means that the ideal 78.5% of efficiency can be achieved when presenting the singular solution of fundamental and second harmonic impedances (as well as when presenting the appropriate bias and input drive condition), which is translated into a singular fundamental frequency solution when designing power amplifiers.

The starting point of the Class-J mode is the Class-B condition, already presented in section 2.4.4. Once the Class-B condition is achieved, the Class-J mode is presented by introducing second harmonic reactance while also presenting reactance at the fundamental impedance [75-79]. It is important to highlight that fundamental and second harmonic reactance have an inverse relationship, this means that a positive fundamental reactance is accompanied by a negative second harmonic reactance as shown in equations (2.49) and (2.50), while third harmonic impedance is considered equal to zero (2.51).

$$Z_{F0} = R_L + j \cdot R_L \tag{2.49}$$

$$Z_{2F0} = 0 - j \cdot \frac{3\pi}{8} \cdot R_L \tag{2.50}$$

$$Z_{3F0} = short - circuit \tag{2.51}$$

The resulting waveforms and load-lines are displayed in Fig. 2.40 and 2.41.

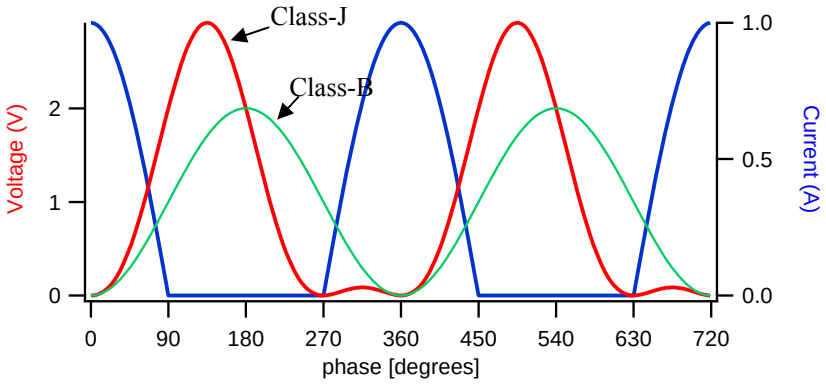

Fig. 2.40 – Class-J and Class-B voltage and current waveforms.

Here the current waveform is kept constant to a half-wave rectified sinusoidal while the introduction of fundamental and second reactive components lead to an approximately half wave rectified sinusoidal voltage waveform with 90° phase overlap between the two and higher peak voltage [76].

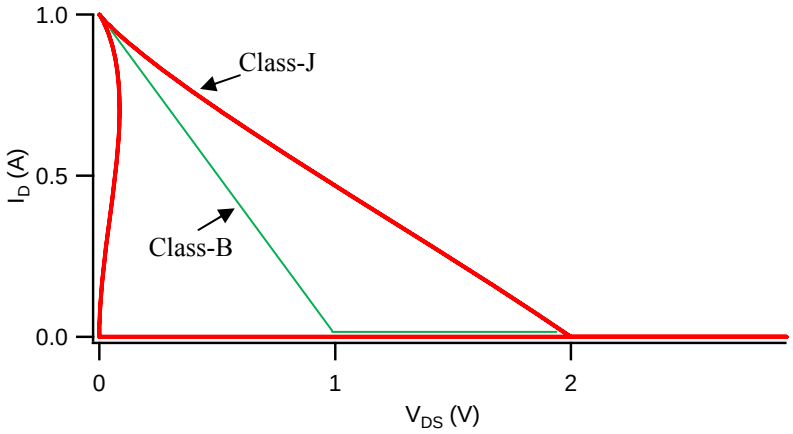

Fig. 2.41 – Class-J and Class-B load-lines.

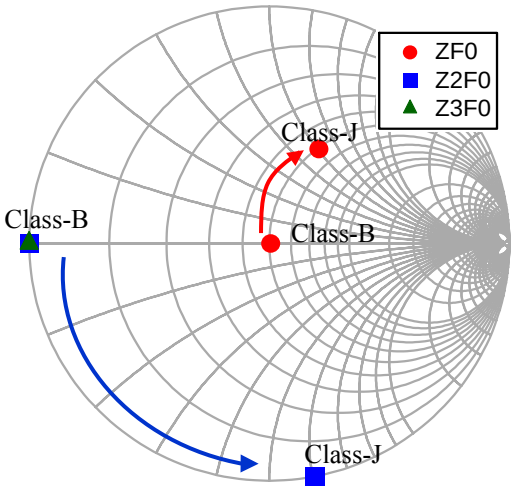

Fig. 2.42 – Class-B and Class-J first two impedances.

The benefit of the Class-J mode is that by presenting simultaneously fundamental and second harmonic reactive impedance in accordance with (2.49) and (2.50) a new solution where the same Class-B output performance in terms of power and efficiency can be achieved. The possibility to have new reactive solutions where the power efficiency state is maintained theoretically constant is translated in frequency when designing the matching networks, leading to the design of broadband power amplifiers with high power and efficiency [76].

The Class-J mode was the starting point and as mentioned in the title of this paragraph it could be said that it is the father of all the broadband/Continuous modes undertaken in this research and presented later in this thesis. In this Class-J mode one new impedance solution has been found. However, it will be demonstrated here that from the standard Class-B solution to the new Class-J solution there are multiple infinite solutions identifying what has been called the "Design Space" [80]. Besides, it will be shown that this design space concept where manipulating simultaneously the harmonic impedances can be applied to the different PA classes still maintaining the high power-efficiency conditions.

2.5 Chapter Summary

Chapter 2 has presented the literature review (state-of-art) of this research which is the basis of the work and therefore indispensable for a better understanding of the following chapters.

Here an initial overview of the various high frequency waveform measurement systems highlighting the aspects of the linear and non-linear effects are described. Furthermore, the different load-pull approaches starting from the passive technique to the more advanced active injection load-pull techniques used for the achievement of high reflection coefficients and therefore high power-efficiency amplifiers have been described. A more detailed explanation of the active envelope load pull (ELP) measurement system and approach has been given, as the various measured data presented in this thesis has been obtained using such a measurement system.

Stepping through the Chapter, a detailed analysis of the different power amplifier classes starting from the linear Class-A state to the more recent and advanced multi solution Class-J mode going through the switch modes and harmonically tuned modes has been presented. Here, the efficiency, output power, gain and linearity concepts necessary for PAs used in modern wireless communication standards have been highlighted.

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Chapter 3

Theoretical Continuous Modes Power Amplifier

3.1 Introduction

Power Amplifier (PA) design for wireless communication has to date been largely focused on improving efficiency and linearity for specified low percentage RF bandwidths. Conventionally, higher efficiency PAs are designed for narrow-band operation [1-6] and cannot be used in broadband applications covering multiple bands in wireless communication systems. Future 4G (Fourth Generation) wireless network systems, which include WiMax (Worldwide Interoperability for Microwave Access), LTE (Long term Evolution) [7], and LTE-Advanced [8] are in continuous progression to satisfy the great demand in mobile phones with high QoS (Quality of Services). The development of a PA design methodology for these advance systems will be required in order to allow more services as higher data-rate transmissions over long distances. However, the achievement of these new technologies with all these services will require larger bandwidths. The challenge in designing broadband PAs is to maintain the same output performance in terms of power and efficiency over bandwidth compared with the standard narrow band modes presented in Chapter 2. For the narrow band modes the aim is to maintain

the required short-circuit and/or open-circuit high harmonic terminations at the device intrinsic current-generator plane ($I_{GEN-PLANE}$) [9], which due to practical constraints must be placed at a distance from the device as it will be shown in the package device in Chapter 5. As mentioned earlier, the request of bandwidth used in the latest wireless networks for the advanced applications, has lead the RFPA/microwave community to improve the PA designs also in terms of bandwidth. Different interesting approaches have been recently presented [10-18].

From Chapter 2 it has been seen that the Class-J mode has presented for the first time a new solution where starting from the Class-B state the output performance is theoretically kept constant. After that, it has been demonstrated that between the Class-B and the Class-J solutions there are infinite solutions where the output performance is ideally kept constant [19]. Therefore, by moving reactively the fundamental and harmonic terminations away from the optimum point and from the short-circuit and open-circuit conditions respectively, these multiple solutions can be exploited. This new world of moving reactively, simultaneously and with the proper phases the fundamental and harmonic impedances have been described in an easy and elegant way through the use of the factorial representation presented the first time by Cripps et. al. [19], who acknowledges the Rhodes singularity condition [20]. In this case by varying only one parameter on the voltage and/or current equations the combination of the right fundamental and harmonic impedances with the proper phase relationship is given, as it will be demonstrated later in this Chapter.

The work presented in this Chapter describes for the first time the theoretical (supported by ADS - Advanced Design System simulations presented in the Appendix C), of the broadband classes termed *"Continuous Modes"* [21, 22, 23]. Here, the multi-solutions exploited for the Class-B mode (Class-J) is applied for the first time to the other standard classes.

In this Chapter the broadband Continuous Modes applied to the Class-A, Class-B, Class-F and inverse Class-F (Class-F^{-1}) cases, where the PA output performance in terms of efficiency and power is maintained at constant levels for a wide band of frequencies is for first time presented. All the theoretical Figures here presented where exploiting the various Continuous Modes have been achieved by

using a new Igor software. The Broadband Continuous Class-AB (not shown) is identical to the Continuous Class-B analysis with the difference that in the Class-AB condition the conduction angle ϑ is $180° < \vartheta < 360°$ while in the Class-B case $\vartheta = 180°$.

3.2 Novel Overall Continuous Modes

Through the use of "*waveform engineering*" [24] and by knowing the different target voltage $v(\theta)$ and current $i(\theta)$ waveforms, it is possible to define the transistor operation modes.

As mentioned in the introduction of this Chapter, the conventional modes have been theoretically explored and further developed [2, 20, 25] during the last decades in order to improve the overall output performance. However, these scientific works have been focused on improving the performance for the specific narrow bandwidths, typically around 5-10% or lower. This is mainly due to the high-Q matching structure used, where operation too far either side of the centre frequency leads to a rapid decrease in both power and efficiency.

The recent Class-J mode, already described in Chapter 2, was the starting point of the new broadband modes presented in this thesis, which have been termed "*Continuous Modes*" [21, 22, 23]. The Continuous Modes are obtained by adding a new operator $(1-\delta\sin\theta)$ on the voltage or current formulations resulting in a new family of voltage or current waveforms. This new family of waveforms lead to a different set of fundamental and harmonic load solutions where output power and efficiency are maintained at constant levels. It is important to highlight that if the operator is applied on the voltage formulation, the voltage waveform will vary while the current waveform remains constant. In this case if the Continuous Mode is applied for example to the conventional Class-F case, when varying the voltage waveform the new broadband mode will be called as *Continuous Class-FV*. Vice-versa, when the operator is applied on the current formulation, in this case using the parameter ξ (thus the operator $1-\xi\sin\theta$), the voltage waveform remains constant and the current waveform is allowed to vary leading to what has been called *Continuous Class-FI.* Same concept is applied to the Class-A, Class-B and

Inverse Class-F (Class-F^{-1}) modes which will be all presented in a detailed analysis in the next paragraphs of this Chapter.

The possibility to have multiple load solutions increases flexibility when designing narrow band PAs, as there is no need to provide the ideal short-circuit and/or open-circuit harmonic terminations. Besides, more importantly this new set of load solutions can be then translated into a useful "*design space*" in the frequency domain, allowing the design of broadband power amplifiers.

Equations (3.1) and (3.2) describe the general formulations for the overall Continuous modes voltage and current waveforms when considering for both first three harmonic components:

$$v(\vartheta) = (1 - \alpha\cos\vartheta - \beta\cos 2\vartheta - \gamma\cos 3\vartheta)\cdot[1 - \delta\sin\vartheta], \tag{3.1}$$

$$i(\vartheta) = (1 + a\cos\vartheta + b\cos 2\vartheta + c\cos 3\vartheta)\cdot[1 - \xi\sin\vartheta], \tag{3.2}$$

where α, γ, β and δ are the parameters describing the voltage waveform and a, b, c and ξ are the parameters describing the current waveform.

Table 3.I shows the voltage and current parameter values just mentioned, and by replacing those values in (3.1) and (3.2), the conventional Class-A, Class-B, Class-F and Class-F^{-1}, as well as the broadband Continuous Class-AV, Continuous Class-AI, Continuous Class-BV, Continuous Class-BI, Continuous Class-FV, Continuous Class-FI, Continuous Class-F^{-1}V and Continuous Class-F^{-1}I modes are achieved. The impedances that "vary" are functions of the two parameters δ and ξ.

TABLE 3.I
V-I WAVEFORM PARAMETERS FOR THE CONVENTIONAL AND CONTINUOUS MODES

PA Modes	**Voltage Parameters**				**Current Parameters**				**Impedances**
	α	**β**	**γ**	**δ**	**a**	**b**	**c**	**ξ**	
Class-A	1	0	0	0	1	0	0	0	Z_{F0}=opt.
Continuous Class-AV	1	0	0	-1÷1	1	0	0	0	Z_{F0}=varies, Z_{2F0}=∞
Continuous Class-AI	1	0	0	0	1	0	0	-1÷1	Z_{F0}=varies, Z_{2F0}=0
Class-B	1	0	0	0	√2	1/2	0	0	Z_{F0}=opt., Z_{2F0}=0
Continuous Class-BV	1	0	0	-1÷1	√2	1/2	0	0	Z_{F0}=varies, Z_{2F0}=varies
Continuous Class-BI	1	0	0	0	√2	1/2	0	-1÷1	Z_{F0}=varies, Z_{2F0}=0, Z_{3F0}=0
Class-F	2/√3	0	1/3√3	0	√2	1/2	0	0	Z_{F0}=opt., Z_{2F0}=0, Z_{3F0}=∞
Continuous Class-FV	2/√3	0	1/3√3	-1÷1	√2	1/2	0	0	Z_{F0}=varies, Z_{2F0}=varies, Z_{3F0}=∞
Continuous Class-FI	2/√3	0	1/3√3	0	√2	1/2	0	-1÷1	Z_{F0}=varies, Z_{2F0}=0, Z_{3F0}=varies
Class-F^{-1}	√2	1/2	0	0	2/√3	0	-1/3√3	0	Z_{F0}=opt., Z_{2F0}=∞, Z_{3F}=0
Continuous Class-F^{-1}V	√2	1/2	0	-1÷1	2/√3	0	-1/3√3	0	Z_{F0}=varies, Z_{2F0}=∞, Z_{3F0}=varies
Continuous Class-F^{-1}I	√2	1/2	0	0	2/√3	0	-1/3√3	-1÷1	Z_{F0}=varies, Z_{2F0}=varies, Z_{3F0}=0

- The high harmonic impedances not specified are short-circuited.

3.3 Continuous Class-AV Mode

By substituting the *Continuous Class-AV* parameter values of Table 3.I in equations (3.1) and (3.2), the current operator [1-ξsinθ] will remain equal to zero while the operator [1-δsinθ] function of δ will be presented on the voltage formulation.

This means that the current waveform will be assumed constant sinusoidal while the new family of waveforms is presented on the voltage, as shown in (3.3) and (3.4):

$$v_{Cont\_AV}(\vartheta) = (1-\cos\vartheta)\cdot[1-\delta\sin\vartheta], \tag{3.3}$$

$$i_{Cont\_AV}(\vartheta) = (1+a\cos\vartheta), \tag{3.4}$$

where both voltage and current are normalised to unity and in this case a=1.

For δ=0 the key operator [1-δsinθ] is equal to 1, thus delivering the conventional sinusoidal Class-A waveforms. When varying δ, the new family of voltage waveforms with higher peaks are presented, as shown in Fig. 3.1. The load-lines are shown in Fig. 3.2 for values of δ=0 and δ=1. Here it can be noted that the maximum current is the same for the different values of δ, while a bigger excursion on the bottom part (voltage axes) is revealed. The load-line for δ=-1 would give the exact same behaviour of δ=1 as the waveforms are presented at the $I_{GEN-PLANE}$ thus symmetric.

It is very important to highlight that that the parameter δ has to vary between -1 and 1 in order to keep the voltage waveforms positive or grazing the zero value for δ=±1 [22]. If δ goes beyond that range, the voltage waveforms drop lower than zero, as highlighted in yellow in Fig. 3.3 where δ=±1.1, with consequently non-linear behaviour accompanied in reduction of power and efficiency. This concept of maintaining the parameter δ between -1 and 1 will be applied for all the Continuous modes presented in this Chapter. However, it will be demonstrated in Chapters 4 and 6 that by adding one more operator in (3.1) and (3.2), the actual ranges of δ and ξ where the voltage and current waveforms are maintained above zero decreases.

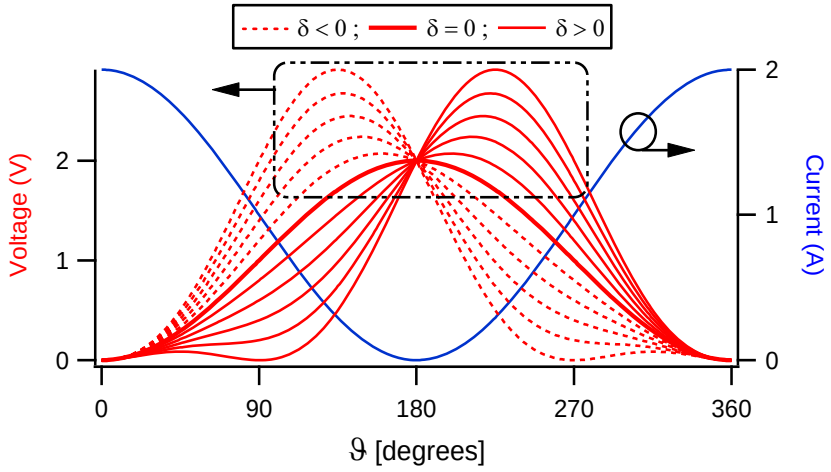

Fig. 3.1 – Theoretical Continuous Class-AV voltage and current waveforms for δ varying between $-1 \leq \delta \leq 1$ in steps of 0.2.

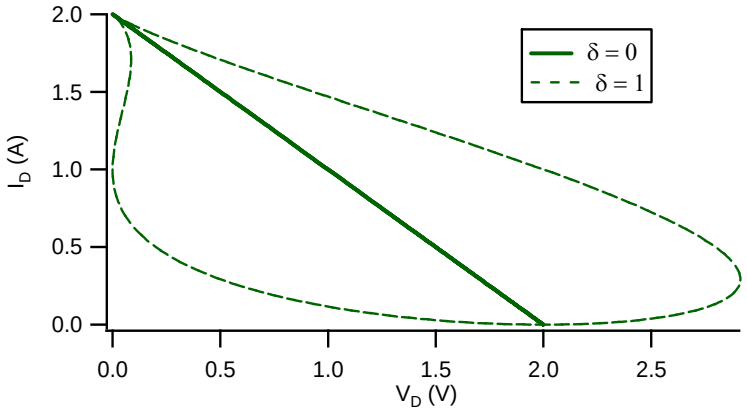

Fig. 3.2 – Theoretical Continuous Class-AV load-lines for δ=0 and δ=1 (δ=-1 is the symmetric load-line of δ=1).

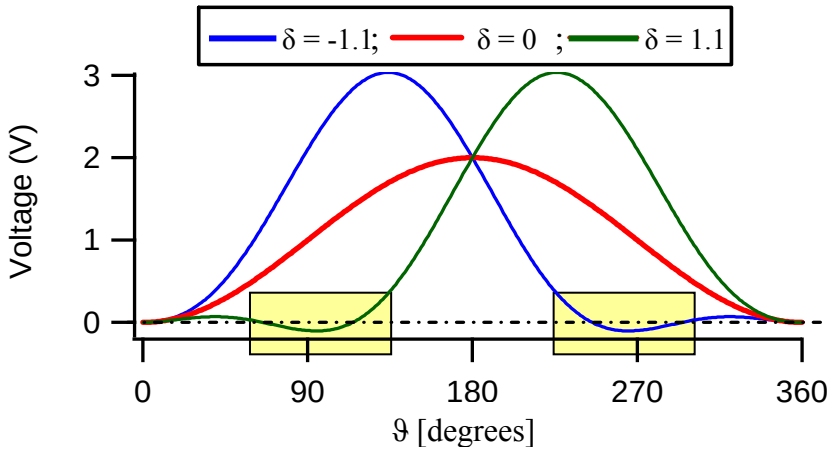

Fig. 3.3 – Theoretical Continuous Class-AV voltage waveforms for δ=0 (red line) and for δ=±1.1 (green and blue lines).

For the conventional Class-A mode the optimum device performance with ideal efficiency of 50% can be obtained by optimizing only the fundamental impedance considering short-circuit the higher harmonic terminations. In this case, as shown in the impedances plotted in Fig. 3.4, if maintaining open-circuited the second harmonic termination, a wide reactive range of fundamental load is revealed. Here by varying the fundamental impedance on its circle of constant resistance, the theoretical 50% drain efficiency and output power (normalized to unity) are maintained at constant level for all the range of δ, as shown in Fig. 3.5 and Fig. 3.6, leading to the new family of Continuous Class-AV voltage waveforms before described. This is due to the fact that by varying the parameter δ, second harmonic content is developed on the voltage waveform, while only fundamental component is ideally presented on the current waveform. This means that the second harmonic current is null leading to an open-circuit second harmonic load. Therefore, the fundamental load is allowed to vary on its circle of constant optimum resistance still maintaining a constant RF output power and drain efficiency.

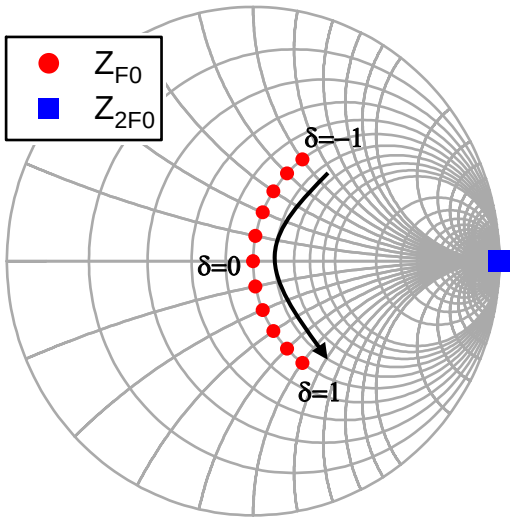

Fig. 3.4 – Theoretical Continuous Class-AV fundamental and second harmonic impedances for δ varying between $-1 \leq \delta \leq 1$ in steps of 0.2.

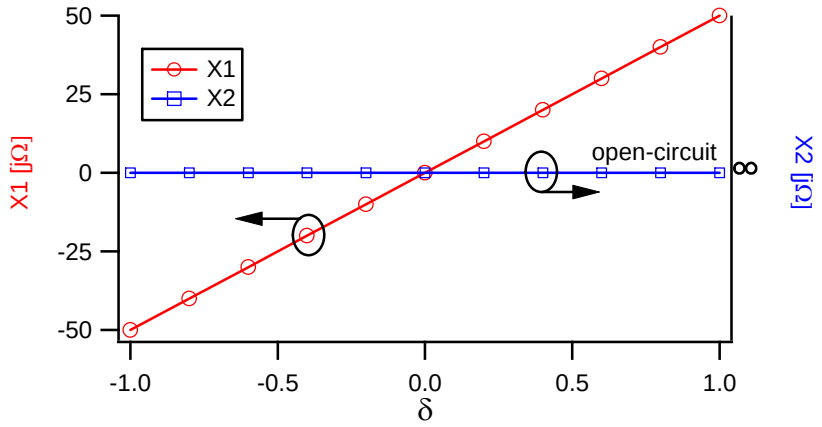

Fig. 3.5 – Theoretical Continuous Class-AV fundamental and second harmonic reactances X1 and X2 for δ varying between $-1 \leq \delta \leq 1$ in steps of 0.2.

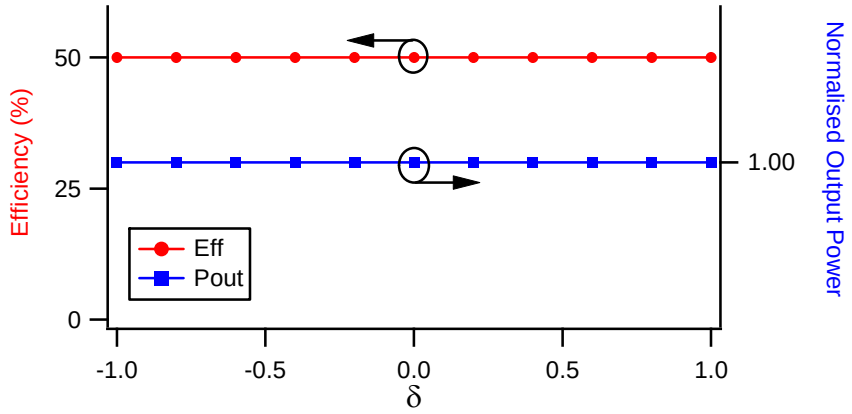

Fig. 3.6 – Theoretical Continuous Class-AV drain efficiency and normalised output power for δ varying between $-1 \leq \delta \leq 1$ in steps of 0.2.

In more details, the achievement of constant output power and drain efficiency with varying δ is due to the fact that the expansion of equation (3.3), leads to

$$v_{Cont\_AV}(\vartheta) = 1 - \cos\vartheta - \delta\sin\vartheta + \frac{\delta}{2}\sin 2\vartheta \,. \tag{3.5}$$

Here, it can be noted that the DC component is not function of δ, thus will remain constant (in this case equal to 1) as well as the real part of both fundamental and second harmonic voltage (the cos terms), with values equal to 1 and 0 respectively. Therefore, when varying the parameter δ, the reactive parts of the fundamental and second voltage vary (the sin terms) but the DC component and the real fundamental voltage will remain invariant.

Therefore, being

$$P_{RF} = \frac{1}{2}\mathrm{Re}\left(V_1 \cdot I_1^{*}\right), \tag{3.6}$$

and maintaining a constant current waveform, the output power will be maintained invariant when varying δ as also shown in Fig. 3.6.

Besides, being the drain efficiency

$$\eta = \frac{P_{RF}}{P_{DC}}, \tag{3.7}$$

where the DC power is

$$P_{DC} = V_{DC} \cdot I_{DC}, \tag{3.8}$$

the DC components of both voltage and current waveforms will be constant resulting in a constant ideal drain efficiency of 50%, again shown in Fig. 3.6.

By applying the Fast Fourier Transform (FFT) on (3.3) (3.4), DC, fundamental and harmonic voltage and current components can be calculated as shown in equations from (3.9) to (3.14):

$$V_{DC} = 1, \tag{3.9}$$

$$V_1 = -\cos\vartheta - \delta\sin\vartheta, \tag{3.10}$$

$$V_2 = 0 + \frac{\delta}{2}\sin 2\vartheta, \tag{3.11}$$

$$I_{DC} = 1, \tag{3.12}$$

$$I_1 = \cos\vartheta, \tag{3.13}$$

$$I_2 = 0. \tag{3.14}$$

The fundamental and harmonic impedances can be calculated by dividing the respective voltage and current complex components. It is important to highlight that equations from (3.9) to (3.14) describe the phasor representation of the voltage and current components.

The generic phasor formulation

$$V(t) = V_r \cos\omega t - V_q \sin\omega t, \tag{3.15}$$

where V_r and V_q are the real and imaginary parts of the voltage component, is

achieved from:

$$V(t) = \mathrm{Re}\left\{\left(V_r + jV_q\right)\cdot\left(\cos\omega t + j\sin\omega t\right)\right\}$$
$$= \mathrm{Re}\left\{\left(V_r + jV_q\right)\cdot e^{j\omega t}\right\}, \quad (3.16)$$

leading to the complex voltage formulation

$$V_{cmplx} = V_r + jV_q\,. \quad (3.17)$$

As it can be noted, the V_r of the phasor and complex representations (equations 3.15 and 3.17) are equivalent, but the reactive part V_q presents different sign. This explains the necessity of changing the sign of the reactive component of the phasor representation for the impedances calculation [26].

Therefore, for the Continuous Class-AV mode the phasor representation of the voltage and current components (equations from 3.9 to 3.14) are described in complex representation as:

$$V_{DC} = 1\,, \quad (3.18)$$

$$V_{1cmplx} = -1 + j\delta\,, \quad (3.19)$$

$$V_{2cmplx} = 0 - j\frac{\delta}{2}\,, \quad (3.20)$$

$$I_{DC} = 1\,, \quad (3.21)$$

$$I_{1cmplx} = 1\,, \quad (3.22)$$

$$I_{2cmplx} = 0\,. \quad (3.23)$$

Dividing the complex voltage components with the appropriate complex current components the Continuous Class-AV fundamental and second harmonic impedances normalized to the fundamental resistance are derived, as shown in (3.24) and (3.25).

$$Z_{LOAD} = -R_{F0} + j\cdot\delta\cdot R_{F0}\,, \quad (3.24)$$

$$Z_{2F0} = \infty \quad \text{(open-circuit)} \quad (3.25)$$

The resistance R_{F0} is the fundamental optimum one, which in this case has been assumed to be 50 Ω. Besides, as it can be seen in (3.24), that fundamental resistance R_{F0} is negative. This is due to the fact that the output current I_{LOAD} has been assumed to flow towards the load (Fig. 3.7). When defining the current I_{DS}

flowing towards the device, the resistance R_{F0} will be positive, therefore the impedance will be

$$Z_{F0} = -Z_{LOAD}\,. \tag{3.26}$$

$$Z_{F0} = R_{F0} - j\cdot\delta\cdot R_{F0}\,, \tag{3.27}$$

where R_{F0} is the fundamental resistance and $X_L = \delta \cdot R_{F0}$ is its reactive part.

The second harmonic impedance is not function of δ and remains constant open-circuit.

In the following analysis describing the other broadband modes the current will be defined to flow towards the device leading to a positive resistance R_{F0}.

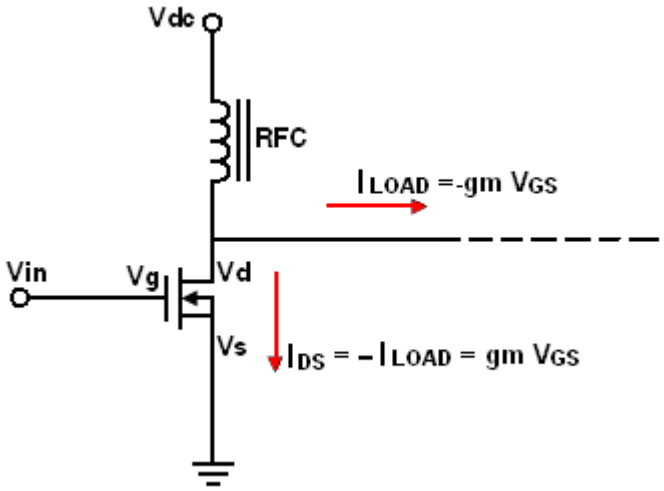

Fig. 3.7 – Current flowing towards the transistor and towards the load.

3.4 Continuous Class-AI Mode

For the Continuous Class-AV mode described in the previous paragraph, the operator [1-δsinθ] was applied on the voltage waveform, while in this new "*Continuous Class-AI*" the operator [1-ξsinθ] is applied on the current formulation. As it can be noted and as already described in the introduction of this Chapter, when applying the operator on the voltage formulation, the parameter δ has been used while in this case (where varying the current waveform) the parameter ξ is used.

Equations (3.28) and (3.29) represent the Continuous Class-AI voltage and current formulations:

$$v_{Cont\_AI}(\vartheta) = (1 - \cos\vartheta), \tag{3.28}$$

$$i_{Cont\_AI}(\vartheta) = (1 + a\cos\vartheta)\cdot[1 - \xi\sin\vartheta], \tag{3.29}$$

where a=1.

Here the same concept described on the Continuous Class-AV but with inverted waveforms is applied. Therefore, the voltage waveform remains constant sinusoidal while the new family of waveforms is achieved on the current side, as shown in Fig. 3.8. The load-lines for ξ=0 and ξ=1 are shown in Fig. 3.9. Here differently from the previous case, when ξ=1 now the maximum achievable voltage (bottom part of the load-lines) remains the same than the standard Class-A case while a wider excursion is obtained on the top of the load-line with current values greater than 2.5 A.

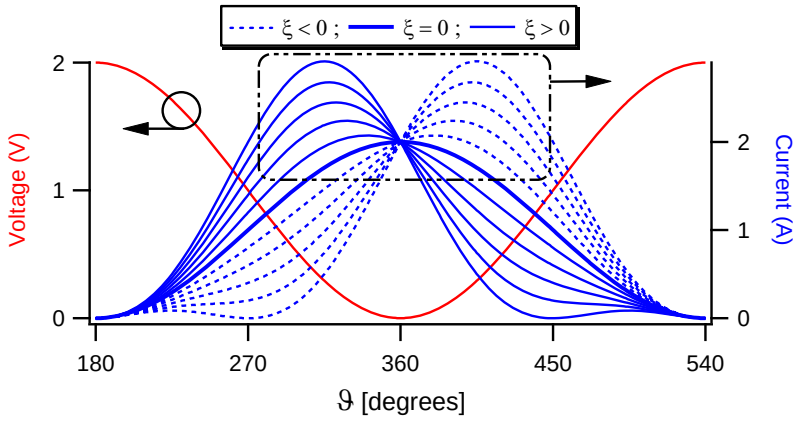

Fig. 3.8 – Theoretical Continuous Class-AI voltage and current waveforms for ξ varying between $-1 \leq \xi \leq 1$ in steps of 0.2.

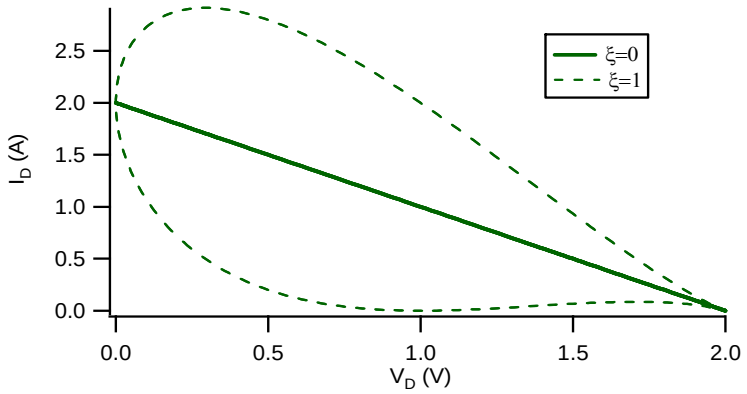

Fig. 3.9 – Theoretical Continuous Class-AI load-lines for ξ=0 and ξ=1 (ξ=-1 is the symmetric load-line of ξ=1).

The complex representation of voltage and current components are described from (3.30) to (3.35).

$$V_{DC} = 1, \tag{3.30}$$

$$V_{1cmplx} = -1, \tag{3.31}$$

$$V_{2cmplx} = 0, \tag{3.32}$$

$$I_{DC} = 1, \tag{3.33}$$

$$I_{1cmplx} = 1 + j \cdot \xi, \tag{3.34}$$

$$I_{2cmplx} = 0 + j \cdot \frac{\xi}{2}. \tag{3.35}$$

Therefore, dividing the voltage components with the respective current components, fundamental and second harmonic impedances will be

$$Z_{F0} = \frac{1}{1+\xi^2} - j\frac{\xi}{1+\xi^2}, \tag{3.36}$$

$$Z_{2F0} = 0 \quad \text{(short-circuit)}. \tag{3.37}$$

As it can be seen from Fig. 3.10 and Fig. 3.11, as well as from equation (3.38) the fundamental load varies on its line of constant conductance G_{F0}. This means that the conductance will remain constant while the susceptance $B_{F0}=\xi \cdot G_{F0}$ varies as a function of ξ with second harmonic load kept short-circuited. This is due to the variation of the current waveform, where second harmonic content is developed while only fundamental component is presented on the voltage waveform.

$$Y_{F0} = G_{F0} + j \cdot \xi \cdot G_{F0}, \tag{3.38}$$

$$Y_{2F0} = short - circuit. \tag{3.39}$$

Again, for all the ξ range, the values of output power and drain efficiency are kept constant to the theoretical conventional Class-A mode as shown in Fig. 3.12. Therefore, when presenting this range of fundamental impedances while maintaining a short-circuit second harmonic termination, a broadband Class-A

(Continuous Class-AI) power amplifier where power and efficiency remain constant can be realised.

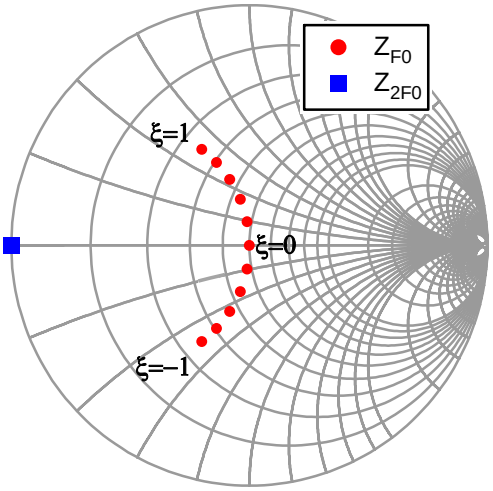

Fig. 3.10 – Theoretical Continuous Class-AI fundamental and second harmonic impedances for ξ varying between $-1 \leq \xi \leq 1$ in steps of 0.2.

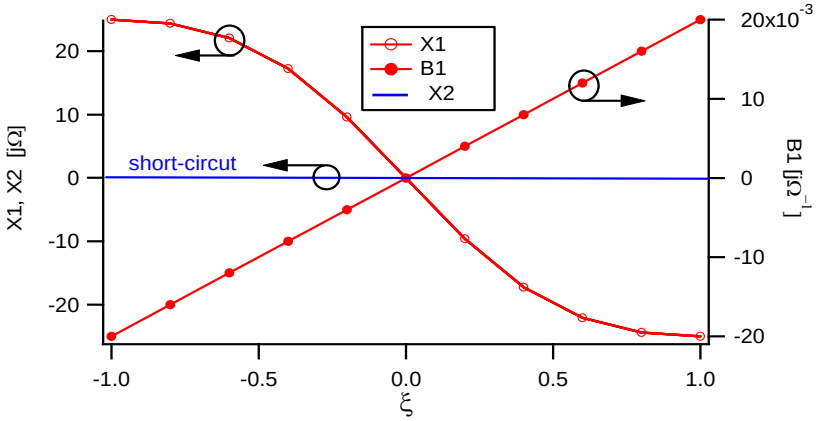

Fig. 3.11 – Theoretical Continuous Class-AI fundamental reactance X1 and susceptance B1 and second harmonic reactances X2 for ξ varying between $-1 \leq \xi \leq 1$ in steps of 0.2.

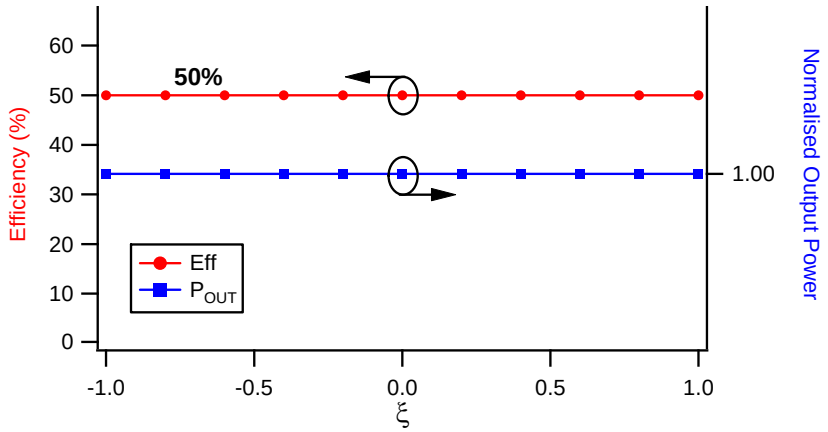

Fig. 3.12 – Theoretical Continuous Class-AI drain efficiency and normalised output power for ξ varying between $-1 \leq \xi \leq 1$ in steps of 0.2.

3.5 Continuous Class-BV (Class-BJ) Mode

As mentioned earlier and explained in Chapter 2 of this thesis, the father of these broadband modes was the Class-J. The "*Continuous Class-BV*" described in this paragraph is just a new way to re-word the well-known Class-BJ [1, 22, 27], which is an extension of the first Class-J mode [28-29], both described for the first time by Cripps [1]. In the first Class-J case, by presenting a new voltage waveform and maintaining a constant half-wave rectified sinusoidal current waveform, another solution was found (the one for δ=1) where output power and drain efficiency are the same as Class-B. Therefore, being the output performance constant when presenting these two extreme load solutions for δ=0 (Class-B) and for δ=1 (Class-J), the idea of the Continuous Class-BV is to provide infinite solutions between the Class-B and the Class-J cases, by presenting the appropriate fundamental and harmonic phase adjustments [22, 27].

The voltage and current waveforms are described in (3.40) and (3.42)

$$v_{Cont\_BV}(\vartheta) = (1-\cos\vartheta)\cdot(1-\delta\sin\vartheta), \tag{3.40}$$

which expands into

$$v_{Cont\_BV}(\vartheta) = 1-\cos\vartheta-\delta\sin\vartheta+\frac{\delta}{2}\sin 2\vartheta, \tag{3.41}$$

$$\begin{aligned} i_{Cont\_BV}(\vartheta) &= I_{peak}\cos\vartheta \qquad 0<\vartheta<\pi/2\,,\ (3/2)\pi<\vartheta<2\pi\,, \\ &= 0 \qquad\qquad\qquad \pi/2<\vartheta<(3/2)\pi\,, \end{aligned} \tag{3.42}$$

where I_{peak} is the maximum current.

When δ=0 the conventional Class-B sinusoidal voltage waveform is achieved. When varying δ different than zero and between -1 and 1, the new family of voltage waveforms is revealed as shown in Fig. 3.13. Fig. 3.14 shows the standard Class-B load-line (δ=0) as well as the load-line for δ=1. The load-line for δ=1 reveal higher voltage values on the bottom part of the line compared with the conventional Class-B case, while the upper part presents current values equal to the standard one.

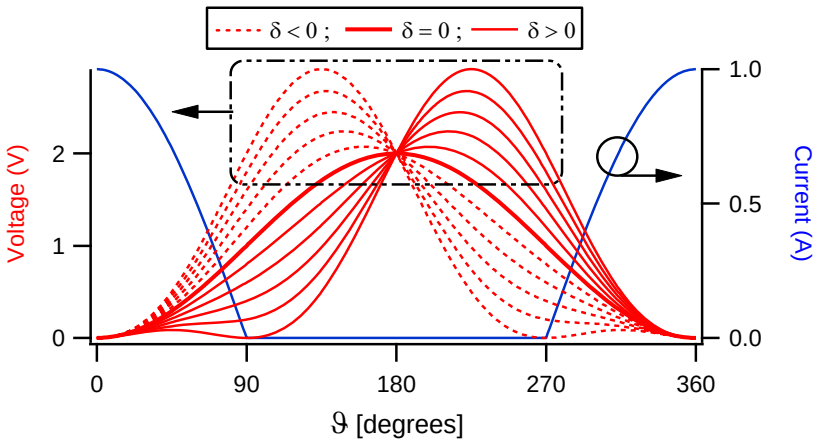

Fig. 3.13 – Theoretical Continuous Class-BV voltage and current waveforms for δ varying between $-1 \leq \delta \leq 1$ in steps of 0.2.

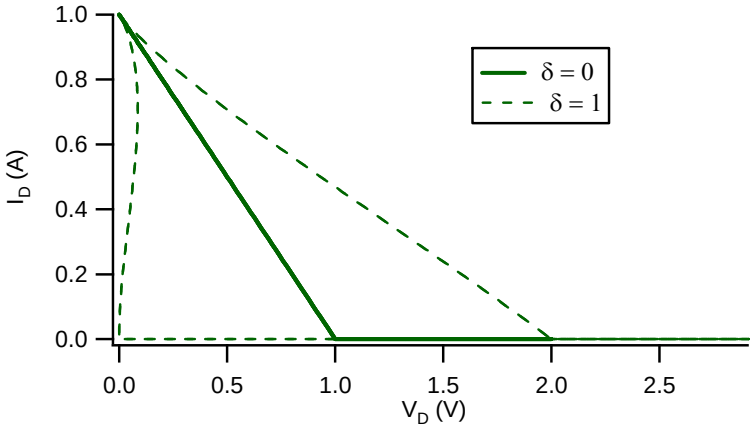

Fig. 3.14 – Theoretical Continuous Class-BV load-lines for δ=0 and δ=1 (δ=-1 is the symmetric load-line of δ=1).

As in the previous case, the expanded voltage formulation shown in (3.41) is the phasor voltage representation, therefore after using the FFT, they can then be described in complex representation as

$$V_{DC} = 1, \tag{3.43}$$

$$V_{1cmplx} = -1 + j \cdot \delta, \tag{3.44}$$

$$V_{2cmplx} = 0 - j \cdot \frac{\delta}{2}, \tag{3.45}$$

Dividing the appropriate voltage and current complex components, when considering the ideal half-wave rectified sinusoidal current waveform shape and

when considering the current flowing into the device, the fundamental and second harmonic impedances are:

$$Z_{F0} = R_{F0} - j \cdot \delta \cdot R_{F0}\,, \tag{3.46}$$

$$Z_{2F0} = 0 + j \cdot \delta \cdot \frac{3\pi}{8} \cdot R_{F0}\,. \tag{3.47}$$

The fundamental real part R_{F0} is assumed to be the optimum one ($R_{F0}=R_{opt}$) , again in this theoretical case it is assumed to be 50 Ω, while the reactive part is $X_{F0}=\delta \cdot R_{F0}$.

The second harmonic resistance is kept constant to zero while the reactive part is $X_{2F0}=\delta \cdot (3\pi/8) \cdot R_{F0}$. While in the Continuous Class-AV and Continuous Class-AI modes the second harmonic impedances were kept constant open-circuit and short-circuit respectively, here the reactive variation of the fundamental load is accompanied by a reactive variation of the second harmonic impedance as well. This is due to the fact that, in this mode both voltage and current waveforms develop second harmonic component. Furthermore, fundamental and second harmonic terminations are related to an inverse relationship where the positive variation of δ is accompanied by a negative variation of fundamental reactance and positive variation of second harmonic reactance from the short-circuit condition and vice-versa, as shown in equations (3.46) (3.47) and in Fig. 3.15 and 3.16.

The variation of both fundamental and second harmonic reactance exposes a wide design space. Here the expected output power and the theoretical Class-B efficiency of 78.5% (assuming infinite harmonic contents and two harmonic voltages) are maintained theoretically constant for the entire δ design space. As explained previously, this is due to the fact that although the variation of δ causes both fundamental and second harmonic load to vary, the DC and resistive parts will remain constant. Therefore, keeping the current waveform constant, leads to a constant output power and drain efficiency, as shown in Fig. 3.17.

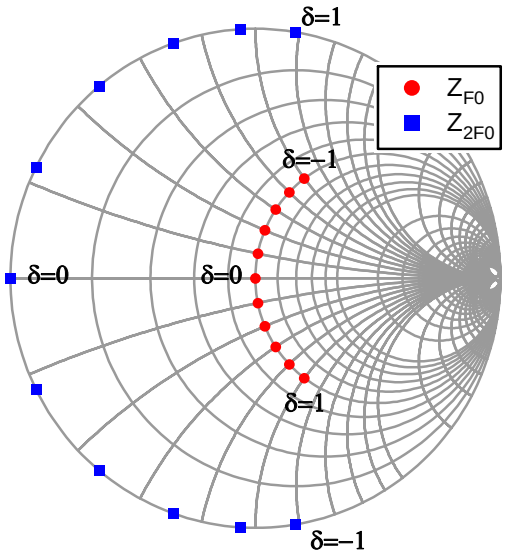

Fig. 3.15 – Theoretical Continuous Class-BV fundamental and second harmonic impedances for δ varying between $-1 \leq \delta \leq 1$ in steps of 0.2.

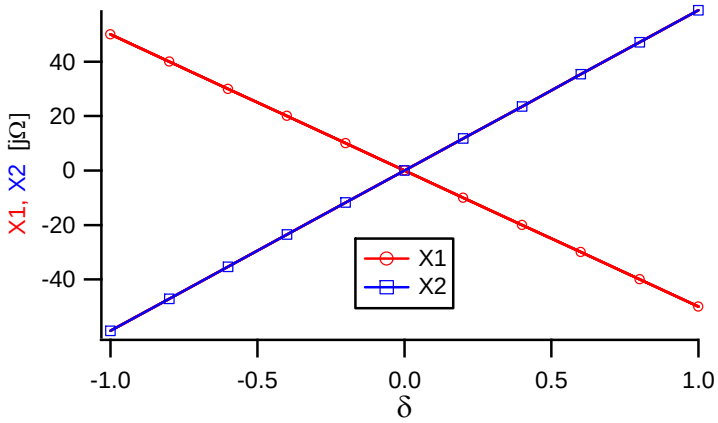

Fig. 3.16 – Theoretical Continuous Class-BV fundamental and second harmonic reactance X1 and X2 for δ varying between $-1 \leq \delta \leq 1$ in steps of 0.2.

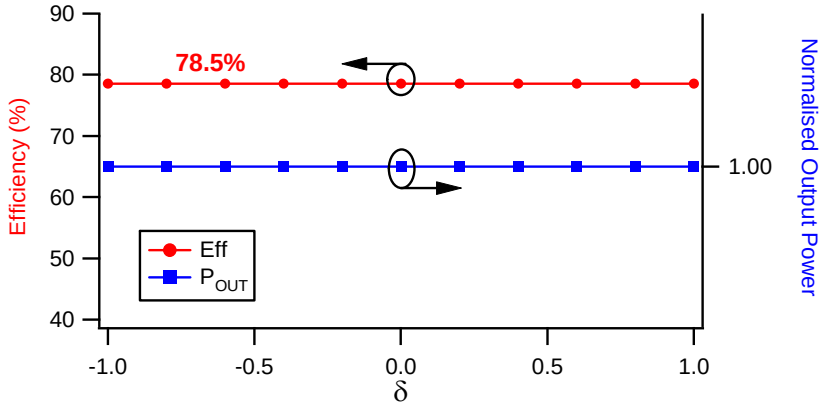

Fig. 3.17 – Theoretical Continuous Class-BV drain efficiency and normalised output power for δ varying between $-1 \leq \delta \leq 1$ in steps of 0.2.

3.6 Continuous Class-BI Mode

In *"Continuous Class-BI"* mode the operator (1-$\xi\sin\theta$) is applied on the current formulation, allowing current waveform to vary from its half-wave rectified sinusoidal shape while maintaining a constant sinusoidal voltage waveform, as shown in (3.48) and (3.49).

$$v_{Cont\_BI}(\vartheta) = (1 - \cos\vartheta) \tag{3.48}$$

$$\begin{aligned} i_{Cont\_BI}(\vartheta) &= (I_{peak}\cos\vartheta)\cdot[1 - \xi\sin\vartheta] \qquad (3/2)\pi < \vartheta < (5/2)\pi\,, \\ &= 0 \qquad\qquad\qquad\qquad \pi < \vartheta < (3/2)\pi\,,\ (5/2)\pi < \vartheta < 3\pi\,. \end{aligned} \tag{3.49}$$

This case is similar to the Continuous Class-AI mode in terms of impedance, as when varying the parameter ξ the fundamental impedance varies reactively while the second harmonic impedance will be a fixed point, in this case a short-circuit. This is due to the fact that, starting from the half-wave rectified sinusoidal current waveform (which presents fundamental and even contents) the higher harmonics will still be developed on the current waveform while the voltage waveform remains sinusoidal. This means that on the voltage waveform only the fundamental component will be developed leading to a short-circuit second harmonic termination (thus independently from the spectrum components developed on the current). The difference between this mode and the Continuous Class-AI is that in this case by biasing the device at the pinch-off $V_{GS}=V_{TH}$, the transistor will remain active for half time (180°) minimizing the overlap between voltage and current waveforms compared with the Class-A condition. This leads to higher efficiency of 78.5%, for now multiple fundamental load solutions which can be translated into a wideband of frequencies.

Fig. 3.18 shows the sinusoidal voltage waveform as well as the new family of Continuous Class-BI current waveforms achieved when considering fundamental impedance varying on the circle of constant conductance from its initial load of 50 Ω value, and constant short-circuit second harmonic load, as shown in Fig. 3.20. Fig. 3.19 shows the load-lines for ξ=0 and ξ=1. As these waveforms are built on the

half-wave rectified sinusoidal shape, for ξ=1 and for V_D<V_{DC} (where V_{DC}=1) the current reaches values greater than the standard load-line, while for V_D>V_{DC} it is equal to zero being the region where the device is OFF [1].

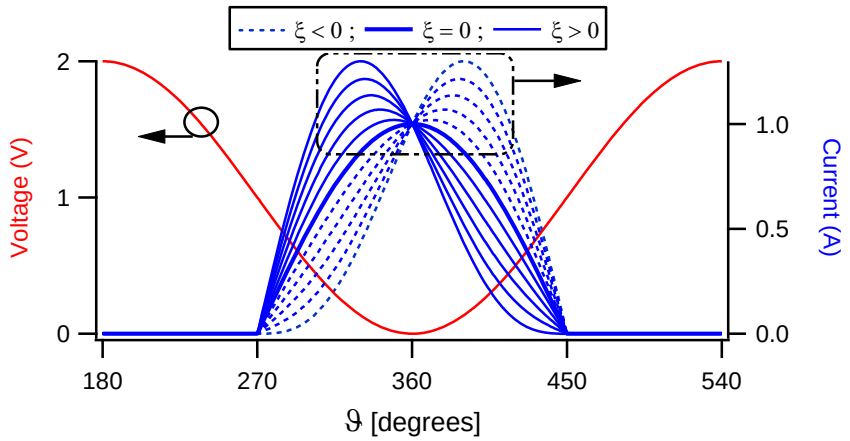

Fig. 3.18 – Theoretical Continuous Class-BI voltage and current waveforms for ξ varying between $-1 \leq \xi \leq 1$ in steps of 0.2.

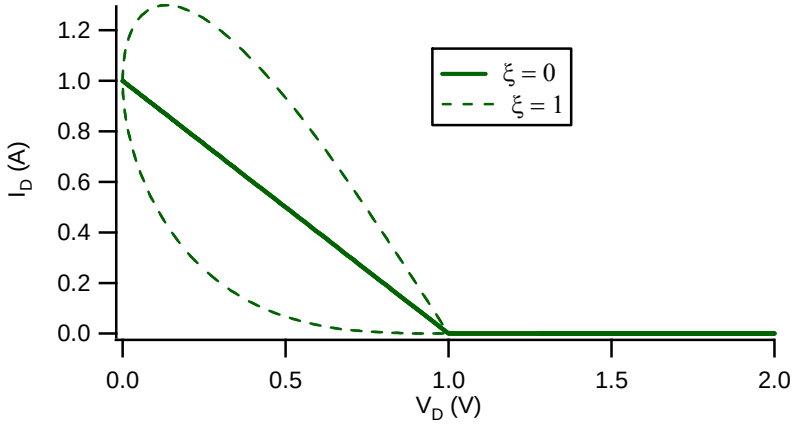

Fig. 3.19 – Theoretical Continuous Class-BI load-lines for ξ=0 and ξ=1 (ξ=-1 is the symmetric load-line of ξ=1).

Again, by FFT voltage and current components, fundamental and second harmonic terminations (here shown as admittances) can be calculated as shown in (3.50) and (3.51).

$$Y_{F0} = G_{F0} + j \cdot \xi \cdot 0.424 \cdot G_{F0}\,, \tag{3.50}$$

$$Y_{2F0} = short - circuit\,. \tag{3.51}$$

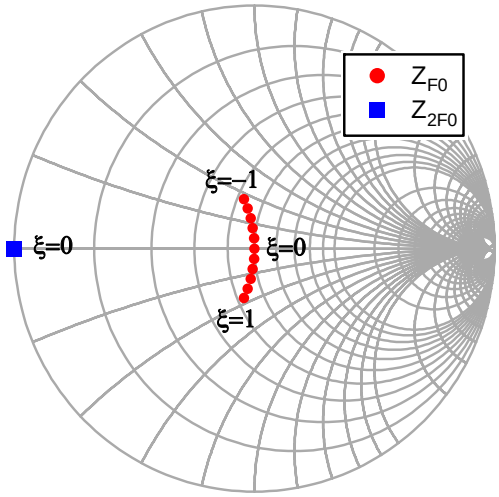

Fig. 3.20 – Theoretical Continuous Class-BI fundamental and second harmonic impedances for ξ varying between $-1 \leq \xi \leq 1$ in steps of 0.2.

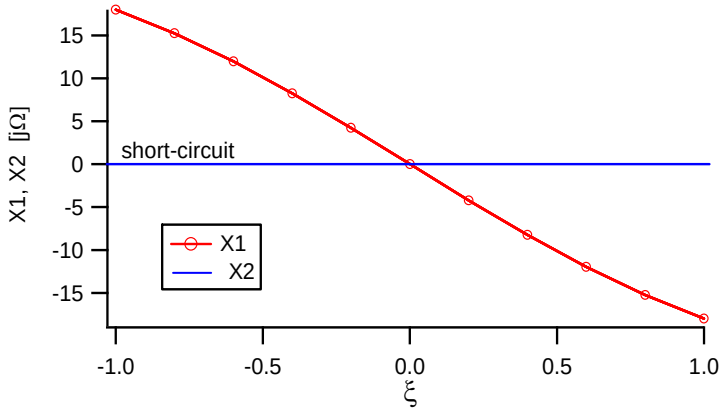

Fig. 3.21 – Theoretical Continuous Class-BI fundamental and second harmonic reactance X1 and X2 for ξ varying between $-1 \leq \xi \leq 1$ in steps of 0.2.

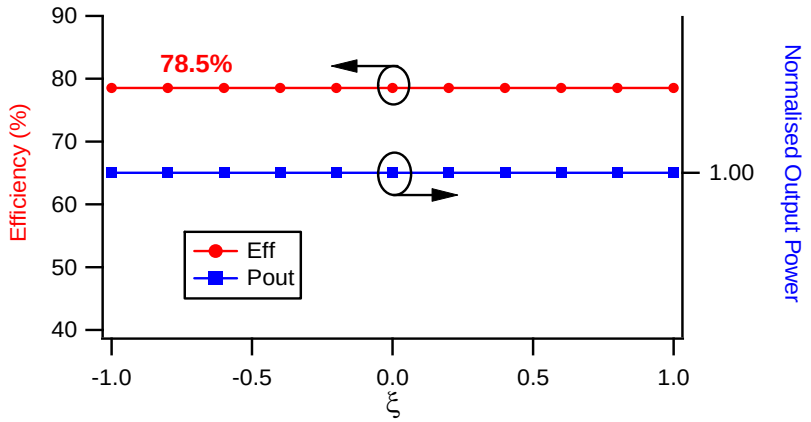

Fig. 3.22 – Theoretical Continuous Class-BI drain efficiency and normalised output power for ξ varying between $-1 \leq \xi \leq 1$ in steps of 0.2.

It is interesting to observe that here the range of the fundamental reactive variation (Fig. 3.20) is smaller if compared with both the Continuous Class-AV (Fig. 3.4), Continuous Class-AI (Fig. 3.10) and Continuous Class-BV (Fig. 3.15) cases. This is due to the fact that when applying the Continuous theory to the current waveform smaller variation of the waveforms are observed.

3.7 Continuous Class-FV Mode

For the cases so far described, only a range of fundamental loads has been revealed for both the Continuous/broadband Class-A modes where varying the voltage and current waveforms as well as the Continuous Class-BI case. However, for Continuous/broadband Class-BV case both fundamental and second harmonic impedance variations have been observed. In all these cases, it was assumed that the higher harmonic impedances (greater than 2) were short-circuited.

The starting point of the "*Continuous Class-FV*" mode [19] is the conventional Class-F condition [1, 30, 31]. Here a half-wave rectified sinusoidal current waveform is presented by biasing the device at its pinch-off and a square voltage waveform is revealed by presenting the optimum fundamental load, short-circuit even harmonics and open-circuit odd harmonic contents. For this analysis, the ideal half wave rectified sinusoidal current waveform (considering infinite harmonic contents) while the truncated four harmonics square voltage waveform will be considered.

Equation (3.52) identifies the ideal half-wave rectified sinusoidal current waveform when taking into account infinite harmonic contents.

$$\begin{aligned} i_{Cont\_FV}(\vartheta) &= I_{peak}\cos\vartheta \qquad 0<\vartheta<\pi/2,\quad (3/2)\pi<\vartheta<2\pi, \\ &= 0 \qquad\qquad\qquad\qquad \pi/2<\vartheta<(3/2)\pi \end{aligned} \tag{3.52}$$

where I_{peak} is the maximum peak current and θ is the conduction angle.

Equation (3.53) identifies the factorised representation of the truncated four harmonics square voltage waveform. Here the voltage waveform is allowed to vary

by applying the operator [1-δsinθ] while the current waveform shape is kept fixed half-wave rectified sinusoidal.

$$v_{Cont\_FV}(\vartheta)=\left(1-\frac{2}{\sqrt{3}}\cos\vartheta\right)^2\cdot\left(1+\frac{1}{\sqrt{3}}\cos\vartheta\right)\cdot[1-\delta\sin\vartheta] \tag{3.53}$$

For δ=0 the conventional Class-F voltage waveform is obtained, highlighted in red in Fig. 3.23. When varying the parameter δ between -1 and 1, the Continuous Class-FV family of voltage waveforms is revealed [19]. The load-lines are very similar to the Continuous Class-BV case (Fig. 3.14). Here, it can noted that higher voltage and current values are reached for δ=1. This is due to the fact that in order to obtain the square shape on the voltage waveform (for the standard case δ=0) a third harmonic component is introduced allowing an increase of fundamental voltage in order to reach the maximum swing. This leads to a higher fundamental current component in order to restore the initial reference fundamental impedance for the comparison with the other modes so far presented.

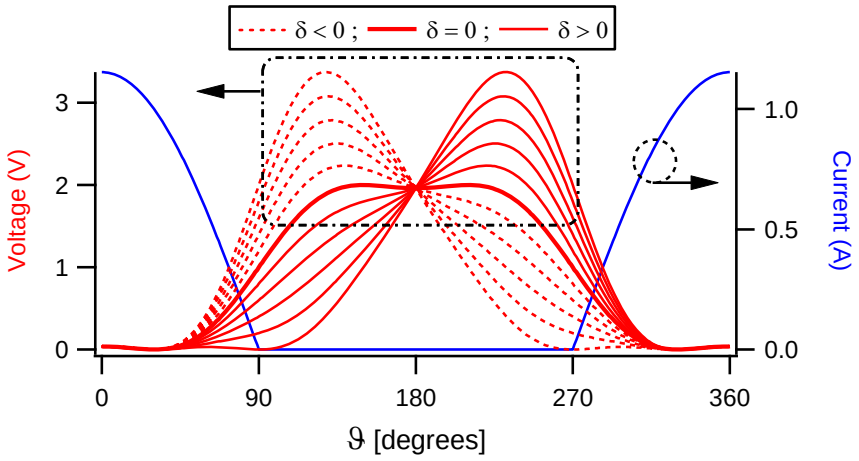

Fig. 3.23 – Theoretical Continuous Class-FV voltage and current waveforms for δ varying between $-1 \leq \delta \leq 1$ in steps of 0.2.

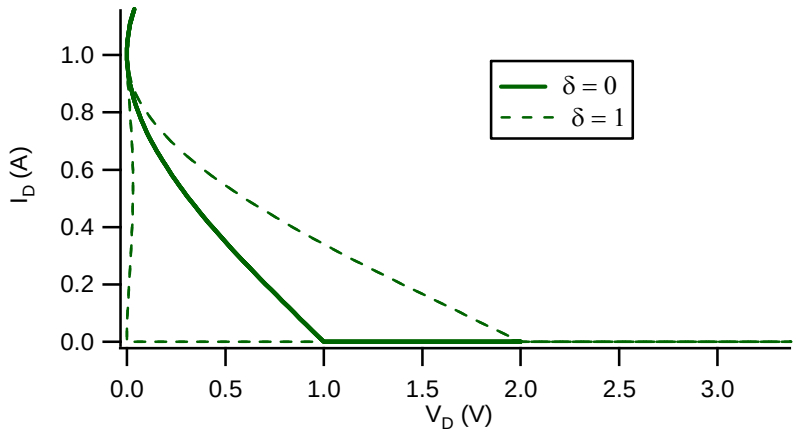

Fig. 3.24 – Theoretical Continuous Class-FV load-lines for δ=0 and δ=1 (δ=-1 is the symmetric load-line of δ=1).

It is important to highlight that for δ=0 the ideal efficiency of 90.7% can be achieved using first three harmonic impedances. When varying δ different than zero (again in the range -1÷1) equation (3.54) introduces a reactive component for the fourth harmonic voltage which can be demonstrated by its expansion:

$$v_{Cont\_FV}(\vartheta)=\left(1+\frac{4}{3\sqrt{3}}\cos^3\vartheta-\frac{3}{\sqrt{3}}\cos\vartheta\right)\cdot\left[1-\delta\sin\vartheta\right]. \tag{3.54}$$

Being:

$$\cos^3\vartheta=\frac{1}{4}\cos 3\vartheta+\frac{3}{4}\cos\vartheta\ , \tag{3.55}$$

leads to

$$v_{Cont\_FV}(\vartheta)=\left(1-\frac{2}{\sqrt{3}}\cos\vartheta+\frac{1}{3\sqrt{3}}\cos 3\vartheta\right)\cdot\left[1-\delta\sin\vartheta\right]. \tag{3.56}$$

As it can be noted, the first bracket of (3.56) is the conventional Class-F mode when taking into account first three harmonic impedances.

Further expansion of (3.46) leads to

$$v_{Cont\_FV}(\vartheta)=1-\frac{2}{\sqrt{3}}\cos\vartheta+\frac{1}{3\sqrt{3}}\cos 3\vartheta-\delta\sin\vartheta+$$
$$+\delta\frac{2}{\sqrt{3}}\sin\vartheta\cos\vartheta-\delta\frac{1}{3\sqrt{3}}\sin\vartheta\cos 3\vartheta. \tag{3.57}$$

Being:

$$\sin\vartheta\cos\vartheta=\frac{1}{2}\sin 2\vartheta \tag{3.58}$$

and

$$\sin\vartheta\cos 3\vartheta=\frac{1}{2}\sin 4\vartheta-\frac{1}{2}\sin 2\vartheta \tag{3.59}$$

the final expanded voltage waveform can be written as:

$$v_{Cont\_FV}(\vartheta)=1-\frac{2}{\sqrt{3}}\cos\vartheta-\delta\sin\vartheta+\frac{7}{6\sqrt{3}}\delta\sin 2\vartheta+\frac{1}{3\sqrt{3}}\cos 3\vartheta-\frac{\delta}{6\sqrt{3}}\sin 4\vartheta \tag{3.60}$$

Here the voltage waveform presents the first four harmonic components, where the second and fourth harmonics present only reactive components (sin terms). This means that the second and fourth harmonic components vary on the edge of the Smith chart (Γ=1) as a function of δ. Therefore, in order to keep the constant ideal efficiency of 90.7%, first four harmonic impedances must be taken into account when varying δ different than zero.

The DC voltage component is equal to unity while the fundamental and harmonic complex ones are described from (3.51) to (3.54):

$$V_{1cmplx}=-\frac{2}{\sqrt{3}}+j\cdot\delta, \tag{3.61}$$

$$V_{2cmplx}=0-j\frac{7}{6\sqrt{3}}\delta, \tag{3.62}$$

$$V_{3cmplx}=\frac{1}{3\sqrt{3}}-j\cdot 0, \tag{3.63}$$

$$V_{4cmplx}=0-j\frac{1}{6\sqrt{3}}\delta. \tag{3.64}$$

By dividing the complex voltage components with the appropriate current components achievable from the ideal half-wave rectified sinusoidal waveform, the first four harmonic impedances can be revealed as shown in (3.65), (3.66), (3.67) and (3.68) and in Fig. 3.25.

$$Z_{F0} = R_{F0} - j \cdot \frac{\sqrt{3}}{2} \cdot \delta \cdot R_{F0} \tag{3.65}$$

$$Z_{2F0} = 0 + j \cdot \delta \cdot 1.375 \cdot R_{F0} \tag{3.66}$$

$$Z_{3F0} = open - circuit \tag{3.67}$$

$$Z_{4F0} = 0 + j \cdot \delta \cdot 0.981 \cdot R_{F0} \tag{3.68}$$

As for the Class-BV mode, fundamental and second harmonic impedances are related to an inverse relationship, where by varying δ positively the fundamental reactance varies with negative sign and second harmonic reactance varies with positive sign. In this case the fourth harmonic reactance varies with positive sign but with different phase compared with the second harmonic load. The third harmonic impedance is kept open-circuited as the half wave rectified sinusoidal current waveform present ideally odd harmonics equal to zero.

Again, by presenting simultaneously the fundamental and harmonic impedances above described, constant output power (normalised to unity) and drain efficiency of 90.7% are achieved for the entire range of δ, which is translated to a wide range of frequencies allowing the design of broadband power amplifiers [32, 33], as it will be shown in Chapter 5.

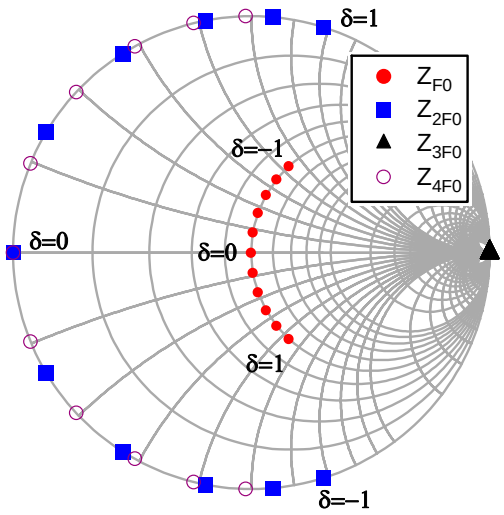

Fig. 3.25 – Theoretical Continuous Class-FV fundamental, second, third and fourth harmonic impedances for δ varying between $-1 \leq \delta \leq 1$ in steps of 0.2.

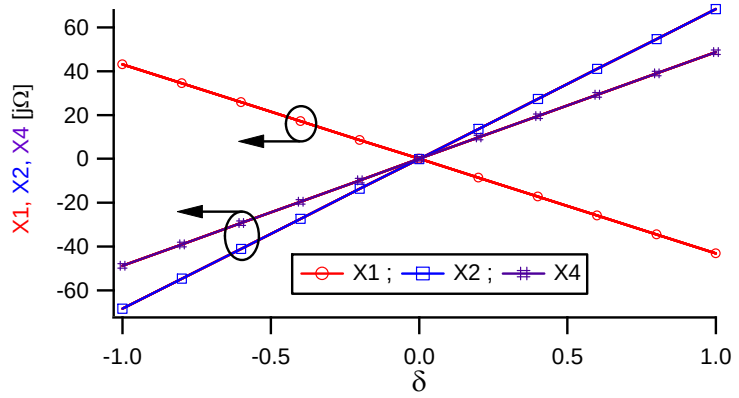

Fig. 3.26 –Theoretical Continuous Class-FV fundamental, second and fourth harmonic reactance X1, X2 and X4, for δ varying between $-1 \leq \delta \leq 1$ in steps of 0.2.

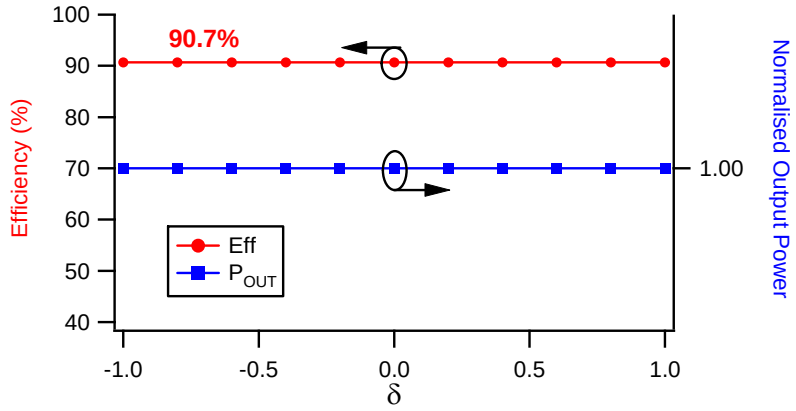

Fig. 3.27 – Theoretical Continuous Class-FV drain efficiency and normalised output power for δ varying between $-1 \leq \delta \leq 1$ in steps of 0.2.

In practical applications, the fourth harmonic component can be ignored. This is a good approximation as the impedance behaviour greater than three do not affect significantly the overall performance. Indeed the design of the output matching network in order to present the appropriate harmonic impedances is already challenging when considering the first three terminations, especially for a wide band of frequencies. In Chapter 5 it will be shown that by presenting appropriate ranges of fundamental, second and third harmonic impedances, where ignoring the fourth harmonic load, high power-efficiency states can be obtained for a very wide band of frequencies.

3.8 Continuous Class-FI Mode

The starting point of this mode termed *"Continuous Class-FI"* is the same than previous Continuous Class-FV case, which means that the current shape is half-wave rectified and the voltage is square. Here, this time it is the current to be varied from its initial shape by using the operator (1-$\xi\sin\theta$) while the voltage waveform is kept limited three harmonic square as shown in (3.69) and (3.70) respectively.

$$v_{Cont\_FI}(\vartheta) = 1 - \frac{2}{\sqrt{3}}\cos\vartheta + \frac{1}{3\sqrt{3}}\cos 3\vartheta\,, \tag{3.69}$$

$$\begin{aligned} i_{Cont\_FV}(\vartheta) &= \left(I_{peak}\cos\vartheta\right)\cdot\left[1-\xi\sin\vartheta\right] \quad (3/2)\pi < \vartheta < (5/2)\pi \\ &= 0 \qquad\qquad \pi < \vartheta < (3/2)\pi, \quad (5/2)\pi < \vartheta < 3\pi \end{aligned} \tag{3.70}$$

Fig. 3.28 shows the new family of Continuous Class-FI waveforms and the constant limited harmonic voltage waveform, with load-lines shown in Fig. 3.29. In this case there is no need to take into account the fourth harmonic impedance as for theoretical analysis of the Continuous Class-FV. This is because the constant limited three harmonic square voltage waveform provides only odd harmonics. Applying the FFT to both voltage and current waveforms and dividing the fundamental and harmonic voltage contents with the respective current components the impedances shown in Fig. 3.30 and 3.31 with their respective admittances also shown in equations (3.71), (3.72) and (3.73) are achieved. Here, the second harmonic load is kept constant while the new family of voltage waveforms are achieved by varying simultaneously fundamental load on the circle of constant susceptance and third harmonic load around the perimeter of the Smith chart from its open-circuit condition. Again, by varying the impedances just described in accordance with this theory, constant normalised output power and 90.7% of drain efficiency can be obtained as shown in Fig. 3.8.5. Besides, as in the previous cases, the two impedances that vary as a function of ξ are related from an inverse relationship. Increasing ξ the fundamental reactance decreases leading to an increase in fundamental susceptance while the third harmonic reactance increases leading to a decrease in third harmonic susceptance, as noted from Fig. 3.31.

$$Y_{F0} = G_{F0} + j \cdot \xi \cdot 0.421 \cdot G_{F0}, \tag{3.71}$$

$$Y_{2F0} = short - circuit, \tag{3.72}$$

$$Y_{3F0} = 0 - j \cdot \xi \cdot 1.516 \cdot G_{F0}, \tag{3.73}$$

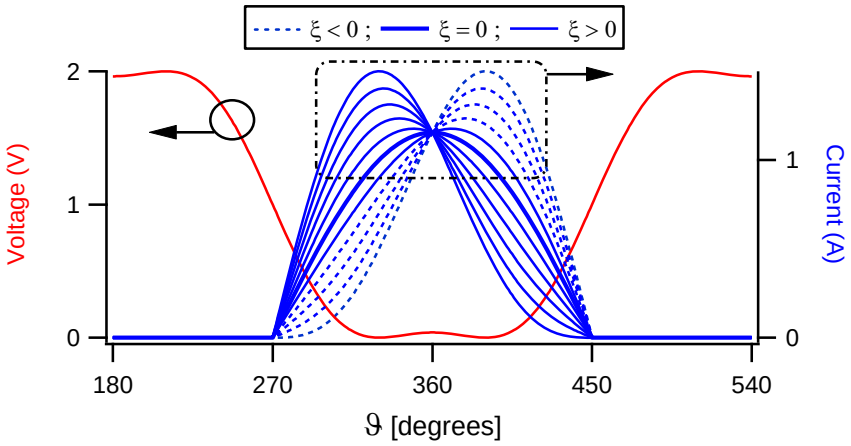

Fig. 3.28 – Theoretical Continuous Class-FI voltage and current waveforms for ξ varying between $-1 \leq \xi \leq 1$ in steps of 0.2.

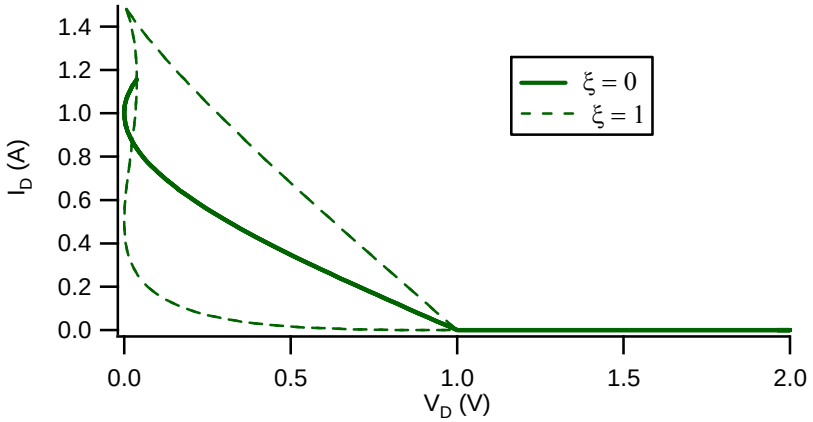

Fig. 3.29 – Theoretical Continuous Class-FI load-lines for ξ=0 and ξ=1 (ξ=-1 is the symmetric load-line of ξ=1).

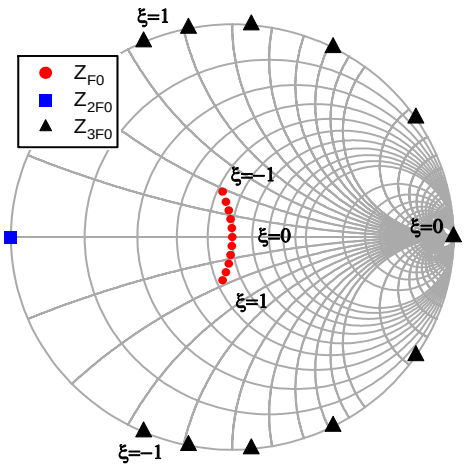

Fig. 3.30 – Theoretical Continuous Class-FI fundamental, second and third harmonic impedances for ξ varying between $-1 \leq \xi \leq 1$ in steps of 0.2.

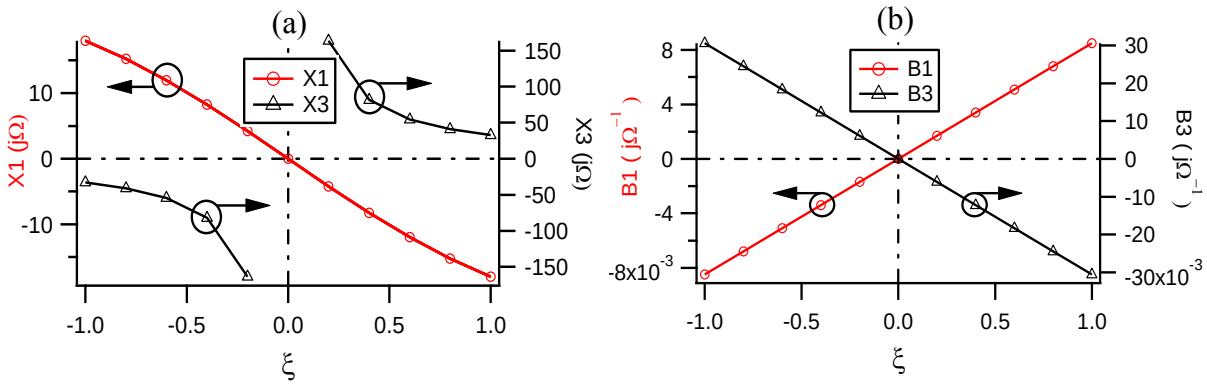

Fig. 3.31 – Theoretical Continuous Class-FI (a) fundamental and third harmonic reactance X1 and X3, and (b) fundamental and third harmonic susceptance B1 and B3, for ξ varying between $-1 \leq \xi \leq 1$ in steps of 0.2.

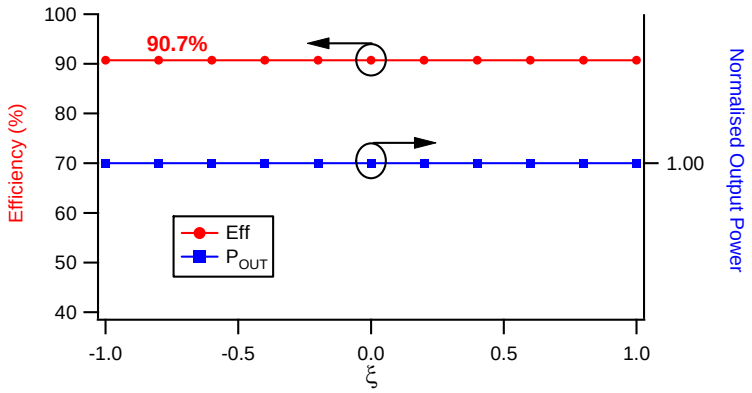

Fig. 3.32 – Theoretical Continuous Class-FI drain efficiency and normalised output power for ξ varying between $-1 \leq \xi \leq 1$ in steps of 0.2.

As for the continuous modes based on the Class-A and Class-B, when varying the current waveform a smaller range of fundamental impedance is achieved compared to one when varying the voltage waveform.

3.9 Continuous Inverse Class-FV (Continuous Class-FV^{-1}) Mode

The starting point of the "*Continuous Inverse Class-FV*" (Continuous Class-FV^{-1}) is the conventional Class-F^{-1} mode presented in Chapter 2, where the inverted Class-F waveforms are obtained by proper use of the harmonic terminations [1, 30, 31]. Here the ideal voltage waveform includes fundamental and even harmonic contents identifying a peaking second harmonic half-wave rectified sinusoidal waveform. The current waveform is obtained by biasing the device for which the quiescent current is half the maximum drain current (Class-A bias point) and by presenting odd harmonic contents, resulting in a square wave. In this case a limited 3 harmonic square current waveform will be assumed. The efficiency is equal to the Class-F when accounting for the same number of harmonics, but with greater output power and PUF, due to the higher peak voltage. In the Continuous Class-FV^{-1} mode the current waveform is maintained as a square wave (truncated third harmonic square) while the operator (1-$\delta\sin\theta$) is applied to the voltage as shown in (3.74), revealing the new Continuous ClassFV^{-1} waveforms shown in Fig. 3.33 with the load-lines provided in Fig. 3.34 [34-35].

The overall drain efficiency would be 90.7% if considering two harmonic contents in the voltage waveform and infinite harmonic contents on the current waveform where presenting the perfect square current shape. In this case, finite harmonic components have been considered in both voltage (two harmonic contents) and current (three harmonic contents) waveforms leading to a drain efficiency of 81.7%.

$$v_{Cont\_FV^{-1}}(\vartheta)=\left(\frac{1}{\sqrt{2}}-\cos\vartheta\right)^2\cdot\left[1-\delta\sin\vartheta\right]$$

$$=\left(1-\sqrt{2}\cos\vartheta+\frac{1}{2}\cos 2\vartheta\right)\cdot\left[1-\delta\sin\vartheta\right] \quad (3.74)$$

$$=1-\sqrt{2}\cos\vartheta-\frac{3}{4}\delta\sin\vartheta+\frac{1}{2}\cos 2\vartheta+\frac{\sqrt{2}}{2}\delta\sin 2\vartheta-\frac{\delta}{4}\sin 3\vartheta, \quad (3.75)$$

$$i_{Cont\_FV^{-1}}(\vartheta) = i_{DC} + a\cos\vartheta + b\cos 2\vartheta - c\cos 3\vartheta\,, \tag{3.76}$$

where in this case for maintaining the 50 Ω fundamental optimum impedance: i_{DC}=1.22, a=√2, b=0 and c=0.23, with a, b and c being fundamental (i_1), second (i_2) and third (i_3) harmonic current components.

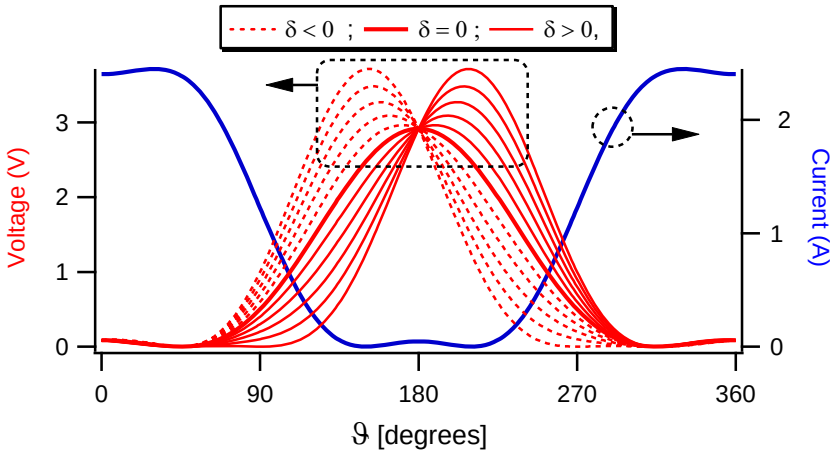

Fig. 3.33 – Theoretical Continuous Class-FV^{-1} voltage and current waveforms for δ varying between $-1 \le \delta \le 1$ in steps of 0.2.

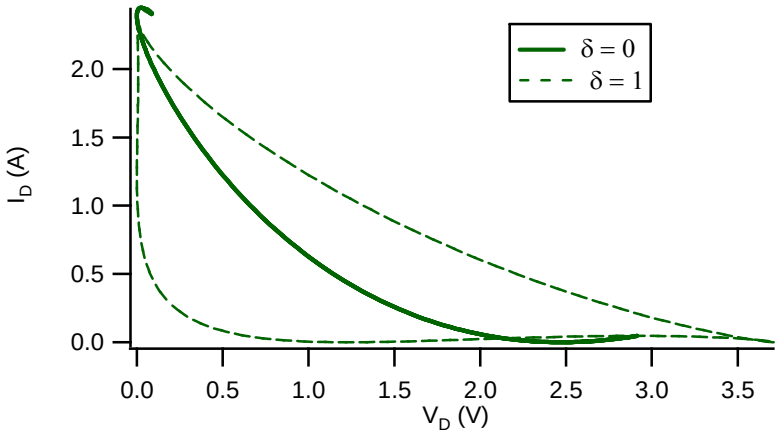

Fig. 3.34 – Theoretical Continuous Class-FV^{-1} load-lines for δ=0 and δ=1 (δ=-1 is the symmetric load-line of δ=1).

The complex voltage components are:

$$V_{1cmplx} = -\sqrt{2} + j\frac{3}{4}\delta \tag{3.77}$$

$$V_{2cmplx} = \frac{1}{2} - j\frac{\sqrt{2}}{2}\delta \tag{3.78}$$

$$V_{3cmplx} = 0 + j\cdot\frac{\delta}{4} \tag{3.79}$$

Therefore, supposing a band limited square current waveform, fundamental and harmonic impedances are:

$$Z_{F0} = R_{F0} - j \cdot \delta \cdot 0.53 \cdot R_{F0}, \tag{3.80}$$

$$Z_{2F0} = open-circuit, \tag{3.81}$$

$$Z_{3F0} = 0 - j \cdot \delta \cdot 1.06 \cdot Z_{F0} \tag{3.82}$$

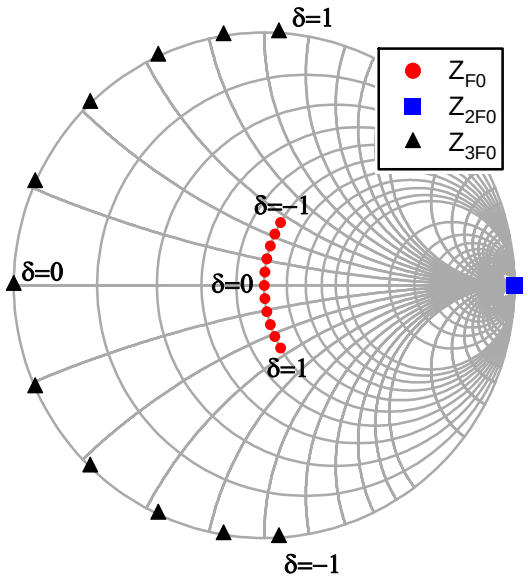

Fig. 3.35 – Theoretical Continuous Class-FV^{-1} fundamental, second and third harmonic impedances for δ varying between -1 ≤ δ ≤ 1 in steps of 0.2.

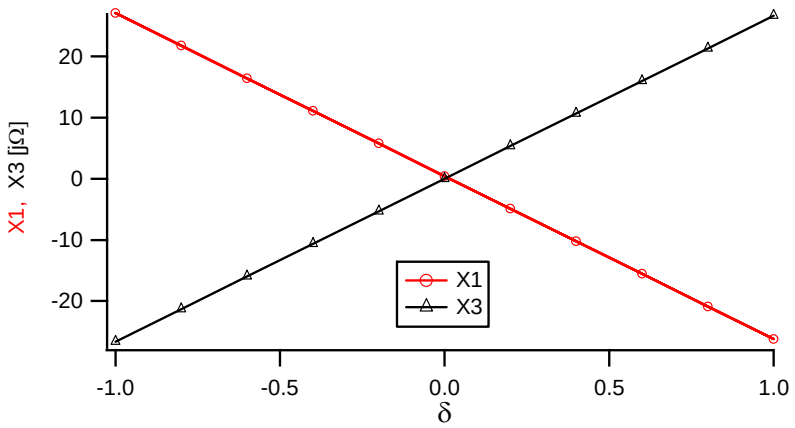

Fig. 3.36 – Theoretical Continuous Class-FV^{-1} fundamental and third harmonic reactance X1 and X3 for δ varying between -1 ≤ δ ≤ 1 in steps of 0.2.

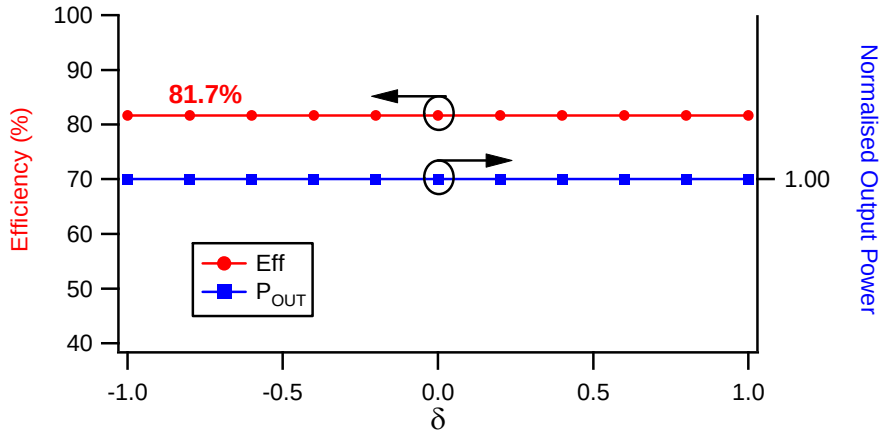

Fig. 3.37 – Theoretical Continuous Class-FV^{-1} drain efficiency and normalised output power for δ varying between $-1 \leq \delta \leq 1$ in steps of 0.2.

In this case the fundamental load varies on its circle of constant resistance while the third harmonic termination varies on the edge of the Smith chart from the short-circuit condition while the second harmonic load is fixed open-circuited. As in the previous cases the output performance is maintained constant (Fig 3.37).

3.10 Continuous Inverse Class-FI (Continuous Class-FI^{-1}) Mode

The last Continuous mode presented in this Chapter is what is called *"Continuous Inverse Class-FI"* (Continuous Class-FI^{-1}) [21]. The starting point is again the conventional Class-F^{-1} condition and the new waveforms are exploited on the current side. Again, the parameter ξ must be varied between -1 and 1, as in all the other modes previously presented. Here, both waveforms have been assumed to be harmonically limited to the third content. Starting from the limited square current waveform, the new family of waveforms is revealed when varying ξ, presenting higher peaks (compared with the standard one) while maintaining a constant harmonic limited voltage waveform, as shown in Fig. 3.38 with load-lines presented in Fig. 3.39.

$$v_{Cont\_FI^{-1}}(\vartheta) = \left(\frac{1}{\sqrt{2}} - \cos\vartheta\right)^2$$

$$= \frac{1}{2} + \cos^2\vartheta - \frac{2}{\sqrt{2}}\cos\vartheta \,. \qquad (3.83)$$

Being

$$\cos^2 \vartheta = \frac{1+\cos 2\vartheta}{2}, \tag{3.84}$$

equation (3.83) expands into

$$v_{Cont\_FI^{-1}}(\vartheta) = 1 - \frac{2}{\sqrt{2}}\cos\vartheta + \frac{1}{2}\cos 2\vartheta, \tag{3.85}$$

while the current formulation is

$$i_{Cont\_FI^{-1}}(\vartheta) = \left(i_{DC} + i_1 \cos\vartheta + i_2 \cos 2\vartheta - i_3 \cos 3\vartheta\right)\cdot\left[1 - \xi \sin\vartheta\right], \tag{3.86}$$

where i_{DC}=1.22, i_1=√2, i_2=0 and i_3=0.203, in order to restore for the conventional case the same optimum fundamental load of 50 Ω.

The expansion of the current formulation leads to

$$i_{Cont\_FI^{-1}}(\vartheta) = i_{DC} + i_1 \cos\vartheta - i_{DC}\,\xi \sin\vartheta - \frac{\xi}{2}(i_1 + i_3)\sin 2\vartheta +$$

$$- i_3 \cos 3\vartheta + i_3 \frac{\xi}{2}\sin 4\vartheta\,. \tag{3.87}$$

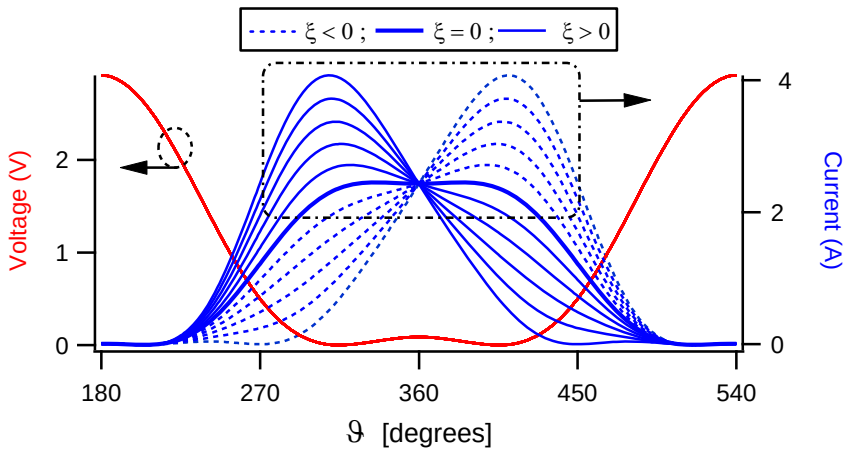

Fig. 3.38 – Theoretical Continuous Class-FI^{-1} voltage and current waveforms for ξ varying between $-1 \le \xi \le 1$ in steps of 0.2.

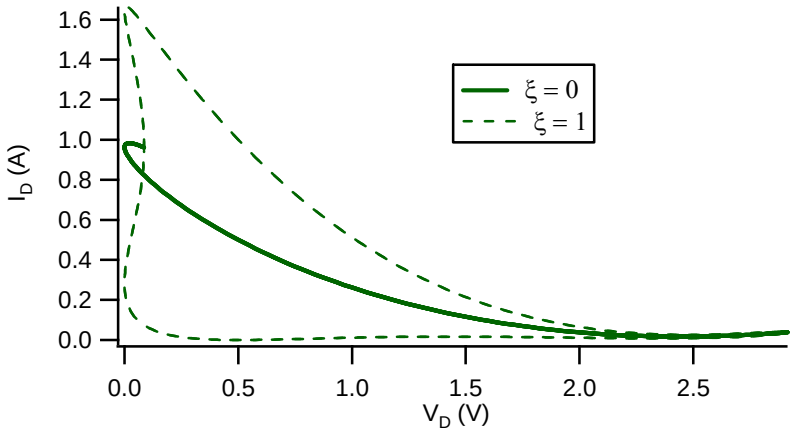

Fig. 3.39 – Theoretical Continuous Class-FI^{-1} load-lines for ξ=0 and ξ=1 (ξ=-1 is the symmetric load-line of ξ=1).

The fundamental and harmonic voltage and current components are:

$$V_{DC} = 1, \tag{3.88}$$

$$V_{1cmplx} = -\sqrt{2}, \tag{3.89}$$

$$V_{2cmplx} = \frac{1}{2}, \tag{3.90}$$

$$V_{3cmplx} = 0, \tag{3.91}$$

$$I_{DC} = 1.22, \tag{3.92}$$

$$I_{1cmplx} = \sqrt{2} + j \cdot 1.22 \cdot \xi, \tag{3.93}$$

$$I_{2cmplx} = 0 + j \cdot 0.808 \cdot \xi, \tag{3.94}$$

$$I_{3cmplx} = -0.203, \tag{3.95}$$

$$I_{4cmplx} = 0 - j \cdot 0.101 \cdot \xi. \tag{3.96}$$

The fundamental, second and third harmonic impedances will be:

$$Z_{F0} = \frac{2}{2+1.488 \cdot \xi^2} \cdot R_{F0} - j \frac{\xi \cdot 1.725}{2+1.488 \cdot \xi^2} \cdot R_{F0}, \tag{3.97}$$

$$Z_{2F0} = 0 + j \cdot 0.618 \cdot \xi \cdot R_{F0}, \tag{3.98}$$

$$Z_{3F0} = short-circuit, \tag{3.99}$$

with the admittances reported in equations from (3.100) to (3.102):

$$Y_{F0} = G_{F0} + j \cdot \xi \cdot \frac{\sqrt{3}}{2} \cdot G_{F0}, \tag{3.100}$$

$$Y_{2F0} = 0 + j \cdot \xi \cdot 1.615 \cdot G_{F0}, \tag{3.101}$$

$$Y_{3F0} = short - circuit. \tag{3.102}$$

As for the Continuous Inverse Class-FV case, for δ=0 the conventional Class-F^{-1} first three harmonic terminations are obtained. Here the optimum fundamental load of 50 Ω, open-circuit and short-circuit second and third harmonic terminations are achieved respectively. As it can be noted from Fig. 3.40 and 3.41, when varying ξ the fundamental admittance varies on its circle of constant conductance while simultaneously the second harmonic termination varies around the perimeter of the Smith chart from the open-circuit condition. Again, in order to maintain the same constant output power and drain efficiency of 81.7% (assuming in this case 3 harmonic components in both voltage and current components) shown in Fig. 3.42, fundamental and second harmonic terminations are related to an inverse relationship where the positive variation of fundamental suceptance is accompanied by a negative variation of second harmonic suceptance (Fig. 3.42 b) with the third harmonic load kept short-circuited.

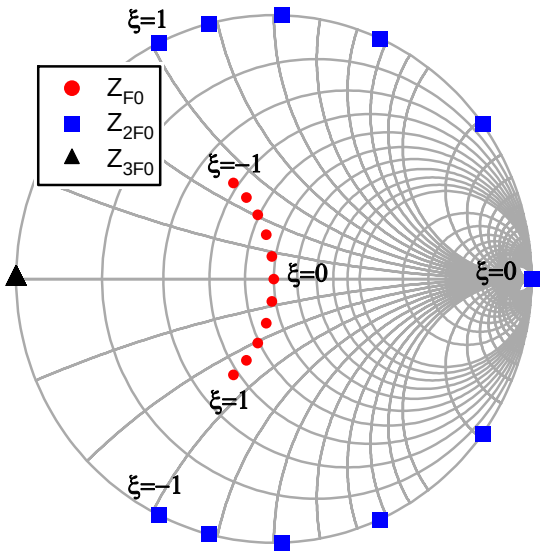

Fig. 3.40 – Theoretical Continuous Class-FI^{-1} fundamental, second and third harmonic impedances for ξ varying between -1 ≤ ξ ≤ 1 in steps of 0.2.

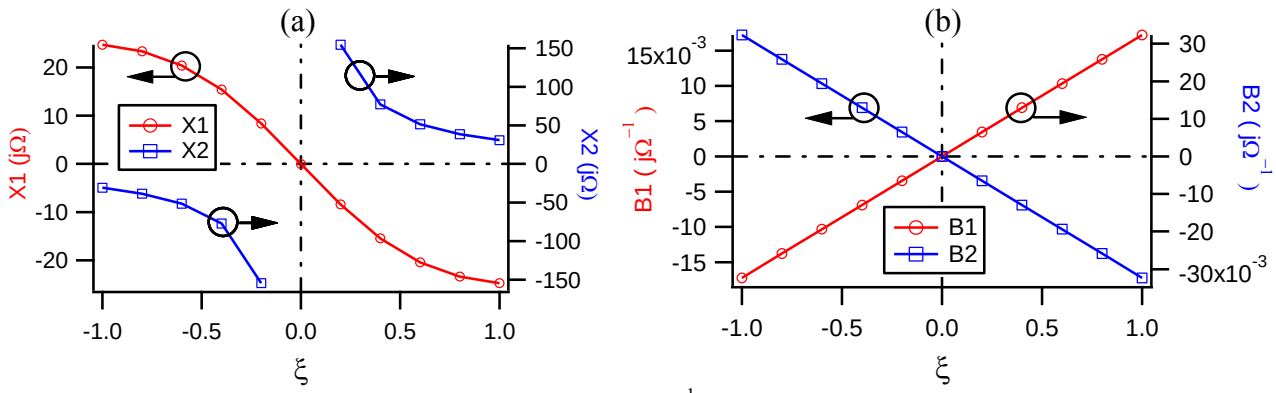

Fig. 3.41 – Theoretical Continuous Class-FI^{-1} fundamental and second harmonic reactance X1 and X1 (a), and fundamental and second harmonic susceptance B1 and B2, for ξ varying between $-1 \leq \xi \leq 1$ in steps of 0.2.

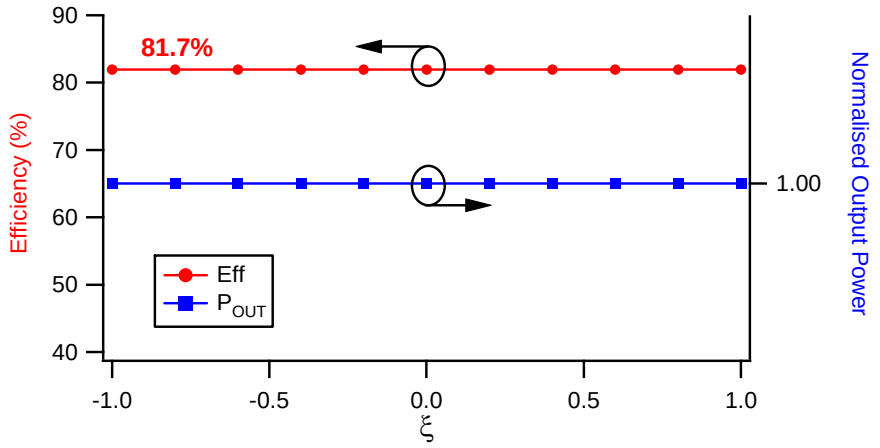

Fig. 3.42 – Theoretical Continuous Class-FI^{-1} drain efficiency and normalised output power for ξ varying between $-1 \leq \xi \leq 1$ in steps of 0.2.

3.11 Chapter Summary

This Chapter has presented the theoretical background defining for the first time the broadband "Continuous Modes". Such novel modes have been applied to the conventional narrow band Class-A, Class-B, Class-F and Class-F^{-1} classes.

Nowadays, the emerging wireless communication networks need wide frequency bands in order to provide the advanced services. This has led the PA community to invest more resources and effort for the investigation of broadband PAs used in the wireless communications.

The novel Continuous theory has demonstrated that the well-known conventional narrow band modes can now be used for wide band applications. Through the factorial representation of the voltage and current waveforms it has been demonstrated that different combinations of fundamental and harmonic impedance solutions for which the output performance does not degrade are obtained. By presenting these appropriate harmonic load solutions, a new family of voltage or current waveforms are revealed maintaining a theoretical constant output performance in terms of power and drain efficiency. It will be demonstrated later on this thesis that the different set of fundamental and harmonic solutions are then translated into a wide design space in the frequency domain, allowing the design of highly power-efficient amplifiers for a wideband of frequencies.

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Chapter 4

Conventional and Continuous Class-F Measurements

4.1 Introduction

In this Chapter 4 the experimental verification of the standard Class-F mode, as well as the new Continuous Class-FV mode power amplifier will be explored. Initially, a developed waveform engineering design procedure where all the different parameters (bias, input power and impedances) are manually adjusted in order to optimise a Class-F design is presented. In this case many measurement iterations involving constant human interactions have been done, in order to provide the device's best performance. After this, it will be demonstrated that starting from minimal DC information about the device itself and using a theoretical predictor it is possible to speed up the measurement activity saving valuable time. Here for the first time the theoretical predictor uses the "Waveform Engineering Postulator" concept in order to achieve targeted waveforms and thus obtain the desired output performance. In addition, for the first time it will be shown through measurement results that once the standard Class-F mode is obtained, by varying properly the fundamental and harmonic impedances, as

theoretically explained in Chapter 2, the Continuous Class-FV output impedance solutions where the optimum output performance is maintained can be revealed.

4.2 Class-F Measurements

4.2.1 Practical Design Limitations

As described in Chapter 2 of this thesis and well known from the general literature review [1-4], the Class-F power amplifier presents a half-wave rectified sinusoidal current waveform and a square voltage waveform at the device current-generator plane $I_{GEN\text{-}PLANE}$ [5]. Here, the theoretical drain efficiency can ideally be 100% [6] when accounting for infinite harmonic content in both current and voltage waveforms and when not considering other non-ideal effects such as the knee voltage. However, the efficiency starts to decrease when dealing with real devices due to practical limitations. The process described in this paragraph will show the actual steps required in order to optimise the overall device performance when working with real devices.

The first limitation is due to the number of harmonics that can be taken into account, this is simply called "*harmonic limitation*". As already said, for the achievement of the ideal 100% efficiency, infinite harmonic content should be taken into account. In reality it is not possible to control the entire spectral content as the complexity and cost would be prohibitive.

The efficiency of a real device is described by two factors: $\eta_{voltage}$ and $\eta_{current}$, which are the ratio between the fundamental voltage and current with the DC voltage and current components respectively [7], as shown in 4.1 and 4.2.

$$\eta_{voltage} = \frac{v_{RF}}{\sqrt{2} \cdot V_{DC}}, \tag{4.1}$$

$$\eta_{current} = \frac{i_{RF}}{\sqrt{2} \cdot I_{DC}}. \tag{4.2}$$

Where $\eta_{voltage}$ is the voltage efficiency describing the voltage harmonic content limitation and $\eta_{current}$ is the current efficiency describing the current harmonic content limitation.

Therefore, the actual overall efficiency will be function of the number of harmonics utilised as shown in (4.3) and Table 4.I

$$\eta_{ideal} = \eta_{current} \cdot \eta_{voltage} = \frac{i_{RF}}{\sqrt{2} \cdot I_{DC}} \frac{v_{RF}}{\sqrt{2} \cdot V_{DC}} \tag{4.3}$$

TABLE 4.I
CLASS-F OPTIMUM DRAIN EFFICIENCY AS A FUNCTION OF UTILISED HARMONICS

	Class-F Efficiency (%)			
N	**M=1**	**M=3**	**M=5**	**M=∞**
1	50	57.7	60.35	63.66
2	70.71	81.6	85.35	90.03
4	75	86.54	90.52	95.48
∞	78.54	90.63	94.8	100

When considering infinite harmonics on both the current and voltage waveforms, $\eta_{voltage} = \eta_{current} = 1$, resulting in an ideal efficiency of 100%, again shown in Table 4.I. If decreasing the harmonic content on the voltage waveform from infinite to five, while still presenting infinite content on the current waveform, the efficiency decreases down to 94.8% [1, 8]. In the measurement system used in Cardiff University [9], first three harmonic contents can be controlled; this means that the maximum drain efficiency achievable can be approximately 90.6%.

However, even if the first three harmonic impedances can be controlled and manipulated, the 90.6% of efficiency still cannot be reached due to the second practical limitation called "*DC offset limitation*" η_{offset}, as shown in (4.4).

The DC offset is due to the achievable minimum current and voltage values (I_{min} and V_{min}), which are not zero. This makes a fraction of DC power unavailable for the RF power conversion, resulting in a reduction of overall efficiency.

$$\eta_{offset} = \left(1 - \frac{V_{knee}}{V_{DC}}\right)\left(1 - \frac{I_{\min}}{I_{DC}}\right) \tag{4.4}$$

In real devices the minimum achievable current can be close to the zero value, while most of the efficiency degradation is actually due to the minimum voltage also known as the knee voltage V_{knee} [1]. The offset efficiency formulation is presented in (4.5), which clearly shows that if minimum current and voltage values

I_{min} and V_{knee} are greater than zero, the η_{offset} is smaller than 1. Supposing that 10% of the overall DC to RF power conversion is loss due to the knee voltage, this results in η_{offset} =0.9.

The overall efficiency η can thus be calculated as

$$\eta = \eta_{voltage} * \eta_{current} * \eta_{offset} . \quad (4.5)$$

Therefore, considering that the measurement system can control up to three harmonic impedances and supposing that the offset limitation is approximately around 0.9, the actual device overall efficiency achievable will be

$$\eta = \eta_{voltage} * \eta_{current} * \eta_{offset} = 0.906 * 0.9 \cong 81\% . \quad (4.6)$$

This value of efficiency around 80% is quite common for a compressed (from 1 to 3 dB gain compression) Class-F power amplifier realisation [10].

These practical limitations are very important to understand when designing power amplifiers, as without any knowledge of the actual number of harmonics used and especially without knowledge of the devices itself it is not possible to quantify how successful the design has been.

4.2.2 Manual Class-F Measurements

The first step in achieving the Continuous Class-F mode is the conventional narrow band Class-F condition. Therefore, before the broadband/Continuous Class-F mode can be presented, it is important to describe the systematic approach [11 and Appendix D] used on the measurement activity in order to provide the optimum standard high efficient Class-F PA design through waveform engineering [12-13].

This approach is based on a systematic methodology which consists of a "manual search" of the best combination of bias condition V_G, input power P_{IN} fundamental and harmonic impedances Z_{F0}, Z_{2F0} and Z_{3F0} in order to achieve the target high efficient Class-F condition. This "manual search" can take many measurement iterations involving constant human interaction, but provides and ensures the best device's performance as the different parameters are continuously adjusted [8, 11].

Measurements have been performed on a wafer-probeable 2 fingers HFET GaN power transistor from QinetiQ with gate width Wg=50 μm and gate length Lg=0.6 μm, operating at 15 V supply voltage, 0.9 GHz fundamental frequency and delivering around 23 dBm of output power. The measurements have been carried out using the active envelope load-pull (ELP) measurement system developed at Cardiff University and already presented in Chapter 2. By using a software environment called Igor (available from WaveMetrics) developed at Cardiff University, measurements can be performed at the measurement plane as well at the device $I_{GEN-PLANE}$ by de-embedding the drain source capacitor C_{DS}. The value of C_{DS} is again achieved by using the same Igor software. Here, the software runs different values of C_{DS} leading to different current waveforms. Therefore, the software compares each waveform with an ideal (in this case) half wave rectified sinusoidal class-B waveform. The waveform which is closer in shape to the ideal half-wave sinusoidal waveform is the one for which the C_{DS} is achieved, in this case C_{DS}=0.04 pF [14].

The half-wave rectified sinusoidal current waveform is achieved with addition of even order Fourier contents generated by the device at its pinch-off point (V_{TH}), where for this device V_{TH}=-5.5 V. This means that by biasing the device at its pinch-off $V_{GS}=V_{TH}$ the third harmonic content (or odd harmonic content, when considering higher harmonics) should be equal to zero, providing the desired current shape.

Therefore, by presenting a $V_{GS}=V_{TH}$ and short-circuit second and third harmonic impedances it is possible to vary simultaneously the drive power and the fundamental impedance in order to find the combination where the drain efficiency is maximised or the best trade-off between power, efficiency and gain is revealed. In this case fundamental impedance Z_{F0}=400+j0 Ω and input power P_{IN}=16 dBm have been found at the $I_{GEN-PLANE}$ for which the device was approximately at 1 dB of gain compression.

This condition is what in this case has been called “pseudo” Class-B condition. This is due to the fact that, although the theoretical the Class-B state is achieved when biasing the device at its pinch-off, in real measurements lower gate bias

voltage are often revealed, where the device tries to go into its "relaxation" mode [8, 12] through the right bias condition.

Fig. 4.1 shows the plot of the third harmonic current function of the bias point V_{GS}. Here, it can be noted that the bias point which minimises the third harmonic current is not the actual pinch-off value V_{TH}=-5.5 V, but slightly lower at V_{GS}=-5.6 V. This can be due to the non-unilateral device characteristic also due to the feedback capacitor as well as the non-linear C_{GS} capacitor behaviour [15-16].

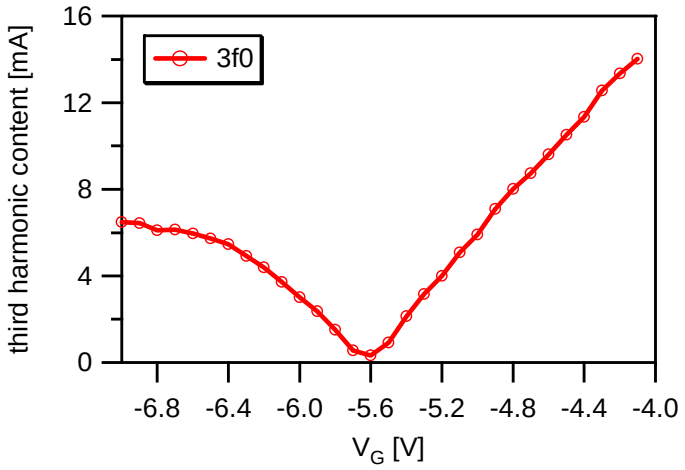

Fig. 4.1 – Measured third harmonic current function of bias voltage.

It is important to highlight that the definition of Class-B bias point of V_{GS}=V_{TH} is valid for the ideal analysis, as the third harmonic current in null. When dealing with real devices it has been demonstrated that the zero third harmonic current can be reached by presenting a bias point lower than pinch-off, still delivering the expected output power, as shown in Fig. 4.2. Once the right bias voltage is obtained, while still presenting short-circuit second and third harmonic terminations, the fundamental impedance can be varied and the actual Class-B condition with the half-wave rectified sinusoidal current waveform and the sinusoidal voltage waveform can be revealed.

The next step is to engineer the voltage waveform towards a square shape thus presenting the Class-F condition. The square voltage waveform is achieved with odd Fourier components resulting from the open circuit termination, which ideally leads to even harmonic voltages equal to zero. In fact, once the current waveform has been selected, harmonic tuning is performed to engineer the voltage waveform.

Leaving the second harmonic impedance at a short-circuit and presenting an open-circuit third harmonic impedance a square-like voltage waveform is revealed. The increase in third harmonic voltage is accompanied by an increase in the fundamental voltage. This means that, in order to maintain a constant fundamental current waveform, when using three harmonics the first harmonic impedance must be increased by a factor of $2/\sqrt{3}$ (approx. 1.154) [1] as shown in Table 2.IV of Chapter 2. Table 4.II and Table 4.III show the Class-F optimum fundamental and harmonic impedances and the output performance at around 2 dB of gain compression. Indeed, Fig. 4.2 shows the behaviour of drain efficiency (η), power added efficiency (PAE), output power (P_{OUT}) and transducer power gain (G_T) function of the input power.

TABLE 4.II
CLASS-F FIRST THREE OPTIMUM HARMONIC IMPEDANCES

Z(f0)	Z(2f0)	Z(3f0)
$0.85\angle 0^o$	$1\angle 179^o$	$1\angle 6^o$

TABLE 4.III
CLASS-F OUTPUT PERFORMANCE

η [%]	P_{OUT}[dBm]	PAE[%]	Gain [dB]
81.02	23.57	78.99	10

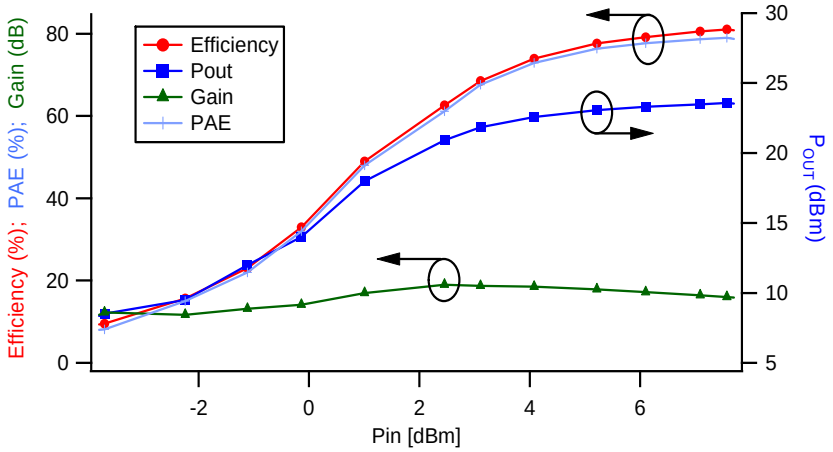

Fig. 4.2 – Measured drain efficiency, PAE, output power and transducer power gain function of the input power sweep.

The plots in Fig. 4.3 show the Class-F voltage and current waveforms (left) as well as the load-lines (right) for different power sweeps. Optimum waveforms are highlighted in red where P_{OUT}=23.57 dBm and drain efficiency η=81.02%.

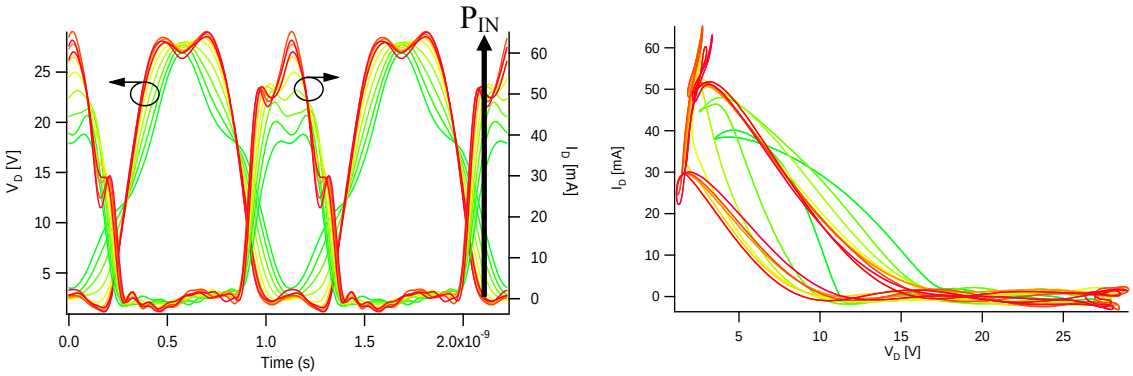

Fig. 4.3 – Measured voltage and current waveforms and load-lines function of P_{IN}.

4.2.3 Speeding-Up the Measurement Activity

The importance of minimizing the time required for the characterization of modern microwave devices, such as those used in the RF Power Amplifier (RFPA) has become critical as it allows manufacturers to gain a competitive advantage.

An established and preferred approach in designing RFPAs is based on non-linear device modelling, where CAD and well-defined device models are used to reduce and ideally eliminate measurement complexity, reducing to a minimum the number of measurements needed to achieve a required or target performance.

However, device models, or sufficiently accurate device models, tend not to be available for the emerging and highly promising device technologies that may be of interest to future PA designers.

Another approach which will not be discussed in this thesis and discussed elsewhere [16-21] is based on "X-parameters". This approach uses the combination of large signal measurements and the CAD approach. Once the large signal measurements are obtained, the CAD simulator can load and use such data to facilitate the PA design.

The alternative design approach is based on direct device measurement and specifically conducting fundamental and harmonic load-pull measurements, possibly at different drive and bias levels and with the design targets usually being

drain efficiency, output power and gain [Appendix D]. As shown in the previous paragraph and in other papers [8, 11, 22], this approach reveals the best design condition but demands significant microwave measurements and involves a high degree of human interaction over a significant time frame.

Here, an intermediate design and optimisation process that lies somewhere between simple modelling and the measurements world, where by combining the two approaches and taking the benefit of both, will be described. Obviously the device cannot be perfectly described using a simple model, but using simple information of the device itself it is shown how measurement and characterisation time can be substantially reduced. The advantage of using an analytical procedure, in this case IGOR software from WaveMetrics [23], is to achieve quick results (without any further simulation). Such results can directly guide and control the load-pull system, indicating the first guess toward the measured optimum output performance [24] [software panels described in Appendix E]. The approach described in this paper is divided into two stages. The first stage involves the extrapolation of simple DC parameters from DCIV measurement data. The DCIV measurements have been conducted by using a voltage supply together with an IGOR software that measures the achieved drain current. From these measured data, a linear or 'modified' hyperbolic tangent approximation of the device's transfer characteristic is then derived. From here, the voltage and current PA waveform postulator firstly presented by Cripps [1] has been developed and used to apply waveform engineering concepts in order to identify high power and high efficiency modes of operation. The resulting postulated achievable current waveforms are initially used to identify optimum bias conditions and then the required harmonic impedances. In the second stage waveform device characterisation is 'guided' using the postulated target waveforms that have been identified and these are then used as the basis for the load-pull measurement activity. It will be shown that, for well-behaved devices and using postulated data generated from first step, satisfactory measurement results can be achieved very quickly. In fact, for both well-behaved and unpredictable and high power/frequency devices, this procedure can give quick 'first-guess' information for bias voltage and impedances information allowing focused load-pull activity to be

quickly conducted. A comparison of output performance achieved using a typical manual measurement procedure described in Section 4.2.1 where the optimum target performance has been achieved using accurate but time consuming load-pull measurements, and this high-speed approach using linear and modified tanh approximations of the device's transfer characteristic have been conducted in order to demonstrate the validity of the approach. For this investigation approach, the same QinetiQ GaN transistors used in Section 4.2.2 operating at 0.9 GHz fundamental frequency and 15 V supply voltage have been used.

4.2.3.1 Automated Approach

The first stage of the developed automated approach is based on DCIV measurement data, from which two approximations of the device's transfer characteristic, linear and modified hyperbolic tangent (tanh) [25] functions are derived. The device used in this experiment is the same of Section 4.2.2. Firstly, for the linear approximation five parameters are extracted to adequately describe the DC boundaries and the device transfer characteristic. Specifically these are drain voltage (V_{DC}), pinch-off voltage (V_{TH}), saturation drain current (I_{DSS}), knee voltage (V_{knee}) and the transconductance (g_m). For the modified tanh approximation, the addition of empirical parameters termed A, B and C are used, as later shown in (4.9). Once the DCIV measured data has been obtained, this is then utilised by the postulator to predict the required drive, bias voltage and harmonic impedances as well as the expected time-domain voltage and current waveforms, output power and efficiency for a specific mode of operation.

Drive level and input bias along with the device's boundary conditions play a significant role in shaping the current waveform. In this analysis, input bias is typically swept over a range around the theoretical Class-F bias setting which will be in the region of the device's pinch-off voltage. The relationship between the postulated output current and voltage waveforms dictate the achievable output power and drain efficiency. The link between the input bias and output current waveform is provided by an appropriate choice of the transfer characteristic as shown later in (4.8) and (4.9).

Fig. 4.4 shows the flowchart of the approach. For a successful optimisation, it is

important to accurately specify and weight the targeted output power level. As an example, for a given bias range the predictor may converge towards a Class-C bias point thus optimising for very high efficiency at the expense of output power. If inaccurate specifications are used, the predictor might not converge, due to the fact that, for example negative impedances would be needed in order to deliver the right output power and/or efficiency [26-28]. In this work only positive impedances will be considered and taken into account. Once the optimum waveforms are identified by the postulator the resulting device conditions are uploaded into the time-domain measurement system software. This then replicates in reality the bias, drive, and harmonic loading conditions identified by the postulator. To facilitate accurate comparison with the waveforms measured at the output reference plane established by the measurement system, the predicted waveforms (which are postulated in the absence of extrinsic and intrinsic parasitic effects) are embedded with the effects of the device output parasitic capacitance. As for the manual measurements, a value of C_{DS}=0.04 pF was used. It should be noted that the embedding of the parasitic output capacitance is necessary to verify the device performance in terms of output power and efficiency, as well as to identify the harmonic loads that need to be presented at the device measurement plane.

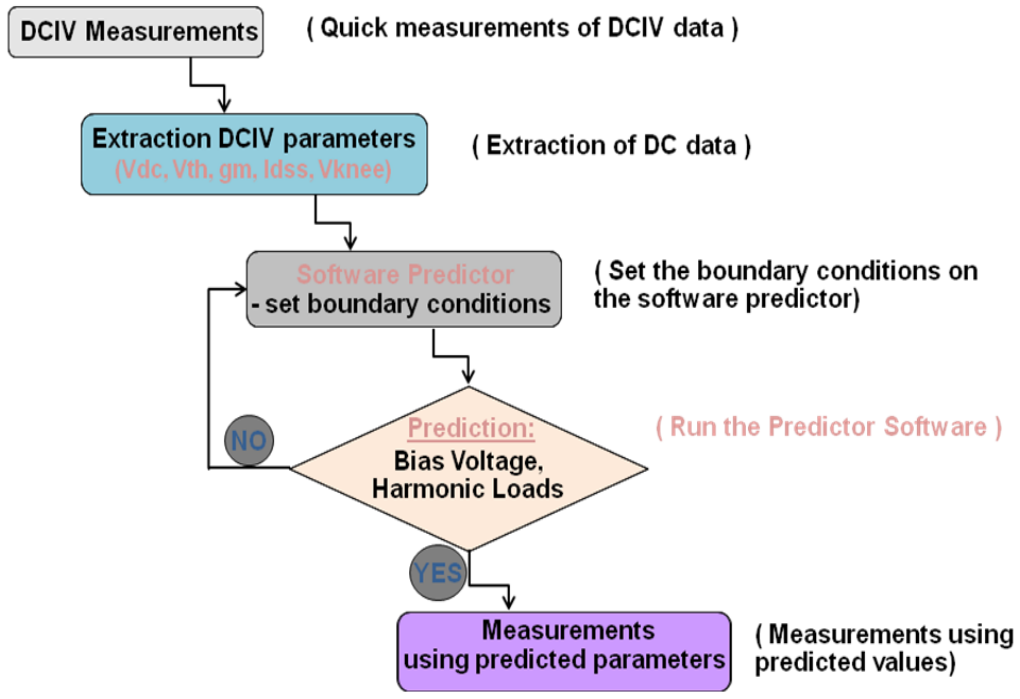

Fig. 4.4 – Flow chart of the approach.

4.2.3.2 Extraction DCIV Parameters

For these measurements, the DC drain voltage was fixed at V_{DS}=15 V. The knee voltage (V_{knee}) is the point that divides the saturation and the linear region of the device and in terms of time domain waveforms can be defined as the minimum value of the achievable RF drain voltage. As it can be seen from Fig. 4.5, the V_{knee} can assume any value between 0 and 4 V. A correct value can be established by knowing the output RF power (P_{OUT}) which is delivered by the device according to the following equation [29]:

$$P_{OUT} = \frac{1}{2}\frac{(V_{DC} - V_{knee}) \cdot I_D}{2}. \tag{4.7}$$

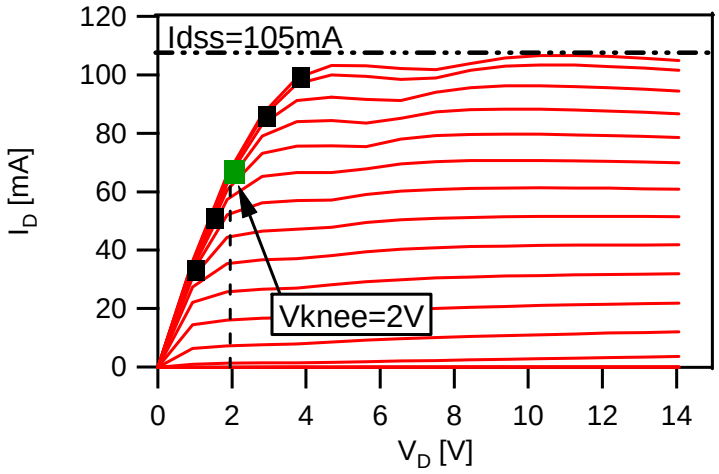

Fig. 4.5 – Measured DCIV.

With reference to equation (4.7) and Fig. 4.5, if operating with a knee voltage of 2 V, the corresponding maximum drain current is approximately 65 mA and achievable output power is approximately 23.2 dBm, which in this case is the closest to the expected value of 23 dBm. The saturation current (I_{DSS}) is the maximum current which the device can deliver and this parameter can again be easily found from DCIV characteristic shown in Fig. 4.5. The pinch-off voltage (V_{TH}) is the gate bias voltage where the device starts to conduct current. This value can be obtained from the extracted transfer characteristic. G_m is the transconductance of the device which is identified by the slope of the transfer characteristic. A, B and C are empirical values introduced and used to fit the modify tanh approximation of the transfer characteristic as close as possible to the

measured one. Table 4.IV summarises the DC extracted parameters which are common to both transfer characteristics.

TABLE 4.IV
EXTRACTED DC PARAMETERS

V_{DC} [V]	V_{TH} [V]	I_{DSS} [mA]	V_{knee} [V]
15	-5.5	105	2

4.2.3.3 Waveform Engineering Prediction

When using both the linear and hyperbolic tangent approximations of the transfer characteristic, additional DC parameters need to be extracted; an example is shown in Table 4.V.

TABLE 4.V
EXTRACTED PARAMETERS FOR DIFFERENT TRANSFER CHARACTERISTICS

Linear	Tanh		
g_m [A/V]	A	B	C
0.43	2.25	0.4	0.316

Using the two simple functions to model the transfer characteristics shown in (4.8) and (4.9), it is possible to generate an idealised three-harmonic Class-F voltage waveform (3rd harmonic square waveform) that achieves good postulated results in terms of bias voltage (V_G) and harmonic impedances.

$$I_{D\_linear} = v_g \cdot g_m \cdot I_{DSS}\left[1 - e^{\frac{V_{DS}}{V_{knee}}}\right], \tag{4.8}$$

$$I_{D\_\tanh} = [(1 + A \cdot \tanh(v_g \cdot B - V_t \cdot C))/2] \cdot 2I_{DSS}\left[1 - e^{\frac{V_{DS}}{V_{knee}}}\right], \tag{4.9}$$

where v_g is the input voltage while A, B and C of (4.9) are three parameters that have been added in order to fit as close as possible the theoretical transfer characteristic to the measured one.

Fig. 4.6 shows that the linear function and especially the tanh function in this case offer good approximations to the measured transfer characteristic.

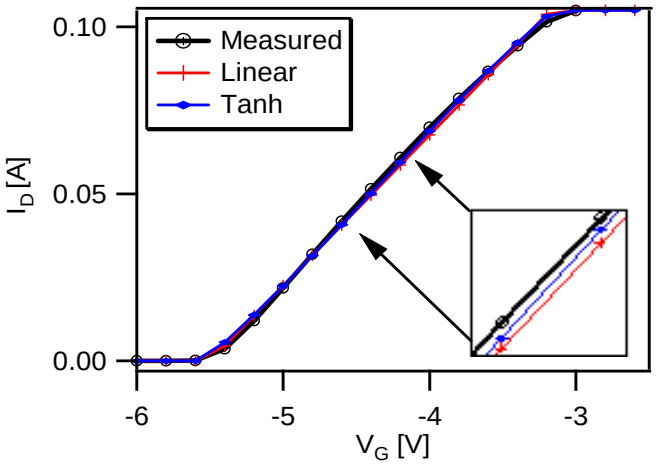

Fig. 4.6 – Measured and postulated linear and hyperbolic tangent characteristics.

Using the DC parameters established for the tanh characteristic, the postulator identifies the optimum bias point and fundamental and harmonic impedances (shown in Table 4.VII) for in this case a Class-F mode of operation. Since this mode relies on a half-wave rectified sinusoidal current waveform, the third harmonic current component is significantly suppressed. The predictor will also develop waveforms such as those in Fig. 4.7, as well as the expected output power and drain efficiency shown later in Table 4.IX.

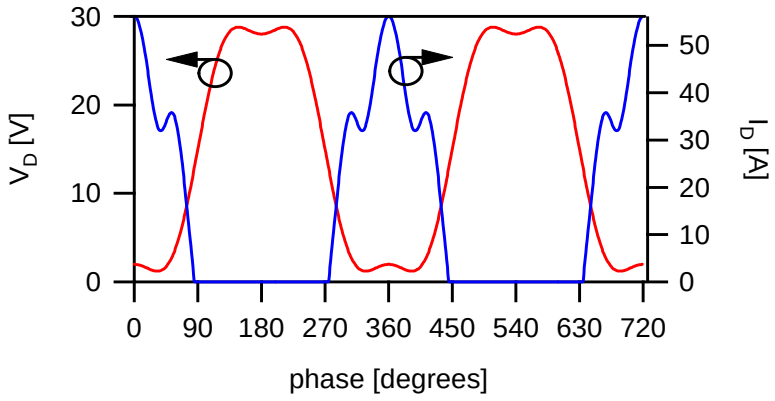

Fig. 4.7 – Predicted Class-F voltage and current waveforms at the $I_{GEN-PLANE}$ using the modified tanh characteristic.

Fig. 4.8 shows the behaviour of the third harmonic current as a function of gate bias voltage (V_G) for the two modelled transfer characteristics as well as from direct measurements. It can be seen here that to minimise the third harmonic current, the hyperbolic tangent function offers a closer fit to the measured device behaviour.

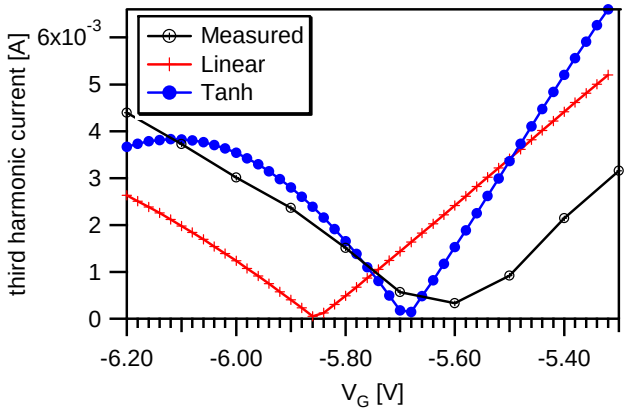

Fig. 4.8 – Third harmonic current amplitude for measured and linear and hyperbolic tangent functions.

In the manual measured case (Fig. 4.1 and 4.8), the Class-F bias point (V_G=-5.6 V) is slightly lower than pinch-off (V_{TH}=-5.5 V) resulting in a higher value of efficiency while still maintaining the expected output power. For both linear and tanh functions, the optimum choice of bias voltage is not the one that exactly minimises the third harmonic current. This is because the aim is to achieve the best trade-off between efficiency and output power. Considering for example the tanh approximation, a bias point of V_G=-5.68 V offers the best postulated efficiency (η=83%). However, this is at the expense of lower output power P_{OUT}=22.7 dBm. Changing the bias voltage to V_G=-5.64 V (shown in Table 4.VI) results in a better compromise between efficiency η=82% and higher output power P_{OUT}=23 dBm.

TABLE 4.VI
IDENTIFIED BIAS VOLTAGE FOR MINIMUM 3RD HARMONIC CURRENT FOR DIFFERENT TRANSFER CHARACTERISTICS

	Measured	***Linear***	***Tanh***
Bias Points	*-5.6 V*	*-5.78 V*	*-5.64 V*

4.2.3.4 Measurements Using Predicted Parameters

Once the required impedances and bias voltage have been identified, the next stage was to use these emulated values directly in the measurement system in order to identify the resulting measured waveforms, output power and efficiency on the real device. Table 4.VII summarises the first three impedances when using the manual procedure and when using the predictor procedure applying both the linear as well as the tanh functions.

TABLE 4.VII.
FUNDAMENTAL AND HARMONIC IMPEDANCES AT OUTPUT MEASUREMENT PLANE

	Z(F0) [Ω]	***Z(2F0) [Ω]***	***Z(3F0) [Ω]***
Manual	616+j2.96	0+j0.43	0+j954
Linear	630+j91	0+j0	2209+j2131
Tanh	626+j90	0+j0	2152+j1708

Fig. 4.9 shows the measured and predicted (inset) load-line for both device plane (green line) and output measurement plane (red line). The predicted load-line has been identified using the hyperbolic tangent characteristic approximation. It can be seen that the measured results agree quite well with those predicted. Besides, noted the knee voltage is approximately 2 V as expected.

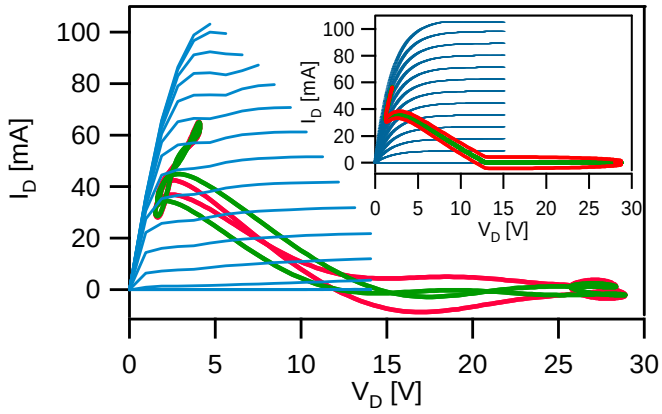

Fig. 4.9 – Measured RF load-line at the $I_{GEN\text{-}PLANE}$ (green line) and output measurement plane (red line) with the predicted load-line inset.

Similarly, as it can be seen from the measured time domain voltage (red line) and current waveform (blue line) in Fig. 4.10, there is a good agreement with the predicted waveforms of Fig. 4.7.

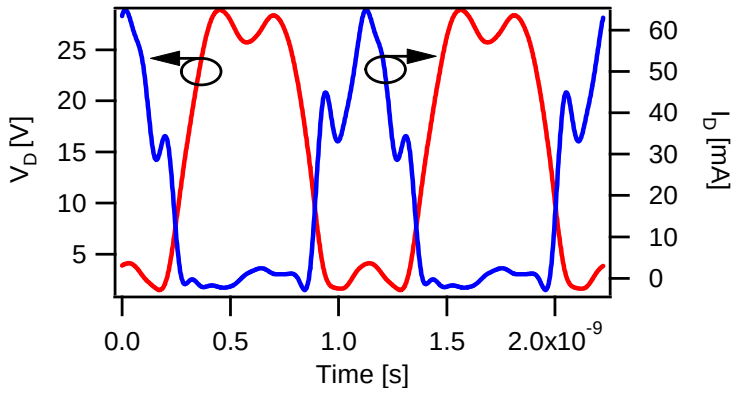

Fig. 4.10 – Measured voltage and current waveforms at the $I_{GEN\text{-}PLANE}$.

4.2.3.5 Results and Comparison

Table 4.VIII shows measurement results achieved using the manual approach where all target parameters have been obtained using lengthy sweeps directly from the measurement activity without any prediction, while Table 4.IX shows the predicted and measurement results when using the predicted linear and modified tanh approximations. It can be noted that the new procedure yields device performances that are close to that achieved when using the manually driven approach. Obviously the predicted values will be closer to the measured equivalents for well-behaved devices. In any case an important first guess can be achieved, greatly reducing the time taken to locate these optimum values.

Interestingly, both linear and hyperbolic tangent functions are able to predict bias point and harmonic impedances that show a very good agreement with those identified using the manual approach thus demonstrating the validity of the approach. For unpredictable devices or higher frequencies, this first guess gives a zoomed window in which load-pull can be conducted for the achievement of the optimum condition, saving valuable time.

TABLE 4.VIII
MANUAL MEASUREMENT RESULTS

	Measurements
Manual	P_{OUT}=23.57dBm η = 81.024

TABLE 4.IX
PREDICTED AND MEASURED RESULTS USING PREDICTION

	Prediction	***Measurements***
Linear	P_{OUT}=22.93dBm η= 82.71%	P_{OUT}= 23.3dBm η = 79.6%
Tanh	P_{OUT}=22.96dBm η = 82 %	P_{OUT}= 23.34dBm η = 80.35 %

In this section it has been demonstrated that armed only with simple DC information describing a real device, it is possible to significantly speed up load-pull measurement activity. The incorporation of simple waveform data derived from a basic set of DC measurements can have a significant impact in supplying important first-guess measurement data including drive, bias and load condition.

This would dramatically improve the time utilisation of the load-pull measurement systems. This work is therefore of high significance to the load-pull measurement community where combining the measurement activity with modelling (albeit simple modelling) knowledge, it is possible to avoid very time consuming measurement activities. Results based upon postulated waveforms show a good agreement with those obtained using a conventional manual search procedure for well behaved devices. Here predictions and measurements have been demonstrated on a single GaN device from QinetiQ, however predictions and measurements have been conducted using different geometries of QinetiQ GaN transistors as well as TriQuint and RFMD (Radio Frequency Microwave Devices) GaAs transistors, all giving satisfactory results.

4.3 Continuous Class-FV Measurements

Section 4.2 has shown and explained a detailed and systematic methodology for the design of very power efficient Class-F power amplifiers. It has been demonstrated that this approach works both when conducting the measurements without any knowledge of the device itself (the manual procedure) and when using a predictor software, which by starting from few DCIV measurements can provide a satisfactory first guess to the measurement system speeding up the overall measurement activity [24].

Nowadays there is a great demand on power amplifier (PA) designers to improve the efficiency over increasingly broad frequency ranges without significantly sacrificing output power levels. The challenge in designing harmonically tuned PA modes such as the standard Class-F and Inverse Class-F [30-34] is to maintain the required short and open circuit harmonic terminations which due to practical constraints must be placed at a distance from the device and generally limit achievable relative bandwidths. However, as theoretically presented in Chapter 3 [35], through a new formulation for the voltage waveform it is possible to design RFPAs (radio frequency power amplifiers) that maintain constant high efficiency and output power over a continuous range of fundamental and second harmonic impedances.

The Continuous Class-FV design space described theoretically in Chapter 3 has been explored experimentally on the ELP measurement system developed at Cardiff University [36]. Again the measurement system allows voltage and current waveforms to be measured at the extrinsic device measurement plane and then shifted to the device intrinsic current-generator plane by de-embedding the drain-source capacitor C_{DS} [5] as explained previously and shown in Fig. 4.11.

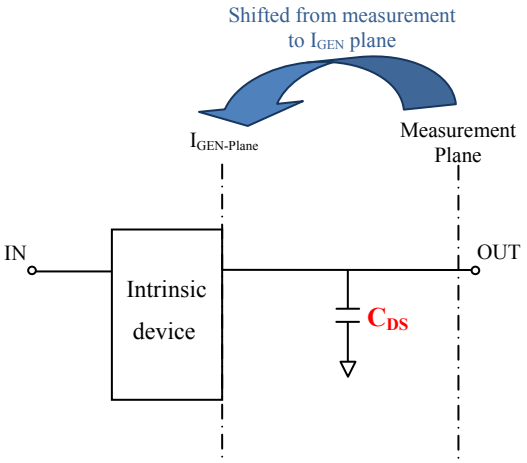

Fig. 4.11 – I_{GEN} and measurement reference planes.

The devices used for the experimental validation of this theory are on-wafer from TriQuint TQPED GaAs (gallium arsenide) Foundry process, specifically 6x50 µm depletion mode. The measurements have been conducted at 0.9 GHz fundamental frequency, using 6 V supply voltage and delivering approximately 20 dBm of output power.

The approach presented in the previous paragraph has been applied to the device in order to achieve the initial conventional Class-F state. First of all a value for the bias voltage V_{GS} is selected for which the third harmonic current is minimised, in this case V_{GS}=-0.85 V. This condition produces the half-wave rectified sinusoidal current waveform required. Once the current waveform is established, the desired Class-B fundamental load Z_{F0_B}=186.2+j0 Ω is determined with higher harmonic impedances being short-circuited. Important to note is that the fundamental impedance is purely resistive as the reference plane has been shifted from the measurement plane to the device current-generator plane through the de-embedding of the drain-source capacitor (C_{DS}) which in this case is C_{DS}=0.14 pF [37]. The

study of waveform engineering at the $I_{GEN-PLANE}$ is important to understand the device behaviour and to establish the various PA modes. The first three harmonic impedances at the measurement plane are: Z_{F0}=0.61∟2.9° (209+j21 Ω), Z_{2F0}=Z_{3F0}=0 (short-circuit). To move towards the Class-F mode, harmonic load-pull is employed to engineer the voltage waveform. Here, the second harmonic impedance is kept at a short-circuit whilst the third harmonic impedance has been open-circuited. In the final step at the $I_{GEN-PLANE}$ the fundamental impedance is scaled by 2/√3 (approx. 1.154) in order to increase the fundamental voltage component and therefore regain the minimum voltage value of the squared waveform that is comparable to the original Class-B mode. In this case an optimum Class-F fundamental impedance R_{F0_F}=215+j0 Ω is obtained. The scaling of the fundamental load also restores the fundamental current swing that was created initially for Class-B. The measured maximum drain efficiency and output power are η=87% and P_{OUT}=20.3 dBm respectively at around 2 dB of gain (G) compression (P2dB), where the power gain is G=27 dB as shown in Fig. 4.12, with the current and voltage waveforms shown in Fig. 4.13. The efficiency does not reach the ideal value of 90.6% as the higher harmonic impedances are not short or open-circuited, but kept close to the 50 Ω characteristic impedance of the measurement system. Additionally, the actual knee voltage is greater than zero, thus explaining the lower measured efficiency compared with theory. However, the achieved drain efficiency is very close to the theoretical one due to the low device knee voltage.

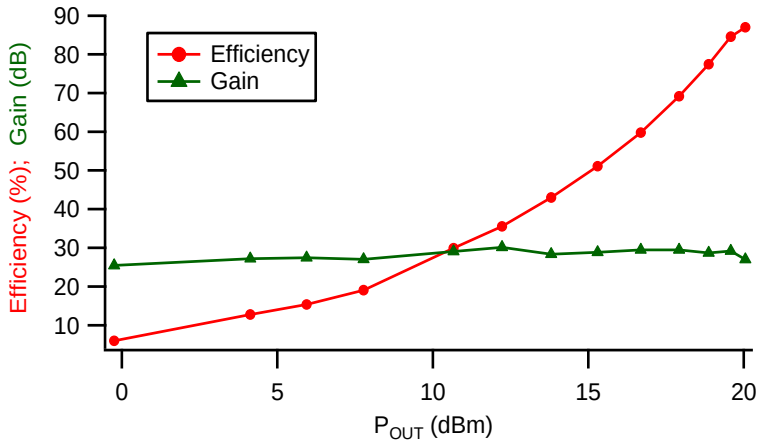

Fig. 4.12 – Measured Class-F efficiency and power gain function of the output power.

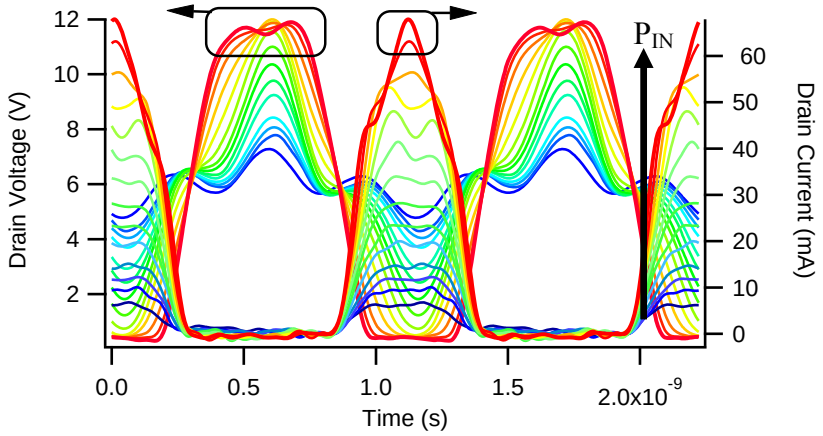

Fig. 4.13 – Measured Class-F voltage and current waveforms at the $I_{GEN-PLANE}$ function of the input power.

Once the conventional Class-F condition has been achieved, by applying the Continuous Class-FV theory [35] described in Chapter 3, the current waveform is kept constant half-wave rectified sinusoidal while the voltage waveform is allowed to vary as shown in Fig. 4.14 and obtained from equations (4.10) and (4.11).

$$v_{cont\_classFV}(\vartheta)=\left(1-\frac{2}{\sqrt{3}}\cos\vartheta\right)^2\cdot\left(1+\frac{1}{\sqrt{3}}\cos\vartheta\right)\cdot\left[1-\delta\sin\vartheta\right] \tag{4.10}$$

$$\begin{aligned} i_{cont\_classFV}(\vartheta) &= I_{peak}\cos\vartheta \qquad 0<\vartheta<\pi/2,\quad (3/2)\pi<\vartheta<2\pi, \\ &= 0 \qquad\qquad\qquad\quad 0<\vartheta<\pi/2 \end{aligned} \tag{4.11}$$

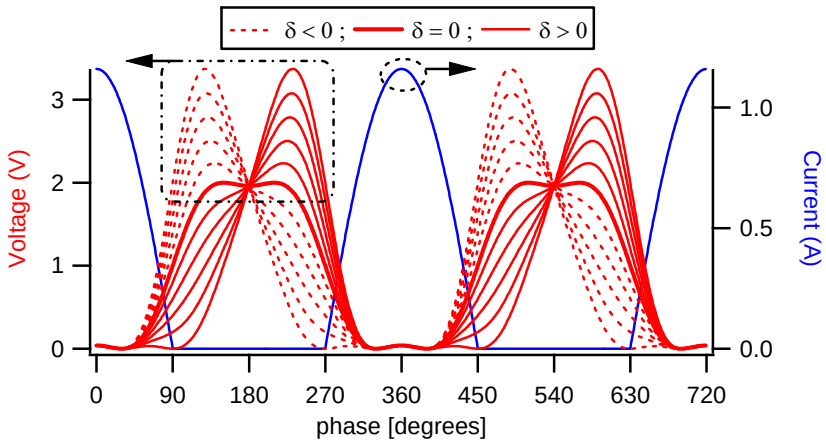

Fig. 4.14 – Theoretical Continuous Class-FV voltage and current waveforms at the $I_{GEN-PLANE}$.

The new design space was explored for the identified range of δ, where $-1 \leq \delta \leq 1$ in order to maintain a positive voltage waveform. Here, the reactance of the fundamental impedance was varied versus a range of second harmonic reactances while maintaining a constant open circuit third harmonic termination.

Fig. 4.15 shows the Smith chart with the measured first three harmonic impedances function of δ. Here, as it can be noted in the yellow circle, for $\delta > 0.5$ the second harmonic impedance is not placed on the edge of the Smith chart, this is due to stability considerations [38]. Therefore, in this case second harmonic loads with reflection coefficient (Γ) smaller than 1 have been presented.

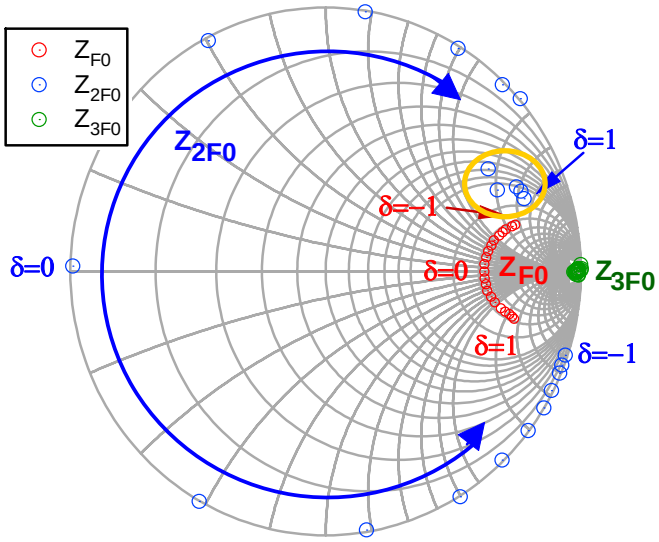

Fig. 4.15 – Measured Continuous Class-FV first three harmonic impedances for $-1 \leq \delta \leq 1$ in steps of 0.1.

Figures 4.16 and 4.17 show the device output performance in terms of both power and efficiency as well as the combination of fundamental and second harmonic reactance function of δ. The variation of δ from -1 to 1 is in fact translated into a variation of X1/R1 from 0.85 to -0.85. During these measurements the third harmonic impedance was maintained open-circuited. Maximum efficiency of 87.0% is achieved for X1/R1=0 (standard Class-F). It is important to highlight that efficiency and output power are maintained at almost constant levels for a wide range of X1/R1 from -0.4 to 0.85, consistent with the theoretical prediction. When moving towards $\delta > 0.5$, the output power and especially efficiency degrades. This is firstly due to the fact that the second harmonic impedance could not be placed on

the edge of the Smith chart as mentioned previously. Besides, in this measurement activity, only the first three harmonic terminations have been controlled. The fourth harmonic impedance is a fixed point somewhere in the Smith chart (usually not too far from the 50 Ω environment characteristic impedance) and can lead to a decrease in efficiency, especially in the two edges of δ=±1) [39]. Therefore, as a function of where the fourth harmonic (as well as the higher harmonics) termination is placed, the output performance can be better in one side of δ or worst in the other side, in this case for δ>0.5.

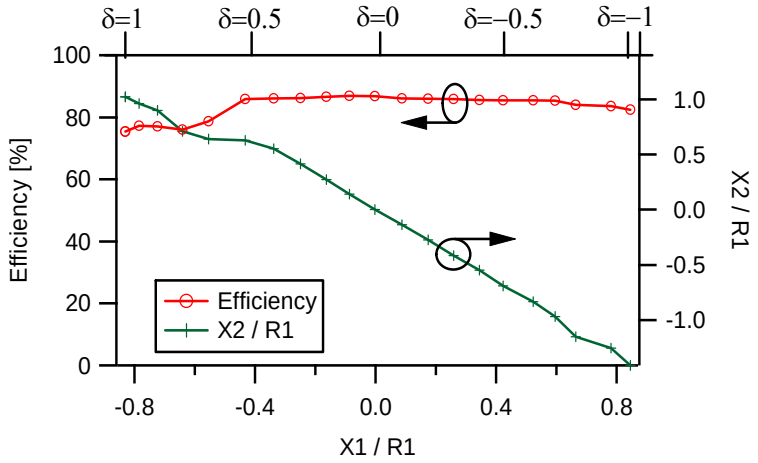

Fig. 4.16 – Measured Continuous Class-FV efficiency for coupled variations of fundamental and second harmonic reactances for -1 ≤ δ ≤ 1 in steps of 0.1 and keeping open-circuited the third harmonic load.

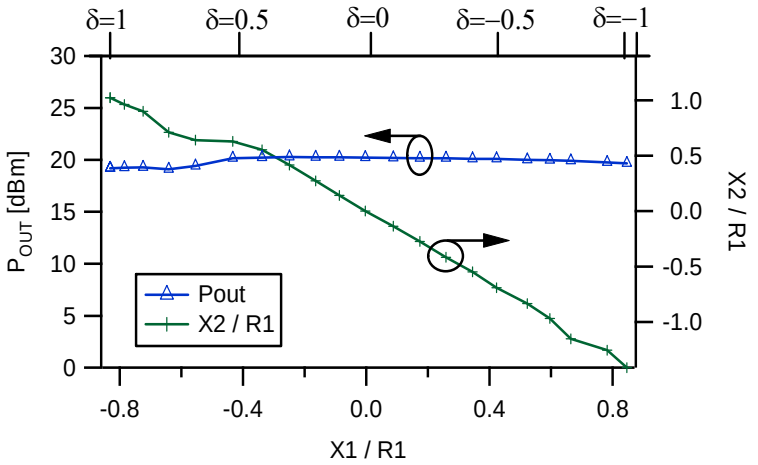

Fig. 4.17 – Measured Continuous Class-FV output power for coupled variations of fundamental and second harmonic reactances for -1 ≤ δ ≤ 1 in steps of 0.1 and keeping open-circuited the third harmonic load.

It is important to remember that the current waveform should be maintained half-wave rectified sinusoidal, thus while stepping through the values of δ, the drive power was actively adjusted in order to keep the current as constant as possible. Fig. 4.18 shows the changes of the available power P_{AVS} (drive power) and as well as the input power which flows into the device. Fig. 4.19 shows the input reflection coefficient at the fundamental frequency during the emulation of the Continuous Class-F mode when varying δ. These changes are thought to be caused by the increased peak values of the drain voltage for $\delta \neq 0$ and explains the need for drive power adjustments during the emulation of this PA mode. Over frequency this can be compensated for in the design of the input matching network.

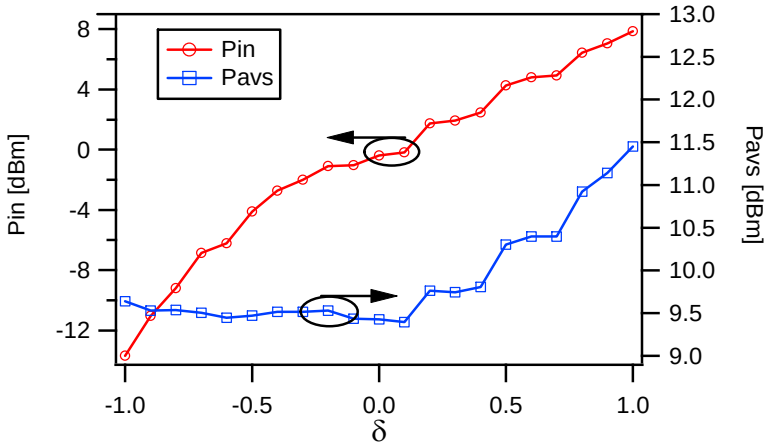

Fig. 4.18 – Measured variations of the input power (input power and available from the source power) during the emulation of the Continuous Class-FV PA mode.

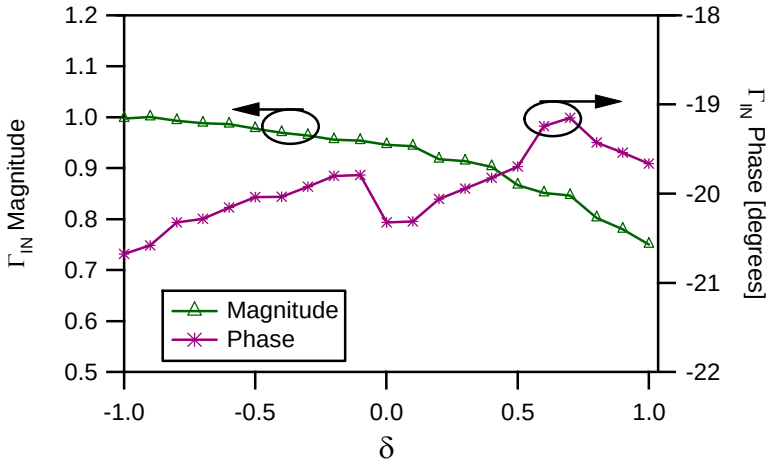

Fig. 4.19 – Measured variations of the input reflection coefficient (magnitude and phase) during the emulation of the Continuous Class-FV mode.

For further investigations contour plots have been measured over the new impedance design space as shown in Fig. 4.20 and 4.21. During these measurements, the drive power has been kept constant. The contour plots demonstrate that both drain efficiency and output power are dependent on the fundamental and second harmonic reactance, and clearly indicate the predicted design space, producing an optimum device performance region of coupled X1 and X2 solutions. The best performance is when the fundamental is positive and second harmonic reactance is negative and vice-versa, as within the Continuous Class-FV mode X1 and X2 have an inverse relationship.

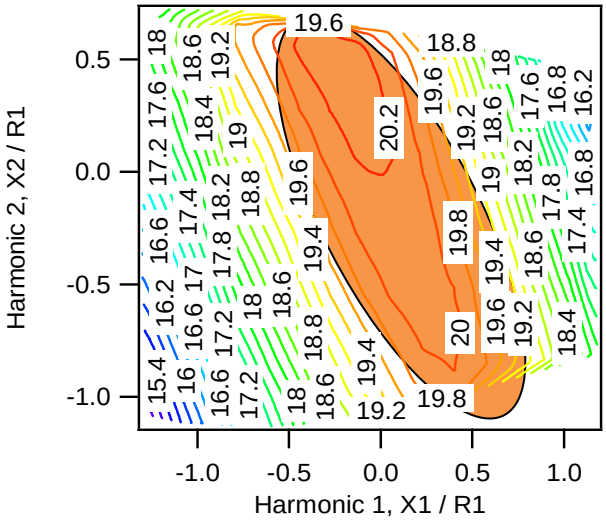

Fig. 4.20 – Measured Continuous Class-FV drain efficiency as a function of normalised X1 and X2 for constant drive signal.

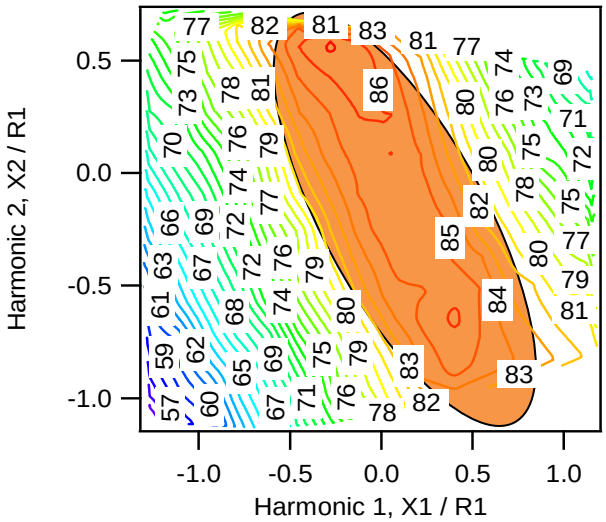

Fig. 4.21 – Measured Continuous Class-FV output power as a function of normalised X1 and X2 for constant drive signal.

Fig. 4.22 shows the measured RF voltage waveforms at the current-generator plane with δ ranging from -1 to 1 with the classic Class-F waveform given for X1/R1=0 (highlighted red waveform). It can be seen that the new family of voltage waveforms are very similar to the theoretical ones presented in Fig. 4.14. Comparing the Continuous Class-FV waveforms with those of the standard Class-F also highlights the increase in peak voltage, which effectively creates the new design space. This concept can be used for low supply voltage or device technologies with high breakdown voltages as the emerging power transistors in GaN (gallium nitride) or AlGaN/GaN (AluminumGaN/GaN) technology[40-44].

Besides, it can be seen in Fig. 4.22 that the peak of the voltage waveforms for $\delta > 0$ (blue lines) don't increase to the same peak of voltage for $\delta < 0$ (green lines). Again, this is due to the fact that for $\delta > 0.5$ a second harmonic impedance with $\Gamma<1$ is presented due to stability considerations.

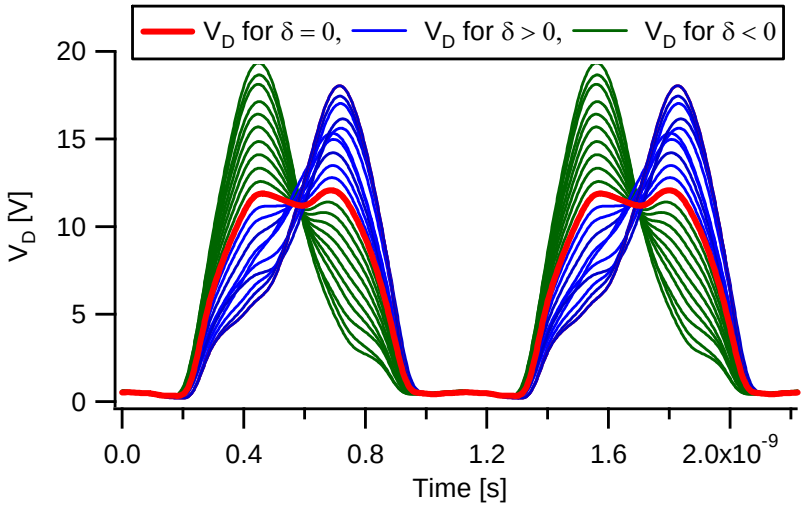

Fig. 4.22 – Measured Continuous Class-FV voltage waveforms at the $I_{GEN-PLANE}$.

4.4 Extending the Continuous Class-FV Theory with Resistive Second Harmonic Termination

So far the Continuous Class-FV mode has demonstrated theoretically and experimentally that starting from the optimum conventional Class-F state and by varying properly fundamental and second harmonic impedances the output performance can be maintained at a constant level. In this case both the

fundamental and the second harmonic terminations are allowed to vary only reactively, which means that Z_{F0} can vary on its circle of constant optimum resistance ($R_{F0}=R_{OPT}$) while Z_{2F0} can only vary on the perimeter of the Smith chart from its short-circuit condition. Unfortunately when designing power amplifiers it is not possible to present terminations with reflection coefficient Γ=1 due to the losses introduced from the matching networks. This means that the harmonic terminations cannot reach the edge of the Smith chart due to the losses introduced from the output matching network. This aspect leads to a new theory on the Continuous Class-FV mode which has been extended and thus called "Extended Continuous Class-FV" mode [45].

A new and more generalised formulation for the voltage waveform is shown in (4.12):

$$v(\vartheta)=(1-\alpha\cos\vartheta)^2\cdot(1+\beta\cos\vartheta)\cdot(1-\delta\sin\vartheta), \tag{4.12}$$

where α, β and γ are three parameters which define the design space. As for the previous broadband/Continuous modes explained in Chapter 3, it is very important that, for each combination of the three parameter values, the voltage waveform is kept above zero in order to maintain the high power efficiency state [46].

$$v(\vartheta)>0. \tag{4.13}$$

In addition, it is important to remember that the current waveform must be kept constant half-wave rectified sinusoidal as shown in (4.11).

Equation (4.12) can be expanded giving the following voltage expression for the $I_{GEN\text{-}PLANE}$:

$$\begin{aligned} v(\vartheta)=V_{DC}&-A_1\cos(\vartheta)-A_2\cos(2\vartheta)-A_3\cos(3\vartheta)+\\ &+B_1\sin(\vartheta)+B_2\sin(2\vartheta)+B_3\sin(3\vartheta)+B_4\sin(4\vartheta), \end{aligned} \tag{4.14}$$

where V_{DC} represents the supply voltage. A_1, A_2 and A_3 represent the voltage components of the real part of the fundamental, second and third harmonic impedances, and B_1, B_2, B_3 and B_4 represent the voltage components of the imaginary part of the fundamental, second, third and fourth harmonic impedances.

This gives:

$$V_{DC} = 1 + \frac{1}{2}\alpha^2 - \alpha\beta \,, \tag{4.15}$$

$$A_1 = 2\alpha - \beta - \frac{3}{4}\alpha^2\beta \,, \tag{4.16}$$

$$A_2 = \alpha\beta - \frac{1}{2}\alpha^2 \,, \tag{4.17}$$

$$A_3 = -\frac{1}{4}\alpha^2\beta \,, \tag{4.18}$$

$$B_1 = \delta\left(\frac{1}{2}\alpha\beta - 1 - \frac{1}{4}\alpha^2\right), \tag{4.19}$$

$$B_2 = \delta\left(\alpha - \frac{1}{2}\beta - \frac{1}{4}\alpha^2\beta\right), \tag{4.20}$$

$$B_3 = \delta\left(\frac{1}{2}\alpha\beta - \frac{1}{4}\alpha^2\right), \tag{4.21}$$

$$B_4 = -\frac{1}{8}\delta\alpha^2\beta \,. \tag{4.22}$$

Real and imaginary harmonic impedances are normalised to the DC voltage (V_{DC}).

For the theoretical Continuous Class-FV mode, to achieve the maximum drain efficiency the second harmonic impedance must be kept reactive. To obtain this, the parameter A_2 in (4.17) is set to zero giving the condition

$$\beta = \alpha/2 \,. \tag{4.23}$$

The presence of the third harmonic voltage allows the increase of fundamental component. Substituting the value $\beta=\alpha/2$ in the real part of the fundamental component, equation (4.16) becomes:

$$A_1 = \frac{3}{8}\alpha^3 - \frac{3}{2}\alpha \,. \tag{4.24}$$

Differentiating (4.24) as shown in (4.25), the maximum amplitude of fundamental voltage (α) for optimum Class-F condition can be determined, as shown in (4.26):

$$A_1'(\alpha) = \frac{9}{8}\alpha^2 - \frac{3}{2} = 0 \,, \tag{4.25}$$

giving

$$\alpha = 2/\sqrt{3} \quad (4.26)$$

As mentioned before, keeping the parameters α and β constant while allowing only the parameter δ to be swept

$$-1 \le \delta \le 1 \quad (4.27)$$

leads to the previously presented Continuous Class-FV voltage formulation where fundamental and second harmonic impedances are allowed to vary only reactively [35]. Therefore by presenting (4.23), (4.26) and (4.27), when δ=0 the conventional Class-F mode is achieved; while when varying δ (again between -1 and 1 in accordance with (4.27)), the Continuous Class-FV family of voltage waveforms are revealed with maximum output power and drain efficiency of 90.7%.

4.4.1 Extended Continuous Class-FV with Second Harmonic Impedance on the Edge of the Smith chart ($\beta=\alpha/2$)

Once the general formulation of the new Extended Continuous Class-F mode is presented, demonstrating the Continuous Class-FV mode, the next step is to vary the parameters α and β as well. The variation of these parameters leads to a resistive second harmonic termination. It will be demonstrated that, even if the variation of these parameters leads to a resistive second harmonic termination, high efficiency can still be achieved greater than a certain pre-determined value, which in this case has been chosen at 75%, but now over a significantly wider design space than that discussed in previous analysis.

Firstly, keeping a constant value of $\beta=\alpha/2$ and varying the other two parameters α and δ, the second harmonic impedance varies still on the edge of the Smith chart, whilst now the fundamental impedance varies both magnitude and phase still achieving high efficiencies states, as shown in Fig. 4.23.

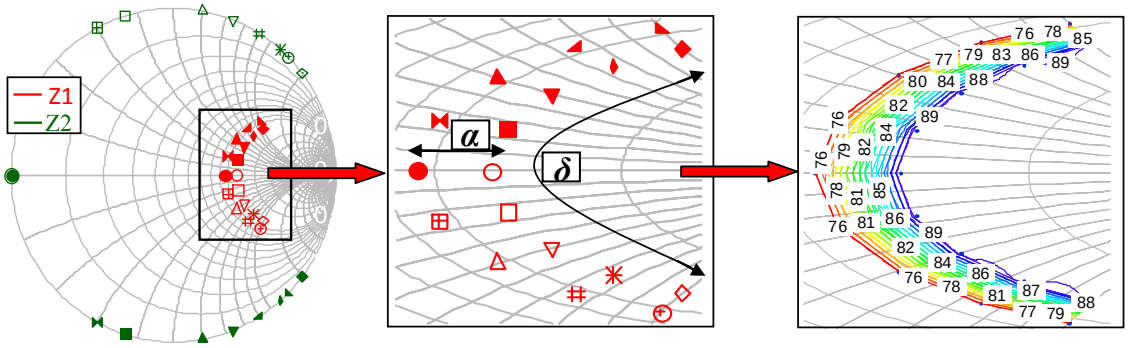

Fig. 4.23 – Theoretical Extended Continuous Class-FV impedances range and efficiency contour plot for the first two harmonic impedances (the third is kept open-circuited) when varying $0.75 \leq \alpha \leq 1$ and $-1 \leq \delta \leq 1$ with α step of 0.5 and δ step of 0.25.

Each fundamental load has its corresponding second harmonic impedance in order to maintain the high output power and drain efficiency states.

Fig. 4.24 shows the voltage waveforms with varying α, keeping $\beta=\alpha/2$ and for $\delta=0$. Note that with increasing values of α, bigger "troughs" in the voltage waveforms are developed. This translates into lower efficiency due to the lower fundamental voltage.

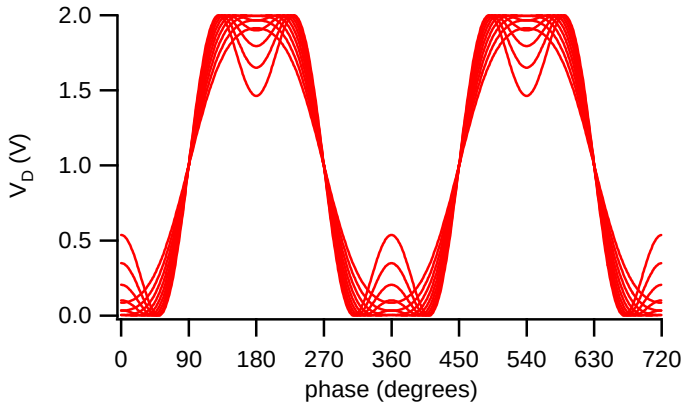

Fig. 4.24 – Theoretical Extended Continuous Class-FV voltage waveforms for constant $\beta = \alpha/2$ and $\delta = 0$ function of α, where $0.75 \leq \alpha \leq 1.55$ in steps of 0.1.

Fig. 4.25 shows the efficiency and output power variation with α for a constant value of $\delta=0$. Note that highest efficiency is achieved for $\alpha = 2/\sqrt{3}$ which is the standard Class-F condition, but a wide range of fundamental impedances can be chosen which still yielding efficiencies greater than 75%. Those theoretical values of efficiency and output power remain constant over the range of $-1 \leq \delta \leq 1$.

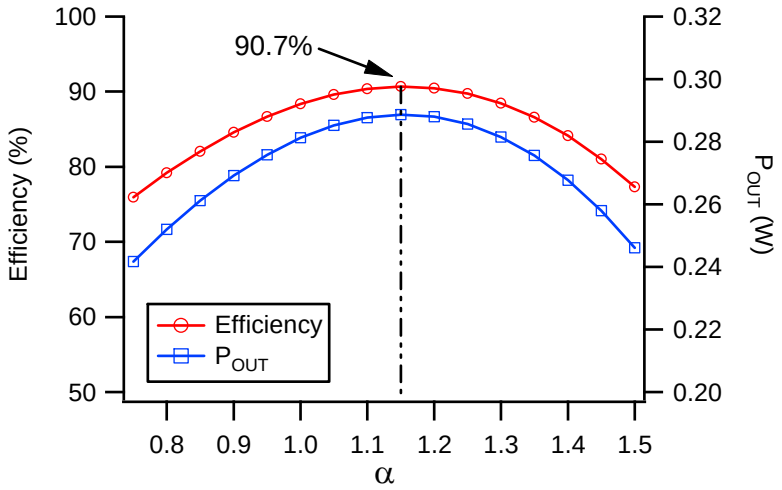

Fig. 4.25 – Theoretical Extended Continuous Class-FV efficiency and output power for constant $\beta = \alpha/2$ and $\delta = 0$ function of α, where $0.75 \leq \alpha \leq 1.55$ in steps of 0.05.

To achieve a non-zero-crossing voltage waveform, the parameter α must not equal zero. In this case, in accordance with (4.28), maintaining efficiency greater than 75% causes the range of α to be restricted to

$$0.75 \leq \alpha \leq 1.5\,. \tag{4.28}$$

4.4.2 Extended Continuous Class-F with Second Harmonic Impedance Inside the Smith chart ($\beta > \alpha/2$)

Following the same procedure of paragraph 4.3.1, the parameters α, δ and now also β will be varied. In the previous section the value of β was restricted to $\beta=\alpha/2$ (A_2=0), thus the second harmonic impedance was swept around the edge of the Smith chart. We now consider the more general case where the second harmonic impedance can be chosen inside the Smith chart, where for $\beta>\alpha/2$, in accordance with (4.14) and (4.17) the parameter A_2 is kept greater than zero.

The new condition of β variation delivers a wider range of design space that guarantees a stipulated minimum output performance.

When changing all three parameters, the range of those parameters which yield a non-zero-crossing voltage waveform and a minimum drain efficiency of 75% is shown in Table 4.X, which is based on (4.13) and for which drain efficiency is kept greater than 75%.

TABLE 4.X
DESIGN SPACE FOR WHICH THE VOLTAGE IS POSITIVE AND THE EFFICIENCY IS GREATER THAN 75%

β=α/2	**β=α/1.9**	**β=α/1.8**	**β=α/1.7**	**β=α/1.6**	**β=α/1.5**	**β=α/1.4**
0.75≤α≤1.5 -1 ≤ δ ≤ 1	0.75≤α≤1.45 -1 ≤ δ ≤ 1	0.8≤α≤1.45 -1 ≤ δ ≤ 1	0.8≤α≤1.35 -0.9≤δ≤0.9	0.85≤α≤1.3 -0.5≤δ≤0.5	0.9≤α≤1.2 -0.2≤δ≤0.2	α=1.05 δ=0

Voltage waveforms are shown for $\beta = \alpha / 1.6$ in Fig. 4.26. Note that with increasing value of α, again bigger troughs in the voltage waveforms are developed. If the parameter β increases, the range of α and δ where voltage waveforms are greater than zero and drain efficiency is greater than 75 % is reduced, as shown in Table 4.X and Fig. 4.27 (as well Fig. 4.29). Again, it can be noted from Fig. 4.27 that for $\beta=\alpha/2$ the efficiency is greater than 75 % (as well as the voltage waveform remaining positive) for a wide range of α ranging from 0.75 to 1.5. For $\beta=\alpha/1.5$ that range is reduced to the α range between 0.9 and 1.2, and for $\beta=\alpha/1.4$ the only point that allows positive voltage and high efficiency (greater than 75%) is α=1.05.

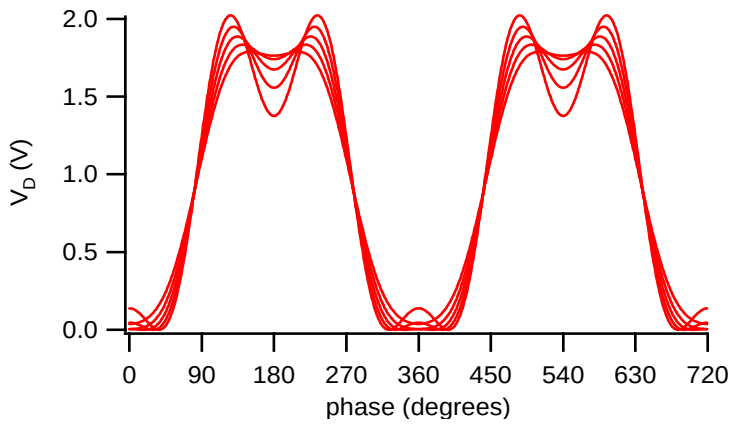

Fig. 4.26 – Theoretical Extended Continuous Class-FV voltage waveforms for constant $\beta = \alpha/2$ and $\delta = 0$ function of α, where $0.75 \leq \alpha \leq 1.55$ in steps of 0.1.

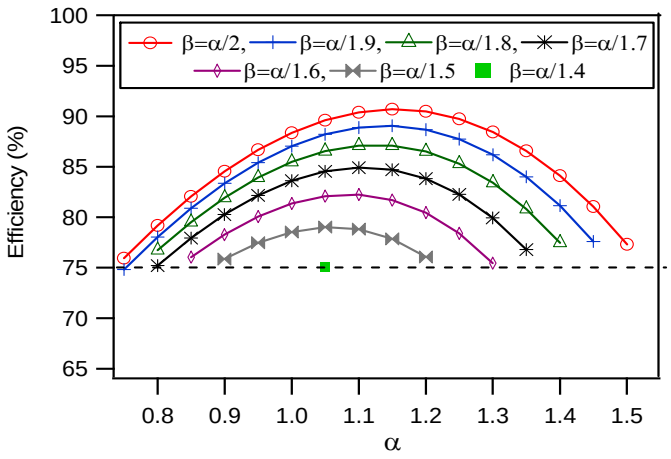

Fig. 4.27 – Theoretical Extended Continuous Class-FV drain efficiency function of α and β for constant $\delta = 0$.

Fig. 4.28 shows the Smith chart with the wide design space that allows very high flexibility in PA design. In this space it is important to note the continuity of this new PA mode. Also in this case, each fundamental load has its appropriate second harmonic load. It shows for example one combination of fundamental impedance (Z1', red triangle, even shown inset) and second harmonic impedance (Z2', green square) in accordance with (4.14) which maintains the stipulated high efficiency state (third harmonic impedance Z3 is kept open). In this case a drain efficiency of 89.5% is achieved.

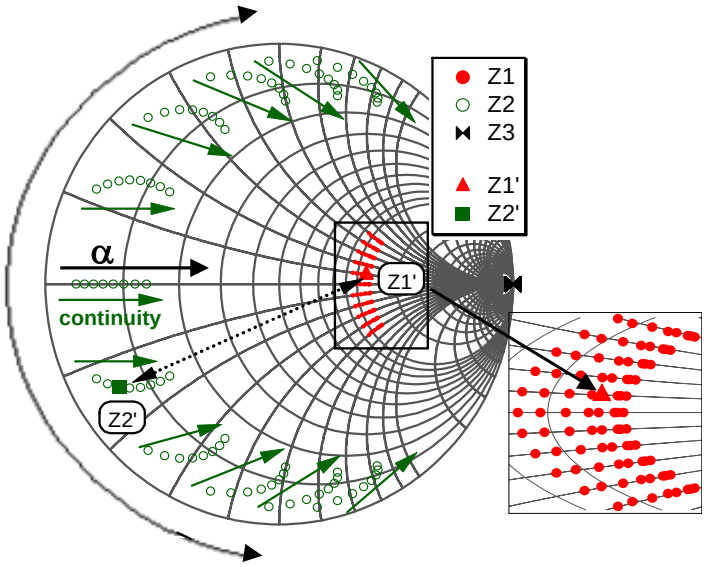

Fig. 4.28 – Theoretical Extended Continuous Class-FV impedances range for fundamental and second harmonic impedance (third harmonic load is kept open-circuited) with $\beta = \alpha / 1.9$ when varying $0.75 \leq \alpha \leq 1.45$ and $-0.5 \leq \delta \leq 0.5$ with both steps of 0.1. Inset collection of fundamental impedances.

Fig. 4.29 shows the maximum efficiency as a function of β for a given optimum α. Note that the efficiency decreases with increasing values of β but efficiencies greater than 75% are still maintained.

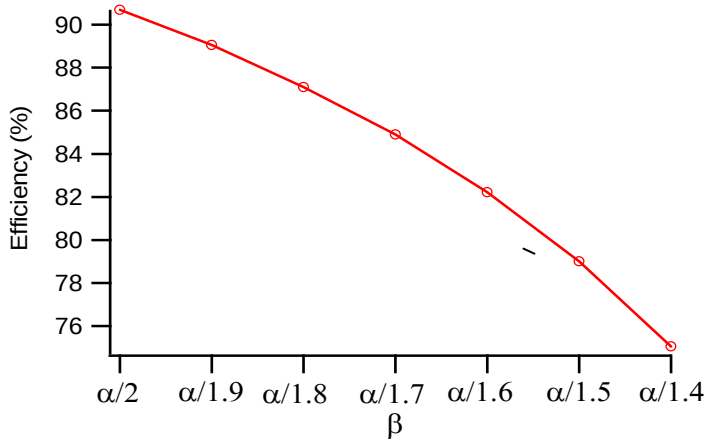

Fig. 4.29 – Theoretical Extended Continuous Class-FV efficiency function of β for $\delta = 0$ and optimum value of $\alpha = 1.15$.

Fig. 4.30 plots efficiency and output power as a function of α and δ with constant $\beta=\alpha/1.6$. Note that for α greater than 0.95, efficiency greater than 75% and voltage>0 (eq. 4.13) are valid for the only $\delta=0$ point (red line). Again this shows that with increasing β, the useful design space decreases.

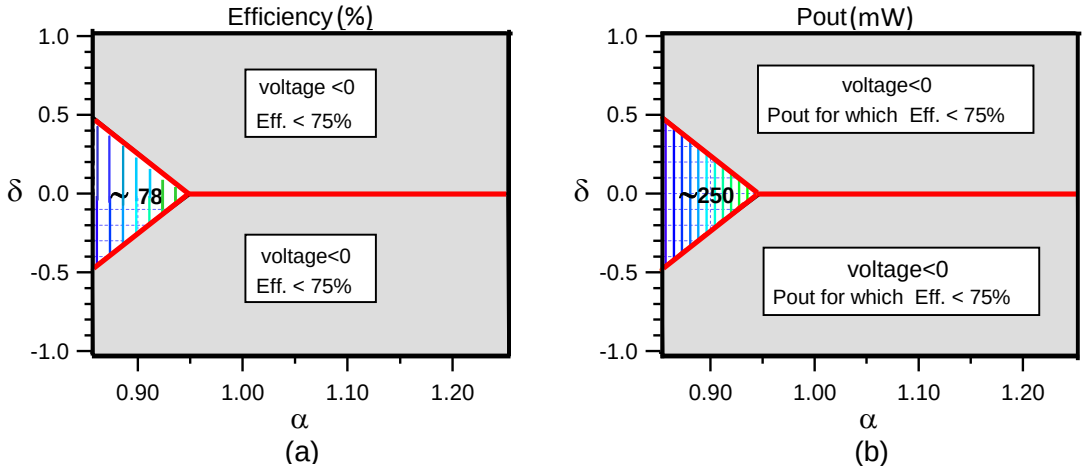

Fig. 4.30 – (a) efficiency and (b) output power contour plot for constant $\beta = \alpha / 1.6$, function of α and δ with $0.85 \leq \alpha \leq 1.3$ and $-0.5 \leq \delta \leq 0.5$ both in steps of 0.1.

4.4.3 Extended Continuous Class-FV Experimental Analysis

As for the standard narrow band Class-F mode and the Continuous Class-FV mode where the terminations are only varied reactively, the Extended Continuous Class-FV mode design space has been explored experimentally on the Cardiff active ELP measurements system [36]. Again, the measurements have been conducted on the 6x50 µm GaAs pHEMT device at 0.9 GHz fundamental frequency and 6 V drain voltage.

Starting from the conventional Class-F state already achieved and explained in Section 4.2 of this Chapter, the theory was experimentally explored for the identified range of δ, α and β with the aim of achieving an even wider design space than the Continuous Class-FV already experimentally presented in Section 4.3. Figures 4.31 and 4.32 show the behaviour of drain efficiency and output power as a function of β and δ. The parameter α has been chosen in order to maintain the maximum range where the voltage waveforms are non-zero-crossing. It can be seen that best performance is achieved for $\beta=\alpha/2$, which is the classic Class-F condition with maximum efficiency of 82.9%. Note that as the parameter β increases, the efficiency and output power decrease, and the range of valid cases (i.e. cases where the voltage is non-zero-crossing and the efficiency is greater than 75%) also decreases. Although the second harmonic impedance has been chosen with a positive real part (i.e. inside the Smith chart), when presenting the appropriate fundamental load in accordance with this new theory the drain efficiency is still kept above the target efficiency of 75%. For X1/R1<-0.7 efficiency drops lower than 75%.

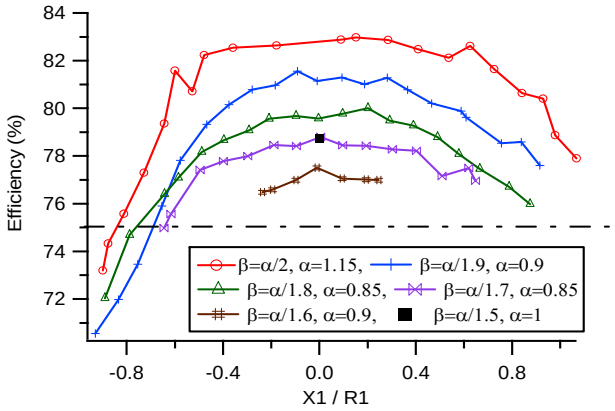

Fig. 4.31 – Measured drain efficiency function of β, α and δ.

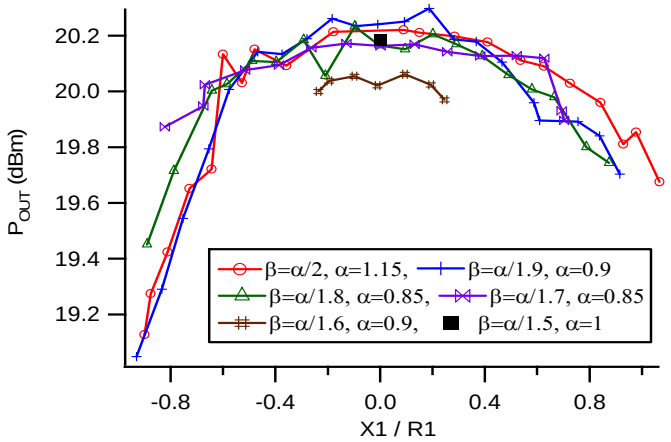

Fig. 4.32 – Measured output power function of β, α and δ.

Fig. 4.33 shows the efficiency function of β and α with constant δ=0. In accordance with the theory, the highest efficiency is achieved for lower values of β (e.g. β=α/2). It also shows that with decreasing α, the efficiency also decreases, and the range where both the efficiency is kept greater than 75% and the voltage is non-zero-crossing decreases with increasing β, as explained theoretically in Sections 4.3.1 and 4.3.2.

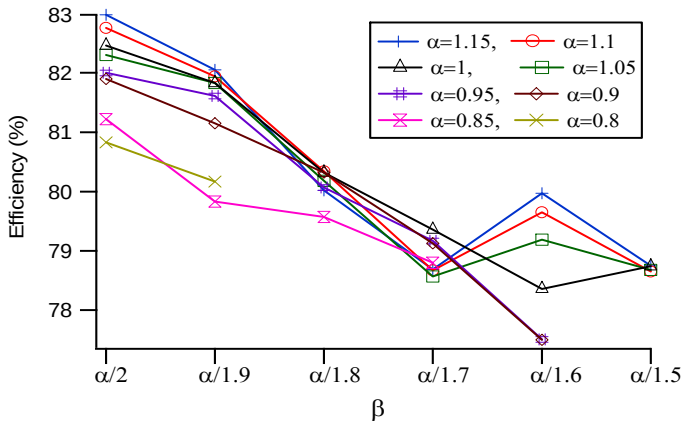

Fig. 4.33 – Measured output power function of β, α and δ.

The new theoretical formulation for the voltage waveforms can incur peak voltages that are greater than twice the supply voltage. Fig. 4.34 shows the variation of peak voltage as the second harmonic impedance is varied over a large design space for the case of fundamental impedance set to 50 Ω. The higher value

zones can be regarded as a potential reliability hazard in PAs, which are designed using entirely empirical tuning techniques. Again, it is important to highlight that this new technique for which an increase of the peak voltage waveforms is revealed (which effectively creates the new design space), can be used for low supply voltage or device technologies with high breakdown voltages such as the emerging devices in AlGaN/GaN technology [42, 44].

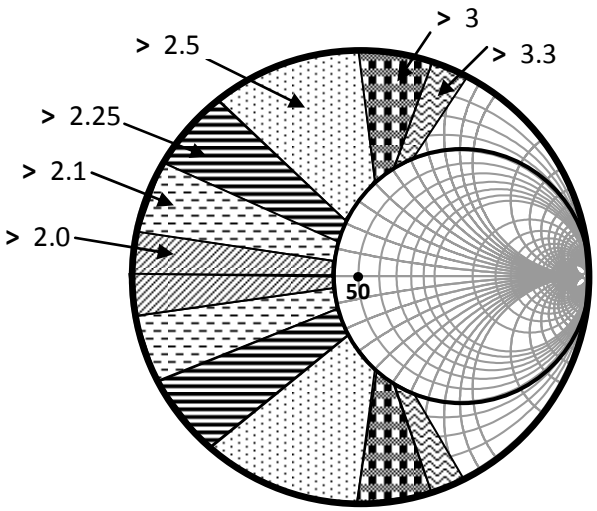

Fig. 4.34 – Peak voltages function of the second harmonic impedances based on a 50 Ω load-line resistance.

4.5 Chapter Summary

This Chapter has initially presented a systematic procedure for engineering voltage and current waveforms for the Class-F mode. Using this procedure it has been demonstrated that very high efficiency states that deliver the expected output power and gain can be obtained. It can be said that the obtained results are very close to the maximum achievable ones when considering the different boundary conditions of the real device.

After that, it has been demonstrated that the systematic measurement procedure can be automated speeding up the overall measurement activity. In this way by using a few measured DC parameters and an appropriate software-predictor, the bias point and fundamental and harmonic impedances can be determined. The revealed bias point and impedances can then be used as a first guess on the measurement system avoiding many sweeps and saving valuable time.

Once the optimum standard Class-F is revealed, the Continuous Class-FV mode and its extension has been experimentally demonstrated. This means that the simultaneous variation of the fundamental and second harmonic terminations from the optimum and short-circuit conditions respectively, the output performance is maintained almost constant, validating the approach.

In addition, a new extended formulation applied to the voltage waveform, named Extended Continuous Class-F has been theoretically and experimentally demonstrated. This leads to different impedance solutions where high efficiency and output power are still maintained thus allowing the realisation of broadband highly power-efficient amplifiers.

4.6 *References*

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Chapter 5

Continuous Class-FV Power Amplifier Realisation

5.1 Introduction

Chapter 3 has presented a detailed theoretical analysis of the overall broadband Continuous modes providing the mathematical formulations and the ideal voltage and current waveforms, while Chapter 4 has been focused on the Continuous Class-FV mode demonstrating experimentally the validity of the new theory on a power transistor through load-pull measurement activity.

To close the loop and verify the actual validity of the Continuous theory on a real PA, the next step, provided in this Chapter, is the design and physical realisation of the highly efficient and broadband Continuous Class-FV power amplifier [1-2]. It will be seen that when designing PAs, especially for a wide band of frequencies, the PA designer has to deal with different issues, for example stability issues, or how to design the output and input matching networks for which the difficulty increases when taking into account high harmonics.

In this Chapter the various steps to follow will be shown, starting from the conventional narrow band Class-F PA design moving to the broadband Continuous Class-FV PA, in order to achieve the highly efficient and broadband PA state.

5.2 Conventional Class-F Design

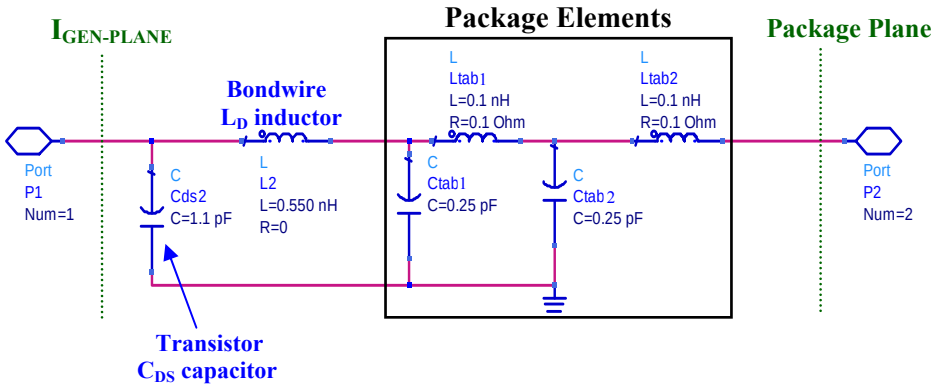
As mentioned on the introduction of this Chapter, so far the Continuous Class-FV theory has been demonstrated through measurement activity. The next step, shown in this Chapter, is the design and the actual realisation of the broadband PA.

For the design of the Continuous Class-FV power amplifier [1] the well-established and accurate model for the CGH40010 10 W GaN (gallium nitride) HEMT (high electron mobility transistor) device from CREE has been used [Appendix B] [3-4]. Simulations have been conducted using Agilent's ADS (advanced design system) CAD (computer added design) software at fundamental frequency F_0=0.9 GHz and drain voltage V_{DS}=28 V. The PA has been realised yielding a very broadband amplifier operating at high efficiency and output power levels normally associated with the narrow band Class-F mode.

Here it will be seen that when moving towards packaged devices and delivering higher power, the de-embedding network plays an important role. This is because in order to understand through waveform engineering the voltage and current waveforms at the $I_{GEN\text{-}PLANE}$, the right de-embedding network must be applied. If not, the output waveforms actually presented at the $I_{GEN\text{-}PLANE}$ will be wrong and even with acceptable voltage and current waveforms the overall output performance will not be optimum.

Fig. 5.1 shows the output de-embedding network applied to the CGH40010 10 W GaN transistor [5]. The elements of packaged transistors can be divided into two main groups: the actual die elements and the package elements [6-7]. At the measurement/package plane the device presents all the parasitic components, this means that the device is presenting both its intrinsic and extrinsic elements as well as the package components. The C_{DS} is the intrinsic parasitic drain-source capacitor which is presented in all solid-state devices while L_D is the extrinsic drain inductor due to the bondwires which interconnect the actual die with the package [8]. It is

important to remember that all the values presented on real transistors are non-linear; however, here a linear behaviour approximation has been adopted in order to facilitate the design [9-11].



Comp	Value	Unit
C_{DS}	1.1	pF
L_D	0.55	nH
Ltab1	0.1	nH
Ltab2	0.1	nH
Ctab1	0.25	pF
Ctab2	0.25	pF

Fig. 5.1 – Output de-embedding network.

When studying the various PA modes through waveform engineering, the waveforms must be presented at the $I_{GEN-PLANE}$, for example half-wave rectified sinusoidal current waveform and square voltage waveform for the Class-F mode. Unfortunately, the $I_{GEN-PLANE}$ is not accessible from outside the package, this means that the measurement plane where the actual voltage and current waveforms can be measured is the outside/package plane as shown in Fig. 5.1. Here, there is no knowledge of waveforms that must be provided in order to obtain the actual Class-F waveforms at the $I_{GEN-PLANE}$. Therefore, in simulations, it is possible to present another network which is symmetrical to the one of Fig. 5.1 but with presenting negative component values as shown in Fig. 5.2. Presenting a mirrored package network with negative values (here called Network 2) will cancel the elements of network 1 (the positive network) providing a transparent overall structure. Now the actual measurement plane will be the $I_{GEN-PLANE}$ (now outside the package), thus allowing waveform engineering to be applied in order to present the desired voltage and current waveforms as in details explained in [5] .

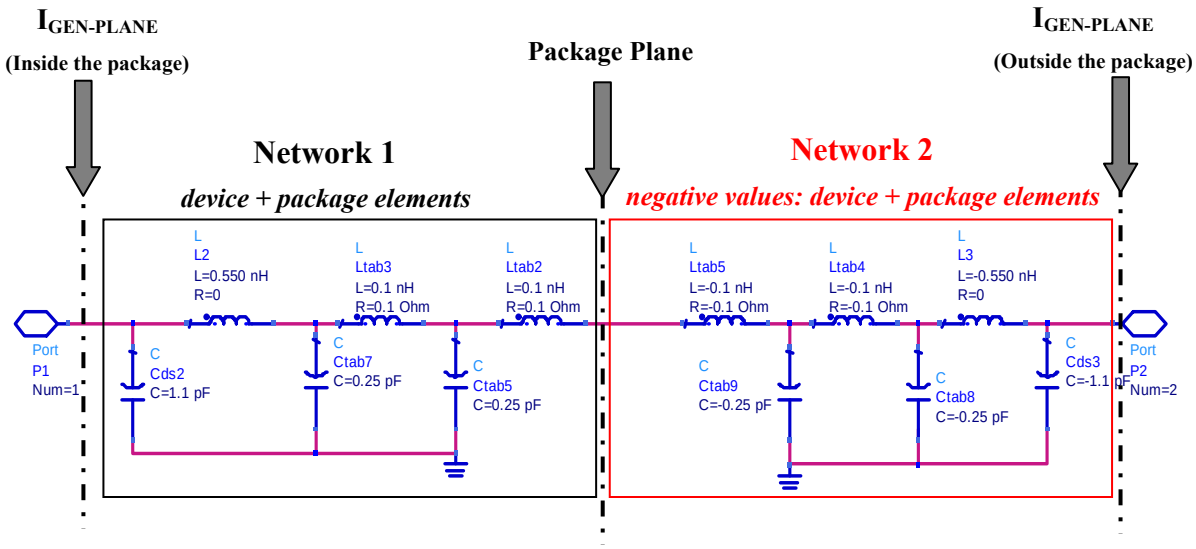


Fig. 5.2 – Output de-embedding network (Network 1) with the mirrored positive network (Network 2) – Overall transparent structure.

Once the right de-embedding network is obtained, the next step is to find the right combination of bias point, input power, fundamental and harmonic terminations for the standard Class-F condition. It is known that the ideal Class-F bias point (equal to the Class-B bias point) is the pinch-off $V_{GS}=V_{TH}$. Fig. 5.3 shows the device DCIV output characteristic (a) for V_{GS} ranking from -3 to 3 in steps of 0.25, and transfer characteristic (b) in this case only for the specific supply voltage V_{DS}=28 V. It can be noted from the transfer characteristic that the device pinch-off point (where the device starts to conduct drain current) is around -2.5 V. This means that in order to present the Class-F bias point $V_{GS}=V_{TH}$=-2.5 V.

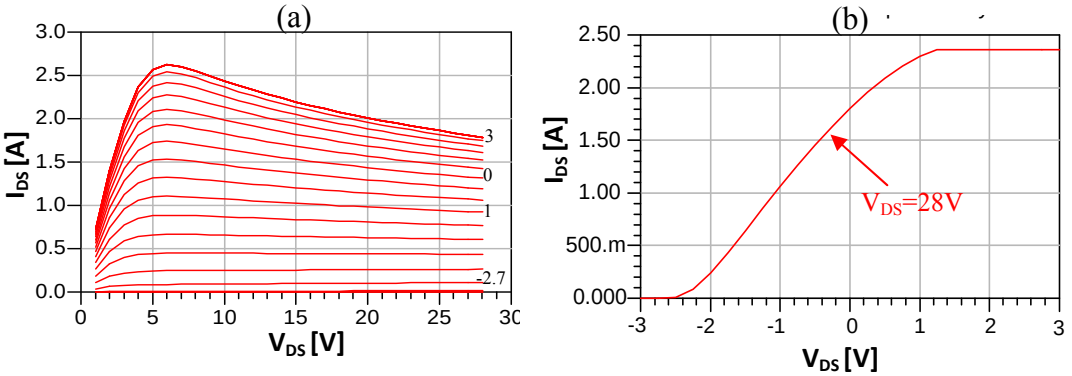


Fig. 5.3 – CREE 10 W GaN HEMT transistor (a) simulated output characteristic, and (b) simulated transfer characteristic.

Unfortunately, as mentioned in the introduction of this Chapter, when designing PAs various difficulties can be met. In the first place, presenting V_{GS}=-2.5 V and

varying the input power and the fundamental impedance with maintaining short-circuited the higher harmonic terminations; the actual output performance was disappointing in terms of drain efficiency. Looking carefully at the output waveforms, it was observed that the actual current waveform presented a conduction angle greater than 180°. This means that the device was biased at its pinch-off at DC but not at its compression point (here around Class-AB bias values), due to some self-bias condition when increasing the input power. The consequence of higher bias point value was greater output power but at the expense of drain efficiency (η), with disappointing values of around η=70%. For the achievement of the half-wave rectified sinusoidal current waveform with 180° conduction angle at around 2 dB of gain compression a bias value of V_{GS}=-4.6V has been found and chosen. Table 5.I and Fig. 5.4 shows the harmonic impedances at both $I_{GEN-PLANE}$ and package plane for the standard narrow band Class-F condition. It can be noted that at the $I_{GEN-PLANE}$ the fundamental and harmonic impedances are presented on the real axes.

TABLE 5.I
FUNDAMENTAL, SECOND AND THIRD HARMONIC IMPEDANCES AT BOTH $I_{GEN-PLANE}$ AND PACKAGE PLANE

$I_{GEN-PLANE}$	
Harmonics	**Impedance Value [Ω]**
F0	44.8 + j*0
2F0	short-circuit
3F0	open-circuit

Package plane	
Harmonics	**Impedance Value [Ω]**
F0	39 + j*11.7
2F0	0.1- j*9
3F0	0.99 + j*119.8

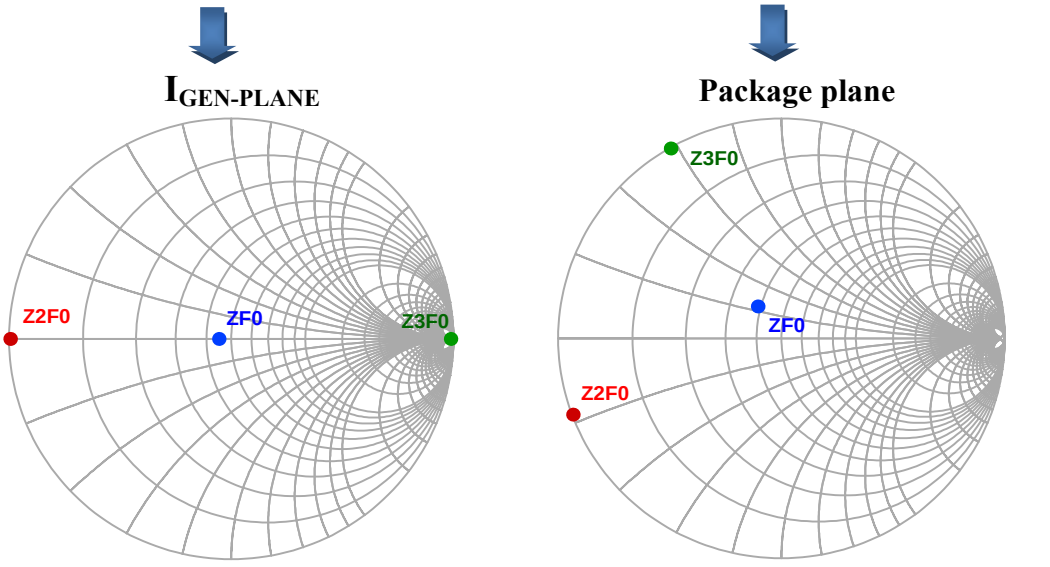
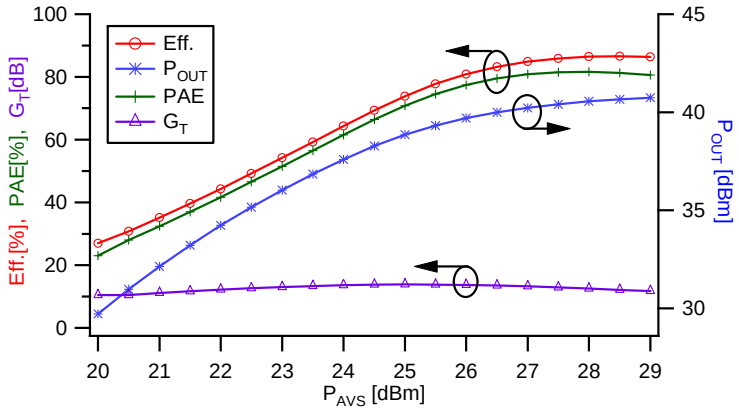


Fig. 5.4 – Smith chart showing F0, 2F0 and 3F0 at both $I_{GEN-PLANE}$ and package plane.

Fig. 5.5 shows the simulated overall output performance in terms of drain efficiency, PAE, output power and transducer power gain (G_T) as a function of the available input power P_{AVS} for a 10 dB dynamic range from P_{AVS} = 20 dBm to P_{AVS} = 29 dBm in steps of 0.5 dB.

At around 2 dB of gain compression (P2 dB), at which the transducer power gain is G_T = 11.7 dB, a drain efficiency η = 86.4%, power added efficiency PAE = 80.6% and output power P_{OUT} = 40.7dBm have been achieved.



Param.	Values
η	86.4%
PAE	80.6%
P_{OUT}	40.7dBm
G_T	11.7dB

Fig. 5.5 – Simulated drain efficiency, PAE, output power and transducer power gain vs. available input power.

The output voltage and current waveforms for the same 10 dB input power sweep are shown in Fig. 5.6.

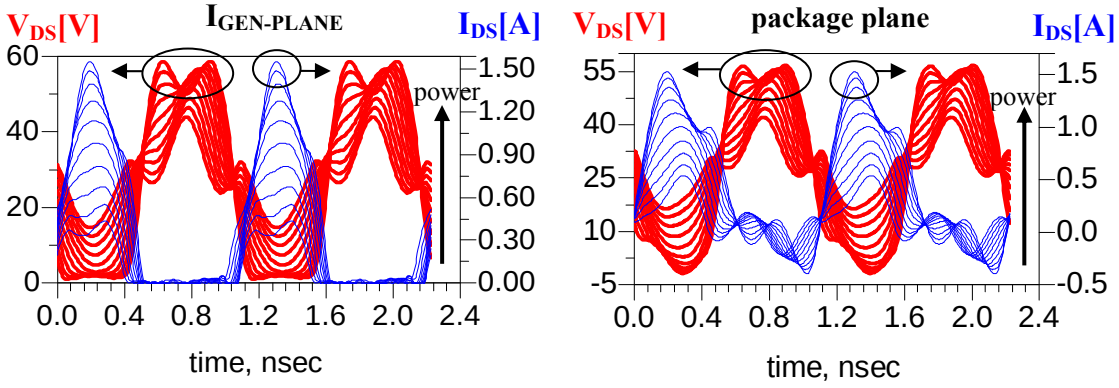


Fig. 5.6 – Simulated voltage and current waveforms at both $I_{GEN-PLANE}$ and package plane.

Here, the half-wave rectified sinusoidal current waveform and truncated three harmonic square voltage waveform are presented at the $I_{GEN-PLANE}$ with peak values up to 1.55 A and 57.6 V respectively. The achieved peak voltage waveform is very close to the theoretical ideal Class-F peak voltage $V_{peak} = 2*V_{DC} = 2*28 = 56$ V. Fig. 5.7 shows the load-line at both reference planes for P_{AVS}=29 dBm (P2 dB).

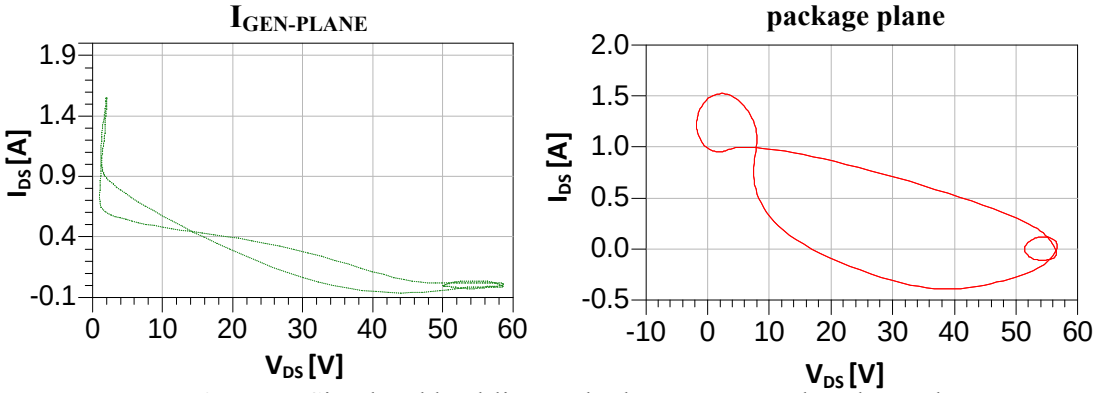


Fig. 5.7 – Simulated load-lines at both $I_{GEN-PLANE}$ and package plane.

Fig. 5.8 shows the spectrum for the first five harmonics for both voltage and current waveforms (magnitude and phase) at 29 dBm of drive level, for which the device is around 2 dB into compression delivering a maximum efficiency of 86.4%. Here, with the voltage waveform being a square shape, the second harmonic voltage content is minimised (as well as the higher even harmonic content), while for the current waveform, being a half-wave rectified sinusoidal shape, the third harmonic content is close to zero (as well as the higher odd harmonic content). The Class-F DC, fundamental, second and third harmonic content values for both voltage and current waveforms are shown in Table 5.II.

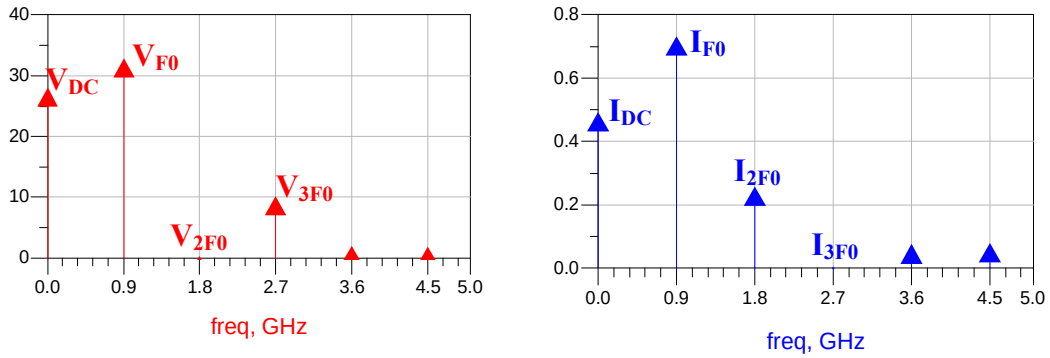


Fig. 5.8 – Spectrum showing first five harmonic V and I contents at the $I_{GEN-PLANE}$.

TABLE 5.II
DC, FUNDAMENTAL, SECOND AND THIRD HARMONIC MAGNITUDE AND PHASE FOR BOTH VOLTAGE AND CURRENT

V_{DC}	V_{F0} [V]	V_{2F0} [V]	V_{3F0} [V]	I_{DC}	I_{F0} [A]	I_{2F0} [A]	I_{3F0} [A]
27.95 ∟0°	32.6 ∟109.5°	0 ∟-14.1°	9.9 ∟148.7°	0.49 ∟0°	0.73 ∟-70.5°	0.25 ∟-143.7°	0 ∟-80.8°

5.3 Continuous Class-FV Design

In previous paragraph the conventional narrow band Class-F mode has been achieved revealing a bias point V_{GS}=-4.6 V, available drive power P_{AVS}=29 dBm and fundamental and harmonic terminations Z_{F0}=44.8+j0, Z_{2F0}=short-circuit and Z_{3F0}=open-circuit at the $I_{GEN\text{-}PLANE}$ by shifting the reference plane through the de-embedding network. Once the standard Class-F state has been achieved it is possible to carry on towards the design of the Continuous Class-FV PA.

5.3.1 Continuous Class-FV Terminations for the 10 W GaN HEMT device

Starting from the optimum fundamental impedance Z_{F0}=44.8+j0, short-circuit and open-circuit second and third harmonic impedances respectively, the Continuous Class-FV theory explained in detail in Chapter 3 and demonstrated through measurements in Chapter 4 has been applied.

From the theoretical voltage waveform

$$v_{cont\_classFV}(\vartheta)=\left(1-\frac{2}{\sqrt{3}}\cos\vartheta\right)^2\cdot\left(1+\frac{1}{\sqrt{3}}\cos\vartheta\right)\cdot\left[1-\delta\sin\vartheta\right] \qquad (5.1)$$

and by presenting a constant half-wave rectified sinusoidal current waveform:

$$i_{cont\_classFV}(\vartheta)=I_{peak}\cos\vartheta \qquad 0<\vartheta<\pi/2,\quad (3/2)\pi<\vartheta<2\pi,$$

$$=0 \qquad 0<\vartheta<\pi/2, \qquad (5.2)$$

the third harmonic impedance results in a constant open-circuit, while the fundamental and second harmonic impedances will be functions of the reactive part X_L which is a function of the key operator δ:

$$Z_{F0} = R_L + j \cdot X_L , \tag{5.3}$$

$$Z_{2F0} = 0 - j \cdot \frac{\pi}{2} \cdot X_L , \tag{5.4}$$

$$Z_{3F0} = \infty , \tag{5.5}$$

with R_L being the optimum fundamental resistive impedance value of 44.8 Ω. As explained in Chapter 3, the reactive part X_L must be varied in a certain range in order to keep the voltage waveform above zero. In this case, for the 10 W GaN HEMT device X_L = ± 38.8 Ω are the minimum and maximum values allowed. Beyond those values, overall output performance reduction would be presented.

Fig. 5.9 (a) shows the Continuous Class-FV range of fundamental and second harmonic impedances at the $I_{GEN-PLANE}$ as well as the fixed open-circuit third harmonic load for which the optimum output performance will be maintained constant. The fundamental and harmonic terminations are shifted to the package plane (b) through the use of the de-embedding network as presented in the previous paragraph. In this case, the new design space has been obtained when maintaining a constant drive power of 29 dBm.

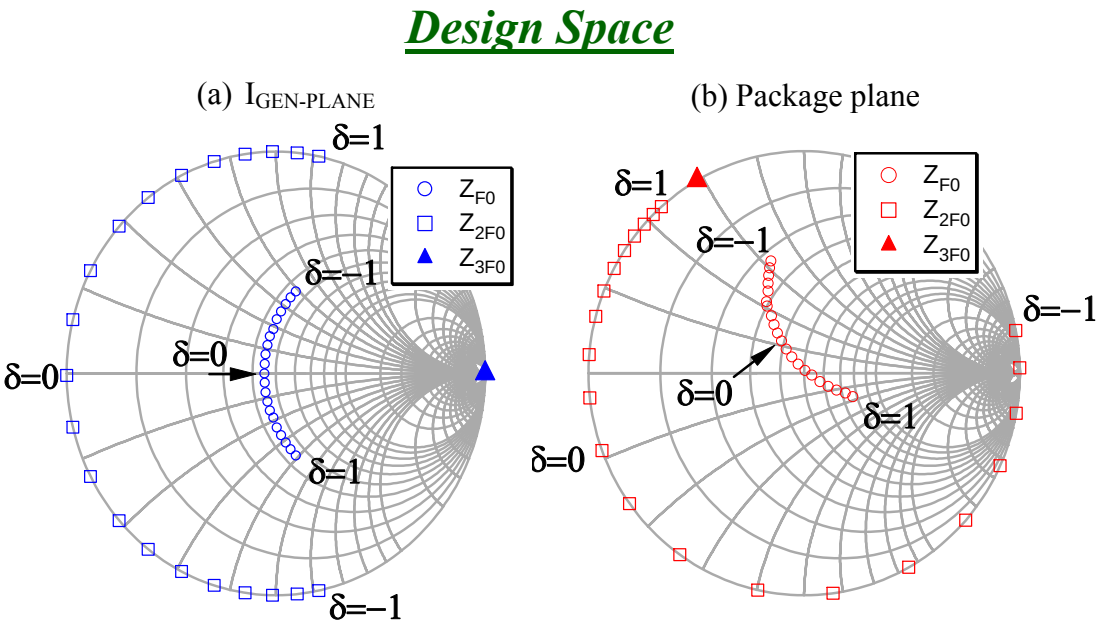


Fig. 5.9 – Simulated Continuous Class-FV first target impedances for the 10W GaN device at the (a) $I_{GEN-PLANE}$ and (b) package plane.

Fig. 5.10 shows simulated engineered current (blue) and voltage (red) waveforms at the $I_{GEN-PLANE}$ for first three harmonic terminations, for the conventional Class-F mode where δ=0 (dotted lines) and for the Continuous Class-FV mode for δ=-1 (solid lines). It can be noted that when varying the parameter δ the current waveform is maintained half-wave rectified sinusoidal, whilst the voltage waveform presents a significantly higher peak value for the Continuous mode, which must be accommodated. The approach does however provide a much wider design space where output power and efficiency are maintained constant [12].

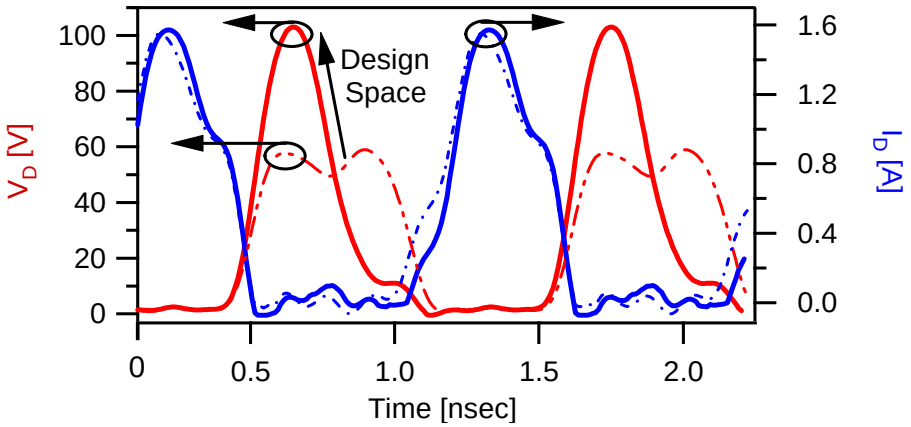


Fig. 5.10 – Simulated Continuous Class-FV voltage (red) and current (blue) waveforms for the standard Class-F mode (dotted line) and for the Continuous Class-FV mode (solid line) for δ=-1.

Fig. 5.11 shows the Continuous Class-FV output performance in terms of drain efficiency, output power, power gain and transducer power gain as a function of δ, which means a function of the target fundamental and harmonic terminations of Fig. 5.9. These output parameters have been called target parameters (i.e. Target η) as they are achieved from the target fundamental and harmonic loads of Fig. 5.9. As it can be noted, drain efficiency and output power are maintained at almost constant level, above 80% with maximum peak of 88.47% for δ=-0.7 and around 40 dBm with maximum value of 40.8 dBm (11.9 W) respectively for the entire range of δ. The transducer power gain G_T, defined as the ratio between the power delivered to the load and the power available from the source [13], is maintained constant as well at around 11 dB with maximum peak value up to

11.8 dB for δ=-0.2, while interestingly the power gain G, defined as the ratio of the power dissipated to the load to the power delivered to the input of the device when this is conjugately matched to the source impedance [13-14], decreases with increasing δ. Here it can be noted that for δ=0 the gain is G=20.3 dB; when varying δ positively it decreases while for δ smaller than zero it increases. This is due to the fact that the variation of δ leads to a different voltage waveform, therefore the fundamental and/or the higher harmonics can be re-injected at the input of the device through the feedback capacitor C_{GD}, causing stability issues. This can be avoided by inserting a series input resistance in the input, in this case with value of 50 Ω, or through the proper design of the input matching and bias networks.

However, the target impedances obtained from the Continuous Class-FV theory provide an almost constant behaviour in terms of drain efficiency, output power and transducer power gain for a wide design space.

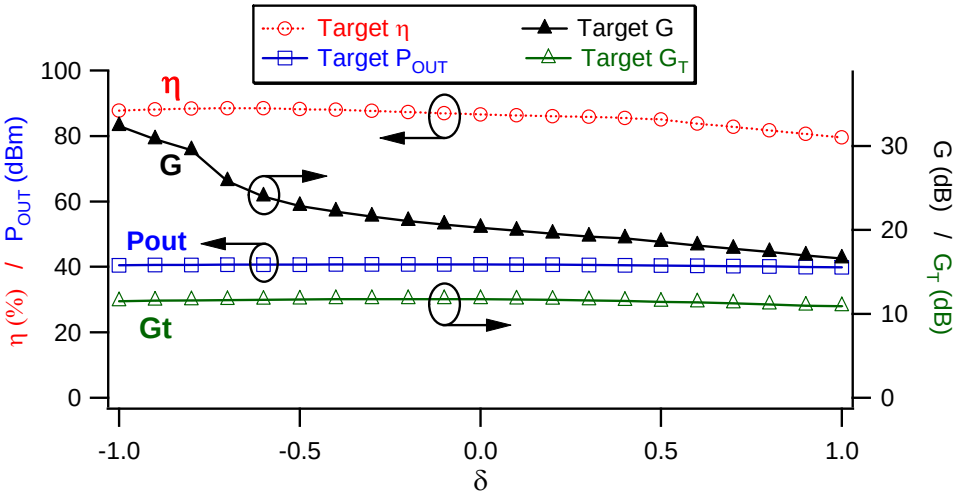


Fig. 5.11 – Simulated Continuous Class-FV η, P_{OUT}, G and G_T for δ varying between -1 and 1 in steps of 0.1.

5.3.2 Output matching network

Once the desired fundamental and harmonic impedances have been revealed, leading to the high power efficiency states with varying δ, the next step is to design the actual output matching networks capable of synthesizing the various terminations provided in first place. So far the design process has been evolved for the fundamental frequency F_0=0.9 GHz. This means that by maintaining the

same constant primary frequency F_0=0.9 GHz and varying the simple parameter δ, the range of fundamental and second harmonic terminations, as well as the constant third harmonic load point, have been carried out providing the design space. The different range of load solutions (fundamental and harmonics) achievable through the Continuous mode theory are target points which can then be designed and achieved in the frequency domain by designing the proper matching networks. In fewer words, the impedance points are translated into a useful frequency design space when designing power amplifiers.

The Continuous Class-FV matching network design starting point was the Class-J mode. In the Class-J theory and design, the two impedances points for both fundamental and second harmonic were the ones for δ=0 and δ=-1. As explained in detail in [5, 14] and in the literature review of this thesis, when the Class-J was presented in the first place, the theoretical points giving the same output performance in terms of power and efficiency were two: the one for δ=0 (Class-B) and the one for δ=-1. Here the design strategy was to give higher priority to the fundamental load allowing to the second harmonic impedances more freedom, as long as such a load was in the right area in accordance with the Class-J theory [15-16]. Only after the Class-J mode had been developed was the Class-BJ presented. Here it has been theoretically and experimentally demonstrated that from δ=0 to δ=±1 there are infinite solutions where the output performance is maintained constant [17]. Therefore, in this Continuous Class-FV case, in contrast to the Class-J design, even if the fundamental load has the biggest impact on the overall output performance, the second harmonic termination was designed with the aim of reaching the target points as well. Besides, in this case the third harmonic impedance should be theoretically open circuit. When designing PAs it is not easy to maintain constant impedances with varying frequency. Therefore while theoretically the third harmonic impedance should be a constant open-circuit point, here very high power efficiency for a wideband of frequencies has been achieved when varying the third harmonic termination on the edge of the Smith chart. The variation of the third harmonic load will be explained in more detail in the next paragraph of this Chapter when presenting what has been termed “Continuous Class-FV3” mode.

When designing standard narrow band Class-F power amplifiers, in order to present the required open-circuit and short-circuit third and second harmonic termination with an optimum fundamental impedance, the matching network of Fig. 5.12 must be presented. By using proper wave length open and short stubs it is possible to easily achieve the Class-F fundamental and harmonic termination as explained in a detailed analysis in [18-19].

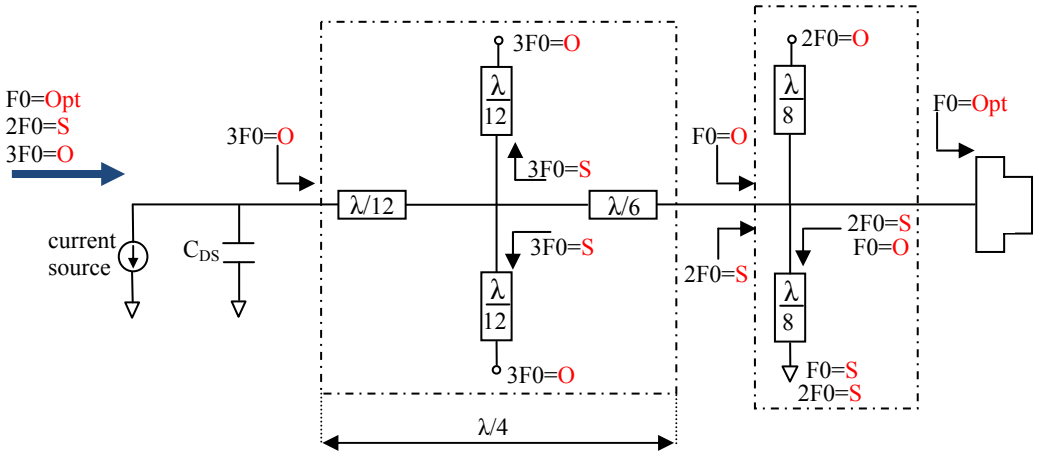


Fig. 5.12 – Theoretical Class-F matching network.

When designing broadband power amplifiers (bandwidth BW>30%), the design of the output matching network becomes much more challenging. In this case it is not possible to present the simple open stub quarter wave length λ\4 at the third harmonic termination (λ\12) and a short stub quarter wave length at the second harmonic termination (λ\8) in order to have an open-circuit and short-circuit third and second harmonic loads respectively. Here, as the target is to present a "range" of fundamental and second harmonic terminations and not frequency points, a variation of each microstrip line (MLIN) element either in terms of width (W) and length (L), will lead to a different behaviour for all the harmonics. This means that if presenting the right range of third and/or second harmonic impedances, when designing for the fundamental load range, a variation of each MLIN will result in a variation of the second and/or third harmonic impedances range as well. Therefore, using the target loads, which should be emulated as closely as possible by the output matching network, the designer can

provide different network topologies [20-21]. The full ADS schematic is presented in Appendix F.

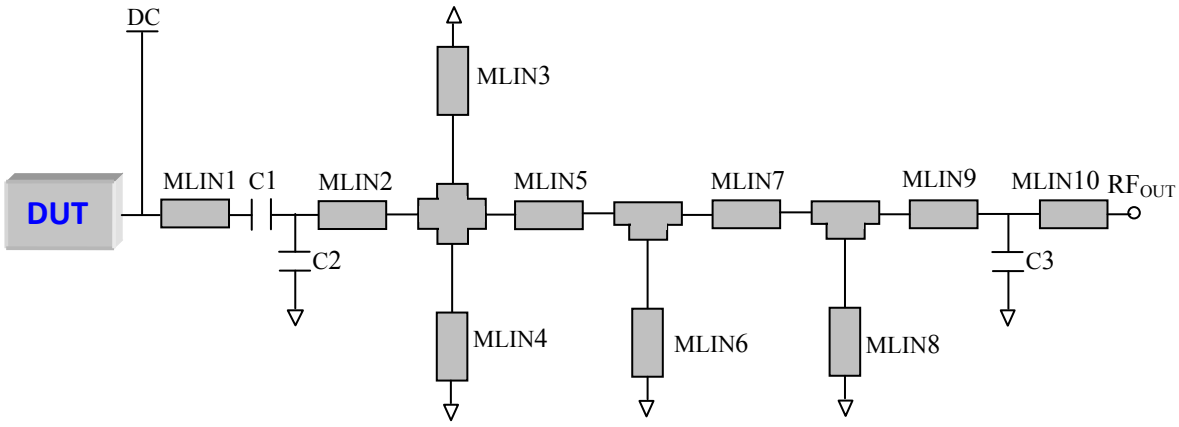


Fig. 5.13 – Continuous Class-FV output matching network topology.

The output matching network used for the realisation of this Continuous Class-FV PA presented in this thesis is shown in the schematic of Fig. 5.13. Again, the complexity of this network is mainly due to two aspects: the importance of fitting the network behaviour to the target range loads for both the fundamental and second harmonic impedance, as well as the accuracy of controlling the third harmonic component without mismatching the first two.

Another aspect of designing PAs is the stability issue. The stability problem is one of the most important and unfortunately undesirable aspects to take into consideration. This is due to the loop caused from the feedback, where the output signal is coupled into the input side as previously stated. Here, the presence of the correct phase and magnitude causes oscillations at certain frequencies. This means that the RF power transistor shows a negative resistance at the input of its bias port.

The 10W GaN power transistor used for this design was unstable for certain frequencies when presenting the Continuous Class-FV impedances. The stability issue is probably due to the fact that for certain frequencies the voltage waveforms present very high peak and therefore this would lead to the drain current floating from the output side to the input side through the C_{GD} capacitor. However, no detailed investigation has been conducted on the stability topic coupled with the

Continuous mode theory. Further investigations can be undertaken in future works. Such oscillation was avoided by simply inserting a 50 Ω series resistance in the input of the transistor thus satisfying the *Rollet's condition* [13]. However, the higher the power and the frequency are, the more pronounced the oscillations would be, meaning that a higher input resistance should be used to overcome such oscillations. Unfortunately in this case higher drive power would be needed with the disadvantage of decrease in gain. For this reason, the PA designer needs to investigate and design the proper input matching and bias networks in order to solve the problem and make the PA stable. Stability issues can be revealed at both low and high (operative) frequencies and above. In order to have a stable PA, the design must be stable for all frequencies (even the ones outside the band of interest). At the band of interest, the stability problem can be solved by introducing at the input a series resistance (in this case 50 Ω) as oscillations are mainly due to the fact that negative resistance are revealed at the input side of the transistor. However this would lead to lower overall gain. At the low frequency (up to few hundreds MHz) as well as at the high frequencies, the stability issue is mainly due to the bias insertion networks [1]. Therefore, it is very important to design the correct bias network in order to avoid oscillation issues. In this case, for the choice of the bias network elements, the standard network (slightly simplified) and decoupling capacitor values given from the CREE datasheet [Appendix B] have been used in both input and output port.

One aspect which has not been so far taken into account is the input matching network which is coupled with the input bias network design. The aim of designing an input matching network is to avoid input mismatch and to reach the desired output power with minimum drive power level, resulting in maximum gain. However, this novel design has been focused on the output matching network, which demonstrates that providing the right combination of fundamental and harmonic impedance points, in accordance with the mathematical theory, multiple solutions delivering constant output power and drain efficiency can be achieved. Nevertheless, in this case an RC parallel network has been used in the input side to mainly provide a constant flat gain along the frequency band, as shown later in Fig. 5.18, and to avoid oscillation issues as previously mentioned.

Fig. 5.14 shows a Smith chart presenting the first three harmonic target terminations as well as the output matching network behaviour. The fundamental impedance range varies from 0.5 GHz to 1.2 GHz, and as it can be noted, the output matching network fundamental load behaviour is in good agreement with the appropriate target loads. The required second harmonic reflection coefficient needs to change rapidly to present the high reflection necessary for the Continuous Class-FV mode. However, despite the resulting resistive second harmonic load, the overall performance does not degrade substantially. This is due to the fact that, although presenting a resistive second harmonic termination, by adjusting the fundamental load in accordance with the "Extended Continuous Class-F" theory, satisfactory output power and drain efficiency performance can be achieved. The Continuous Class-FV theory leads to a variation in only fundamental and second harmonic termination while maintaining a constant open-circuit third harmonic load. Therefore, when this Continuous Class-FV PA was designed, there was no knowledge on where the third harmonic impedance range should be. In this design, to keep expected output performance over bandwidth, it has been found that the third harmonic termination has to stay "somewhere" close to the edge of the Smith chart (Γ=1). However, as mentioned earlier, the theoretical explanation of this concept will be presented through theoretical analysis and measurement in Section 5.4 of this Chapter.

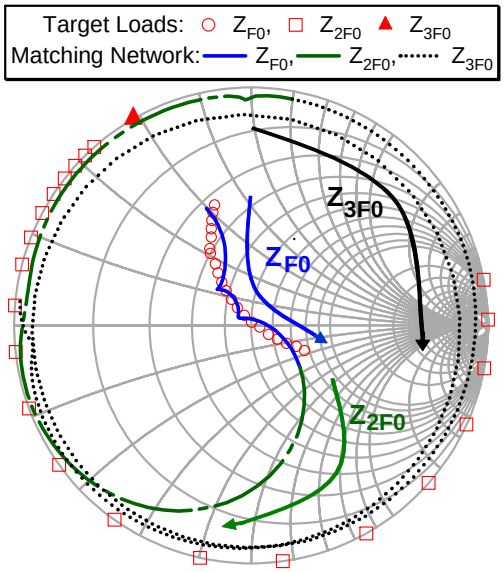


Fig. 5.14 – Continuous Class-FV target loads and output matching network behaviour.

Once the design has been completed the next step before the actual physical realisation is the Momentum simulations. This step is very important as it takes into account the various electromagnetic field effects. For the Continuous Class-FV PA momentum simulation an RT/duroid 5880 substrate has been used. After the Momentum simulations the overall output performance, especially in terms of efficiency, was slightly degraded. Here, small adjustments have been made on the matching network microstrip lines in order to improve the overall output performance. Fig. 5.15 shows the Continuous Class-FV layout as well as the substrate RT/duroid 5880 parameters used.

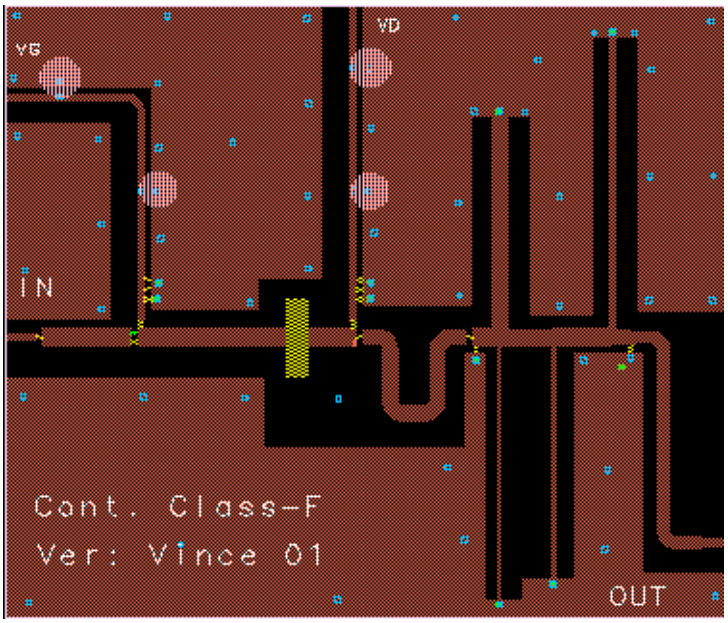
Layout	**RT/duroid 5880**		
	Parameter	**Unit**	**Name**
	H=0.508	mm	Thickness
	εr=2.2		Relative constant dielectric
	T=17.5	μm	conductor thickness
	Mur=1		relative permeability
	Cond=5.961e7		conductor conductivity
	TanD=0.0009		dielectric loss tang
	Hu=3.9x10^{34}	mil	cover height
	R=0	mm	Rough

Fig. 5.15 – Continuous Class-FV layout and substrate RT/duroid 5880 characteristic.

Fig. 5.16 shows the Continuous Class-FV simulated performance when using the matching network of Fig. 5.13. Here the drain efficiency is greater than a target minimum value of 70% with maximum value up to 83.4% from 0.52 GHz to 1.16 GHz. In this range of frequencies the output power is maintained at

an almost constant level around 40 dBm as well as the transducer power gain with an average value of 11 dB.

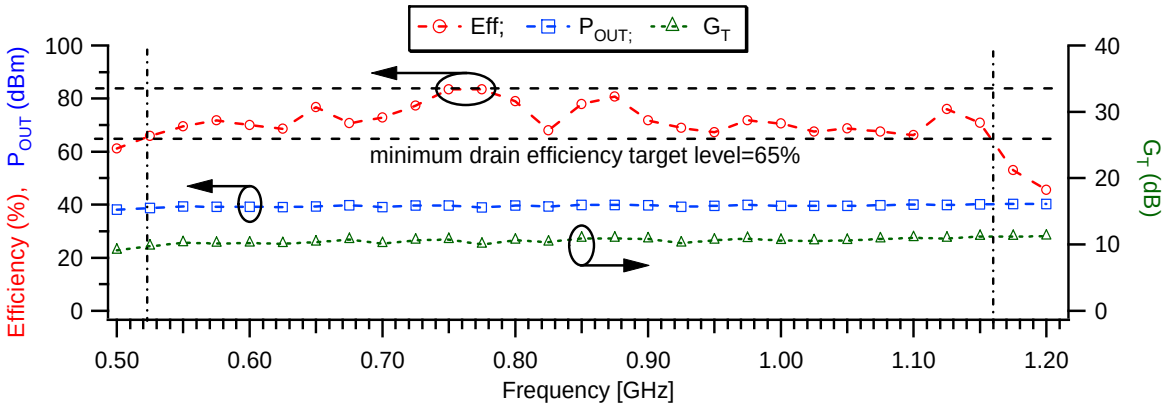


Fig. 5.16 – Simulated Continuous Class-FV drain efficiency, output power and transducer power gain as a function of frequency.

5.3.3 Continuous Class-FV PA Realisation

Once the CAD design has been completed, the next step is the physical implementation of the Continuous Class-FV power amplifier as shown in the photo of Fig 5.17 [1] with the PA size of 11.6 x13.7 cm^2.

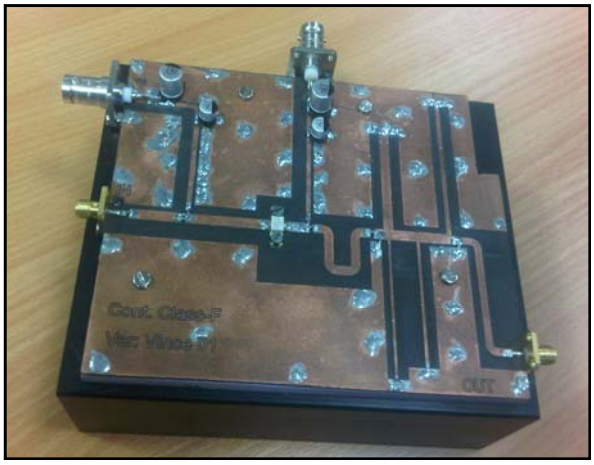


Fig. 5.17 – Photo of the realised Continuous Class-FV 10 W power amplifier (size 11.6x13.7 cm^2).

The broadband Continuous Class-FV PA measured output performance is shown in Fig. 5.18. Here, the simulated performance (of Fig. 5.16) is displayed too in order to compare simulated (dotted lines) and measured (solid lines) results. The PA delivers efficiency greater than 65% with maximum peak up to 80% (average efficiency of 74%) over a wide band of frequencies from 0.55 GHz to

1.1 GHz resulting in an octave (66.6%) bandwidth. In this range of frequencies the output power is greater than 39.3 dBm (8.5 W) with a maximum value of 41.2 dBm (13.2 W), with an average power of 40.2 dBm = 10.5 W. The average transducer power gain is around 11 dB, from 9.5 dB to 12 dB, across the bandwidth. Besides, the PA performance shows that for a smaller range of frequencies, ranging from 0.55 to 0.925 GHz, higher efficiency greater than 70% is obtained resulting in around 51% of bandwidth.

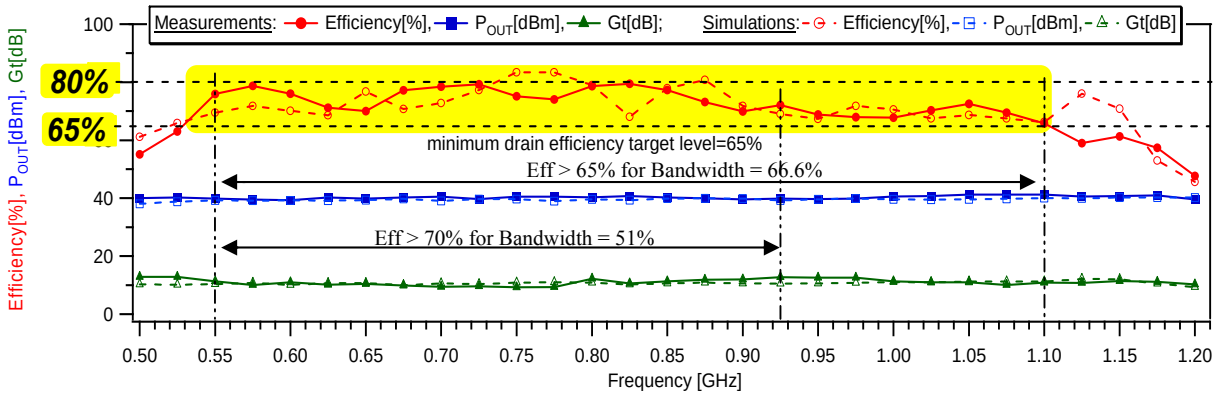


Fig. 5.18 – Measured (solid lines) and simulated (dotted lines) Continuous Class-FV drain efficiency, output power and transducer power gain function of frequency.

Figures 5.19, 5.20 and 5.21 show the drain efficiency, output power and the gain of the Continuous Class-FV PA versus the input power sweep (15 dB dynamic range) for the lower frequency F_L=0.55 GHz, the centre frequency F_C=0.825 GHz and the upper frequency F_H=1.1 GHz respectively.

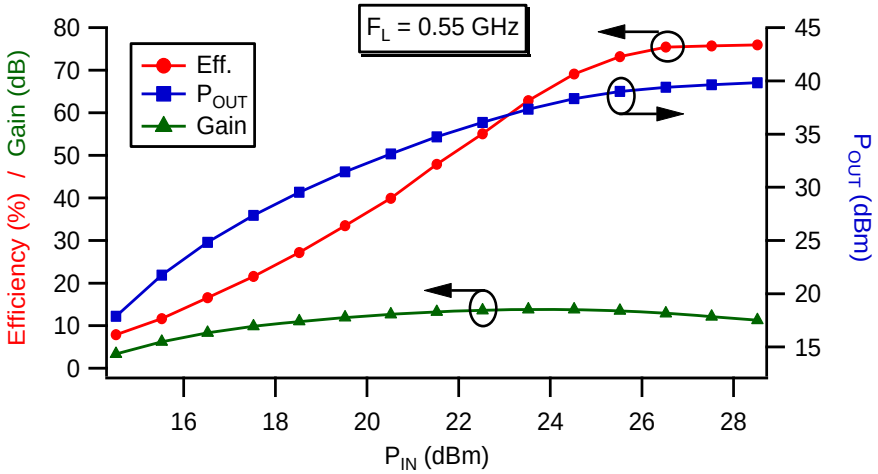


Fig. 5.19 – Measured Continuous Class-FV drain efficiency, output power and gain at the lower frequency F_L=0.55 GHz as a function of input power.

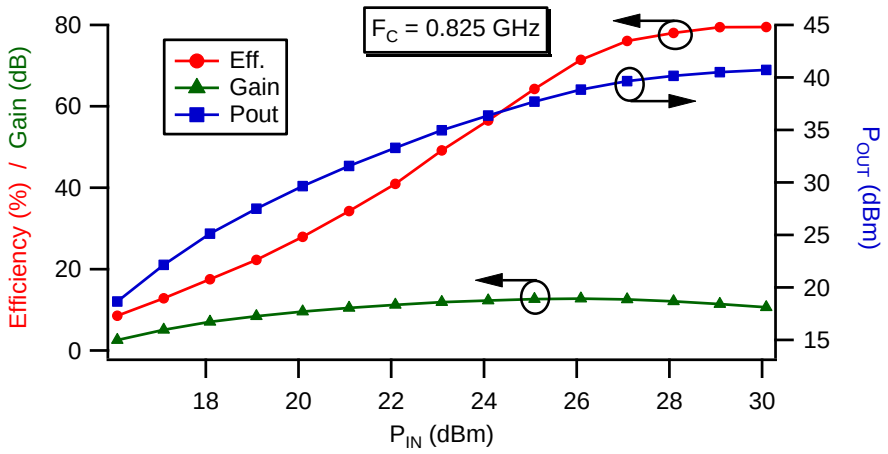


Fig. 5.20 – Measured Continuous Class-FV drain efficiency, output power and gain at the centre frequency F_C=0.825 GHz function of input power.

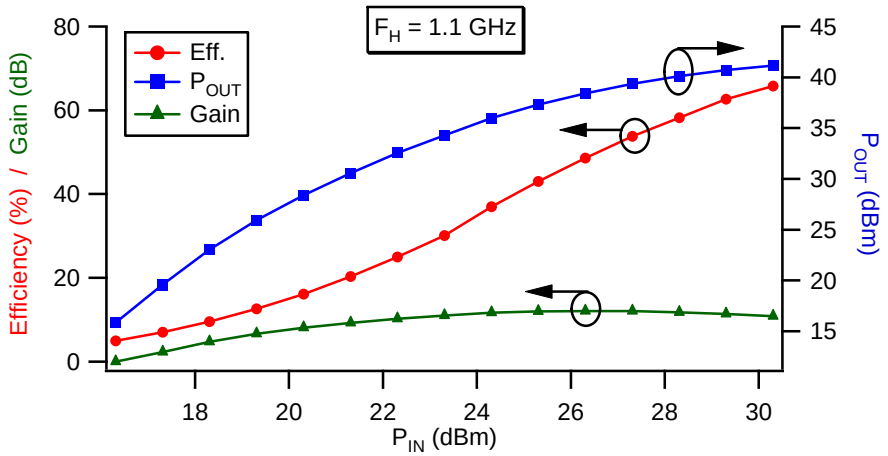


Fig. 5.21 – Measured Continuous Class-FV drain efficiency, output power and gain at the upper frequency F_H=1.1 GHz function of input power.

5.3.4 Continuous Class-FV Linearity performance

This thesis has not been focused on linearity investigation as the main focus is to improve the power-efficiency state for a wideband of frequencies through the new Continuous Mode technique so far explained. However, some information of the Continuous Class-FV linearity performance is reported in this paragraph. As known and already mentioned in Chapter 2 of this thesis, efficiency and linearity are two inversely proportional parameters. This means that the higher the efficiency is, the lower the linearity will be and vice-versa. In fact, the Class-A PA is the most linear mode but with a maximum theoretical efficiency of 50%.

The Class-F mode for example can ideally reach efficiency up to 100% (when considering infinite harmonics and V_{knee}=0) but the high efficiency state is achieved thanks to the presence of the higher harmonics which will inevitable degrade the linearity. Therefore, the Class-F as well as the Continuous Class-FV modes are by definition highly efficient but non-linear power amplifiers.

Despite the non-linear behaviour of these modes, there are different linearization techniques that can significantly improve the linearity of a highly efficient PA [22-24]. In this case, for the realised Continuous Class-FV PA it will be shown the final linearity performance without and with a "generic" predistortion technique [25].

Initially, the linearity characterisation of the PA has been exploited without the use of any predistortion technique. Here, a GSM (Global System for Mobile Communications) test signal was used with a modulation frequency of 200 KHz and the output spectrum measured at around 7 dB output power BO (Back Off) from the 2 dB of gain compression where the average power and drain efficiency were around 35 dBm and 35-45% respectively. Figures 5.22, 5.23 and 5.24 show the ACP (adjacent channel power) measurement results at three different frequencies: lower frequency F_L=0.55 GHz, central frequency F_C=0.83 GHz and upper frequency F_H=1.1 GHz respectively. Table 5.III sums up the ACPR (Adjacent channel power ratio) referred to the 200 KHz GSM signal for the lower, centre and upper frequency as well as for the frequencies ranking from 0.6 GHz to 1 GHz in steps of 0.1 GHz. As it can be noted from those figures as well as from Table 5.III, for the different frequencies the ACPR is quite low compared with the standards adopted for the modern wireless communication of around -45 dBc [26].

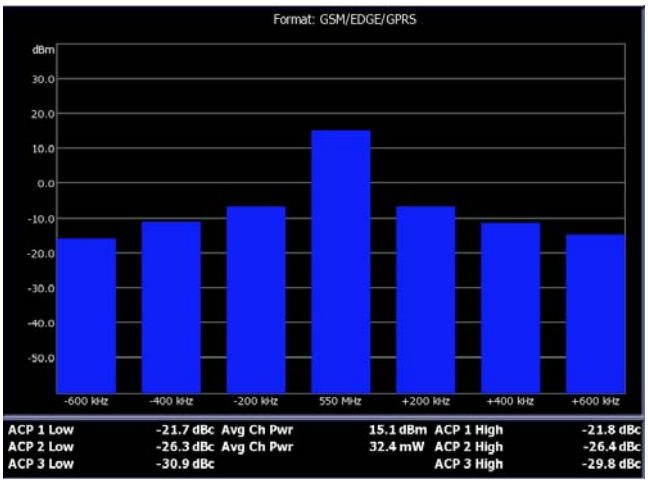


Fig. 5.22 – Measured ACP for a 200 KHz GSM signal at centre frequency 0.55 GHz without using predistortion.

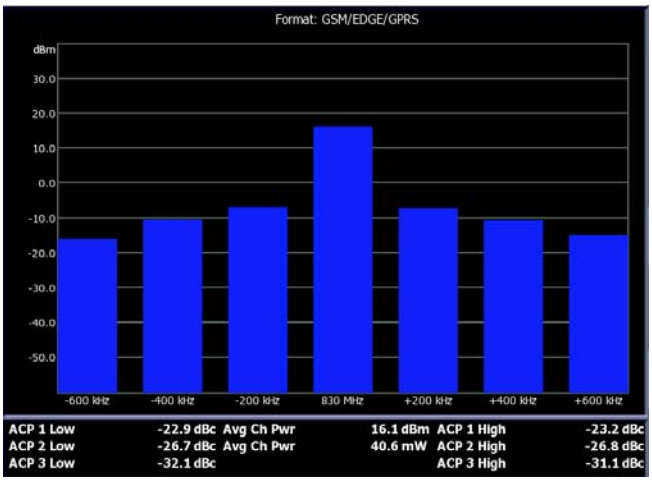


Fig. 5.23 – Measured ACP for a 200 KHz GSM signal at centre frequency 0.83 GHz without using predistortion.

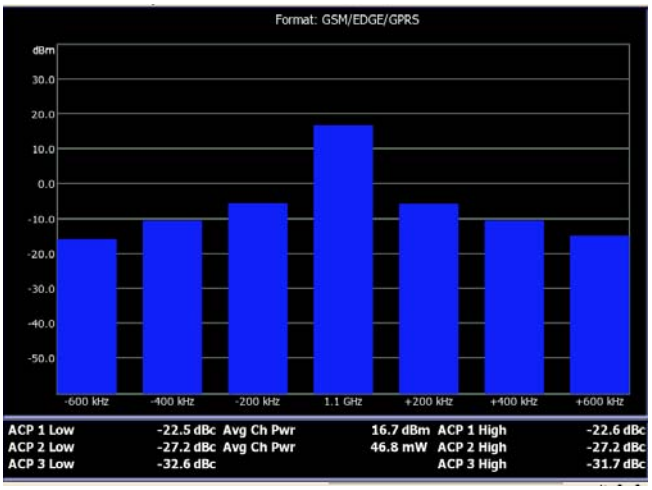


Fig. 5.24 – Measured ACP for a 200 KHz GSM signal at centre frequency 1.1 GHz without using predistortion.

TABLE 5.III
SPECTRUM CONTENT VALUES WITHOUT USING PREDISTORTION

Freq (GHz)	ACP 1 Low (dBc)	ACP 1 High (dBc)	ACP 2 Low (dBc)	ACP 2 High (dBc)	ACP 3 Low (dBc)	ACP 3 High (dBc)
0.55	-21.7	-21.8	-26.3	-26.4	-30.9	-29.8
0.6	-22.5	-22.6	-26.3	-26.2	-30.9	-30.1
0.7	-22.5	-22.4	-26.4	-26.7	-31.5	-30.5
0.8	-22.8	-22.8	-26.6	-26.5	-31.9	-31.3
0.83	-22.9	-23.2	-26.7	-26.8	-32.1	-31.1
0.9	-22.7	-22.9	-26.5	-26.6	-31.8	-31.1
1	-22.9	-22.9	-27.4	-27.2	-34.2	-34
1.1	-22.5	-22.6	-27.2	-27.2	-32.6	-31.7

Later, a "generic" predistortion technique, which will not be discussed in this thesis but discussed elsewhere [25], was applied. In this case the investigation was carried out using a 10 MHz LTE (Long Term Evolution) test signal at 0.8 GHz of frequency. Here the PA was delivering around 27 dBm of average output power and as it can be noted from the Fig. 5.25 as well as from Table 5.IV, the ACPR for the 10 MHz bandwidth signal was reduced from around -17 dBc to around -44 dBc after applying the predistortion. Therefore, the improvement in linearity is approximately 27 dBc in comparison with the output spectrum without the use of the generic predistortion.

In this Section it is important to highlight that these broadband/Continuous modes, for which reactive terminations are provided for fundamental and harmonic impedances, can be predistorted, thus improving the overall linearity performance. In this case the improvement is from around -17 dBc to around -44 dBc, necessary for the modern communications standards.

TABLE 5.IV
SPECTRUM CONTENT VALUES WITH USING PREDISTORSION

Freq (GHz)	ACP 1 Low (dBc)	ACP 1 High (dBc)	ACP 2 Low (dBc)	ACP 2 High (dBc)
0.8	-45.41	-45.31	-48.14	-49.46

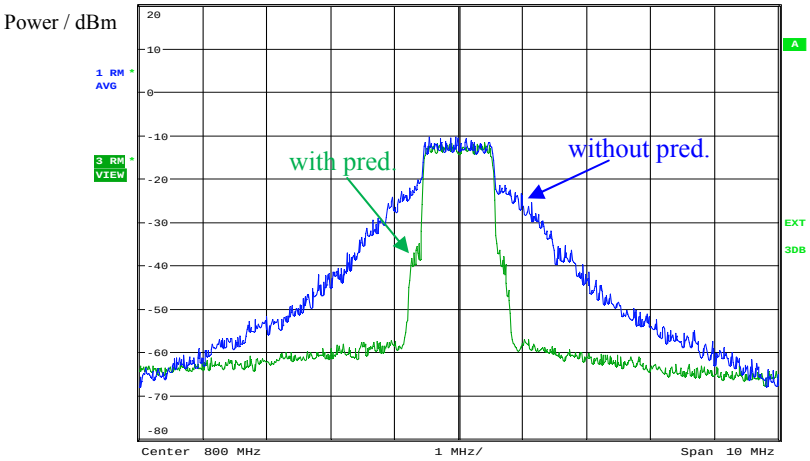


Fig. 5.25 – Measured output spectrum for the 10 MHz LTE signal at 0.8 GHz of frequency with (green) and without (blue) the use of the generic predistortion.

5.4 Continuous Class-FV Mode Extended to the Third Harmonic Termination

As mentioned earlier, the Continuous Class-FV theory leads to a variation in only first two harmonic terminations while maintaining a constant open-circuit third harmonic load. In this manner the output power and drain efficiency can be maintained theoretically at a constant level.

Also, in Chapter 3 the Continuous Inverse Class-FI mode has been described (with the measurement validation presented later in Chapter 6), where the new formulation can also be applied to the current waveform, thus identifying a new family of waveforms on the current side. Here by simultaneous variation of fundamental and second harmonic susceptance, while maintaining a constant short-circuit third harmonic load, it has again been demonstrated that is possible to maintain ideally constant power and efficiency.

However, as shown in paragraph 5.3 of this Chapter, in real PA designs the variation of the impedance solutions are translated into design space in the frequency domain. Therefore, no constraints can be applied to any termination (in this case the constant open-circuit third harmonic load) that inevitably vary somewhere inside the Smith chart. In the realisation of the Continuous Class-FV PA design, it has been noted that, although the third harmonic termination cannot

be maintained constant, when varying it around the edge of the Smith chart excellent output performance is demonstrated.

5.4.1 Theoretical Continuous Class-FV3

In this Section the Continuous Class-FV theory is extended to the third harmonic termination, now termed Continuous Class-FV3 [27].

In the Continuous Class-FV mode only the voltage waveform is allowed to vary while maintaining a constant current waveform. In the Continuous Class-FI mode that variation is applied on the current waveform while maintaining a constant voltage waveform. Therefore, the idea was that, if both waveforms are allowed to vary simultaneously, this should allow the variation of the fundamental and second harmonic impedance as well as the third harmonic termination. The simultaneous variation of both voltage and current waveforms is what happens in reality in real power transistors, as it is not possible to maintain perfectly constant any waveform when varying the different parameters (i.e. output impedances). This is because voltage and current waveforms are related through the knee region [14].

Initially, the voltage equation adopted to describe the Continuous Class-FV3 voltage waveform was taken directly from the Continuous-FV mode (eq. 5.1), while the current equation was taken directly from the Continuous Class-FI mode (eq. 3.70, but in this case assuming first 2 harmonic components), both without any further adjustment, as shown in (5.6) and (5.7).

$$v(\vartheta)=\left(1-\frac{2}{\sqrt{3}}\cos\vartheta\right)^{2}\cdot\left(1+\frac{1}{\sqrt{3}}\cos\vartheta\right)\cdot(1-\delta\sin\vartheta), \tag{5.6}$$

$$i(\vartheta)=\left(1+\frac{2}{\sqrt{2}}\cos\vartheta+\frac{1}{2}\cos 2\vartheta\right)\cdot(1-\delta\sin\vartheta). \tag{5.7}$$

Those equations lead to the waveforms shown in Fig. 5.26 as a function of δ, with the relative impedance points shown in the Smith chart of Fig. 5.27.

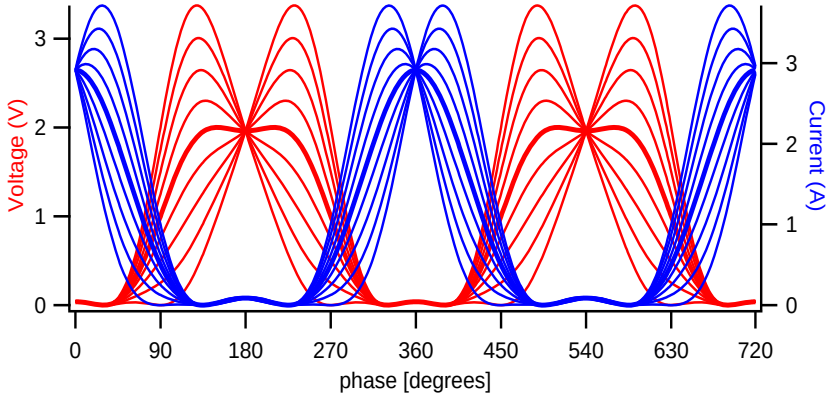


Fig. 5.26 – Theoretical Continuous Class-FV3 voltage and current waveforms for δ ranking between -1 and 1.

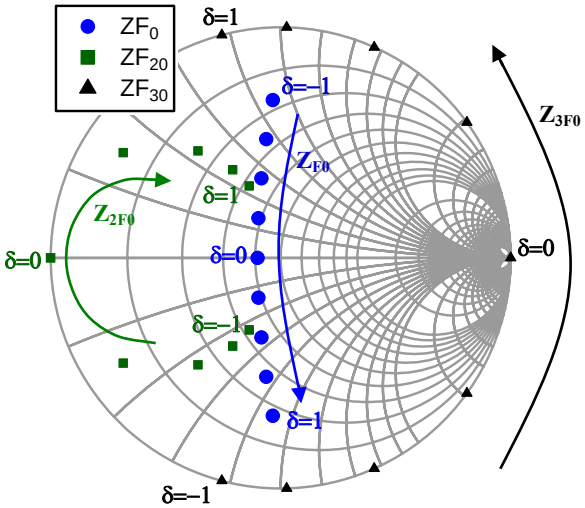


Fig. 5.27 – Theoretical Continuous Class-FV3 range of first three impedances for δ ranking between -1 and 1.

The second harmonic impedances goes inside the Smith chart with varying δ. This will obviously lead to a decrease in power and efficiency as the power is dissipated in such harmonics. Besides, the third harmonic load varies with the wrong direction; this would make the output matching network harder (if not impossible) to design.

After looking carefully into the maths, it has been discovered that in order to have constant power and efficiency through the simultaneous variation of first, second and now also third harmonic terminations, i.e. through the variation of both voltage and current waveforms, some adjustment of such equations was

necessary, as shown in (5.8) and (5.9). As it can be noted, the voltage equation remains the same while a modified correction is applied on the current equation.

Now the simple variation of the parameter δ, will lead to a variation of both voltage and current formulations, leading to a variation on both fundamental and second harmonic impedances as well allowing a reactive excursion of the third harmonic termination without any loss of power and/or efficiency.

$$v(\vartheta)=\left(1-\frac{2}{\sqrt{3}}\cos\vartheta\right)^{2}\cdot\left(1+\frac{1}{\sqrt{3}}\cos\vartheta\right)\cdot(1-\delta\sin\vartheta), \tag{5.8}$$

$$i(\vartheta)=\left(1+\frac{2}{\sqrt{2}}\cos\ \vartheta+\frac{1}{2}\cos\ 2\vartheta\right)\cdot\left(1+\frac{\delta}{5}\sin\ 5\vartheta\right). \tag{5.9}$$

The Smith Chart of Fig. 5.28 shows the desired range of fundamental, second and third harmonic impedances when dividing the appropriate voltage and current Fourier components function of the parameter δ. Now both the second and the third harmonic terminations vary on the perimeter of the Smith chart. Indeed the three impedances vary with the right direction, which has been accommodated by varying the sign on the second bracket of 5.2. The possibility to move and vary the fundamental, the second and now also the third harmonic termination with frequency allows an easier process when designing the matching network in order to present such impedances.

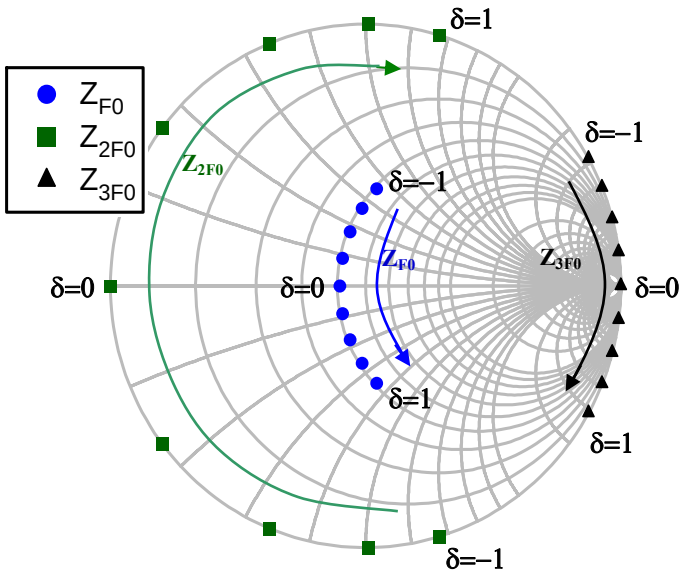


Fig. 5.28 – Theoretical Continuous Class-FV3 range of first three impedances for δ ranking between -1 and 0. Impedances between 0 and 1 will be the mirrored ones.

Expanding the two equations (5.8) and (5.9), the following voltage (V_n) and current (I_n) components are obtained:

$$V_1 = -\frac{2}{\sqrt{3}} + j\delta\,, \qquad I_1 = \frac{2}{\sqrt{2}}\,, \tag{5.10}$$

$$V_2 = -j\frac{7}{6\sqrt{3}}\delta\,, \qquad I_2 = \frac{1}{2}\,, \tag{5.11}$$

$$V_3 = \frac{1}{3\sqrt{3}}\,, \qquad I_3 = -j\frac{\delta}{20}\,, \tag{5.12}$$

$$V_4 = j\frac{1}{6\sqrt{3}}\delta\,, \qquad I_4 = -j\frac{1}{5\sqrt{2}}\delta\,, \tag{5.13}$$

$$V_5 = 0\,, \qquad I_5 = -j\frac{1}{5}\delta\,, \tag{5.14}$$

$$V_6 = 0\,, \qquad I_6 = -j\frac{1}{5\sqrt{2}}\delta\,, \tag{5.15}$$

$$V_7 = 0\,, \qquad I_7 = -j\frac{1}{20}\delta\,, \tag{5.16}$$

The components from V_1 to V_7 represent the voltage Fourier components from 1st to the 7th harmonic, as well as the components from I_1 to I_7 represent the corresponding current Fourier components. It should be noted, the voltage components from 4 to 7 are set to zero, while higher current components (up to the 7th) have been considered; this can be justified as a good approximation in most practical cases, based on the probability that higher voltage harmonics will usually be suppressed by the device parasitic capacitances.

Figures 5.29 and 5.30 show the theoretical voltage and current waveforms and the respective load-lines when applying (5.1) and (5.2) for δ ranging between -1 and 0 with step of 0.5. The range $0 \leq \delta \leq 1$ (not displayed) would give the mirrored waveforms of $-1 \leq \delta \leq 0$.

When applying this theory, and including harmonic content greater than 3 (up to 7th), optimum results can be obtained, however it will be seen in the measurement results that satisfactory output performance can still be achieved by considering only the first three harmonic components.

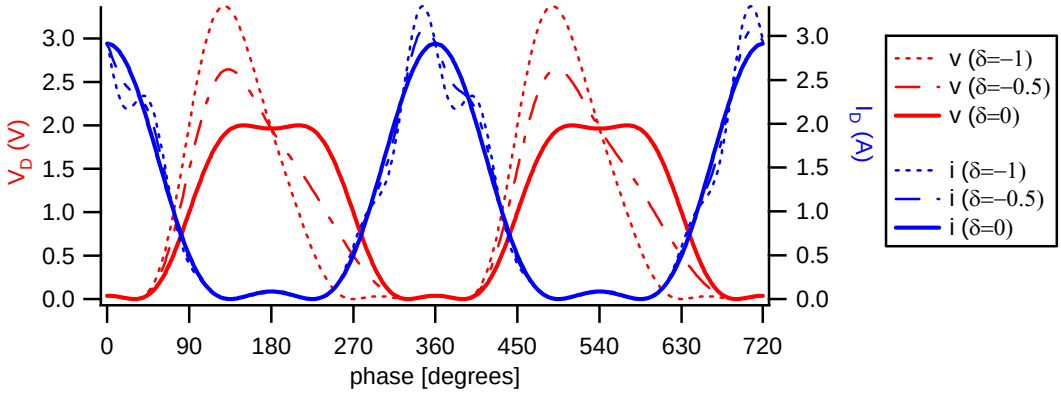


Fig. 5.29 – Theoretical Continuous Class-FV3 voltage and current waveforms for δ varying between -1 and 0 in steps of 0.5.

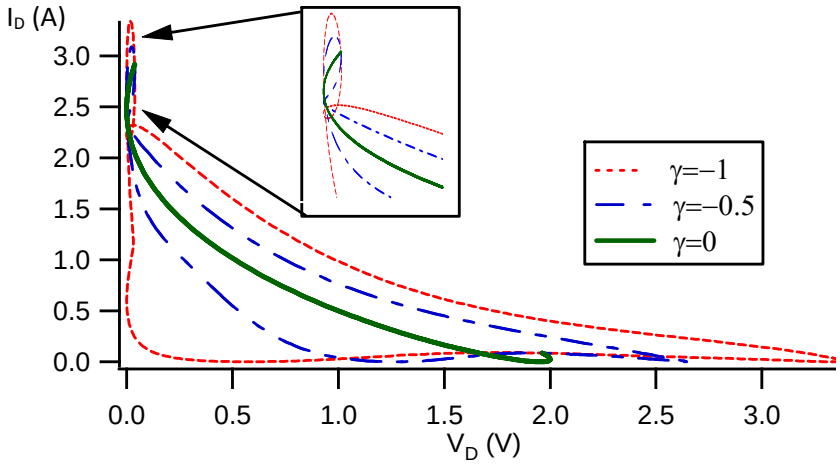


Fig. 5.30 – Theoretical Continuous Class-FV3 load-lines for δ varying between -1 and 0 in steps of 0.5

5.4.2 Continuous Class-FV3 Measurement Results

The theoretical analysis reported in Section 5.4.1 has been applied experimentally on a 6x200 µm (1.2 mm) AlGaN/GaN power transistor from Fraunhofer IAF [28], using a 28 V supply voltage at 1 GHz fundamental frequency. As for the Continuous Class-FV measurements presented in Chapter 4, these experimental results have been carried out on the active ELP measurement system developed at Cardiff University [29].

Initially the standard Class-F mode has been obtained through the process implemented in [30-31]. For this power transistor, with bias voltage of V_G=-3.1 V (pinch-off voltage V_{TH}=-2.4 V), input power of P_{IN}=14 dBm (source available

power P_{AVS}=20.4 dBm) and presenting Z_{F0}=0.49∟45.8°, Z_{2F0}=1∟-180° and Z_{3F0}=1∟68° at the extrinsic plane, an efficiency of η=80.6%, output power of P_{OUT}=35.9 dBm and available gain of G_{AV}=15.4 dB have been achieved at around 1.5-2 dB of gain compression. Once the standard Class-F mode has been obtained the first three harmonic impedances have been simultaneously varied as explained in section 5.4.1. Theory and measurements have been performed at the device intrinsic plane after de-embedding the drain-source capacitor C_{DS}=0.45 pF.

Fig. 5.31 shows the measured output performance in terms of power, efficiency and gain as a function of δ, for a constant source available power P_{AVS}=20.4dBm.

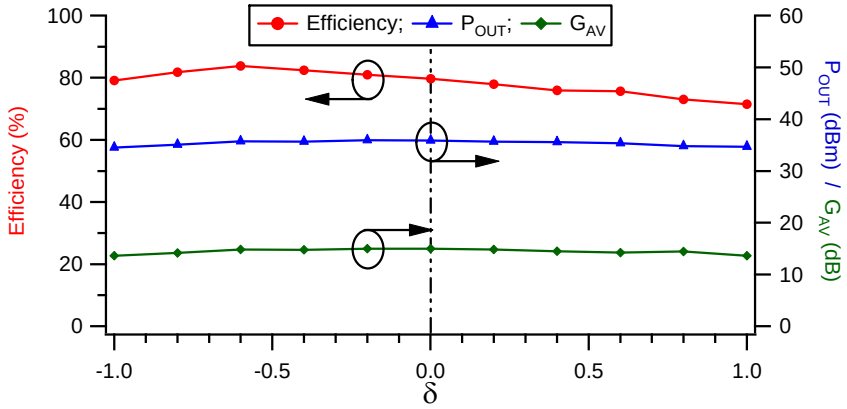


Fig. 5.31 – Measured Continuous Class-F3 drain efficiency, output power and available gain for -1 ≤ δ ≤ 1 in steps of 0.2.

As can be seen, the output power and available gain are maintained at an almost constant level with varying δ, at around 35.5-35.8 dBm and 15 dB respectively. Interestingly, moving toward δ<0 the efficiency increases, reaching a maximum value of 83.7% for δ=-0.6 whilst for δ>0 it decreases when approaching towards the edge of δ. This may be caused either by the non-unilateral device characteristic or some non-linearity in the device transconductance as well as the influence of the higher harmonics.

Fig. 5.32 shows the measured Continuous Class-FV3 voltage and current waveforms for constant P_{AVS}=20.4 dBm. Both voltage and current waveforms vary as a function of δ (between -1 and 0 in steps of 0.5), which means that all of the first three harmonic impedances are being varied, revealing the new design space.

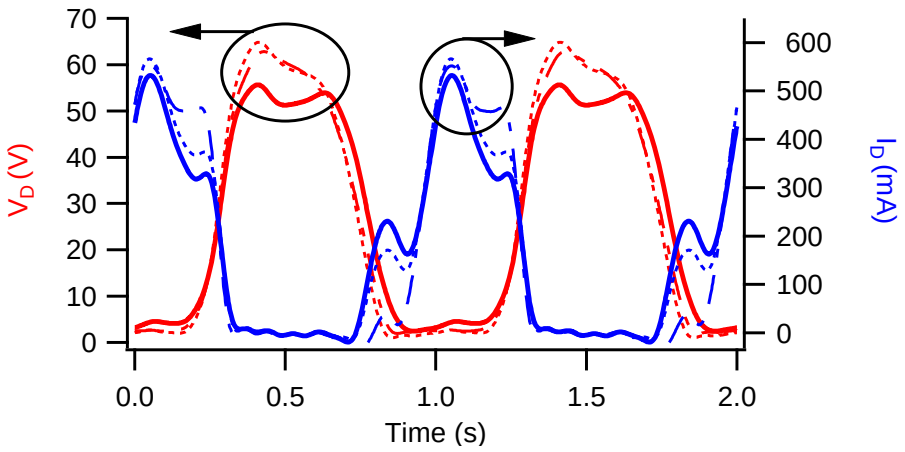


Fig. 5.32 – Measured Continuous Class-F3 voltage (red lines) and current (blue lines) waveforms for $-1 \leq \delta \leq 0$ in steps of 0.5.

Fig. 5.33 shows efficiency and output power as a function of the input bias voltage V_G and the parameter δ. It can be seen that decreasing V_G from its original value of -3.1 V, the efficiency increases up to 85% for V_G=-3.6 V and δ=-0.5 while still maintaining satisfactory output power of 35.7 dBm (3.7 W) at almost the same compression level, G_{AV}=14.7 dB. Fig. 5.34 shows the drain efficiency and gain behaviour function of the output power sweep for gate bias V_G=-3.1 V and for different values of δ from -1 to 1 in steps of 0.5. Here it can be noted as well that the highest efficiency of 83.7% is obtained for δ=-0.5 (green line), while higher linear gain of around 18.7 dB is achieved for δ=-1 (blue line). However, in this case of δ=-1 the device compresses revealing lower efficiency and output power.

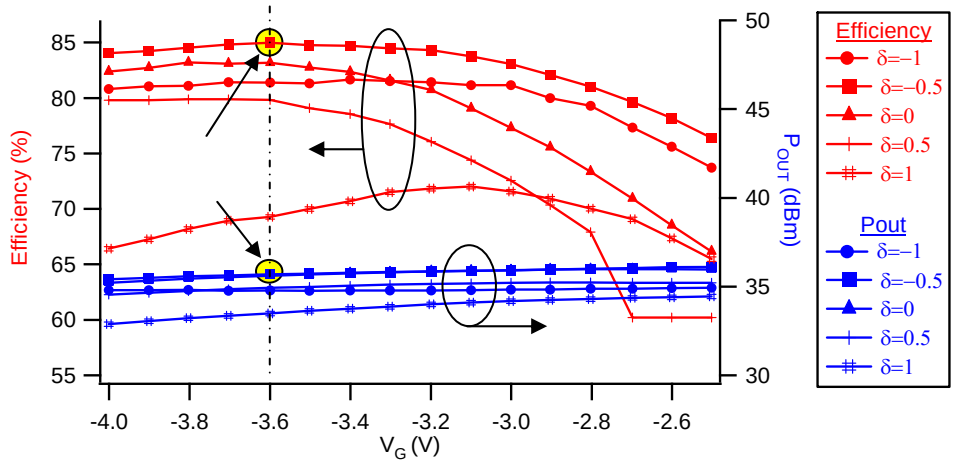


Fig. 5.33 – Measured drain efficiency and output power function of gate bias V_G and δ, where $-4 < V_G < -2.7$V in steps of 0.1 and $-1 \leq \delta \leq 1$ in steps of 0.5.

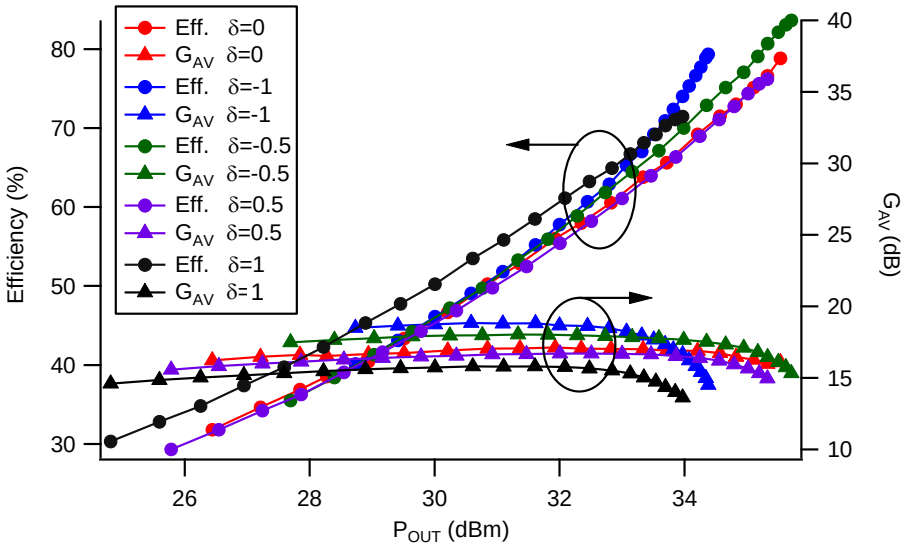


Fig. 5.34 – Measured drain efficiency and gain Vs output power sweep for different values of δ, where $-1 \leq \delta \leq 1$ in steps of 0.5.

5.5 Chapter Summary

This Chapter has demonstrated the full realisation of a 10 W highly efficient and broadband Continuous Class-FV PA. Starting from the standard Class-F design procedure, the various steps for the realisation of the broadband PA have been demonstrated. Here, knowing the right fundamental and harmonic impedances utilising the Continuous mode theory, the appropriate output matching network has been designed in order to present the target impedances for which the high power-efficiency state is revealed. The realised Continuous Class-FV PA has shown satisfactory results comparable with the simulated performance. Here, the measured drain efficiency between 65% and 80% for an octave bandwidth of 0.55-1.1 GHz with the expected output power of around 10.5 W and gain of 11 dB has been achieved. Linearity performance has been presented as well, showing the possibility of linearity improvement when applying a generic predistortion technique. In addition, as previously known, it would be difficult, if not impossible, to maintain constant (in this case open-circuit) the third harmonic load (or other impedances) when designing the output matching network. Therefore, a new formulation for the current waveform has been presented revealing different range for the third harmonic reactive termination as well. This would allow for an easier and more flexible design when varying the first three harmonic impedances for the realisation of highly power efficient and broadband PAs.

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Chapter 6

Conventional and Continuous Inverse Class-F Measurements

6.1 Introduction

This Chapter will provide the experimental design procedure for an optimum Inverse Class-F power amplifier design, and starting from here, the Continuous Inverse Class-F modes will be experimentally explored through measurement activity.

Once the standard Inverse Class-F mode is obtained through the appropriate design approach, the next step forward moved towards the design of a broadband power amplifier is the Continuous Inverse Class-F state. These modes consist of two different broadband modes termed Continuous Inverse Class-FV and Continuous Inverse Class-FI, as already theoretically presented in Chapter 3. The Continuous Inverse Class-FV design space consists of new output impedance solutions achieved through the variation of the voltage waveform while maintaining a constant current waveform. Vice-versa, in the Continuous Inverse Class-FI, the new output terminations are achieved by varying the current waveform while maintaining a constant voltage waveform.

Here, it will be demonstrated through measurement results that in both cases, the new admittance solutions will reveal constant output performance in terms of power and efficiency. Indeed, an extended current formulation will be presented revealing a yet wider design space for which the output performance does not significantly degrade.

A first attempt for the realisation of the Continuous Inverse Class-FI PA has been made as shown in Section 6.6. It will be seen that although the results do not satisfy the initial target, high power-efficiency can be still achieved for a very wide band of frequencies.

6.2 Standard Inverse Class-F

6.2.1 Practical limitations

As described in the Class-F and Continuous Class-FV/FI measurement sections of Chapter 4, when measuring real power transistors in a real measurement system environment, practical limitations must be taken into account. Therefore, as for the Class-F case, the Inverse Class-F perfect theoretical voltage and current waveforms cannot be achieved.

The different Class-F and Inverse Class-F classes of operation have different properties that can be exploited when considered in conjunction with different device technologies. This concept is especially valid when dealing with broadband PA modes. For example, for the realisation of a Class-F power amplifier the first three harmonics must be taken into account. This means that if the f_T of the device is 90 GHz the maximum fundamental design frequency (F_0) cannot go above 30 GHz as the third harmonic will be $3*F_0=3*30=90$ GHz. Besides, as shown in [1] the device efficiency is function of the impedances ratio. Fig. 6.1 shows the measured efficiency as a function of the ratio Z_{2F0}/Z_{F0} for a GaAs pHEMT device [1]. Here, for fixed optimum fundamental and third harmonic impedances the second harmonic load was varied, and as can be noted, the efficiency decreases as the ratio increases. This means that for high optimum impedances (small device sizes) better performance can be achieved in Class-F configuration whilst when dealing with big device sizes (small fundamental impedance) a better output

performance could be revealed for example in the Inverse Class-F configuration. More details of this concept can be found in [2].

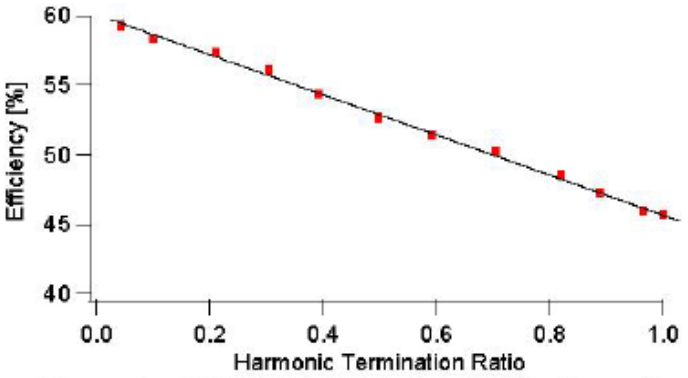

Fig. 6.1 – Measured efficiency vs. harmonic terminations ratio [1].

6.2.2 Standard Inverse Class-F Measurements

For the standard Inverse Class-F mode a square current waveform and a half-wave rectified sinusoidal voltage waveform must be presented at the device intrinsic current generator plane [3-10]. As mentioned earlier in this thesis, infinite harmonic content cannot be considered in real measurements, thus more realistic finite harmonic content waveforms are required. In this case harmonic terminations since up to three can be controlled therefore a three harmonic square current waveform and a second harmonic peaking voltage waveform would be considered.

The approach followed for the initial standard Inverse Class-F design procedure can be found in detail in [11]. Here, by using the same 6x50 μm GaAs device from TriQuint (used for the Continuous Class-FV measurements shown in Chapter 4), the initial gate bias voltage and input power sweeps have been performed in order to find the right bias point for the appropriate input power. Considering the same concept of the Class-F approach where the half-wave rectified sinusoidal current waveform was revealed by presenting a null third harmonic current component, in this Inverse Class-F case the bias voltage has been chosen in order to minimise the second harmonic content component. This bias voltage is typically the Class-A bias point for which $I_{DC}=I_{MAX}/2$. Since the transistor is an input voltage controlled current source, this means that the drain current waveform is achieved by proper engineering of the input voltage [12]. Therefore, when biasing the device in Class-

A, the initial Class-A sinusoidal current waveform should ideally be revealed and maintained even when varying the output fundamental and harmonic impedances. However, in real devices, the drain voltage and current waveforms are related to each other through the knee region, as well as through the feedback gate-drain capacitor C_{GD}. This means that the voltage and current waveforms interact with each other when varying the fundamental and harmonic impedances.

Fig. 6.2 shows the contour plot of second harmonic content as a function of the available source power (P_{av}) and the gate bias voltage (V_g). In this case the second harmonic content is minimised at around 0.5-1 mA for V_g values of around -0.3 ÷ -0.4 V. Thus, for an optimum design at the higher-end of the available input power level of 4 dBm a value of V_g=-0.4 has been chosen.

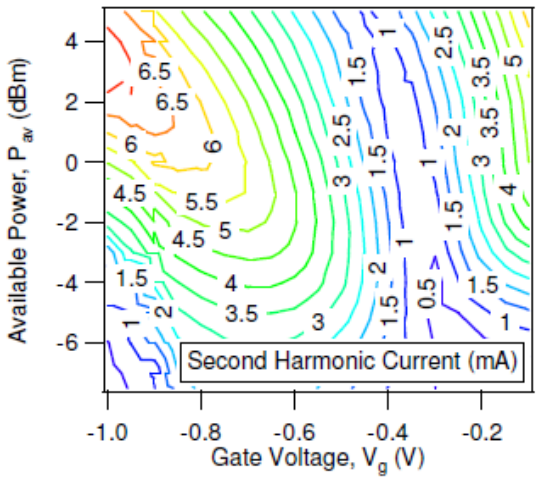

Fig. 6.2 – Measured second harmonic content as a function of input power and gate bias voltage [11].

It is important to highlight that the different approaches have demonstrated that the standard Inverse Class-F mode can be achieved by biasing the device either in Class-A and Class-B mode [3, 4, 12]. In the Class-A mode the initial sinusoidal current waveform is significantly clipped. When biasing the device in Class-B, the current waveform would initially be half-wave rectified sinusoidal, this means that the bottom part of the waveform is already squared, then by introducing third harmonic current component the top part of the waveform can also be clipped. The downside is that in this case 6 dB more drive power is in theory necessary, which means a possible decrease of 6 dB in the overall gain.

Once the right bias voltage has been chosen (in this case a Class-A bias), the appropriate output terminations must be presented in order to obtain the Inverse Class-F state, thus the appropriate Inverse Class-F voltage and current waveforms as shown in Fig. 6.3.

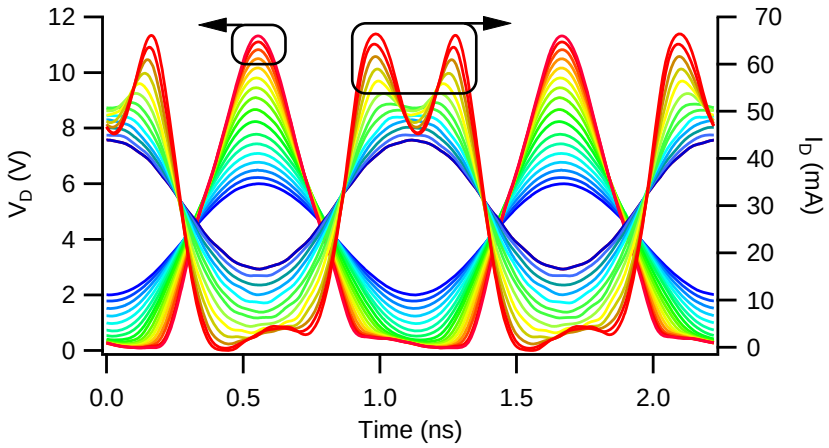

Fig. 6.3 – Measured voltage and current waveforms function of the input power sweep.

The measurements are performed at the intrinsic current generator plane, hence an open-circuited second harmonic termination and a short-circuited third harmonic load have been provided while the fundamental impedance has been varied. The optimum trade-off between efficiency, output power and gain has been found for a fundamental impedance of Z_{F0}=165+j0 Ω. Fig. 6.4 shows the measured output performance in terms of drain efficiency, available gain and output power. Drain efficiency η=80.4%, gain of G=18 dB and output power of P_{OUT}=19.4 dBm were achieved at approximately 2-3 dB of gain compression.

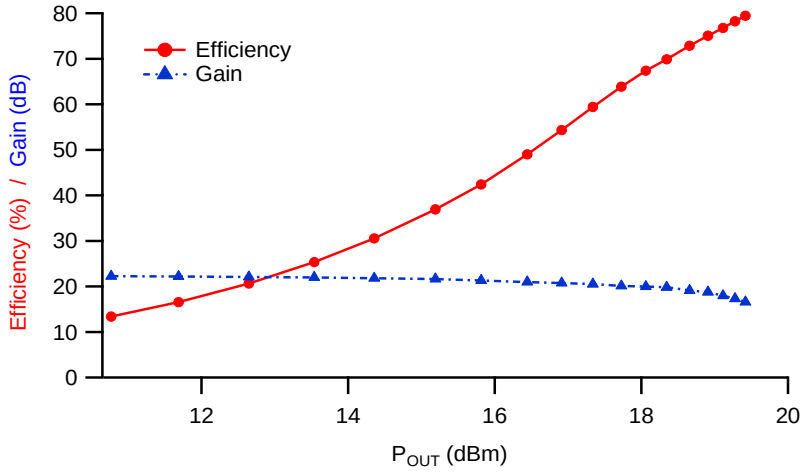

Fig. 6.4 – Measured efficiency and gain function of the output power sweep.

6.3 Continuous Inverse Class-FV Measurements

The previous section has discussed the Inverse Class-F mode optimum design procedure presenting the experimental measurements required to optimise the power transistor efficiency, output power and gain. In this standard case the design was performed for the standard combination of the first three harmonic impedances. Once the standard singular solution Inverse Class-F mode is obtained, the Continuous Inverse Class-FV theory shown in Chapter 3 can be applied in order to realize the new broadband mode [13-14]. Therefore, with the same DC drain voltage V_{DC}=4 V, working frequency F_0=0.9 GHz, input bias voltage V_G=-0.4 V and starting from the optimum fundamental impedance Z_{F0} =165+j0 Ω, open circuit second harmonic impedance Z_{2F0} and short-circuit third harmonic termination Z_{3F0} at around 4 dB of gain compression, such impedances have been swept in accordance with the Continuous Inverse Class-FV theory, with the voltage and current equations shown in (6.1) and (6.2):

$$v_{Cont\_FV^{-1}}(\vartheta)=\left(1-\sqrt{2}\cos\vartheta+\frac{1}{2}\cos 2\vartheta\right)\cdot\left[1-\delta\sin\vartheta\right] \tag{6.1}$$

$$i_{Cont\_FV^{-1}}(\vartheta)=i_{DC}+i_1\cos\vartheta+i_2\cos 2\vartheta-i_3\cos 3\vartheta \tag{6.2}$$

where in this case a finite number of harmonics in both voltage and current waveforms have been considered.

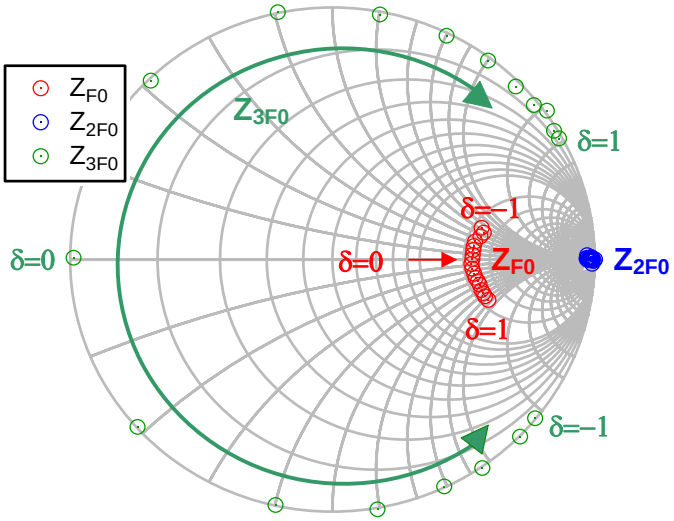

Fig. 6.5 – Measured Continuous Inverse Class-FV first three harmonic impedances for $-1 \le \delta \le 1$ in steps of 0.1.

Varying the empiric parameter δ, the simultaneous variation of fundamental and third harmonic impedances have been identified and reported in Fig. 6.5.

When varying δ, the fundamental impedance varies on its circle of constant resistance (where R_{F0}=165Ω) while the third harmonic termination varies around the perimeter of the Smith chart from the short-circuit condition. The second harmonic load is a fixed open-circuit. In this case, as opposed to the Continuous Class-FV case of Chapter 4, there are no oscillation issues observed with varying the different loads, thus the third harmonic termination could be placed in the right position around the Smith chart for the entire δ range (between -1 and 1) in accordance with the mathematical formulation [13].

Fig. 6.6 shows drain efficiency and output power function of fundamental and third harmonic reactances X_1 and X_3 both normalised to the fundamental resistance R_1. Here the inverse relationship between X_1 and X_3 can be noted (green line).

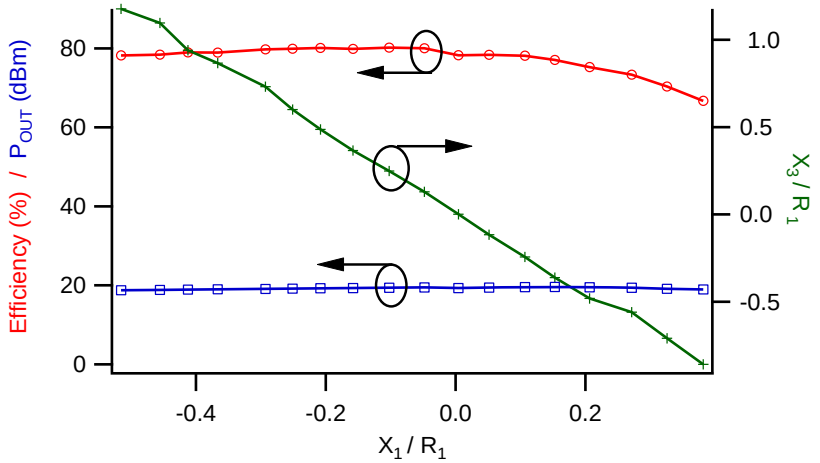

Fig. 6.6 – Measured Continuous Inverse Class-FV drain efficiency and output power for coupled variations of fundamental and third harmonic reactance for $-1 \leq \delta \leq 1$ in steps of 0.1 and keeping short-circuited the third harmonic load.

Fig. 6.7 shows the output performance in terms of drain efficiency, output power, available gain and available input power (P_{AVS}) with varying δ. Output power is maintained at an almost constant level around 19.5 dBm (from 19.2 to 19.6 dBm) for all the range of δ. The drain efficiency is maintained greater than 75% for $-0.5 \leq \delta \leq 1$ with a maximum peak value of 80.1% for $\delta = 0.4$, but starts degrading for $\delta < -0.5$. The maximum value of gain G_{AV}=15 dB (@ P4 dB) is achieved when $\delta = 0$, which then decreases with δ, down to around 10dB. This is

due to the fact that with varying δ, the input power (P_{AVS}) needs to be adjusted in order to maintain the square current waveform (as shown in Fig. 6.7).

It is important to highlight that the gain shows an increase in the region of δ between around -0.4 and 0. This can easily been explained by observing the device input behaviour as shown in Fig. 6.8. In such δ range the input reflection coefficient is greater than 1 causing the stability problem and therefore the increase in gain. Therefore, this behaviour must be taken into account and properly addressed when designing the PA input matching network.

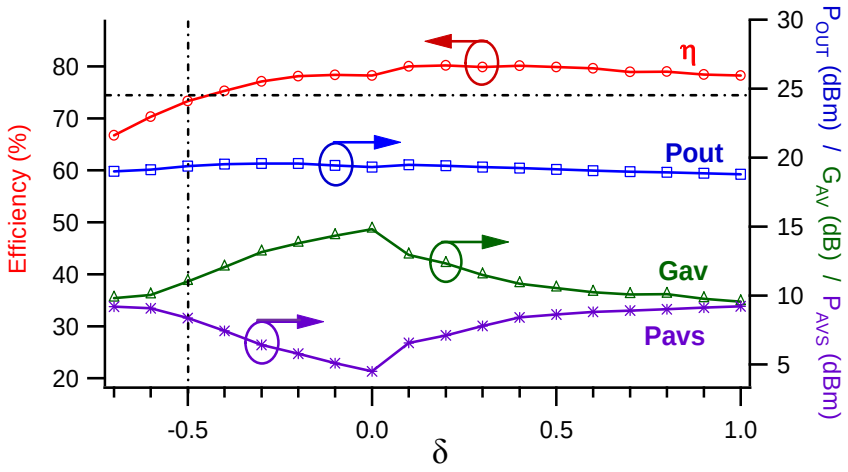

Fig. 6.7 – Measured Continuous Inverse Class-FV drain efficiency, output power, available gain and available input power for $-0.7 \leq \delta \leq 1$ in steps of 0.1.

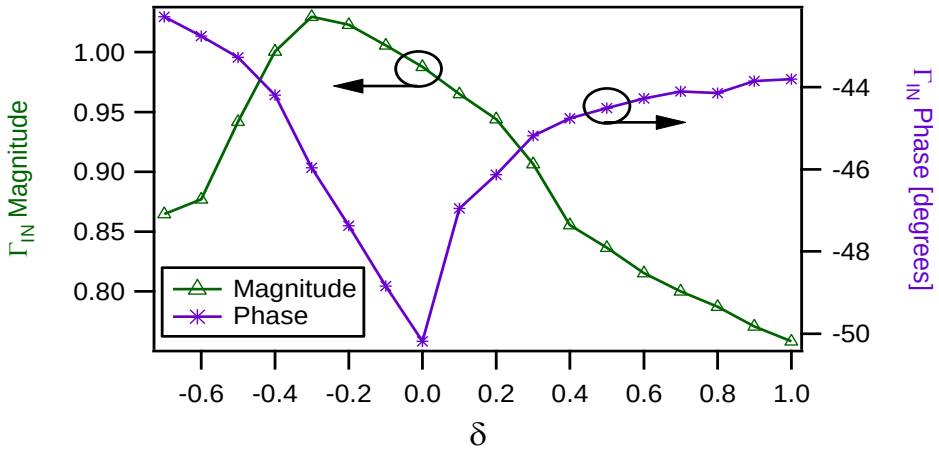

Fig. 6.8 – Measured Continuous Inverse Class-FV input reflection coefficient magnitude and phase for $-0.7 \leq \delta \leq 1$ in steps of 0.1.

The drain efficiency and output power should remain constant along the δ variation [13], but as it can be noted from the measured results [14] the output performance tend to degrade towards the edges of δ. In this particular case the drain efficiency degrades when varying δ with negative sign and especially below -0.5. This can be due to the interaction with the knee region [12], the non-unilateral characteristic of the device, the feedback capacitor [15] as well as the non-ideal de-embedding. In this on-wafer device, only the drain-source capacitor C_{DS} needed to be de-embedded, but when working with packaged devices it is very important to use a de-embedding network that is as accurate as possible in order to follow the right line of constant resistance when varying δ.

The plots in Fig. 6.9 and 6.10 show the measured Continuous Inverse Class-FV voltage and current waveforms for δ varying between -0.7 and 1 in steps of 0.1. As it can be noted, the measured current waveforms (Fig. 6.10) are maintained at an almost constant level of around 70 mA (peak value) with varying δ. This can be achieved by varying the input power as already shown in Fig. 6.7. The variation of the input power in order to keep constant such waveforms can be exploited during the input matching network design. However, the variation of δ leads to the variation of the voltage waveforms as shown in Fig. 6.9, thus revealing the new family of Continuous Inverse Class-FV waveforms. The harmonic limited half-wave rectified (second harmonic peaking) sinusoidal voltage waveform is obtained for δ=0 (blue waveform) with maximum peak at around 12 V, consistent with the computed standard Inverse Class-F state $V_{PEAK}=\pi*V_{DC}$ value where V_{DC}=4 V. When varying the parameter δ the new family of waveforms with higher peak-to-average ratio (PAR) are achieved, revealing the new design space.

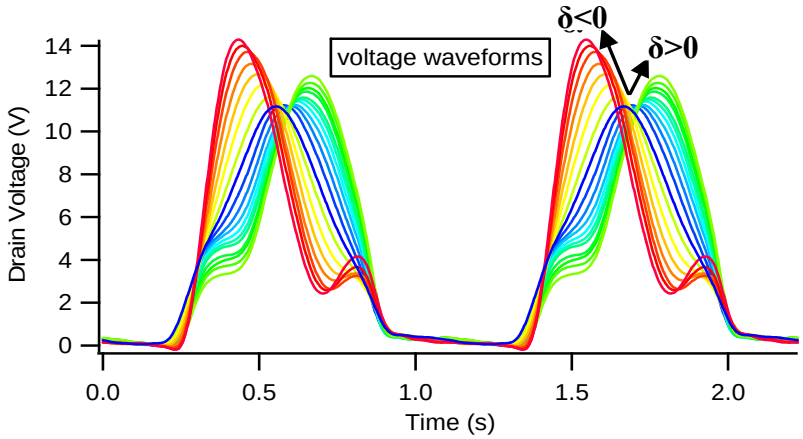

Fig. 6.9 – Measured Continuous Inverse Class-FV voltage waveforms for between -0.7 and 1 in steps of 0.1.

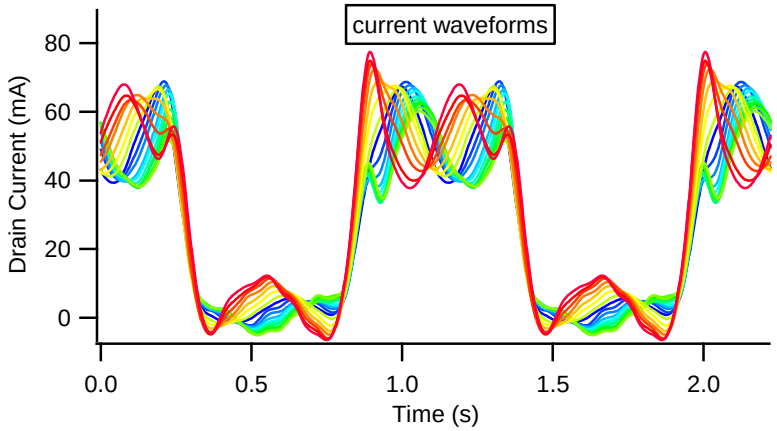

Fig. 6.10 – Measured Continuous Inverse Class-FV current waveforms for between -0.7 and 1 in steps of 0.1.

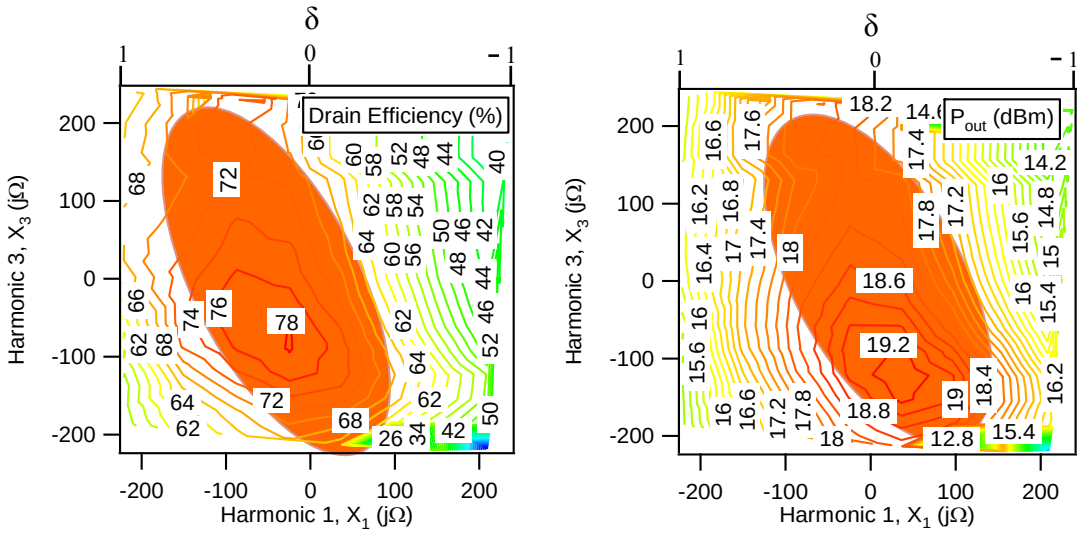

Fig. 6.11 – Measured Continuous Inverse Class-FV drain efficiency (left) and output power (right) as a function of X_1 and X_3 for constant input power.

To provide more insight, contours have been plotted over the entire design space function of fundamental and third harmonic impedances, shown in Fig. 6.11.

For these measurements the second harmonic load is kept open-circuited and the input drive power is kept constant. These Figures do not show the actual optimum device behaviour as shown in Figures 6.6 and 6.7 because as already mentioned, here the input power was maintained at a constant value. Nevertheless, it can still be seen that the best behaviour is obtained when fundamental reactance X_1 is positive and third harmonic reactance X_3 is negative and vice-versa (approx.) in accordance with the theory and highlighted in orange.

6.4 Continuous Inverse Class-FI Measurements

Section 6.3 has shown the Inverse Class-FV measurements where fundamental and third harmonic impedances were varied leading to a new family of Inverse Class-F voltage waveforms while maintaining a constant current waveform. In this section it will be demonstrated that the drain efficiency and output power can be maintained reasonably constant for different current waveforms while maintaining the voltage waveform constant [16]. The Continuous Inverse Class-FI equations (shown in (6.3) and (6.4)) and already presented in Chapter 3 of this thesis, are similar to the previous Continuous Inverse Class-FV ones with the exception that now the operator [1-δsinθ] is applied to the current equation:

$$v_{Cont\_FI^{-1}}(\vartheta) = \left(1 - \sqrt{2}\cos\vartheta + \frac{1}{2}\cos 2\vartheta\right) \quad , \tag{6.3}$$

$$i_{Cont\_FI^{-1}}(\vartheta) = \left(i_{DC} + i_1\cos\vartheta + i_2\cos 2\vartheta - i_3\cos 3\vartheta\right)\cdot\left[1 - \delta\sin\vartheta\right], \tag{6.4}$$

where in this case: i_{DC}=0.37, i_1=0.43, i_2=0 and i_3=0.43.

The variation of the voltage and the current waveforms depends on the variation of the fundamental and harmonic impedances. This means that depending on the device properties and behaviour as well as the design target the different PA modes can be adopted.

As in the previous cases, measurements have been performed on the same wafer-probeable transistor from TriQuint at 0.9 GHz operating frequency and 4 V of DC drain voltage.

Therefore, starting from the optimum standard Inverse Class-F implemented in section 6.2, the parameter δ was varied leading to the new fundamental and second harmonic termination ranges and constant short-circuited third harmonic load shown in the Smith chart of Fig. 6.12. Note that the positive variation of δ leads to a positive variation of the second harmonic termination and a negative variation of the fundamental load.

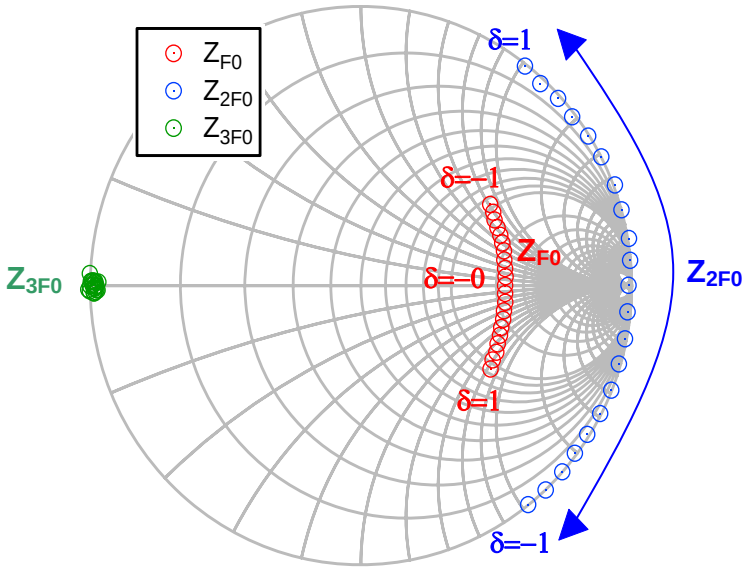

Fig. 6.12 – Measured Continuous Inverse Class-FI first three harmonic admittances for $-1 \leq \delta \leq 1$ in steps of 0.1.

This concept can also be presented in terms of admittances Y=G+jB. In this case, when varying the parameter δ, the conductance G remains constant while the variation will be applied on the susceptance B. Therefore, the fundamental load varies on its circle of constant conductance (G1) (variation on B1) while the second harmonic susceptance B2 (Z2F0) varies inversely proportional to B1 on the perimeter of the Smith chart from the open-circuit point.

The relative voltage and current waveforms are provided in Fig. 6.13. For the standard Inverse Class-F mode (waveform highlighted in red) as already demonstrated in the sections 6.1 and 6.2 the maximum drain current peak reaches around 70 mA. When varying δ the voltage waveforms are maintained almost

constant while a big variation on the current waveforms is observed. This leads to the output performance shown in Fig. 6.14. Here, the measured drain efficiency and output power are constant to around 79-80% and 19.5-20 dBm respectively for the range of δ between -1 and 1, thus satisfying the theory.

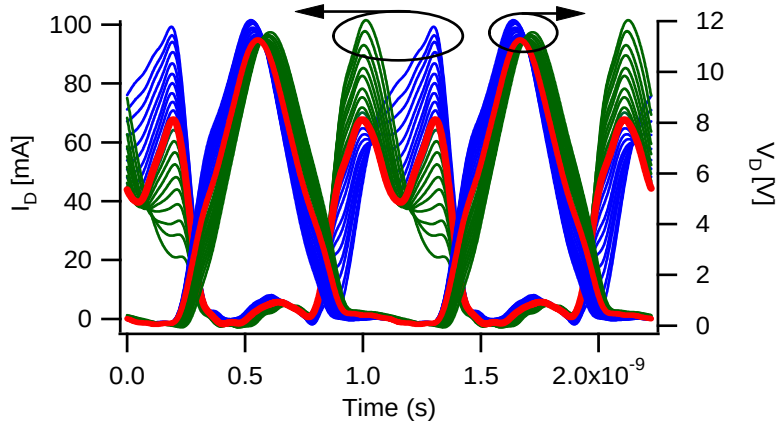

Fig. 6.13 – Measured Continuous Inverse Class-FI voltage and current waveforms for $-1 \leq \delta \leq 1$ in steps of 0.1.

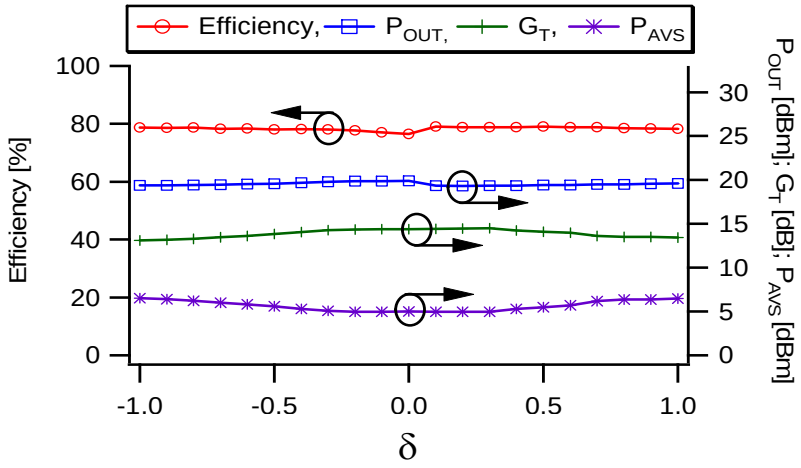

Fig. 6.14 – Measured Continuous Inverse Class-FI drain efficiency, output power transducer power gain and available input power for $-1 \leq \delta \leq 1$ in steps of 0.1.

Fig. 6.15 shows the measured drain efficiency surface plot as a function of different combinations of fundamental and second harmonic susceptances. A maximum constant efficiency of about 79-80% is achieved for the entire range of δ between -1 to 1, for which the inverse relationship of B1 and B2 is valid in accordance with (6.4). When presenting different load combinations, for example B1 and B2 either positive or negative, the device performance clearly degrades.

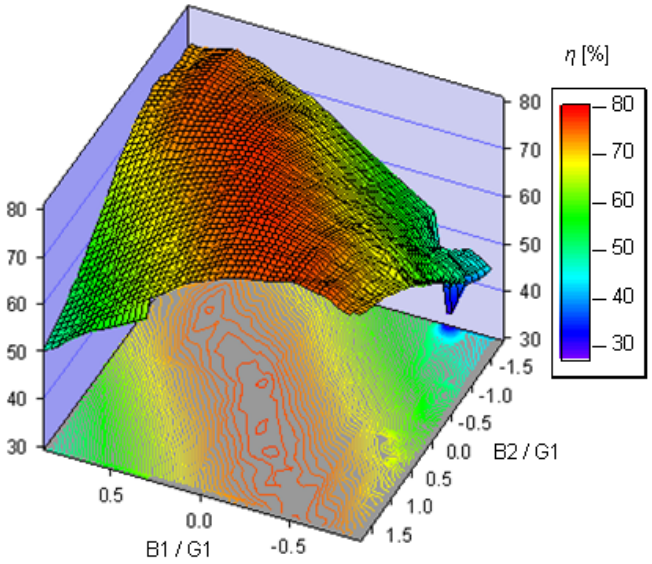

Fig. 6.15 – Measured Continuous Inverse Class-FI drain efficiency as a function of B1 and B2 both normalised to G1 for constant drive signal

Another interesting behaviour to observe is the load-line shown in Fig. 6.16. Here, for the DUT, when δ=0 the optimum trade-off between power and efficiency is found for a drain DC quiescent current around 35mA. This corresponds to an RF current swing that does not extend up to I_{max}, as shown in the highlighted red current waveform of Fig. 6.13, because of the increasing V_{min} in the knee region. Now, for this device, when dealing with the new Continuous Inverse Class-FI mode, (i.e. for δ=±1, dotted load-lines in Fig. 6.16), it is possible to utilize the full current drive capability without compromising efficiency.

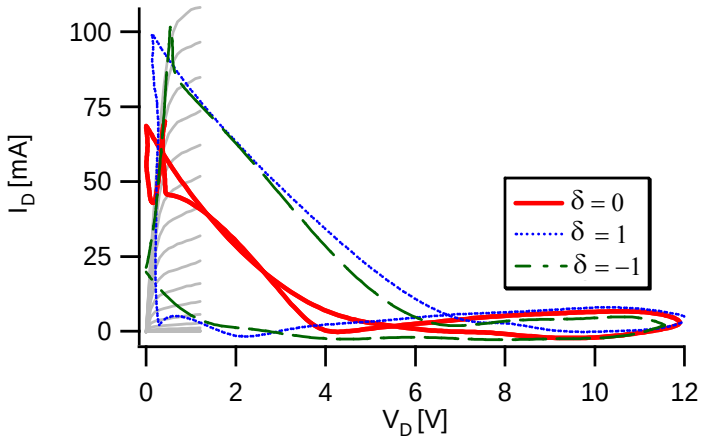

Fig. 6.16 – Measured DCIV and RF load-line for $\delta = 0$ (red highlighted solid line), for $\delta = 1$ (blue dotted line) and for $\delta = -1$ (green dotted line).

6.5 Extended Continuous Inverse Class-FI Theory and Measurement Results

In the previous Section the experimental results of the Continuous Inverse Class-F mode, for which a new family of current waveforms are revealed, has been presented. In that case it has been seen that when varying the second harmonic impedance around the edge of the Smith chart from the open-circuit condition, and by adjusting the susceptance of the fundamental load from zero, constant optimum output performance can be maintained.

Section 6.5.1 will describe a novel theory for which the second harmonic termination is allowed to vary inside the Smith chart ($\Gamma<1$) [17] and then, based upon such theory, experimental results will be presented in Section 6.5.2.

6.5.1 Extended Continuous Inverse Class-FI Theory with Resistive Second Harmonic Termination

When dealing with real PAs, it is not possible to realize ideal matching networks with reflection coefficients equal to unity. This means for instance that the harmonic impedances (in this case the second harmonic load) cannot be maintained as a perfect open-circuit. For this reason, a new mathematical formulation for the current waveform that allows the impact of a second harmonic load with $\Gamma< 1$ to be considered, in the presence of an optimum fundamental load, is now derived.

Equation (6.5) is the formulation for the constant second harmonic peaking half-wave rectified sinusoidal voltage waveform $v(\varphi)$, whilst (6.6) represents the general current formulation $i(\varphi)$ for "Continuous Inverse Class-F mode with resistive second harmonic load" which will be termed "Extended Continuous Class-F^{-1}" and which will be a function of both parameters δ and α.

$$v(\vartheta)=\left(\frac{1}{\sqrt{2}}+\cos\vartheta\right)^2 \tag{6.5}$$

$$i(\vartheta)=\left(i_{DC}-i_1\cos\vartheta+i_3\cos 3\vartheta\right)\cdot\left(1+\alpha\cos\vartheta\right)\cdot\left(1-\delta\sin\vartheta\right). \tag{6.6}$$

Extending equation (6.6) gives:

$$i(\vartheta)=\left(i_{DC}-\frac{\alpha}{2}i_1\right)+(\alpha i_{DC}-i_1)\cos\vartheta+\delta\left(\frac{\alpha}{4}i_3+\frac{\alpha}{4}i_1-i_{DC}\right)\sin\vartheta+$$
$$+\frac{\alpha}{2}(i_3-i_1)\cos 2\vartheta+\frac{\delta}{2}(i_3+i_1-\alpha i_{DC})\sin 2\vartheta+i_3\cos 3\vartheta+$$
$$+\delta\frac{\alpha}{4}i_1\sin 3\vartheta-\frac{\delta}{2}i_3\sin 4\vartheta-\delta\frac{\alpha}{4}i_3\sin 5\vartheta, \qquad (6.7)$$

where:

$$I_{DC}=i_{DC}-\frac{\alpha}{2}i_1, \qquad (6.8)$$

$$\mathrm{Re}al(I_1)=\alpha\cdot i_{DC}-i_1, \qquad (6.9)$$

$$\mathrm{Re}al(I_2)=\frac{\alpha}{2}(i_3-i_1), \qquad (6.10)$$

$$\mathrm{Re}al(I_3)=i_3, \qquad (6.11)$$

$$\mathrm{Im}ag(I_1)=\delta\left(\frac{\alpha}{4}i_3+\frac{\alpha}{4}i_1-i_{DC}\right), \qquad (6.12)$$

$$\mathrm{Im}ag(I_2)=\frac{\delta}{2}(i_3+i_1-\alpha\cdot i_{DC}), \qquad (6.13)$$

$$\mathrm{Im}ag(I_3)=\delta\frac{\alpha}{4}i_1 \qquad (6.14)$$

$$\mathrm{Im}ag(I_4)=-\frac{\delta}{2}i_3, \qquad (6.15)$$

$$\mathrm{Im}ag(I_5)=-\delta\frac{\alpha}{4}i_3. \qquad (6.16)$$

I_{DC} represents the quiescent current. *Real(I_1,I_2,I_3)* (equations from 6.9 to 6.11) represent the real part of the current components of the fundamental, second and third harmonic impedances, and *Imag(I_1,I_2,I_3,I_4,I_5)* (equations from 6.12 to 6.16) represent the imaginary part of the current components of the fundamental, second, third, fourth and fifth harmonic impedances. The real parts greater than three and the imaginary parts greater than five are equal to zero.

The Continuous Inverse Class-FI mode presented in Section 6.4, for which the second harmonic impedance varies around the perimeter of the Smith chart from

the open-circuit condition, is computed when α=0 in (6.6). Here the highest efficiency of 81.85% can be obtained when considering three harmonics for both current and voltage.

When varying δ and including the parameter $\alpha \neq 0$ a new enlarged design space where fundamental and second harmonic loads can now both be located inside the Smith Chart is presented, as shown in Fig. 6.17.

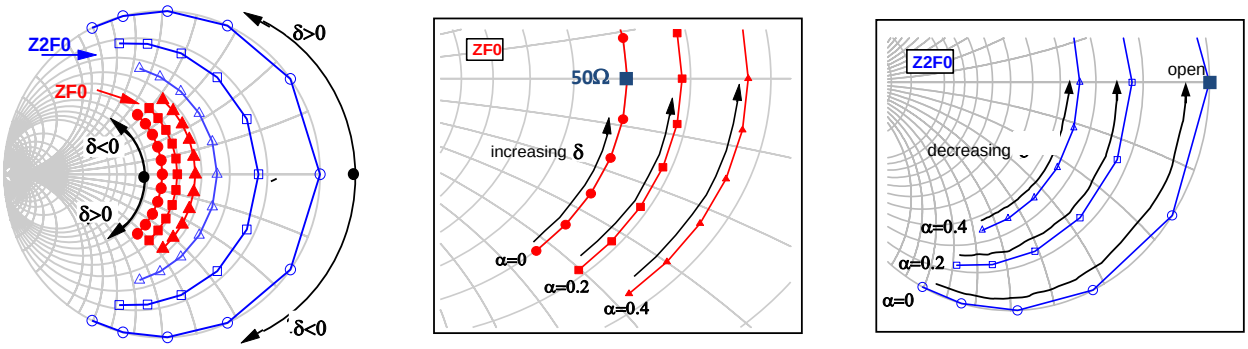

Fig. 6.17 – Theoretical Extended Continuous Inverse Class-FI for the first two harmonic impedances (third harmonic load is kept short-circuited) when varying $-1 \leq \delta \leq 1$ both in steps of 0.2.

When varying the second harmonic load inside the Smith chart (α>0) the output performance starts to slowly degrade, but by properly adjusting the fundamental load in accordance with the theory, useful performance in terms of power and efficiency can still be achieved.

Fig. 6.18 shows the theoretical computed new family of current waveforms as a function of both parameters α and δ. The current waveform amplitudes decrease with increasing α. This is due to the fact that by increasing α, the fundamental impedance also increases, therefore maintaining a constant half-wave rectified sinusoidal voltage waveform, the current waveforms then must decrease in magnitude. Besides, it can be noted that if considering the standard class-F^{-1} (α=0, red waveforms), when increasing α, bigger troughs in the waveforms are developed. As already mentioned earlier, the parameter δ and now also α must be varied between -1 and 1 to maintain non-zero crossing current waveforms.

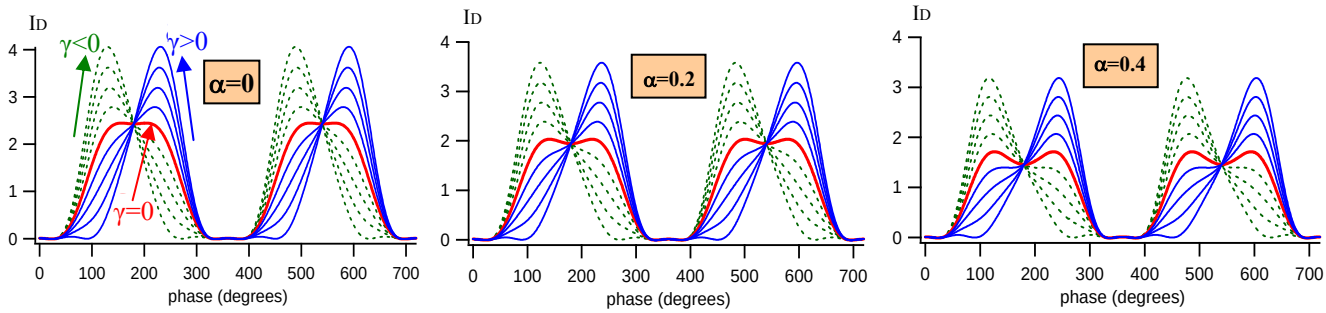

Fig. 6.18 - Theoretical extended Continuous Class-FI^{-1} current waveforms for $-1 \leq \delta \leq 1$ in steps of 0.25 and $0 \leq \alpha \leq 0.4$ in steps of 0.2.

It can be seen from Fig. 6.19 that drain efficiency varies with α, but would be maintained constant with varying δ. However, it is important to highlight that in order to present a positive second harmonic impedance (inside the Smith chart), the parameter α should be constrained between 0 and 1. This is because for negative values of α, $-1 < \alpha < 0$, the current waveform will still be positive, but negative second harmonic impedances need to be presented [18-19] in order to allow the Continuous mode to exist.

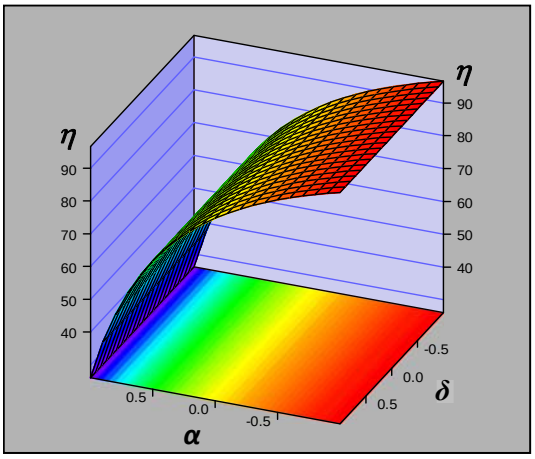

Fig. 6.19 – Theoretical Extended Continuous Inverse Class-FI efficiency (η) contour plot function of α and δ with both been varied between -1 and 1.

Fig. 6.20 shows the variation of efficiency as a function of α with a constant value of δ=0. It can be seen that for α=0 the standard Class-F^{-1} with drain efficiency (η) of 81.85% is obtained. When increasing α, the value of efficiency starts to decrease, but considering a certain pre-determined target minimum value of efficiency, in this case η=70%, thus giving a maximum value for α=0.4, a very large range of impedances can be obtained maintaining efficiencies greater than

70%. The small degradation in efficiency is traded-off against the advantage of having multiple solutions in order to facilitate the design of broadband PAs. It should be noted that for $\alpha<0$ the efficiency increases from its optimum of 81.85% up to almost 100%. Again, this is due to the fact that for $\alpha<0$ negative second harmonic impedances are presented. For the analysis and measurements presented in this paper, only positive values of α, thus positive impedances, have been considered.

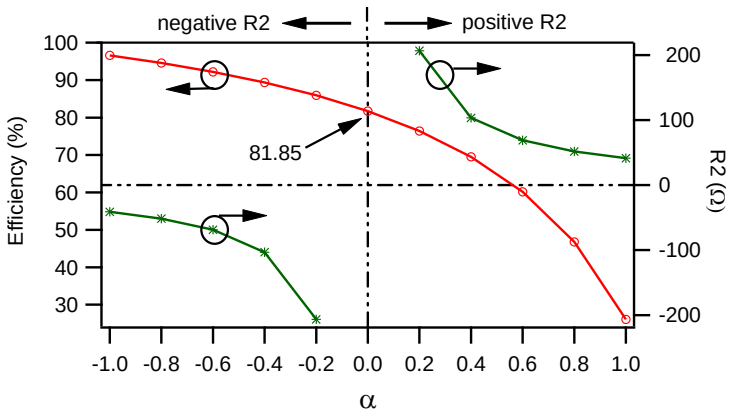

Fig. 6.20 – Theoretical Extended Continuous Inverse Class-FI efficiency and second harmonic resistance function of $-1 \leq \alpha \leq 1$ in steps of 0.2, for constant δ=0.

Table 6.I shows the reflection coefficient of both fundamental and second harmonic impedances as a function of α, for $0 \leq \alpha \leq 0.4$ with steps of 0.1, for a constant value δ=0 and considering a 50 Ω optimum fundamental load for the standard class-F^{-1}.

TABLE 6.I
REFLECTION COEFFICIENTS (Γ) OF FUNDAMENTAL AND SECOND HARMONIC IMPEDANCES AS A FUNCTION OF ALPHA

	α=0	***α=0.1***	***α=0.2***	***α=0.3***	***α=0.4***
|Γ| @ Z_{F0}	0	0.046	0.096	0.15	0.21
|Γ| @ Z_{2F0}	1	0.78	0.61	0.46	0.34

The phases of both Z_{F0} and Z_{2F0} are all equal to zero for the different values of α, as in this case a constant value δ=0 has been considered (impedances on the real axes of the Smith chart). Besides, as it can be seen from both Table 6.I and Fig.

6.17, starting from the standard Class-F^{-1} condition (α=0) where Z_{F0}=50 Ohm (0∠0°) and Z_{2F0}=open-circuit (1∠0°), increasing the value of α, the fundamental load goes toward higher impedances whilst the second harmonic load goes inside the Smith chart. The third harmonic impedance is kept constant at a short-circuit.

6.5.2 Experimental Results

The design space defined theoretically in Section 6.5.1 has been experimentally explored using the same active envelope load-pull (ELP) measurement system developed at Cardiff University and described in Chapter 2.

The measurements have been carried out on the same GaAs power transistor at 4 V of drain voltage and 1 GHz fundamental frequency.

Initially, the same process applied in Section 6.2 has been applied to the standard Inverse Class-F state. Here, for the 1 GHz frequency condition, the optimum device bias voltage and fundamental impedance for which the best trade-off of power, efficiency and gain has been obtained were V_{GS}=-0.45 V and Z_{F0}= 150+j*0 Ω (at the device current generator plane) respectively. The second and third harmonic impedances were open-circuited and short-circuited respectively. Again, once this initial point was established, the new theory described in the previous Section was applied and the new impedance points have been investigated (function of α and δ) as shown in the Smith chart of Fig. 6.21.

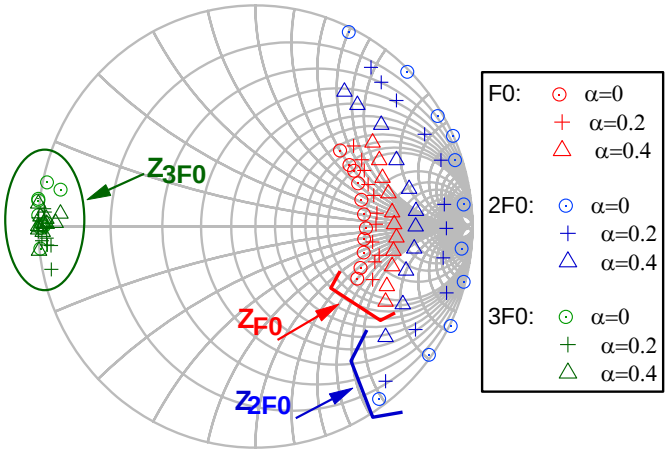

Fig. 6.21 - Measured extended continuous Inverse Class-F range of fundamental (red) second (blue) and third (green) harmonic loads for α=0 (circles), α=0.2 (crosses) and α=0.4 (triangles).

Fig. 6.22 shows the measured current and voltage waveforms for the impedance points presented in Fig. 6.21, which means for $0 \leq \alpha \leq 0.4$ and for $-1 \leq \delta \leq 1$ both with steps of 0.2; in addition the load-lines for $0 \leq \alpha \leq 0.4$ with step of 0.2 and for $-1 \leq \delta \leq 1$ with step of 1 are also presented. As predicted in the theoretical waveforms (Fig. 6.18), when increasing the parameter α, the achievable maximum peak current waveform decreases. Again, the waveforms for δ=0 (red ones) show bigger troughs with increasing α, consistent with theoretical predictions.

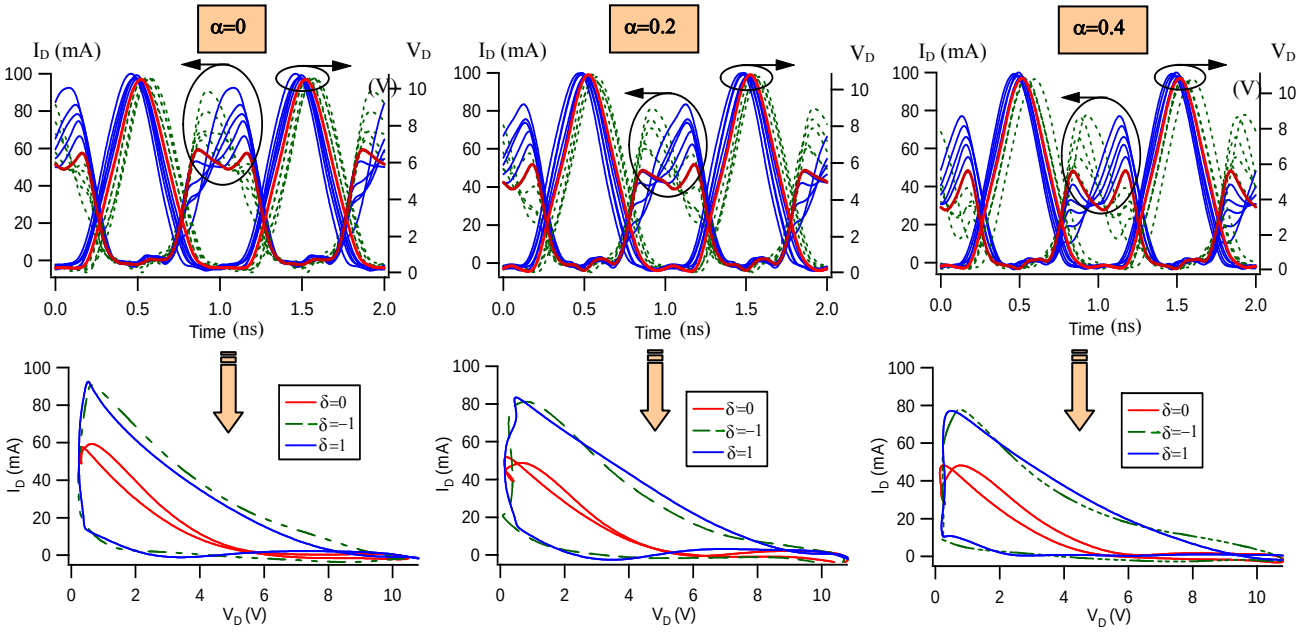

Fig. 6.22 - Measured extended continuous class-F^{-1} current waveforms when varying $-1 \leq \delta \leq 1$ in steps of 0.2 and $0 \leq \alpha \leq 0.4$ in steps of 0.2 and load-lines for $-1 \leq \delta \leq 1$ in steps of 1 and $0 \leq \alpha \leq 0.4$ in steps of 0.2.

All these new current waveforms are achieved for fundamental and second harmonic impedances varied in accordance with equations (6.9), (6.10), (6.12) and (6.13) and shown in Fig. 6.22, therefore in this case such equations have been normalized to the optimum initial fundamental impedance of R_l=150+j0 Ω. For all the measurements, the third harmonic impedance was set close to a short-circuit whilst the higher impedances greater than three have been considered to be equal to the measurement system characteristic impedance, i.e. 50 Ω.

Figures 6.23 and 6.24 show the measured drain efficiency, output power, available gain and source available power as a function of both α and δ. It can be seen that when varying the parameter δ, the device output performance can be

maintained as almost invariant. The power is approximately constant for the whole range of δ whilst the efficiency is maintained greater than 70% with maximum peak up to 80.9%. The efficiency drops on the edges of the range for the last points of δ=±1. The available gain decreases with decreasing δ, this is due to the fact that for δ<0 the device need to be driven harder in order to maintain a constant voltage waveform, this requirement is also identified in the P_{AVS} trace.

When varying the parameter α, the output performance is obviously degraded as the second harmonic impedance goes inside the Smith chart. However, by adjusting the fundamental impedance in accordance with this new theory, efficiencies greater than 70% can still be achieved, thus allowing the realization of high efficiency Class-F^{-1} PAs, but now for a significantly expanded design space. This will then translate into the ability to design circuits with variable reactive impedances, tracking this "design space" over a wider band of frequencies.

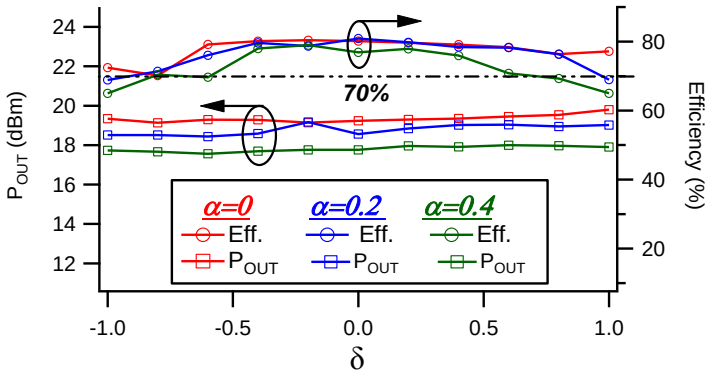

Fig. 6.23 - Measured drain efficiency and output power when varying $-1 \leq \delta \leq 1$ and $0 \leq \alpha \leq 0.4$ with both in steps of 0.2.

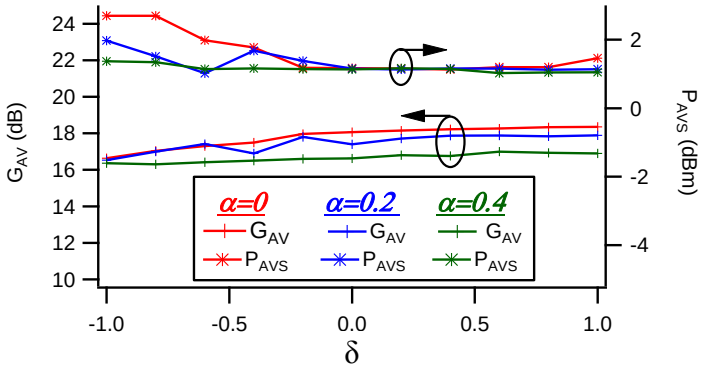

Fig. 6.24 - Measured available gain G_{AV} and source available power when varying $-1 \leq \delta \leq 1$ and $0 \leq \alpha \leq 0.4$ with both in steps of 0.2.

6.6 Continuous Inverse Class-FI PA Realisation

Here a first PA design based on the Continuous Inverse Class-FI approach has been realised. The design and realisation of this mode was based on the same 10 W GaN HEMT device from CREE that was used for the realisation of the Continuous Class-FV at 28 V of drain voltage and 2 GHz of fundamental frequency.

Initially the device was optimised in order to present the optimum classic Inverse Class-F state. The different parameters: input bias V_{GS}, input power P_{IN} and fundamental and harmonic impedances have been swept for the achievement of the best trade-off between power, efficiency and gain.

Optimum Inverse Class-F bias voltage V_{GS}=-2.7 V, input available power P_{IN}=33 dBm and fundamental and harmonic impedances Z_{F0}=54.3+j0.37 Ω, Z_{2F0}=open-circuit and Z_{3F0}=short-circuit have been found at the device intrinsic current generator plane after de-embedding the package and extrinsic elements. Fig. 6.25 shows the simulated drain efficiency, output power and gain function of the input power sweep for the bias voltage and impedances previously described. Maximum drain efficiency of DE=84.7%, output power of P_{OUT}=41.2 dBm and gain of G=18 dB have been achieved for which the device is at around 2 dB of gain compression with maximum linear gain of 22.5 dB. Fig. 6.26 shows the related Inverse Class-F half-wave rectified sinusoidal voltage waveform (second harmonic peaking) and the compressed square current waveform at both the device intrinsic and package plane with the load-lines shown in Fig. 6.27.

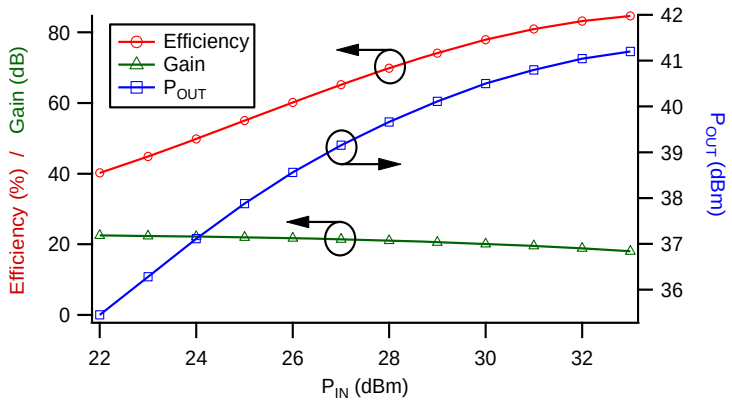

Fig. 6.25 – Drain efficiency, output power and gain as a function of the input power sweep.

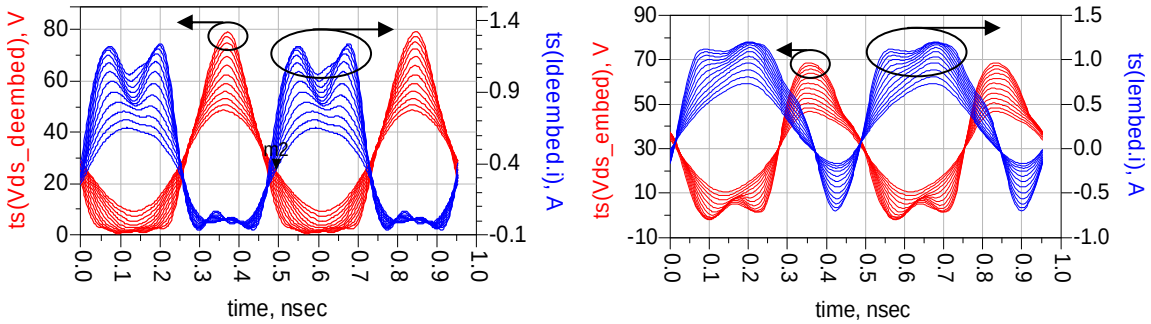

Fig. 6.26 – Drain voltage (red) and current (blue) waveforms at the device intrinsic current generator plane (left) and device package plane (right) function of the power sweep.

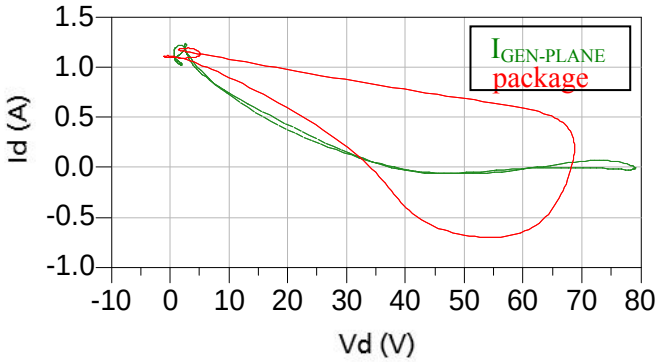

Fig. 6.27 – Load-lines at the device intrinsic plane (green) and package plane (red) at input power P_{IN}=33 dBm.

After achieving the standard Inverse Class-F state, the Continuous Inverse Class-FI mode theory presented in Chapter 3 has been applied and the various ranges of fundamental and second harmonic impedance have been identified at the device current generator plane ($I_{GEN-plane}$) and then shifted to the package plane (as detailed in Chapter 5) as shown respectively in the Smith charts of Fig. 6.28.

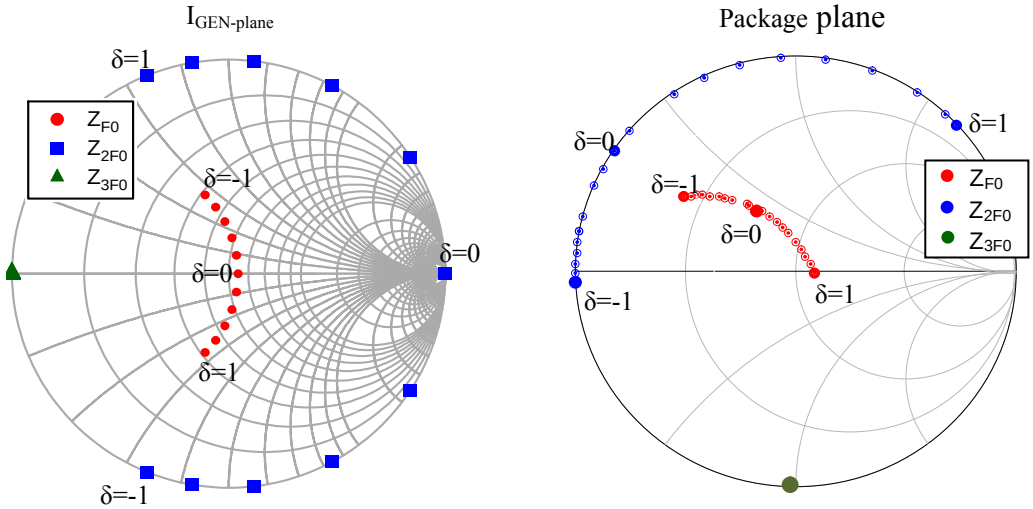

Fig. 6.28 – Continuous Inverse Class-FI first three harmonic impedances at the intrinsic plane (left) and package plane (right).

The different impedance points determined by applying the Continuous theory can then be considered points on the Smith chart where the output performance is maintained constant. Therefore by designing the appropriate output matching network capable of synthesising such impedances as a function of frequency, as shown in the in the PA layout of Fig. 6.29 (the green circles represent the decoupling capacitors), the constant optimum output performance is obtained over a given bandwidth, with the simulated results shown in Fig. 6.31.

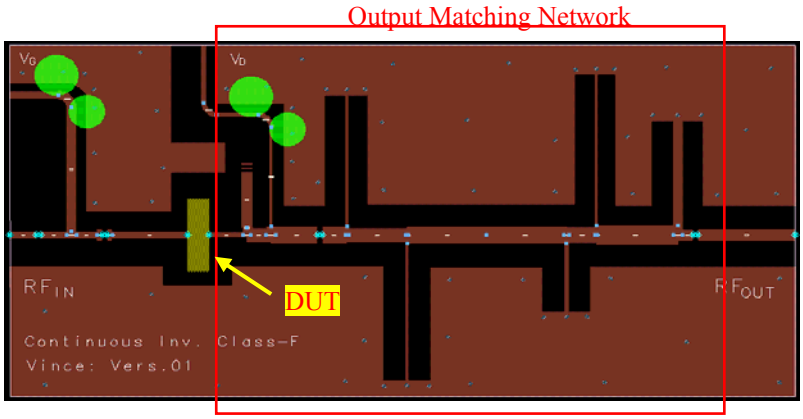

Fig. 6.29 – Continuous Inverse Class-FI Layout.

From the simulation results it can be noted that the performance is maintained almost constant over the frequency band 1.2-2.8 GHz. In particular, the power is maintained almost constant between 39.9 dBm and 41.4 dBm in the frequency range 1.2-2.6 GHz while the gain is maintained around 15 dB and 17 dB in the whole range 1.2-2.8 GHz. The drain efficiency is kept greater than 60 % with maximum peak up to around 78% in the frequency range 1.5-2.6 GHz. It is important to highlight that the high power-efficiency state cannot ideally reach or break the octave bandwidth with the Continuous theory. This is due to the fact that the fundamental and harmonic impedance will be overlapped. However, real designs cannot maintain the performance perfectly constant over frequency. Such power-efficiency tends to degrade on the edge of the given bandwidth as shown in the measurement results presented in this thesis.

Fig. 6.30 shows the photo of the actual Continuous Class-FI^{-1} PA realisation. Unfortunately the measured results do not match with the simulation performance.

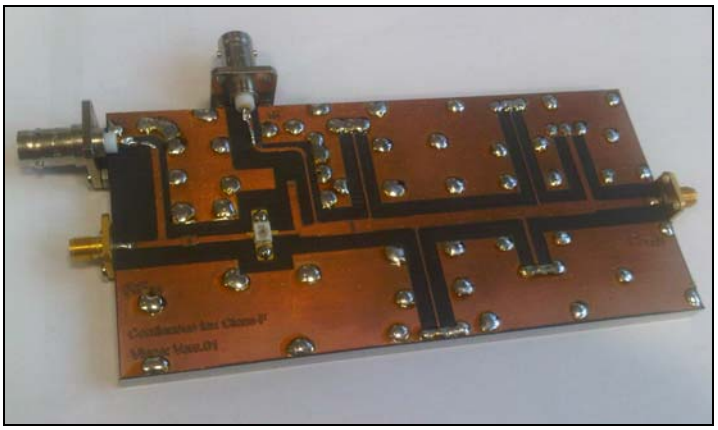

Fig. 6.30 – Continuous Inverse Class-FI photo.

First of all it can be noted from the measured results of Fig. 6.31 that the frequency range for which acceptable output results are achieved is smaller compared with simulation performance, in this case from around 1.3 GHz to 2 GHz. Here, the drain efficiency is maintained greater than 50% from 1.2 to 2.05GHz (with maximum value of 64% at 1.5 GHz) however still resulting in around 49% of bandwidth. The output power is maintained almost constant around 40-41 dBm from 1.2 to 2.1 GHz. However, disappointing gain between 5 and 10dB has been achieved in the requested bandwidth. This is mainly due to the fact that such PA has not been matched in the input side, even though better gain performance was expected.

Despite the disappointing results compared with the simulation performance, it can be noted that the output power and gain are maintained around constant for almost 50% bandwidth in the frequency range 1.2-2.7 GHz. The drain efficiency can be surely improved (at the higher frequency greater than around 1.5GHz) of around 5-10% over the bandwidth by designing a more accurate output matching network, while the gain can be improved 5-10 dB more if taken into account and designing the input matching network.

The improvement of such new PA mode can be addressed in further research and future work (as some considerations have been given in Future Work of Chapter 7), studying the different behaviours of the Continuous inverted and Continuous non-inverted PA modes for the actual PA realisations.

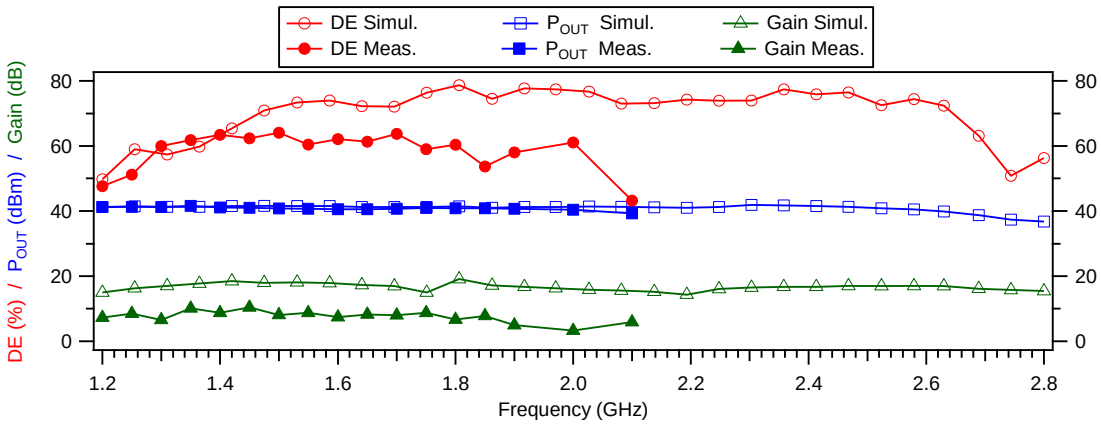

Fig. 6.31 – Simulated and measured Continuous Inverse Class-FI drain efficiency (DE), output power (P_{OUT}) and Gain function of frequency.

6.7 Chapter Summary

In this Chapter the full procedure for an optimum Class-F^{-1} PA design has been initially shown. Here it has been shown that by sweeping the different parameters in the appropriate way: input bias, input power and fundamental and harmonic impedances, an optimum Class-F^{-1} PA design can be realised. Starting from here, a new theory termed Continuous Inverse Class-F has been applied. In this theory (presented in detail in Chapter 3) it has been discovered that by varying properly and reactively the fundamental and harmonic terminations from the short or open-circuit points, different voltage and/or current waveforms are obtained for which the output device performance is maintained almost constant from the initial optimum classic Class-F^{-1}. The theory has been applied on both the voltage and current waveforms, therefore named Continuous Class-FV^{-1} and Continuous Class-FI^{-1}. Indeed, an extended mathematical formulation applied on the current waveform has shown that by varying the second harmonic load inside the Smith chart from the open-circuit condition and adjusting properly reactively, and now also resistively the fundamental impedance the output performance does not degrade significantly from its optimum behaviour. The measurements carried out on the GaAs pHEMT transistor have shown a good agreement with the theoretical performance thus validating this new broadband PA approach.

Furthermore, for the first time the physical Continuous Inverse Class-FI PA has been realised. Here the PA performance does not match the same performance carried out in the simulation design. However, high power-efficiency has been still achieved in the frequency range between 1.3 GHz and 2 GHz.

6.8 *References*

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Chapter 7

Conclusion and Future Work

7.1 Conclusion

The research presented in this thesis aimed to explore new modes for the realisation of high power-efficiency and broadband power amplifiers (PAs) used in wireless communications. The continuous demand of wireless services has led the scientific community to improve such networks, and as a result, cellular phones and base stations have improved considerably in the last few years.

The objective of developing new power amplifier modes comes hand-in-hand with the concept of waveform engineering which is related to multi-harmonic output matching requirements.

From the literature review, as shown in **Chapter 2**, the different combinations of input bias and output impedances lead to the different standard PA classes, starting from the linear Class-A state, through the switched modes Class-D and Class-E to the high-efficiency harmonically tuned Class-F and Inverse Class-F. These standard PA modes have shown in the last 20-30 years the possibility of delivering high output overall performance for "*narrow band*" frequencies. This means that to satisfy the wide bandwidth requirements of nowadays and future

4G-5G standards new practical solutions need to be developed. Therefore, a new research investigating for the first time what has been here termed "*Continuous Mode*" has been in this thesis undertaken.

The discovery of these "*Continuous Modes*", explained theoretically in **Chapter 3,** shows for the first time that any standard PA mode reveals a continuous set of waveforms where output power and drain efficiency are maintained theoretically constant. The different waveforms are revealed by presenting simultaneously and properly different fundamental and harmonic terminations. Therefore, the possibility of having different solutions where the output performance does not change is translated in what has been termed "*Design Space"* where the overall PA performance does not degrade from its initial optimum behaviour.

The Continuous Modes described experimentally in Chapter 3 have been experimentally demonstrated in **Chapter 4** on the Class-F mode, in this case termed *Continuous Class-FV*. The experimental measurements have shown that once the standard Class-F mode is obtained delivering in this case 20 dBm of output power and around 80-85% of drain efficiency, the new *Continuous Class-FV* mode can maintain such output performance over different load solutions, which is translated into different frequency points allowing the realisation of high power-efficiency and now broadband PAs. Indeed, an extended theory of the Continuous Class-FV mode has been for the first time theoretically and experimentally presented through measurement results for which the fundamental and second harmonic impedances were allowed to vary both reactively and resistively while still keeping the overall performance greater then a certain value, in this case 75%.

The actual physical PA realisation using the *Continuous Class-FV* approach has been here for the first time realised and presented in **Chapter 5**. The realised PA delivers drain efficiency between 65% and 80% for an octave (66.7%) bandwidth. In this range of frequencies output power was between 39.3 dBm and 41.2 dBm. The average gain was around 11 dB (from 9.5 dB to 12 dB) across the bandwidth. Furthermore, here it has been seen that when designing broadband PAs, the harmonic terminations cannot easily be constrained to short-circuit and/or open-

circuit conditions with varying frequency. Therefore, the possibility of presenting the appropriate variable third harmonic termination as well as the fundamental and second harmonic is an important step for the realisation of broadband PAs allowing easier, more flexible and achievable design requirements. The measurement results varying simultaneously the first three terminations have delivered satisfactory performance thus validating the new approach.

Chapter 6 describes the experimental measurements conducted for the achievement of the Continuous mode applied to the Inverse Class-F state. Here both the voltage and current waveforms have been varied by applying the different theories termed *Continuous Class-FV* and *Continuous Class-FI*. As for the Continuous Class-F case, the measurements show a good agreement with the theoretical results, where the output performance in terms of drain efficiency and output power was maintained almost constant at around 75-80% and 19-20 dBm respectively. Again, as for the Continuous Class-FV, an extended version of the Continuous Inverse Class-FI mode has been theoretically and experimentally presented.

Table 7.I shows the State-of-Art (last 5 years: 2009-2013) summarizing some of the single ended broadband power amplifiers operating for L band, S band and below. Despite different techniques can be applied for the achievement of broadband PAs, after the introduction of the class-J [1-2] and then the Continuous mode approach [3-8] presented in this thesis, various PA using such techniques for the realisation of broadband PAs operating in the mobile phone communication frequency range have been exploited and realised.

As it can be noted from such Table 7.I, the first Class-J PA was realized in 2010 at Cardiff University [2], showing for the first time the possibility to realize broadband PAs through proper fundamental and second harmonic matching delivering efficiency in the range of 60-70% for the broadband spectrum BW=60% (BW=Bandwidth).

The first realisation of Continuous Class-FV PA (presented in this thesis) highlighted in red in Table 7.I, has shown a broadband (BW=67%) power amplifier while delivering efficiency greater than Class-J, in this case >65% with maximum

peak up to 80%. The choice of realizing Class-J or Continuous Class-F PA depends of the trade-off between the linearity and efficiency requirement, as explained in Chapter 2 of this thesis.

Overall, the novelty of this research was in presenting new theoretical analysis supported by measurement results as well as the actual power amplifier realisation for which the output performance is maintained constant for different load solutions, thus validating the novel approach. As explained throughout this thesis, the different *Continuous Mode* output load solutions for which the PA performance remains constant/satisfactory, allows the realisation of broadband power amplifiers by proper output matching. Such wideband PAs can therefore be used in mobile phones and base station transmitters for the next generation of wireless communication standards.

TABLE 7.I
STATE-OF-ART OF BROADBAND POWER AMPLIFIERS IN THE MOBILE PHONE COMMUNICATION FREQUENCY RANGE

Year [Ref]	Freq (GHz)	BW (%)	DE & PAE (%)	Pout (dBm)	Mode
2009 [9]	2-2.5 2.1-2.7	22.2 25	PAE > 71 PAE > 53	38.5-41 39.7-41	ClassE
2009 [10]	1.9-2.9	42	DE = 60-65	45-45.8	Simplified real frequency technique
2010 [2]	1.4-2.6	60	DE = 60-65	40	Class-J
2010 [5]	**0.55-1.1**	**67**	**DE = 65-80**	**39.3-41.2**	**This work Continuous Class-FV**
2010 [11]	1.9-4.3	78	DE = 57-72	40-41.7	Source-pull/load-pull
2011 [12]	1-2	67	PAE≈50	48-50	Source-pull/load-pull
2011 [13]	0.9-2-2	83.9	63-89	40-43	Class-E
2011 [14]	2.3-2.7	16	60-69	40-40.8	Class-J
2012 [15]	0.5-1.8	113	50-69	39-40.8	Class-J
2012 [15]	1.6-2.2	33	55-68	40-41	Class-J
2012 [16]	0.9-1.5	50	55-61	43.2 (avg)	Exploiting wideband large signal matching
2012 [17]	1.3-3.3	87	DE = 60-83	40-40.4	Continuous ClassF / Continuous ClassF^{-1}
2013[18]	0.1-1	163	PAE=54.5-61.3	30.7-31.7	Feedback technique
2013[19]	2.25-3.075	31	DE = 50-58	24-27	Class-J

7.2 Future Work

The work discussed in this thesis has provided a significant step forward for the realisation of new broadband power amplifiers used in the ongoing wireless communication systems.

Various theories supported by experimental results with an actual PA realisation have been discussed. However, this section outlines the future work necessary in moving forward the work undertaken in this thesis.

7.2.1 Linearity in Continuous Modes

Stepping through this thesis it can be noted that this research was mainly focused on the optimisation of power and efficiency for the broadband spectrum requirements.

Another very important parameter which has not been investigated for these new Continuous Modes (however shown in the PA realisation of Chapter 5) is the "*linearity*". The linearity is the parameter which refers to the fidelity of the signal. Therefore, any wireless network must satisfy the requirements of high efficiency, high power and high gain for the specified broadband frequency spectrum as well as satisfying the appropriate linearity requirements of the used standard. For example, the UMTS (Universal Mobile Telecommunication System) standard requires WCDMA (Wideband Code Division Multi Access) modulation with 5 MHz bandwidth and adjacent channel power ratio (ACPR) of -45 dBc at the offset frequency of 5 MHz with a signal of PAR of 7 dB to 10. This means that the third order intermodulation (IM3) signals must be at least -45dBc lower than the fundamental carrier.

Unfortunately, high power-efficiency over a wide band of frequencies with high linearity performance is not easy (or even possible), or very expensive in actual applications. High efficiency systems would degrade the linearity performance and vice versa as shown in Fig. 7.1.

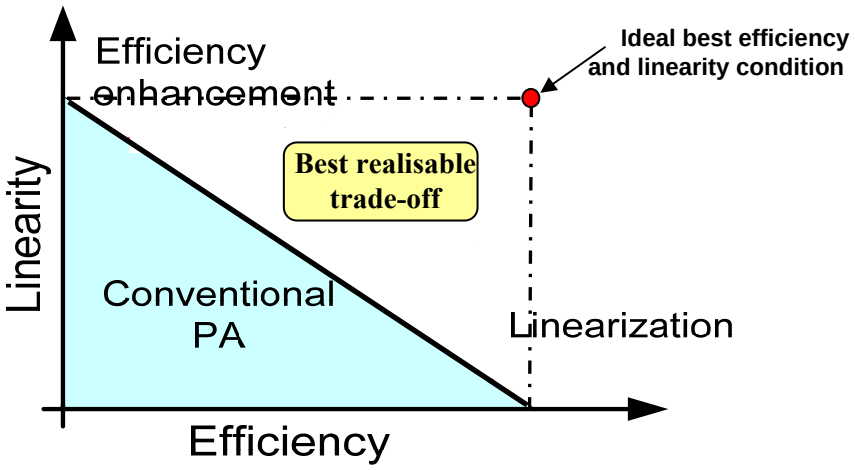

Fig. 7.1 – Linearity and Efficiency trade-off.

There are different enhancement techniques for the realisation of linear power amplifiers, starting from the known predistortion approaches [1, 20] to the more advanced baseband impedances enhancements [21-22], through other advanced linearization techniques as [23-26].

Furthermore, it is common that once the high efficiency state is obtained using highly efficient but non-linear modes, linear operation can be achieved by reducing the RF input power to a level that is sufficiently low to avoid saturation of the active devices. When a high degree of linearity is required, the back-off mode of operation inevitably degrades overall efficiency and output power. Consequently, as indicated in Fig. 7.1, in modern RF power amplifier applications fulfilling linearity, for preserving fidelity of the signal, as well as power amplifier efficiency, imposes two conflicting design requirements.

The Continuous Modes presented in this work show how to design broadband power amplifiers. In particular by varying properly and simultaneously the fundamental and high harmonic output impedances the power and efficiency are maintained constant. However, no theoretical or experimental investigations have been carried out in terms of linearity when presenting the different load conditions. In this work, the linearity has only been measured on the Continuous Class-FV PA presented in Chapter 5. It is important to highlight that the Continuous-broadband

PA was designed/built from the Class-F mode, thus from a non-linear mode as high harmonics are taken into account for the achievement of the high efficiency state. However, it has been demonstrated that despite the non-linear behaviour of such PA, these Continuous modes can be predistorted by using a generic linearity pre-distortion enhancement technique [27] as shown in Chapter 5. Therefore, the linearity can definitely be improved satisfying the requirements of 3G as well as present and future 4G and 5G standards.

Future work can be addressed on the study of the linearity performance of the Continuous modes when presenting different reactive fundamental and high harmonic load conditions. Any new solution would probably show a different linearity result, therefore, future work in this area would reveal if these broadband modes deliver worse or better linearity performance compared with the classic narrow band modes.

7.2.2 Continuous Class-AI Considerations

Chapter 3 has presented the overall Continuous modes applied on the various classes, and it has been theoretically demonstrated that each standard case reveals a continuum of waveforms. Such theoretical analysis was also accompanied by simulations results confirming the validity of the new approach. Unfortunately such simulation analysis, described in Appendix C, did not deliver the desired output performance when applied on the Class-AI case. Despite the variation of the parameter ξ, the current waveform did not vary from its starting sinusoidal shape. This is probably due to the fact that only first two harmonic terminations have been taken into account. The thinking is that if considering more than two harmonics, at least up to the third, the approach will work on this mode as well. The use of the third harmonic termination would probably improve the performance on the Continuous Class-AV as well. However, this mode needs to be improved with further investigations; therefore it can be left open for future work carrying on the research presented in this thesis.

7.2.3 Continuous Inverse Class-FI PA Considerations

Chapter 3 has presented the theoretical broadband Continuous PA modes applied to the different standard PA states showing that each standard mode reveals a continuum of waveforms/solutions through the correct combination of fundamental and harmonic terminations, where the overall output performance does not degrade. Using an active load-pull measurement system capable of presenting the proper fundamental and harmonic output impedances some of the Continuous theories have also been validated through measurement results, in this case applied to the Class-F and the Inverse Class-F modes.

The actual physical power amplifiers have been realised based on the Continuous Class-FV [4-5] and Continuous Inverse Class-FI modes [6]. The Continuous Class-FV has revealed satisfactory results in terms of both power-efficiency and bandwidth. The Continuous Inverse Class-FI did not reach the targeted specifications.

The simulation based on the Continuous Inverse Class-FI design has revealed very good performance both in terms of power, efficiency and gain in the wide frequency range from 1.2 GHz to 2.6 GHz. However, despite the satisfactory simulations the actual PA did not deliver the expected performance.

This could be due to the fact that in the non-inverted mode the current waveform corresponds almost entirely with a voltage that is inside to the knee clipping region. Therefore the associated current waveform takes place through very small changes in the lower part of the voltage waveform. This means that a very small variation in the bottom part of the voltage waveform corresponds to a large variation in the top part of the current waveform.

This concept can however be investigated in future work. Successful work in this area, where allowing the realisation of the Continuous modes based on both inverted and non-inverted classes, would allow the PA community to realise broadband power amplifiers for different specifications, device properties and conditions, increasing the PA design flexibility and applicability.

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Appendices

Appendix A

ELP (Envelope Load Pull) Panels

The active envelope load-pull (ELP) measurement system calibration can be divided in two parts:

1. Calibration of the measurement system (small signal and large signal calibration).
2. Calibration of the ELP boxes (fiundamental, second and third harmonic impedances).

In this Appendix Section a brief explanation of the ELP panels available from the ELP Igor software developed at Cardiff University would be given. Detailed information of how to calibrate the measurement system and the ELP boxes is available in reference [13, 32] of Chapter 2.

Measurement System Calibration

Fig. A1 shows the panel for the measurement system:

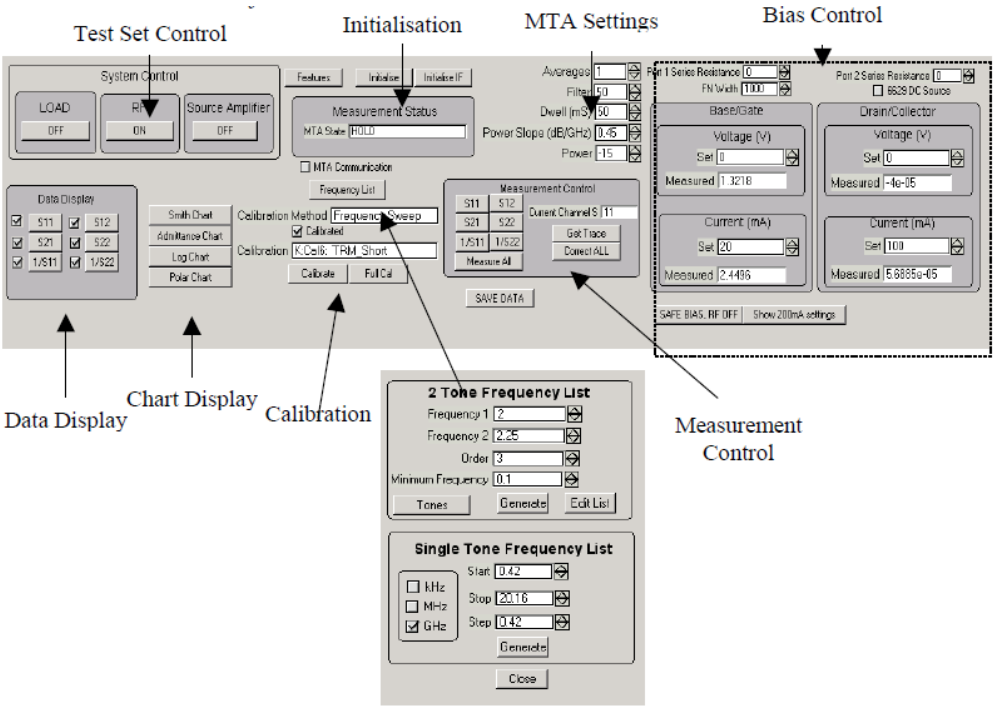


Fig. A1 – Measurement system calibration main panel.

- ***Initialisation***: enables IGOR to access to the GBIP Bus and initialise the measurement system instrumentation and switches.
- ***IF Initialisation***: Opens the IF measurement control box to control the low frequency IF test set.
- **Test Set Control**: RF, source and load switch control.
- **MTA Settings**: These control the MTA during the sweep mode of operation.
- **Bias Control:** Set the voltage and current for the DC supplies. Note negative voltage for the 6629 are supplied using an inverter.ed using the check box. Port resistance will de embed the voltage drop across resistor in the DC network.
- **Features**: Opens a second panel with additional options. Bias Dependent s-parameters.Waveform Biasing, this enables s-parameter measurements at DC Data points loaded from a file.
- **Measurement Control**: This performs sparameter measurements. Individual s-parameter buttons will produce calibrated input and output reflection coefficients.
  - *Measure All* Measures the four s-parameters to produce real s-parameters.
  - *Correct All* converts measured data from corrected reflection coefficients to s-parameters.
- **Chart Display**: This displays the relevant chart for data display and automatically displays the s-parameter checked in the data display box.
- **Data Display**: Once an s-parameter measurement has been performed, the data can be appended to a display chart manually. Check box allows automatic display of data with the chart display.
- **Frequency List**: This defines the frequency points for the MTA. The 2 Tone frequency list generates a list of frequency components generated within the bandwidth of the MTA system.
- **Calibration**: Opens the dialogue boxes to perform the s-parameter calibration and the absolute Full calibration of the system. Check box will display Corrected or Raw data on chart.

ELP Calibration

Fig. A2 shows the panel for the ELP calibration panel:

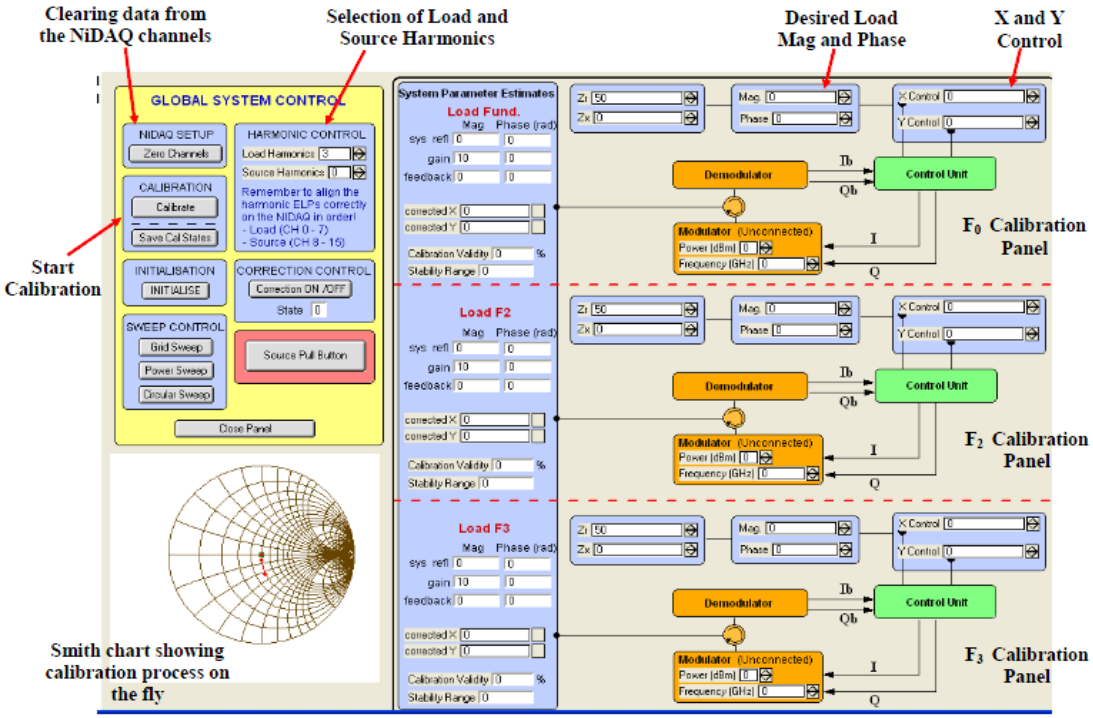


Fig. A2 – ELP calibration main panel.

- **Zero channel**: this clear the NiDAQ (digital to analog interface board from National Instruments) channel.
- **Harmonic control**: here it is possible to specify the number of harmonics to be controlled (maximum up to the 3rd).
- **Calibrate**: with this button the ELP software starts the calibration procedure. In few words, the software presents some target impedance points function of the frequency (for example usually around 15 points) as well it presents the actual impedances presented by the system. Therefore, knowing the error between target values and the one actual presented, the software can calculate the a2 wave values (for the three impedances) needed.

Output Waveform Measurement Software

Fig. A3 shows the overall output waveform measurement main panel.

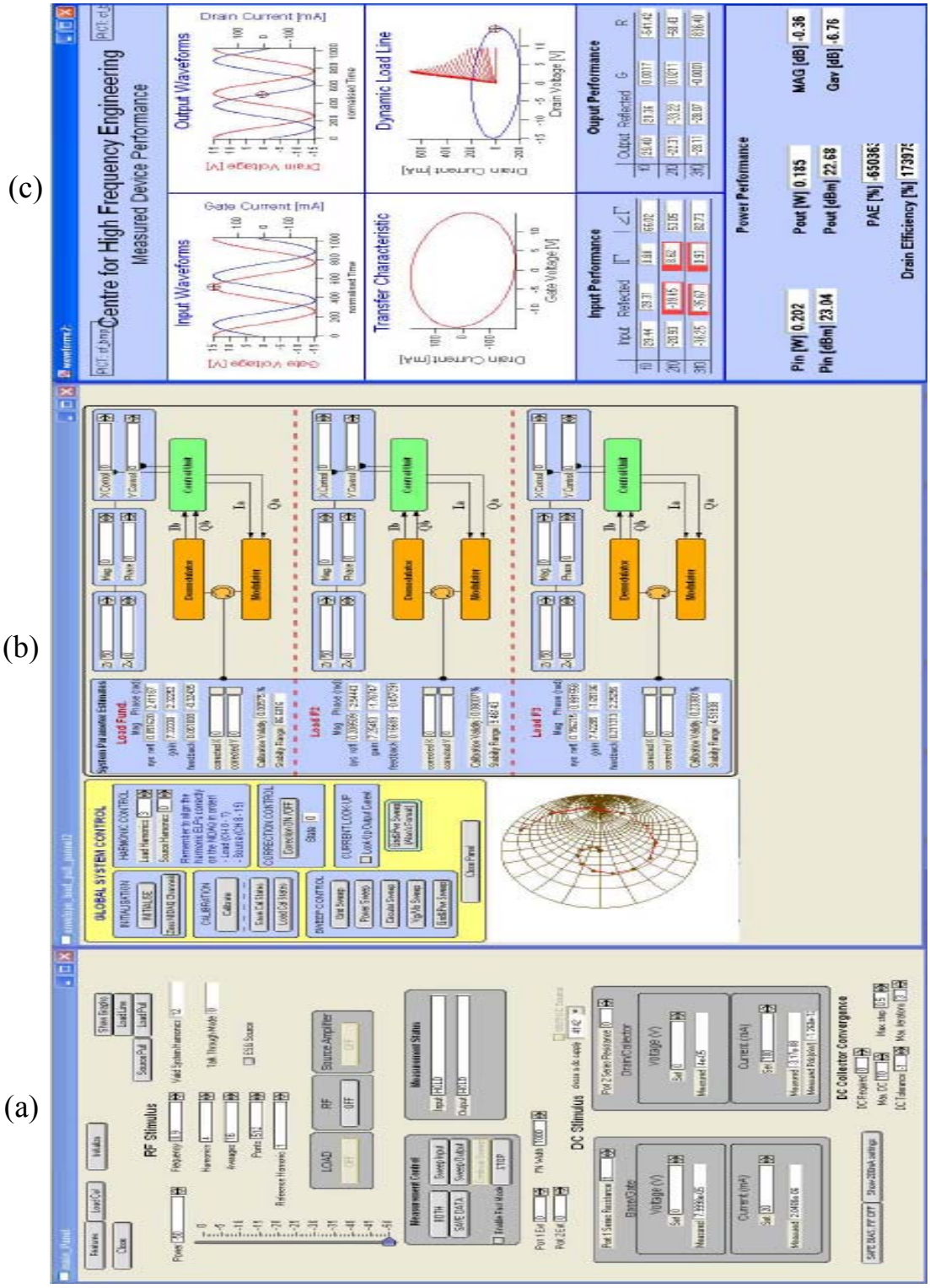


Fig. A3 – ELP waveform measurement software.

The overall measurement panel of Fig. A3 can be divided into 3 parts: a), b) and c).

(a)

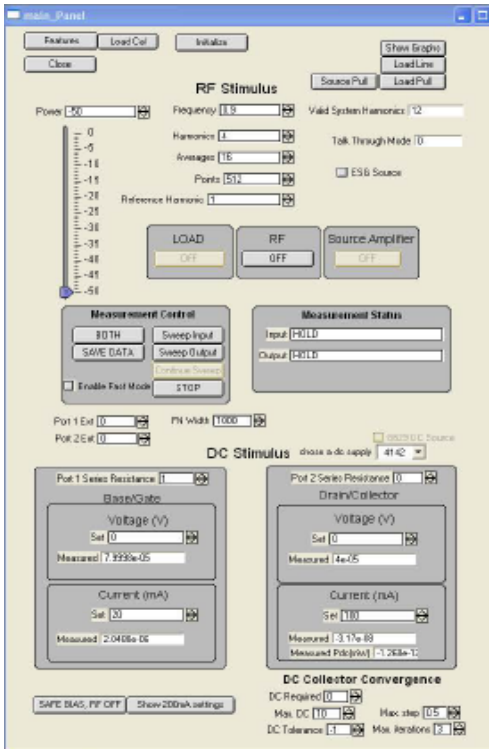


Fig. A4

In the **a)** part of the output panel (Fig. A4) it is possible to set the following different parameters:

- **Initialise**: enables IGOR to access the GBIP Bus and configures the measurement system instrumentation and switches.
- **Features**: enables to open a new window with DC supply options.
- **Load Cal:** from here it is possible to upload the calibration file.
- **RF Stimulus**: here it is possible to control the RF input power (maximum up to 0 dBm to avoid and damage on the MTA), the operating fundamental frequency, the number of harmonics taken into account, the averaging (default=64) and number of trace data points (default=512).
- **Measurement control**: here the button BOTH starts the single measurement, besides t is possible to do input and output power sweep as well as save the data.
- **DC Stimulus**: enables the setting of the input and output DC bias conditions.

(b)

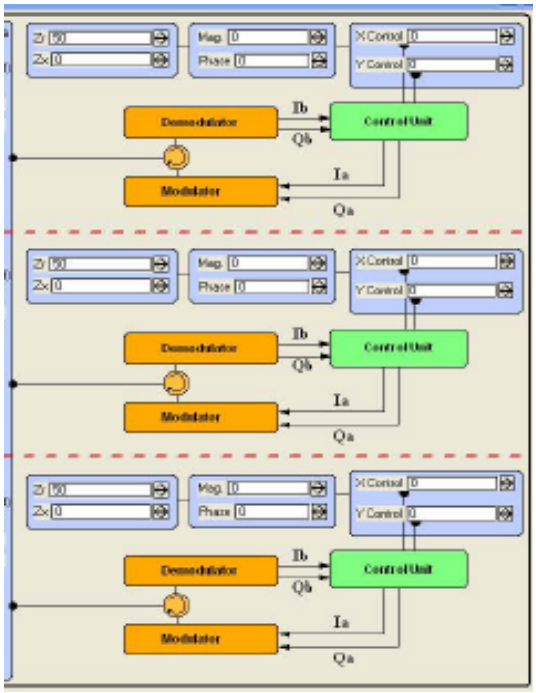


Fig. A5

The **b)** part of the panel (Fig. A5) enables the fundamental and harmonic impedances to be set.

- Here the impedances can be set either as real and imaginary or magnitude and phase or in Cartesian coordinate (X and Y).

(c)

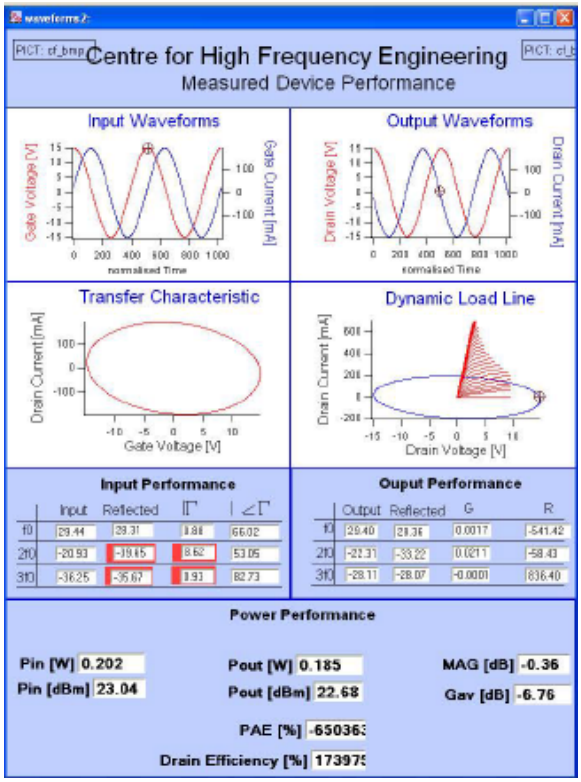


Fig. A6

The **c)** part of the overall panel (Fig. A6) displays the input and output voltage (red) and current waveforms, the transfer characteristic, the DCIV and load-line.

Furthermore it shows the input and output fundamental, second and third harmonic impedance as well as the achieved measured output parameters such as: input power, output power, drain efficiency, PAE available gain and maximum available gain

Appendix B

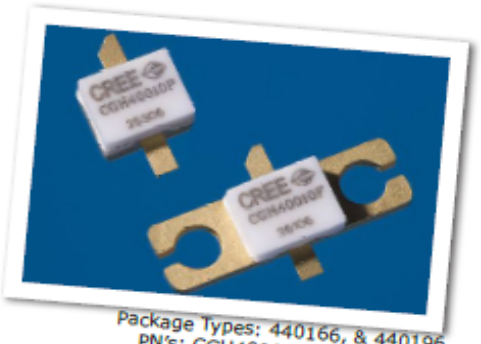
Cree CGH40010F 10 W GaN HEMT datasheet

CREE

CGH40010

10 W, RF Power GaN HEMT

Cree's CGH40010 is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). The CGH40010, operating from a 28 volt rail, offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making the CGH40010 ideal for linear and compressed amplifier circuits. The transistor is available in both screw-down, flange and solder-down, pill packages.



Package Types: 440166, & 440196
PN's: CGH40010F & CGH40010P

FEATURES

- Up to 6 GHz Operation
- 16 dB Small Signal Gain at 2.0 GHz
- 14 dB Small Signal Gain at 4.0 GHz
- 13 W typical P_{SAT}
- 65 % Efficiency at P_{SAT}
- 28 V Operation

APPLICATIONS

- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, Linear amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA waveforms

RoHS COMPLIANT

Rev 3.1 – March 2011

Large Signal Models Available for SiC & GaN

Subject to change without notice.
www.cree.com/wireless

1

Absolute Maximum Ratings (not simultaneous) at 25°C Case Temperature

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DSS}	84	Volts
Gate-to-Source Voltage	V_{GS}	-10, +2	Volts
Storage Temperature	T_{STG}	-65, +150	°C
Operating Junction Temperature	T_J	225	°C
Maximum Forward Gate Current	I_{GMAX}	4.0	mA
Soldering Temperature[1]	T_S	245	°C
Screw Torque	τ	60	in-oz
Thermal Resistance, Junction to Case[2]	$R_{\theta JC}$	8.0	°C/W
Case Operating Temperature[2,3]	T_C	-40, +150	°C

Note:
[1] Refer to the Application Note on soldering at www.cree.com/products/wireless_appnotes.asp
[2] Measured for the CGH40010F at P_{DISS} = 14 W.
[3] See also, the Power Dissipation De-rating Curve on Page 6.

Electrical Characteristics (T_C = 25°C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[1]						
Gate Threshold Voltage	$V_{GS(TH)}$	-3.8	-3.3	-2.3	V_{DC}	V_{DS} = 10 V, I_D = 3.6 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-3.0	–	V_{DC}	V_{DS} = 28 V, I_D = 200 mA
Saturated Drain Current	I_{DS}	2.9	3.5	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BR}	120	–	–	V_{DC}	V_{GS} = -8 V, I_D = 3.6 mA
RF Characteristics[2] (T_C = 25°C, F_0 = 3.7 GHz unless otherwise noted)						
Small Signal Gain	G_{SS}	12.5	14.5	–	dB	V_{DD} = 28 V, I_{DQ} = 200 mA
Power Output[3]	P_{SAT}	10	12.5	–	W	V_{DD} = 28 V, I_{DQ} = 200 mA
Drain Efficiency[4]	η	55	65	–	%	V_{DD} = 28 V, I_{DQ} = 200 mA, P_{SAT}
Output Mismatch Stress	VSWR	–	–	10 : 1	Ψ	No damage at all phase angles, V_{DD} = 28 V, I_{DQ} = 200 mA, P_{OUT} = 10 W CW
Dynamic Characteristics						
Input Capacitance	C_{GS}	–	4.5	–	pF	V_{DS} = 28 V, V_{GS} = -8 V, f = 1 MHz
Output Capacitance	C_{DS}	–	1.3	–	pF	V_{DS} = 28 V, V_{GS} = -8 V, f = 1 MHz
Feedback Capacitance	C_{GD}	–	0.2	–	pF	V_{DS} = 28 V, V_{GS} = -8 V, f = 1 MHz

Notes:
[1] Measured on wafer prior to packaging.
[2] Measured in CGH40010-TB.
[3] P_{SAT} is defined as I_G = 0.36 mA.
[4] Drain Efficiency = P_{OUT} / P_{DC}

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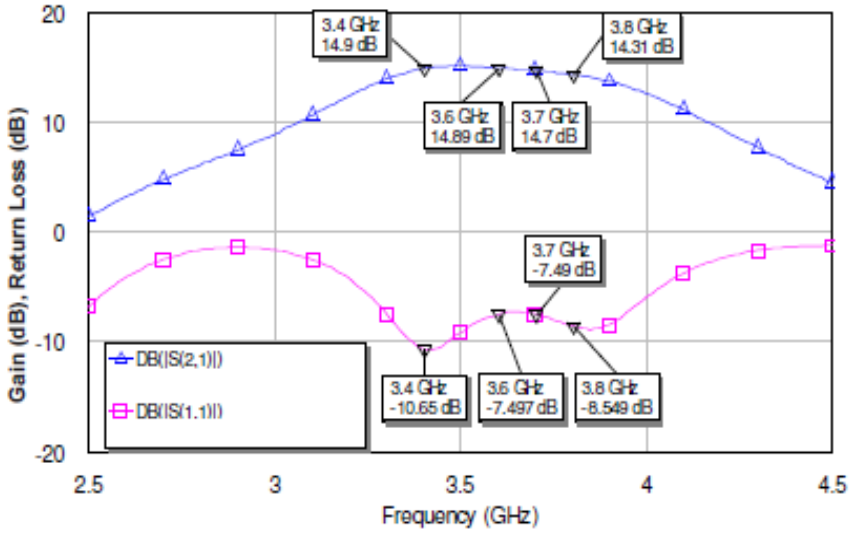
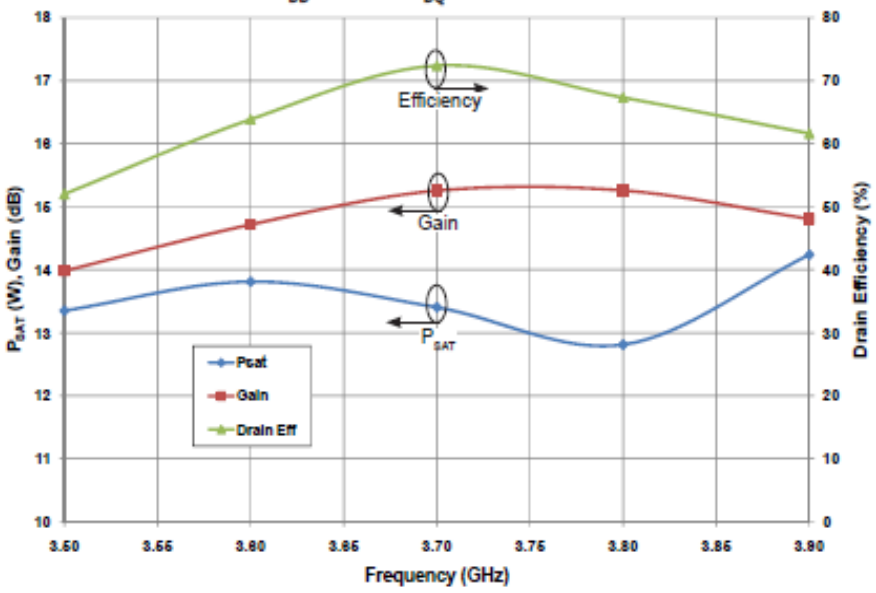
Typical Performance

Small Signal Gain and Return Loss vs Frequency of the CGH40010 in the CGH40010-TB



P_{SAT}, Gain, and Drain Efficiency vs Frequency of the CGH40010F in the CGH40010-TB
V_{DD} = 28 V, I_{DQ} = 200 mA



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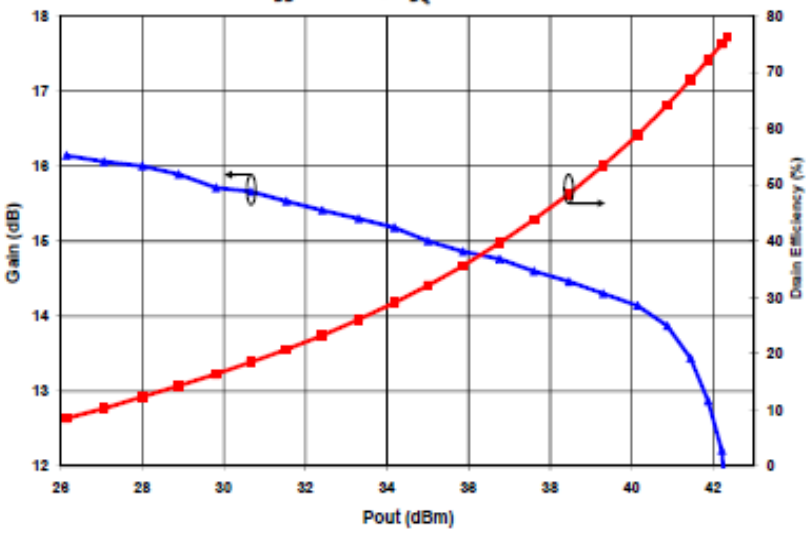
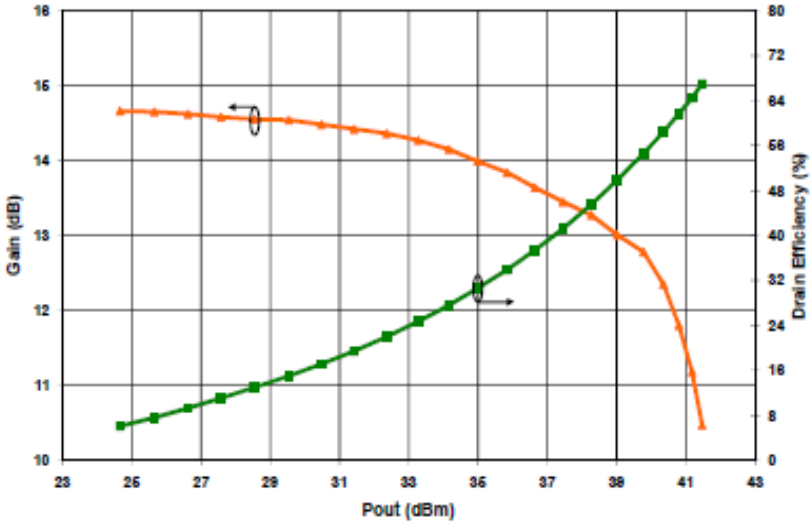
Typical Performance

Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for Drain Efficiency at 2.0 GHz
V_{DD} = 28 V, I_{DQ} = 200 mA



Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for Drain Efficiency at 3.6 GHz
V_{DD} = 28 V, I_{DQ} = 200 mA



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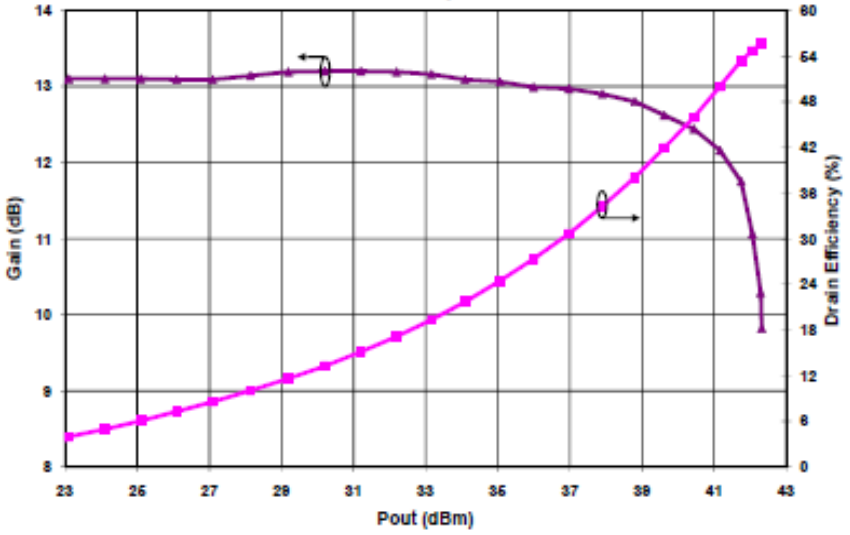
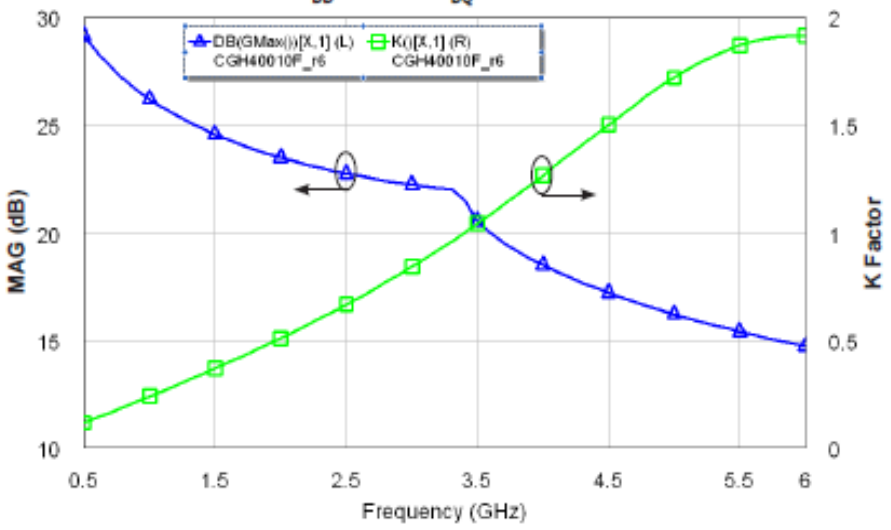
Typical Performance

Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for P1 Power at 3.6 GHz
V_{DD} = 28 V, I_{DQ} = 200 mA



Simulated Maximum Available Gain and K Factor of the CGH40010F
V_{DD} = 28 V, I_{DQ} = 200 mA



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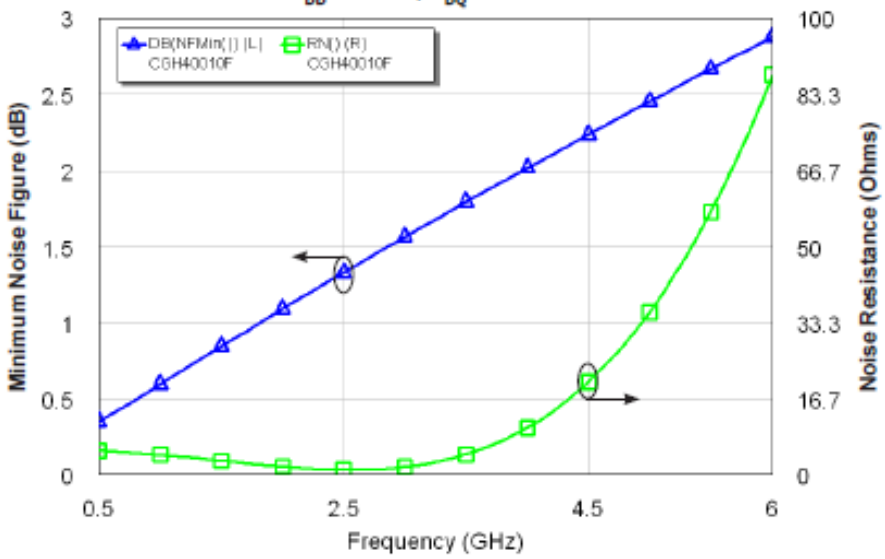
Typical Noise Performance

Simulated Minimum Noise Figure and Noise Resistance vs Frequency of the CGH40010F
V_{DD} = 28 V, I_{DQ} = 100 mA



Electrostatic Discharge (ESD) Classifications

Parameter	Symbol	Class	Test Methodology
Human Body Model	HBM	1A > 250 V	JEDEC JESD22 A114-D
Charge Device Model	CDM	1 < 200 V	JEDEC JESD22 C101-C

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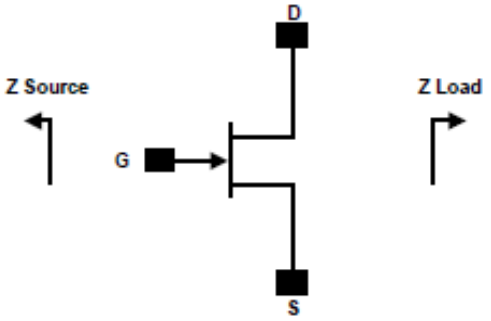
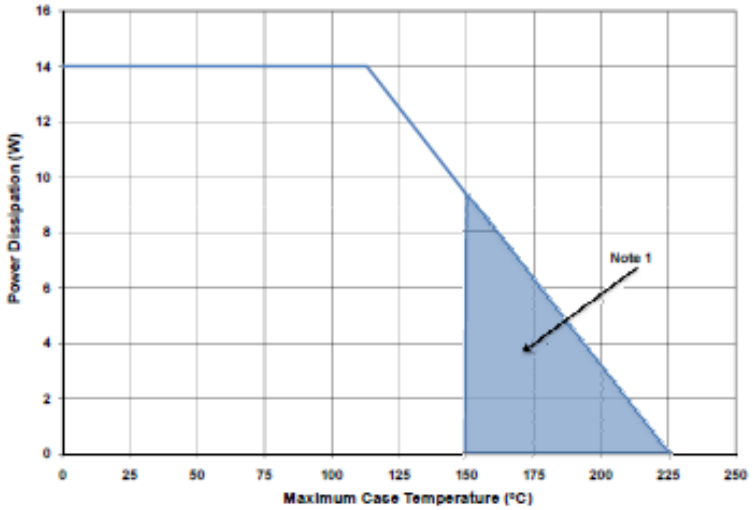
Source and Load Impedances



Frequency (MHz)	Z Source	Z Load
500	20.2 + j16.18	51.7 + j15.2
1000	8.38 + j9.46	41.4 + j28.5
1500	7.37 + j0	28.15 + j29
2500	3.19 - j4.76	19 + j9.2
3500	3.18 - j13.3	14.6 + j7.46

Note 1. V_{DD} = 28V, I_{DQ} = 200mA in the 440166 package.
Note 2. Optimized for power, gain, P_{SAT} and PAE.
Note 3. When using this device at low frequency, series resistors should be used to maintain amplifier stability.

CGH40010 Power Dissipation De-rating Curve



Note 1. Area exceeds Maximum Case Operating Temperature (See Page 2).

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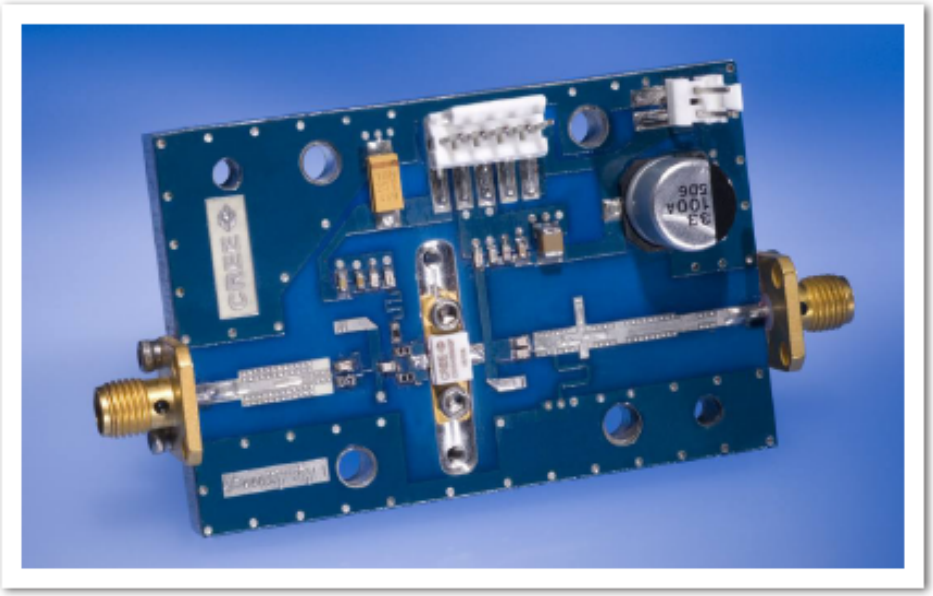
CGH40010-TB Demonstration Amplifier Circuit Bill of Materials

Designator	Description	Qty
R1,R2	RES,1/16W,0603,1%,0 OHMS	1
R3	RES,1/16W,0603,1%,47 OHMS	1
R4	RES,1/16W,0603,1%,100 OHMS	1
C6	CAP, 470PF, 5%,100V, 0603	1
C17	CAP, 33 UF, 20%, G CASE	1
C16	CAP, 1.0UF, 100V, 10%, X7R, 1210	1
C8	CAP 10UF 16V TANTALUM	1
C14	CAP, 100.0pF, +/-5%, 0603	1
C1	CAP, 0.5pF, +/-0.05pF, 0603	1
C2	CAP, 0.7pF, +/-0.1pF, 0603	1
C10,C11	CAP, 1.0pF, +/-0.1pF, 0603	2
C4,C12	CAP, 10.0pF,+/-5%, 0603	2
C5,C13	CAP, 39pF, +/-5%, 0603	2
C7,C15	CAP,33000PF, 0805,100V, X7R	2
J3,J4	CONN SMA STR PANEL JACK RECP	1
J2	HEADER RT>PLZ.1CEN LK 2 POS	1
J1	HEADER RT>PLZ .1CEN LK 5POS	1
-	PCB, RO4350B, Er = 3.48, h = 20 mil	1
Q1	CGH40010F or CGH40010P	1

CGH40010-TB Demonstration Amplifier Circuit



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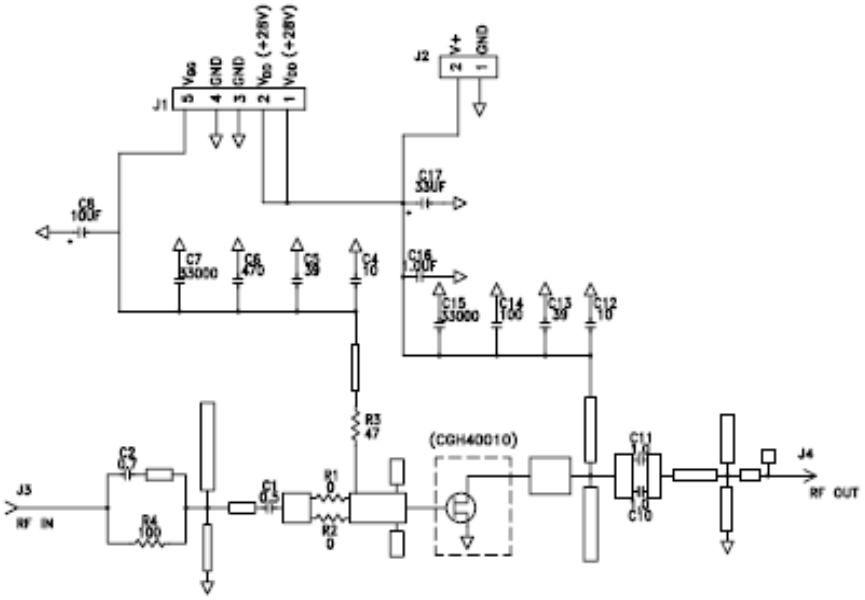
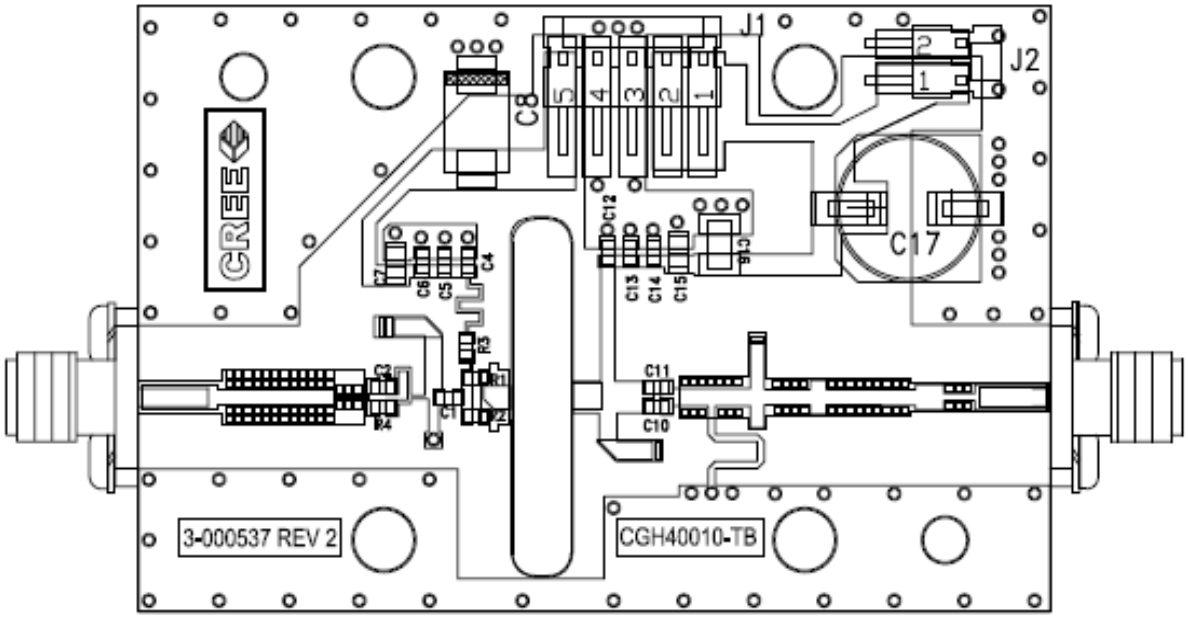
CGH40010-TB Demonstration Amplifier Circuit Schematic



CGH40010-TB Demonstration Amplifier Circuit Outline



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CREE

Typical Package S-Parameters for CGH40010
(Small Signal, V_{DS} = 28 V, I_{DQ} = 100 mA, angle in degrees)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.909	-123.34	17.19	108.22	0.027	21.36	0.343	-90.81
600 MHz	0.902	-133.06	14.86	101.82	0.028	15.60	0.329	-98.65
700 MHz	0.897	-140.73	13.04	96.45	0.028	10.87	0.321	-104.84
800 MHz	0.894	-146.96	11.58	91.78	0.029	6.84	0.317	-109.84
900 MHz	0.891	-152.16	10.41	87.61	0.029	3.33	0.316	-113.95
1.0 GHz	0.890	-156.60	9.43	83.82	0.029	0.19	0.318	-117.42
1.1 GHz	0.889	-160.47	8.62	80.31	0.029	-2.66	0.321	-120.40
1.2 GHz	0.888	-163.90	7.93	77.02	0.029	-5.28	0.326	-123.02
1.3 GHz	0.887	-166.99	7.34	73.90	0.029	-7.72	0.332	-125.36
1.4 GHz	0.887	-169.80	6.82	70.92	0.029	-10.01	0.338	-127.51
1.5 GHz	0.887	-172.39	6.38	68.05	0.029	-12.18	0.345	-129.50
1.6 GHz	0.887	-174.80	5.98	65.28	0.028	-14.24	0.353	-131.37
1.7 GHz	0.887	-177.07	5.63	62.59	0.028	-16.21	0.360	-133.15
1.8 GHz	0.887	-179.22	5.32	59.97	0.028	-18.09	0.369	-134.87
1.9 GHz	0.887	178.73	5.04	57.41	0.028	-19.91	0.377	-136.54
2.0 GHz	0.888	176.76	4.78	54.89	0.027	-21.66	0.385	-138.17
2.1 GHz	0.888	174.86	4.55	52.42	0.027	-23.35	0.393	-139.77
2.2 GHz	0.888	173.02	4.34	49.99	0.027	-24.98	0.402	-141.34
2.3 GHz	0.888	171.23	4.15	47.60	0.026	-26.56	0.410	-142.90
2.4 GHz	0.889	169.48	3.97	45.24	0.026	-28.08	0.418	-144.45
2.5 GHz	0.889	167.76	3.81	42.90	0.026	-29.55	0.426	-145.99
2.6 GHz	0.890	166.07	3.66	40.59	0.025	-30.98	0.434	-147.53
2.7 GHz	0.890	164.39	3.53	38.30	0.025	-32.36	0.442	-149.06
2.8 GHz	0.890	162.74	3.40	36.03	0.025	-33.69	0.450	-150.59
2.9 GHz	0.891	161.10	3.28	33.78	0.024	-34.97	0.458	-152.12
3.0 GHz	0.891	159.46	3.17	31.55	0.024	-36.20	0.465	-153.65
3.2 GHz	0.892	156.21	2.97	27.12	0.023	-38.51	0.479	-156.72
3.4 GHz	0.893	152.96	2.79	22.73	0.022	-40.63	0.493	-159.80
3.6 GHz	0.893	149.69	2.64	18.38	0.022	-42.52	0.505	-162.90
3.8 GHz	0.894	146.38	2.50	14.05	0.021	-44.17	0.517	-166.03
4.0 GHz	0.894	143.03	2.38	9.72	0.020	-45.56	0.527	-169.19
4.2 GHz	0.894	139.61	2.28	5.40	0.019	-46.67	0.537	-172.39
4.4 GHz	0.895	136.11	2.18	1.07	0.019	-47.46	0.546	-175.64
4.6 GHz	0.895	132.53	2.09	-3.29	0.018	-47.90	0.554	-178.95
4.8 GHz	0.895	128.85	2.01	-7.68	0.017	-47.96	0.561	177.69
5.0 GHz	0.895	125.06	1.94	-12.10	0.017	-47.61	0.568	174.25
5.2 GHz	0.895	121.15	1.88	-16.58	0.016	-46.84	0.573	170.72
5.4 GHz	0.895	117.11	1.82	-21.12	0.016	-45.67	0.578	167.10
5.6 GHz	0.895	112.94	1.77	-25.73	0.015	-44.12	0.582	163.38
5.8 GHz	0.895	108.62	1.72	-30.42	0.015	-42.30	0.586	159.54
6.0 GHz	0.895	104.15	1.68	-35.20	0.015	-40.33	0.589	155.56

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Fax: +1.919.869.2733
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Typical Package S-Parameters for CGH40010
(Small Signal, V_{DS} = 28 V, I_{DQ} = 200 mA, angle in degrees)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.911	-130.62	18.41	105.41	0.022	19.44	0.303	-112.24
600 MHz	0.906	-139.65	15.80	99.47	0.023	14.31	0.299	-119.83
700 MHz	0.902	-146.70	13.80	94.50	0.023	10.17	0.298	-125.50
800 MHz	0.899	-152.41	12.22	90.19	0.023	6.68	0.299	-129.85
900 MHz	0.898	-157.17	10.96	86.34	0.024	3.67	0.302	-133.28
1.0 GHz	0.896	-161.24	9.92	82.82	0.024	0.99	0.305	-136.05
1.1 GHz	0.896	-164.79	9.06	79.56	0.024	-1.41	0.309	-138.34
1.2 GHz	0.895	-167.95	8.33	76.49	0.024	-3.62	0.314	-140.30
1.3 GHz	0.895	-170.80	7.70	73.57	0.023	-5.66	0.320	-142.01
1.4 GHz	0.894	-173.41	7.17	70.78	0.023	-7.56	0.326	-143.54
1.5 GHz	0.894	-175.82	6.70	68.08	0.023	-9.35	0.332	-144.94
1.6 GHz	0.894	-178.09	6.28	65.47	0.023	-11.05	0.338	-146.24
1.7 GHz	0.894	179.78	5.92	62.92	0.023	-12.66	0.345	-147.48
1.8 GHz	0.894	177.75	5.59	60.43	0.023	-14.19	0.352	-148.68
1.9 GHz	0.894	175.81	5.30	57.99	0.023	-15.65	0.358	-149.84
2.0 GHz	0.894	173.94	5.04	55.59	0.022	-17.05	0.365	-150.99
2.1 GHz	0.894	172.13	4.80	53.23	0.022	-18.39	0.372	-152.12
2.2 GHz	0.894	170.37	4.58	50.91	0.022	-19.67	0.379	-153.26
2.3 GHz	0.895	168.65	4.38	48.61	0.022	-20.90	0.386	-154.39
2.4 GHz	0.895	166.96	4.20	46.33	0.021	-22.08	0.393	-155.54
2.5 GHz	0.895	165.30	4.03	44.08	0.021	-23.20	0.400	-156.69
2.6 GHz	0.895	163.66	3.88	41.84	0.021	-24.27	0.407	-157.85
2.7 GHz	0.895	162.04	3.74	39.63	0.021	-25.28	0.414	-159.03
2.8 GHz	0.895	160.43	3.60	37.43	0.020	-26.25	0.420	-160.22
2.9 GHz	0.896	158.83	3.48	35.24	0.020	-27.16	0.427	-161.42
3.0 GHz	0.896	157.24	3.37	33.06	0.020	-28.02	0.433	-162.64
3.2 GHz	0.896	154.06	3.16	28.74	0.019	-29.57	0.446	-165.13
3.4 GHz	0.896	150.87	2.98	24.44	0.019	-30.88	0.457	-167.69
3.6 GHz	0.896	147.66	2.82	20.16	0.018	-31.95	0.468	-170.31
3.8 GHz	0.897	144.41	2.68	15.89	0.018	-32.76	0.478	-173.00
4.0 GHz	0.897	141.10	2.56	11.61	0.017	-33.30	0.488	-175.77
4.2 GHz	0.897	137.72	2.45	7.33	0.017	-33.55	0.497	-178.61
4.4 GHz	0.897	134.26	2.35	3.03	0.017	-33.50	0.505	178.47
4.6 GHz	0.897	130.71	2.26	-1.31	0.016	-33.18	0.512	175.46
4.8 GHz	0.896	127.06	2.17	-5.68	0.016	-32.58	0.518	172.36
5.0 GHz	0.896	123.30	2.10	-10.09	0.016	-31.74	0.524	169.16
5.2 GHz	0.896	119.42	2.04	-14.57	0.016	-30.72	0.529	165.86
5.4 GHz	0.896	115.41	1.98	-19.10	0.016	-29.60	0.534	162.44
5.6 GHz	0.896	111.26	1.92	-23.71	0.016	-28.46	0.537	158.89
5.8 GHz	0.895	106.97	1.87	-28.40	0.017	-27.41	0.540	155.20
6.0 GHz	0.895	102.53	1.82	-33.19	0.017	-26.54	0.543	151.36

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Typical Package S-Parameters for CGH40010
(Small Signal, V_{DS} = 28 V, I_{DQ} = 500 mA, angle in degrees)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.914	-135.02	18.58	103.70	0.020	18.36	0.300	-126.80
600 MHz	0.909	-143.57	15.88	98.05	0.020	13.67	0.302	-133.51
700 MHz	0.906	-150.23	13.83	93.33	0.021	9.90	0.304	-138.40
800 MHz	0.904	-155.61	12.23	89.23	0.021	6.77	0.307	-142.08
900 MHz	0.903	-160.09	10.95	85.56	0.021	4.08	0.311	-144.94
1.0 GHz	0.902	-163.93	9.91	82.21	0.021	1.71	0.314	-147.23
1.1 GHz	0.901	-167.29	9.04	79.09	0.021	-0.41	0.319	-149.10
1.2 GHz	0.901	-170.29	8.31	76.15	0.021	-2.35	0.323	-150.69
1.3 GHz	0.900	-173.00	7.69	73.35	0.021	-4.12	0.328	-152.07
1.4 GHz	0.900	-175.50	7.15	70.66	0.021	-5.78	0.333	-153.29
1.5 GHz	0.900	-177.81	6.69	68.07	0.021	-7.32	0.338	-154.41
1.6 GHz	0.900	-179.98	6.27	65.54	0.021	-8.77	0.344	-155.44
1.7 GHz	0.900	177.96	5.91	63.08	0.020	-10.15	0.349	-156.43
1.8 GHz	0.899	176.00	5.59	60.67	0.020	-11.45	0.355	-157.38
1.9 GHz	0.899	174.12	5.30	58.30	0.020	-12.68	0.361	-158.30
2.0 GHz	0.899	172.31	5.04	55.97	0.020	-13.85	0.366	-159.22
2.1 GHz	0.899	170.54	4.80	53.67	0.020	-14.96	0.372	-160.14
2.2 GHz	0.900	168.83	4.58	51.40	0.020	-16.01	0.378	-161.06
2.3 GHz	0.900	167.15	4.39	49.16	0.019	-17.01	0.384	-161.99
2.4 GHz	0.900	165.49	4.21	46.94	0.019	-17.95	0.390	-162.93
2.5 GHz	0.900	163.87	4.04	44.73	0.019	-18.85	0.396	-163.88
2.6 GHz	0.900	162.26	3.89	42.54	0.019	-19.69	0.402	-164.86
2.7 GHz	0.900	160.66	3.75	40.37	0.019	-20.48	0.407	-165.85
2.8 GHz	0.900	159.08	3.62	38.21	0.019	-21.21	0.413	-166.86
2.9 GHz	0.900	157.51	3.50	36.05	0.018	-21.89	0.418	-167.89
3.0 GHz	0.900	155.93	3.39	33.91	0.018	-22.52	0.424	-168.95
3.2 GHz	0.900	152.79	3.18	29.65	0.018	-23.61	0.435	-171.12
3.4 GHz	0.900	149.64	3.00	25.40	0.017	-24.48	0.445	-173.38
3.6 GHz	0.900	146.45	2.85	21.17	0.017	-25.11	0.454	-175.73
3.8 GHz	0.900	143.23	2.71	16.93	0.017	-25.51	0.463	-178.17
4.0 GHz	0.900	139.94	2.58	12.69	0.017	-25.67	0.471	179.30
4.2 GHz	0.900	136.58	2.47	8.43	0.016	-25.60	0.479	176.67
4.4 GHz	0.899	133.14	2.38	4.15	0.016	-25.32	0.486	173.94
4.6 GHz	0.899	129.61	2.29	-0.17	0.016	-24.85	0.492	171.12
4.8 GHz	0.899	125.97	2.21	-4.53	0.016	-24.24	0.498	168.18
5.0 GHz	0.898	122.23	2.13	-8.94	0.016	-23.54	0.503	165.13
5.2 GHz	0.898	118.36	2.07	-13.41	0.016	-22.80	0.507	161.96
5.4 GHz	0.898	114.36	2.01	-17.95	0.017	-22.11	0.511	158.66
5.6 GHz	0.897	110.22	1.95	-22.56	0.017	-21.54	0.514	155.22
5.8 GHz	0.897	105.94	1.90	-27.26	0.018	-21.16	0.517	151.63
6.0 GHz	0.897	101.51	1.86	-32.04	0.019	-21.04	0.519	147.87

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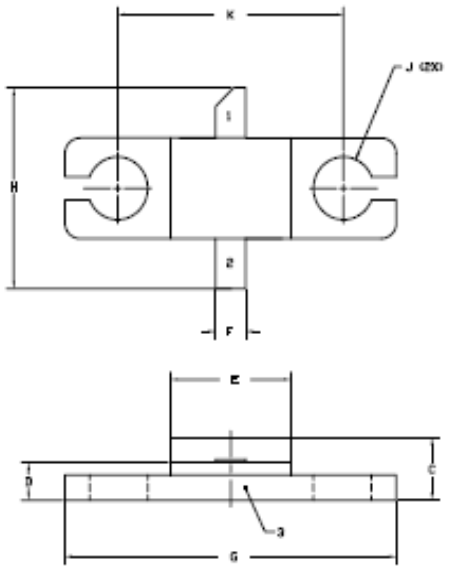
Product Dimensions CGH40010F (Package Type — 440166)



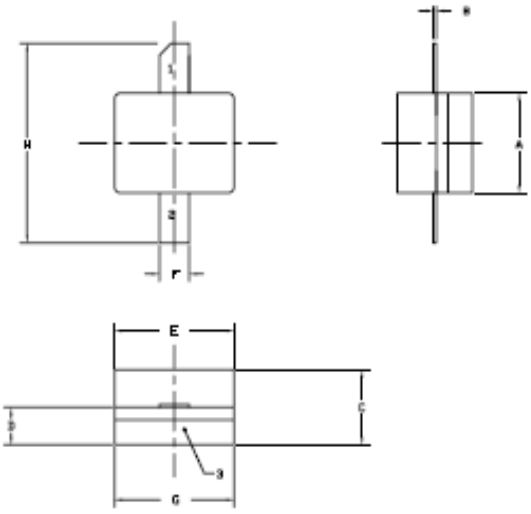
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.005" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.010" IN ANY DIRECTION.
5. ALL PLATED SURFACES ARE NI/AU

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.155	0.165	3.94	4.19
B	0.004	0.006	0.10	0.15
C	0.115	0.135	2.92	3.43
D	0.057	0.067	1.45	1.70
E	0.195	0.205	4.95	5.21
F	0.045	0.055	1.14	1.40
G	0.545	0.555	13.84	14.09
H	0.280	0.360	7.87	8.38
J	# .100		2.54	
K	0.375		9.53	

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE

Product Dimensions CGH40010P (Package Type — 440196)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.005" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.010" IN ANY DIRECTION.
5. ALL PLATED SURFACES ARE NI/AU

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.155	0.165	3.94	4.19
B	0.003	0.006	0.10	0.15
C	0.115	0.135	2.92	3.17
D	0.057	0.067	1.45	1.70
E	0.195	0.205	4.95	5.21
F	0.045	0.055	1.14	1.40
G	0.195	0.205	4.95	5.21
H	0.280	0.360	7.112	9.114

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE

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4600 Silicon Drive
Durham, NC 27703
USA Tel: +1.919.313.5300
Fax: +1.919.869.2733
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For more information, please contact:

Cree, Inc.
4600 Silicon Drive
Durham, NC 27703
www.cree.com/wireless

Ryan Baker
Marketing
Cree, RF Components
919.407.7816

Tom Dekker
Sales Director
Cree, RF Components
919.407.5639

Cree, Inc.
4600 Silicon Drive
Durham, NC 27703
USA Tel: +1.919.313.5300
Fax: +1.919.869.2733
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Appendix C

Continuous Modes Simulation Results Applied on the 10W GaN HEMT Transistor

For the validation of the new broadband Continuous modes based on the different classes and theoretically presented in Chapter 3, simulation analysis using the Agilent ADS (Advanced Design System) on the accurate model for the CGH40010W GaN HEMT (high electron mobility transistor) transistor from CREE [Appendix B] have been performed. Simulations have been conducted at 28 V of supply voltage and two different fundamental frequencies: 0.9 GHz for the Continuous modes applied on the Class-A state and 2.1 GHz for all the other ones. The Figures from C1 to C21 show the different family of voltage and current waveforms exploited at the device intrinsic current-generator plane as well as the different range of fundamental and high harmonic terminations at both the current generator-plane and the package measurement plane. Indeed, for each mode the device output behaviour in terms of power, drain efficiency and gain as well as the input power function of the two parameters δ and ξ is shown.

Continuous Class-AI

The simulation results applied on the 10 W GaN transistor exploiting the Continuous Class-AI mode where varying the current waveform did not deliver the expected performance shown in the theoretical paragraph 3.4 of Chapter 3. Therefore, this mode needs to be investigated more in details and it is thus proposed as future work carrying on the research undertaken in this thesis as discussed in the Future Work of Chapter 7.

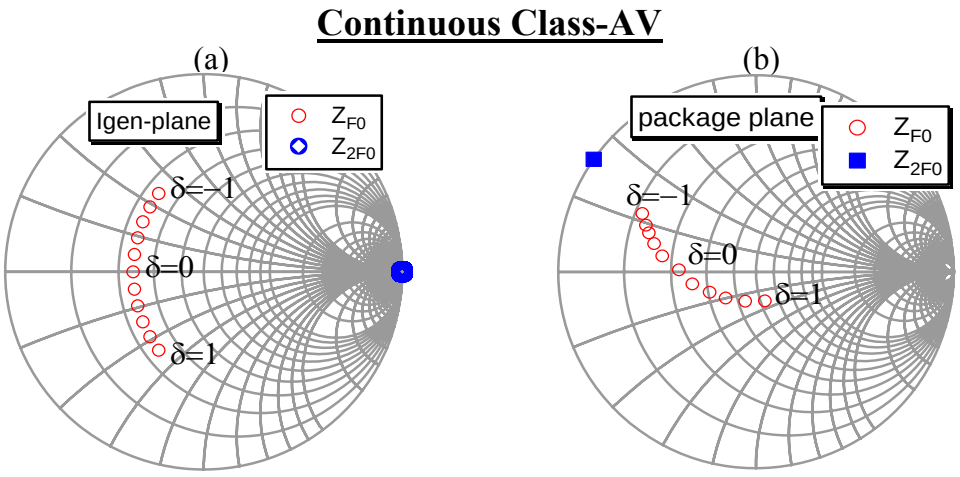

Fig. C1 – Simulated Continuous Class-AV fundamental and second harmonic impedances at both (a) $I_{GEN-PLANE}$ and (b) package plane for δ varying between -1 and 1 in steps of 0.2.

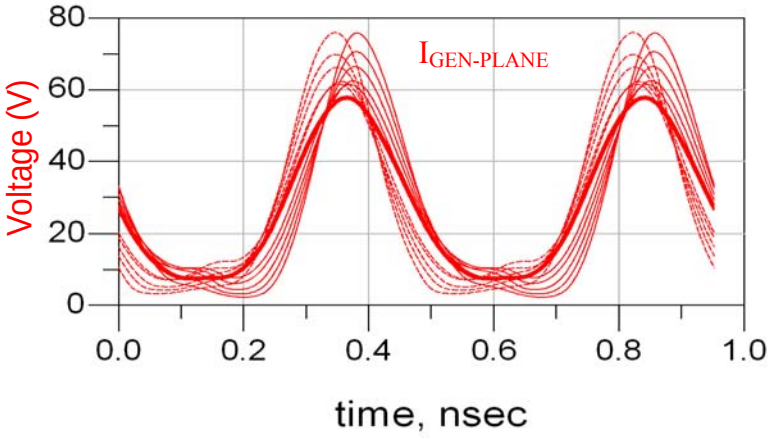

Fig. C2 – Simulated Continuous Class-AV voltage waveforms at the $I_{GEN-PLANE}$ for δ varying between -1 and 1 in steps of 0.2.

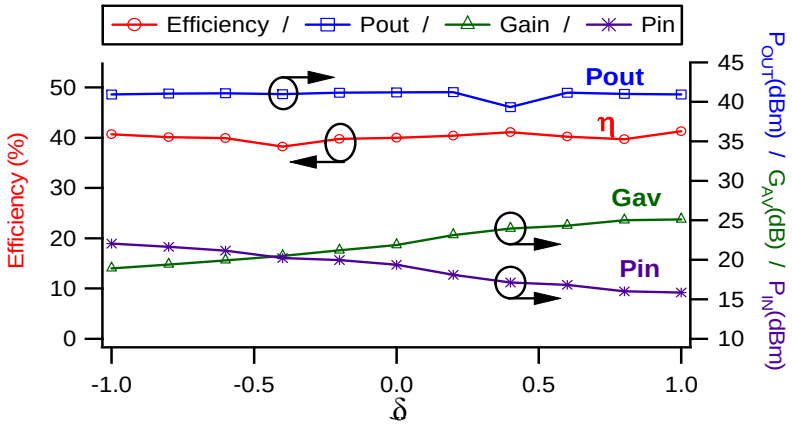

Fig. C3 – Simulated Continuous Class-AV drain efficiency, output power, available gain and input power for δ varying between -1 and 1 in steps of 0.2.

Continuous Class-BV

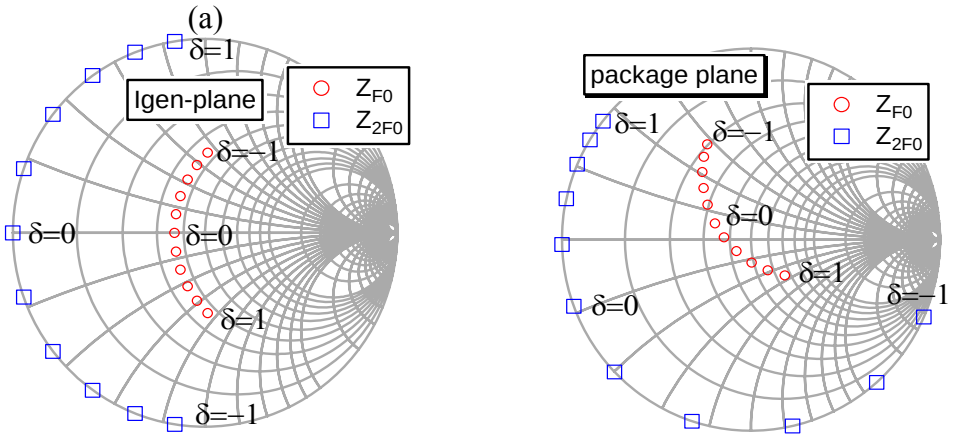

Fig. C4 – Simulated Continuous Class-BV fundamental and second harmonic impedances at both (a) $I_{GEN-PLANE}$ and (b) package plane for δ varying between -1 and 1 in steps of 0.2.

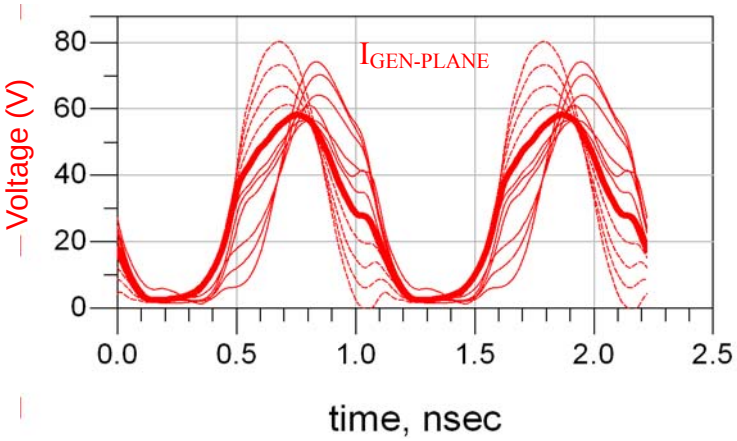

Fig. C5 – Simulated Continuous Class-BV voltage waveforms at the $I_{GEN-PLANE}$ as well as fundamental and second harmonic impedances at the measurement package plane for δ varying between -1 and 1 in steps of 0.2.

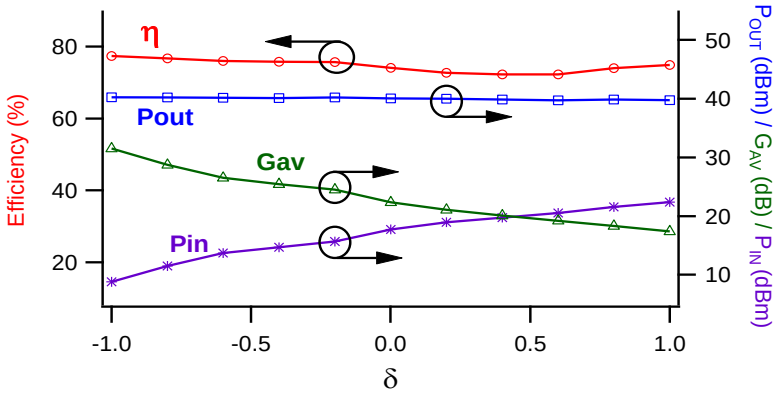

Fig. C6 – Simulated Continuous Class-BV drain efficiency, output power, available gain and input power for δ varying between -1 and 1 in steps of 0.2.

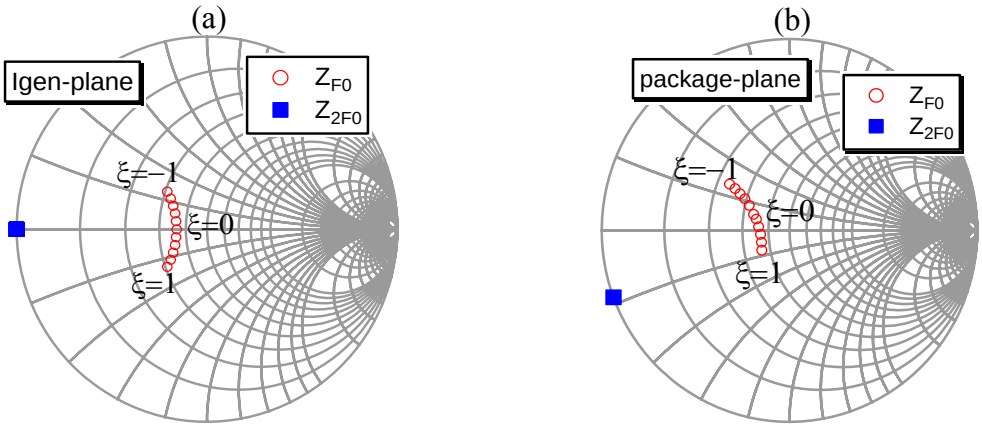

Fig. C7 – Simulated Continuous Class-BI fundamental and second harmonic impedances at both (a) $I_{GEN-PLANE}$ and (b) package plane for ξ varying between -1 and 1 in steps of 0.2.

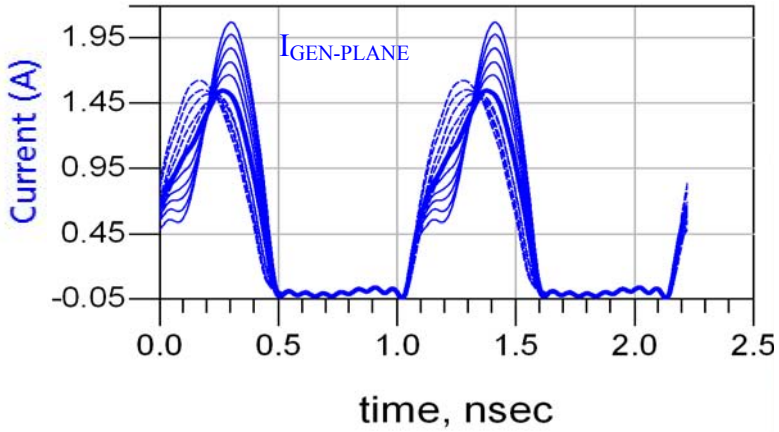

Fig. C8 – Simulated Continuous Class-BI current waveforms at the $I_{GEN-PLANE}$ plane for ξ varying between -1 and 1 in steps of 0.2.

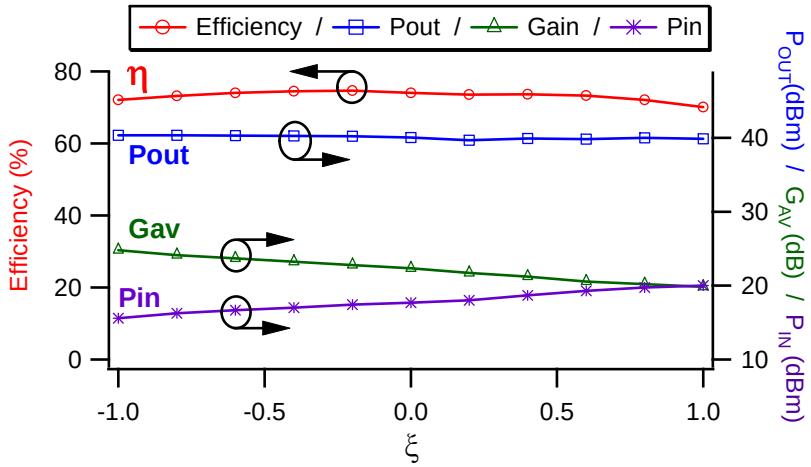

Fig. C9 – Simulated Continuous Class-BI drain efficiency, output power, available gain and input power for ξ varying between -1 and 1 in steps of 0.2.

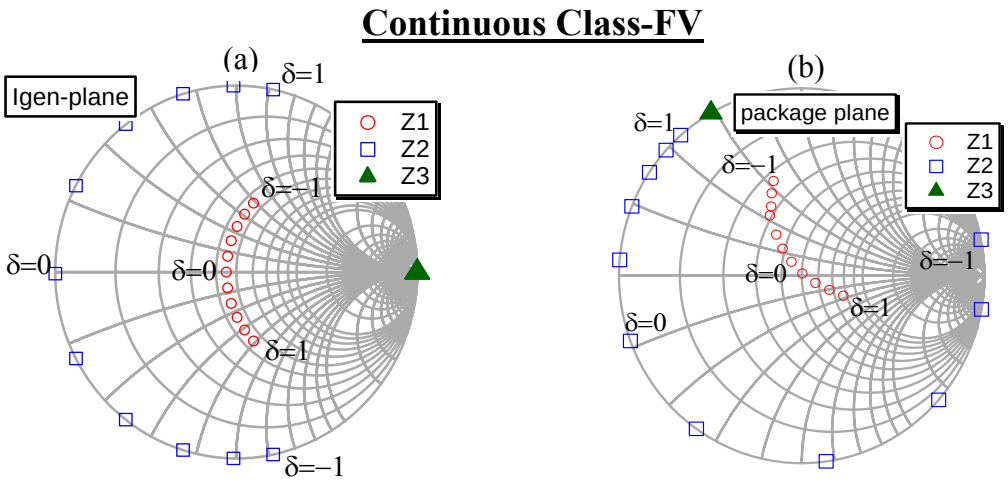

Fig. C10 – Simulated Continuous Class-FV fundamental, second and third harmonic impedances at both (a) $I_{GEN-PLANE}$ and (b) package plane for δ varying between -1 and 1 in steps of 0.2.

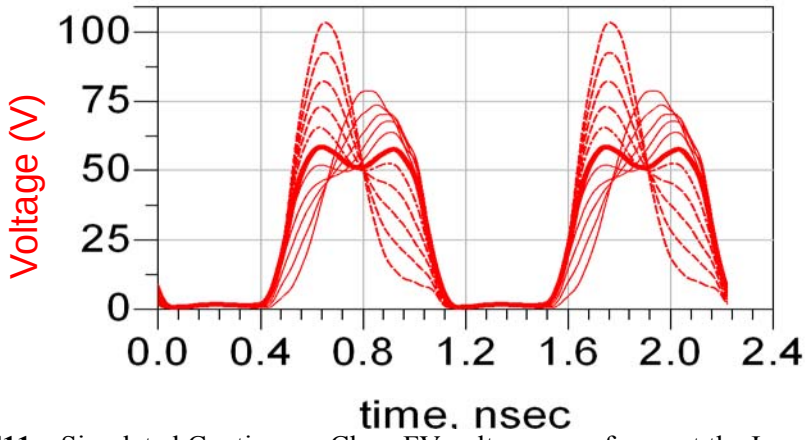

Fig. C11 – Simulated Continuous Class-FV voltage waveforms at the $I_{GEN-PLANE}$ δ varying between -1 and 1 in steps of 0.2.

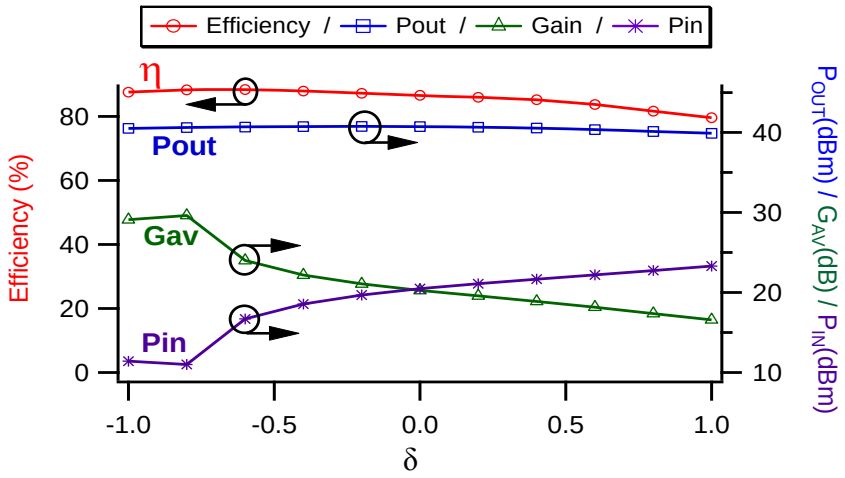

Fig. C12 – Simulated Continuous Class-FV drain efficiency, output power, available gain and input power for δ varying between -1 and 1 in steps of 0.2.

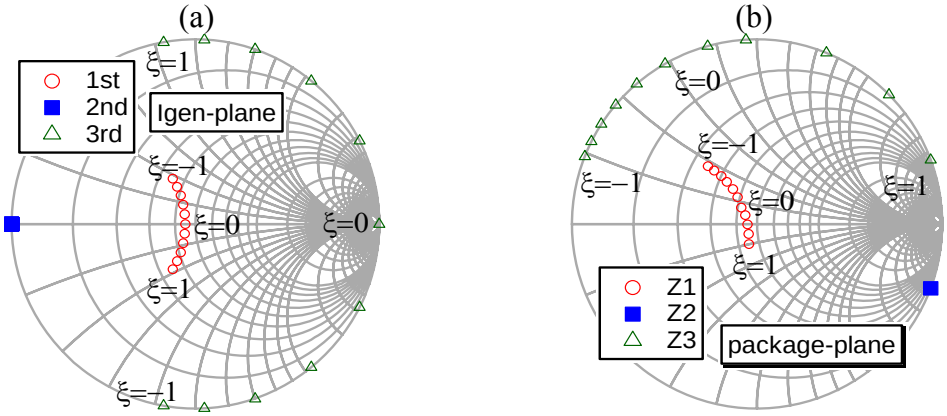

Fig. C13 – Simulated Continuous Class-FI fundamental, second and third harmonic impedances at both (a) $I_{GEN-PLANE}$ and (b) package plane for ξ varying between -1 and 1 in steps of 0.2.

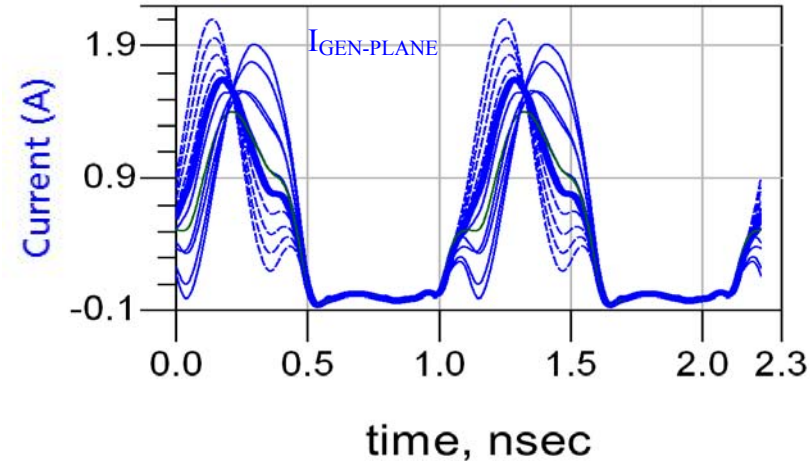

Fig. C14 – Simulated Continuous Class-FI current waveforms at the $I_{GEN-PLANE}$ for ξ varying between -1 and 1 in steps of 0.2.

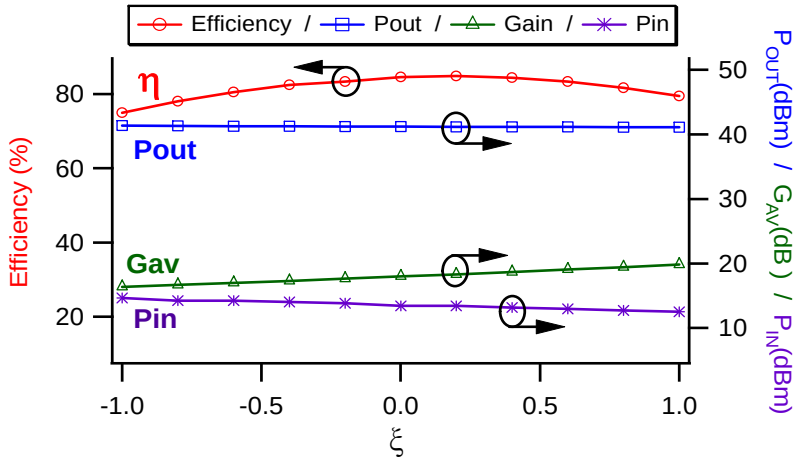

Fig. C15 – Simulated Continuous Class-FI drain efficiency, output power, available gain and input power for ξ varying between -1 and 1 in steps of 0.2.

Continuous Class-FV^{-1}

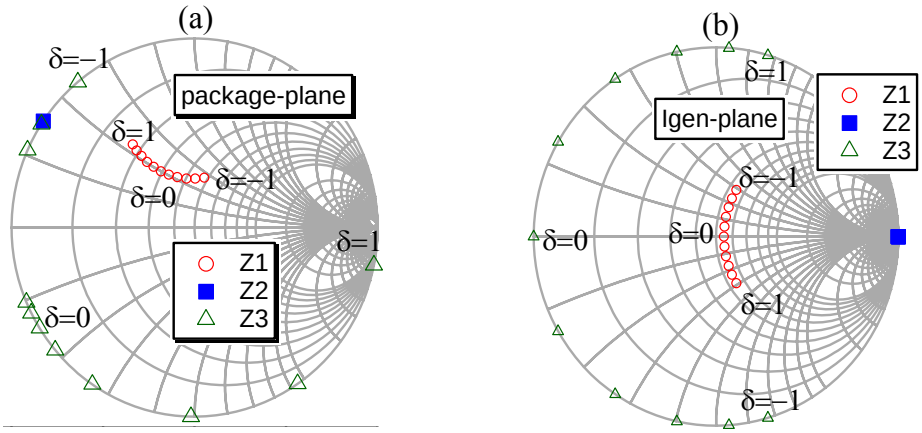

Fig. C16 – Simulated Continuous Class-FV^{-1} fundamental, second and third harmonic impedances at both (a) $I_{GEN-PLANE}$ and (b) package plane for δ varying between -1 and 1 in steps of 0.2.

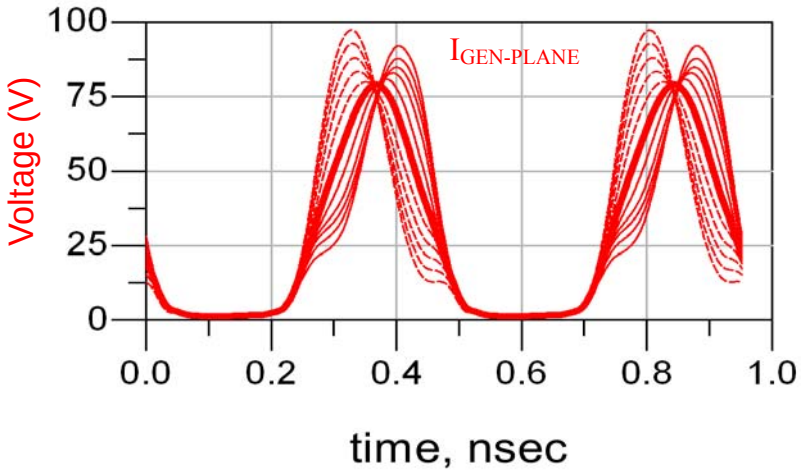

Fig. C17 – Simulated Continuous Class-FV^{-1} voltage waveforms at the $I_{GEN-PLANE}$ as well as fundamental, second and third harmonic impedances at the package plane for δ varying between -1 and 1 in steps of 0.2.

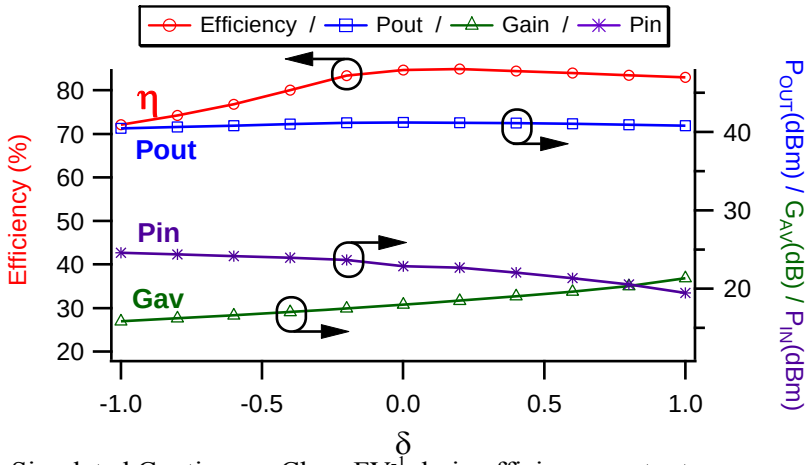

Fig. C18 – Simulated Continuous Class-FV^{-1} drain efficiency, output power, available gain and input power for δ varying between -1 and 1 in steps of 0.2.

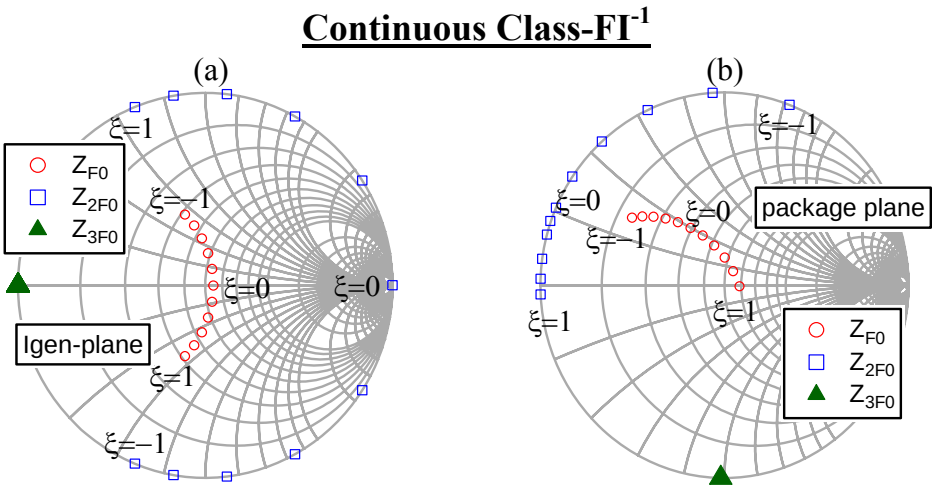

Fig. C19 – Simulated Continuous Class-FI^{-1} fundamental, second and third harmonic impedances at both (a) $I_{GEN-PLANE}$ and (b) package plane for ξ varying between -1 and 1 in steps of 0.2.

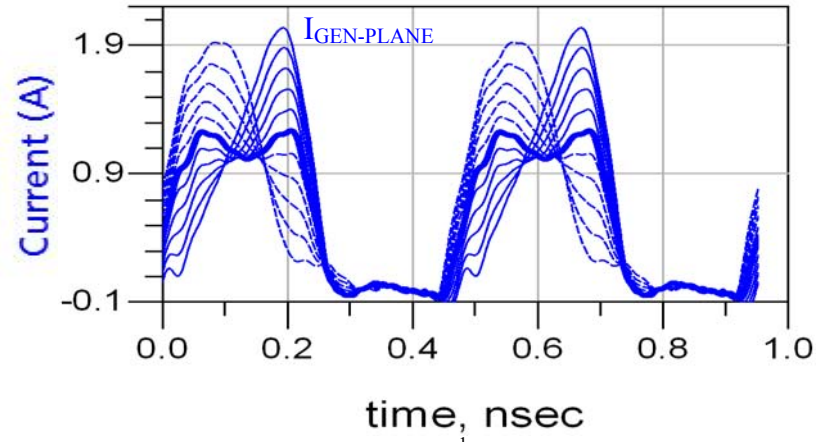

Fig. C20 – Simulated Continuous Class-FI^{-1} current waveforms at the $I_{GEN-PLANE}$ for ξ varying between -1 and 1 in steps of 0.2.

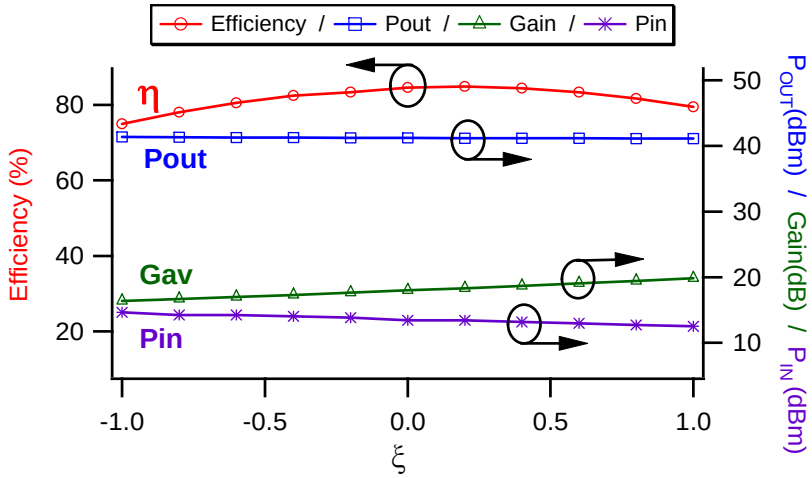

Fig. C21 – Simulated Continuous Class-FI^{-1} drain efficiency, output power, available gain and input power for ξ varying between -1 and 1 in steps of 0.2.

The various simulations applied on the different classes have shown the ability of the Continuous mode approach to provide new waveform solutions on both voltage and current. This means that the new impedance solutions are able to provide an almost constant (or greater than a satisfactory target) output performance in terms of power and drain efficiency. Each mode cannot obviously provide the perfect constant solutions with changing δ or ξ due to practical issues as no perfect de-embedding or no symmetrical device characteristic. However, with the exception of the Continuous Class-AI mode which is proposed for future research, the simulations have shown satisfactory output performance validating the approaches.

Table C.I shows the various ranges output parameters as drain efficiency, output power, gain as well the input power drive function of the different Continuous classes.

All the classes, again with the exception of the Class-AI (not displayed), have delivered the desired performance. The output power was the one expected with average at around 40 dBm as well as the drain efficiency with approximately the Class-A around 40%, Class-B around 70-77%, Class-F around 80-80% and Inverse Class-F at around 72-84%. As it can also be noted, a big variation on the gain is obtained due to the different input power levels provided for the achievement of these modes. This is firstly due to the fact that the input transistor was not matched, therefore varying the parameters δ or ξ different input power levels need to be presented in order to maintain the constant voltage or current waveform. Indeed, the gain variation can be associated to stability considerations. This explains the high gain values greater than 20-25 dB for some classes and δ or ξ points. Stability issues can obviously be overcome when designing the power amplifier input matching network and the proper bias networks.

TABLE C.I
SIMULATED OUTPUT PERFORMANCE FOR THE DIFFERENT CONTINUOUS MODES

Modes	DE (%)	P_{OUT} (dBm)	Gain (dB)	P_{IN} (dBm)
Cont. Class-AV	38.8 – 41.3	39.3 – 41.2	18.9 – 25.1	15.9 – 22
Cont. Class-AI	–	–	–	–
Cont. Class-BV	72.2 – 77.4	39.7 – 40.3	17.4 – 31	8.8 – 22.4
Cont. Class-BI	70.1 – 74.7	39.7 – 40.4	19.9 – 24.8	15.6 – 20
Cont. Class-FV	79.6 – 88.4	39.9 – 40.8	16.6 – 29.6	11 – 23.3
Cont. Class-FI	82.8 – 86.6	40.4 – 40.8	19.4 – 20.8	19.5 – 20.3
Cont. Class-FV^{-1}	72.1 – 84.8	40.5 – 41.2	15.9 – 21.3	19.3 – 24.6
Cont. Class-FI^{-1}	75 – 84.8	41.1 – 41.4	16.4 – 19.9	21.3 – 25

Appendix D

Class-F Measurements on the IAF 6x200 µm transistor

Chapter 5 has shown the validity of the Continuous Class-F3 theory through measurement results applied on the 6x200 µm width transistor from the Fraunhofer Institute (IAF). However, before the Continuous Mode where varying the first three harmonic terminations can be applied, the device must initially be optimised in standard Class-F. This means that the various parameters (presented in Chapter 4 and 5 in a different transistor) as input bias, input power and fundamental and harmonic impedances must properly be varied going through the pseudo-ClassB, ClassB and finally the ClassF state.

Specifics:

- Investigation type: Class-F
- F_0 = 1 GHz
- V_{DC} = 28 V
- Wg = 6 x 200 µm = 1.2 mm
- Lg = 0.25 µm
- I_{DSS} = 900 mA/mm

DCIV:

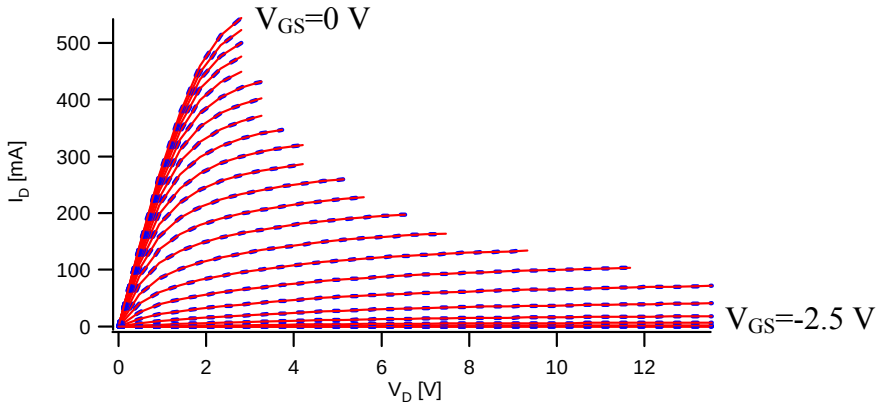

Fig. D1 – DCIV for V_{GS} from -2.5 V to 0 V in steps of 0.1 V.

- The device pinch-off has been found at V_{GS}=-2.4 V

Identification Pseudo-ClassB point:

For V_{GS}=-2.4 V and impedances greater than two short-circuited the fundamental impedance was swept for different drive power levels.

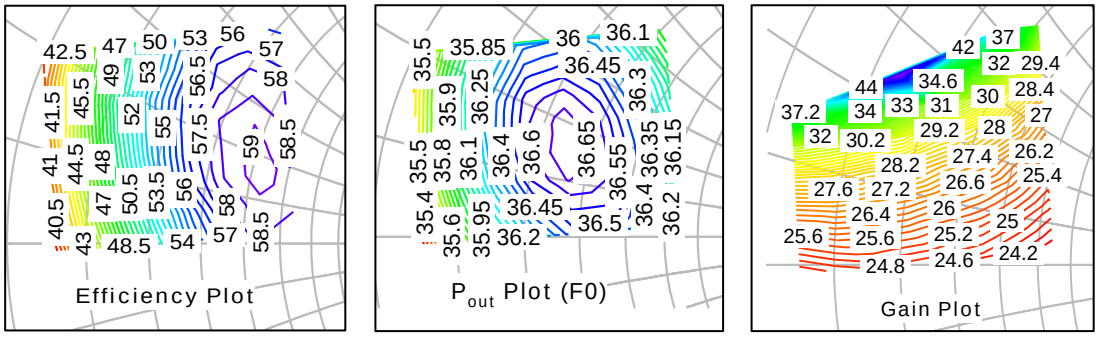

Fig. D2 – Load-pull contour for Efficiency, P_{OUT} and Gain.

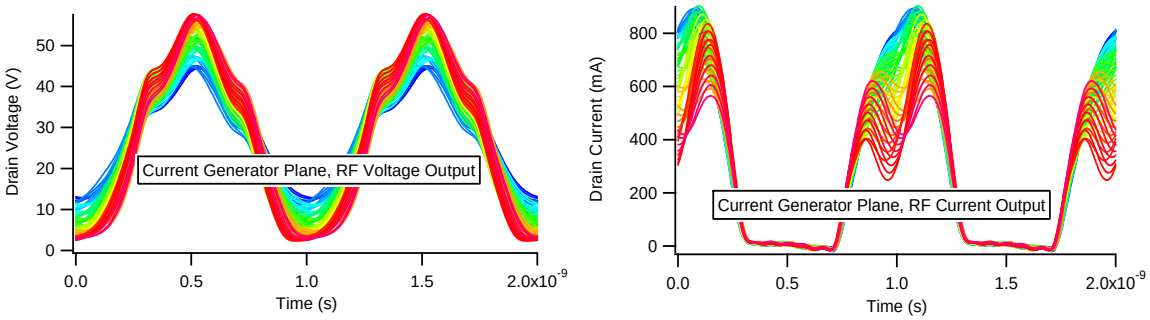

Fig. D3 – Pseudo-ClassB voltage and current waveform at the $I_{GEN\text{-}Plane}$.

Table D.I

	Γ	Z (Ω)	Y (S)	I_{DC} (A)
η_{max} = 59%	0.21 ∠27.5°	71.9+j15	0.013-j2.78*10^{-3}	0.2924
P_{max}=36.7dBm	0.14 ∠61.7°	55.46+j14.7	0.016-j4.46*10^{-3}	0.2655

- In this case a trade-off value of Z_{F0} = 0.18 ∠20° has been chosen.

Therefore:

V_{DC}= 28 V
V_{GS} = -2.4 V
Z_{F0} = 0.18 ∠ 20°
Zn = 0 for n > 1

→

Eff. = 58.5%
P_{OUT} = 36.5 dBm
Gain = 25 dB

Identification Class-B point:

The next step is to optimise the bias point to correctly engineer the drain current waveform. Here, presenting the fundamental impedance of the pseudo-ClassB point and again leaving short-circuit the high harmonic terminations, the input power and input bias point have been varied. Fig. D4 shows the contour plot with the measured third harmonic current as well as drain efficiency, P_{OUT} and gain Vs. the available input power.

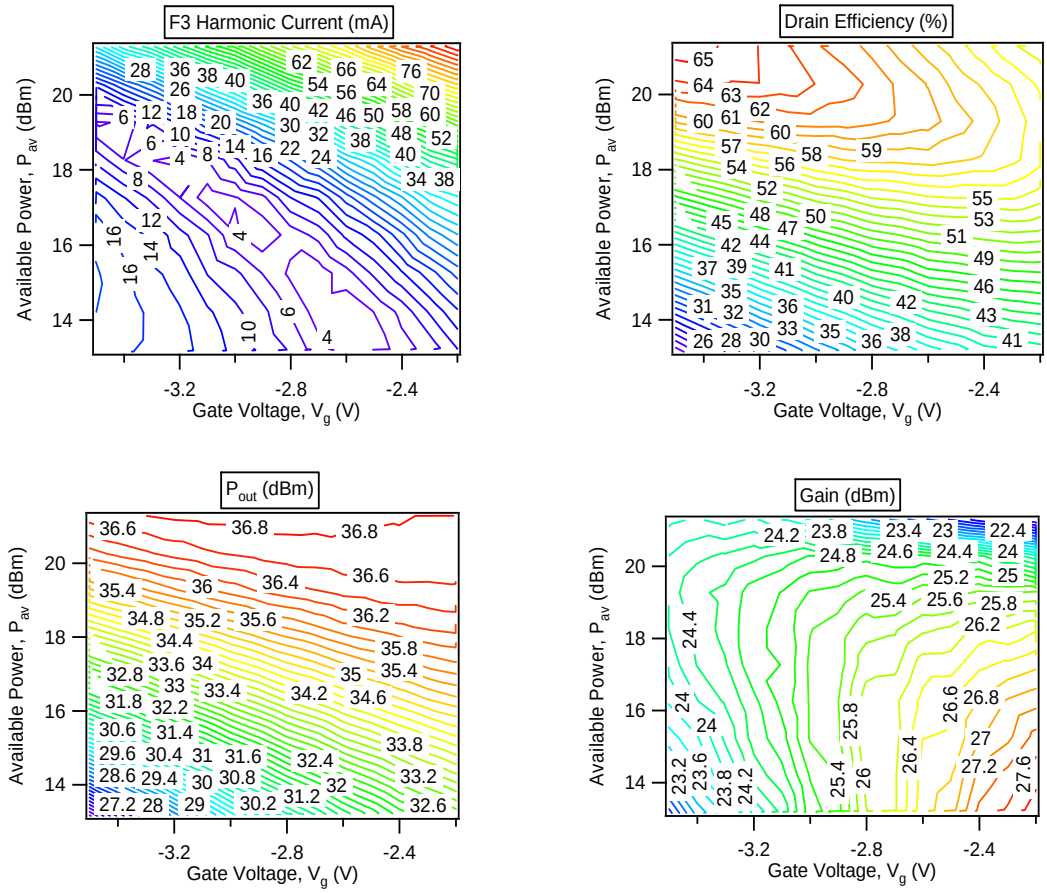

Fig. D4 – Load-pull contour plot showing: 3rd harmonic current magnitude, drain efficiency, output power and gain.

The trade-off between bias voltage and available input power for which small third harmonic content as well as high efficiency, output power and gain are revealed is V_{GS}=-3.1 V and P_{AVS}=20.1 dBm.

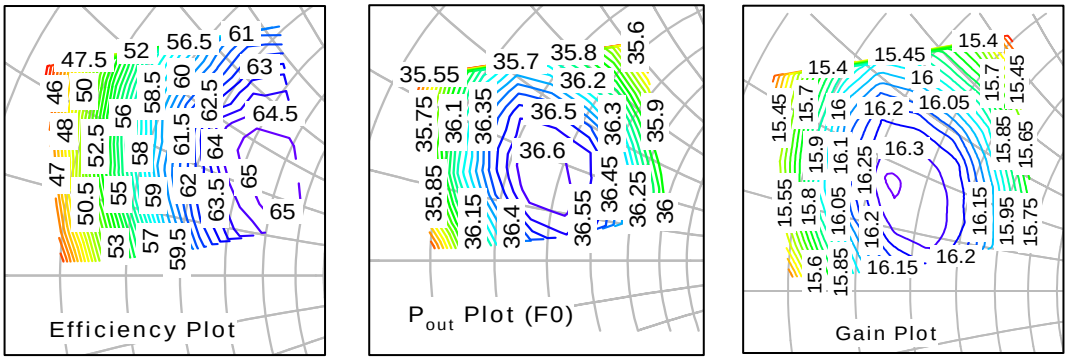

Fig. D5 – Load-pull contour plot showing: drain efficiency, output power and gain.

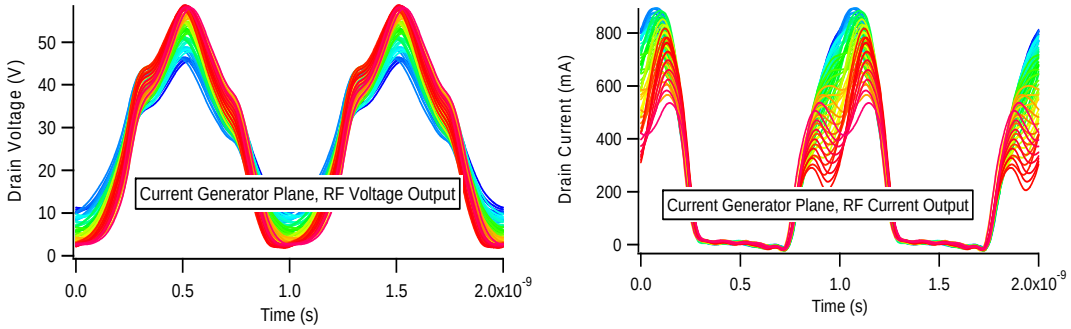

Fig. D6 – Class-B voltage and current waveform at the $I_{GEN\text{-}Plane}$.

Table D.II

	Γ	**Z (Ω)**	**Y (S)**	**I_{DC} (A)**
η_{max} = 64%	0.31 ∠20.77°	87.5+j121.3	0.01-j2.62*10^{-3}	0.21824
P_{max}=35.8dBm	0.16 ∠72.6°	52.63+j17.24	0.017-j5.62*10^{-3}	0.2744

- In this case a trade-off value of Z_{F0} = 0.17 ∠30.5° has been chosen.

Therefore:

V_{DC}= 28 V
V_{GS} = -3.1 V
P_{AVS}=20.2 dBm
Z_{F0} = 0.17 ∠ 30.5°
Zn = 0 for n > 1

→

Eff. = 58.5%
P_{OUT} = 36.5 dBm
Gain = 25 dB

Identification Class-F point:

The Class-B mode presents a half-wave rectified sinusoidal current waveform and a sinusoidal voltage waveform. In order to square the voltage waveform for the achievement of the Class-F mode, the third harmonic load, Z_{3F0}, has to be set to an open-circuit. Taking into account the drain-source capacitor C_{DS} of this device, which has been found to be $\mathbf{C_{DS} = 0.45pF}$, shows that the current generator-plane will rotate to the measurement-plane into the upper-hemisphere of the Smith chart.

Through sweeping the third harmonic phase from -90° to 90° around the open-edge of the Smith chart it was found that the actual optimal load was $\mathbf{Z_{3F0} \approx 1 \angle 55^o}$. The second harmonic impedance was swept around the short-edge of the Smith chart and the optimum value was actually $\mathbf{Z_{2F0} = 1 \angle 180^o}$ (ideal short-circuit)

Once the optimum higher harmonic terminations have been identified, to reach the maximum swing voltage, the fundamental impedance must be increased by around $2/\sqrt{3}$. In this case optimum trade-off of Eff, P_{OUT} and Gain was found for which fundamental impedance is $\mathbf{Z_{F0} = 0.42 \angle 28°}$.

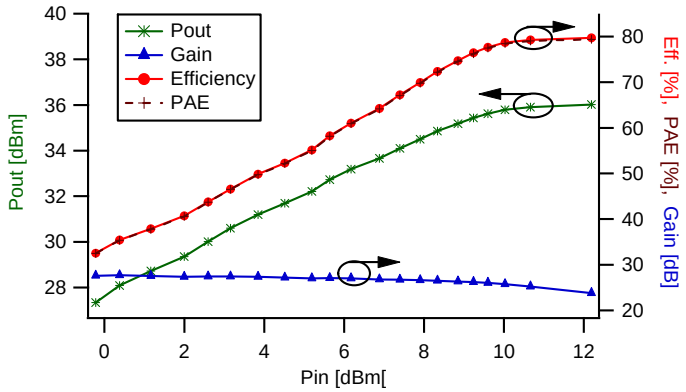

Fig. D7 - Output parameters and measured drain efficiency, PAE, otuput power and gain Vs. input power.

Therefore:

Final Class-F performance:

Z_{F0}= 0.42 ∠ 28°
Z_{2F0}=1∠ 180(short)
Z_{3F0}=1 ∠ 55.5°
Zn = 0 for n > 3
V_{GS} = -3.1 V
V_{DS} = 28 V
C_{DS} = 0.45 pF

P_{OUT}= 36 dBm
Gain = 23.8 dB
Drain Eff.=79.7%
PAE=79.35%

Below are reported the Class-F load-lines and output voltage and current waveforms at both the measurement and intrinsic device plane:

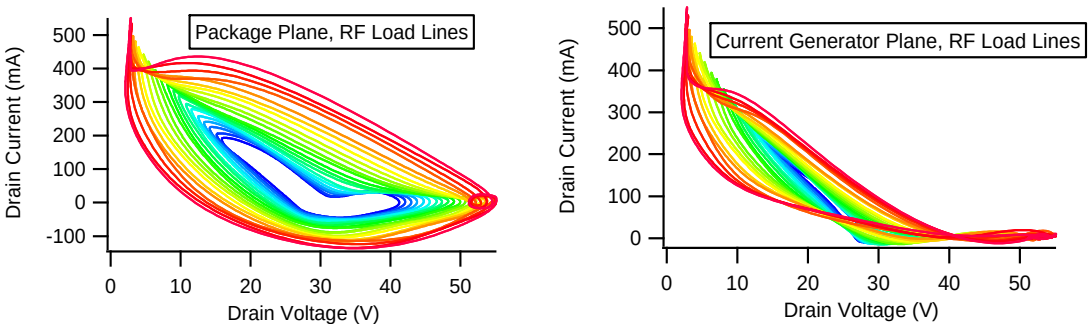

Fig. D8 - load-line at the package measurement and intrinsic device plane.

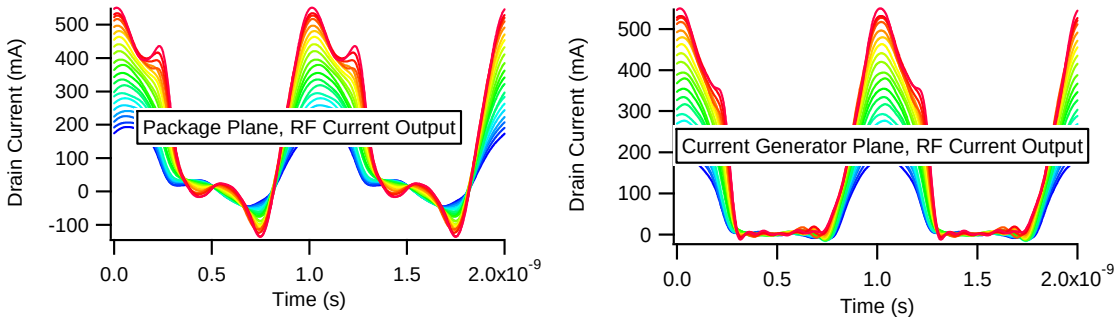

Fig. D9 - Current waveforms at the package measurement and intrinsic device plane.

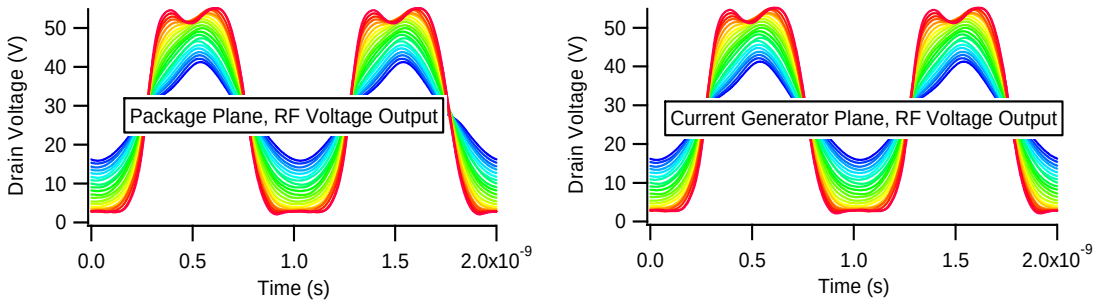

Fig. D10 - Voltage waveforms at the package measurement and intrinsic device plane.

Appendix E

Predictor Waveform Engineering Software Panels

Fig. E1 shows the panel of the Igor predictor software used for the achievement of the initial parameters: bias, fundamental and harmonic output impedances in order to speed-up the measurement activity. This panel is referred to the intrinsic device plane.

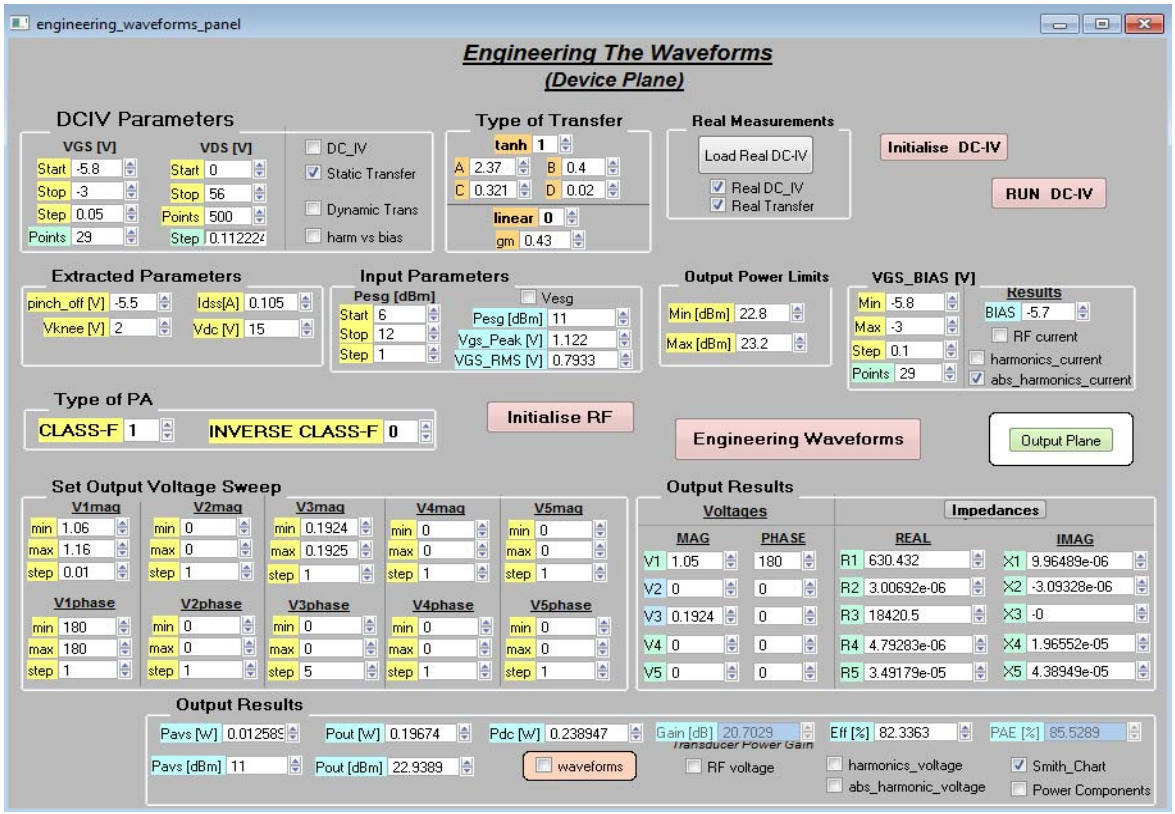

Fig. E1 – Predictor software panel screenshot – at the intrinsic device plane.

In the yellow boxes the appropriate parameters must be set by the user, then running the predictor software the blue boxes return the predicted values.

- ***Initialise DC-IV button***: this button initialise the DCIV predicted characteristic.
- ***Run DC-IV button****:* this button run the DCIV.
- ***DCIV Parameters***: here the input (V_{GS}) and output (V_{DS}) bias point ranges can be set.
- ***Type of Transfer***: here the different transfer characteristic can be chosen. If using the linear function switch the linear box to 1 and the tanzh box to 0 and chose the gm value. Vice-versa, for the tanh function chose the appropriate value (A, B, C and D) that describe such characteristic. For both linear and tanh characteristic the values of gm, A, B, C and D can be chosen by fitting the transfer predicted characteristic to the measured one which can be uploaded with the "*Real Measurement*" button.
- ***Extracted Parameters***: here must be uploaded the measured DC values of V_{TH}, V_{DS}, V_{KNEE} and I_{DSS}.
- ***Input Parameters***: here chose a range of input power. The predictor will return (in the blue boxes) the values of the input voltage.
- ***Output power limits***: set here the appropriate output power limits. It is important to highlight that if the range is too wide compared with the optimum expected the predictor could converge towards very low power for which the efficiency is maximised.
- ***VGS Bias***: here the input bias range can be set. The blue box will return the predicted bias point.
- ***Type of PA***: select the class-F of class-F^{-1} PA mode.
- ***Initialise RF button***: this button initialise the RF performance.
- ***Set output voltage sweep***: here fundamental and harmonics (up to the 5^{th}) voltage contents range in terms of magnitude and phase can be set. Such contents are normalised to the DC voltage.
- ***Output results***: here it is shown the output voltage and impedance values (again up to the 5^{th} harmonic). Furthermore the output performance in terms of power, drain efficiency, DC power and input available power P_{AVS} are shown. Indeed by clicking the appropriate boxes it can be shown the figures with the predicted: voltage and current waveforms, Smith chart and spectrum voltage and current harmonic.
- ***Engineering Waveforms button***: this button runs the RF predicted performance sweeping the whole parameters.
- ***The output plane button*** opens the window shown in Fig. E2.

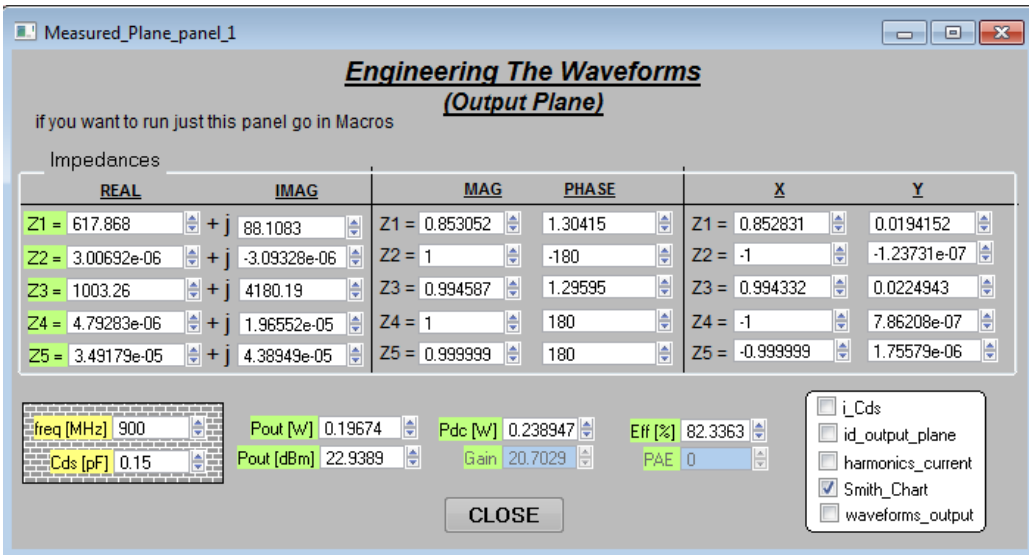

Fig. E2 – Panel at the measured device plane.

As said in Chapter 4, this software can be applied for transistor on-wafer. This means that the only the drain source capacitor needs to be de-embedded. The panel in Fig. E2 shows the first 5 harmonic impedances at the intrinsic device current generator plane. Such impedances can be obtained by setting the drain-source capacitor and the operating fundamental frequency.

Appendix F

Continuous Class-F ADS Schematic

INPUT SIDE:

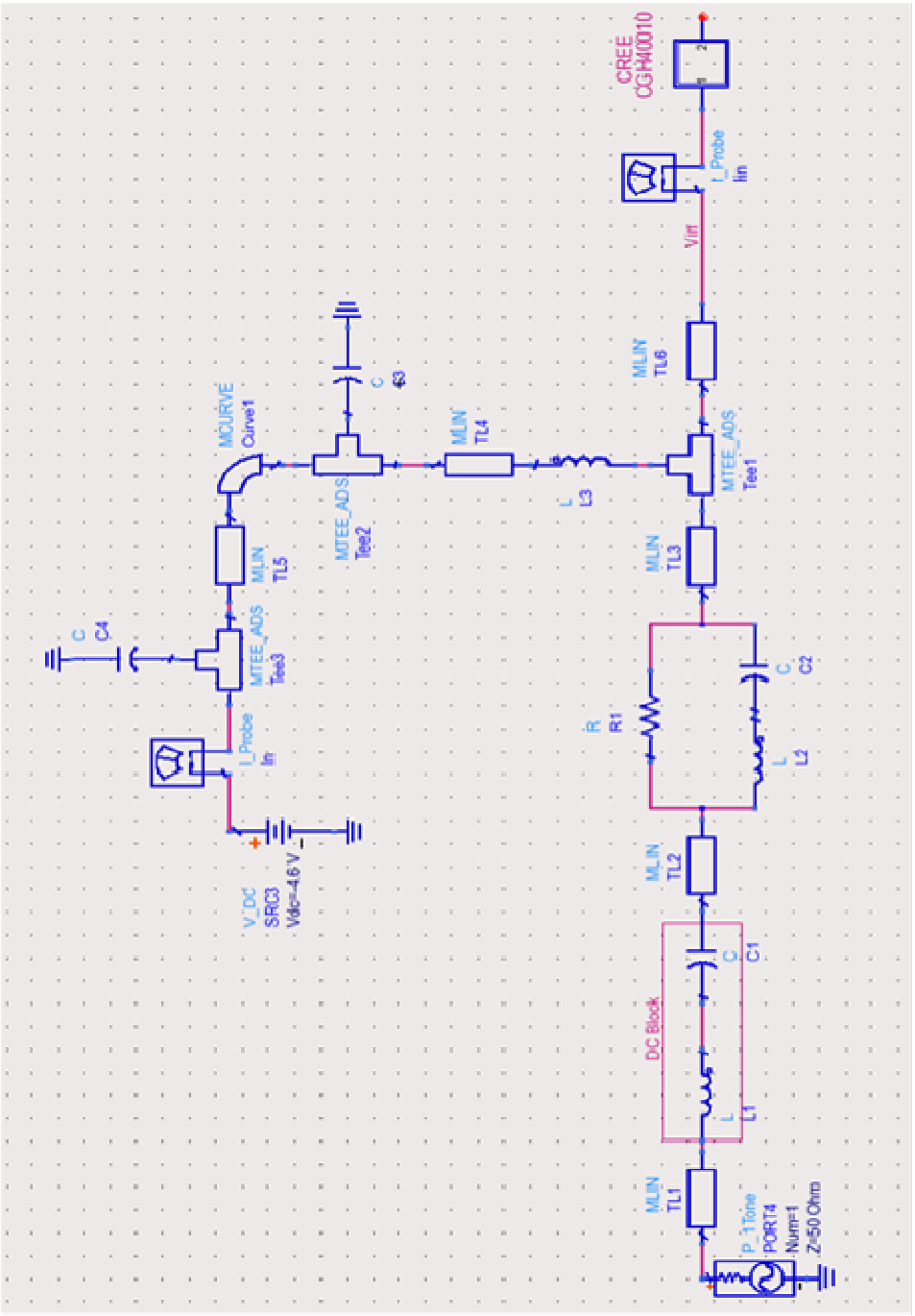

Fig. F1 - Schematic – Input side

OUTPUT SIDE:

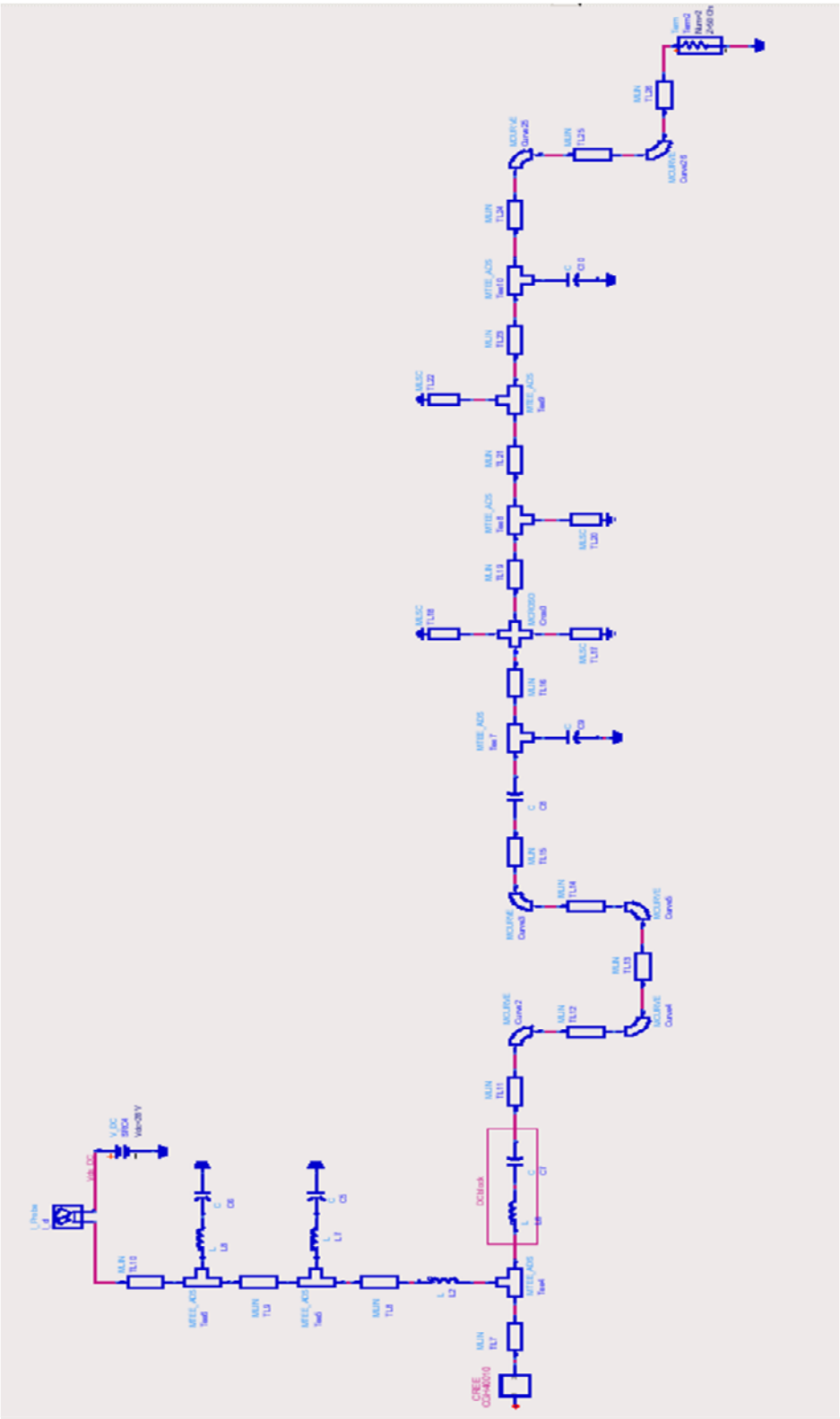

Fig. F2 - Schematic – Output side.

Publication 1.

Title:

The Continuous Class-F Mode Power Amplifier

Authors:

V. Carrubba, A. L. Clarke, M. Akmal, J. Lees, J. Benedikt. P. J. Tasker, S. C. Cripps.

Conference:

IEEE European Microwave Conference (EuMC), pp. 432-435, September 2010.

The Continuous Class-F Mode Power Amplifier

V. Carrubba, A. L. Clarke, M. Akmal, J. Lees, J. Benedikt, P. J. Tasker, S. C. Cripps

Cardiff School of Engineering, Cardiff University, Cardiff, CF24 3AA, United Kingdom

carrubbav@cardiff.ac.uk

Abstract — **This paper presents, for the first time the theoretical introduction and experimental validation of the "Continuous Class-F Mode Power Amplifier" that provides for a new design space for the design of high efficiency and broadband power amplifiers. Starting from the standard class-F mode, this work shows that it is possible to maintain constant or even improved output power and efficiency for coupled variations of fundamental and second harmonic impedances. The investigation was carried out on GaAs pHEMT devices and demonstrates that a near constant efficiency between 82% and 87% can be achieved along with a constant output power of 20dBm, over a wide range of fundamental and second harmonic loads.**

I. Introduction

There is now a great demand on power amplifier (PA) designers to improve efficiency and linearity over increasingly broad frequency ranges without significantly sacrificing output power levels. The challenge in designing harmonically tuned PA modes such as class-F and inverse class-F [1],[2] is to maintain the required short and open circuit harmonic terminations, which due to practical constrains must be placed at a distance from the device, and generally limit achievable relative bandwidths. However, recent publications [3],[4] have shown a theoretical formulation for the voltage waveforms in RF power amplifiers (RFPAs) and introduce new PA modes that maintain a constant and high efficiency over a continuous range of fundamental and second harmonic impedances. The results presented to date have demonstrated a continuous set of waveforms unifying the class-B and class-J modes of operation, allowing more flexibility in PA design. This work builds on this new theoretical formulation and extends it, for the first time, to the class-F PA mode of operation. The new "continuous class-F mode PA" shows that there are many more useful solutions that guarantee the same or even higher output power and efficiency of around 85%.

The time-domain waveform measurement system used in these measurements for the validation of the continuous class-F mode is based on the Microwave Transition Analyzer (MTA). The MTA allows input and output waveforms to be sampled. A sweeper in the source provides the necessary input power to drive the device at the fundamental frequency. An active harmonic envelope load-pull (ELP) system [5] is used to present the requested three harmonic impedances which is necessary for a wide range of measurements where harmonic impedances are continuously varied.

II. Conventional Class-F PA Design

The ideal class-F power amplifier mode requires a square voltage waveform and a half-rectified current waveform at its output current-generator plane [6]. These waveforms are typically described by the following equations [7]:

$$v_D(\vartheta) = V_{DC} + V_1\cos(\vartheta) + V_3\cos(3\vartheta) + V_5\cos(5\vartheta) + ,..... \quad (1)$$

$$i_D(\vartheta) = I_{DC} - I_1\sin(\vartheta) - I_2\cos(2\vartheta) - I_4\cos(4\vartheta) + ,..... \quad (2)$$

Assuming a spectral content that includes an infinite number of harmonics an efficiency of 100% can be achieved. When reducing the number of utilized harmonics to three, the maximum efficiency reduces to 90.7% [1]. It is important to note however that in practice the current waveform is not limited to three harmonic components, hence the replication of such truncated modes requires higher harmonics to be short-circuited. The key in achieving such high efficiencies is that the presence of higher harmonics that allow for an increase in the fundamental voltage.

In practical PA design, the current waveform is obtained through a suitable DC bias of the device, typically around the ideal class-B point of operation. The correct output voltage waveform is then obtained using an output filter generating odd-harmonic voltage components at the current-generator plane. This implementation requires the even harmonics to be shorted to prevent the harmonic content of the current waveform being imposed on that of the voltage. This requirement presents a significant design challenge as any shunt resonator can be placed only at the extrinsic plane of the transistor.

III. The Theoretical Continuous Class-F Mode

Through investigations into this new power amplifier mode, it becomes clear that when working with a constant open third harmonic impedance, a shorted second harmonic component is not a unique solution for achieving maximum efficiency and output power. The required voltage waveforms are defined by the equation (3), which has been derived from the generic factorial representation of voltage waveforms as defined by Cripps [4].

$$v(\vartheta) = \left(1 - \frac{2}{\sqrt{3}}\cos\vartheta\right)^2 \cdot \left(1 + \frac{1}{\sqrt{3}}\cos\vartheta\right) \cdot (1 - \gamma\sin\vartheta), \quad (3)$$

where γ is an empirical parameter, which is swept over the range $-1 \le \gamma \le 1$ in order to sustain a positive voltage for all angles. If that voltage waveform crosses zero at any point, the device current will drop immediately to zero resulting in a drastic reduction of power and efficiency and highly non-linear behaviour. This new family of voltage waveforms, derived from (3), is shown in Fig. 1.

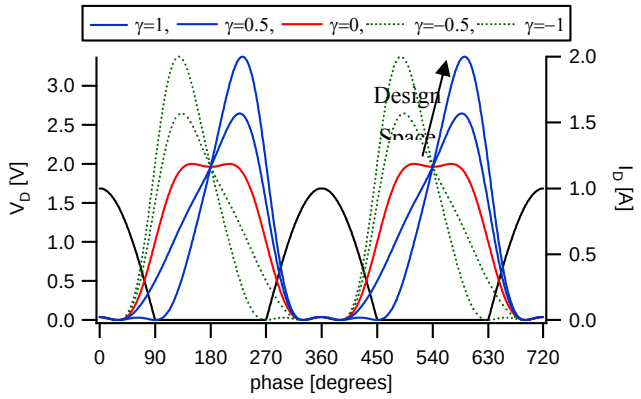

Fig. 1 Continuous class-F current waveform (black line) and voltage waveforms for $-1 \le \gamma \le 1$ with steps of 0.5.

For $\gamma = 0$, the standard class-F voltage waveform is achieved with a theoretical drain efficiency of 90.7%. For all other values of γ, the new voltage waveforms still maintain the standard class-F power and efficiency performance. Throughout the complete waveform set the current waveform (black line) is maintained as a constant half-rectified sinusoid.

The key to engineering this new PA mode lies in changing the reactive component of the fundamental load whilst varying the phase of the second harmonic impedance, in accordance with (3). In this way, it is possible to keep the voltage waveform above zero and maintain a constant, high efficiency state. The required impedances are shown in Fig. 2 with γ changing from -1 to 1 generating second harmonic reactance that vary around the edge of the smith chart, while the fundamental harmonic impedance simultaneously varies on a circle of constant resistance.

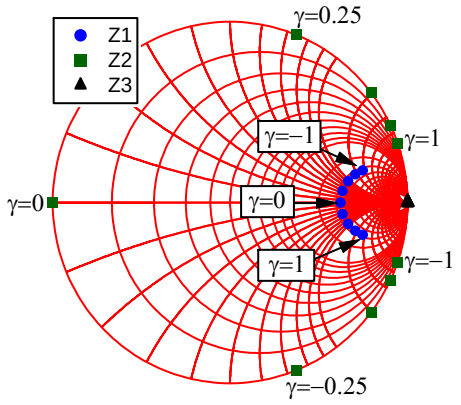

Fig. 2 Continuous class-F impedance range for the first three harmonic impedances when varying $-1 \le \gamma \le 1$ with steps of 0.25.

This collection of valid loads represents a new "design space" which allows increased flexibility in PA design. In this space different values of fundamental and second harmonic impedances can be chosen to maintain the same theoretical output power and efficiency. The important aspect to highlight is that PA designers do not necessary need to provide a short second harmonic impedance in an actual PA design, but have a choice of a significantly wider design space over which optimum device performance is maintained.

Fig. 3 shows the reactive part of the fundamental and second harmonic impedances, normalized to the fundamental resistance R1, against the empiric parameter γ. It can be seen that when increasing γ, the second harmonic reactance increases whilst the fundamental reactance decreases.

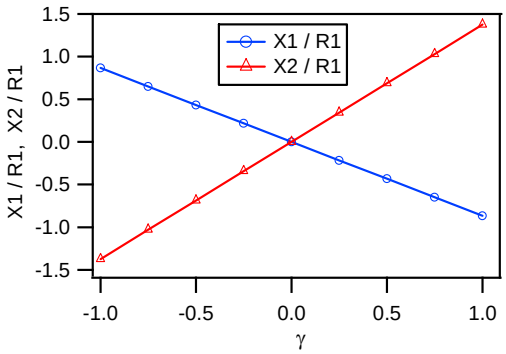

Fig. 3 Theoretical fundamental and second harmonic reactive impedances (X1 and X2) as a function of γ, for $-1 \le \gamma \le 1$ with steps of 0.25.

For $\gamma = 0$ with X1/R1=X2/R1=0, the standard class-F mode is obtained. For all other values of γ, a change of X1 must be accompanied by a negative change of X2 to maintain constant output power and efficiency.

IV. Experimental Verification

The design space defined theoretically in the previous section has been explored experimentally using the ELP active load-pull system developed at Cardiff University [5]. The measurement system allows voltage and current waveforms to be measured at the extrinsic device plane and then shifted to the output generator plane by de-embedding the drain-source capacitor C_{DS} [8]. The measurements have been conducted on-wafer on a power transistor at 0.9GHz, 6V of drain voltage and delivering 20dBm of output power.

A. Using the Class-F mode as starting point for the Continuous Class-F

Before the new PA mode can be explored, the class-F condition must initially be achieved [9]. In a first step a value for the bias voltage (V_G) is selected for which the third harmonic current is minimized. This condition produces the half-rectified sinusoid current waveform required. Once the current waveform is established, the desired class-B fundamental load is determined with higher harmonic impedances being short-circuited. To move toward the class-F mode, harmonic load-pull is employed to engineer the voltage waveform. Here, the second harmonic impedance is kept at a short whilst the third harmonic impedance is open-circuited. In the final step the fundamental impedance is scaled by $4/\pi$ to increase the fundamental voltage component and therefore regain the minimum voltage value of the squared waveform that is comparable to the original class-B mode. The scaling of the fundamental load also restores the fundamental current swing that was created initially for class-B.

Following this procedure a maximum efficiency of 87.0% and output power of 20.26dBm is achieved. Considering that higher harmonic impedances were not short or open-circuits, but kept at the 50Ω characteristic impedance of the measurement system, and that the actual knee-voltage is larger than zero, the achieved performance is still close to the theoretical optimum of 90.7%.

B. Validation of the Continuous Class-F

After achieving the class-F condition the new design space was explored for the identified range of γ. Here, the reactance of the fundamental impedance (X1) was varied versus a range of second harmonic reactance.

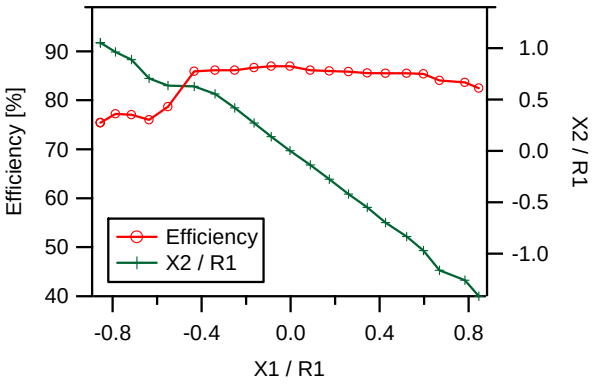

Fig. 4. Measured efficiency for coupled variations of fundamental and second harmonic reactance with an open-circuited third harmonic impedance.

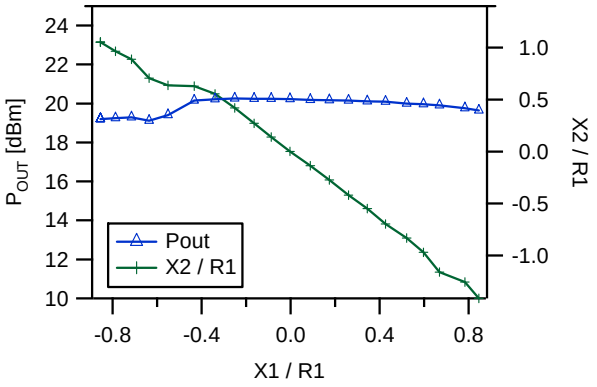

Fig. 5. Measured output power for coupled variations of fundamental and second harmonic reactance with an open-circuited third harmonic impedance.

While stepping through the values of γ, the drive power to the device was actively adjusted to keep the output power constant. In fact, the required drive power adjustment was larger than initially expected, resulting in the experimental verification of this new continuous class-F mode from γ=-1 to 1. This translates to a variation of X1/R1 from 0.85 to -0.85. During these measurements the third harmonic impedance was maintained as an open circuit. Figures 4 and 5 show an extracted plot of measured efficiency and power over the range of X1 and X2. Maximum efficiency of 87.0% is achieved for X1/R1=0 (class-F). It is important to highlight that efficiency and output power are maintained at almost constant levels for a wide range of X1/R1 from -0.4 to 0.85, consistent with the theoretical prediction.

For further investigations contour plots have been measured over the new impedance design space as shown in Fig. 6 and 7.

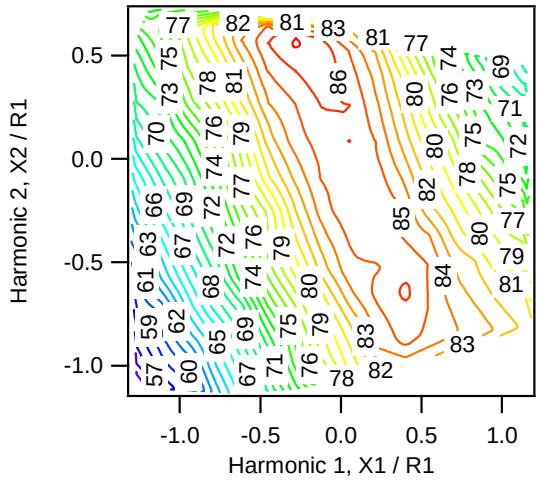

Fig. 6. Measured drain efficiency as a function of normalized X1 and X2, measured for constant drive signal.

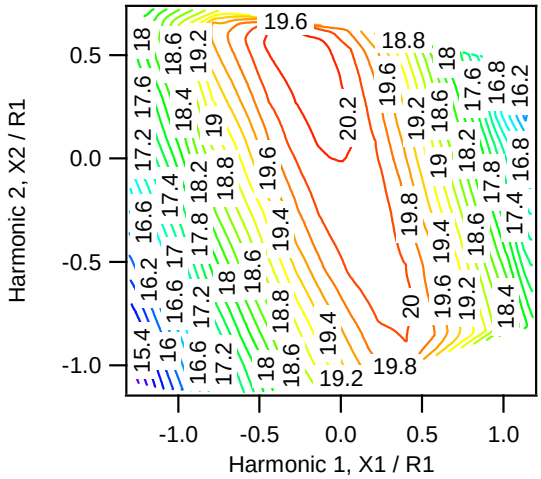

Fig. 7. Measured output power as a function of normalized X1 and X2, measured for constant drive signal.

During these measurements, the drive power has been kept constant. The contour plots demonstrate that both drain efficiency and output power are dependent on the fundamental and second harmonic reactance, and clearly indicate the predicted design space, producing an optimum device performance ridge of coupled X1 and X2 solutions.

Device performance degrades most when both the fundamental and second harmonic reactances are either positive or negative, as within the continuous class-F mode X1 and X2 have an inverse relationship. In practical design such variations over frequency could be incorporated into the design of the output matching network.

Interestingly, the realisation of the continuous class-F mode does not seem to require an exact relationship between the two harmonic voltage components and therefore allows some additional design flexibility.

Fig. 8 depicts the changes of input reflection coefficient at the fundamental frequency during the emulation of the continuous class-F mode. These changes are thought to be caused by the increased peak values of the drain voltage for $\gamma \neq 0$ and explain the need for drive power adjustments during the emulation of this PA mode. Again, over frequency, this can be compensated for in the design of the input matching network.

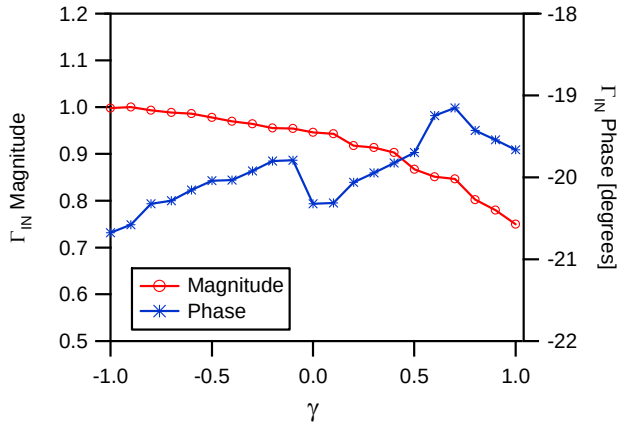

Fig. 8. Measured variations of the input reflection coefficient during the emulation of the continuous class-F PA mode.

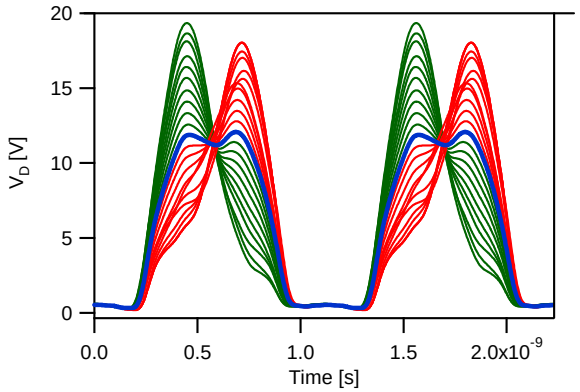

Fig. 9. Measured RF voltage waveforms at current-generator plane for 'continuous class-F mode', with γ ranging from -1 to 1.

Fig. 9 shows measured RF voltage waveforms at the current-generator plane with γ ranging from -1 to 1 with the classic class-F waveform given for X1/R1=0 (highlighted waveform). It can be seen that the waveforms are very similar to the theoretical ones from Fig. 1.

Comparing the continuous class-F waveforms with those of the standard class-F also highlights the increase in peak voltage, which effectively creates the new design space, but at the same time must be tolerated by the device technology.

Besides it can be seen that the peak of voltage waveforms for $\gamma > 0$ (red lines) don't raise to the same peak of voltage waveforms for $\gamma < 0$ (green lines), this is because for $\gamma > 0.5$ (X1/R1<-0.4) the second harmonic impedances cannot be placed on the edge of the smith chart. This is due to the nature of the device with consequence of non-optimum behaviour as even shown in Fig. 4 and 5.

V. Conclusion

This paper has presented for first time a new power amplifier mode that the authors have termed "Continuous Class-F". The novel theoretical formulation for the voltage waveform allows for the realization of constant efficiency and output power, equivalent to the standard class-F mode, over a wider design space. This allows the achievement of broadband, high efficiency RFPAs. It is important to emphasize that the opportunity to move away from a unique solution toward a constellation of solutions allows the PA designer increased flexibility over the topology of subsequent matching networks. The paper clearly shows that it is possible to vary simultaneously, fundamental and second harmonic impedances to maintain the desired output performance that is consistent with that of the original class-F, producing constant drain efficiencies around 85%. Future work will focus on extensions of the new design space, its sensitivity and its dependence on the underlying device technology.

Acknowledgment

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Publication 2.

Title:

On the Extension of the Continuous Class-F Mode Power Amplifier

Authors:

V. Carrubba, A. L. Clarke, M. Akmal, J. Lees, J. Benedikt. P. J. Tasker, S. C. Cripps.

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On the Extension of the Continuous Class-F Mode Power Amplifier

Vincenzo Carrubba, Alan. L. Clarke, Muhammad Akmal, Jonathan Lees, Johannes Benedikt, Paul J. Tasker, *Senior Member, IEEE, and* Steve C. Cripps, *Fellow Member, IEEE*

Abstract — **The Extended Continuous Class-F Mode RFPA (RF power amplifier) is presented for the first time. The introduction and experimental validation of this novel PA mode demonstrates a new design space over a wide band of frequencies. This paper will show that high output power and drain efficiency, equivalent to the class-F mode, can be maintained by varying the reactive components of fundamental and second harmonic impedances in accordance with the new formulation of the voltage waveform. Additionally it will be shown that, by varying both phase and magnitude of the fundamental and second harmonic impedances, a yet wider design space can be achieved, where the efficiency is maintained at a level greater than a certain target value. For the validation of this new theory, an experimental investigation was carried out on GaAs pHEMT devices and demonstrates that high output power and drain efficiency between 75% and 83% can be achieved over a wide range of fundamental and second harmonic loads.**

***Index Terms*—Broadband amplifiers, microwave amplifiers, microwave measurements, power amplifiers, RF circuits.**

I. INTRODUCTION

POWER Amplifier (PA) design for wireless communication has to date been largely focused on improving efficiency and linearity for specified low percentage RF bandwidths. Conventionally, higher efficiency PAs are designed for narrow-band operation [1] and cannot be used in broadband applications covering multiple bands in wireless communication systems. Future 4G (Fourth Generation) wireless network systems, which include WiMax (Worldwide Interoperability for Microwave Access) and LTE (Long term Evolution), are in continuous progression to satisfy the great demand in mobile phones with high QoS (Quality of Services). The development of a PA design methodology for these advance systems will be required in order to allow more services as higher data-rate transmissions over long distances. However the achievement of these new technologies with all these services will require larger bandwidths.

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The authors are with the Centre for High Frequency Engineering, Cardiff School of Engineering, Cardiff University, CF24 3AA, Cardiff, U.K. (email: carrubbav@cardiff.ac.uk; ClarkeA4@cardiff.ac.uk; akmalm1@cardiff.ac.uk; leesj2@cardiff.ac.uk; Benedikt@cardiff.ac.uk; tasker@cardiff.ac.uk; stevehywave@aol.com).

The challenge in designing broadband PAs is to maintain the same performance in terms of linearity, output power and efficiency compared with standard narrow-band modes such as class-F or inverse class-F [1], [2]. For these two PA modes the aim is to maintain the required short and open circuit harmonic terminations, which due to practical constraints must be placed at a distance from the device. However this generally limits the achievable relative bandwidth. Recent publications [3], [4], [5], [6] have shown a theoretical formulation for the voltage waveforms in RF power amplifiers (RFPAs) and introduce new PA modes that maintain a constant and high efficiency over a continuous range of fundamental and second harmonic impedances. The results presented to date have demonstrated a continuous set of waveforms unifying the class-B and class-J modes of operation, allowing more flexibility in PA design. This work builds on this new theoretical formulation and extends, to the class-F PA mode of operation. The new "Extended Continuous Class-F mode PA" shows that there are many more useful solutions that guarantee high output power and efficiency. This "design space" allows the designer more flexibility in the realization of passive networks having greater relative bandwidth than in conventional design approaches. The time-domain waveform measurement system used in these measurements for the validation of the extended continuous class-F mode is based on the Microwave Transition Analyzer (MTA). The MTA allows input and output waveforms to be sampled. A sweeper in the source provides the necessary input power to drive the device at the fundamental frequency. An active harmonic envelope load-pull (ELP) system [7] is used to present the stipulated three harmonic impedances that are necessary for the wide range of measurements where harmonic impedances are continuously varied.

II. STANDARD CLASS-F DESIGN

The ideal class-F PA mode requires a squared-up voltage waveform containing only fundamental and odd higher harmonic components and a half-wave rectified sinusoidal current waveform at its output current-generator plane [8].

These waveforms can be represented by the equations (1) and (2) [2], [9]:

$$v_D(\vartheta) = V_{DC} - V_1\cos(\vartheta) - V_3\cos(3\vartheta) - V_5\cos(5\vartheta) - ,..... \quad (1)$$

$$i_D(\vartheta) = \begin{cases} I_{peak}\cos(\vartheta) & -\pi/2 < \vartheta < \pi/2 \\ 0 & -\pi < \vartheta < -\pi/2 \\ & \pi/2 < \vartheta < \pi \end{cases}, \quad (2)$$

where I_{peak} is the peak current and ϑ represents the conduction angle.

Assuming a spectral content that includes an infinite number of harmonics, an ideal efficiency of 100% can be achieved, when the voltage waveform becomes a perfect square wave. When reducing the number of utilized voltage harmonics to three, the maximum efficiency is reduced to 90.7%. It is important to note however that in practice the current waveform is not limited to three harmonic components, hence the replication of such truncated modes (half rectified waveform) still requires higher odd harmonics to be short-circuited [2].

The key in achieving such high efficiencies is to arrange for the presence of harmonics to allow an increase in the fundamental voltage component, whilst maintaining the condition that the voltage never reaches zero during the RF cycle. In practical PA design, the current waveform is engineered through a suitable DC biasing of the device, typically around the ideal "zero-bias" class-B point of operation. The correct output voltage waveform is then obtained using a passive output network which provides the necessary harmonic terminations at the current-generator plane. This conventional implementation has been considered to require the even harmonics to be short circuited to prevent the harmonic content of the current waveform being imposed on that of the voltage. This requirement presents a significant design challenge as any shunt resonator can only be placed at the extrinsic plane of the transistor, contributing to a very restricted frequency range of operation.

III. CONTINUOUS CLASS-F MODE

Recent investigations into this new power amplifier mode [5] have shown that, when working with constant open-circuited third harmonic impedance, a shorted second harmonic component is not a unique solution for achieving maximum efficiency and output power. The required voltage waveforms are defined by (3), which has been derived from the generic factorial representation of voltage waveforms as defined by Cripps [4].

$$v(\vartheta)=(1-\alpha\cos\vartheta)^2\cdot(1+\beta\cos\vartheta)\cdot(1-\gamma\sin\vartheta), \qquad (3)$$

where α, β and γ are three parameters which define the design space. It is very important that, for each combination of the three values, the voltage waveform is kept above zero:

$$v(\vartheta)>0. \qquad (4)$$

If the voltage waveform crosses zero at any point, the device current will drop immediately to zero resulting in a drastic reduction of power and efficiency and highly non-linear behaviour.

Equation (3) can be expanded to give the following expression for the current-generator plane voltage:

$$v(\vartheta)=V_{DC}-A_1\cos(\vartheta)-A_2\cos(2\vartheta)-A_3\cos(3\vartheta)+ +B_1\sin(\vartheta)+B_2\sin(2\vartheta)+B_3\sin(3\vartheta)+B_4\sin(4\vartheta), \qquad (5)$$

where V_{DC} represents the supply voltage. A_1, A_2 and A_3 represent the voltage components of the real part of the fundamental, second and third harmonic impedances, and B_1, B_2, B_3 and B_4 represent the voltage components of the imaginary part of the fundamental, second, third and fourth harmonic impedances.

This gives:

$$V_{DC}=1+\frac{1}{2}\alpha^2-\alpha\beta, \qquad (6)$$

$$A_1=2\alpha-\beta-\frac{3}{4}\alpha^2\beta, \qquad (7)$$

$$A_2=\alpha\beta-\frac{1}{2}\alpha^2, \qquad (8)$$

$$A_3=-\frac{1}{4}\alpha^2\beta, \qquad (9)$$

$$B_1=\gamma\left(\frac{1}{2}\alpha\beta-1-\frac{1}{4}\alpha^2\right), \qquad (10)$$

$$B_2=\gamma\left(\alpha-\frac{1}{2}\beta-\frac{1}{4}\alpha^2\beta\right), \qquad (11)$$

$$B_3=\gamma\left(\frac{1}{2}\alpha\beta-\frac{1}{4}\alpha^2\right) \qquad (12)$$

$$B_4=-\frac{1}{8}\gamma\alpha^2\beta. \qquad (13)$$

Real and imaginary harmonic impedances are normalised to the DC voltage (V_{DC}).

For the theoretical continuous class-F, to achieve the maximum drain efficiency, the second harmonic impedance must be kept reactive. To obtain this, the parameter A_2 in (8) is set to zero, giving the condition

$$\beta=\alpha/2. \qquad (14)$$

The presence of the third harmonic voltage allows the increase of fundamental component. Substituting the value $\beta=\alpha/2$ in the real part of the fundamental component (7):

$$A_1=\frac{3}{8}\alpha^3-\frac{3}{2}\alpha. \qquad (15)$$

Differentiating (15) as shown in (16), the maximum amplitude of fundamental voltage (α) for optimum class-F condition can be determined, as shown in (17):

$$A_1'(\alpha)=\frac{9}{8}\alpha^2-\frac{3}{2}=0, \qquad (16)$$

giving

$$\alpha=2/\sqrt{3}. \qquad (17)$$

Keeping the parameters α and β constant, γ is the only parameter to be swept to reveal the continuous class-F mode:

$$-1\le\gamma\le1. \qquad (18)$$

In accordance with (14), (17) and (18), the new family of voltage waveforms, as a function of γ, are derived from (5), and are illustrated in Fig. 1 [5]. For γ=0, the standard class-F voltage waveform is achieved with a theoretical drain efficiency of 90.7% (highlighted red line). For all other values of γ, the new voltage waveforms still maintain the class-F power and efficiency performance, but have significantly modified waveforms. We assume that the device has sinusoidal input excitation and is biased for Class B operation, resulting in a half-wave rectified sinusoidal current waveform.

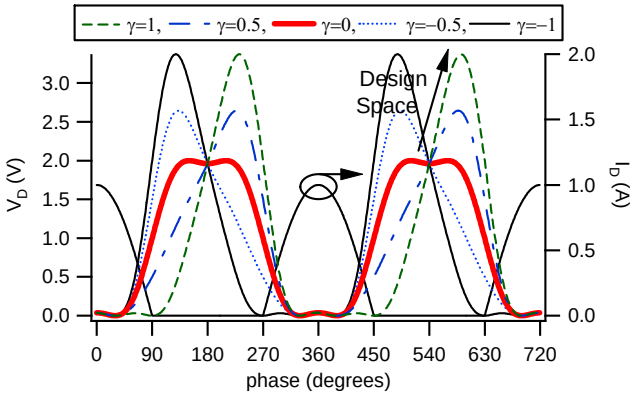

Fig. 1. Theoretical continuous class-F current and voltage waveforms, for $-1 \le \gamma \le 1$ with steps of 0.5.

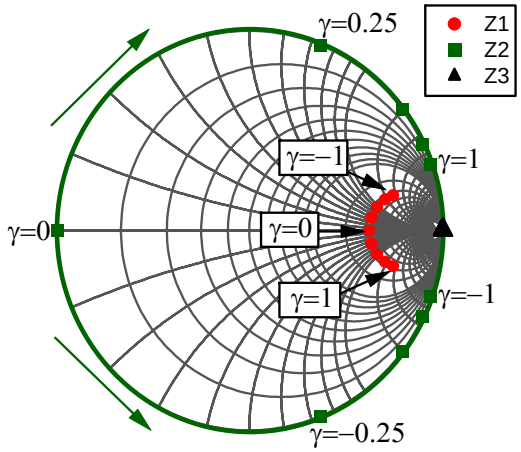

Fig. 2. Continuous class-F impedance range for the first three harmonic impedances when varying $-1 \le \gamma \le 1$ with steps of 0.25.

The key to engineering this new PA mode lies in changing the reactive component of the fundamental load whilst varying the phase of the second harmonic impedance, in accordance with (5). In this way, it is possible to keep the voltage waveform above zero and maintain a constant, high efficiency state. The required impedances are shown in Fig. 2 with γ changing from -1 to 1 generating a second harmonic reactance that varies around the edge of the Smith chart, while the fundamental harmonic impedance simultaneously varies on a circle of constant resistance.

This set of viable loads represents a new "design space" which allows increased flexibility in PA design. In this space different corresponding values of fundamental and second harmonic impedances can be chosen to maintain the same theoretical output power and efficiency. The important aspect to highlight is that PA designers do not necessarily need to provide a short-circuit second harmonic impedance in an actual PA design, but have a choice of a significantly wider design space over which optimum device performance is maintained.

Fig. 3 shows drain efficiency and reactance of the fundamental and second harmonic impedances normalized to the fundamental resistance R_1, against the parameter γ. It can be seen that when increasing γ, the second harmonic reactance increases whilst the fundamental reactance

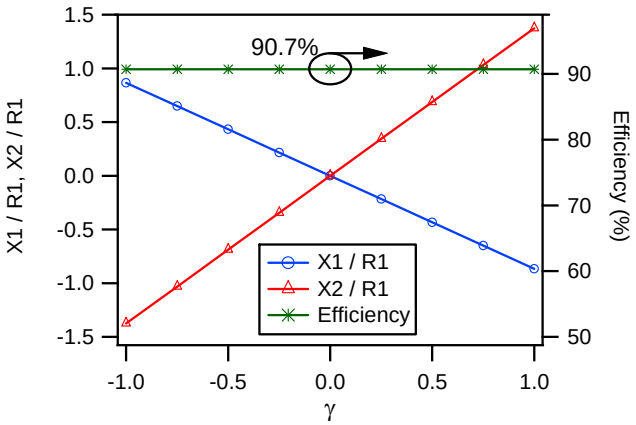

Fig. 3. Theoretical efficiency and fundamental and second harmonic reactive impedances (X_1 and X_2), normalized to R_1, as a function of γ, for $-1 \le \gamma \le 1$ with steps 0.25.

decreases, in this case the efficiency is kept constant to an ideal value of 90.7%.

For γ=0 with $X_1/R_1=X_2/R_1=0$, the standard class-F mode is obtained. For all other values of γ, a change of X_1 must be accompanied by a negative change of X_2 in accordance with (5) to maintain constant output power and efficiency.

IV. THE EXTENDED CONTINUOS CLASS-F MODE

In previous section, using a constant value of $\beta=\alpha/2$ and $\alpha=2/\sqrt{3}$ (1.154 approx.), the parameter γ was varied and the "Continuous class-F mode" which defines a new design space has been revealed. This new design space allows second harmonic impedance to be varied on the edge of the Smith chart whilst fundamental impedance is swept to the circle at constant resistance maintaining constant maximum output power and drain efficiency. The next step is to vary the parameters α and β in order to maintain the drain efficiency greater than a certain pre-determined useful value which has been chosen here as 75%.

$$\eta > 75\%. \tag{19}$$

Obviously the continuous class-F mode explained in Section III, delivers the maximum efficiency because the value of α was chosen in order to represent the standard class-F condition, having an efficiency of 90.7%. In this case when varying α, β and γ it will be shown that efficiency greater than 75% can be maintained over a significantly wider design space than that discussed in previous section.

The continuous class-F mode and its extension are achieved when voltage waveforms are positive. In order to avoid that voltage waveforms drop below zero, for $\beta=\alpha/2$ the following conditions must be achieved:

$$-2 \le \alpha \le 2\,, \quad \alpha \ne 0\,, \tag{20}$$

$$-1 \le \gamma \le 1\,. \tag{21}$$

The range of α and γ shown in (20) and (21) will be smaller taking into account different values of β

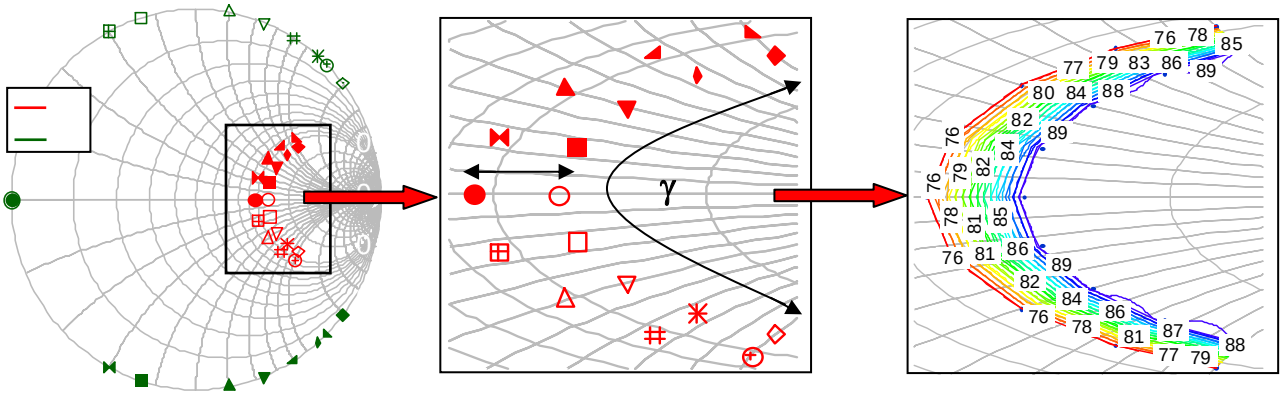

Fig. 4. Continuous class-F impedance range and efficiency contour plot for the first two harmonic impedances (the third is kept as an open) when varying $0.75 \le \alpha \le 1.25$ and $-1 \le \gamma \le 1$ with α step of 0.5 and γ step of 0.25.

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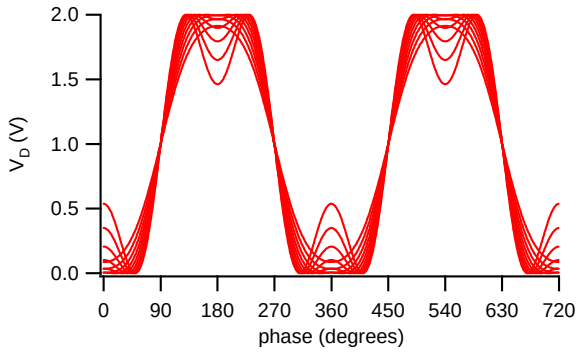

Fig. 5. Theoretical voltage waveforms for constant $\beta=\alpha/2$ and $\gamma=0$ function of α, where $0.75 \le \alpha \le 1.55$ with steps of 0.1.

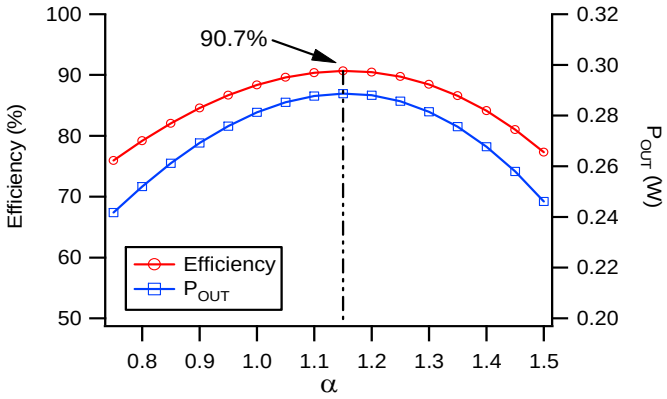

Fig. 6. Efficiency and output power for constant $\beta=\alpha/2$ and $\gamma=0$ function of α, where $0.75 \le \alpha \le 1.5$ with steps of 0.05.

A. Extending the Continuous Class-F with second harmonic impedance on the edge of the Smith chart ($\beta=\alpha/2$)

Here with a constant value of $\beta=\alpha/2$ and varying the other two parameters α and γ, the second harmonic impedance varies still on the edge of the Smith chart, whilst the fundamental impedance varies both magnitude and phase still achieving high efficiencies states, as shown in Fig. 4. Each fundamental load has its corresponding second harmonic impedance in order to maintain high output power and drain efficiency.

Fig. 5 shows the voltage waveforms with varying α, keeping $\beta=\alpha/2$, for $\gamma=0$. Note that with increasing values of α, bigger "troughs" in the voltage waveforms are developed. This translates into lower efficiency due to the lower fundamental voltage.

Fig. 6 shows the efficiency and output power variation with α for a constant value of $\gamma=0$. Note that highest efficiency is achieved for $\alpha = 2/\sqrt{3}$ which is the class-F condition, but a wide range of fundamental impedances can be chosen which still yield efficiencies greater than 75%. Those theoretical values of efficiency and output power remain constant over the range of $-1 \le \gamma \le 1$.

To achieve a non zero-crossing voltage waveform, the parameter α must be non-zero and lie between -2 and 2, as shown in (20). In this case, in accordance with (5), maintaining efficiency greater than 75 % causes the range of α to be further restricted,

$$0.75 \le \alpha \le 1.5 . \qquad (22)$$

B. Extending the Continuous Class-F with second harmonic impedance inside the Smith chart ($\beta>\alpha/2$)

Following the same procedure of Section *A*, the parameters α, γ and now also β will be varied. In the previous section the value of β was restricted to $\beta=\alpha/2$ ($A_2=0$), thus the second harmonic impedance was swept around the edge of the Smith chart. We now consider the more general case where the second harmonic impedance can be chosen inside the Smith chart, where for $\beta>\alpha/2$, in accordance with (8) and (5) the parameter A_2 is kept greater than zero.

The new condition of β variation delivers a wider range of design space that guarantees a stipulated minimum output performance.

When changing all three parameters, the range of those parameters which yield a non zero-crossing voltage waveform and a minimum drain efficiency of 75% is shown in Table I, which is based on (4) and (19).

Voltage waveforms are shown for $\beta = \alpha / 1.6$ in Fig. 7. Note that with increasing value of α, again bigger troughs in the voltage waveforms are developed. If the parameter β increases, the range of α and γ where voltage waveforms are greater than zero and drain efficiency is greater than 75 % is reduced, as shown in Fig.8. For $\beta=\alpha/2$ the efficiency is greater than 75 % for a wide range of α ranging from 0.75 to 1.5. For $\beta=\alpha/1.5$ that range of α is between 0.9 and 1.2, and for $\beta=\alpha/1.4$ the only point that allows positive voltage and high efficiency is $\alpha=1.05$.

$\beta = \alpha / 2$	$\beta = \alpha / 1.9$	$\beta = \alpha / 1.8$	$\beta = \alpha / 1.7$	$\beta = \alpha / 1.6$	$\beta = \alpha / 1.5$	$\beta = \alpha / 1.4$
$0.75 \le \alpha \le 1.5$	$0.75 \le \alpha \le 1.45$	$0.8 \le \alpha \le 1.45$	$0.8 \le \alpha \le 1.3$	$0.85 \le \alpha \le 1.3$	$0.9 \le \alpha \le 1.2$	$\alpha = 1.05$
$-1 \le \gamma \le 1$	$-1 \le \gamma \le 1$	$-1 \le \gamma \le 1$	$-0.9 \le \gamma \le 0.9$	$-0.5 \le \gamma \le 0.5$	$-0.2 \le \gamma \le 0.2$	$\gamma = 0$

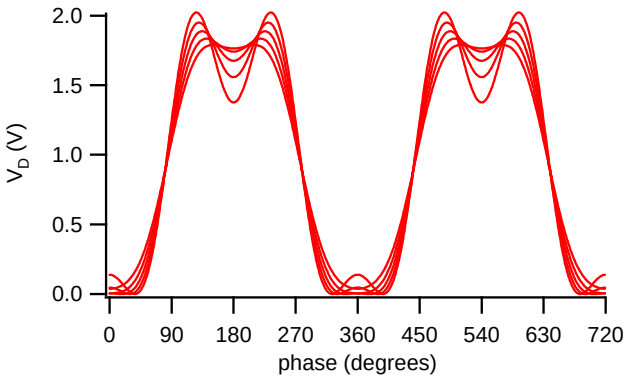

Fig. 7. Theoretical voltage waveforms for constant $\beta = \alpha / 1.6$ and $\gamma = 0$ function of α, where $0.85 \le \alpha \le 1.3$ with steps of 0.1.

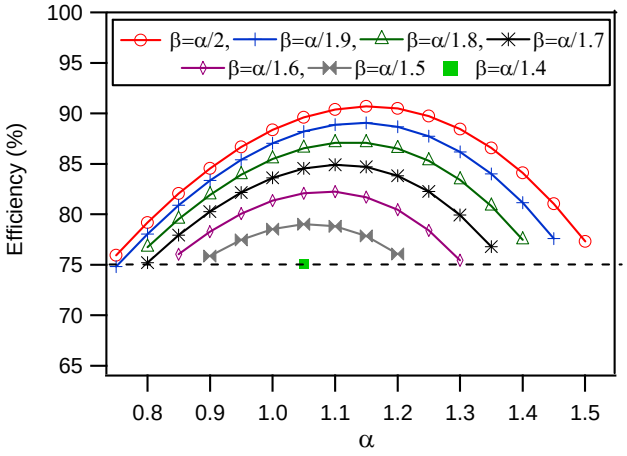

Fig. 8. Drain efficiency function of α and β for constant γ=0.

Fig. 9 shows the wide design space, which allows very high flexibility in PA design. In this space it is important to note the continuity of this new PA mode. Also in this case, each fundamental load has its appropriate second harmonic load. It shows for example one combination of fundamental impedance (Z1', red triangle, even shown inset) and second harmonic impedance (Z2', green square) in accordance with (5) which maintain the stipulated high efficiency state (third harmonic impedance Z3 is kept open). In this case a drain efficiency of 89.5% is achieved.

Fig. 10 shows the maximum efficiency as a function of β for a given optimum α. Note that the efficiency decreases with increasing values of β but efficiencies greater than 75% are still maintained.

Fig. 11 plots efficiency and output power as a function of α and γ with constant $\beta=\alpha/1.6$. Note that for α greater than 0.95, (4) and (19) are valid for just γ=0 (red line). Again it shows with increasing β, the useful design space decreases.

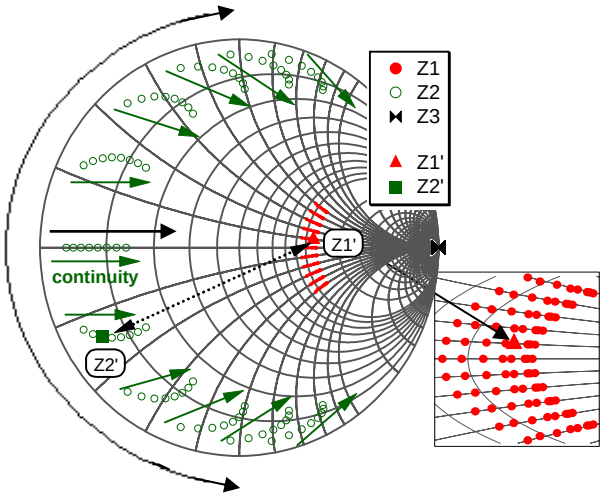

Fig. 9. Extended continuous class-F impedance range for the first three harmonic impedances with $\beta=\alpha/1.9$ when varying $0.75 \le \alpha \le 1.45$ and $-0.5 \le \gamma \le 0.5$ with both steps of 0.1, inset collection of fundamental impedances.

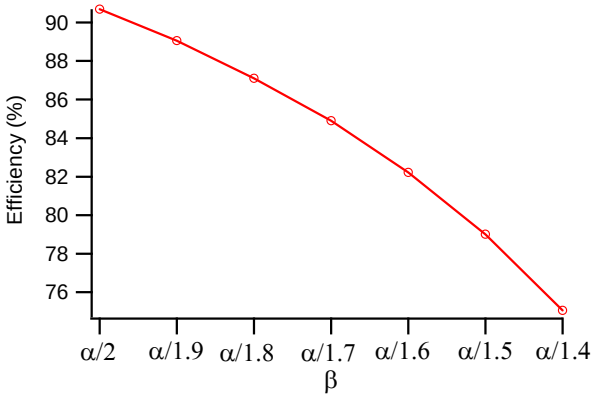

Fig. 10. Extended Continuous class-F efficiency function of β for γ=0 and optimum value of α =1.15.

VI. Experimental Analysis and Verification

The design space defined theoretically in the previous section has been explored experimentally using the ELP active load-pull system developed at Cardiff University [7]. The ELP load-pull architecture is shown in Fig. 12.

The device transmitted signal b_2 is down converted to the baseband frequencies using an I/Q modulator. Here, the down converted I_b and Q_b signals, are then injected in an electronic control-unit box, and by setting the correct values of the external variables X and Y (thorugh GPIB cable) the

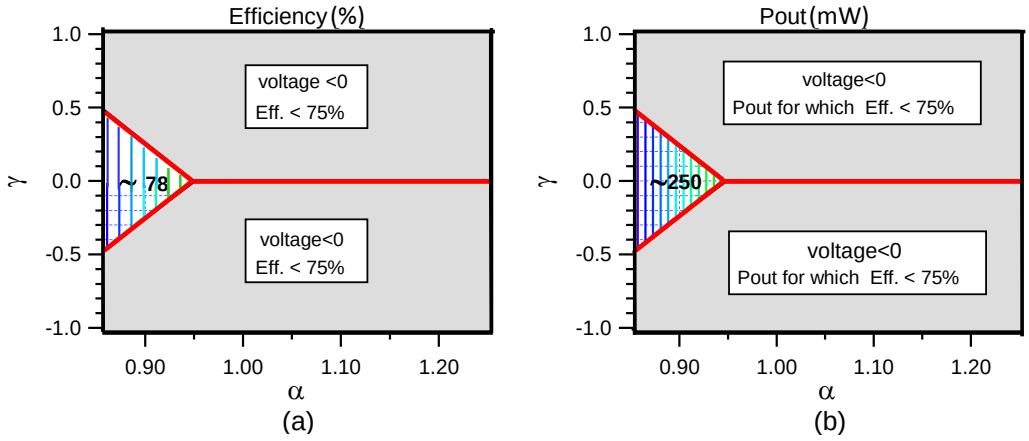

Fig. 11. Efficiency (a) and output power (b) contour plot for constant $\beta=\alpha/1.6$, function of α and γ, with $0.85 \le \alpha \le 1.3$ and $-0.5 \le \gamma \le 0.5$ with both steps of 0.1.

required signals I_a and Q_a are achieved (by using a software developed in Cardiff University).

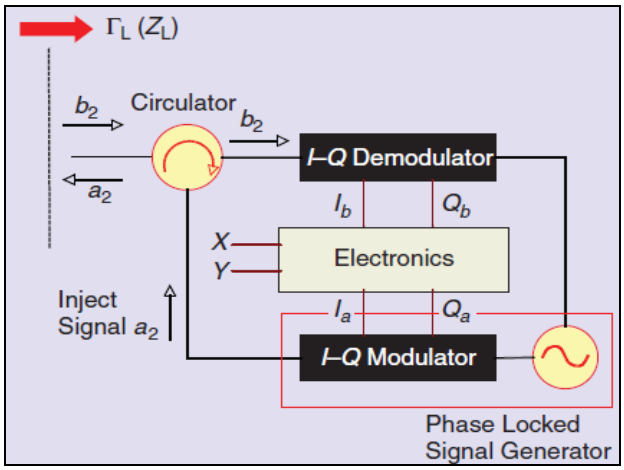

Fig. 12. Envelope load-pull (ELP) architecture.

These signals can then be up converted to the RF frequency, and the wave a_2 will go into the output of the DUT (device under test). The emulated load reflection coefficient (Γ) is therefore given by the ratio of the reflected (a_2) and the transmitted (b_2) waves, as shown in (23).

$$\Gamma(t) = \frac{a_2}{b_2} = X(t) + jY(t) \qquad (23)$$

The measurement system allows voltage and current waveforms to be measured at the external (package) device plane and then shifted to the device output generator plane by de-embedding the drain-source capacitor C_{DS} [10]. Devices used in this paper are on-wafer from TriQuint TQPED GaAs Foundry process, specifically 6x50 µm depletion mode. The measurements have been conducted at 0.9 GHz, using 6 V drain supply voltage and approximately 20 dBm of output power.

A. *Starting point: Class-F condition*

Before the new PA modes can be explored, the class-F condition must be initially achieved [11]. In this first step, a value for the bias voltage (V_G) is selected for which the third harmonic current is minimized. This condition produces the half-rectified sinusoidal current waveform required. Once the current waveform is established, the desired class-B fundamental load is determined with higher harmonic impedances being short-circuited. To move toward the class-F mode, harmonic load-pull is employed to engineer the voltage waveform. Here, the second harmonic impedance is kept at a short whilst the third harmonic impedance is open-circuited.

In the final step the fundamental impedance is scaled by $4/\pi$ to increase the fundamental voltage component and therefore regain the minimum voltage value of the squared waveform that is comparable to the original class-B mode. In this case an optimum fundamental impedance R_1=215+j*0 Ω is obtained. The scaling of the fundamental load also restores the fundamental current swing that was created initially for class-B.

The measured maximum efficiency does not reach the ideal value of 90.7% because the higher harmonic impedances were not short or open-circuits, but kept close to the 50 Ω characteristic impedance of the measurement system. Additionally, the actual knee-voltage is greater than zero, thus explaining the measured maximum efficiency value of 82.89% and output power of 20.22 dBm.

B. *Validation of the Continuous Class-F ($\beta=\alpha/2$)*

After achieving the class-F condition, a new design space for a constant β and α was explored for the identified range of γ. Here, the reactance of the fundamental impedance (X_1) was varied versus a range of second harmonic reactances (X_2). While stepping through the values of γ the drive power to the device was adjusted to keep the drain current constant. This resulted in experimental verification of this new continuous class-F mode from γ =-1 to 1, which translates to a variation of X_1/R_1 from 1.05 to -0.9 and of X_2/R_1 from -1.7 to 0.75. During these measurements the third harmonic impedance was maintained at an open circuit.

Fig. 13 shows an extracted plot of measured efficiency and power over the range of X_1 and X_2. Maximum efficiency of 82.89% is achieved for $X_1/R_1=0$ (class-F). It is important to highlight that efficiency and output power are maintained at almost constant levels for a wide range of X_1/R_1 from -0.5 to 1.05, consistent with the theoretical prediction. For $X_1/R_1<-0.5$ output power and the efficiency drop. This is due to the fact that the load-pull system was not able to place the second harmonic impedance on the edge of the smith chart in accordance with (3) due to stability issues, so was kept constant around 48°. This limitation is also attributed to the non-unilateral characteristics of this device.

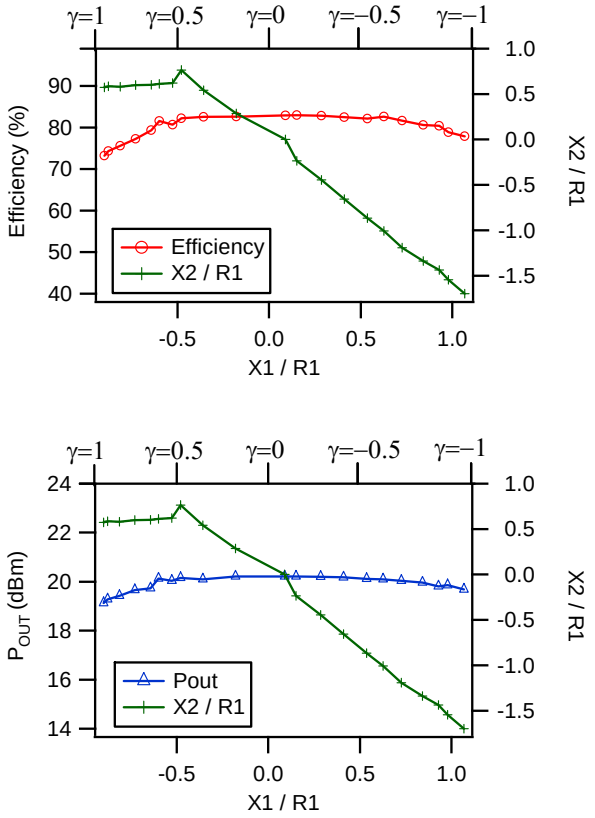

Fig. 13. Measured efficiency and output power for coupled variations of fundamental and second harmonic reactance with $\beta=\alpha/2$, $\alpha=1.15$ and keeping open-circuited the third harmonic impedance.

For further investigations contour plots have been measured over the new impedance design space as shown in Fig. 14. During these measurements, the drive power has been kept constant. The contour plots demonstrate that both drain efficiency and output power are dependent on the fundamental and second harmonic reactance, and clearly indicate the predicted design space, producing an optimum device performance region of coupled X_1 and X_2 solutions. Best performance is when the fundamental is positive and second harmonic reactance is negative, and vice versa, as within the continuous class-F mode X_1 and X_2 have an inverse relantionship. In practical design such variations over frequency could be incorporated into the design of the output matching network. The impedances of the standard class-F mode are highlighted with the red squares in Fig. 14.

Fig. 15 shows measured RF voltage waveforms at the current-generator plane with γ ranging from -1 to 1, along with the classic class-F waveform ($X_1/R_1=0$, highlighted). It can be seen that the waveforms are very similar to the theoretical predictions shown from Fig. 1. For $\gamma>0$ (blue waveforms) the voltage waveforms don't reach the maximum peak of around 20V due to the stability issues explained previously.

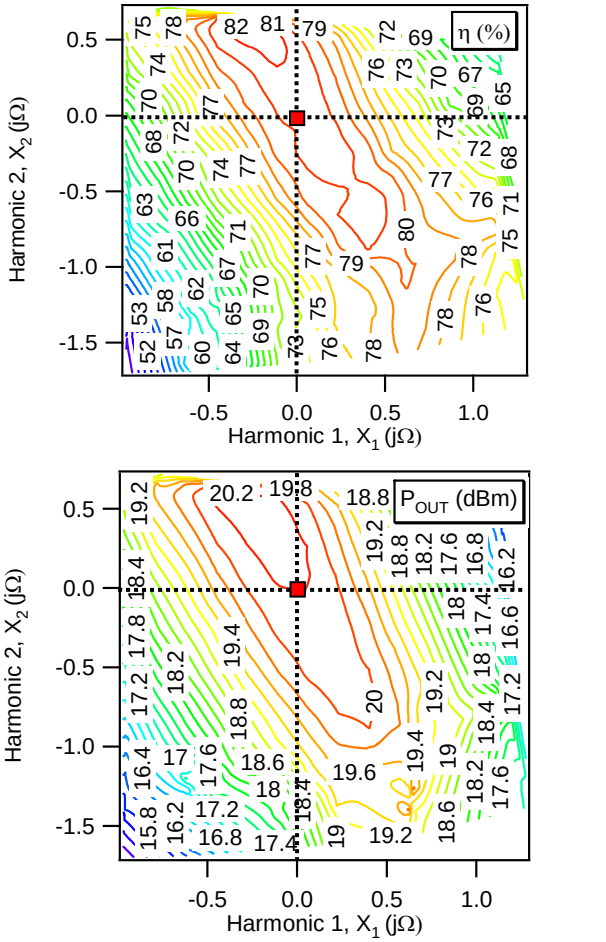

Fig. 14. Measured efficiency and output power as a function of normalized X_1 and X_2, measured for constant drive signal.

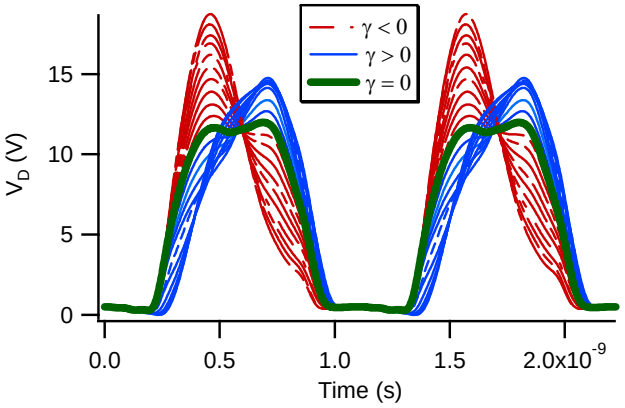

Fig. 15. Measured RF voltage waveforms at current-generator plane for 'continuous class-F mode', with γ ranging from -1 to 1.

Comparing the continuous class-F waveforms with those of the standard class-F also highlights the increase in peak voltage, which effectively creates the new design space, but at the same time must be tolerated by the device technology. Although this may at first sight appear to be a serious

limitation for extended modes, there are in practice many cases where such high peak voltages can be tolerated (e.g. GaN devices, low voltage supply applications).

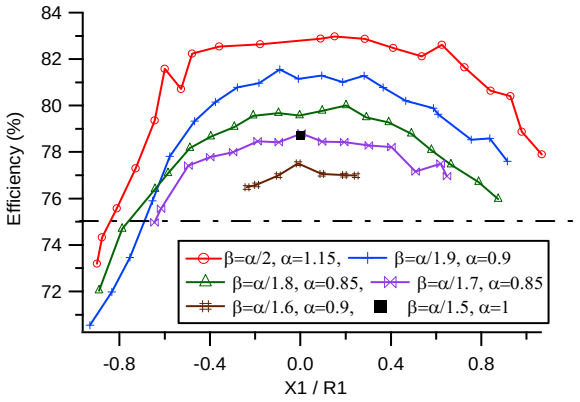

Fig. 16. Measured drain efficiency function of β, α and γ.

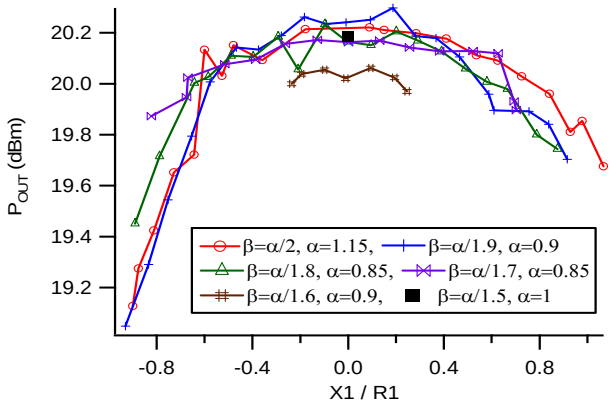

Fig. 17. Measured output power function of β, α and γ.

C. *Validation of the Extended Continuous Class-F (β>α/2)*

In this section it will be demonstrated that the design space for a stipulated power and gain performance can be further extended in comparison to that already discussed in section V.B. The new PA mode that the authors have called "Extended Continuous Class-F" provides a collection of valid load points that describes a design space wider than continuous class-F. In this case, in accordance with (3), the second harmonic impedance can be chosen inside the Smith chart but efficiencies greater than 75 % can still be obtained.

Figure 16 and 17 show the behavior of drain efficiency and output power as a function of β and γ. The parameter α has been chosen in order to maintain the maximum range where voltage waveforms are non zero-crossing. It can be seen that best performance is achieved for β=α/2, which is the class-F condition with maximum efficiency of 82.89%. Note that as the parameter β increases, the efficiency and output power decrease, and the range of valid cases (i.e. cases where both the voltage is non zero-crossing and efficiency greater than 75%) also decrease. Although the second harmonic impedance has been chosen with a positive real part (i.e. inside the Smith chart), drain efficiency is still kept above the target efficiency of 75%. For X_1/R_1<-0.7 efficiency drops lower than 75%.

Fig. 18 shows the efficiency function of β and α with constant γ=0. In accordance with the theory, the highest efficiency is achieved for lower values of β (e.g. β=α/2). It also shows that with decreasing α, the efficiency also decreases, and the range where both the efficiency is kept greater than 75% and the voltage is non zero-crossing decrease with increasing β, as explained theoretically in section III and IV.

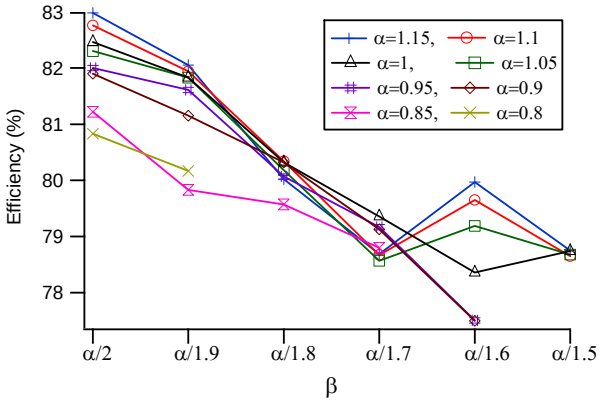

Fig. 18. Measured drain efficiency function of β and α, with constant γ=0.

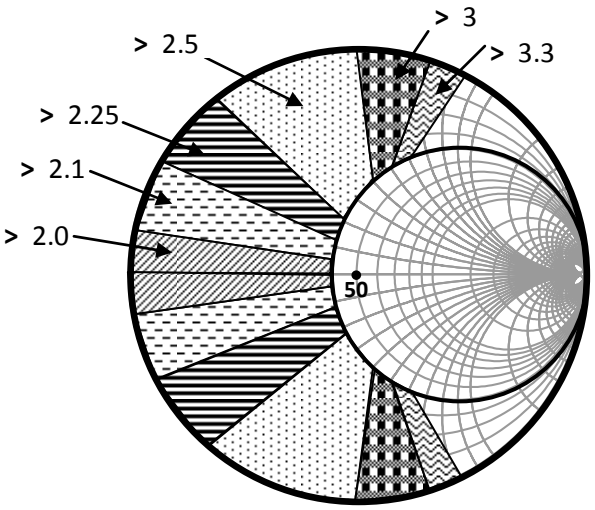

Fig. 19. Peak voltages function of the second harmonic impedances based on a 50 Ohm load-line resistance.

The new theoretical formulation for the voltage waveforms can incur peak voltages that are higher than twice the supply voltage. Fig. 19 shows the variation of peak voltage as the second harmonic impedance is varied over a large design space for the case of fundamental impedance set to 50 Ω. The higher value, zones can be regarded as a potential reliability hazard in PAs, which are designed using entirely empirical tuning techniques.

VI. Conclusion

This paper has presented for the first time a new formulation for the voltage waveform that allows the realization of high efficiency and output power states over a wide range of frequencies. The new PA mode has demonstrated that a drain efficiency greater than a certain target value which has been chosen around 75%, can be achieved over a significant impedance space. It has been shown that it is possible to have different magnitudes and phases of fundamental and second harmonic terminations that still maintain high levels of output performance. The importance of moving from a singular solution (standard

class-F) to an extended design space allows PA designers increased flexibility for the realization of the matching networks. In particular, PA designers do not need to struggle anymore in order to achieve the exact short-circuit condition for the second harmonic load in order to obtain the high efficient class-F condition. With this new theory, different fundamental and second harmonic impedances can be chosen in accordance with the new voltage formulation, still maintaining high efficiency and output power. Future work will focus on the design and realization of this new PA mode, and also its extension to different modes such as inverse
Class-F.

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Vincenzo Carrubba received the B.Sc. degree in electronic engineering and the M.Sc. degree in microelectronic engineering from the University of Catania, Catania, Italy, in 2005 and 2008, respectively.

He is currently working toward the Ph.D. degree in electronic engineering with the Centre for High Frequency Engineering, Cardiff University, Cardiff, Wales, U.K. His research interests include the development of active load-pull techniques, the characterization of microwave devices and the design of broadband power amplifiers used in wireless communications.

Alan L. Clarke (S'08) received the M.Eng. degree in electronic engineering from Cardiff University, Wales, U.K., in 2007, and is currently working toward the Ph.D. degree in electronic engineering at Cardiff University.

He is currently with the Centre for High Frequency Engineering, Cardiff University. His research interests include the development of rapid active load-pull techniques and microwave device characterization for the power amplifier (PA) design process.

Muhammad Akmal received the B.Sc. (Hons) degree in electrical engineering from Bahauddin Zakariya University, Multan, Pakistan, in 2005, the M.Sc. degree in electronic engineering from the Cardiff University, Cardiff, United Kingdom, in 2008, and is currently working toward the Ph.D. degree at Cardiff School of Engineering in Cardiff University.

His current research interests are enhancing the modulated waveform measurement system, characterization of memory effects, linearization, design and characterization of high-power and spectrum-efficient RF power amplifiers.

Jonathan Lees received the B.Eng. degree in electronic engineering from Swansea University, U.K., in 1992, and the M.Sc. and Ph.D. degrees from Cardiff University, Cardiff, U.K., in 2001 and 2006, respectively.

From 1992 to 2002, he was with QinetiQ, where he developed global positioning and advanced optical instrumentation tracking systems. He is a Chartered Engineer and he is now a Research Associate with the Centre for High Frequency Engineering, Cardiff University, where his research continues into power amplifiers design, load-pull, and large signal measurement systems.

Johannes Benedikt received the Dipl.-Ing degree from the University of Ulm, Ulm, Germany, in 1997, and the Ph.D. degree from Cardiff University, Cardiff, U.K., in 2002. During this time, he took on an additional position as a Senior Research Associate with Cardiff University starting in October 2000, where he supervised a research program with Nokia on RFPAs. In December 2003, he was appointed a Lecturer with Cardiff University, where he was responsible for furthering research in the high-frequency area. In April 2010 he was awarded a Professorship at Cardiff University. His main research focus is on development of systems for the measurement and engineering of RF current and voltage waveforms and their application in complex PA design.

Paul J. Tasker (M'88-SM'07) received the B.Sc. degree in physics and electronics and Ph.D. degree in electronic engineering from Leeds University, U.K., in 1979 and 1983, respectively.

From 1984 to 1990 he worked as a Research Associate with Cornell University, Ithaca, NY, with Prof. L. Eastman, where he was involved in the early development of HFET transistors. From 1990 to 1995, he was a Senior Researcher and Manager with the Fraunhofer Institute for Applied Solid State Physics (IAF), Freiburg, Germany, where he was responsible for the development of millimeter wave MMICs. He joined the School of Engineering, Cardiff University, Cardiff, U.K., as a Professor in the summer of 1995, where he has been establishing the Cardiff University and Agilent Technology Centre for High Frequency Engineering. The center's research objective is to pioneer the development and application of RF-IV waveform and engineering systems, with a particular focus to addressing the PA design problem. He has contributed to over 200 journal and conference publications and given a number of invited conference workshop presentations.

Dr. Tasker has been appointed as an IEEE Distingueshed Microwave Lecturer for the term of 2008-2010.

Steve C. Cripps received the Ph.D. degree from Cambridge University, Cambridge, U.K.

He worked for Plessey Research on GaAsFET hybrid circuit development. Later, he joined Waitkins-Johnson's Solid State Division, Palo Alto, CA, and he has held Engineering and Management positions at WJ, Loral, and Celeritek. During this period, he designed the industry's first 2-8 and 6-19 GHz 1 watt solid-state amplifiers. In 1983, he published a technique for microwave power amplifier design, which has become widely adopted in the industry. In 1990, he became an independent consultant and was active in a variety of commercial RF product developments, including the design of several cellular telephone PA MMIC products. In 1996, he returned to the U.K., where he is consulting activities continue to be focused in the RFPA area. He has recently been appointed a Professional Research Fellow at Cardiff University, U.K. He has recently authored a second edition of his best selling book, *RF Power Amplifiers Design for Wireless Communication* (Artech House, 2006).

Dr. Cripps was a recipient of the 2008 IEEE Microwave Applications Award. He is currently vice-chair of the High Power Amplifier Subcommittee of the Technical Coordination and Technical Program Committees of the IEEE Microwave Theory and Techniques Society, and writes the regular
"Microwave Bytes" column in the *IEEE Microwave Magazine*.

Publication 3.

Title:

High-speed device characterization using an active load-pull system and waveform engineering postulator

Authors:

V. Carrubba, A. L. Clarke, S. P. Woodington, W. McGenn, M. Akmal, A. Almuhaisen, J. Lees, S. C. Cripps, P. J. Tasker, J. Benedikt.

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High-Speed Device Characterization Using an Active Load-Pull System and Waveform Engineering Postulator

V. Carrubba, A. L. Clarke, S. P. Woodington, W. McGenn, M. Akmal, A. AlMuhaisen, J. Lees, S. C. Cripps, P. J. Tasker, J. Benedikt

Center for High Frequency Engineering, Cardiff University, Cardiff, CF24 3AA, Wales, UK
email:carrubbav@cardiff.ac.uk

***ABSTRACT* – This paper presents a methodology that provides estimation of the parameters necessary for the high-speed characterization of transistor devices used in modern microwave power amplifiers. The key in achieving this significant measurement speed improvement is the use of a systematic waveform postulation methodology in combination with an active harmonic load-pull system. The methodology is based on a rapid and systematic procedure that initially requires only a few DC measurement parameters to approximate to approximate the device´s transfer characteristic and boundary conditions. Using these parameters, it is then possible to accurately estimate or ´postulate´ the idealized output current and voltage waveforms, in this case for a three harmonic class-F mode. These waveforms are rich in information and provide harmonic load impedances as well as other key postulated parameters that can then be used to ´guide´ the harmonic active load-pull measurement system resulting in a very time-efficient characterization process.**

***Index Terms* – Microwave devices, microwave measurements, parameter estimation, power amplifiers, predictive models.**

I. INTRODUCTION

The importance of minimizing the time required for the characterization of modern microwave devices, such as those used in the RF Power Amplifier (RFPA) has become critical as it allows manufacturers to gain competitive advantage.

An established and preferred approach in designing RFPAs is based on non-linear device modeling, where CAD and a well defined device model is used to reduce and ideally eliminate measurement complexity, reducing to a minimum the number of measurements needed to achieve a required or 'target' performance. In reality however, sufficiently accurate device models tend not to be available for the emerging and highly promising device technologies that may be of interest to future PA designers. The alternative design approach is based on direct device measurement and specifically conducting exhaustive fundamental and harmonic load-pull measurements, possibly at different drive and bias levels and with the design targets usually being drain efficiency and output power. As can be imagined, this approach demands significant microwave measurement hardware and involves a high degree of human interaction over a significant time frame. This paper describes an intermediate design and optimization process that lies somewhere between simple modeling and measurements world, where by combining the two approaches, it is possible to benefit from the advantages of both. Obviously, the device cannot be perfectly described using such a simple model, but using simple information of the device itself it is shown how measurement and characterization time can be substantially reduced. The advantage of using an analytical procedure, in this case IGOR software from WaveMetrics, is to achieve quick results (without any further simulation) which can directly guide and control the load-pull system, indicating the first guess toward the measured optimum output performance. The approach described in this paper is divided into two stages. The first stage involves the extrapolation of simple DC parameters from DCIV measurement data, from which a linear or 'modified' hyperbolic tangent approximation of the device's transfer characteristic is derived. From here the voltage and current PA waveform postulator, firstly presented by Cripps [3], has been developed and used to apply waveform engineering concepts in order to identify high power and high efficiency modes of operation. The resulting, postulated, achievable current waveforms are initially used to identify optimum bias conditions and then the required harmonic impedances. In the second stage, waveform device characterization is 'guided' using the postulated target waveforms that have been identified, and these are then used as the basis for the load-pull measurement activity. It will be shown that for well behaved devices, and using postulated data generated from first step, satisfactory measurement results can be achieved very quickly. In fact, for both well-behaved and unpredictable devices, this procedure can give a quick 'first-guess' information for bias voltages and impedances, allowing focused load-pull activity to be quickly conducted. A comparison of output performance achieved using a typical manual measurement procedure, where the optimum target performance has been achieved using accurate but long load-pull measurements, and this high-speed approach using linear and modified tanh approximations of the device's transfer characteristic have been conducted in order to demonstrate the validity of the approach. For this investigation, QinetiQ GaN transistors operating at 0.9GHz of frequency, 15V of drain voltage and delivering 23dBm of output power are used. Measurements have been carried out using the active envelope load-pull (ELP) measurement system[4] developed at Cardiff University.

II. AUTOMATED APPROACH

The first stage of the developed automated approach is based on DCIV measurement data, from which the two approximations of the device's transfer characteristic are derived. Firstly, for the linear approximation, five parameters are extracted to adequately describe the DC boundaries and the device transfer characteristic. Specifically, these are drain voltage (V_{DC}), pinch-off voltage (V_t), saturation drain current (I_{DSS}), knee voltage (V_{knee}) and the transconductance (g_m). For the modified tanh approximation, the addition of empirical parameters termed A, B and C are used, as shown in (3). Once achieved the quick DCIV measured data, these are then utilized by the postulator to predict the required drive, bias voltage and harmonic impedances, as well as the expected time-domain voltage and current waveforms, output power and efficiency for a specific mode of operation.

Drive level and input bias along with the device's boundary conditions play a significant role in shaping the current waveform. In this analysis, input bias is typically swept over a range around the theoretical class-F bias setting, which will be in the region of the device's pinch-off voltage. The relationship between the postulated output current and voltage waveforms dictate the achievable output power and drain efficiency. The link between the input bias and output current waveform is provided by an appropriate choice of the transfer characteristic as shown later in (2) and (3).

For a successful optimization, it is important to accurately specify and weight the targeted output power level. As an example, for a given bias range the predictor may converge towards a class C bias point thus optimizing for very high efficiency at the expense of output power. Once the optimum waveforms are identified by the postulator, the resulting device conditions are uploaded into the time-domain measurement system software, which then replicates in reality the bias, drive, and harmonic loading conditions identified by the postulator. To facilitate accurate comparison with the waveforms measured at the output reference plane established by the measurement system, the predicted waveforms (which are postulated in the absence of extrinsic and intrinsic parasitic effects) are embedded with the effects of the device output parasitic capacitance. For these measurements, a value of C_{DS}=0.04pF was used. It should be noted that the embedding of the parasitic output capacitance is necessary to verify the device performance in terms of output waveforms, as well as to identify the harmonic loads that need to be presented at the device measurement plane.

III. IMPLEMENTATION OF AUTOMATED APPROACH

A. Extraction of DCIV Parameters

For these measurements, the DC drain voltage was fixed at V_{DS}=15V. The knee voltage (V_{knee}) is the point that divides the saturation and the linear region of the device and in terms of time domain waveforms, can be defined as the minimum value of the achievable RF drain voltage. As it can be seen from Fig. 1, V_{knee} can assume any value between 0 and 4V. A correct value can be established by knowing the output RF power (P_{OUT}) which is delivered by the device according to the following equation:

$$P_{OUT} = \frac{1}{2}\frac{(V_{DC} - V_{knee})\cdot I_D}{2} \quad (1)$$

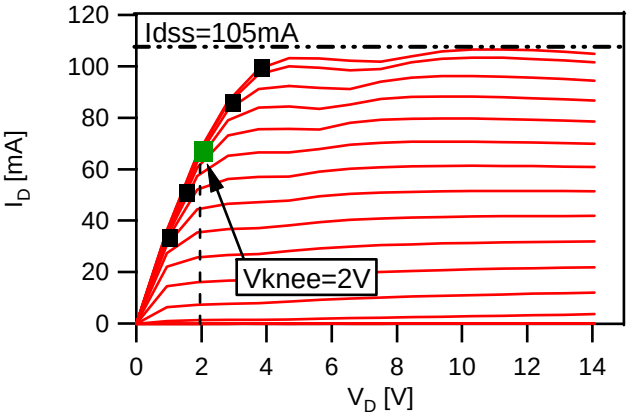

Fig. 1. Measured DCIV.

With reference to equation (1) and Fig. 1, if operating with a knee voltage of 2V, the corresponding maximum drain current is approximately 65mA and achievable output power is approximately 23.2dBm, which in this case is the closest to the datasheet value of 23dBm. The saturation current (I_{DSS}) is the maximum current which the device can deliver, and this parameter can again be easily found from DCIV characteristic shown in Fig. 1. The pinch-off voltage (V_t) is the gate bias voltage where the device starts to conduct current. This value can be obtained from the extracted transfer characteristic. G_m is the transconductance of the device which is identified by the slope of the transfer characteristic. A, B and C are empirical values used to fit as close as possible the modify tanh approximation of the transfer characteristic to the measured one. Table 1 summarizes the DC extracted parameters which are common to both transfer characteristics.

TABLE I
EXTRACTED DC PARAMETERS

V_{DC} [V]	V_t [V]	I_{DSS} [mA]	V_{knee} [V]
15	-5.5	105	2

B. Waveform Engineering Prediction

When using both the linear and hyperbolic tangent approximations of the transfer characteristic, additional DC parameters need to be extracted; example is shown in Table II.

TABLE II
EXTRACTED PARAMETERS FOR DIFFERENT TRANSFER CHARACTERISTIC

Linear	Tanh		
g_m [A/V]	A	B	C
0.43	2.25	0.4	0.316

Using these two simple functions to model the transfer characteristics as shown in (2) and (3), it is possible to generate an idealized three-harmonic class-F voltage waveform (3rd harmonic square waveform) that achieves good postulated results in terms of bias voltage (V_G) and harmonic impedances.

$$I_{D\_linear} = v_g \cdot g_m \cdot I_{DSS}\left[1 - e^{\frac{V_{DS}}{V_{knee}}}\right], \quad (2)$$

$$I_{D\_\tanh} = [(1 + A \cdot \tanh(v_g \cdot B - V_t \cdot C))/2] \cdot 2I_{DSS}\left[1 - e^{\frac{V_{DS}}{V_{knee}}}\right] \quad (3)$$

where v_g is the input voltage.

Fig. 2 shows that the linear function and especially the tanh function in this case offer good approximations to the measured transfer characteristic.

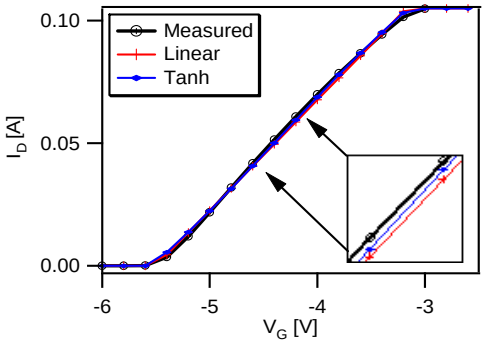

Fig. 2. Measured linear and hyperbolic tangent characteristics.

Using the DC parameters established for the tanh characteristic, the postulator identifies the optimum bias point and harmonic impedances for, in this case a class-F mode of operation. As this mode relies on a half rectified sinusoidal current waveform, the third harmonic current component is significantly suppressed.

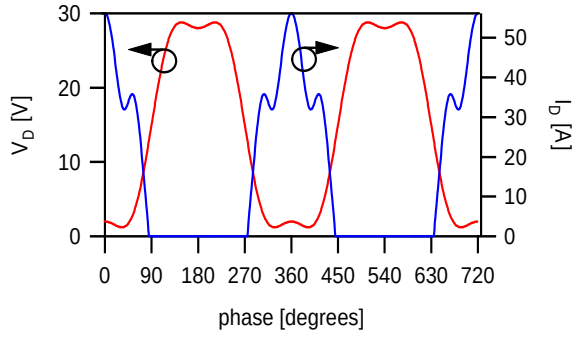

Fig. 3. Predicted class-F voltage and current waveforms at the current-generator plane using the modified tanh characteristic.

The predictor will also develop waveforms such as those in Fig. 3, as well as the expected output power and drain efficiency, shown later in Table VI. Fig. 4 shows the behavior of the third harmonic current as a function of gate bias voltage (V_G) for the two modeled transfer characteristics as well as from direct measurements. It can be seen here that to minimize the third harmonic current (to achieve the half rectified sinusoidal current waveform), the hyperbolic tangent function offers a closer fit to the measured device behavior.

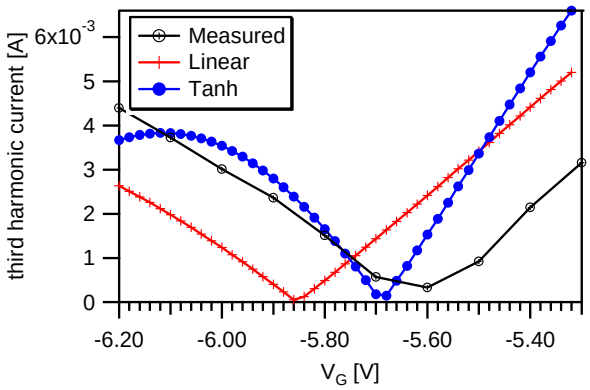

Fig. 4. Third harmonic current amplitude for measured, linear and hyperbolic tangent functions.

In the manually measured case in Fig. 4, the class-F bias point (V_G=-5.6V) is slightly lower than pinch-off (Vt=-5.5V) resulting in a higher value of efficiency still maintaining the expected output power. For both linear and tanh functions, the optimum choice of bias voltage is not the one that exactly minimize the third harmonic current. This is because the aim is to achieve the best trade-off between efficiency and output power. Considering for example the tanh approximation, a bias point of V_G=-5.68 V offers the best postulated efficiency (η=83%), but this is at the expense of lower output power P_{OUT}=22.7dBm. Changing the bias voltage to V_G=-5.64V (shown in Table III) results in a better compromise between efficiency η=82% and higher output power P_{OUT}=23dBm.

TABLE III
IDENTIFIED BIAS VOLTAGE FOR MINIMUM 3RD HARMONIC CURRENT FOR DIFFERENT TRANSFER CHARACTERISTICS

	Measured	***Linear***	***Tanh***
Bias Points	*-5.6 V*	*-5.78 V*	*-5.64 V*

B. Measurements using predicted parameters

Once the required bias voltage and harmonic impedances have been identified as shown in Tables III and IV, the next stage was to use these emulated values directly in the measurement system in order to identify the resulting measured waveforms, output power and efficiency on real devices. Fig. 5 shows the measured and predicted (inset) load-line for both device plane (green line) and output measurement plane (red line). The predicted load-line has been identified using the hyperbolic tangent characteristic approximation. It can be seen that the measured results agree quite well with those predicted. Besides it can be seen that the knee voltage is approximately 2V, as expected.

TABLE IV
FUNDAMENTAL AND HARMONIC IMPEDANCES AT OUTPUT MEASUREMENT PLANE

	Z(f0) [Ω]	***Z(2f0) [Ω]***	***Z(3f0) [Ω]***
Manual	616+j2.96	0+j0.43	0+j954
Linear	630+j91	0+j0	2209+j2131
Tanh	626+j90	0+j0	2152+j1708

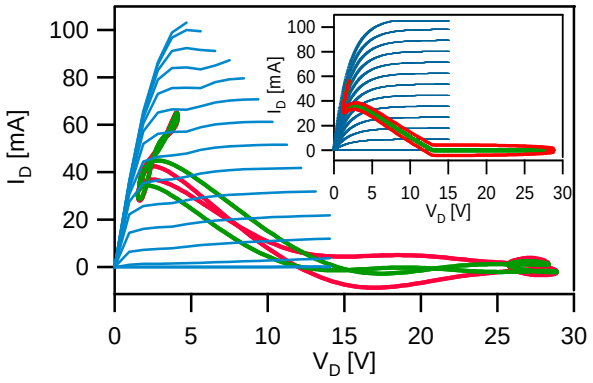

Fig. 5. Measured RF load-line at device current-generator plane (green line) and output measurement plane (red line) with the predicted RF load-line inset.

Similarly, as it can be seen from the measured time domain voltage and current waveform in Fig. 6, there is a good agreement with predicted waveforms of Fig. 3.

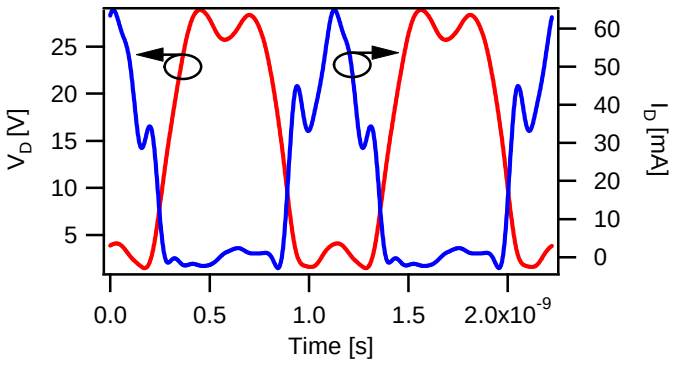

Fig. 6. Measured voltage and current waveforms at the device current-generator plane.

IV. RESULTS AND COMPARISON

Table V shows measurement results achieved using the manual procedure [2], where all target parameters have been obtained using long sweeps directly from the measurement activity without any prediction. Table VI shows predicted results, and measurement results when using the predicted linear and modified tanh approximations. As it can be seen, the new procedure yields device performances that are close to that achieved when using the manually driven approach. Obviously the predicted values will be closer to the measured equivalents for well behaved devices. In any case, an important first guess can be achieved, greatly reducing the time taken to locate these optimums values.

Interestingly, both linear and hyperbolic tangent functions are able to predict bias point and harmonic impedances that show a very good agreement with those identified using the manual approach, thus demonstrating the validity of the approach. For unpredictable devices or higher frequencies, starting from this first guess which gives a zoomed window, load-pull can be conducted for the achievement of the optimum condition.

TABLE V
MANUAL MEASUREMENT RESULTS

	Measurements
Manual	Pout=23.57dBm η = 81.024

TABLE VI
PREDICTED AND MEASURED RESULTS USING PREDICTION

	Prediction	***Measurements***
Linear	Pout=22.93dBm η= 82.71%	Pout= 23.3dBm η = 79.6%
Tanh	Pout=22.96dB η = 82 %	Pout= 23.34dBm η = 80.35 %

V. Conclusion

This paper has demonstrated that armed only with simple DC information describing a real device, it is possible to significantly speed up load-pull measurement activity. The paper emphasizes how the incorporation of simple waveform data, derived from basic set of DC measurements, can have a significant impact in supplying important first-guess measurement data including drive, bias and load condition, improving dramatically the time utilization of the load-pull measurement systems. This work is therefore of high significance to the load-pull measurement community where combining the measurement activity with modeling (albeit simple modeling) knowledge, it is possible to avoid very time consuming, exhaustive measurement activities. Results based upon postulated waveforms show a good agreement with those obtained using a conventional manual search procedure for well behaved devices. Predictions and measurements have been conducted using different geometries of QinetiQ GaN transistors, and TriQuint and RFMD GaAS transistors all giving satisfactory results.

ACKNOWLEDGEMENT

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Publication 4.

Title:

A Novel Highly Efficient Broadband Continuous Class-F RFPA Delivering 74% Average Efficiency for an Octave Bandwidth

Authors:

V. Carrubba, J. Lees, J. Benedikt, P. J. Tasker, S. C. Cripps.

Conference:

IEEE MTT-S Microwave Symposium Digest, pp.1-4, June 2011.

A Novel Highly Efficient Broadband Continuous Class-F RFPA Delivering 74% Average Efficiency for an Octave Bandwidth

V. Carrubba, J. Lees, J. Benedikt, P. J. Tasker, S. C. Cripps

Center for High Frequency Engineering, Cardiff University, Cardiff, CF24 3AA, Wales, UK

carrubbav@cardiff.ac.uk

***Abstract* — A novel, highly efficient and broadband RF power amplifier (PA) operating in "continuous class-F" mode has been realized for first time. The introduction and experimental verification of this new PA mode demonstrates that it is possible to maintain expected output performance, both in terms of efficiency and power, over a very wide bandwidth. Using recently established continuous class-F theory, an output matching network was designed to terminate the first three harmonic impedances. This resulted in a PA delivering an average drain efficiency of 74% and average output power of 10.5W for an octave bandwidth between 0.55GHz and 1.1GHz. A commercially available 10W GaN HEMT transistor has been used for the PA design and realization.**

Index Terms — ***Microwave measurements, microwave theory and techniques, power amplifiers, power transistors, wideband.***

I. INTRODUCTION

The overall efficiency of wireless communication networks is predominantly determined by the power amplifier (PA) stage. Low efficiency generally translates into increased running costs for base stations and reduced battery life for mobile handsets. Linearity is an equally important performance target as it refers to the fidelity of the signal. Once the expected performance is achieved in terms of efficiency and output power, the next step is to address the requirement of increased bandwidth. Wireless communication networks work for different ranges of frequencies, which depend on application and location. The development of emerging 4G (Fourth Generation) multi-purpose wireless communication networks, such as LTE (Long Term Evolution) that provide higher data-rates (downlink peak rates of at least 100Mbit/s and uplink of at least 50Mbit/s) motivates the microwave community to improve PA performance also in terms of bandwidth. In these new communication systems, bandwidth is very important, specifically as it is needed in order to transfer large amount of data over finite communications channels.

Reported results on efficient class-F or inverse class-F power amplifiers [1] have shown that high efficiency states can be achieved for narrow bandwidths, typically less than 10%. In these cases, deviation from the center frequency will degrade efficiency and output power due to the high-Q resonant tuning conditions usually associated with the narrow band modes. In the continuous class-F mode presented here [2], it is shown that it is possible to have multiple impedance solutions, maintaining the expected output performance over a wider design space and hence bandwidth. Critically, this means that it is now possible to achieve the high efficiency associated with conventional class-F designs, without the requirement of presenting narrow band short and open harmonic terminations. As these new solutions provide higher peaks in the voltage waveforms, GaN devices have been used. In recent years, GaN technologies have become very interesting for the development of broadband applications due to the advantages of high voltage operation in comparison with other technologies.

The class-J power amplifier [3] has demonstrated that starting from the class-B mode, it is possible to achieve high efficiency states for a wideband of frequencies when controlling the first two harmonic impedances. The continuous class-F approach demonstrates that starting from the standard narrow band class-F mode and varying the first two harmonic impedances (while keeping the third harmonic termination open-circuited) it is possible to achieve higher efficiency and output power over an even wider bandwidth than class-J mode.

Design has been conducted using the now well-established and accurate non-linear model for the CGH40010 10W GaN (gallium nitride) HEMT (high electron mobility transistor) device from CREE. Based on simulations results, a PA has been realized yielding a very broadband amplifier operating at high efficiency and at output power levels normally associated with the narrow band class-F mode.

II. THE CONTINUOUS CLASS-F MODE ANALYSIS

Recent investigations into this new PA mode [2] have demonstrated that with constant open-circuited third harmonic impedance, the shorted second harmonic termination is not a unique solution for the achievement of optimum efficiency and output power. The required voltage waveforms are defined by equation (1), [2], which has been derived from the generic factorial representation of voltage waveforms, originally derived by Cripps [4]:

$$v(\vartheta)=\left(1-\frac{2}{\sqrt{3}}\cos\vartheta\right)^2\cdot\left(1+\frac{1}{\sqrt{3}}\cos\vartheta\right)\cdot(1-\gamma\sin\vartheta) \qquad (1)$$

Expanding the first two brackets in (1) gives:

$$v(\vartheta)=\left(1-\frac{2}{\sqrt{3}}\cos\vartheta+\frac{1}{3\sqrt{3}}\cos 3\vartheta\right)\cdot(1-\gamma\sin\vartheta) \qquad (2)$$

The first bracket of (2) is the standard voltage formulation for the conventional class-F mode (i.e. with γ=0), which has no second harmonic component. The last bracket of (1) and (2) is a defining term (1- γ sinϑ) that characterizes the new design space. The variation of γ must result in an entirely positive voltage waveform. Zero crossing or negative voltage waveforms will result in interaction with the knee region, and highly non-linear behavior, usually accompanied by reduced power and efficiency. Varying the γ parameter between -1 and 1, a family of voltage waveforms that provide multiple solutions to maintain constant output performance in terms of power and efficiency can be obtained [2]. Over this range of γ, at the device current-generator plane (Igen-plane) the fundamental impedance varies on a circle of constant resistance whilst the second harmonic impedance remains purely reactive, as shown in Fig. 1(a) [2]. The third harmonic impedance is maintained as an open-circuit. A constant half-wave rectified current waveform has also been assumed for all values of γ.

For the conventional class-F mode (γ=0) at 0.9GHz, the simulated input power was swept in order to identify the target 2dB of gain compression. For this compression point (where P_{IN}=20.5dBm) a peak drain efficiency of 86.4% has been obtained with 40.7dBm device output power at a drain voltage of 28V. In accordance with (1) and for the input power previously achieved (P_{IN} @ P2dB), the first three harmonic terminations have been computed at the Igen-plane and then shifted to the device-package measurement plane for γ varying from -1 to 1, as shown in Fig. 1(b).

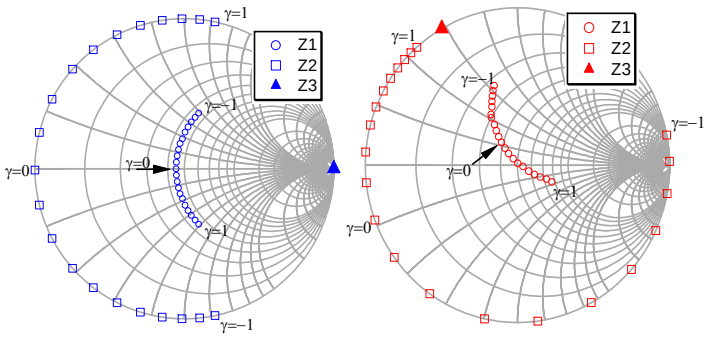
Equations (3) and (4) represent the continuous class-F fundamental and second harmonic impedances at the Igen-plane in order to maintain constant output power and drain efficiency.

$$Z_{F_0} = R_L + j\cdot X_L\,, \qquad (3)$$

$$Z_{2F_0} = 0 - j\cdot\frac{\pi}{2}\cdot X_L \qquad (4)$$

For the 10W GaN HEMT device the fundamental real component impedance is R_L=44.8Ω. To keep a positive voltage waveform, X_L=±38.8Ω are the minimum and maximum values allowed for the reactive fundamental component. Beyond those values of X_L non-linear behavior will be presented. The third harmonic impedance is kept open-circuited at the Igen-plane, resulting in 1∠120° at the package measurement plane.

Fig. 2 shows simulated engineered current and voltage waveforms at the Igen-plane for first three harmonic terminations, for the conventional class-F mode and for the continuous class-F mode for γ =-1.



(a) (b)

Fig. 1. First three harmonic target impedances for the 10W GaN HEMT device at the Igen-plane (a) and at the device-package measurement plane (b).

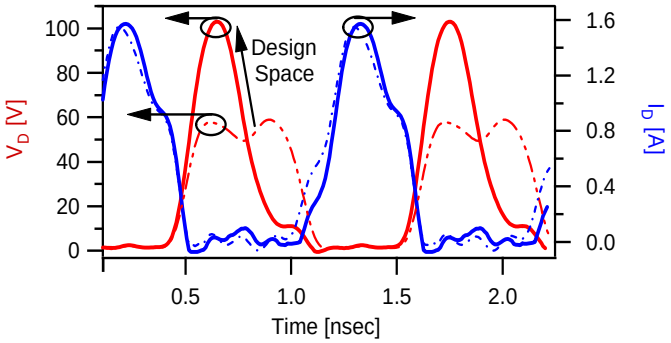


Fig. 2. Simulated current and voltage waveforms at the Igen-plane for a 10W GaN HEMT device for the standard Class-F mode (dotted lines) and "Continuous Class-F" mode (solid lines) for γ=-1.

It can be seen that the current waveform is maintained as half-wave rectified sinusoidal whilst the voltage waveform presents a significantly higher peak value for the continuous mode, which must be accommodated. The approach does however provide a much wider design space where output power and efficiency are maintained constant [2].

III. DESIGN OF BROADBAND CONTINUOUS CLASS-F PA

The PA has been designed using a 10W GaN HEMT transistor and a non-linear CAD approach with the aim of maximizing the drain efficiency whilst delivering the expected output power over significant bandwidth. As efficiency isrelated to the input bias voltage, drive power level and harmonic terminations, an iterative procedure has been applied to rapidly find these parameters [5]. In this case, bias voltage V_G=-4.6V, available input power P_{AVS}=29dBm and harmonic terminations at the package plane shown in section II have been presented.

A. Output matching network design

Target harmonic impedances have been obtained for a single frequency of 0.9GHz with varying γ through the use of equation(1). In PA design, the aim of the output matching network is generally to present the requested terminations

over a specified range of frequencies. Fig. 3 shows the broadband output matching network used for the continuous class-F design.

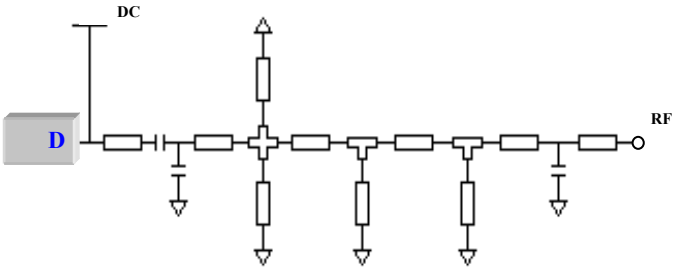


Fig. 3. Continuous class-F output matching network schematic

Fig. 4 shows the target loads and the behavior of the output matching network over a bandwidth of 0.5-1.2GHz. The fundamental component is shown as a solid blue line. The required second harmonic reflection coefficient needs to change rapidly to quickly present high reflection necessary for the continuous class-F mode (green solid/dotted line), whilst the third harmonic component varies around the edge of the Smith chart (black dotted line).

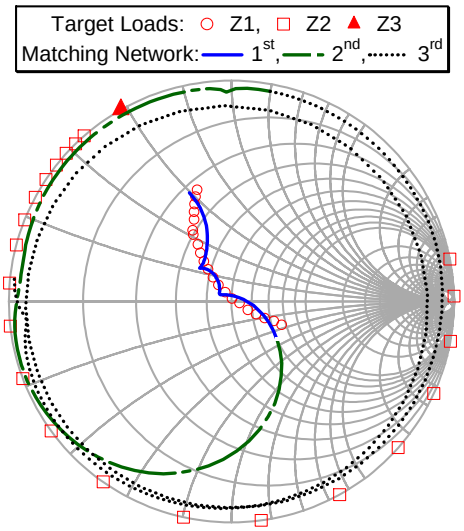


Fig. 4. Target loads and S-parameters for the Continuous Class-F output matching network.

It is important to highlight that the complexity of the matching network (Fig. 3) is mainly due to two aspects: the importance of fitting the network behavior over frequency to the target loads and the accuracy of controlling the third harmonic component. Theoretically the third harmonic impedance should be considered as a constant point (red triangle in Fig. 4), but when designing the matching network for first two harmonics it obviously varies significantly on the Smith chart. To keep expected output performance over the bandwidth, it has been found that the third harmonic termination has to stay as close as possible to the edge of the Smith chart, as shown in Fig. 4.

B. Theoretical Second Harmonic termination inside the Smith chart

When designing and realizing PAs, it is not possible to devise ideal matching networks that present purely reactive impedances, as shown in Fig. 4. This is mainly due to the influence of the assumed broadband 50 Ohm termination. For this reason it is important to establish a target efficiency for which the second harmonic impedance can present a real component without losing too much output performance in terms of power and efficiency.

Equation (5) represents a more general formulation for the continuous class-F mode:

$$v(\vartheta) = (1 - \alpha \cos \vartheta)^2 \cdot (1 + \beta \cos \vartheta) \cdot (1 - \gamma \sin \vartheta) \qquad (5)$$

In this case, varying the parameters α, β and γ it is possible to present second harmonic impedances inside the Smith chart and achieve the correspondent fundamental impedance for which efficiency and output power are maximized. This explains why it is possible to have high efficiency and output power over the bandwidth without perfect short terminations. This is counter-intuitive, but represents an important advance in PA theory. Again, it is important that the voltage waveform is kept above zero to avoid non-linear behavior of the device. Fig. 5 shows the theoretical fundamental and second harmonic impedances as a function of α, β and γ in accordance with (5).

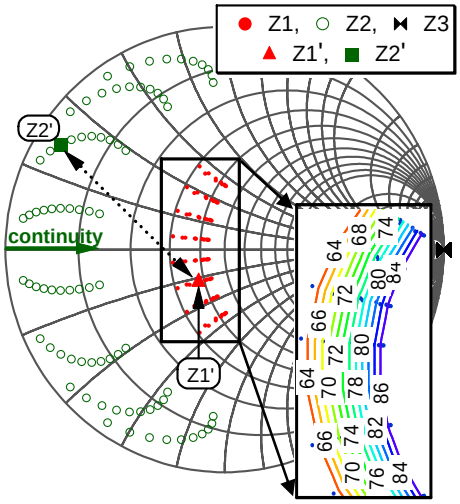


Fig. 5. Extended continuous class-F mode with second harmonic impedance inside the Smith chart with $\beta=\alpha/1.9$ when varying α between 0.6 and 1.5 and γ between -0.7 and 0.7, inset efficiency contour for fundamental load points.

It can be seen that varying the second harmonic termination inside the Smith chart and varying fundamental load in accordance with (5), high efficiency states greater than 64% can still be achieved (i.e. Z1' and Z2' is one optimum combination). The third harmonic impedance is kept open circuited.

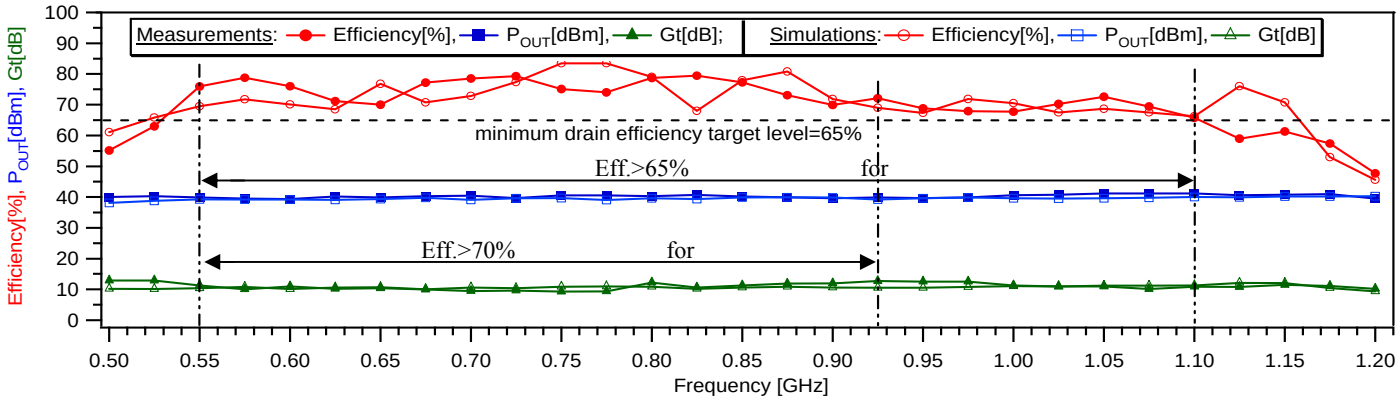


Fig. 6 Measured and simulated drain efficiency, output power and transducer power gain for the realized continuous class-F PA across the bandwidth from 0.5GHz to 1.2GHz.

IV. REALIZATION AND MEASUREMENTS OF THE BROADBAND CONTINUOUS CLASS-F PA

The physical implementation of the continuous class-F power amplifier is shown in Fig. 7. Fig. 6 shows the simulated and measured behavior of drain efficiency, output power and transducer power gain over frequencies ranging between 0.5GHz and 1.2GHz. It can be seen how measured results fit well with simulated results. A minimum target efficiency of 65% was chosen.

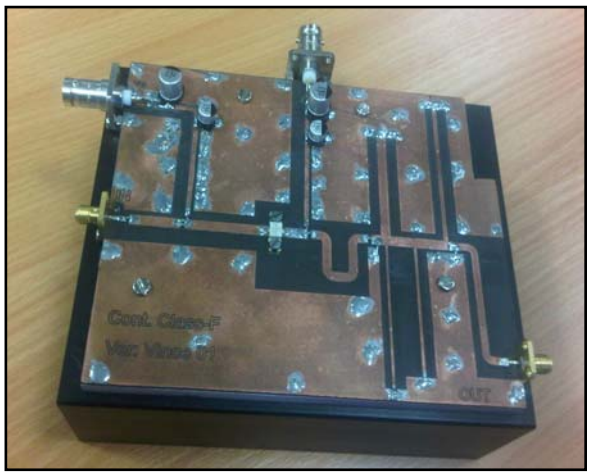


Fig. 7. Realized Continuous Class-F 10W power amplifier.

The realized continuous class-F PA delivers efficiency greater than 65% with maximum peak up to 80% (average efficiency of 74%) over a wide band of frequencies from 0.55GHz to 1.1GHz resulting in an octave (66.6%) bandwidth. In this range of frequencies output power is greater than 39.3dBm with a maximum value of 41.2dBm (average power of 40.2dBm=10.5W). The average transducer power gain is around 11dB, from 9.5dB to 12dB, across the bandwidth. Besides, the PA performance shows that for a smaller range of frequency, ranging from 0.55 to 0.925GHz, higher efficiency greater than 70% is obtained resulting in around 51% of bandwidth.

V. Conclusion

This paper has presented for first time the realization of the "continuous class-F" power amplifier. Using a systematic design process the theoretical identification of continuous class-F fundamental and second harmonic terminations have been carried out over the wide design space. It has been shown that the fabricated continuous class-F PA delivers the expected output power of around 10.5W for a very wide band of frequencies from 0.55GHz to 1.1GHz, resulting in an octave bandwidth. Very high efficiency state from 65% up to 80% (average efficiency of 74%) across the octave bandwidth, and greater than 70% over 51% bandwidth has been obtained. In this work the realization of a highly efficient and broadband PA has demonstrated the validation of the continuous class-F theory.

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Publication 5.

Title:

Exploring the design Space for Broadband PAs using the Novel "Continuous Inverse Class-F Mode"

Authors:

V. Carrubba, A. L. Clarke, M. Akmal, Z. Yusoff, J. Lees, J. Benedikt, S. C. Cripps, P. J. Tasker.

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Exploring the Design Space for broadband PAs using the Novel "Continuous Inverse Class-F Mode"

V. Carrubba, A. L. Clarke, M. Akmal, J. Lees, J. Benedikt, S. C. Cripps, P. J. Tasker

Center for High Frequency Engineering
Cardiff University
Cardiff, Wales, United Kingdom
carrubbav@cardiff.ac.uk

Abstract — **This paper presents a novel formulation for the inverse class-F mode of operation, termed the "continuous inverse class-F mode", resulting in an extended or continuous set of 'allowed' current waveforms. In comparison to the classical inverse class-F mode, this approach provides a much wider design space for the realization of broadband power amplifiers, where output performance can be maintained through the proper termination of harmonic current components over bandwidth. By varying simultaneously the susceptance of fundamental and second harmonic terminations, it will be shown how drain efficiency and output power can be maintained at constant high levels over significant bandwidth. For the validation of this new theory, measurements have been carried out on GaAs pHEMT transistor at 0.9GHz and at a drain voltage of 4V.**

Keywords – inverse class-F mode; microwave measurements; power amplifiers; broadband; high efficiency.

I. Introduction

The evolution of the various operational modes used in microwave power amplifier (PA) design has largely been motivated by the aim to improve efficiency, output power and linearity over relatively narrow operational bandwidths [1]. The challenge now is to maintain the same or better performance over the significant modulation bandwidths demanded by emerging 4G (Fourth Generation) wireless network systems, as well as the desire to provide the mobile communications industry with cost efficient PA architectures that can simultaneously support multiple modulation standards such as GSM, W-CDMA and LTE.

When using classical narrow band modes, such as class-F and inverse class-F [1-2], the optimum drain efficiency and output power is achieved by presenting required singular impedances, generally short-circuit and open-circuit harmonic terminations. In such cases, the high-efficiency states achieved are limited to narrow bands of frequency due to the high-Q matching structures used, and operation too far either side of the center frequency can lead to a rapid decrease in both efficiency and output power. However, recent publications [3-4] have demonstrated that is possible to achieve the same constant output performance in terms of drain efficiency and output power for different combinations of harmonic load condition, increasing the flexibility for PA designers and making very broadband PAs much more realizable, "in press" [5]. This previous work [4] has focused on varying fundamental and second harmonic terminations either side of the class-F case where the fundamental impedance Z_{f0} is tuned fundamental impedance Z_{f0} is tuned for optimum trade-off between power and efficiency and the second harmonic impedance Z_{2f0} is tuned to a short-circuit, whilst the third harmonic impedance Z_{3f0} is maintained at a constant open-circuit. This results in significant and specific 'shaping' of the voltage waveforms whilst the current waveforms are maintained constant. The new work presented in this paper will show, for the first time, how similar performance can be achieved by performing the current waveforms whilst maintaining a constant voltage waveform. In this case, again fundamental and second harmonic terminations have been varied, but this time around an open-circuit second harmonic impedance, whilst the third harmonic impedance is maintained at a short-circuit. Through this new 'continuous' inverse class-F broadband mode, the expected, classical inverse class-F performance can still be achieved, but now over a significant bandwidth.

These different continuous inverted and non-inverted modes of class-F operation have different properties that can be exploited when considered in conjunction with different device technologies for broadband PA design.

II. "Class-J" And "Continuous Class-F" Modes PA Overview

Before exploring the new continuous inverse class-F mode, an overview of the recent activity in the area of broadband PA modes will be presented. The "class-J" [3] and "continuous class-F" [4] modes both present a wide design space through the use of the factorial representation of voltage waveforms, as defined for the first time by Cripps [6].

The conceptual starting point for both the "class-J" and "continuous class-F" mode is the class-B condition, where a half-wave rectified sinusoidal current waveform and sinusoidal voltage waveform are developed at the current generator plane ($I_{gen\text{-}plane}$) within the device. In the class-J mode, maintaining a constant short-circuit third harmonic impedance while varying the fundamental and second harmonic reactances in accordance with the class-J voltage formulation, exposes a wide design space where the expected output power and the theoretical class-B efficiency of 78.5% (assuming infinite harmonic content and three

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harmonic voltages) can be achieved. In the continuous class-F mode, the fundamental and second harmonic impedances have been varied in accordance with the continuous class-F theory, whilst maintaining constant open-circuit the third harmonic impedance. In this case, as the expected conventional class-F mode, constant output power and drain efficiency of 90.7% (assuming infinite harmonic current content and three harmonic voltage content) can be achieved over the expected range of load conditions.

III. The Novel "Continuous Inverse Class-F" Mode of Operation

The work into class-J and continuous class-F PA modes both present a new formulation for the voltage waveform. This means that a constant unchanged half-wave rectified sinusoidal current waveform was assumed by proper input bias condition and input power, therefore the new family of voltage waveforms have been identified by varying the harmonic terminations.

Differently from the class-J and continuous class-F modes, the novel "continuous inverse class-F mode" relies upon a new formulation for the current waveforms shown in (1) whilst the voltage waveform is maintained constant at half-wave rectified sinusoidal.

$$i(\vartheta) = (i_{DC} - i_1 \cos\vartheta + i_2 \cos 2\vartheta + i_3 \cos 3\vartheta)\cdot(1 - \xi \sin\vartheta), \quad (1)$$

where in this case: $i_{DC} = 0.37$, $i_1 = 0.43$, $i_2 = 0$, $i_3 = 0.06$.

It can be seen how the first bracket of (1) represents the classical inverse class-F mode square current waveform for the first three harmonic components. The second bracket represents the "key operator" where by varying □, a new design space for fundamental and second harmonic loads can be revealed, as shown in Fig. 1. Importantly, this mode delivers output power and drain efficiency equivalent to that

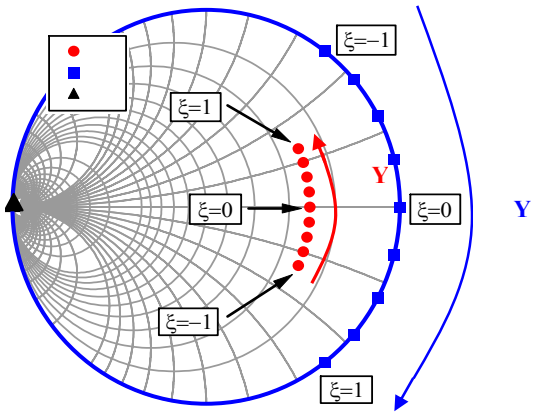

Figure 1. Admittance chart for the theoretical "continuous inverse class-F" admittances range for the first three harmonic loads, when varying -1≤ξ≤1 with steps of 0.25.

of the standard narrow band inverse class-F mode, allowing the achievement of wider bandwidth.

The admittance Smith chart in Fig. 1 shows that, with a constant Y3, when varying the second harmonic admittance Y2 around the perimeter in accordance with (1), the corresponding fundamental admittance Y1 varies on a circle of constant susceptance. It is important to highlight that when using this new inverse mode, it is not longer a requirement for PA designers to attempt to engineer a perfect, 'singular' open circuit for the second harmonic.

Fig. 2 shows the theoretical current waveforms for the new "continuous inverse class-F" mode. These waveforms are achieved by assuming the admittance conditions explained previously and shown in Fig. 1 together with a constant three harmonic half-wave rectified sinusoidal voltage waveform. By varying ξ, the new design space is revealed, characterized by higher peak values in the current waveforms. It is important to highlight that for this mode to work successfully, non-zero crossing current waveforms are essential. This property is achieved by ensuring that the parameter ξ is limited to variations between -1 and 1. If ξ is set beyond that range, the current drops below zero resulting in strongly non-linear behavior coupled with a significant reduction in power and efficiency.

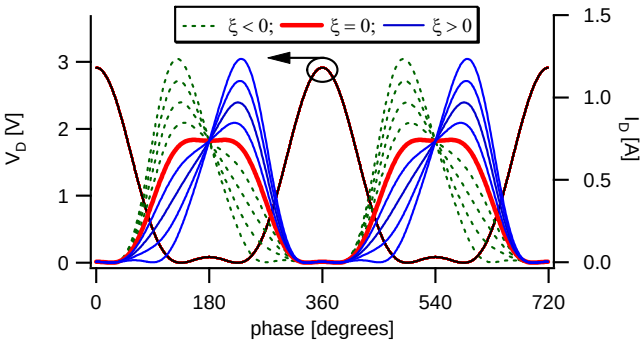

Figure 2. Theoretical continuous inverse class-F current and voltage waveforms for -1≤ξ≤1 with steps of 0.2.

For the case where ξ=0, a classical inverse class-F current waveform is obtained, as shown centrally highlighted in red in Fig. 2. Assuming three harmonic content for both current and voltage waveforms, this delivers a theoretical drain efficiency of 81.85%. The new family of current waveforms is presented for the other values of ξ, either side of ξ=0. It should be noted that when varying the harmonic terminations as a function of ξ, the shape of the voltage waveform would normally be expected to vary. For this analysis, this has been avoided through small adjustments of the input drive, and for each load condition, the output voltage has been restored to its original half-wave rectified sinusoidal shape. Being able to control the current waveform through adjustment in fundamental and second harmonic impedance may seem counter-intuitive at first, but in real devices, such variations can have a big impact on both voltage and current waveforms as they are both related by the knee region, as shown in (2) [1].

$$i_d(\vartheta) = v_g \cdot g_m \cdot I_{\max}\left(1 - e^{-(v_{ds}/V_{knee})}\right), \quad (2)$$

where v_g represents the input voltage (bias and drive), g_m is the device's transconductance, I_{max} represents the device's saturation current and V_{knee} is the knee voltage. As it can be seen from (2), when V_{knee}=0 (ideal transistor), the drain current is only function of the input voltage v_g and of the device's characteristics (g_m and I_{max}). This means that the device behaves as an input voltage controlled current source. When dealing with real transistors, the knee voltage is not zero, and the drain current will be function of the drive, the drain voltage as well as the fundamental and harmonic impedances giving rise to the output voltage waveform.

Therefore, when varying the harmonic impedances, if the output voltage waveform can be maintained constant through proper variation of the input drive, the current waveform can be controlled in such a way to allow this new mode to exist.

The powerful concept of this new current formulation is that, by simply varying the single parameter ξ, and by slightly adjusting the input power, the correct harmonic admittances that allow a constant output performance to be maintained can be identified.

Although varying this parameter causes fundamental and second harmonic admittances to vary, both fundamental and second harmonic conductances will be maintained constant. Therefore, assuming a constant voltage waveform, a constant output power over a wide range of ξ will be maintained. As DC current and voltage components will also be maintained constant, this leads to constant drain efficiency as well.

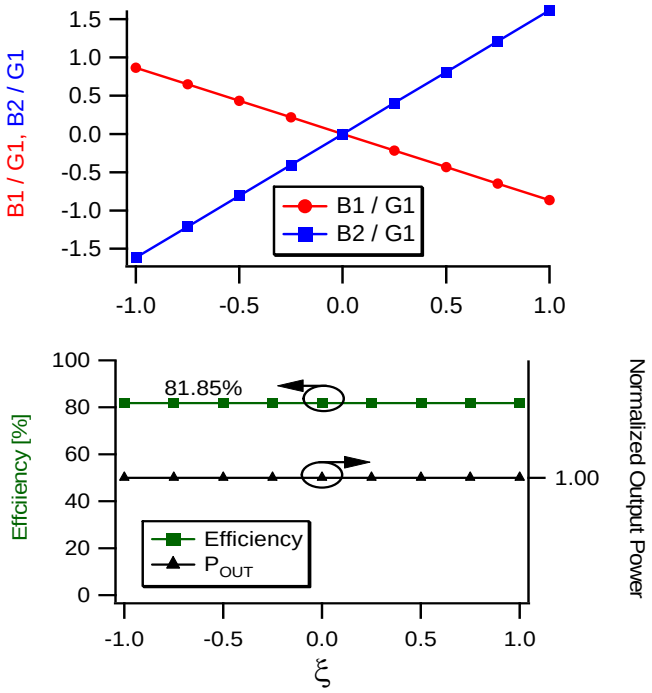

Figure 3. Theoretical fundamental and second harmonic susceptances (B1 and B2) both normalised to the fundamental conductance (G1) and efficiency and output power function of ξ, for -1≤ξ≤1 with steps of 0.25.

Fig. 3 shows the behavior of fundamental and second harmonic susceptances B1 and B2, both normalized to the fundamental conductance G1, as well as output power and efficiency as a function of ξ. It can be seen that increasing ξ from -1 to 1, the required fundamental susceptance decreases whilst the second harmonic susceptance increases. Choosing simultaneously those points of fundamental and second harmonic susceptances (with third harmonic load kept ideally as a short-circuit) a constant output power (here normalized to unity) and a drain efficiency of 81.85% are maintained over the entire range of ξ.

IV. Measurements And Results

The active load-pull measurement system developed at Cardiff University [7] has been used for the experimental validation of this new theory. Measurements have been carried out on a wafer-probeable transistor from TriQuint, at a fundamental frequency of 0.9GHz and 4V of drain voltage.

A. The Novel Current Waveforms

The standard narrow-band inverse class-F mode produces a peak output voltage of $\pi*V_{DC}$ and as the breakdown voltage of this device is known to be in the region of 12V, a drain DC voltage of 4V has been used. In the standard case (where ξ=0), and for the device used in this experiment, the optimum trade-off between power and efficiency is found for a drain DC quiescent current around 35mA. As shown in Fig. 4, this corresponds to an RF current swing that does not extend up to I_{max}, because of the increasing V_{min} in the knee region. Now, for this device, when dealing with the new continuous inverse class-F mode, (i.e. for ξ=±1, dotted load-lines in Fig. 4), it is possible to utilize the full current drive capability without compromising efficiency.

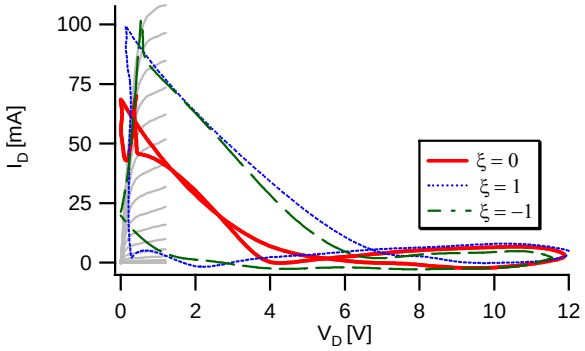

Figure 4. Measured DCIV and RF load-line for ξ=0 (red highlighted solid line), for ξ=1(blue dotted line) and for ξ=−1 (green dotted line).

The process implemented in [8] has been used in order to obtain an optimized standard inverse class-F design. An initial gate bias and input power sweep has been conducted in order to achieve the right bias voltage. For the standard inverse class-F mode, the bias voltage has been chosen in order to minimize the second harmonic current component which is typically around the class-A bias point. For the device used, V_G=-0.45V has been chosen. As measurements have been conducted at the device's $I_{gen-plane}$, a short-circuit third harmonic impedance and an open-circuit second harmonic impedance has been provided, whilst the fundamental impedance has been swept. In order to achieve the best trade-off between output power and drain efficiency, a fundamental load impedance of Z_l=165+j*0Ω has been chosen where output power P_{OUT}=19.4dBm and drain efficiency η=78.7% have been obtained. Drive power during the fundamental sweep was such that the device was approximately 3dB into gain compression. On establishing the conventional inverse class-F mode, the parameter ξ is swept, presenting the harmonic terminations that produce the new set of current waveforms as shown in Fig. 5.

For the standard inverse class-F mode (waveform in red highlighted), a maximum drain current of around 70mA has been achieved. With the new continuous current waveforms, as already explained in previous section, a increased current area can now be explored allowing the realization of the wide design space but without sacrificing any output power or more importantly drain efficiency. Whilst varying the

parameter ξ, the drive power was adjusted in order to maintain the constant half-wave rectified sinusoidal voltage waveform.

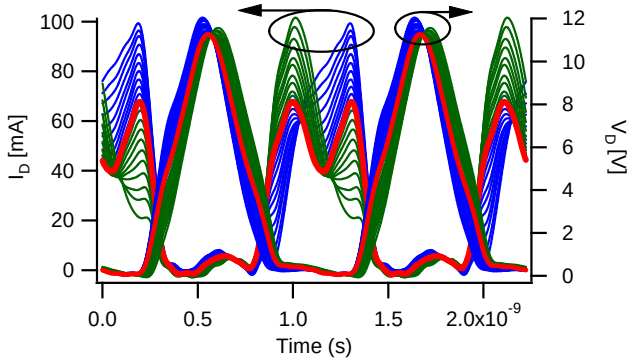

Figure 5. Measured current waveforms for -1≤ξ≤1 with steps of 0.1.

Fig 6 shows the resulting measured source available power (P_{AVS}), transducer power gain (G_T), drain efficiency (η) and output power (P_{OUT}) as a function of ξ, which means as a function of the harmonic loads of Fig. 1. The small variation of the gain is due to the variation of the input power in order to maintain constant the output voltage waveform. Output power and efficiency are maintained constant at around 20dBm and 79-80% respectively, over the entire range of ξ.

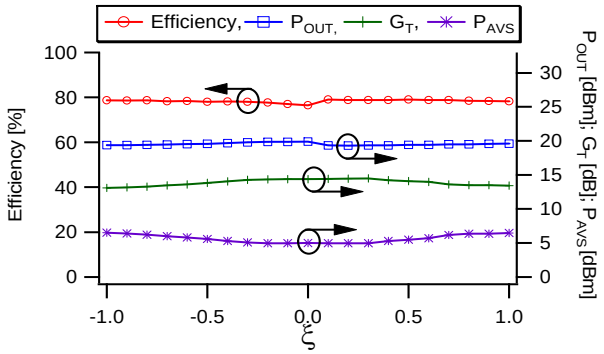

Figure 6. Measured source available power P_{AVS}, drain efficiency η, output power P_{OUT} and transducer power gain G_T for -1≤ξ≤1 with steps of 0.1.

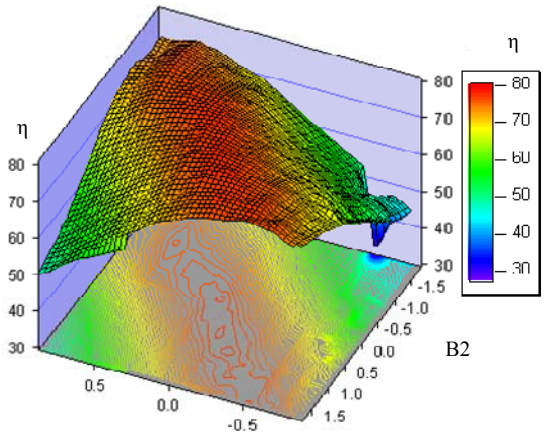

Figure 7. Measured drain efficiency as a function of fundamental and second harmonic susceptances (B1 and B2) normalised to the fundamental conductance (G1), measured for constant input power.

Fig 7 shows the measured drain efficiency surface plot as a function of different combinations of fundamental and second harmonic susceptances. A maximum constant efficiency of

about 79-80% is achieved for the entire range of ξ ranging between -1 to 1, for which the inverse relationship of B1 and B2 is valid in accordance with (1). When presenting different load combinations, for example B1 and B2 both positive or both negative, the device performance clearly degrades.

V. Conclusion

This paper has presented for the first time the continuous inverse class-F mode. The new way to present the current waveform unifies the conventional narrow band inverse class-F PA with this novel mode. It has been demonstrated that varying just one parameter of the current formulation, combinations of the harmonic terminations that maintain constant output performance can be achieved. Varying the second harmonic load from the open-circuit and changing simultaneously the fundamental susceptance in accordance with the newt current formulation a wider design space that maintain constant drain efficiency and output power are obtained. The possibility to have multiple solutions allows easier way to design broadband PAs. Measurements demonstrated that constant drain efficiency of around 79-80% and output power of 20dBm has been achieved over the wide design space.

Acknowledgment

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Publication 6.

Title:

Inverse Class-FJ: Experimental Validation of a New PA Voltage Waveform Family

Authors:

V. Carrubba, J. J. Bell, R. M. Smith, M. Akmal, Z. Yusoff, J. Lees, J. Benedikt, P. J. Tasker, S. C. Cripps.

Conference:

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Inverse Class-FJ: Experimental validation of a New PA Voltage Waveform Family

V. Carrubba[*#], J. J. Bell[*], R. M. Smith[*], M. Akmal[*], Z. Yusoff[*], J. Lees[*], J. Benedikt[*], P. J. Tasker[*], S. C. Cripps[*]

[*]*Center for High Frequency Engineering, Cardiff University, Cardiff, CF24 3AA, Wales, UK*

[#]*Fraunhofer Institute for Applied Solid State Physics (IAF), Tullastrasse 72, 79108 Freiburg, Germany*

vincar80@alice.it

***Abstract* — This paper presents for the first time an experimental validation of the continuous inverse class-F mode with varying the voltage waveforms, also known as inverse class-FJ. Starting from the standard inverse class-F condition and varying fundamental and third harmonic impedances whilst maintaining an open-circuit second harmonic load it will be demonstrated that output power and drain efficiency can be maintained at near constant values. For the validation of the approach, experimental measurements have been conducted on-wafer on a GaAs pHEMT device operating at 4V supply voltage and 0.9GHz fundamental frequency. The experimental results show that output power of 19.3-19.6dBm and drain efficiency of 75-80% can be maintained for different sets of fundamental and third harmonic impedance solutions, which can then be translated in a useful design space for designing broadband power amplifiers.**

***Index Terms* — broadband amplifiers, design methodology, energy efficiency, microwave circuits, microwave amplifiers.**

I. INTRODUCTION

Power Amplifier (PA) designers have in recent decades focused on improving the transistor efficiency (η), output power (P_{OUT}), gain (G) and linearity. High power efficiency is required in order to increase mobile phones battery life and minimize CO_2 emissions. High gain can reduce the number of stages required, thus minimizing manufacturing costs. High linearity is required for communication signals transmission. All these targets have been so far improved for a narrow band of frequencies. In this case different PA modes can be used in order to perform different services at different frequencies. The next step is to achieve all the targets so far explained: η, P_{OUT}, G and linearity but for a wideband of frequencies. In this case a single PA could be used to cover different frequencies, reducing overall costs. The new formulation of the voltage waveform for the achievement of multiple harmonic impedance solutions, the so called "design space", has been discovered by Cripps [1]. Subsequently, many different modes have been identified by applying the design space concept: Class-J [2], Class-BJ [3], Continuous Class-F [4]. Extended work on the continuous class-F mode shows that it is possible to maintain a certain pre-determined high efficiency value by varying the second harmonic impedance inside the Smith chart away from the short-circuit condition [5].

For all these modes, the current waveform is maintained constant while the new formulation has been applied to the voltage waveform, identifying the design space.

Another mode, which has already been identified as "Continuous Inverse Class-F" [6], shows that this concept can also be applied to the current waveform. In this case the voltage waveform is maintained constant and the new family of waveforms is achieved on the current side. Being able to control the current waveforms through adjustment in fundamental and second harmonic impedances (while the 3rd harmonic load is kept short-circuited) seems counter-intuitive at first, but in real devices such variations can have a significant impact on both voltage and current waveforms as they affect the interactions with the knee region [1]. In this case by simultaneously varying fundamental and second harmonic loads and by slightly adjusting the input power (depending on the device's characteristics) the new family of current waveforms can be identified [6].

Another paper [7] shows a new version of the continuous inverse class-F, called inverse class-FJ. Here, differently from [6] the new formulation has been applied to the voltage waveform. In that case only the theoretical analysis has been reported.

This paper will show the experimental verification of the inverse class-FJ explained theoretically in [7] by performing measurements on-wafer on a 20dBm GaAs transistor at 4V supply voltage and 0.9GHz fundamental frequency.

II. THEORETICAL INVERSE CLASS-FJ

For the continuous inverse class-F mode, in this case called inverse class-FJ, the current waveform is maintained as a constant square wave, whilst the new formulation is applied to the voltage waveform, as shown in (1):

$$v_{F^{-1}J}(\vartheta) = \left[\frac{1}{\sqrt{2}} - \cos(\vartheta)\right]^2 \cdot [1 - \alpha \sin(\vartheta)]$$

$$= \left[1 - \sqrt{2}\cos(\vartheta) + \frac{1}{2}\cos(2\vartheta)\right] \cdot [1 - \alpha \sin(\vartheta)] \quad (1)$$

For α=0 the second bracket of (1) will be equal to 1, this means that the standard inverse class-F mode with the harmonic limited half-wave rectified sinusoidal voltage waveform is achieved (first bracket).

When varying the parameter α, a new family of voltage waveforms is identified, while maintaining the ideal square current waveform as shown in Fig. 1.

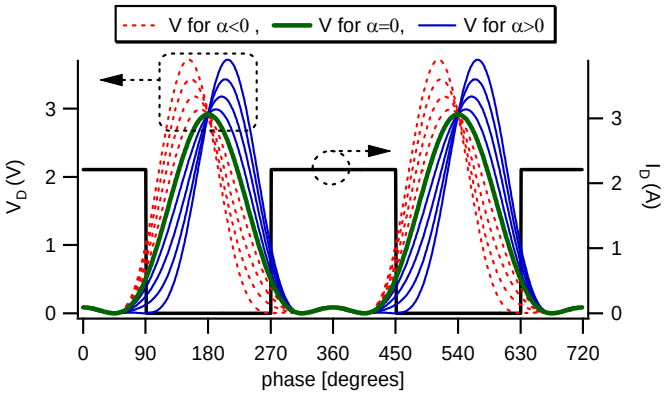

Fig. 1. Inverse Class-FJ current and voltage waveforms for α varying $-1 \leq \alpha \leq 1$ in steps of 0.25.

To ensure that the voltage waveforms remain positive, α must be varied in the range $-1 \leq \alpha \leq 1$. If α goes beyond that range, the voltage waveform drops lower than zero resulting in a drastic reduction in power and efficiency. All the voltage waveforms shown in Fig. 1 will have the same optimized output power and drain efficiency of the classic inverse class-F mode [7]. Fig. 2 shows the reactive parts of fundamental and third harmonic impedances as well as drain efficiency and output power normalized to unity. It can be noted that when increasing α, the required fundamental reactance decreases while the third harmonic reactance increases (the second harmonic load is kept open-circuited). Choosing simultaneously those points of fundamental and third harmonic reactances (with $R_{F0}=R_{OPT}$ and $R_{3F0}=0$) constant output power (normalized to unity) and efficiency (in this case η=81.9%, considering three harmonic contents in both voltage and current waveforms) can be achieved for all the range of α ranking between -1 and 1.

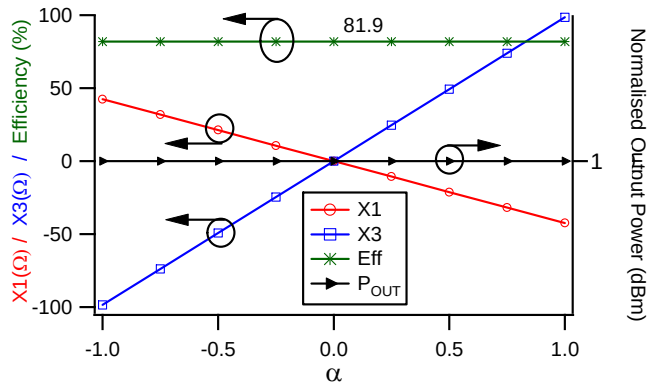

Fig. 2. Theoretical fundamental and third harmonic reactances, output power and drain efficiency function of α varying between -1 and 1 in steps of 0.25.

By applying a Fast Fourier Transform (FFT) and dividing the harmonic voltage components with the appropriate harmonic current contents (from the square waveform) the fundamental and harmonic impedances can be calculated [7].

Fig. 3 shows the first 3 harmonic impedances when considering a 50Ω fundamental resistance. It is important to remember that when varying α, the fundamental impedance develops an imaginary component while the resistive component is ideally maintained at constant value, which in this case is considered to be 50Ω. The second harmonic impedance is kept open-circuited.

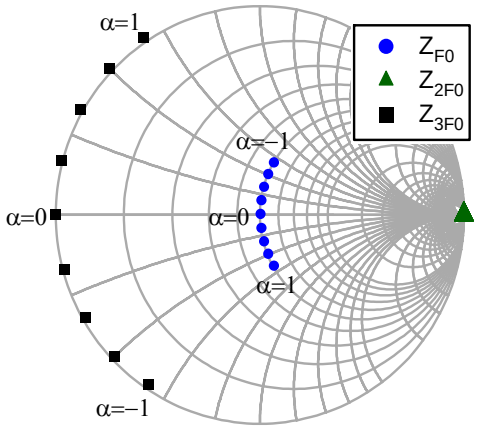

Fig. 3. Inverse Class-FJ first three harmonic impedances for α varying $-1 \leq \alpha \leq 1$ in steps of 0.25, when optimum fundamental resistance R_{F0}=50Ω.

III. MEASUREMENT VALIDATION

The theoretical analysis reported in detail in [7] and briefly described on section II of this paper has been applied experimentally on a 20dBm GaAs power transistor at 4V drain voltage and 0.9GHz fundamental frequency. The measurements have been carried out on the active envelope load-pull (ELP) system developed at Cardiff University [8].

The first set of measurements was performed in order to achieve the standard inverse class-F state. Following the inverse class-F measurement procedure [9], bias voltage of V_{GS}=-0.8V, $Z_{F0}=0.53\angle 0°$, Z_{2F0}=open-circuit and Z_{3F0}=short-circuit have been identified at the device current-generator plane [10] by de-embedding the drain-source capacitor C_{DS}=0.3pF.

For those values of bias voltage, fundamental and harmonic loads, a drain efficiency of η=78.4%, output power P_{OUT}=19.3dBm and available gain G_{AV}=15dB (≈3dB of gain compression) have been achieved. From this starting point the parameter α was then varied. Fig. 4 shows drain efficiency, output power, available gain and available input power (P_{AVS}) with varying α. Output power is maintained almost at constant level around 19.5dBm (from 19.3 to 19.6dBm) for all the range of α. The drain efficiency is maintained greater than 75% for $-0.5 \leq \alpha \leq 1$ with a maximum peak value of 80.1% for α=0.4, but starts degrading for α<-0.5. The maximum value of gain G_{AV}=15dB is achieved when α=0, which then decreases with α, down to around 10dB. This is due to the fact that with varying α, the input power (P_{AVS}) needs to be adjusted in order to maintain the square current waveform as shown in Fig. 4.

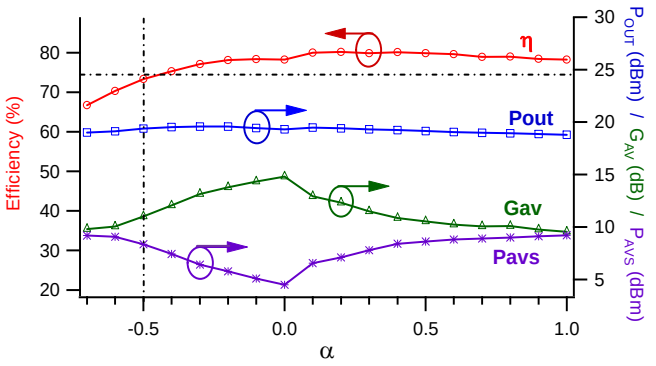

Fig. 4. Measured Inverse Class-FJ drain efficiency, output power, available gain and available input power for α varying between $-0.7 \leq \alpha \leq 1$ in steps of 0.1.

Theoretically output power and efficiency should remain constant for all the range of α as shown in [7]. Here, measurements demonstrate that the output performance degrades towards the edges of the α range, in this particular case the drain efficiency degrades when varying α with negative sign and especially below -0.5. This can be due to the interaction with the knee region, the non-unilateral characteristic of the device, the feedback capacitor as well as the non-ideal de-embedding. In this on-wafer device, only the drain-source capacitor C_{DS} needed to be de-embedded, but when working with package devices it is very important to use a de-embedding network as accurate as possible in order to follow the right line of constant resistance when varying α.

The plots in Fig. 5 and 6 show the measured inverse class-FJ voltage and current waveforms for α varying between -0.7 and 1 in steps of 0.1.

As it can be seen, the inverse class-FJ voltage waveforms vary with changing α. The harmonic limited half-wave rectified sinusoidal voltage waveform is achieved when α=0 (blue waveform) with maximum peak at around 12V being for the inverse class-F mode $V_{peak}=\pi*V_{DC}$ where V_{DC}=4V. When varying the parameter α, the new family of voltage waveforms are achieved with higher peak-to-average ratio (PAR), giving the new design space.

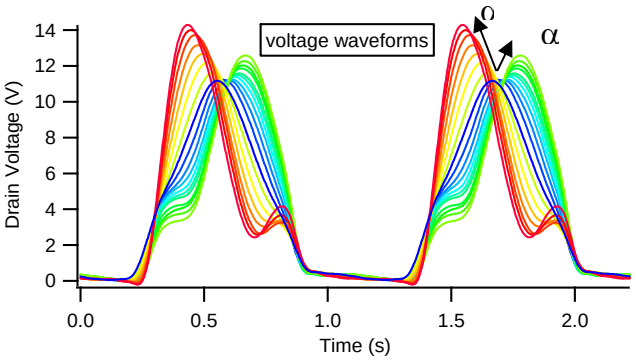

Fig.5. Measured Inverse Class-FJ voltage waveforms for α varying between $-0.7 \leq \alpha \leq 1$ in steps of 0.1.

The measured current waveforms are maintained with an almost constant level of around 70mA by adjusting the input power when moving towards the edges of α.

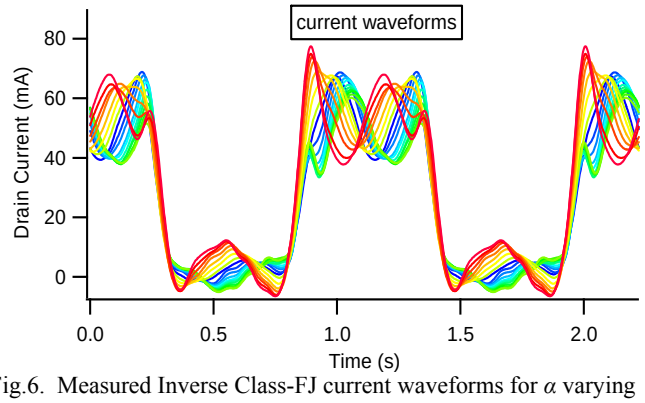

Fig.6. Measured Inverse Class-FJ current waveforms for α varying

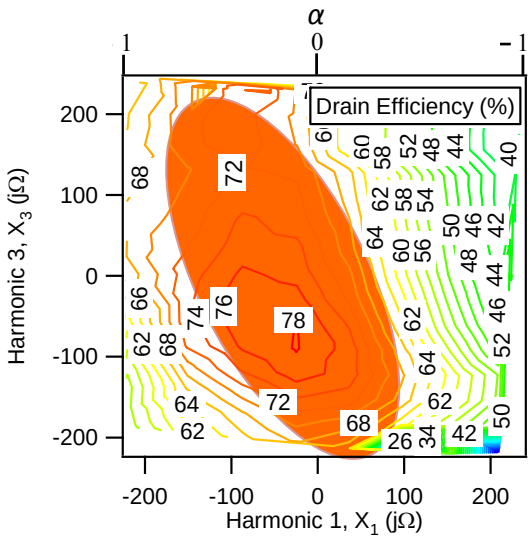

Fig. 7. Measured drain efficiency as a function of X_1 and X_3 for constant input power.

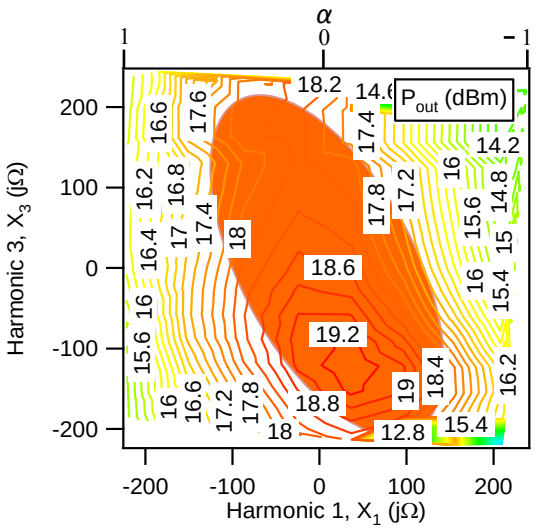

Fig.8. Measured output power as a function of X_1 and X_3 for constant input power.

To provide more insight, contours have been plotted over the entire design space function of fundamental and third harmonic impedances as shown in Fig. 7 and 8. For these measurements the second harmonic load is kept open-circuited and the input drive power is kept constant.

These figures do not show the actual optimum device behavior as shown in Fig. 4 because as already mentioned the input power was maintained at constant value. Nevertheless, it can still be seen that the best behavior is obtained when fundamental reactance X_1 is positive and third harmonic reactance X_3 is negative and vice-versa (approx.), as highlighted in orange.

IV. OBSERVATION

The first important observation is that these new continuous/broadband modes increase flexibility when designing narrow band PAs. This is because we do not need to provide the perfect open-circuit and short-circuit second and third harmonic impedances, but by choosing (in this case) reactive third harmonic load and by adjusting the fundamental impedance in accordance with the theoretical formulation constant output performances can be achieved. Secondly, the possibility of having multiple load solutions is translated into a wide "design space" in terms of frequency when designing PAs. This allows the design of high power efficiency and broadband PAs, as demonstrated in [11].

V. CONCLUSION

This paper has presented for the first time the experimental validation of the "continuous inverse class-F" mode with varying the voltage waveforms, also called "inverse class-FJ". It has been demonstrated that when varying reactively the third harmonic impedance around the edge of the Smith chart from the short-circuit and by adjusting simultaneously with opposite sign the reactive part of the fundamental impedance, constant output power and drain efficiency can be maintained over a wide design space. The measurements show that when dealing with real devices, the output performance is not perfectly maintained constant over the entire α design space as many other components must be taken into account such as feedback, non-unilateral device characteristic and de-embedding issues. However, it has been demonstrated that output power of 19.3-19.6dBm and drain efficiency of 75-80% can be maintained for a very wide range of impedances solutions.

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Publication 7.

Title:

The Continuous Inverse Class-F Mode with Resistive Second Harmonic Impedance

Authors:

V. Carrubba, M. Akmal, R. Quay, J. Lees, J. Benedikt, S. C. Cripps, P. J. Tasker.

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The Continuous Inverse Class-F Mode with Resistive Second Harmonic Impedance

Vincenzo Carrubba, *Member, IEEE*, Muhammad Akmal, *Member, IEEE,* Rüdiger Quay, *Senior Member, IEEE*, Jonathan Lees, Johannes Benedikt, Steve C. Cripps, *Fellow, IEEE,* and Paul J. Tasker, *Senior member, IEEE*

Abstract — **In this paper, an extended version of the continuous class-F^{-1} mode power amplifier (PA) design approach is presented. A new formulation describing the current waveform in terms of just two additional parameters, while maintaining a constant half-wave rectified sinusoidal voltage waveform, allows multiple solutions of fundamental and second harmonic impedances that provide optimum perform to be computed. By varying only the imaginary parts of fundamental and second harmonic impedances, it is shown that output performance in terms of power and efficiency is maintained constant and equal to that achievable from the standard class-F^{-1}. Indeed, when presenting resistive second harmonic impedances, it will be demonstrated that the fundamental load can be adjusted to maintain satisfactory output performances greater than a certain pre-determined target value. The measurements, conducted on a GaAs pHEMT device at 1 GHz, show a good agreement with the theoretical analysis, revealing drain efficiencies greater than 70% for a very large range of load solutions, which can translate to an ability to accommodate reactive impedance variations with frequency when designing broadband PAs.**

***Index Terms*—Broadband amplifiers, microwave devices, microwave measurements, power amplifiers, radio frequency.**

I. INTRODUCTION

CELLULAR phone technology has improved considerably over time. During the last decades different narrow band power amplifier (PA) modes have been theoretically and experimentally explored [1-2] and further developed [3]. Through the use of waveform engineering and by knowing the different drain voltage and current waveforms, it is possible to define the transistor operation modes. Therefore, by shaping those waveforms, output power, gain and efficiency can be optimized. However, the standard modes starting from the linear class-A to the high-efficiency class-F or inverse class-F (class-F^{-1}) perform for the singular frequency solution [1-6]. The world ongoing standards 3G (third generation) have driven the research on what will be the new emerging 4G (fourth generation) such as LTE-Advanced (Long Term Evolution Advanced) [7]. In these new emerging high quality wireless communication standards one of the main aim is to provide higher data rates, around 100Mb/s for high mobility communication such as from cars and trains and 1 Gb/s for low mobility communication such as pedestrians or when stationary [8]. Such standards are not only characterized by higher data rates, but they are also characterized in terms of user capacity and advanced services. This means that the optimum output performance required from the power amplifier for the singular frequency needs to be now obtained for a wide band of the spectrum frequency. Therefore, broadband and/or multiband power amplifiers for which the overall output performance is optimized are nowadays required and under continuous development. Different techniques have been so far adopted for the realization of both multiband [9-10] and broadband power amplifiers [11-15]. Furthermore, recent investigations have shown theoretical analysis supported by experimental results [16-20] as well as actual PA realizations [21-26] where the fundamental and harmonic loads can be varied properly from the optimum condition still maintaining the requested output performance.

This paper presents for the first time an extended mathematical formulation applied to the inverse class-F mode allowing the proper match of fundamental and harmonic impedances. Starting from the standard inverse class-F state for which optimum fundamental impedance, open-circuit second harmonic load and short-circuit third harmonic termination are required, by varying properly such impedances it will be demonstrated that the output performance does not change significantly. More specifically, by moving the second harmonic termination inside the Smith chart (resistive second harmonic load from the open-circuit condition), thus varying the magnitude and phase of such harmonic and adjusting properly the magnitude and phase of the fundamental load in accordance with this new theory, satisfactory output power and drain efficiency are achieved. The third harmonic termination is maintained fixed at short-circuit.

The possibility of applying the different theories termed "continuous modes" [16-20] on both the inverted and non-inverted classes of operation have different advantages which can be exploited with different technology, device´s size and different operating frequencies.

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Vincenzo Carrubba and Rüdiger Quay are with the Fraunhofer Institute for Applied Solid State Physics (IAF), Tullastrasse 72, 79108, Freiburg, Germany.

The other co-authors are with the Centre for High Frequency Engineering, Cardiff School of Engineering, Cardiff University, CF24 3AA, Cardiff,U.K(e-mails:vincenzo.carrubba@iaf.fraunhofer.de; akmalm1@cardiff.ac.uk; leesj2@cardiff.ac.uk; Benedikt@cardiff.ac.uk; Ruediger.Quay@iaf.fraunhofer.de; ; stevehywave@aol.com; tasker@cardiff.ac.uk).

For the device size, the choice of using the inverted or non-inverted mode depends of the ratio between the harmonics and fundamental impedances as demonstrated here [27]. In terms of frequency, if the device presents low f_T but high operating frequency is required, the non-inverted mode would be a preferable choice. This is due to the fact that only first two impedances need to be optimized while the third harmonic termination would probably be short-circuited due to the drain-source capacitor C_{DS}.

The paper is organized as follows. Section II presents briefly the theoretical analysis of the (a) standard inverse class-F and (b) continuous inverse class-F mode where varying the second harmonic impedance only on the edge of the Smith chart. Furthermore, a detailed new extended theoretical analysis based on the continuous inverse class-F mode with varying both the reactive and resistive parts of fundamental and second harmonic impedances are presented in Section II (c). The measurement system has been described in Section III A and practical measurements on a power transistor are presented in Section III B. Finally conclusions are given in Section IV.

II. Standard, Reactive Continuous, and Resistive-Reactive Continuous Inverse Class-F Modes

The inverse class-F PA requires a square current waveform and a half-wave rectified sinusoidal voltage waveform at its intrinsic current-generator plane. These waveforms are achieved by presenting the optimum fundamental impedance Z_{F0} (function of the device-under-test DUT), open-circuit second harmonic load Z_{2F0} and short-circuit third harmonic termination Z_{3F0}. The constant values of the fundamental and harmonic impedances lead to an optimised inverse class-F PA for the given fixed frequency.

Recent investigations [16-20] have shown that it is actually possible to move the second and/or third harmonic impedance from the short-circuit and/or open-circuit condition by proper variation of the fundamental load, exploiting a new design space.

Equation (1) shows the standard half-wave rectified sinusoidal voltage waveform *v(φ)* (second harmonic peaking), while (2) shows the new formulation for the current waveform *i(φ)*.

$$v(\vartheta)=\left(\frac{1}{\sqrt{2}}+\cos\vartheta\right)^2=1+\frac{2}{\sqrt{2}}\cos\vartheta+\frac{1}{2}\cos 2\vartheta, \tag{1}$$

$$i(\vartheta)=\left(i_{DC}-i_1\cos\vartheta+i_3\cos 3\vartheta\right)\cdot \cdot\left(1+\alpha\cos\vartheta\right)\cdot\left(1-\gamma\sin\vartheta\right). \tag{2}$$

Where i_{DC}, i_1 and i_3 represent the DC, fundamental and third harmonic current components respectively when α=γ=0. The parameters α and γ are empiric parameters which will describe the new design space. The voltage waveform is normalized to unity.

As it can be noted, the voltage waveform is not a function of either α and γ while the current waveform will vary with such parameters.

Expanding equation (2) gives:

$$i(\vartheta)=\left(i_{DC}-\frac{\alpha}{2}i_1\right)+(\alpha i_{DC}-i_1)\cos\vartheta+\gamma\left(\frac{\alpha}{4}i_3+\frac{\alpha}{4}i_1-i_{DC}\right)\sin\vartheta+$$

$$+\frac{\alpha}{2}(i_3-i_1)\cos 2\vartheta+\frac{\gamma}{2}(i_3+i_1-\alpha i_{DC})\sin 2\vartheta+i_3\cos 3\vartheta+$$

$$+\gamma\frac{\alpha}{4}i_1\sin 3\vartheta-\frac{\gamma}{2}i_3\sin 4\vartheta-\gamma\frac{\alpha}{4}i_3\sin 5\vartheta\cdot \tag{3}$$

Where:

$$I_{DC}=i_{DC}-\frac{\alpha}{2}i_1, \tag{4}$$

$$\mathrm{Re}al(I_1)=\alpha\cdot i_{DC}-i_1, \tag{5}$$

$$\mathrm{Re}al(I_2)=\frac{\alpha}{2}(i_3-i_1), \tag{6}$$

$$\mathrm{Re}al(I_3)=i_3, \tag{7}$$

$$\mathrm{Im}ag(I_1)=\gamma\left(\frac{\alpha}{4}i_3+\frac{\alpha}{4}i_1-i_{DC}\right), \tag{8}$$

$$\mathrm{Im}ag(I_2)=\frac{\gamma}{2}(i_3+i_1-\alpha\cdot i_{DC}), \tag{9}$$

$$\mathrm{Im}ag(I_3)=\gamma\frac{\alpha}{4}i_1, \tag{10}$$

$$\mathrm{Im}ag(I_4)=-\frac{\gamma}{2}i_3, \tag{11}$$

$$\mathrm{Im}ag(I_5)=-\gamma\frac{\alpha}{4}i_3\cdot \tag{12}$$

I_{DC} represents the quiescent current. *Real(I_1,I_2,I_3)* (equations from 5 to 7) represent the real part of the current components of the fundamental, second and third harmonic impedances, and *Imag(I_1,I_2,I_3,I_4,I_5)* (equations from 8 to 12) represent the imaginary part of the current components of the fundamental, second, third, fourth and fifth harmonic impedances. The real parts greater than three and the imaginary parts greater than five are equal to zero.

(a) Standard Inverse Class-F (Γ=1; Phase=0)

When the parameters α=γ=0, as it can be noted from (3) and from equations from (4) to (12), all the imaginary parts are equal to zero as well as the real part of the second harmonic current termination Real(I_2), thus equation (3) leads to the first bracket of (2). Here the optimum fundamental load, open-circuit second harmonic load and short-circuit third harmonic termination are presented as shown in Fig. 1 (admittance points for γ=0). These impedances reveal the standard inverse class-F square current waveform and the second harmonic peaking half-wave rectified sinusoidal voltage waveform as shown in black and red respectively in Fig. 2.

(b) Reactive Continuous Inverse Class-F (Γ=1; Phase≠0)

Keeping α=0 and varying the parameter γ, the second harmonic termination varies reactively on the edge of the Smith chart from its open-circuit condition while the fundamental impedance varies on its circle of constant susceptance with an inverse relationship as shown in Fig. 1 (as well as in Fig. 3). It is important to highlight that for this mode to work successfully, non-zero crossing current waveforms are essential, which means that the parameter γ has to vary between -1 and 1.

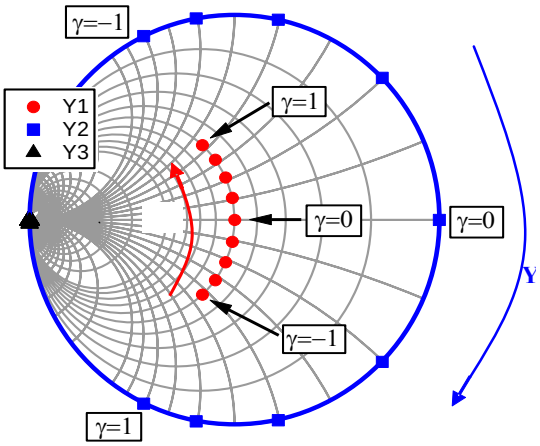

Figure 1. Admittance chart for the theoretical continuous inverse class-F admittances range for the first three harmonic loads, when varying -1≤ γ ≤1 in steps of 0.25.

The proper variation of fundamental and second harmonic load (with keeping a constant short-circuit third harmonic termination) leads to the waveforms shown in Fig. 2. Here, for γ>0 and γ<0 the family of continuous current waveform is shown (blue and green respectively) defining the new design space. Although varying the parameter γ causes the required fundamental and second harmonic susceptances to vary, both fundamental and second harmonic conductances remain constant. Therefore, assuming a constant voltage waveform, a constant optimum output power (in Fig. 3 normalised to unity) over a wide range of γ can be maintained. As DC current and voltage components will also be maintained constant, this leads to constant drain efficiency as well, which in this case is 81.85% as three harmonic contents are considered in both voltage and current waveforms as shown in Fig. 3. Note that B1 and B2 are inversely proportional in order to maintain a constant output power and efficiency.

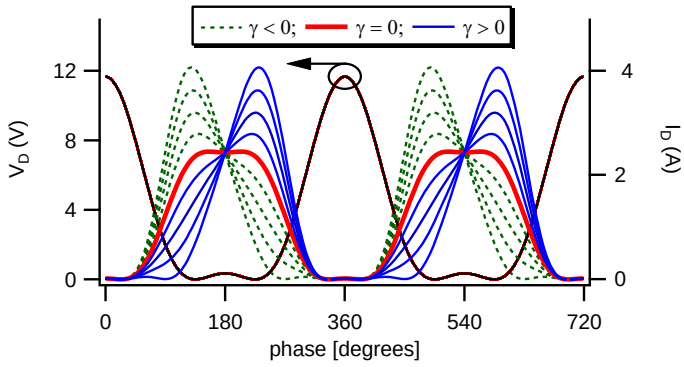

Figure 2. Theoretical continuous inverse class-F current and voltage waveforms for -1≤ γ ≤1 in steps of 0.25.

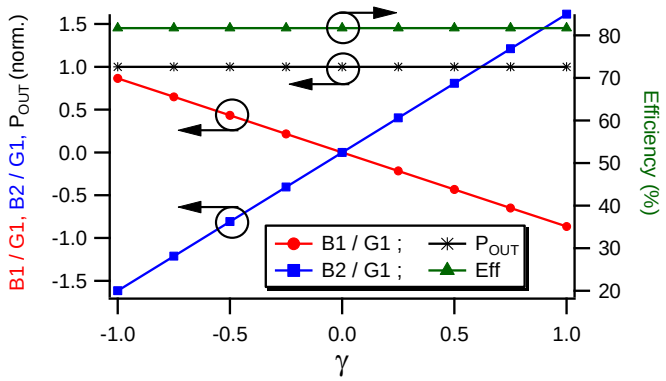

Figure 3. Theoretical fundamental and second harmonic susceptances (B1 and B2) both normalized to the fundamental conductance (G1) and efficiency and output power (normalized to unity) for -1≤ γ ≤1 in steps of 0.25.

(c) Reactive-Resistive Continuous Inverse Class-F (Γ<1; Phase≠0)

As shown so far, despite the reactive variation of the fundamental impedance, if adjusting properly the second harmonic impedance on the perimeter of the Smith chart (Γ=1, Phase≠0) the optimum inverse class-F output power and efficiency can still be maintained constant.

However, when dealing with real PAs, it is not possible to realize ideal matching networks with reflection coefficient equal to unity. This means for instance that the harmonic impedances (in this case the second harmonic load) cannot be maintained as a perfect open-circuit.

For this reason, the new mathematical formulation taking into account and varying both parameter α and γ is presented. When varying γ and including the parameter α≠0 a new enlarged design space that the authors have termed reactive-resistive continuous inverse class-F mode (or extended continuous inverse class-F mode), where fundamental and second harmonic loads can now both be located inside the Smith Chart is presented, as shown in Fig. 4. When varying the second harmonic load inside the Smith chart (α>0) the output performance start to slowly degrade, but by properly adjusting the fundamental load in accordance with (2), useful performance in terms of power and efficiency can still be achieved. Fig. 5 shows the theoretical computed new family of current waveforms as a function of both parameters α and γ. The current waveform amplitudes decrease with increasing α. This is due to the fact that by increasing α, the fundamental impedance also increases in accordance with equation (2), therefore maintaining a constant half-wave rectified sinusoidal voltage waveform, the current waveforms then must decrease in magnitude. Besides, it can be noted that if considering the standard class-F^{-1} (α=0, red waveforms), when increasing α, bigger troughs in the waveforms are developed. As already mentioned earlier, the parameter γ and now also α must be varied between -1 and 1 to maintain a non-zero crossing current waveforms. It can be seen from Fig. 6 that drain efficiency varies with α, but it would be maintained constant with varying γ. However, it is important to highlight that in order to present a positive second harmonic impedance (inside the Smith chart), the parameter α should be constrained between 0 and 1.

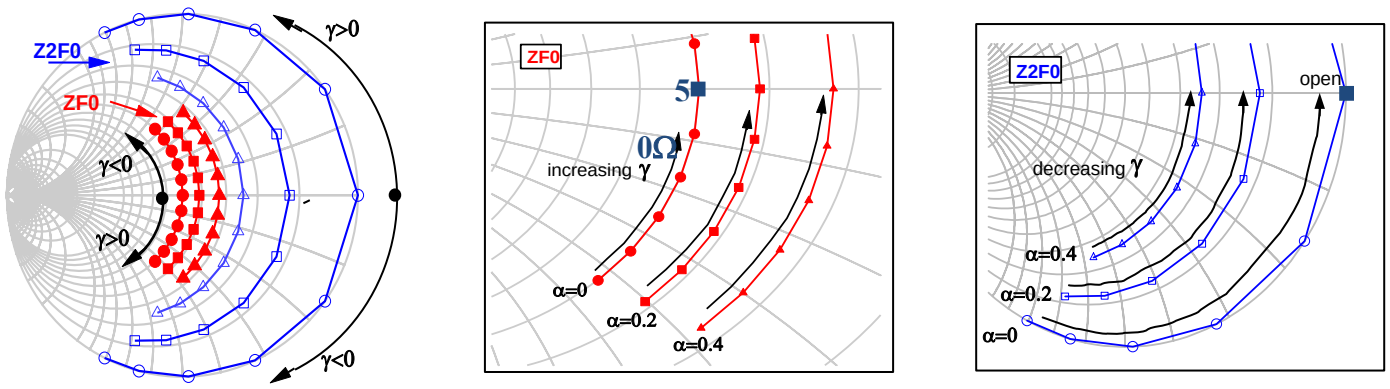

Figure. 4. Extended Continuous Class-F^{-1} for the first two harmonic impedances (third harmonic load is kept short-circuited) when varying -1 ≤ γ ≤ 1 and 0 ≤ α≤ 0.4 both in steps of 0.2.

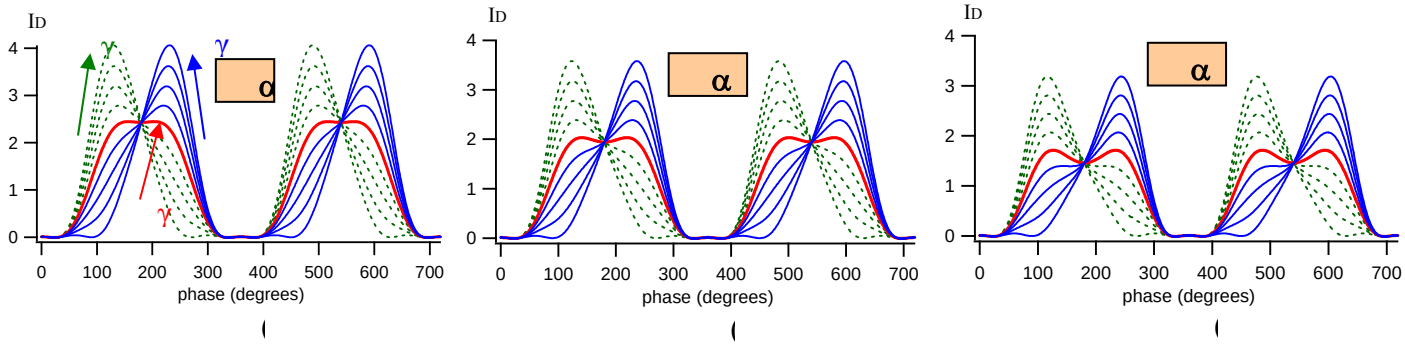

Figure. 5. Theoretical extended continuous class-F^{-1} current waveforms when varying -1 ≤ γ ≤ 1 in step of 0.25 and 0 ≤ α ≤ 0.4 in steps of 0.2.

This is because for negative values of α, -1 < α < 0, the current waveform will still be positive, but negative second harmonic impedances need to be presented in order to allow the continuous mode to exist.

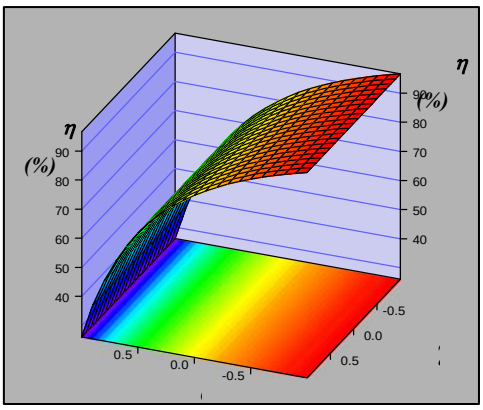

Figure 6. Theoretical efficiency (η) contour plot function of α and γ with both been varied between -1 and 1.

Fig. 7 shows the variation of efficiency as a function of α with a constant value of γ=0. It can be seen that for α=0 the standard class-F^{-1} with drain efficiency (η) of 81.85% is obtained. When increasing α, the value of efficiency starts to decrease, but considering a certain pre-determined target minimum value of efficiency, in this case η=70% has been chosen thus given a maximum value for α=0.4, a very large range of impedances can be obtained maintaining efficiencies greater than 70%. The small degradation in efficiency is traded-off against the advantage of having multiple solutions in order to facilitate the design of broadband PAs. It should be noted that for α<0 the efficiency increase from its optimum 81.85% ´up to almost 100%. This is due to the fact that for α<0 in accordance with (2) negative second harmonic impedances are presented [28]. For the analysis and measurements presented in this paper, only positive values of α have been considered.

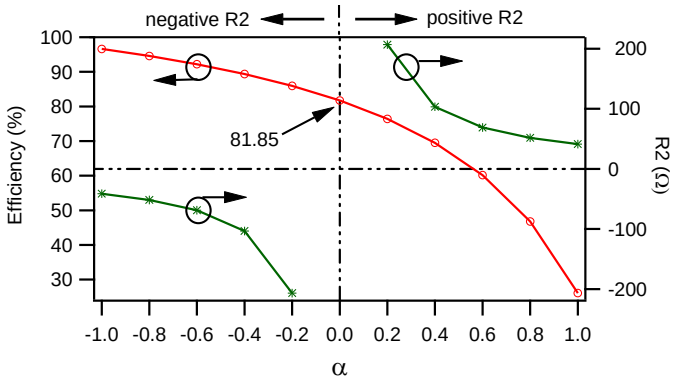

Figure 7. Theoretical efficiency and second harmonic resistance function of α with –1 ≤ α ≤ 1 in steps of 0.2, for constant γ = 0.

Table I shows the reflection coefficient of both fundamental and second harmonic impedances as a function of α, for 0 ≤ α ≤ 0.4 with step 0.1, for a constant value γ=0 and considering a 50 Ω optimum fundamental load for the standard class-F^{-1}.

TABLE I

REFLECTION COEFFICIENTS (Γ) OF FUNDAMENTAL AND SECOND HARMONIC IMPEDANCES AS A FUNCTION OF ALPHA

	α=0	***α=0.1***	***α=0.2***	***α=0.3***	***α=0.4***
|Γ| @ Z_{F0}	0	0.046	0.096	0.15	0.21
|Γ| @ Z_{2F0}	1	0.78	0.61	0.46	0.34

The phases of both Z_{F0} and Z_{2F0} are all equal to zero for the different values of α, as in this case a constant value γ=0 has been considered (impedances on the real axes of the Smith chart). Besides, as it can be seen from both Table I and Fig. 4, starting from the standard class-F^{-1} condition (α=0) where Z_{F0}=50 Ohm (0∠0°) and Z_{2F0}=open-circuit (1∠0°), increasing the value of α, the fundamental load goes toward higher impedances whilst the second harmonic load goes inside the Smith chart. The third harmonic impedance is kept constant at a short-circuit.

III. Experimental Measurements

A. Measurement system description

The design space defined theoretically in the previous sections has been explored experimentally using the active envelope load-pull (ELP) measurement system developed at Cardiff University [29].

The measurement system configuration using the ELP architecture is shown in Fig. 8. This system is based on the Microwave Transition Analyzer (MTA) sampling scope demonstrated by M. Demmler et al. [30].

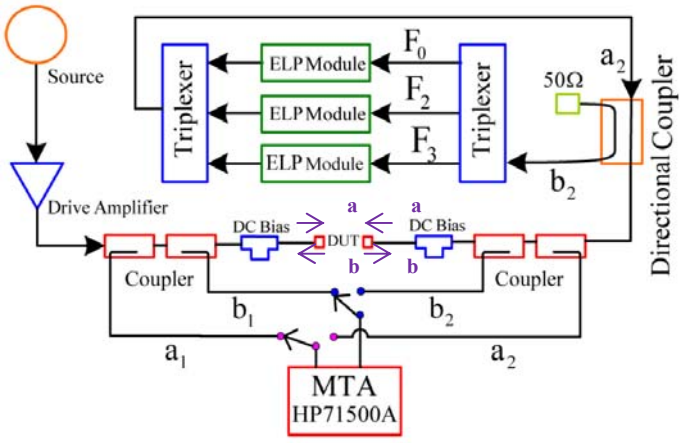

Figure 8. Measurement system architecture in the active envelope load-pull (ELP) configuration.

The input signal is provided by a Synthesised Sweeper Source (83640A), delivering power up to 25dBm. Here a linear broadband drive power amplifier (PA) is necessary for delivering the required power to the input of the DUT. As it can be seen, the input signal a_1 is coupled using a broadband directional coupler where additional attenuators could be used in order to reduce the overall power sent to the MTA ports to less than the maximum safe power allowed (in the order of 0 dBm). A test set of switches is used allowing the two channel MTA to operate as a four channel receiver measuring the overall incident and reflected travelling waveforms. Channel 1 is used to measure both the incident waves at the input a_1 and output a_2 of the DUT while channel 2 is used to measure the reflective waves b_1 and b_2 determined by the direction of the switches. The DC biasing of the device is achieved by using two bias tees, one at the input and one at the output of the DUT, with a current capability of 0.5A at the RF bandwidth from 45MHz to 40GHz. For higher power (current) capability hybrid couplers can be used. In this case the DC signal can still go through the bias tee joining then the RF signal which can go through the hybrid coupler. The fundamental and harmonic impedances are presented by using the ELP technique [29]. In this technique, the device transmitted signal b_2 flows through the directional coupler with the aim of isolating the transmitted wave b_2 with the injected signal a_2. The transmitted signal b_2, which is rich in harmonic content, is then divided into the three harmonics F_0, F_2 and F_3 through an appropriate triplexer and the three signals can therefore flow into the ELP modules. A detailed analysis and explanation of the ELP configuration can be found in [29].

It is important to highlight that the continuous theory presented in this paper can be experimentally explored by using different harmonic load-pull systems [31-33], being the main target of this work to present the appropriate terminations. Active harmonic load-pull systems would give better performance if compared with the passive load-pull systems as the high harmonic terminations can be easily presented with reflection coefficient Γ=1 (on the edge of the Smith chart) necessary for the high efficiency states. For the passive load-pull systems, reflection coefficient equal to unity cannot be achieved, leading to degradation to the overall performance. This is primarily due to the fact that any losses introduced between the device itself and the load-ull system will reduce the maximum magnitude of the modified signal a_2, limiting the range of load impedances that can be presented. However, recent works have demonstrated passive load-pull systems with Γ near to unity [34-35].

B. Measurement results

The measurements have been carried out on a 20dBm GaAs transistor from TriQuint at 4V of drain voltage and 1GHz of fundamental frequency.

The standard narrow-band class-F^{-1} mode produces a peak output voltage of $\pi*V_{DC}$ and with the breakdown voltage of this device known to be in the region of 12V, a drain DC voltage of 4V has been used. In the standard case (where α=γ=0), and for the device used in this experiment, the optimum trade-off between power and efficiency was found for a drain DC quiescent current around 35mA. As it can also be noted from Fig. 9, this corresponds to an RF current swing up to around 65mA which is not the maximum achievable because of the increasing V_{min} in the knee region. Now, for this device, when dealing with the new continuous inverse class-F mode, it is possible to utilize the full current drive capability without compromising efficiency. The process implemented in [36] has been used to obtain an optimized standard class-F^{-1} design. An initial gate bias and input power sweep has been conducted in order to achieve the right bias voltage. For the standard class-F^{-1} mode, the optimum bias voltage has been chosen in order to minimize the second harmonic current component, which is typically around the class-A bias point. For the device used, V_G=-0.45V has been chosen. As measurements have been conducted at the device's current generator plane, a short-circuit third harmonic impedance and an open-circuit second harmonic impedance has been provided, whilst the fundamental impedance has been swept. To achieve the best trade-off between output power and drain efficiency, a fundamental load impedance of Z_1=150+j*0 Ω has been chosen at the device current-generator plane, after de-embedding a drain source capacitor C_{DS}=0.23pF [37].

Fig. 9 shows the measured standard inverse class-F voltage and current waveforms for different input power (at the device intrinsic plane) while Fig. 10 shows the measured drain efficiency and available gain function of the output power sweep. Drain efficiency of η=80.1%, gain of G_{AV}=17.9dB and output power of P_{OUT}=19.2dBm have been obtained at approximately 3dB of gain compression.

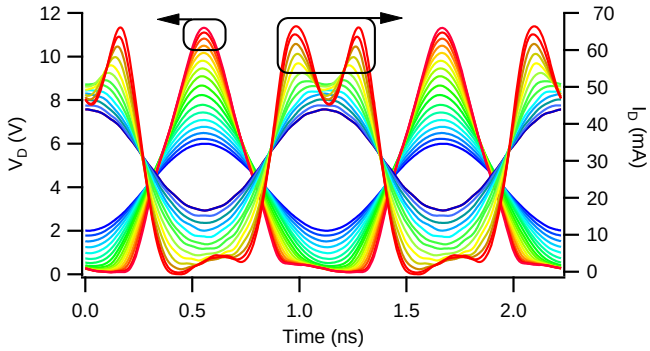

Figure 9. Measured inverse class-F voltage and current waveforms function of input power.

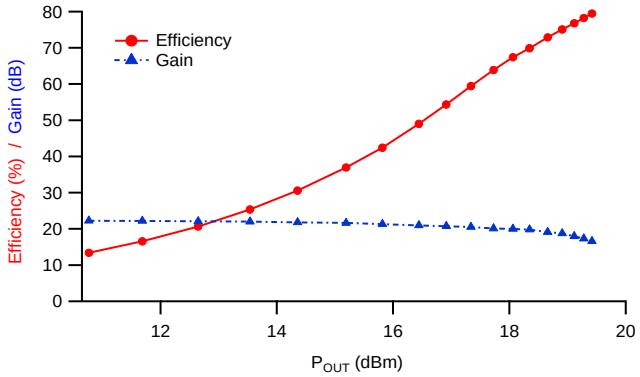

Figure 10. Measured inverse class-F efficiency and available gain function of output power sweep.

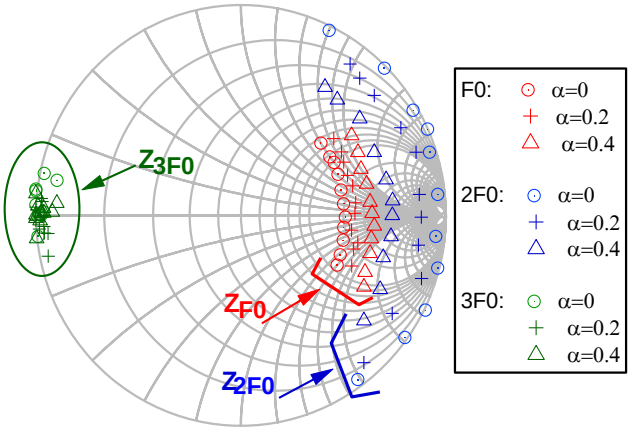

Figure 11. Measured extended continuous inverse class-F range of fundamental (red) second (blue) and third (green) harmonic loads for α=0 (circles), α=0.2 (crosses) and α=0.4 (triangles).

Once the conventional class-F^{-1} mode was established, at around the 2-3dB of compression the parameters α and γ have been varied and the new solutions of fundamental and second harmonic loads have been identified as shown in Fig. 11. The third harmonic load is kept around the short-circuit point.

Fig. 12 shows the measured current and voltage waveforms for the impedance points presented in Fig. 11, which means for $0 \le \alpha \le 0.4$ and for $-1 \le \gamma \le 1$ with both steps of 0.2; besides the load-lines for $0 \le \alpha \le 0.4$ with step of 0.2 and for $-1 \le \gamma \le 1$ with step of 1 are also presented. As predicted in the theoretical waveforms (Fig. 5), when increasing the parameter α, the achievable maximum peak current waveform decreases.

Again, the waveforms for γ=0 (red ones) show bigger troughs with increasing α, consistent with theoretical predictions.

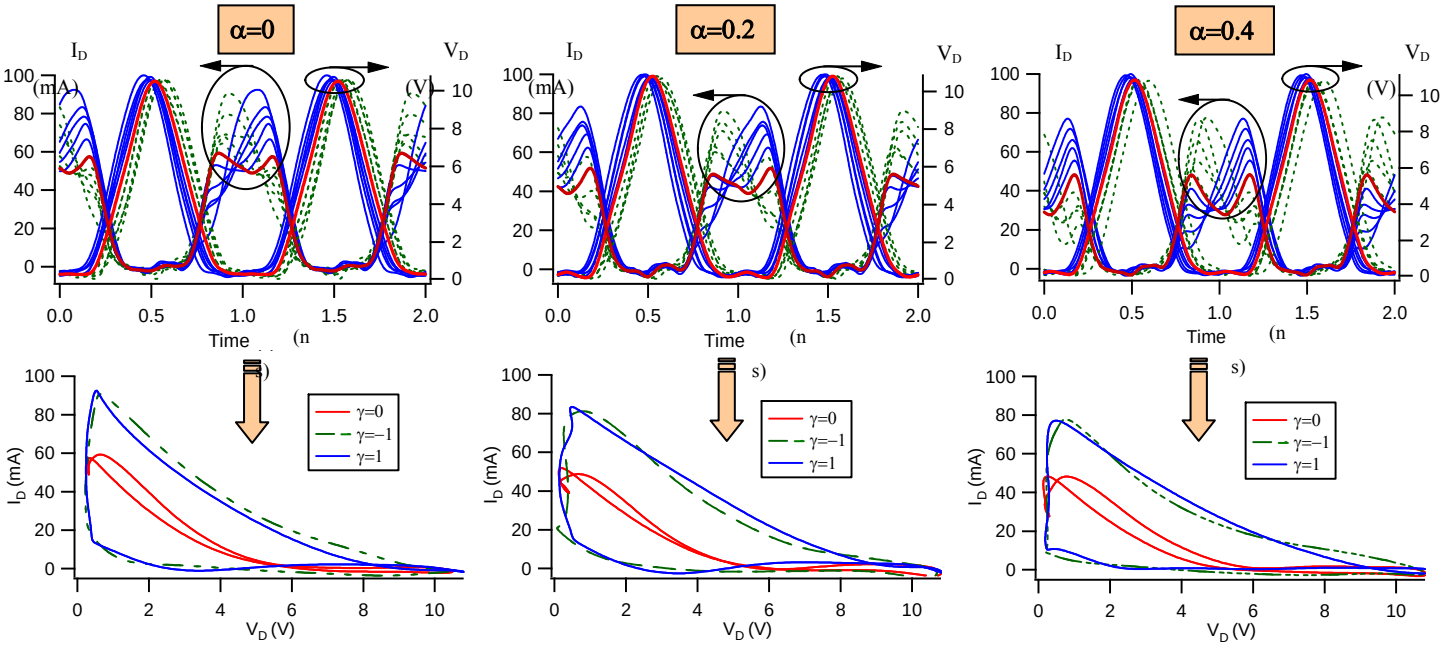

Figure. 12. Measured extended continuous class-F^{-1} current waveforms when varying $-1 \le \gamma \le 1$ in steps of 0.2 and $0 \le \alpha \le 0.4$ in steps of 0.2 and load-lines for $-1 \le \gamma \le 1$ in steps of 1 and $0 \le \alpha \le 0.4$ in steps of 0.2.

All these new current waveforms are achieved for fundamental and second harmonic impedances varied in accordance with equations (5), (6), (8) and (9) and shown in Fig. 11, therefore in this case such equations have been normalized to the optimum initial fundamental impedance of R_1=150+j0 Ω. For all the measurements the third harmonic impedance was set to around the short-circuit whilst the higher impedances greater than three have been considered to be equal to the measurement system characteristic impedance, i.e. 50 Ω.

Figures 13 and 14 show the measured drain efficiency, output power, available gain and source available power as a function of both α and γ. It can be seen that with varying the parameter γ, the device output performance can be maintained almost invariant. The power is approximately constant for all the range of γ whilst the efficiency is maintained greater than 70% with maximum peak up to 80.9%; dropping just on the edges of the range for the last points of γ=±1. The available gain decreases with decreasing γ, this is due to the fact that for γ<0 the device need to be driven harder in order to maintain a constant voltage waveform, this requirement is also identified in the P_{AVS} trace.

When varying the parameter α, the output performance is obviously degraded as the second harmonic impedance goes inside the Smith chart. However, adjusting the fundamental impedance in accordance with this new theory, efficiencies greater than 70% can still be achieved, thus allowing the realization of high efficiency class-F^{-1} PAs, but now for a significantly expanded design space. This will then translate into the ability to design circuits with variable reactive impedances, tracking this "design space" over a wider band of frequencies.

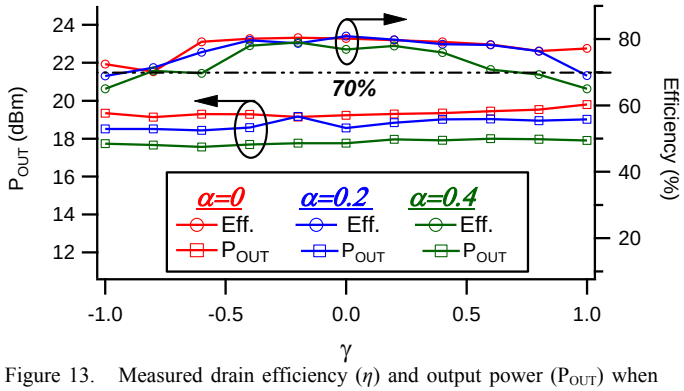

Figure 13. Measured drain efficiency (η) and output power (P_{OUT}) when varying -1 ≤ γ ≤ 1 and 0 ≤ α ≤ 0.4 with both in steps of 0.2.

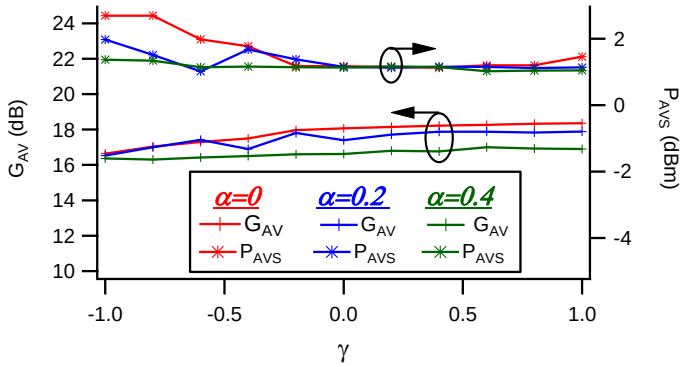

Figure 14. Measured available gain (G_{AV}) and source available power (P_{AVS}) when varying -1 ≤ γ ≤ 1 and 0 ≤ α ≤ 0.4 with both in steps of 0.2.

The possibility of having different solutions with different current waveforms with varying the output impedances is counter intuitive. In ideal devices the drain current is obtained through the input voltage, being the transistor an input voltage controlled current source. Therefore, once the current waveform is achieved by proper input drive, the voltage waveform would be function of the output impedances. However, in real devices the actual drain current varies with varying the impedances being the output related to the input through the feedback capacitor as well as being the drain voltage and current waveforms related to each other through the knee region [1]. In this case by varying properly the impedances and by adjusting slightly the input power (as shown in Fig. 14) it is possible to main an almost fixed voltage waveform as reported in Fig. 12.

IV. Conclusion

This paper has presented an extended formulation on the current waveform for the continuous class-F^{-1}. Starting from the standard narrow band class-F^{-1} condition, it has been demonstrated that varying the second harmonic load around the edge of the Smith chart from the open-circuit condition and adjusting the phase of the fundamental impedance, constant output performances can be maintained. Additionally, it has been demonstrated that when presenting a resistive second harmonic load, the new current formulation will change both magnitude and phase of the required fundamental load, providing the right condition in order to maintain the desired drain efficiency greater than a certain pre-determined value, which here the authors have chosen at 70%. The main aim of this work is to provide to the PA designer different useful waveform solutions providing high power and efficiency. Thus introducing higher flexibility in the PA design process, thanks to providing the opportunity to accommodate reactive impedance variations with frequency when designing broadband PAs.

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Vincenzo Carrubba received the B.Sc. degree in electronic engineering and the M.Sc. degree in microelectronic engineering from the University of Catania, Catania, Italy, in 2005 and 2008, respectively. In 2008 he started working on his Ph.D. degree in electronic engineering with the Centre for High Frequency Engineering, Cardiff University, Cardiff, Wales, U.K. During this time his research interests were the development of active load-pull techniques, the characterization of RF/microwave devices and the design of narrow band and broadband power amplifiers used in wireless communications.

He is currently working at the Fraunhofer Institute for Applied Solid-State Physics (IAF), Freiburg, Germany. Here his main interests include the design of hybrid and MMIC broadband power amplifiers.

Muhammad Akmal was born in Gujranwala, Pakistan. He received the B.Sc. degree in electrical engineering with distinction from Bahauddin, Zakariya University, Multan, Pakistan, in 2005. From 2005 to 2006, he was with Alcatel Telecom Pakistan as a Technical Support Engineer, Lahore, Pakistan, where he was involved in the maintenance, troubleshooting and all the major operational applications of Alcatel 1000 E 10 MM a high capacity Network Switching Subsystem (NSS). He joined Cardiff School of engineering in September 2006 and earned the M.Sc degree in electronic engineering with distinction from Cardiff University, Cardiff, United Kingdom, in 2008, and is currently working toward the Ph.D degree at Centre for High Frequency Engineering, Cardiff University, UK.

His current research interests are developing the modulated waveform measurement system, characterization of nonlinear distorsion in microwave power transistors, linearization, design and measurements of high-power and spectrum-efficient power amplifiers.

Rüdiger Quay received the Diploma degree in physics from Rheinisch-Westfälische Technische Hochschule (RWTH), Aachen, Germany, in 1997, and a second Diplom in economics in 2003. He received his doctoral degree in technical sciences (with honors) from the Technische Universität Wien, Vienna, Austria. In 2009 he received the venia legendi in microelectronics, again from the Technische Universität Wien.

He is currently a research engineer with the Fraunhofer Institute of Applied Solid-State Physics, Freiburg, Germany, heading the RF-devices and characterization group. He has authored and coauthored over 100 refereed publications and three monographs. He is member of IEEE, MTT, and chairman of MTT-6.

Jonathan Lees received the B.Eng. degree in electronic engineering from Swansea University, U.K., in 1992, and the M.Sc. and Ph.D. degrees from Cardiff University, Cardiff, U.K., in 2001 and 2006, respectively.

From 1992 to 2002, he was with QinetiQ, where he developed global positioning and advanced optical instrumentation tracking systems. He is a Chartered Engineer and he is now a Lecturer with the Centre for High Frequency Engineering, Cardiff University, where his research continues into power amplifiers design, load-pull, and large signal measurement systems.

Johannes Benedikt received the Dipl.-Ing degree from the University of Ulm, Ulm, Germany, in 1997, and the Ph.D. degree from Cardiff University, Cardiff, U.K., in 2002. During this time, he took on an additional position as a Senior Research Associate with Cardiff University starting in October 2000, where he supervised a research program with Nokia on RFPAs. In December 2003, he was appointed a Lecturer with Cardiff University, where he was responsible for furthering research in the high-frequency area. In April 2010 he was awarded a Professorship at Cardiff University. His main research focus is on development of systems for the measurement and engineering of RF current and voltage waveforms and their application in complex PA design.

Steve C. Cripps received the Ph.D. degree from Cambridge University, Cambridge, U.K.

He worked for Plessey Research on GaAsFET hybrid circuit development. Later, he joined Waitkins-Johnson's Solid State Division, Palo Alto, CA, and he has held Engineering and Management positions at WJ, Loral, and Celeritek. During this period, he designed the industry's first 2-8 and 6-19 GHz 1 watt solid-state amplifiers. In 1983, he published a technique for microwave power amplifier design, which has become widely adopted in the industry. In 1990, he became an independent consultant and was active in a variety of commercial RF product developments, including the design of several cellular telephone PA MMIC products. In 1996, he returned to the U.K., where he is consulting activities continue to be focused in the RFPA area. He has recently been appointed a Professional Research Fellow at Cardiff University, U.K. He has recently authored a second edition of his best selling book, *RF Power Amplifiers Design for Wireless Communication* (Artech House, 2006).

Dr. Cripps was a recipient of the 2008 IEEE Microwave Applications Award. He is currently vice-chair of the High Power Amplifier Subcommittee of the Technical Coordination and Technical Program Committees of the IEEE Microwave Theory and Techniques Society, and writes the regular
"Microwave Bytes" column in the *IEEE Microwave Magazine*.

Paul J. Tasker (M'88-SM'07) received the B.Sc. degree in physics and electronics and Ph.D. degree in electronic engineering from Leeds University, U.K., in 1979 and 1983, respectively.

From 1984 to 1990 he worked as a Research Associate with Cornell University, Ithaca, NY, with Prof. L. Eastman, where he was involved in the early development of HFET transistors. From 1990 to 1995, he was a Senior Researcher and Manager with the Fraunhofer Institute for Applied Solid State Physics (IAF), Freiburg, Germany, where he was responsible for the development of millimeter wave MMICs. He joined the School of Engineering, Cardiff University, Cardiff, U.K., as a Professor in the summer of 1995, where he has been establishing the Cardiff University and Agilent Technology Centre for High Frequency Engineering. The center's research objective is to pioneer the development and application of RF-IV waveform and engineering systems, with a particular focus to addressing the PA design problem. He has contributed to over 200 journal and conference publications and given a number of invited conference workshop presentations.

Dr. Tasker has been appointed as an IEEE Distingueshed Microwave Lecturer for the term of 2008-2010.

Publication 8.

Title:

Continuous-ClassF3 Power Amplifier Mode Varying Simultaneously First 3 Harmonic Impedances

Authors:

V. Carrubba, R. Quay, M. Schlechtweg, O. Ambacher, M. Akmal, J. Lees, J. Benedikt, P. J. Tasker, S. C. Cripps.

Conference:

IEEE MTT-S Microwave Symposium Digest, pp.1-3, June 2012.

Continuous-ClassF3 Power Amplifier Varying Simultaneously First 3 Harmonic Impedances

[*,†]V. Carrubba, [*]R. Quay, [*]M. Schlechtweg, [*]O. Ambacher, [†]M. Akmal, [†]J. Lees, [†]J. Benedikt, [†]P. J. Tasker, [†]S. C. Cripps

[*] Fraunhofer Institute for Applied Solid-State Physics, Tullastrasse 72, 79108 Freiburg, Germany

[†] Centre for High Frequency Engineering, Cardiff University, CF24 3AA Cardiff, UK

***Abstract* — This paper presents for the first time the broadband Continuous-ClassF3 mode power amplifier (PA) extended to include a variable reactance third harmonic impedance. It will be demonstrated that by proper manipulation of the voltage and current waveforms different optimum impedance solutions can be identified. When designing PAs, the harmonic impedances cannot easily be constraint to open-circuit and/or short-circuit points with varying frequency. Therefore, the possibility to vary the third harmonic reactance as well as the second harmonic and fundamental reactance with frequency would allow for an easier, more flexible and achievable design requirement. Measurements on a GaN power transistor have delivered around 34.5-35.9 dBm of output power, 80-85 % of drain efficiency and 13.7-15.5 dB of available gain at 1 GHz of fundamental frequency for the various combination of first three load solutions. The measurements demonstrate that constant or greater output performance can be obtained over a wide PA design space when varying properly the first three harmonic loads. The different reactive impedance solutions carried out at the single frequency can then be translated into frequency domain, allowing the design of high power-efficiency broadband power amplifiers.**

a) Index Terms — Broadband amplifiers, gallium nitride, microwave devices, microwave measurements, power amplifiers.

I. INTRODUCTION

The power amplifier (PA) stage used in wireless communication networks is one of the most crucial and therefore important components. Here different requirements must be satisfied such as efficiency, output power, gain and linearity. Nowadays, these requirements need to be satisfied for the broadband spectrum. This means that the overall specifics need to be optimized for a wide range of frequencies.

In the last years different broadband PA modes have been demonstrated, as some of those here presented [1-4]. Broadband PAs can deliver satisfactory performance over a wider bandwidth when compared with the narrow band modes [1-2]. In particularly, the Continuous-ClassF mode [3] has shown that by moving the second harmonic impedance from the short-circuit condition and by simultaneously adjusting the fundamental load in accordance with the Continuous-ClassF theory while maintaining a fixed open-circuit the third harmonic load, output power and drain efficiency can be maintained constant. Nevertheless, in real PA design the third harmonic termination cannot be considered as a fixed open-circuit point, as it will move somewhere with frequency.

This paper demonstrates for the first time how the Continuous-ClassF mode can deliver high power efficiency states for different combination of fundamental, second and now third harmonic load solutions, therefore termed Continuous-ClassF3. Besides, the experimental results show that by presenting these new reactive solutions and varying the gate bias point (V_{GS}), greater efficiency can be achieved without trading-off a significant amount of output power.

II. THEORETICAL CONTINUOUS-CLASSF3

The Continuous-ClassF mode presented in [3] has shown a new formulation for the voltage waveform while maintaining an ideal constant half-wave rectified sinusoidal current waveform. Therefore, leading to a simultaneous variation of the fundamental and second harmonic reactances when maintaining a constant open-circuit third harmonic impedance. In this manner the output power and drain efficiency can be maintained theoretically at constant level.

In reality when designing PAs it is difficult to maintain any fundamental or harmonic impedance constant with frequency. The drain current cannot be considered as a fixed constant waveform (in this case half-wave rectified sinusoidal). This is due to the relationship between input and output through the gate-drain capacitor C_{GD} as well as the knee voltage (V_{knee}) interaction, for which drain voltage and current waveforms are related to each other ($i_D=-g_m \cdot V_{gs} \cdot I_{max} \cdot (1-e^{-Vds/Vknee})$) [1].

In [3] it is shown that in order to have high power-efficiency conditions over bandwidth, the third harmonic termination should move "somewhere" around the edge of the Smith chart (from the open-circuit condition) with frequency, but no theoretical or experimental verification has to date been reported. In this work for the first time the Continuous theory has been extended, allowing reactive excursions of the third harmonic impedance as well.

Equations (1) and (2) represent the voltage and current waveform formulations.

$$v(\vartheta) = \left(1 - \frac{2}{\sqrt{3}}\cos\vartheta\right)^2 \cdot \left(1 + \frac{1}{\sqrt{3}}\cos\vartheta\right) \cdot (1 - \gamma\sin\vartheta), \quad (1)$$

$$i(\vartheta) = \left(1 + \frac{2}{\sqrt{2}}\cos\vartheta + \frac{1}{2}\cos 2\vartheta\right) \cdot \left(1 + \frac{\gamma}{5}\sin 5\vartheta\right). \quad (2)$$

Varying the only parameter γ it is possible to obtain the desired range of fundamental, second and now third harmonic impedances, as shown in Fig. 1.

Expanding (1) and (2), the voltage (V_n) and current (I_n) components from (3) to (9) are obtained:

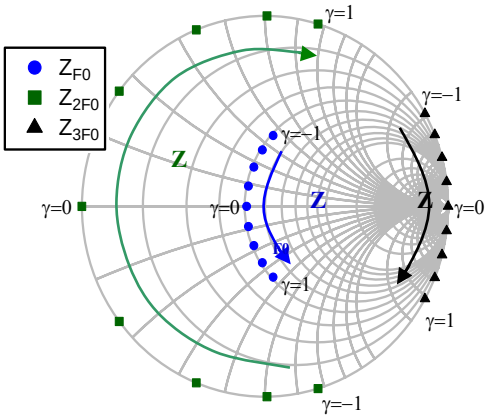

Fig. 1. Theoretical first 3 harmonic impedances when considering R_{F0}=40 Ω at the intrinsic current generator plane.

$$V_1 = -\frac{2}{\sqrt{3}} + j\gamma\,, \qquad I_1 = \frac{2}{\sqrt{2}}\,, \tag{3}$$

$$V_2 = -j\frac{7}{6\sqrt{3}}\gamma\,, \qquad I_2 = \frac{1}{2}\,, \tag{4}$$

$$V_3 = \frac{1}{3\sqrt{3}}\,, \qquad I_3 = -j\frac{\gamma}{20}\,, \tag{5}$$

$$V_4 = j\frac{1}{6\sqrt{3}}\gamma\,, \qquad I_4 = -j\frac{1}{5\sqrt{2}}\gamma\,, \tag{6}$$

$$V_5 = 0\,, \qquad I_5 = -j\frac{1}{5}\gamma\,, \tag{7}$$

$$V_6 = 0\,, \qquad I_6 = -j\frac{1}{5\sqrt{2}}\gamma\,, \tag{8}$$

$$V_7 = 0\,, \qquad I_7 = -j\frac{1}{20}\gamma\,. \tag{9}$$

The components from V_1 to V_7 represent the voltage Fourier components from 1st to the 7th harmonic, as well as the components from I_1 to I_7 represent the corresponding current Fourier components. It should be noted, the voltage components from 5th to 7th are set to zero, while higher current components (up to the 7th) have been considered; this can be justified as a good approximation in most practical cases, based on the probability that higher voltage harmonics will usually be suppressed by the device parasitic capacitances.

Fig. 2 and 3 show the theoretical voltage and current waveforms and load-lines when applying (1) and (2) for γ ranging between -1 and 0 with step of 0.5.

The range $0 < \gamma \leq 1$ (not displayed) would give the mirrored waveforms of $-1 \leq \gamma \leq 0$. Despite the waveforms (and load-lines) present different shapes with varying γ, the overall power and efficiency is ideally kept constant. This is due to the fact that the new combination (ratio) of voltage and current waveforms leads to the variation on the imaginary parts of first three impedances with the real parts and DC components kept constant. This condition ensures theoretically a constant output power and drain efficiency.

When applying this theory, and including harmonic content greater than 3 (up to 7th), optimum results can be obtained, however it will be seen in the measurement section of this paper that satisfactory output performance can still be achieved by considering only the first three harmonic components.

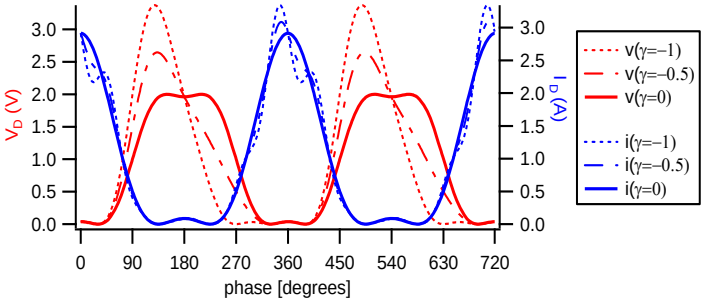

Fig. 2. Theoretical Continuous-ClassF3 voltage and current waveforms for γ varying between -1 and 0 in steps of 0.5.

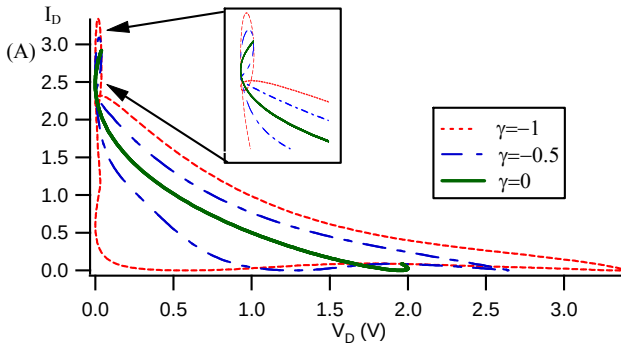

Fig. 3. Theoretical Continuous-ClassF3 load-lines for γ varying between -1 and 0 in steps of 0.5.

Therefore, dividing the voltage components by the appropriate current components (e.g. V_1/I_1), the fundamental and harmonic impedances can be obtained where optimum output power and drain efficiency (in this case 81.7% as finite harmonic contents for both voltage and current waveforms have been considered) are maintained constant.

III. MEASUREMENT RESULTS

The theoretical analysis reported in section II has been applied experimentally on a 1.2 mm of periphery GaN power transistor [5], using a 28 V supply voltage at 1 GHz fundamental frequency.

Initially the standard Class-F mode has been obtained. Here, with bias voltage of V_G=-3.1 V, input power of P_{IN}=14 dBm (source available power P_{AVS}=20.4 dBm) and presenting Z_{F0}=0.49∟45.8°, Z_{2F0}=1∟-180° and Z_{3F0}=1∟68° at the extrinsic plane, an efficiency of η=80.6 %, output power of P_{OUT}=35.9 dBm and available gain of

G_{AV}=15.5 dB have been achieved at 1.5 dB of gain compression. Once the standard Class-F mode has been obtained the first three harmonic impedances have been simultaneously varied as explained in previous section. Theory and measurements have been performed at the device intrinsic plane after de-embedding the drain-source capacitor C_{DS}=0.45 pF.

Fig. 4 shows the measured output performance in terms of power, efficiency and gain as a function of γ, for a constant source available power P_{AVS}=20.4 dBm.

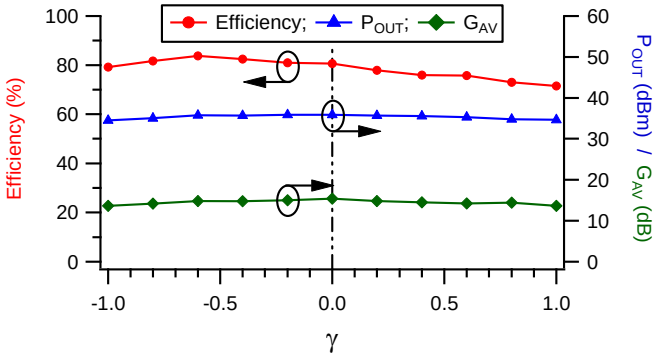

Fig. 4. Measured Continuous-ClassF3 drain efficiency, output power and available gain for $-1 \le \gamma \le 1$ in steps of 0.2.

As it can be seen, the output power and available gain are maintained at an almost constant level with varying γ, at around 34.5-35.9 dBm and 13.7-15.5 dB respectively. Interestingly moving toward γ<0 the efficiency increases, reaching a maximum value of 83.7 % for γ=-0.6 whilst for γ>0 it decreases when approaching towards the edge of γ. This is caused either by the non-unilateral device characteristic and some non-linearity in the device transconductance.

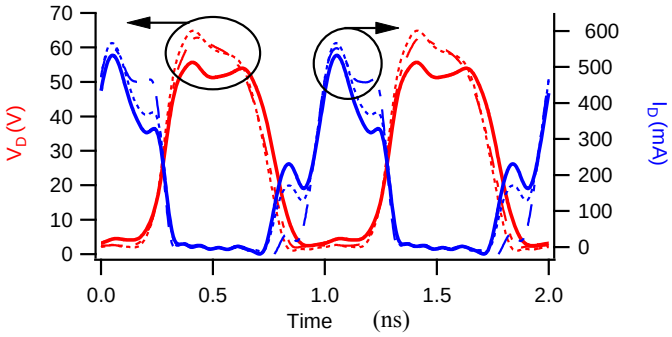

Fig. 5. Measured Continuous-ClassF3 voltage (red lines) and current (blue lines) waveforms for $-1 \le \gamma \le 0$ in steps of 0.5.

Fig. 5 shows the measured Continuous-ClassF3 voltage and current waveforms for constant P_{AVS}=20.4 dBm. Both voltage and current waveforms vary as a function of γ (between -1 and 0 in steps of 0.5), which means that all of the first three harmonic impedances are being varied, revealing the new design space.

Fig. 6 shows efficiency and output power as a function of bias V_G and the parameter γ. It can be seen that decreasing the bias voltage from its original value of -3.1 V, the efficiency increases up to 85 % for V_G=-3.6 V and γ=-0.5 while still maintaining satisfactory output power of 35.7dBm (3.72W) at almost the same compression level, where G_{AV}=14.7 dB.

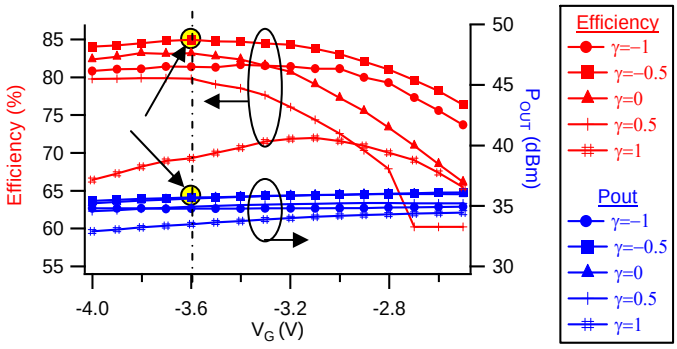

Fig. 6. Measured drain efficiency and output power function of gate bias V_G and γ, where $-4 \le V_G \le -2.7$ V in steps of 0.1 and $-1 \le \gamma \le 1$ in steps of 0.5.

IV. CONCLUSION

This paper has presented for the first time the Continuous Class-F3 mode PA, which allows for continuous power and high efficiency performance for specified reactive terminations at fundamental, second and third harmonics. It has been demonstrated that by appropriate variation of the first three harmonic impedances a wide range of useful solutions where constant and even improved output performance can be achieved. The extension of the continuous mode theory up to the third harmonic is an important step in broadband design as in reality when designing PAs, fixed harmonic loads cannot easily be maintained constant with varying frequency. Measurements on a GaN power transistor have demonstrated the validity of the approach.

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Publication 9.

Title:

Dual-Band Class-ABJ AlGaN/GaN High Power Amplifier

Authors:

V. Carrubba, S. Maroldt, M. Mußer, H. Walcher, M. Schlechtweg, R. Quay, O. Ambacher

Conference:

IEEE European Microwace Conference (EuMC), pp. 635-638, October 2012.

Dual-Band Class-ABJ AlGaN/GaN High Power Amplifier

V. Carrubba, S. Maroldt, M. Mußer, H. Walcher, M. Schlechtweg, R. Quay, O. Ambacher
Fraunhofer Institute for Applied Solid State Physics (IAF), Tullastraße 72, 79108 Freiburg, Germany
vincenzo.carrubba@iaf.fraunhofer.de

Abstract — **This paper presents a dual-band multiharmonic Class-ABJ high power amplifier (PA) realized in AlGaN/GaN technology. In the Class-ABJ theory power and efficiency are theoretically maintained constant for the wide band spectrum frequency due to the ability to accommodate simultaneous fundamental and harmonic reactive terminations. Here it will be shown that by using the Class-ABJ theory, it is possible to optimize power, gain and efficiency for different frequency bands in a high PA design. The realized Class-ABJ power amplifier delivers drain efficiency greater than 55% with output power and gain greater than 42.4-44.4 dBm and 10-11 dB respectively for the two frequency bands 2.05-2.22 GHz and 2.45-2.58 GHz at around 2-3 dB of compression level.**

Keywords - broadband amplifiers; Class-J; GaN; high power amplifiers; multiband.

I. Introduction

The continuous demands of services in the wireless communication field have led to significant improvements starting from the device transistor technology to the overall wireless networks.

AlGaN/GaN high electron mobility transistors (HEMT) on SiC substrate have raised a lot of interest in the last years for the realization of power amplifiers (PAs) used in the ongoing 3G (third generation) and 4G (fourth generation) standards for mobile phones and base stations [1]. This is due to the ability of the AlGaN/GaN technology to achieve high output performance over the broadband spectrum as well as the ability of reaching high power capability, high gain, high frequency, robustness and reliability [2].

Various broadband and multiband power amplifier techniques have been so far presented and described as some shown here [3],[4]. However, the advanced AlGaN/GaN transistor technology accompanied with the knowledge of harmonic output matching terminations lead to the ability of realizing PAs with high power-efficiency over the desired frequencies range.

This paper shows a multiharmonic multiband Class-J PA designed from the standard Class-AB mode, therefore called Class-ABJ [5]. It is known that the Class-ABJ mode is used for the realization of broadband power amplifiers. Here, by using such theory, the main aim of this work is to realize and demonstrate a PA delivering high power-efficiency state as well as constant gain for the dual band frequencies 2.1-2.2 GHz and 2.5-2.6 GHz.

II. GaN Technology for High Power Transistors

The high power HEMT devices applied in this work are based on a GaN semiconductor technology using 3-inch semi-insulating SiC substrates. The epitaxial grown heterostructure consists of highly resistive layers: a thick GaN buffer, followed by an AlGaN barrier, including a thin GaN cap layer. The GaN HEMTs are fabricated with a gate length of 0.5 µm with a technology optimized for high reliability and robustness up to an operation voltage of 50 V [2]. Therefore an integrated source terminated field plate is used to reduce the electric field strength in the gate region, which allows a maximum breakdown voltage of > 200 V. The technology includes a front side and backside process with front-to-back via holes. The output current of a typical unit cell transistor with a gate width of 1.2 mm yields 670 mA/mm and a maximum current gain cut-off frequency of 19 GHz. Large signal measurements of these devices under Class-AB operation at 2 GHz show an output power density of 5 W/mm at 40 V supply voltage and more than 6.5 W/mm at 50 V while a power added efficiency of > 65% is obtained. The high operation voltage of the presented devices increases the output impedance of high power devices and therefore allows a better broadband matching. A high power device with a total gate width of 9.6 mm is used for the design and the realization of the power amplifier in this work.

III. Class-ABJ PA Mode

Starting from the standard single frequency solution Class-AB state and by varying properly the fundamental and harmonic impedances it is possible to have different solutions in terms of output waveforms for which the device output performance does not degrade. This PA mode is termed Class-BJ [5] or in this case Class-ABJ as the DUT (device under test) has been biased in Class-AB. The Class-ABJ PA has been designed by using the Agilent ADS (advanced design system) environment and the nonlinear model of the AlGaN/GaN HEMT devices described in Section II.

A. Step 1: Class-AB PA for the fixed frequency

The first step for the realization of such PA is the standard Class-AB state. Here, for drain voltage V_D=40 V at the fixed frequency 2.4 GHz (around the center frequency) and by biasing the device in Class-AB for which the quiescent current Idq=70 mA, fundamental and harmonic impedances with the input power have been swept in order

to find the best trade-off between output power, gain and drain efficiency.

Being the Class-ABJ a mode which rely on the use of the voltage and current waveforms at the intrinsic device plane, by de-embedding the parasitics of the AlGaN/GaN device, the proper waveforms therefore the output behavior can be revealed. Here, for fundamental impedance Z_{F0}=20.9+j0 Ω and keeping short-circuit the second and third harmonic terminations, the optimum standard Class-AB state is achieved.

Fig. 1 shows the standard Class-AB performance in terms of drain efficiency, output power and gain function of the input power sweep P_{IN}. Drain efficiency of DE=64.9%, output power of P_{OUT}=44.6 dBm (28.9 W) with gain of G=21.3 dB at around the 2 dB of gain compression have been obtained. The Class-AB voltage and current waveforms are plotted in Fig. 2 showing the sinusoidal voltage waveforms and the rectified sinusoidal current waveforms with conduction angle greater than 180° due to the Class-AB bias condition.

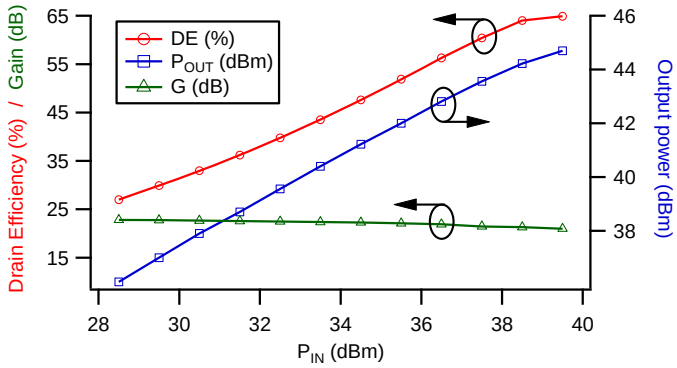
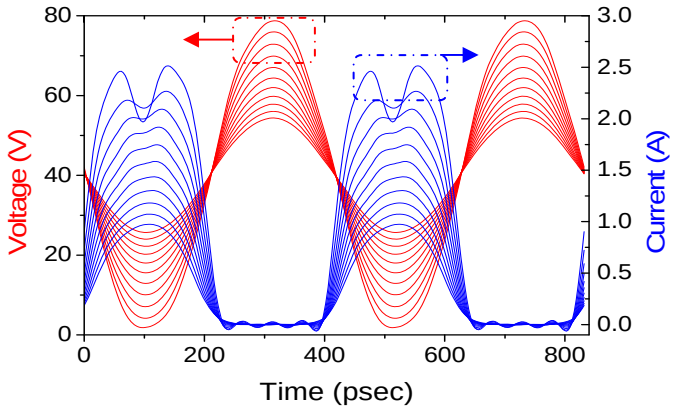


Figure 1. Simulated standard Class-AB drain efficiency, output power and gain function of the input power sweep.

Figure 2. Simulated standard Class-AB voltage (red) and current (blue) waveforms at the intrinsic device plane function of the input power sweep.



B. Step 2: Class-ABJ fundamental and harmonic loads

Once the standard Class-AB state is designed and the real part of the fundamental impedance R_{F0} is optimized for the proper input power, the next step is the achievement of the different ranges of fundamental and second harmonic impedance solutions. By applying the Class-ABJ theory [5], the new family of voltage waveforms $v_{ABJ}(\theta)$ is revealed. The equation of such voltage waveforms is shown in (1) while the current waveform is kept constant rectified sinusoidal:

$$v_{ABJ}(\vartheta) = (1-\cos\vartheta)\cdot(1-\delta\sin\vartheta)$$

$$= 1-\cos\vartheta-\delta\sin\vartheta+\frac{\delta}{2}\sin 2\vartheta, \qquad (1)$$

where ϑ is the conduction angle and δ is the parameter that defines the new Class-ABJ voltage waveforms, as shown in Fig. 3 in this case for δ = -1.

It can be noted that the standard cosinusoidal voltage waveform (1-cosϑ) is now multiplied with another sinusoidal waveform (1-δsinϑ) as shown in (1).

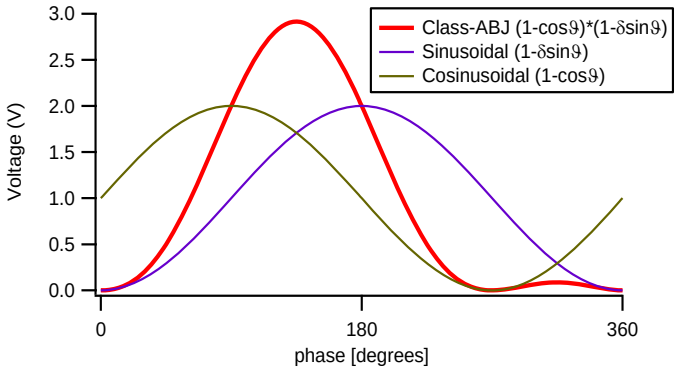


Figure 3. Theoretical Class-ABJ (1-cosϑ)*(1-δsinϑ) voltage waveform for δ=-1(red); cosinusoidal waveform (green); and sinusoidal waveform for δ=-1 (blue).

In this case it is intuitive that the new Class-ABJ voltage waveforms would lead to different impedance solutions with varying the parameter δ, however, it is not intuitive that such new impedance solutions lead theoretically to the same output performance in terms of power and efficiency [5],[6]. This is because the voltage waveform is varied with only its reactive part. Therefore, since the output power is proportional to the real parts of the fundamental voltage and current components, this leads to a constant optimum P_{OUT}. Besides, being the DC voltage and current contents constant as well with varying such parameter δ, this leads to a constant optimum drain efficiency.

Equations (2), (3) and (4), show the Class-ABJ fundamental, second and high harmonic terminations for which the output performance is constant. Note that when δ=0 the standard Class-AB impedances where the reactive parts are equal to zero (thus at the intrinsic device plane) are achieved. When varying the parameter δ between -1 and 1 in order to keep the voltage waveform positive [5],[6] different fundamental and second harmonic impedances are revealed. It can be noted that fundamental and second harmonic impedances are inversely proportional with varying δ. Positive values of δ lead to negative fundamental reactive parts and positive second harmonic reactive termination, and vice-versa for negative values of δ. The harmonic terminations greater than 2 are short-circuited.

$$Z_{F0} = R_{F0} - j\cdot\delta\cdot R_{F0}, \qquad (2)$$

$$Z_{2F0} = 0 + j\cdot\delta\cdot\frac{3\pi}{8}\cdot R_{F0}, \qquad (3)$$

$$Z_{nF0} = 0, \qquad \text{for n} > 2 \qquad (4)$$

For the AlGaN/GaN device used in this work, starting from the optimum fundamental load Z_{F0} = 20.9+j0 Ω and Z_{2F0} =short-circuit and by applying (2) and (3) with δ varying between -1 and 0 in step of 0.5, the Class-ABJ terminations have been carried out. For the impedance points for δ>0 the second harmonic impedance could not be placed on the edge of the Smith chart (Γ=1) with the different phases (function of δ). This was due to stability considerations which have been overcome with the proper input matching network (IMN) and the proper bias network design, as it will be mentioned in Step 3.

C. *Step 3: Class-ABJ output matching network*

So far, by using the Class-ABJ theory, the fundamental and second harmonic reactive impedance solutions, where constant output performance is achieved, have been carried out for the constant frequency F_0=2.4 GHz. Now, the possibility of having different reactive impedances for the fixed frequency is translated into the possibility to accommodate different optimum frequency solutions when designing the output matching network (OMN). This means that, if the impedance solutions are considered in the Smith chart as target points, the PA designer can now design the proper OMN in order to present those target impedances. Therefore, with this approach, high power-efficiency broadband power amplifiers can be realized.

Fig. 4 shows the Class-ABJ output matching network capable of synthesize the fundamental and second harmonic output impedances carried out for the DUT by applying the Class-ABJ theory.

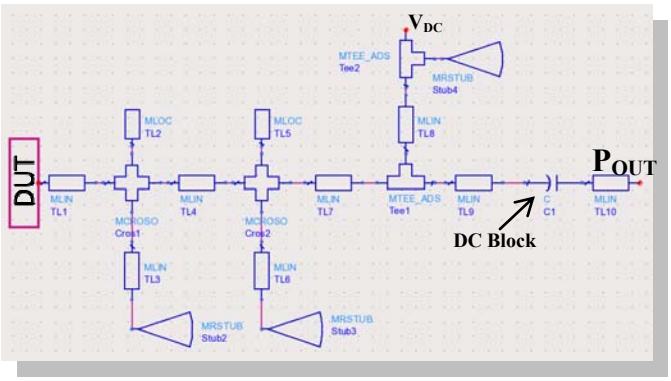


Figure 4. Class-ABJ output matching network.

For each fundamental target load corresponds the proper second harmonic termination point as demonstrated from theory [7]. Therefore, the OMN shown in Fig. 4 is able to present simultaneously the different fundamental and second harmonic terminations. The IMN (not shown in details in the paper but shown in the PA photo of Fig. 5) has been realized to match the low input impedance of the DUT to the 50 Ω source characteristic impedance in order to maximize the gain. Different resistors and capacitors have been added in both the RF path and in the bias network to overcome stability issues.

IV. Class-ABJ Power Amplifier Realization and Measurement Results

Fig. 5 shows the photograph of the realized Class-ABJ PA as well as the 9.6mm AlGaN/GaN powerbar. The measurements have been performed at drain voltage V_D=40V and input bias voltage V_{GS}=-1.62 V for which the quiescent current was Idq=70 mA.

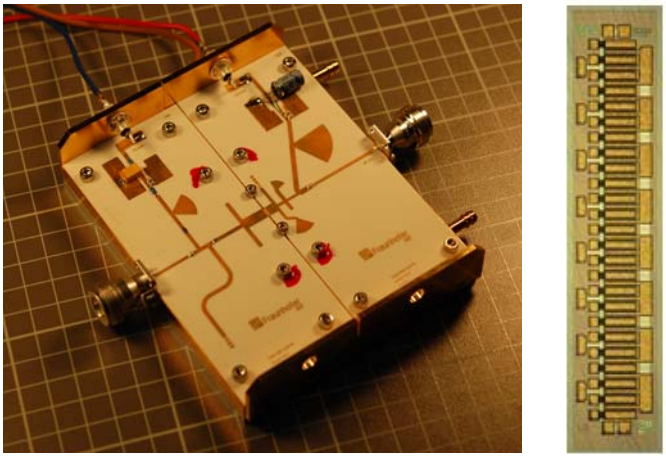


Figure 5. Photograph of the realized Class-ABJ PA and powerbar.

Fig. 6 shows the measured output performance in terms of drain efficiency, output power and gain function of the input power sweep and for different frequencies in the two bands 2.08-2.22 GHz and 2.48-2.6 GHz with frequency step of 20 MHz. As it can be noted, in the low-band (left graph) the drain efficiency and output power increase with the input power in a similar way for the different frequencies. Here the drain efficiency is around 55-60% for all the frequencies from 2.08 GHz to 2.22 GHz. The output power reaches the maximum value of around 44.4-44.6 dBm while the linear gain is around 13-14 dB, going down to around 10-11 dB at the 3 dB compression point where the maximum efficiency and power are revealed. In the upper-band (right graph) from 2.48 GHz to 2.6 GHz, the drain efficiency and power present different behavior for the different frequencies, however still efficiency greater than 50-55% is achieved. Here the power is lower compared with the low-band, between 42 dBm and 43 dBm with delivering around the same linear gain of 14 dB.

Fig. 7 shows the drain efficiency, PAE, output power and gain Vs frequency when delivering an average gain of around 10.5 dB. Here, it is clearly shown that the output power and gain do not decrease significantly in the entire bandwidth between 2.05 GHz and 2.6 GHz.

Both the output power and gain are maintained around 42.4-44.4 dBm and 10-11 dB respectively. Furthermore, the drain efficiency is maintained greater than 55% in the frequency ranges 2.05-2.22 GHz and 2.48-2.58 GHz as highlighted in yellow. In the same frequency bands, the PAE is greater than 50%.

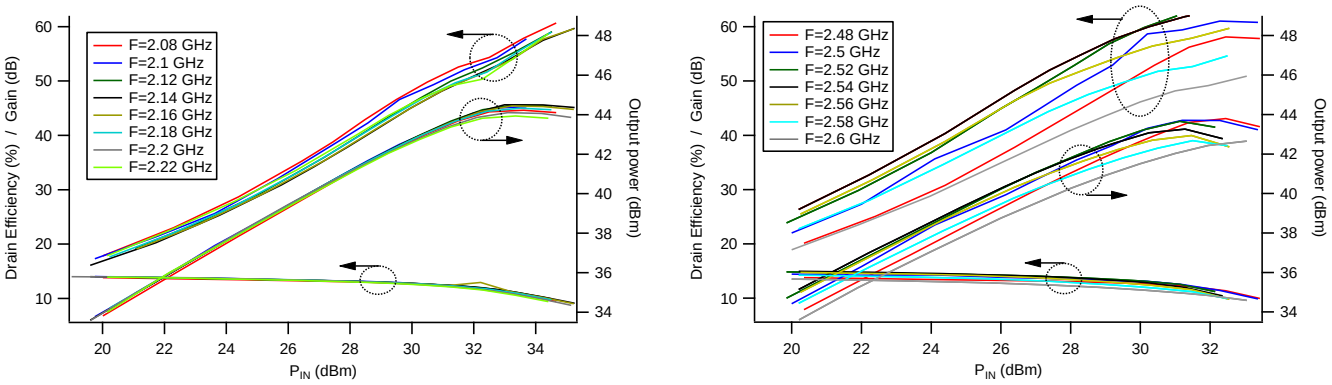


Figure 6. Measured Dual-Band Class-ABJ drain efficiency, P_{OUT} and gain for the low-band 2.08-2.22 GHz (left) and high-band 2.48-2.6GHz (right).

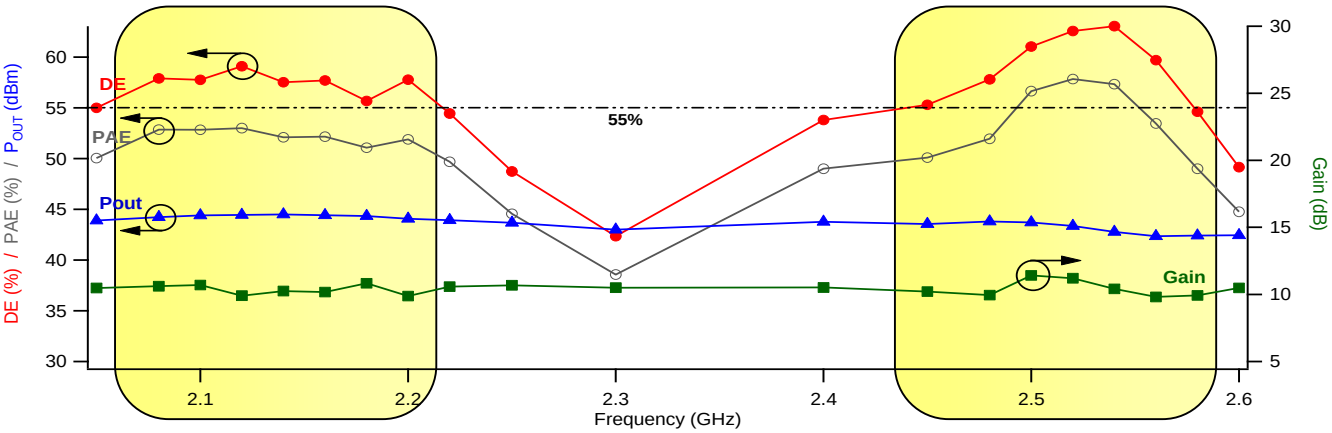


Figure 7. Measured Class-ABJ drain efficiency, PAE, P_{OUT} and gain Vs frequency.

The maximum drain efficiency is DE=63% achieved at 2.54 GHz. It is interesting to note that, despite the design requirement was to optimize the power-efficiency in the two requested bandwidths, by using the Class-ABJ theory, the middle band (around 2.25-2.45 GHz) still delivers satisfactory output power and gain, while the drain efficiency is still above 45%, thus not presenting consistent degradations if compared with other different multiband designs [3],[4].

V. Conclusion

In this work the design steps, the realization and the measurement results of a dual-band Class-ABJ power amplifier is presented. By using the Class-ABJ theory, the proper fundamental and second harmonic terminations have been carried out, focusing on the two band of interest 2.1-2.2 GHz and 2.5-2.6 GHz. The PA delivers drain efficiency, output power and gain greater than 55%, 44.2 dBm and 10 dB respectively for both the low and upper frequency bands between 2.08-2.22 GHz and 2.48-2.58 GHz. The maximum peak of drain efficiency is 63% achieved at 2.54 GHz, while maximum peak power of 44.6 dBm (28.9 W) is delivered at 2.14 GHz.

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