AIP Journal of Applied Physics

GaAs on Si epitaxy by aspect ratio trapping: Analysis and reduction of defects propagating along the trench direction

Tommaso Orzali, Alexey Vert, Brendan O'Brien, Joshua L. Herman, Saikumar Vivekanand, Richard J. W. Hill, Zia Karim, and Satyavolu S. Papa Rao

Citation: Journal of Applied Physics **118**, 105307 (2015); doi: 10.1063/1.4930594
View online: http://dx.doi.org/10.1063/1.4930594
View Table of Contents: http://scitation.aip.org/content/aip/journal/jap/118/10?ver=pdfcov
Published by the AIP Publishing

Articles you may be interested in

Heteroepitaxy of GaAs on (001) ⇒ 6° Ge substrates at high growth rates by hydride vapor phase epitaxy
J. Appl. Phys. **113**, 174903 (2013); 10.1063/1.4803037

Effects of annealing and substrate orientation on epitaxial growth of GaAs on Si
J. Appl. Phys. **106**, 083514 (2009); 10.1063/1.3248372

Defect reduction of GaAs/Si epitaxy by aspect ratio trapping
J. Appl. Phys. **103**, 106102 (2008); 10.1063/1.2924410

Defect reduction of GaAs epitaxy on Si (001) using selective aspect ratio trapping
Appl. Phys. Lett. **91**, 021114 (2007); 10.1063/1.2756165

High-speed GaAs metal gate semiconductor field effect transistor structure grown on a composite Ge ⁄ Ge x Si 1 − x ⁄ Si substrate
J. Appl. Phys. **101**, 084501 (2007); 10.1063/1.2722245

Reuse of AIP Publishing content is subject to the terms at: https://publishing.aip.org/authors/rights-and-permissions. Download to IP: 131.251.253.89 On: Mon, 09 May 2016 08:17:41

JOURNAL OF APPLIED PHYSICS 118, 105307 (2015)

GaAs on Si epitaxy by aspect ratio trapping: Analysis and reduction of defects propagating along the trench direction

Tommaso Orzali,[1,a)] Alexey Vert,[1] Brendan O'Brien,[1] Joshua L. Herman,[2] Saikumar Vivekanand,[2] Richard J. W. Hill,[3] Zia Karim,[4] and Satyavolu S. Papa Rao[1]
[1]*SEMATECH, 257 Fuller Rd Suite 2200, Albany, New York 12203, USA*
[2]*College of Nanoscale Science and Engineering, SUNY Polytechnic Institute, 251 Fuller Road, Albany, New York 12203, USA*
[3]*Now at Micron Technologies, 8000 S Federal Way, Boise, Idaho 83716, USA*
[4]*AIXTRON, Inc., 1139 Karlstad Dr., Sunnyvale, California 94089, USA*

(Received 8 July 2015; accepted 27 August 2015; published online 14 September 2015)

The Aspect Ratio Trapping technique has been extensively evaluated for improving the quality of III-V heteroepitaxial films grown on Si, due to the potential for terminating defects at the sidewalls of SiO_2 patterned trenches that enclose the growth region. However, defects propagating along the trench direction cannot be effectively confined with this technique. We studied the effect of the trench bottom geometry on the density of defects of GaAs fins, grown by metal-organic chemical vapor deposition on 300 mm Si (001) wafers inside narrow (<90 nm wide) trenches. Plan view and cross sectional Scanning Electron Microscopy and Transmission Electron Microscopy, together with High Resolution X-Ray Diffraction, were used to evaluate the crystal quality of GaAs. The prevalent defects that reach the top surface of GaAs fins are {111} twin planes propagating along the trench direction. The lowest density of twin planes, $\sim 8 \times 10^8\,\mathrm{cm}^{-2}$, was achieved on "V" shaped bottom trenches, where GaAs nucleation occurs only on {111} Si planes, minimizing the interfacial energy and preventing the formation of antiphase boundaries. © *2015 AIP Publishing LLC*.
[http://dx.doi.org/10.1063/1.4930594]

I. INTRODUCTION

Since the 1980s, monolithic integration of III-V semiconductors on Si has attracted a great amount of interest due to the possibility of combining the superior electronic and optoelectronic properties of III-Vs, with the high manufacturability of Si-based microelectronics. III-V light sources integrated onto Si chips or waveguides would compensate for the poor silicon efficiency as a light emitter, and are promising candidates for the realization of photonic integrated circuits.[1,2] Moreover, III-V semiconductors with high effective mobility and injection velocity, such as InGaAs and InAs, are considered promising candidates to replace Si as the channel material in sub-7 nm node n-channel Metal-Oxide-Semiconductor Field-Effect Transistor.[3–5] However, the large lattice and thermal expansion coefficient mismatch, along with the difference in crystal polarity between III-Vs and Si, generate a high density of defects in heteroepitaxial layers which can deteriorate device performance and reliability. Several techniques have been investigated extensively to control defects on III-V heterostructures on Si, such as wafer bonding,[2,6] the use of strain relaxed buffer layers,[7] the use of a low temperature nucleation layer,[8,9] or the aspect ratio trapping (ART) approach.[10] The main advantage of the ART approach is to confine threading dislocations and {111} planar defects, such as stacking faults and nanotwins, at the bottom of the trench, leaving the upper part of the III-V film potentially defect free;[10,11] moreover, the low aspect ratio required to effectively trap defects[12] allows to reduce the III-V layer thickness, limiting the stress caused by the thermal expansion coefficient mismatch. However, antiphase boundaries (APB), which primarily form along {110} planes, and {111} planar defects oriented along the trench direction, cannot be trapped with this technique,[13,14] and propagate to the film surface becoming sources of scattering and carrier recombination. Within the ART approach, APB control has been achieved by engineering the trench bottom shape in order to enable double-step formation,[11,12] or by promoting the development of {111} facets during the Si fin etch step with alkaline solutions, such as potassium hydroxide,[15] tetramethylammonium hydroxide[16] or ammonium hydroxide (NH_4OH).[17] However, a method to prevent the propagation of {111} defects along the trench direction has not been yet proposed.

In this paper, we study the impact of the trench bottom geometry on the crystal quality of GaAs films, grown by metal-organic chemical vapor deposition (MOCVD) on 300 mm Si (001) wafers, using the ART approach. In particular, we investigate the influence of Si {111} facets intentionally created at the bottom of the trenches. The layers are characterized by cross sectional/plan view (PV) Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM), together with High Resolution X-Ray Diffraction (HRXRD). Particular attention is dedicated to the characterization of defects and the estimation of their density.

II. EXPERIMENTAL DETAILS

GaAs films were grown on patterned 300 mm on-axis Si (001) wafers in an AIXTRON CRIUS-R MOCVD system.

[a)]Author to whom correspondence should be addressed. Electronic mail: tommaso.orzali@sematech.org. Tel.: +1 518 649 1058.

 © 2015 AIP Publishing LLC

Reuse of AIP Publishing content is subject to the terms at: https://publishing.aip.org/authors/rights-and-permissions. Download to IP: 131.251.253.89 On: Mon, 09 May 2016 08:17:41

SEMI-standard 300 mm wafers with (001) silicon surface were used to fabricate test structures for III-V epitaxial experiments, where all line patterns were printed along the [110] axis, or at 45° to the [001] axis. A "short loop" process flow consisted on the formation of 180 nm thick thermal SiO_2 on Si, followed by lithography and reactive ion etching (RIE) of the oxide to define [110] oriented trenches, with an opening width of 65 nm and 130 nm pitch. The RIE step created a 15 nm deep Si recess at the bottom of the trenches, as shown in Figure 1(a), with ~6 nm of oxide over the Si (001) surface and 3 nm over the lateral {110} Si surfaces (Figure 1(b)). The trench length along [110] covered the full die lithographic field dimension, or 25.4 mm.

Substrate cleaning prior to deposition plays a critical role and strongly affects the quality of III-V films. The cleaning step is required to remove the SiO_2 from the silicon surface, and to passivate it with hydrogen, preventing the re-formation of native oxide when wafers are exposed to ambient atmosphere during transfer steps. Hydrogen passivation is achieved *in-situ* by the cleaning process and, depending on the ambient air conditions, is stable for several hours.

Cleaning and hydrogen passivation of Si wafers by vapor hydrogen fluoride (HF) and wet HF processes are described in detail in the literature.[18,19] In this development, we used both cleaning approaches to target different oxide removal thicknesses and selectively expose different Si facets, to study their effect on GaAs nucleation. Sample 1 was cleaned with the vapor HF/NH_3 process, targeted to remove 2–3 nm of silicon dioxide and leave the (001) surface at the trench bottom covered with a few nm of SiO_2, which prevented GaAs nucleation on that (001) surface. At the same time, the sidewalls at the very bottom of the trench recess became free of the oxide exposing Si {110} and {111} facets. Sample 2 was cleaned with the wet HF chemistry, to completely remove the oxide from the trench bottom and allow GaAs to nucleate on (001) as well. Sample 3 was cleaned with wet HF similar to sample 2, to completely remove SiO_2, and was subsequently subjected to a wet NH_4OH anisotropic etch, with the purpose of forming only preferential {111} Si facets and obtaining a "V" shaped trench bottom profile. As the last step, sample 3 was cleaned with the vapor HF/NH_3 process. After the cleaning, wafers were loaded in the MOCVD tool and kept under vacuum prior to deposition. All samples were first baked at high temperature (>800 °C) for a few minutes in pure H_2 ambient, to remove any native oxide that potentially formed during the transfer step to the MOCVD tool. During the high temperature bake step, samples 1 and 2 showed significantly faster thermal etch of trench bottom {110} planes compared to {111} planes, and the silicon region receded completely under the SiO_2 sidewalls, leaving only {111} facets exposed, along with the (001) plane. This could be explained by the lower surface energy associated with {111} planes. As a result, sample 1 had only {111} facets exposed, as (001) was still covered with a thin layer of oxide, while sample 2 exposed both {111} and (001) planes. Sample 3 alternatively exposed only {111} planes, with the typical "V" shape geometry.

The high temperature bake is also needed to promote the formation of double steps on Si (001) surface and prevent antiphase domains formation.[20] This was valid for sample 2, where Si (001) surface was exposed. Since double steps always form along one of the ⟨110⟩ directions,[21] we intentionally oriented the trenches along [110]. In samples 1 and 3, where Si (001) has been masked or etched away, the formation of APBs was avoided by nucleating GaAs only on {111} planes, as Si {111} single steps do not induce the formation of APBs during III-V heteroepitaxy.[14,30]

In order to evaluate the impact of the trench bottom geometry on the GaAs crystal quality, bake and growth conditions were kept the same for all three samples: GaAs films were grown at low pressure by using trimethylgallium as group-III precursors, and tertiarybutylarsine (TBAs), as well as arsine (AsH_3), as group V precursors. Pd-purified hydrogen was chosen as the carrier gas. All temperatures reported in this study are measured with a multi-channel pyrometer, allowing real-time surface temperature profile reading. The GaAs on Si growth process has been first developed on blanket wafers.[9] Considering that 50% of the wafer surface is covered by SiO_2 trenches, the precursors' flow rate used in Ref. 9 had to be reduced to compensate for loading effects and achieve the same growth rate inside the trenches.

After the bake, the Si surfaces were saturated with arsenic to insure charge neutrality along the interface and promote the growth of single domain GaAs:[20] this was achieved by introducing TBAs in the reactor at low temperature (<500 °C) before the GaAs nucleation step. Arsenic atoms adsorb on Si (001) and form a highly inert arsenic passivated

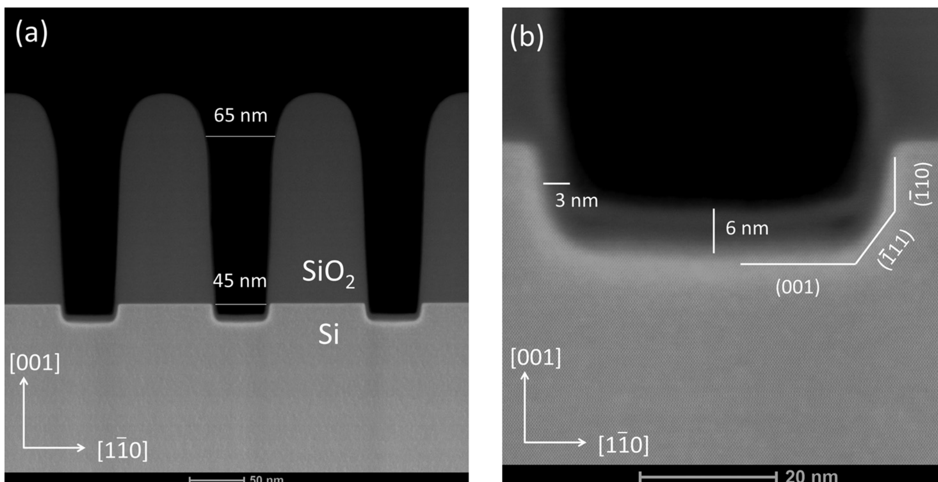

FIG. 1. (a) High-Angle Annular Dark Field Scanning Transmission Electron Microscopy (HAADF-STEM) image of the trench pattern cross section along [1$\bar{1}$0]. (b) High magnification HAADF-STEM image of the silicon recess at the trench bottom.

Reuse of AIP Publishing content is subject to the terms at: https://publishing.aip.org/authors/rights-and-permissions. Download to IP: 131.251.253.89 On: Mon, 09 May 2016 08:17:41

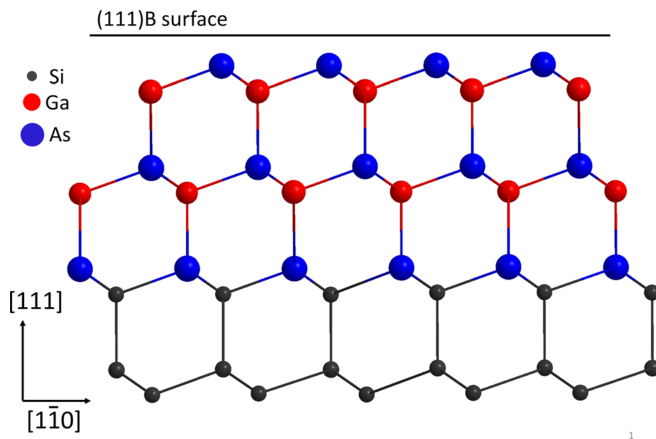

FIG. 2. Schematic representation of the GaAs on Si (111) interface. As substitutes Si at the topmost site of the Si (111) double plane. GaAs grows exposing the (111) B surface.

surface, self-limited to a single monolayer (ML) of coverage.[20] The same concept applies to Si {111}: arsenic passivates Si {111} with a chemically stable monolayer, which removes the (7×7) reconstruction and leaves a (1×1) surface, where As substitutes Si at the topmost site of the Si {111} double plane.[22] GaAs on Si (111) grows exposing the (111) B surface, as shown in Figure 2.

GaAs on Si films were grown in two steps: a GaAs low temperature nucleation layer was first deposited at $T < 450\,°C$ using TBAs with a low V/III ratio. Low temperature is required to limit Ga adatoms diffusivity and promote the formation of a high density of small nucleation islands, whose slow coalescence generates a smooth and closed GaAs layer on Si, in a quasi 2D growth mode. Another advantage of selectively growing on {111} facets comes from the fact that the energy balance for the growth of GaAs on Si (111) is lower than on Si (001), which allows promoting a Stranski-Krastanov, or "layer-plus-island," growth[23] instead of the 3D Volmer-Weber growth, as it is normally the case for GaAs on (001) Si.[29] Trenches were subsequently filled with the GaAs film grown at 615 °C and keeping a constant V/III ratio of 100 while using AsH_3 as a precursor.

III. RESULTS AND DISCUSSION

Figure 3(a) shows a low magnification top-down view SEM image of sample 1: dark lines correspond to SiO_2. Grey contrast in GaAs lines is directly related to the fins' height: brighter areas correspond to taller fins while dark spots indicate the presence of pits. The higher magnification image in the inset of Figure 3(a) points at the presence of tilted planar defects intersecting GaAs fins and generating a "V" shaped step at the top surface, as confirmed by the tilted view SEM image shown in Figure 3(b). Step edges tend to charge up in top view SEM and appear bright. Fin height non uniformities are evident in Figure 3(b).

In order to investigate the presence of tilted planar defects and correlate them with the fin morphology non-uniformities observed in Figure 3, we performed cross sectional TEM along [110], the direction parallel to the trenches. Figure 4(a) shows the cross sectional TEM micrograph of a pit in the GaAs fin: two dimensional translational Moiré fringes are visible at the trench bottom and are generated by the superposition of the Si and GaAs crystal lattices at the {111} interface. Several {111} planar defects, forming an angle of 54.7° with the (001) plane, nucleate at the trench bottom and intersect underneath the pit. Some kink and annihilate, others travel all the way up to the surface. The close up Scanning Transmission Electron Microscopy (STEM) image reported in Figure 4(b), a magnification of the area enclosed by the white square in Figure 4(a), allow classifying them as twins. Twin planes alter the stacking sequence of the GaAs zinc blende (ZB) crystal structure and are the prevalent defects observed in sample 1. Twin boundaries are suspected to act as scattering centers and significantly affect carriers' mobility, by inducing a strain field and thereby changing the carriers' effective mass.[24] The [111] oriented ZB GaAs crystal structure consists of alternating Ga and As monolayers, having a two dimensional triangular lattice of either Ga or As. Each monolayer can be classified into type A, B, or C, based on the lateral position occupied by the atoms in the lattice. In a perfect ZB crystal, the atoms stacking sequence along [111] is ··ABC|ABC··; the presence of a twin boundary changes the stacking sequence in ··BAC|ABC·· as schematized in Figure 4(b), where As and Ga atoms have been arbitrarily assigned. Twinned lamellae in the cross sectional TEM micrographs are only a few monolayers (ML) thick. Their presence seems to be related to the formation of the pit in Figure 4(a), as a local variation in growth rate can occur during the formation of the twin boundary or when two twinned planes kink and annihilate. Complete annihilation occurs when two kinking planes contain the same number of twinned ML, but it is only partial if they have different thicknesses, as shown in Figure 4(b), where a 3 ML twin meets a 6 ML one, and annihilates only 3 of its 6 ML.

Figure 5(a) reports the example of two thin twinned lamellae kinking almost at the fin's surface and creating a

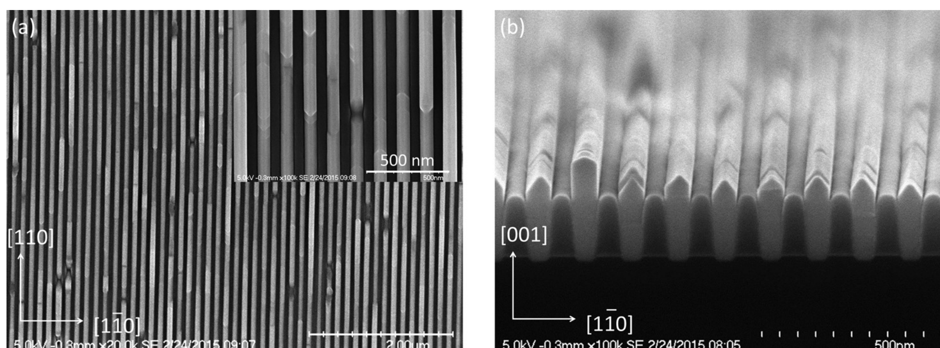

FIG. 3. Sample 1: (a) Top-down view SEM image of GaAs selectively grown in 180 nm deep SiO_2 trenches with a nominal width of 65 nm. Inset: high magnification top-down view SEM image. (b) Tilted view SEM image of a cross section along [1$\bar{1}$0].

Reuse of AIP Publishing content is subject to the terms at: https://publishing.aip.org/authors/rights-and-permissions. Download to IP: 131.251.253.89 On: Mon, 09 May 2016 08:17:41

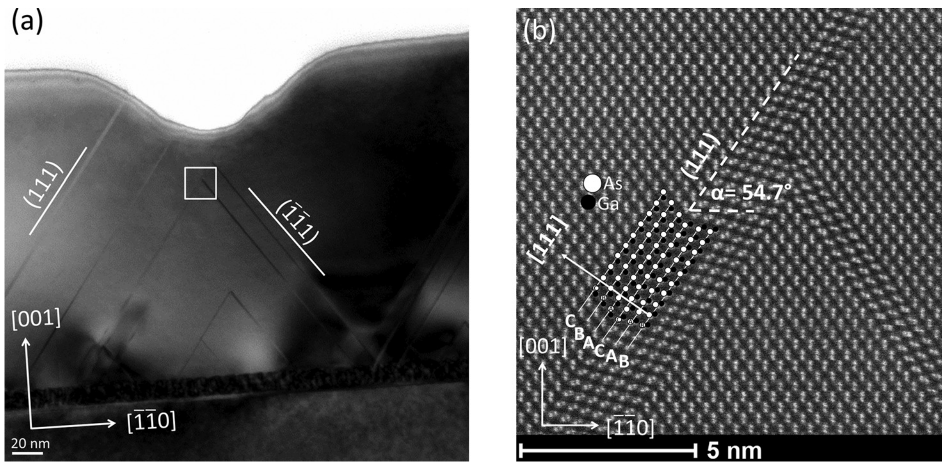

FIG. 4. Sample 1: (a) TEM dark field image of the cross section of a GaAs fins along [110], the direction parallel to the trenches. (b) HAADF-STEM of the area enclosed by the white square in Figure 4(a). The ball structural model schematically explains how the twin boundary changes the stacking sequence in ··BAC|ABC··; As (white) and Ga (black) atoms have been arbitrarily assigned.

shallow pit where they meet, as shown in the inset close-up STEM micrograph. Both twin planes originate at the GaAs/Si interface and travel all the way up to the surface, where they eventually meet, as indicated by the white dotted lines in Figure 5(a). According to these two examples, the higher the number of twinned lamellas and kinks stacked along the [001] direction, the larger the depth of the formed pit.

A closer inspection of the GaAs/Si interface along [110] in Figure 5(a) shows that twin boundaries mainly originate whenever the bottom oxide layer presents some roughness. Figure 5(b) reports a high resolution STEM image of the GaAs/Si interface: the dark horizontal band at the bottom is generated by the overlapping of GaAs and Si crystal lattices. At the bottom right of the micrograph, a SiO_2 hillock disrupts the GaAs crystal order creating a local strain field, as suggested by the dark region around it. The formation of a twinned plane is likely the mechanism of choice to release part of the stress in the GaAs crystal. Twin planes form easily as a result of their relatively low formation energy,[25] which can be normally overcome at the typical GaAs growth temperature. Nonuniformities in the oxide thickness can be either due to differential stress in the post-RIE Si surface, resulting in varying oxide growth, or due to variations in oxygen/silicon intermixing by energetic species in the RIE plasma. The high density of twin planes observed along [110] by cross sectional TEM explains the morphology irregularities detected in both planar and tilted view SEM images reported in Figure 3; steps seem to form when a single twin plane reaches the surface, while pits originate when several twin planes kink and annihilate along the [001] direction underneath the pit.

Figure 6 shows the cross sectional STEM micrograph along $[1\bar{1}0]$ where, after the vapor HF/NH_3 cleaning step, the trench width increases at the bottom and the top to 50 and 70 nm, respectively. From Figure 6, we estimate that the corresponding critical dimension (CD) loss is of the order of 3 nm/side, which is in a good agreement with the HF/NH_3 clean oxide removal target thickness. A thin $\sim$3 nm SiO_2 layer covers (001) Si surface at the bottom of the trench, leaving only Si {111} facets exposed for GaAs to nucleate. During the low temperature nucleation step, GaAs covers {111} planes with a few nm thick uniform layer. Two GaAs seeds nucleate, respectively, from $(1\bar{1}1)$ and $(\bar{1}11)$ Si facets, and coalesce during the following high temperature growth step, increasing the risk of stacking faults formation at the merging front;[21] these should nevertheless form on $(1\bar{1}1)$ and $(\bar{1}11)$ planes and get trapped at the oxide sidewalls. The darker region at the GaAs/Si interface is associated with a strain field in the III-V layer. Strain is released through the formation of {111} planar defects or threading dislocations that terminate at the oxide sidewalls, leaving the upper part of the fin free of defects. At these process conditions, GaAs fins expose {111} facets, as frequently reported within the ART approach:[10,13] the driving force for their formation is

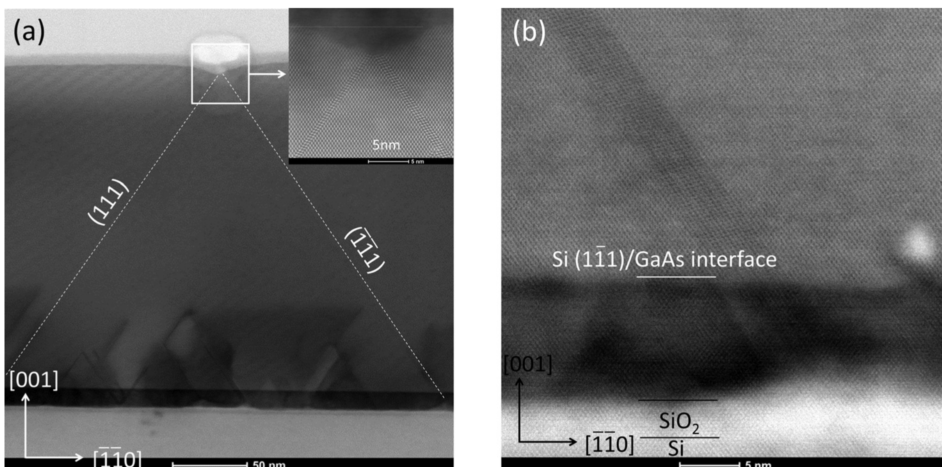

FIG. 5. Sample 1: (a) Bright Field STEM image of the cross section of a GaAs fins along [110]. Inset: high magnification HAADF-STEM of the shallow pit. (b) Bright Field STEM magnification of the GaAs/Si interface along [110].

Reuse of AIP Publishing content is subject to the terms at: https://publishing.aip.org/authors/rights-and-permissions. Download to IP: 131.251.253.89 On: Mon, 09 May 2016 08:17:41

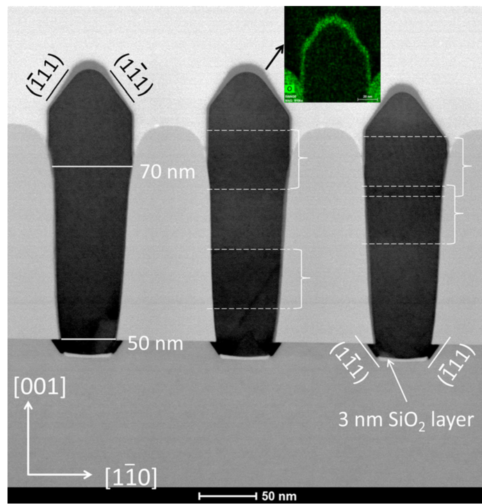

FIG. 6. Sample 1: bright Field STEM image of the cross section of GaAs fins along $[1\bar{1}0]$, the direction perpendicular to the trenches. Inset: (EDS)-TEM map of the Oxygen Kα peak.

believed to be the minimization of the oxide sidewall/III-V fin interfacial energy, which is achieved with the intrinsic reduction in contact area that occurs when {111} facets form.[26] The top of the GaAs fin is covered with a thin layer of native oxide that is expected to form when the sample is exposed to the ambient, as confirmed by the Energy Dispersive X-Ray Spectroscopy STEM-EDS map of the Oxygen Kα peak reported in the inset in Figure 6.

Dark horizontal bands are visible in the upper part of the fins and indicate the presence of (111) or $(\bar{1}\bar{1}1)$ twin planes intersecting the cross sectional TEM plane. The dotted white lines in Figure 6 indicate where the intersection occurs. High resolution TEM of the planes' intersection does not reveal any crystal periodicity disruption. This is expected, as twinned lamellae are generally only a few monolayers thick and their contribution to the overall sample thickness is minimal. No antiphase boundaries have been observed on this sample, confirming the assumption that III-V nucleation on Si {111} surfaces produces single crystal layers.

In order to remove completely from the Si (001) surface the residual silicon oxide present after the RIE step, and improve the control of the trench bottom roughness, we applied a long wet clean (3 min) with dilute HF (0.35%) on sample 2, targeting an oxide removal thickness of 7 nm. Pre-deposition bake and GaAs growth conditions were the same of sample 1. The top-down view SEM image reported in Figure 7(a) shows a much more uniform GaAs fin morphology, without pits and with reduced variability in the fins' height: bright areas correspond again to slightly taller fins, as shown in the tilted view SEM image reported in Figure 7(b) but, this time, there is no clear evidence of {111} planar defects intersecting the surface and creating steps or pits. The improved morphology uniformity suggests a significantly lower density of defects.

The cross sectional STEM micrograph along $[1\bar{1}0]$ (Figure 8(a)) shows the presence of voids over the Si (001) surface, suggesting that, despite the removal of the oxide isolation layer, GaAs nucleates preferentially on {111} facets. A similar behavior has been reported for both GaAs and InP nucleation on "V"-grooved Si (001),[27] and can be explained with the lower energy balance required for GaAs to nucleate on Si {111}. Si (001) contributes only partially to the growth. GaAs nucleates principally on $(1\bar{1}1)$ and $(\bar{1}11)$ facets; when the two growing fronts meet and the trench bottom is filled, the void is enclosed and GaAs growth proceeds along the [001] direction through {111} planes. Voids are defined by GaAs {111} planes, whose formation seems to be energetically favored to the development of a strained GaAs/Si (001) interface. An equilibrium condition is reached when the void covers almost a third of the (001) plane (inset in Figure 8(a)). Void dimensions vary along [110], as suggested by Figure 8(a), where the GaAs fin in the middle shows a constriction in the void tunnel. The absence of voids on sample 1 could be related to the presence of the amorphous SiO_2 layer, which does not have any epitaxial relationship with GaAs and hence prevents the buildup of lattice mismatch induced strain that makes the formation of the void energetically favored, as is the case for Si (001).

Due to the aggressive cleaning conditions adopted, the trench width increased to ~60 nm at the bottom and ~80 nm at the top, as shown in Figure 8(a), indicating a CD loss of ~7 nm/side. As a consequence of the larger trench width, the fin height results smaller, ~230 nm against the ~250 nm measured on sample 1. This is consistent with the attenuation of the loading effect due to the reduction in total SiO_2 covered area. Different types of defects originate at the GaAs/Si interface and terminate on the trench sidewalls. Both threading dislocations and stacking faults have been identified at the bottom of the trenches. The upper part of the fin appears free of defects: dark horizontal bands observed on sample 1 are not present this time, suggesting a lower density of (111)

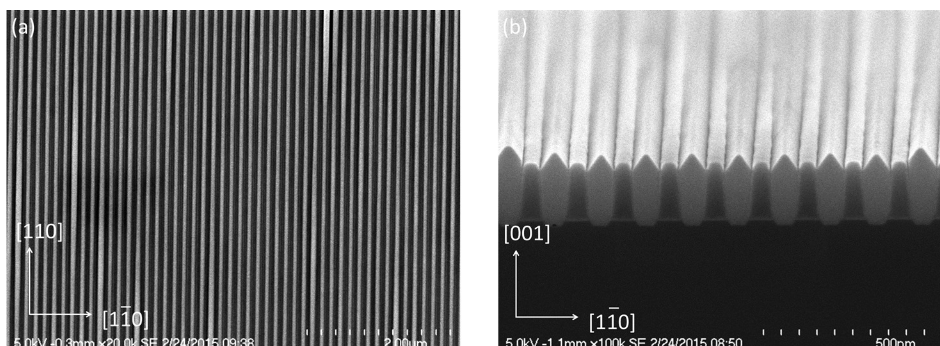

FIG. 7. Sample 2: (a) Top-down view SEM image. (b) Tilted view SEM image of a cross section along $[1\bar{1}0]$.

Reuse of AIP Publishing content is subject to the terms at: https://publishing.aip.org/authors/rights-and-permissions. Download to IP: 131.251.253.89 On: Mon, 09 May 2016 08:17:41

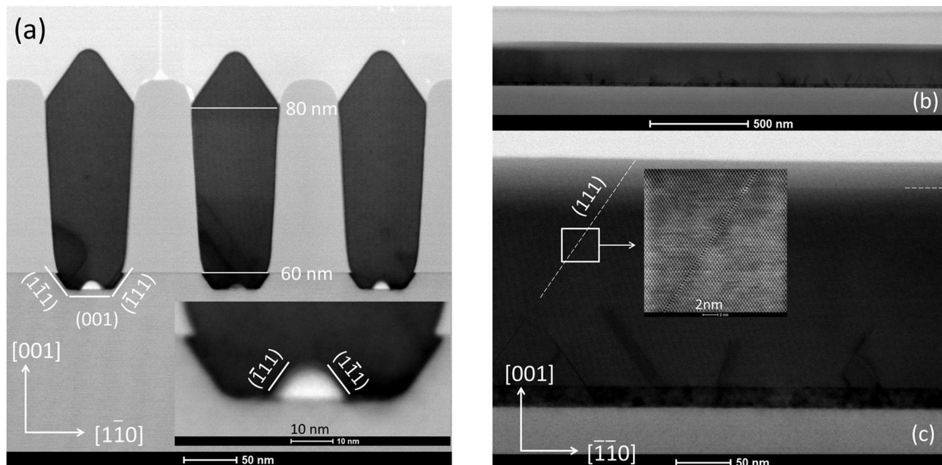

FIG. 8. Sample 2: (a) Bright Field STEM image of the cross section along [1$\bar{1}$0]. Inset: high magnification bright field STEM image of the trench bottom. (b) and (c) Low and high magnification BF-STEM images of the cross section along [110]. Inset: high magnification HAADF-STEM of the (111) planar defect.

or ($\bar{1}\bar{1}$1) planar defects, in agreement with the lower density of steps and pits observed in the SEM images.

Figures 8(b) and 8(c) show a low and a high magnification cross sectional STEM images along [110]. The dark band at the trench bottom is generated by the superposition of GaAs and Si crystal lattices in the trench recess; the dotted horizontal line in Figure 8(c) indicates the oxide sidewall top. Dark meandering lines in the lower half of the fin are threading dislocations annihilating on the oxide walls. The remaining upper half of the fin shows an overall low density of defects. Few {111} twin planes have been identified in the ~2.5 μm long portion inspected, but only a small number travel to the surface, as indicated by the dotted line in Figure 8(c): the high magnification STEM micrograph reported in the inset shows that it consists of a single monolayer thick twinned plane. The improved control of the trench bottom roughness seems to be responsible for the density reduction of twin planes compared to sample 1. The creation of voids at the GaAs/Si(001) interface may as well play a role in preventing the buildup of excessive stress in the growing film and its consequent relaxation through stacking faults formation.

The third sample investigated in this study was obtained by applying an NH_4OH anisotropic etch after the wet HF cleaning step, with the aim of removing completely the Si (001) surface and forming only {111} facets at the trench bottom, achieving the typical "V" shape geometry. The same pre-deposition bake and GaAs growth conditions of samples 1 and 2 were applied. Figure 9(a) shows the top view SEM image of [110] oriented GaAs fins: the contrast uniformity along the trenches suggests an excellent control of the growth rate and the fins' height. The tilted view SEM image in Figure 9(b) confirms the good fin morphology uniformity, and the absence of steps on the GaAs fin top in the sample portion investigated.

The cross sectional STEM image along [1$\bar{1}$0] allows to examine in detail the trench bottom shape (Figure 10(a)). A deep (~75 nm) "V" shaped groove is formed as a consequence of the NH_4OH etch, with {111} facets extensively undercutting the SiO_2 sidewalls for ~25 nm on both sides. The "V" groove apex is rounded, due to the presence of small {113} and (001) facets, as indicated in the inset in Figure 10(a), which likely form during the high temperature bake step. The trench width increased to ~70 nm at the bottom and ~90 nm at the top, indicating an overall CD loss of ~12 nm/side, 7 nm of which are attributed to the wet HF step. As in the previous cases, threading dislocations and stacking faults are confined at the trench bottom, leaving the upper part of the fin free of defects. Voids are present in the undercut area beneath the sidewalls and likely formed to minimize interfacial energy of the oxide sidewall/III-V fin. The total GaAs fin height is 225 nm, measured from the summit to the V shape apex but, due to the "V" groove depth of 75 nm, fins do not go beyond the trench sidewalls.

Figures 10(b) and 10(c) show, respectively, a low and a high magnification cross sectional STEM image along [110]. The dark band at the trench bottom is generated by the superposition of Si and GaAs crystal lattices in the "V" groove; the dotted horizontal line in Figure 10(c) indicates the oxide sidewall bottom. Very few {111} planar defects have been identified in the ~2.5 μm long portion inspected, and none of them reached the surface. All defects observed are

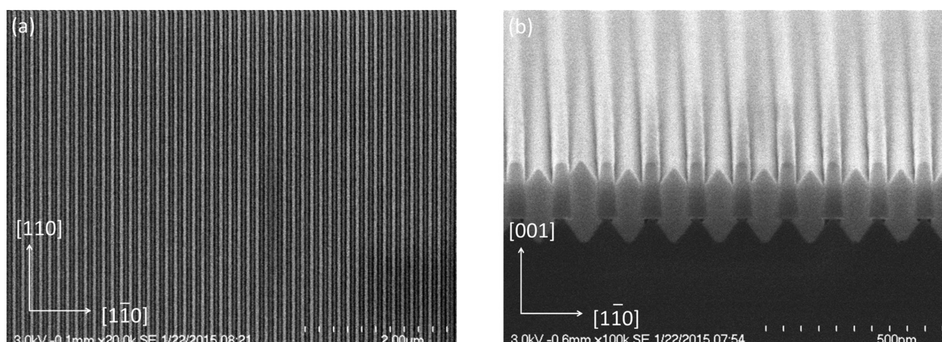

FIG. 9. Sample 3: (a) Top-down view SEM image. (b) Tilted view SEM image of a cross section along [1$\bar{1}$0].

Reuse of AIP Publishing content is subject to the terms at: https://publishing.aip.org/authors/rights-and-permissions. Download to IP: 131.251.253.89 On: Mon, 09 May 2016 08:17:41

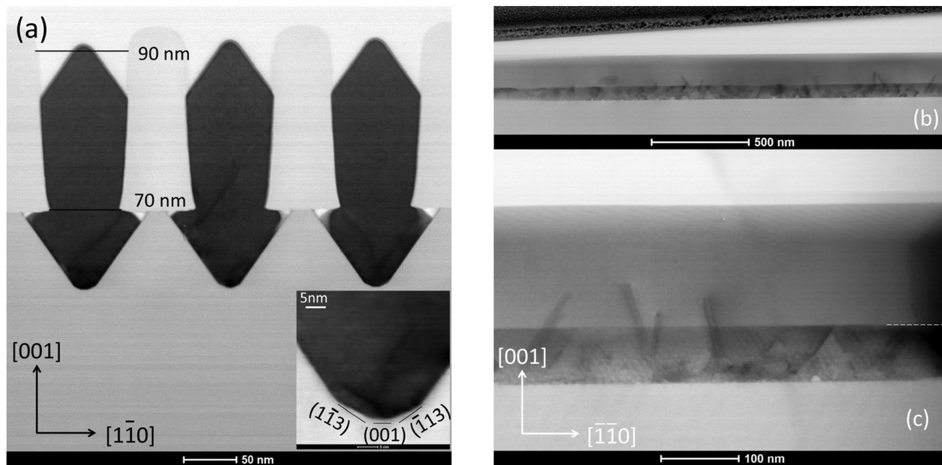

FIG. 10. Sample 3: (a) bright field STEM image of a cross section along [1$\bar{1}$0], the direction perpendicular to the trenches. Inset: high magnification bright field STEM image of the trench bottom. (b) and (c) Low and high magnification BF-STEM images of a cross section along [110], the direction parallel to the trenches.

confined at the trench bottom, making the upper part of the GaAs fin portion inspected free of defects.

A widely used technique to estimate the defect density in III-V layers is HRXRD. Two main measurements are usually performed: ω-2θ scans near the (004) symmetric reflection from the underlying substrate, to determine the films' composition, and ω-scans across selected peaks, to study defectiveness in the respective layers. The full width at half maximum (FWHM) of the ω-scan (rocking curve) is directly related to the concentration of defects that disrupt the perfect parallelism of atomic planes in the film. However, it contains information about highly defective interfaces in III-V heterostructures as well, due to the probe depth of X-rays being in the micrometer range. Despite this drawback, the technique is useful to compare relative defect densities between the layers of comparable thickness and composition. We performed ω-2θ scans and ω-scans of the GaAs (004) peak of the three samples, using an XRD setup aligned along [1$\bar{1}$0], i.e., perpendicular to the trenches direction. The results are reported in Figure 11: ω-2θ scans have been normalized to the intensity of the Si peak, and the same scaling factor has been applied to ω-scans. A completely relaxed GaAs layer has a lattice constant of 5.653 Å and a (004) symmetric peak separation with Si of -5538 arc s, in the ω-2θ scan. GaAs (004) peaks of all three samples overlap at ~ -5700 arc s, indicating tensile strain along [001]. Such strain is likely caused by the thermal expansion coefficient mismatch between GaAs (5.73×10^{-6} °C^{-1}) and SiO_2 ($\sim 5.6 \times 10^{-7}$ °C^{-1}, depending on the oxide density). Assuming that the thermal expansion coefficients are independent from the temperature, the thermal strain can be expressed with $E_{th} = (\alpha_f - \alpha_s) \times (T_g - T_r)$, where α is the thermal expansion coefficient of the film (α_f) and the substrate (α_s), which in this case are the oxide sidewalls, and T_g is the growth temperature, while T_r is the room temperature. If $\alpha_f > \alpha_s$, $E_{th} > 0$, tensile stress is applied on the epi layer (and a compressive stress is applied on the oxide sidewalls). The formation of twin planes likely contributes to partially release the tensile strain. The slight GaAs peak position shift towards the left of sample 3, indicating higher strain compared to samples 1 and 2, could hence explain its lower density of twins. The ω-scan FWHM of GaAs (004) peaks is reported in Figure 11(b) and is in good agreement with the cross sectional TEM estimation of the defect density. Samples 1, 2, and 3 have, respectively, a GaAs (004) FWHM of 1328, 959, and 647 arc s. In Ref. 10, Li *et al.* reported a low record FWHM of 190 arc s for MOCVD grown GaAs on Si ART with a thickness of 1.5 μm. However, as already mentioned, this technique is useful to compare relative defect densities between layers of comparable thickness, as thicker films give smaller FWHM. As a matter of fact, by increasing the GaAs fin height of Sample 3 from 225 nm to 420 nm, we observed an FWHM reduction to 443 arc s.

The most reliable technique to estimate the defect density of epitaxial films is PV TEM. We report in Figure 12(a) the PV-STEM micrograph of sample 2. The bright stripes correspond to the silicon oxide sidewalls while the dark stripes indicate the GaAs fins. The highly defective trench bottom has been removed during the preparation of the TEM lamella, and only the upper part of the GaAs fins with a low defect density, which includes the {111} top facets, has been

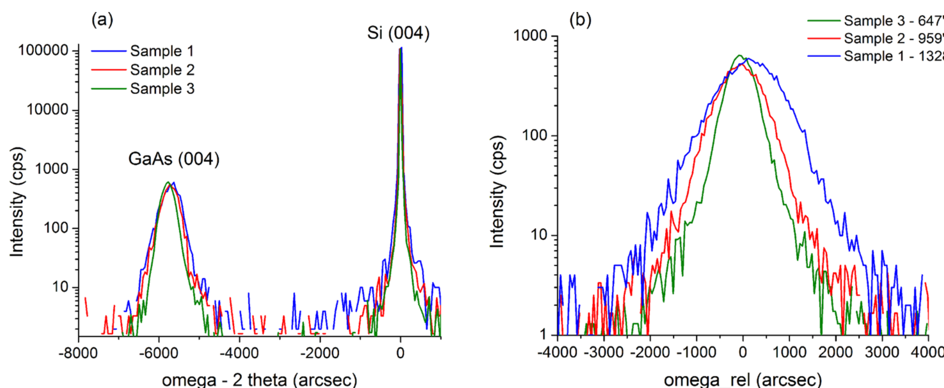

FIG. 11. (a) HRXRD ω-2θ scans near the Si (004) symmetric reflection and (b) ω-scans across GaAs (004) peaks of samples 1, 2, and 3. The respective ω-scans FWHM values are reported in the legend.

Reuse of AIP Publishing content is subject to the terms at: https://publishing.aip.org/authors/rights-and-permissions. Download to IP: 131.251.253.89 On: Mon, 09 May 2016 08:17:41

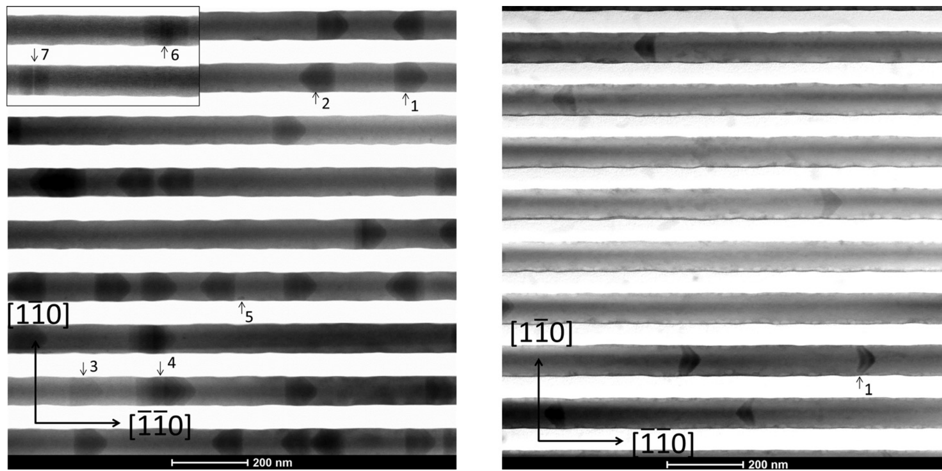

FIG. 12. (a) Plan-view bright field STEM image of a 1.2 μm × 1.2 μm portion of sample 2. Inset: another area of the same sample showing twin planes kinking and annihilating. (b) Plan-view bright field STEM image of a 1.2 μm × 1.2 μm portion of sample 3.

inspected. Shaded areas along the fins correspond to twin planes intersecting the TEM lamella: the edge of the twin plane intersecting the {111} faceted fin top has a triangular shape in PV-STEM, while the opposite edge intersecting the lower surface of the lamella appears like a vertical line oriented along [1$\bar{1}$0]. Two single twin planes propagating in opposite directions have been highlighted with numbers 1 and 2 in Figure 12(a), and indicate a (111) and a ($\bar{1}\bar{1}$1) twin, respectively. Background contrast non-uniformities along the lines correspond to slight sample thickness variations or fin height differences. For example, defects 1 and 2 look much darker than defect 3, where the TEM lamella is thinner. Several twin planes can overlap along the [001] direction, as in the case of defect number 4, which consists of a stack of 4 parallel twinned (111) planes. The higher the number of twin boundaries overlapping along [001], the darker the area appears on PV-STEM. Defect number 5, as well as all line defects at the very edge of the trenches, are threading dislocation trapped at the bottom of the trench. The defect highlighted with number 6 in the inset of Figure 12(a) identifies two twin planes kinking and partially annihilating, with the thicker one reaching the surface, similar to what was reported in Figure 4(b). Defect 7 instead identifies two twin planes kinking and completely annihilating. Counting the defects on a $2.5 \times 2.5\,\mu$m area gave a twin plane density of $\sim 3 \times 10^9\,\mathrm{cm}^{-2}$.

Figure 12(b) reports the PV-STEM of sample 3 which shows, as expected, a lower density of planar defects. The planar defect density calculated over a $2.5 \times 2.5\,\mu$m area is $\sim 8 \times 10^8\,\mathrm{cm}^{-2}$. Background contrast non-uniformities along the lines correspond again to slight sample thickness variation or fin height differences. Due to the depth of the "V" shaped groove, a higher portion of the highly defective trench bottom had to be removed during the preparation of the TEM lamella; nonetheless, defects terminating at the oxide sidewalls are still visible in the PV-TEM micrograph. None of them reaches the fin surface. In Figure 12(b), a few nanotwins have a striped contrast as, for example, the defect highlighted with number 1. This is a consequence of a small off-axis tilt on some of the fins that bent during the sample preparation, and is a normal occurrence for very thin TEM lamellas.

Ultimately, no APBs have been observed in any of these plan-view micrographs, confirming that {111} mediated growth promotes the formation of single domain GaAs films.

The higher density (4×) of twin planes observed in sample 2 can be attributed to the presence of the Si (001) plane at the trench bottom. Despite the formation of voids that cover a third of the GaAs/Si (001) interfacial area, the (001) plane is still involved in the GaAs nucleation step and generates additional stress in the layer. Twin planes are not usually observed on blanket GaAs on Si (001), where TD are the most common type of defects encountered,[9] but have often been reported in III-V ART samples.[14,28] This suggests that the layer confinement between oxide sidewalls might have a role in their formation, either because of the thermal expansion coefficient mismatch between silicon oxide and III-V layers, or because of the oxide sidewalls' roughness that locally generates stress in the growing layer, inducing the formation of twinned planes as the preferred mechanism of stress relaxation, as observed in sample 1. As a matter of fact, PV-STEM clearly shows that oxide sidewalls are not perfectly flat and do show finite roughness contributing to their slightly ragged profile. An in-depth discussion on nanotwins' formation mechanism in the ART samples is beyond the scope of this study. However, it is worth mentioning that Li *et al*. demonstrated defect free GaAs on Si grown on 270 nm wide trenches.[31] If twin planes form as a consequence of the tensile strain generated by the thermal expansion coefficient mismatch between GaAs and SiO_2, increasing the GaAs to SiO_2 volume ratio should help minimizing strain and preventing the formation of twin planes. The trench width of 270 nm used in Ref. 31 gives a GaAs to SiO_2 volume ratio almost 3 times larger than in this study, and could indeed explain the absence of nanotwins.

Defect density evaluation through plan-view and cross sectional TEM, even if accurate and unavoidable for process development, is destructive, expensive, and time consuming, therefore not ideal in a high volume manufacturing environment. We demonstrated that a complementary non-destructive approach that uses the combination of plan-view SEM, to inspect fin morphology non-uniformities, and HRXRD, to measure the III-V layers' rocking curve FWHM, allows for a fast defect density evaluation that can be

Reuse of AIP Publishing content is subject to the terms at: https://publishing.aip.org/authors/rights-and-permissions. Download to IP: 131.251.253.89 On: Mon, 09 May 2016 08:17:41

adopted as useful in-line metrology technique in a hybrid 300 mm III-V/Si Fab.

IV. CONCLUSIONS

In conclusion, we have used the ART approach to study the impact of three different trench bottom geometries on the crystal quality of GaAs fins grown in sub-100 nm trenches patterned on 300 mm Si (001) substrates. A high density of twin planes propagating along the trench direction has been observed in all samples. The lowest density of $\sim 8 \times 10^8\,\text{cm}^{-2}$ was obtained on "V" shaped bottom trenches, where GaAs nucleation occurs only on {111} Si planes, minimizing the interfacial energy and preventing the formation of antiphase boundaries. Despite the absence of APB and TD in the samples' portions inspected, twin planes propagating along the trench direction cannot be trapped with the ART approach. Twin boundaries are suspected to act as scattering centers, and their density will have to be significantly reduced before GaAs fins on Si could be used in photonic or logic applications. It is not clear whether their formation is intrinsic to the confined growth inside SiO_2 trenches or can be prevented through process optimization steps that aim at reducing the tensile strain in GaAs layers or at minimizing the oxide sidewall surface roughness.

[1]Y. Halioua, A. Bazin, P. Monnier, T. J. Karle, G. Roelkens, I. Sagnes, R. Raj, and F. Raineri, Opt. Express **19**(10), 9221–9231 (2011).
[2]K. Tanabe, K. Watanabe, and Y. Arakawa, Sci. Rep. **2**, 349 (2012).
[3]J. A. del Alamo, Nature **479**(7373), 317 (2011).
[4]G. Dewey, B. Chu-Kung, R. Kotlyar, M. Metz, N. Mukherjee, and M. Radosavljevic, 2012 Symposium on VLSI Technology (VLSIT) (2012), p. 45.
[5]M. Heyns *et al.*, in Proceedings of International Electron Devices Meeting (IEDM), 2011, p. 13.1.1.
[6]M. Yokoyama, R. Iida, S. H. Kim,N. Taoka, Y. Urabe, T. Yasuda, H. Takagi, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka, and S. Takagi, in *Proceedings of IEEE International Electron Devices Meeting* (IEDM), p. 3.1.1–3.1.4.
[7]N. J. Quitoriano and E. A. Fitzgerald, J. Appl. Phys. **102**, 033511 (2007).
[8]Q. Li, C. Wah Tang, and K. May Lau, Appl. Phys. Express **7**, 045502 (2014).
[9]T. Orzali, T.-W. Kim, A. Vert, G. Huang, J. L. Herman, S. Vivekanand, P. Y. Hung, M. Kelman, R. J. W. Hill, Z. Karim, and S. Papa Rao, J. Cryst. Growth **427**, 72–79 (2015).
[10]J. Z. Li, J. Bai, C. Major, M. Carroll, A. Lochtefeld, and Z. Shellenbarger, J. Appl. Phys. **103**, 106102 (2008).
[11]G. Wang, M. R. Leys, R. Loo, O. Richard, H. Bender, N. Waldron, G. Brammertz, J. Dekoster, W. Wang, M. Seefeldt, M. Caymax, and M. M. Heyns, Appl. Phys. Lett. **97**, 121913 (2010).
[12]R. Loo, G. Wang, T. Orzali, N. Waldron, C. Merckling, M. R. Leys, O. Richard, H. Bender, P. Eyben, W. Vandervorst, and M. Caymax, J. Electrochem. Soc. **159**(3), H260–H265 (2012).
[13]R. Cipro, T. Baron, M. Martin, J. Moeyaert, S. David, V. Gorbenko, F. Bassani, Y. Bogumilowicz, J. P. Barnes, N. Rochat, V. Loup, C. Vizioz, N. Allouti, N. Chauvin, X. Y. Bao, Z. Ye, J. B. Pin, and E. Sanchez, Appl. Phys. Lett. **104**, 262103 (2014).
[14]M. Paladugu, C. Merckling, R. Loo, O. Richard, H. Bender, J. Dekoster, W. Vandervorst, M. Caymax, and M. Heyns, Cryst. Growth Des. **12**(10), 4696–4702 (2012).
[15]H. Seidel, L. Csepregi, A. Heuberger, and H. Baumgärtel, J. Electrochem. Soc. **137**(11), 3612–3626 (1990).
[16]K. Biswas and S. Kal, Microelectron. J. **37**, 519 (2006).
[17]W. Kern, "Chemical Etching of Silicon, Germanium, GalliumArsenide, and Gallium Phosphide," RCA Rev. **39**, 278 (1978).
[18]D. B. Fenner, D. K. Biegelsen, and R. D. Bringans, J. Appl. Phys. **66**(1), 419–424 (1989).
[19]M. Tomoyasu, M. L. Funk, K. A. Pinto, M. Odagiri, L. Chen, A. Yamashita, and H. Takahashi, U.S. patent No. 7,877,161, U.S. Patent and Trademark Office, Washington, DC, 2011.
[20]S. M. Ting and E. A. Fitzgerald, J. Appl. Phys. **87**(5), 2618 (2000).
[21]K. Volz, A. Beyer, W. Witte, J. Ohlmann, I. Nemeth, B. Kunert, and W. Stolz, J. Crys. Growth **315**(1), 37–47 (2011).
[22]O. Sakata, H. Hashizume, and H. Kurashina, Phys. Rev. B **48**(15), 11408 (1993).
[23]H. Y. Xu, Y. N. Guo, Y. Wang, J. Zou, J. H. Kang, Q. Gao, H. H. Tan, and C. Jagadish, J. Appl. Phys. **106**, 083514 (2009).
[24]K. Shimamura, Z. Yuan, F. Shimojo, and A. Nakano, Appl. Phys. Lett. **103**, 022105 (2013).
[25]F. J. Glas, Appl. Phys. **104**, 093520 (2008).
[26]S. Jiang, C. Merckling, W. Guo, N. Waldron, M. Caymax, W. Vandervorst, M. Seefeldt, and M. Heyns, J. Appl. Phys. **115**, 023517 (2014).
[27]A. Krost, R. F. Schnabel, F. Heinrichsdorff, U. Rossow, D. Bimberg, and H. Cerva, J. Cryst. Growth **145**, 314–320 (1994).
[28]S. W. Kim, Y. D. Cho, C. S. Shin, W. K. Park, D. H. Kim, and D. H. Ko, J. Cryst. Growth **401**, 319–322 (2014).
[29]Yu. B. Bolkhovityanov and O. P. Pchelyakov, Phys.-Usp. **51**(5), 437–456 (2008).
[30]J. R. Patel, P. E. Freeland, M. S. Hybertsen, and D. C. Jacobson, Phys. Rev. Lett. **59**, 2180 (1987).
[31]J. Z. Li, J. Bai, J.-S. Park, B. Adekore, K. Fox, M. Carroll, A. Lochtefeld, and Z. Shellenbarger, Appl. Phys. Lett. **91**, 021114 (2007).

Reuse of AIP Publishing content is subject to the terms at: https://publishing.aip.org/authors/rights-and-permissions. Download to IP: 131.251.253.89 On: Mon, 09 May 2016 08:17:41