

Balancing Control for Grid-scale Battery Energy Storage Systems



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ABSTRACT

Grid-scale battery energy storage systems (BESSs) are becoming increasingly attractive as the connection of a BESS has been shown to improve the dynamic behaviours of the power grid. A key problem with BESSs is the potential for poor utilisation of mismatched cells and reliability issues resulting from the use of a large number of cells in series. This thesis proposes a technique for state-of-charge balancing of many thousands of cells individually (i.e. not in packs) using a tightly integrated power electronic circuit coupled with a new control system design. Cells are organised in a hierarchical structure consisting of modules, sub-banks, banks and phases. The control strategy includes five levels of balancing: balancing of cells within a module, balancing of modules within a sub-bank, sub-banks within a bank, banks in a phase and balancing between phases. The system seeks to maximise the accessible state-of-charge range of each individual cell, thereby enhancing the overall capacity of the system. The system is validated in simulation for a 380 kWh BESS using 2835 lithium-ion cells where charge balancing is demonstrated for mismatched cells. A ‘peak sharing’ concept is implemented to manage voltage constraints so that alternative modules assume a portion of the load when certain modules are not capable of meeting the demand. An experimental validation has been performed to demonstrate the effectiveness of the balancing control. This work is intended to address the challenges of eventual scaling towards a 100 MWh+ BESS, which may be composed of hundreds of thousands of individual cells.

DECLARATION

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DEDICATION

For Guan Jiunn

For Zhe Swen

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ACRONYMS

AC	Alternating Current
BESS	Battery Energy Storage System
BMS	Battery Management System
CSC	Current Source Converter
DC	Direct Current
DOD	Depth-of-discharge
DQ	Direct-quadrature
ESS	Energy Storage System
FPGA	Field Programmable Gate Array
GTO	Gate-turn-off
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commuted Thyristor
Li-ion	Lithium-ion
MML	Modular Multi-level
MOSFET	Metal-oxide-semiconductor Field-effect Transistor
MV	Medium-voltage
NaS	Sodium-sulphur
NiCd	Nickel-cadmium
NiMH	Nickel-metal Hydride
OCV	Open Circuit Voltage
PCC	Point of Common Coupling

PCS	Power Conversion System
PI	Proportional-integral
PLL	Phase-locked-loop
PWM	Pulse-width Modulation
SEI	Solid-electrolyte Interface
SM	Sub-modules
SoC	State-of-charge
SoH	State-of-health
VCO	Voltage Controlled Oscillator
VHDL	VHSIC (Very High Speed Integrated Circuit) Hardware Description Language
VSC	Voltage Source Converter

NOMENCLATURE

Ampere-hour (Ah) efficiency: The quantity of electricity measured in Ampere-hours which may be delivered by a cell or battery under specified conditions.

Ampere-hour capacity: The total number of Ampere-hours or watt-hours that can be withdrawn from a fully charged cell, indicated by Ah or mAh.

Battery: Two or more electrochemical cells connected together electrically in series, parallel, or both, to provide the required operating voltage and current levels.

C-rate: Charge or discharge current, in Ampere, expressed in multiples of the rated capacity. For example, C/10 charge current for a cell rated at 20 Ah is: $20 \text{ Ah}/10 = 2 \text{ A}$.

Capacity: See Ampere-hour capacity.

Cell: The smallest electrochemical unit of a battery used to generate or store electrical energy.

Coulombic efficiency: See Ampere-hour efficiency.

Cut-off voltage: The cell voltage at which the discharge process is terminated (it is generally a function of discharge rate).

Cycle life: The number of times a cell can be discharged and re-charged until the cell capacity drops to a specified minimum value usually 80 % of rated capacity.

Depth of discharge: The quantity of electricity (Ampere-hours) removed from a fully charged cell, expressed as a percentage of its rated Ampere-hour capacity.

Energy density: The ratio of the energy available from a cell to its volume (Wh/L) or mass (Wh/kg).

Internal resistance: Expressed in ohms, the total DC resistance to the flow of current through internal components (grids, active materials, separators, electrolyte, straps, and terminal) of a cell.

Module: The smallest modular unit, consisting of a number of individual cells connected together electrically in series, parallel, or both.

Nominal voltage: The average voltage of the cell. The operating voltage of the system may go above or below this value.

Open circuit voltage (OCV): The difference in potential between the terminals of a cell when no load is applied.

Pack: Two or more modules connected in series, parallel or both.

Power density: The ratio of the available power from a cell to its volume (W / L).

Round-trip efficiency: The ratio of energy put in (in MWh) to energy retrieved from storage (in MWh).

Self-discharge: The loss of useful capacity of a cell on storage due to internal chemical action (local action) and parasitic currents.

State-of-charge (SoC): The present cell capacity in relation to maximum capacity.

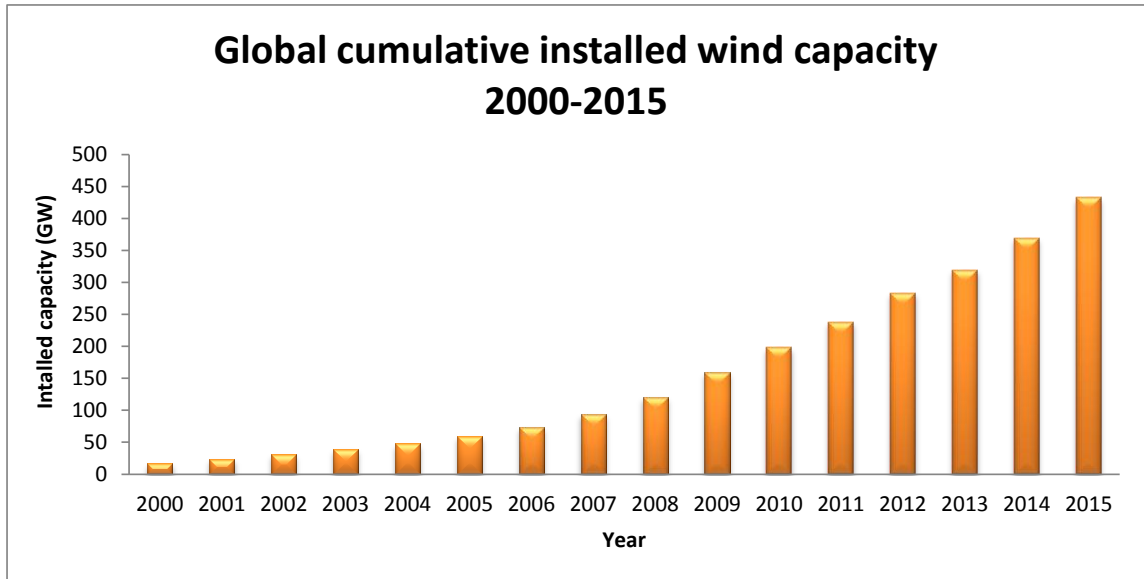
Terminal voltage: The difference in potential between the terminals of a cell when a load is applied.

CHAPTER 1 INTRODUCTION

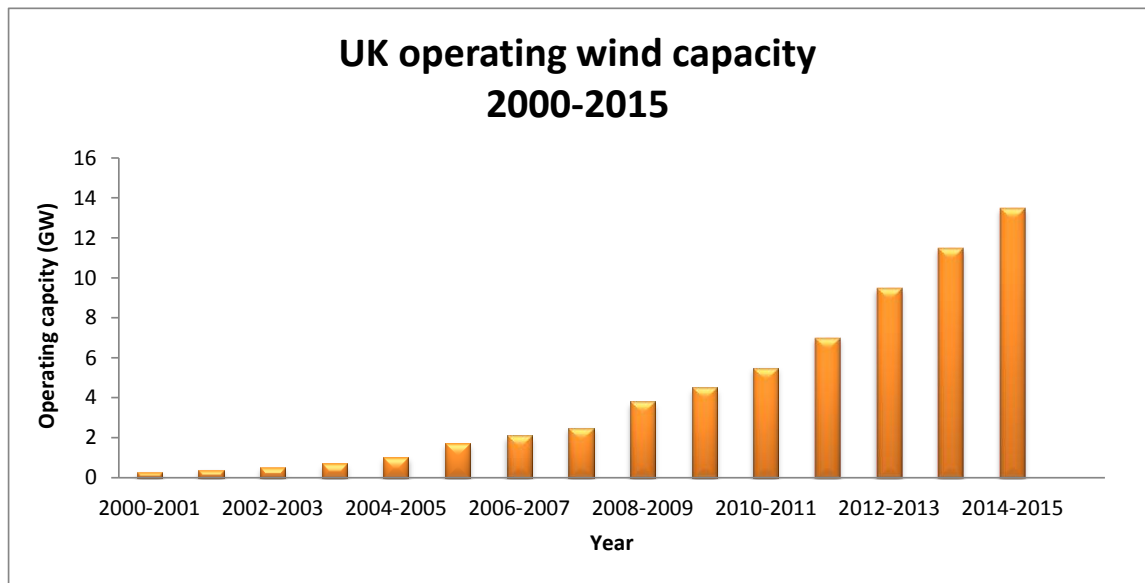
1.1 Background

Driven by the desire to reduce greenhouse emissions, there has been a renewed push to minimise the use of traditional fossil fuels for electric energy generation [1-3]. The UK has adopted a number of policies promoting decarbonisation of the electricity sector. As part of meeting the target for reducing overall UK greenhouse gas emissions by 80 % by 2050, these policies mandate that 15 % of its total energy must come from renewable energy resources by 2020 [4], which have led to an increasing market penetration of renewable energy resources such as wind and solar [5-7]. Figure 1.1(a) depicts the global cumulative installed capacity of wind power, while Figure 1.1(b) shows the operating capacity of wind power in the UK context from 2000 to 2015. Global installed wind capacity has grown at an average rate of 23 % per year over the last ten years (since 2005), reaching more than 430 GW by the end of 2015. The Global Wind Energy Council (GWEC) predicts that wind power could provide 25-30 % of global electricity supply by 2050 [8-9].

However, the introduction of large quantities of intermittent generation along with changes in demand patterns, such as widespread adoption of electrical vehicle charging [10-11], poses great challenges for future electrical networks [12-14]. Very rapid, large fluctuations in power flow caused by variations in wind and solar generation can severely affect the control of voltage and frequency on the grid [15-16] and introduce issues with system stability, reliability and power quality [17-19].



(a)



(b)

Figure 1.1(a) Global cumulative installed wind capacity 2000-2015, (b) UK operating wind capacity 2000-2015 (adapted from [1] [8-9])

There are different approaches to mitigate intermittency of generation such as increasing or decreasing flexible generation, demand-side management, network solutions such as reinforcements and investment in interconnection, transmission and/or distribution networks [20], or through the use of energy storage system (ESS), which can absorb or release energy to buffer the mismatch between generation and load over periods of minutes to hours [21].

Energy storage in an electricity generation and supply system enables the decoupling of electricity generation from demand to deal with the intermittency of renewable energy resources and the unpredictability of their outputs. The electricity that can be produced at times of either low-demand low-generation cost or from intermittent renewable energy resources is stored and shifted in time for release at times of high-demand high-generation cost or when the load is greater than the generation. Appropriate integration of renewable energy resources with ESSs provides an important approach for a greater market penetration and results in primary energy and emission saving [22].

ESSs have various grid applications covering a wide spectrum, ranging from large-scale generation and transmission-related systems, to distribution networks and customers. These applications include increasing the renewable energy penetration, improving the power quality and stability, load leveling, peak shaving, frequency control, upgrading the transmission line capability, and mitigating the voltage fluctuations [21-23]. Figure 1.2 shows the characteristics for several ESSs in terms of power rating, which identifies potential grid applications, and duration of discharge, indicating the suitability of each ESS to utility applications. The use of pumped hydro and compressed air ESSs has been motivated by the need for long life cycles where the stored energy is used for real-time or

short notice support and optimisation of the generation, transmission and distribution (G, T & D) ranged from milliseconds to few minutes [24-25].

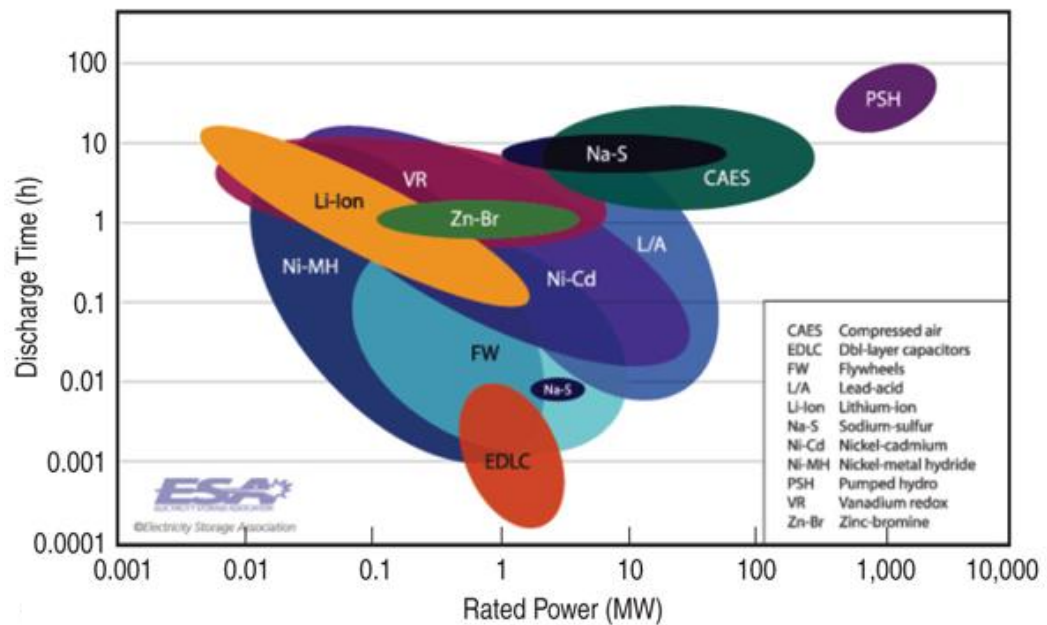


Figure 1.2 Potential grid applications for ESSs [23]

In the past decade, a broad portfolio of energy storage technologies has emerged from new modular pumped hydro with reservoirs that have less environmental impact than earlier concepts, to supercapacitors, a large family of batteries, superconducting magnetic energy storage, flywheels, synthetic natural gas, and others. Figure 1.3 classifies storage technologies into mechanical, electrochemical, chemical, electrical and thermal ESSs according to the form of energy used.

As indicated in Figure 1.2, there are several ESSs that are based on batteries. Battery energy storage systems (BESSs) are a promising technology for grid applications as they can deliver fast and flexible dynamic response; they are able to react to grid demands nearly instantaneously. BESSs provide a wide range of energy storage capacity up to 100 MWh with high efficiency [24-26]. BESS is a valuable, fast reacting contribution especially

for buffering the energy difference between short-term predictions and measurements of wind and solar generation.

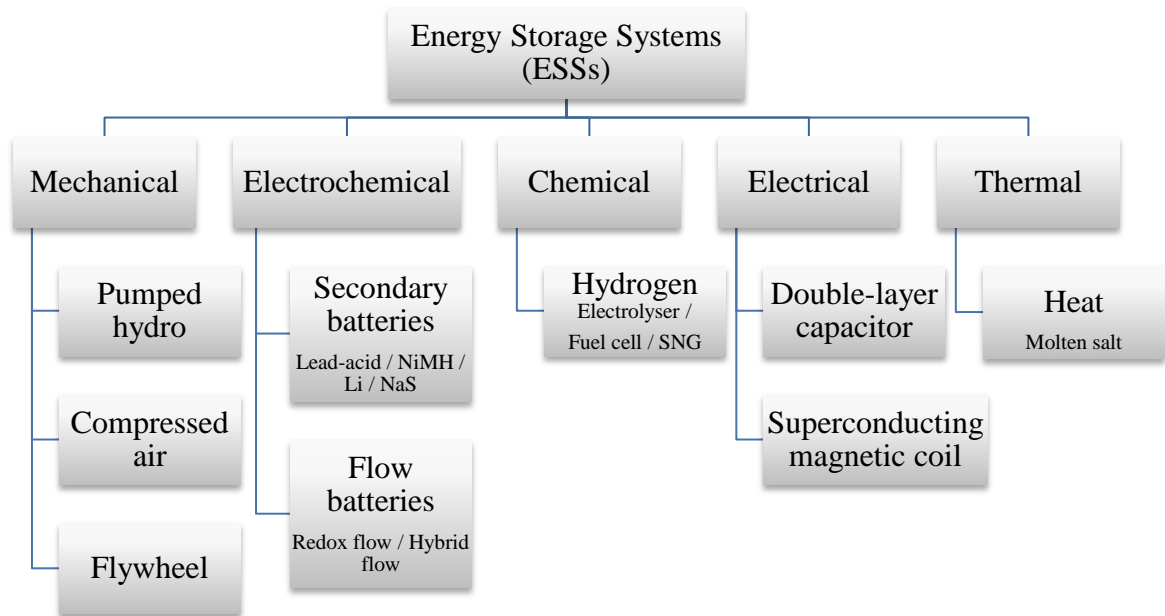


Figure 1.3 Classification of ESSs according to energy form

Figure 1.4 shows power and energy densities for different secondary battery technologies which helps to identify the optimal operative range for each technology; most of these technologies are currently being investigated for grid-scale BESSs. Lithium-ion (Li-ion) technologies outperform competing technologies such as Nickel-metal hydride (NiMH), Nickel-cadmium (NiCd), and lead-acid in terms of energy density while providing high specific power.

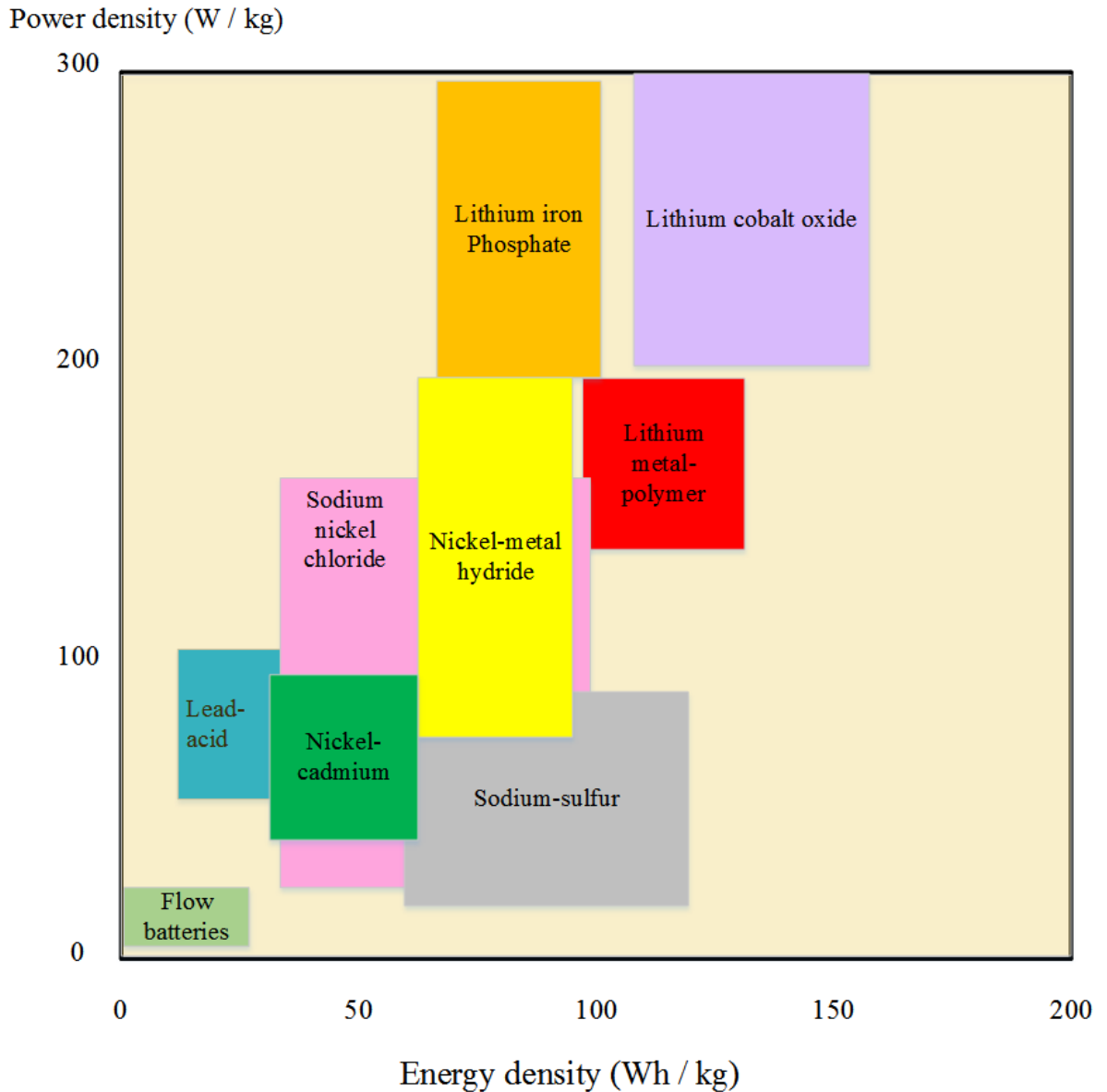


Figure 1.4 Power and energy densities for different secondary battery technologies (adapted from [27-29])

Figure 1.5 shows the integration of solar and wind power to the grid with a BESS where the BESS stores energy when excess power is generated and releasing it at times of greater demand, which performs load leveling.

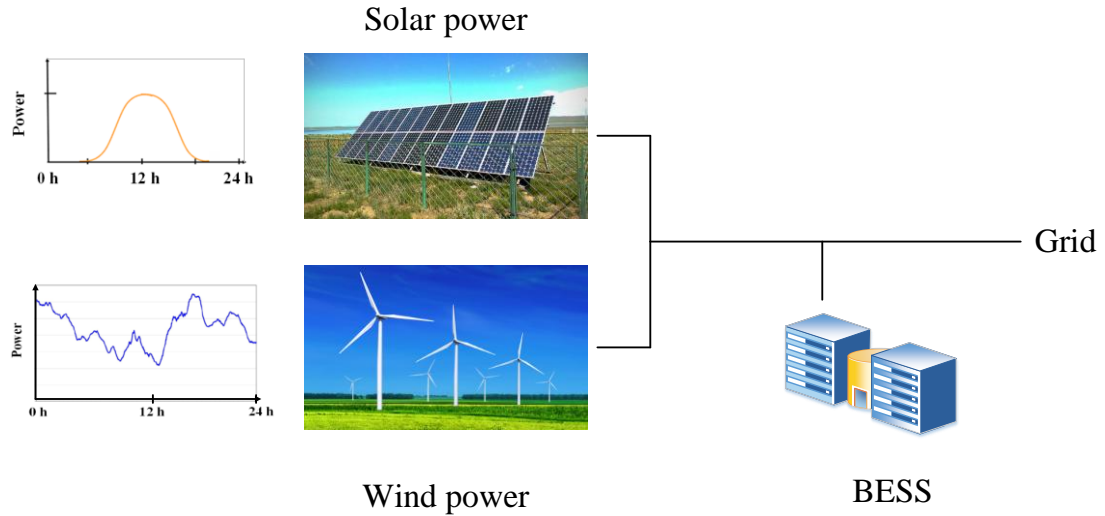


Figure 1.5 Integration of wind and solar into the grid with a BESS

Grid support using several types of battery technologies has been studied extensively and the connection of a BESS to the grid has been shown to improve the dynamic behaviours of the power grid [30]. Li-ion cells, in particular, are the subject of much interest due to several advantages [31]. The latest technologies such as lithium iron phosphate and nano-lithium titanate oxide have addressed important aspects such as cell safety, calendar life and fast charge capability [32]. However, cell variation arising due to manufacturing tolerances and as a result of differing operating conditions across a set of cells remains a key problem, leading to unequal state-of-charge (SoC) occurring between cells within a battery pack. Over many charge and discharge cycles, differences between cells can cause major failures due to the overcharging or deep discharging of individual cells, leading to serious deterioration in system performance [33]. Although some of these dangers can be mitigated by limiting charge–discharge cycles to occur over a smaller range of system SoC, this has a direct negative impact on the storage density and overall cost of the BESS. These deficiencies potentially impede Li-ion technology from being used

extensively in a large BESS. This work proposes the precise and continual SoC balancing of many thousands of cells individually (i.e. not in packs) using a tightly integrated power electronic circuit coupled with a new control system design. The proposed technique seeks to maximise the accessible SoC range of each individual cell, thereby enhancing the overall capacity of the system [34].

1.2 Research Objectives

The objectives of the research presented in this thesis were:

- To develop a circuit and control topology for a grid-scale BESS
- To investigate the close integration of a cascaded H-bridge multi-level converter and a large number of cells interfacing with an AC electrical grid
- To develop a balancing control for a grid-scale BESS using a hierarchical structure that can be used to scale the system to the very large number of cells required for a practical grid-scale BESS
- To develop a balancing control that maximises the accessible SoC range of each individual cell by ensuring that weak cells do not limit the capacity of the BESS

1.3 Contributions of the Thesis

1.3.1 Chapter 2 – Literature Review

A literature review was undertaken, covering the following areas:

- Grid-scale ESSs: pumped hydro, compressed air and battery
- Grid-scale BESSs: Lead-acid, Li-ion, Nickel-based

- Remarks on the battery system and power conversion system (PCS) of selected grid-scale BESSs
- Balancing control in BESSs
- Balancing algorithms in BESSs
- SoC estimation
- Challenges in using BESSs – managing cell failure

1.3.2 Chapter 3 – Proposed Structure for a Grid-scale BESS

A literature review was undertaken, covering the following areas:

- Medium-voltage PCSs
- Two-level and multi-level voltage source converters
- PCSs in grid-scale BESSs
- Limitation of existing grid-connected BESSs
- The use of PCSs for cell balancing in grid-scale BESSs

1.3.3 Chapter 4 – Balancing Control using a Hierarchical Structure

The main contributions of Chapter 4 are as follows:

- Integration of a cascaded H-bridge multi-level converter and a large number of cells for direct DC-AC conversion, providing the scope for selectively charging and discharging some cells over the others
- Cell organisation in a hierarchical arrangement: modules, sub-banks, banks and phases

- Development of five levels of SoC balancing control in a grid-scale BESS: balancing of cells within a module, balancing of modules within a sub-bank, sub-banks within a bank, banks in a phase and balancing between phases
- Showed that a constant of proportionality, β can be used to set the strength of charge balancing
- Zero-sequence voltage injection for SoC balancing control between phases
- Active and reactive power control in the proposed BESS using direct-quadrature (dq) control
- Modeling of Li-ion cell using MATLAB Simulink
- Development of an integrated approach including vectorisation and variable simulation time steps for simulation of a large number of cells
- Validation of balancing control in a 380 kWh BESS using 2835 Li-ion cells in MATLAB Simulink

1.3.4 Chapter 5 – Managing Voltage Constraints using Peak Sharing

The main contributions of Chapter 5 are as follows:

- Development of peak sharing algorithm for alternative modules to assume a portion of the load when certain modules are not capable of meeting the demand
- Demonstration of peak sharing in managing voltage constraints for a 380 kWh BESS in MATLAB Simulink

1.3.5 Chapter 6 – Experimental System

The main contributions of Chapter 6 are as follows:

- Development of the SoC balancing control using Altera Quartus II system, Terasic Cyclone IV E on Altera DE0-Nano development board and MATLAB
- Experimental SoC estimation based on Coulomb counting
- Bi-directional power flow control with the integration of charging and discharging capabilities into the system
- Showed that maximum cell capacity can be obtained through a series of experiments
- Showed that pre-defined SoC can be set for individual cells through a series of experiments
- Validation of SoC balancing control using two modules consisting of 24 NiMH cells for two levels of balancing: balancing of cells within a module and balancing of modules
- Demonstration of the acceleration of module SoC convergence rate using higher β value
- Showed that all cells' open circuit voltage (OCV) stay close within acceptable margin upon termination of the SoC balancing control
- Demonstration of the effectiveness of peak sharing in managing voltage constraints when a high β value is used for the SoC balancing control

1.3.6 Research Questions and Outcomes – Summary

The three main identified research in the thesis with the related outcomes, are shown in Table 1.1.

Table 1.1 Thesis research questions and outcomes

Research question:	Outcomes:
What is the circuit topology for a grid-scale BESS?	A 380 kWh grid-scale BESS was developed based on the close integration of a cascaded H-bridge multi-level converter and Li-ion cells interfacing with an AC electrical grid. A down-scaled experimental BESS was designed, constructed and tested to validate the simulation work.
What is the control strategy for a grid-scale BESS?	Cells are organised in a hierarchical structure consisting of modules, sub-banks, banks and phases. The control strategy includes five levels of balancing: balancing of cells within a module, balancing of modules within a sub-bank, sub-banks within a bank, banks in a phase and balancing between phases.
How does the control strategy improve capacity utilisation and system reliability?	The SoC balancing control was developed to maximise the accessible SoC range of each individual cell by ensuring that weak cells do not limit the capacity of the system. Peak sharing was implemented to manage voltage constraints to avoid severely limiting the system performance.

1.4 Publications by the Author

1.4.1 Journal Publication

C. A. Ooi, D. Rogers, N. Jenkins, “Balancing control for grid-scale battery energy storage system”, *Proceedings of the ICE – Energy*, vol. 168, no. 2, pp. 145–157, 2015.

1.4.2 Research Conferences and Meetings

C. A. Ooi, D. Rogers, N. Jenkins, “Balancing control for grid-scale battery energy storage systems”, UK Energy Storage Conference 2014, 25-27 November 2014, The University of Warwick.

C. A. Ooi, D. Rogers, N. Jenkins, “State-of-charge balancing control for grid-scale energy storage systems using cascaded H-bridge multilevel inverter”, 5th HVDC Colloquium, 9-11 July 2014, Imperial College London.

CHAPTER 2 LITERATURE REVIEW

This chapter provides a comprehensive review of grid-scale energy storage systems (ESSs) including pumped hydro, compressed air and battery energy storage systems (BESSs), with particular attention paid to BESSs and their associated balancing control. This chapter also gives an overview of state-of-charge (SoC) estimation methods commonly used in BESSs.

2.1 Grid-scale ESSs

Energy demand varies widely, on both a daily and seasonal basis [35]; it is a great challenge for energy suppliers to meet the demand of loads that have high peak-to-base demand ratios [36]. A mismatch of demand to electrical supply means that power is not always available when it is required and on other occasions, there is excess power [37]. Energy suppliers must have sufficient installed capacity to meet peak demand [38-39].

There are a number of ways to mitigate intermittency of generation and the mismatch between generation and demand such as adding flexible generation to the system (e.g. open cycle gas turbines [40]), controlling loads on the system (demand-side response) [41] or through the use of ESSs, which can absorb or release energy to buffer the mismatch between generation and load over periods of minutes to hours. The high penetration of wind and solar into the energy market over the past decades has driven interest in ESSs to facilitate the large-scale deployment of intermittent, carbon-free energy resources [42-44]. When properly designed and integrated, ESSs can be used to compensate for the intermittent nature of renewable energy resources by partially decoupling energy generation from demand that exhibit temporal mismatches [7], smooth out this variability and allow

unused electricity to be dispatched at a later time thus improving system stability, reliability and power quality [45-47]. For instance, when there is a mismatch between the availability of wind or solar and demand, ESSs can facilitate time-shifting of loads [48]. It can also be used in offsetting voltage rise (or fall) caused by sudden large rises (or drops) in power availability due to the intermittency [49-50].

De-coupling of generation from demand is feasible with grid-scale ESSs, it decreases the necessity of constant monitoring and prediction of peak demands [51]. In Figure 2.1, ESSs can be used to stabilise the intermittency from wind and solar by smoothing out their output variability in order to meet electricity demand pattern. ESSs are charged when electricity is abundant, and discharged into the grid when electricity is more valuable. Energy suppliers need to build only adequate generating capacity to meet average demands rather than peak demands, thus avoiding the building of additional thermal power plant operating only during the peak hours [52-54]. Fewer and cheaper electricity transmission and distribution network upgrades are required [55-56].

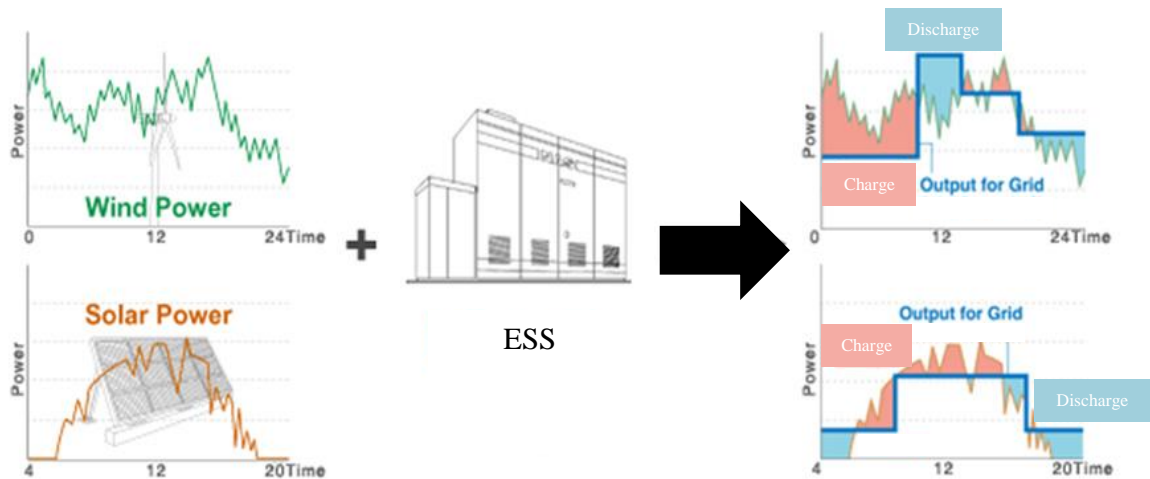


Figure 2.1 Wind and solar energy intermittency stabilisation by ESS (adapted from [57])

A wide variety of storage technologies exists, each has its own distinct characteristics that makes it ideal for certain grid services but less so for others. They are widely different in terms of round-trip efficiency, lifetime, costs, maturity, scalability, energy/power density, response time, reliability, site specificity, environmental impact, recyclability etc. Table 2.1 summarises the features of major storage technologies; a comprehensive discussion can be found in literature [49] [58-72]. The following section outlines a detailed description and discussion of major storage technologies.

2.1.1 Pumped Hydro ESSs

A pumped hydro ESS typically consists of two reservoirs located at different elevations; it employs off-peak or surplus electricity to pump water from a lower elevation reservoir up to another reservoir at a higher elevation where it is stored as gravitational potential energy. During periods of high demand, the stored water is released from the upper reservoir through a hydroelectric turbine into the lower reservoir to produce high-value electricity for peak hours. During periods of low demand, the water is pumped back up to re-charge the upper reservoir and to allow the cycle to be repeated [58].

Pumped hydro ESS is a mature energy storage technology storing large amount of energy for relatively long periods and it is the most widely implemented grid-scale EES. With about 300 systems operating worldwide [73] and an installed capacity of 135–140 GW at present [74], it accounts for 99 % of worldwide bulk storage capacity and contributes to about 3% of global generation [75]. Various pumped hydro storage plants exist with typical ratings around 1000 MW and individual plant range up to 3000 MW [76].

Table 2.1 ESSs comparison [49] [58-72]

	Pumped Hydro	Compressed Air	Secondary Batteries	Super-conducting magnetic	Flywheel	Super-capacitor
Maturity	Mature	Deployed	Mature	Under construction	Under construction	Deployed
Round-trip efficiency (%)	70-85	50-75	65-90	~95	~90	~90
Response time	Seconds-minutes	Minutes	Seconds	Milliseconds	Milliseconds	Seconds
Energy range	0.5–10 GWh	50–5000 MWh	0.5–50 MWh	0.5–1500 MWh	1–5 MJ	1-10 MJ
Power range	0.5-3 GW	3-400 MW	0.5-80 MW	10-1000 MW	0.1-3 MW	0.1-5 MW
Cycle life (cycles)	> 50000	> 10000	2000	> 50000	> 100000	50000
Lifespan (years)	25+	20+	3-15	5-20	20	5-20
Charge duration	Hours	Hours	Minutes-hours	< Seconds	15 minutes	Seconds
Discharge duration	Hours	Hours	Minutes-hours	Hours	Seconds-minutes	Seconds
Modularity	No	No	Yes	Possible	Yes	Yes
Siting ease	Poor	Poor	Good	Poor	Good	Good
Environmental impact	Large	Large	Moderate	Moderate	Low	Moderate
Advantages	Rapid response time, large capacity	Rapid response time	High efficiency, high energy density, fast dynamic response	High efficiency	Rapid response time, high cycles	Rapid response time, high power density
Disadvantages	Geographically constrained	Low efficiency, geographically constrained	High cost, limited cycle life, safety issues	High cost , low energy density, cooling system required	High cost , tensile strength limitations	High cost, low energy density
Primary applications	Energy management / backup / regulation service	Energy management / backup / renewable integration	Power quality / frequency regulation	Power quality / frequency regulation	Load leveling / frequency regulation / peak shaving / transient stability	Power quality / frequency regulation

Taking into account the conversion loss and evaporation loss from the exposed water surface, the round-trip efficiency is about 70–80 % [77]. Despite the fact that pumped hydro ESS is the largest-capacity form of available grid ESSs with low operation and maintenance cost [78], the major shortcoming of pumped hydro ESS lies in the scarcity of suitable terrains with significant elevation difference between two large reservoirs. With the restriction of site selection, the deployment of pumped hydro plant requires a long lead time (typically around 10 years) and a high capital investment, which can only be recouped over decades [79].

Pumped hydro ESS is mainly used in energy management, it is often able to store hundreds to thousands of MW per installation and it can respond to load changes within seconds, thus permitting the time-shifting of energy where baseload power plants such as nuclear and coal-fired plants continue to operate at peak efficiency, while reducing the need for peaking power plants that use costly fuels [80]. Pumped hydro ESSs have also been used in frequency control, load leveling, peak shaving, spinning reserve and supply reserve [72].

Due to an increasing push to reduce the environmental impacts, recent suggestion is underground pumped hydro ESS where flooded mine shafts, underground caves, oceans, quarries, ground water systems or other caverns composed of competent rock formations are used as reservoirs [70] [81].

Examples of deployed pumped hydro ESS installed worldwide includes Bath County, US (3003 MW) [82-83], Huizhou, China (2448 MW) [84], Okutataragi, Japan (1932 MW) [85-86], and Dinorwig, UK (1728 MW) [87]. The recently announced North Sea Link allows up to 1400 MW of power flowing from UK to Norway when wind power

generation is high and electricity demand is low in the UK, in order to conserve water in Norway's reservoirs. It can help to ensure secure electricity supplies by allowing power to flow from Norway when demand is high in the UK and there is low wind generation [88].

2.1.2 Compressed Air ESS

A compressed air ESS decouples the compression and expansion cycles in a conventional gas turbine technology into two separated processes [89]. During low demand, energy is stored by compressing air into an underground reservoir or an air-tight vessel/piping system, typically 4.0–8.0 MPa [90]. Cheaper off-peak baseload electricity is used to compress the air. When energy is required to be injected into the grid, the stored compressed air is released and heated by a heat source from the combustion of fossil fuel (conventional diabatic system) [91-92] or the heat recovered from the compression process in newer systems (adiabatic system) [93-95]. The compressed air energy is captured by a turbine that is connected to a generator to produce electricity. In an adiabatic system, the waste heat from the exhaust is captured and recycled via a recuperator which is operated to re-use the exhaust heat energy. The cycle efficiency is improved from 42 % to 54 % in [96-97] where it reduces the fuel consumption by 22–25 %. A variety of storage vessels can be used such as salt caverns, hard rock caverns, depleted natural gas fields, naturally occurring aquifers, porous rock formations, abandoned mines, underwater bladders, and above-ground tanks [98].

Compressed air ESS is another commercially available technology capable of providing very large power output (over 100 MW within a single unit) besides pumped hydro ESS [99]. It is a relatively mature technology with round-trip efficiency of 85 %

accounting for both thermal and electrical input energies [100]. A typical compressed air ESS has a rated power of 50-400 MW. A compressed air ESS can provide fast start-up of about 9 minutes for an emergency and 12 minutes in normal condition, while a conventional combustion turbine peaking power plant typically requires 20–30 minutes [55]. The use of compressed air ESS includes peak shaving, frequency and voltage control, and load shifting. It has also been used as spinning reserve to smooth the power output of integrated wind energy [101-102].

There are currently five compressed air ESSs in operation, with a few others are pilot plants or in planning stage [103]. The first plant using an underground compressed air reservoir was constructed in Huntorf, Germany since 1978 [104]. It has shown excellent performance with 90 % availability and 99 % starting reliability [105]. Over three decades of successful operation, it achieved a capacity of 290 MW initially, which was increased to 321 MW in 2006 [97]. The compressed air plant located in McIntosh, Alabama, US, has been in operation to deliver 110 MW since 1991 [106]. Both plants have demonstrated the technical feasibility and viability for load management [107].

Many power plants have been proposed; however, some of them encountered siting problems and were abandoned. For example, after 8 years of planning, the 2700 MW Iowa Stored Energy Park project in Norton, Ohio was terminated as the planned geological formation is unable to deliver the desired capacity [108-109].

2.1.3 Battery Energy Storage Systems (BESSs)

Following the successful demonstration of several BESSs such as 17 MW / 14 MWh BEWAG AG in Berlin for frequency regulation, 20 MW / 14 MWh PREPA in

Puerto Rico for spinning reserve, frequency control and voltage regulation, and 10 MW / 40 MWh Southern California Edison in Chino, California for load leveling, rapid spinning reserve and instantaneous frequency control, BESSs have emerged as one of the most promising technologies for grid-scale ESSs, offering a wide range of grid applications, with these systems now providing more than 10 years of operational experience [110].

As illustrated in Figure 2.2, each electrochemical cell¹ consists of two electrodes; a positive electrode (anode) and a negative electrode (cathode) together with a solid, paste, or

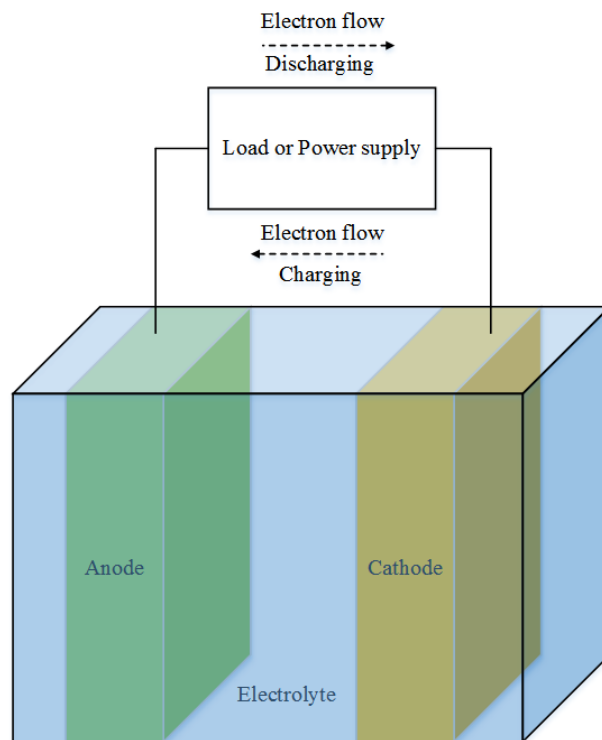


Figure 2.2 Simplified diagram of a cell

¹ The basic “building block” of a battery that converts chemical energy into electrical energy and vice versa. It consists of two electrodes (an anode and a cathode), electrolyte, a separator between the anode and cathode, and some type of cell container [427-434]. See Nomenclature for details.

liquid electrolyte. A cell is charged when it undergoes an internal chemical reaction under a potential applied to both electrodes; i.e. by oxidation of the anode to generate electrons, and reduction of the cathode to consume electrons flowing through an external circuit. The reaction is reversible, allowing a cell to deliver the absorbed energy, or discharge through an external load [111].

A simplified illustration of BESS architecture is represented in Figure 2.3. A typical BESS consists of a battery pack, power conversion system (PCS), monitoring and control unit, protective circuitry, AC transformer, and grid connection [112]. A number of individual cells are configured in various series and/or parallel arrays and are assembled into a battery module to obtain the desired voltage and current levels. Multiple modules are connected in series and/or parallel to form a battery pack. A cell converts electrical energy into chemical energy for storage and it is charged and discharged using DC current. Thus, a self-commutating PCS is required to interface the DC system to the AC grid via a transformer. A PCS provides bi-directional current flow and voltage polarity of power conversion between the AC and DC systems with fast response. It regulates the flow of real and reactive power between the grid and the battery pack, which can be delivered or absorbed independently according to the needs of the system, up to the rated apparent power of the PCS [113]. The PCS is a four-quadrant DC-AC converter connecting the DC system to the grid via a transformer.

The monitoring and control unit provides interface to coordinate the operation of a BESS, which manages the system based on measurements internal (i.e. SoC) and external (i.e. bus-bar voltage) to the system. It includes a battery management system (BMS), which

monitors and controls the status and health of cells, with several aims such as to protect the cells from damage, and to ensure optimum use of cells etc. [114].

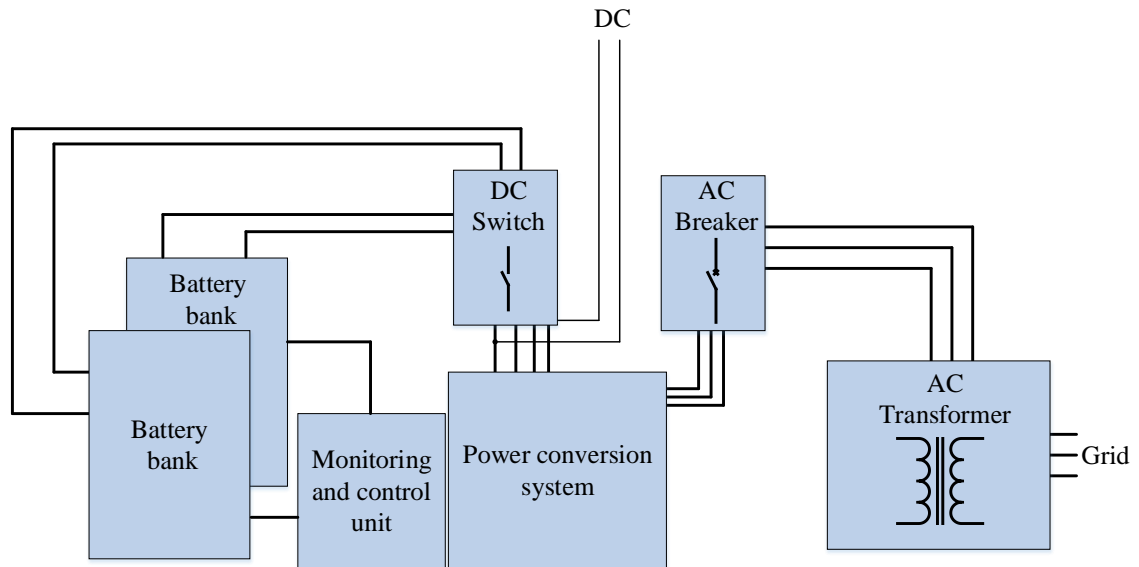


Figure 2.3 Simplified configuration of a BESS (adapted from [112])

BESSs can deliver fast and flexible dynamic response, high efficiency and wide range of energy storage capacity. BESSs are able to respond to grid demands or load changes nearly instantaneously and also have the capacity to function over longer durations [115-116]. BESSs are typically modular, so they can be easily scaled to the size determined by the energy needs for a particular application. The installation of a BESS takes a relatively short time frame (often within 12 months) compared to 10 years for a pumped hydro ESS [117]. In general, grid-scale BESSs can reach round-trip efficiencies of 70–80 % with very low standby losses and they have lifetime of about 3–15 years (depending on the operating conditions and cell technology) [118].

Due to the electrochemical nature of the conversion, there are several key challenges which greatly affect a cell's operation. Studies [119-120] have reported that cell

degradation mechanisms of irreversible capacity loss are accelerated by elevated temperature, where the temperature accelerates the degradation of the cathode and formation of solid-electrolyte interface (SEI) on the anode. SEI formation on the anode is the main contributor to the increased internal resistance of a cell, which is non-reversible and cannot be improved with cycling. Both capacity loss and increased internal resistance are major factors of cell degradation which significantly affects a cell's lifespan [121-122].

Another major concern is cell's cycle life, which is defined as the number of charge/discharge cycles that a cell can provide depending on the depth-of-discharge (DOD) (fraction of stored energy that can be withdrawn) [123]. A lithium-ion (Li-ion) cell is expected to reach end-of-life (80 % capacity remaining) after 350 cycles at 100 % DOD, 1000 cycles at 50 %, and 1700 cycles at 25 % [124]. Shallow DOD cycling improves the total Ampere-hour throughput in the lifetime of a cell [125]. For example, cell A must be limited to 30 % DOD to get a comparable cycle life to cell B that is at 75 % DOD. This means that cell A must be 2.5 times larger in capacity than cell B in order to get a comparable cycle life [126]. At present, although high cost has been the main barrier to the BESS's deployment in grid-scale facilities [127], owing to the vastly increased penetration of electric vehicles, industries have been significantly investing in improving the battery cost competitiveness, and it is expected that the battery price will drop dramatically by 2020 either in a linear or accelerating fashion [128].

Grid support using several types of battery technologies has been studied extensively and the connection of a BESS to the grid has been shown to improve the dynamic behaviours of the power grid [36]. BESSs offer a wide range of grid applications and several BESSs have been installed and deployed for the purposes such as load leveling,

spinning reserve, black start capability, power system management, peak shaving, wind and solar energy smoothing, grid stabilisation, diminished congestion, frequency and voltage regulation, electric vehicle charging stations, power factor correction, and others [129-130].

Several battery technologies have been around for a long time in conventional BESSs and are considered mature such as lead acid, nickel-cadmium (NiCd), nickel-metal hybrid (NiMH), Li-ion and sodium-sulphur (NaS). There are emerging battery technologies such as redox flow with potential low cost and sodium nickel chloride with wider operating temperature range, which have been used in recent pilot projects and laboratory tests [131]. Table 2.2 compares various battery technologies used in grid-scale BESSs on several key factors such as energy density, cycle efficiency, lifespan, self-discharge, advantages as well as limitations.

Table 2.2 Battery technologies comparison [132-138]

	Lead-acid	NiCd	NiMH	Li-ion	NaS	Vanadium redox flow	Zinc-bromine
Nominal cell voltage (V)	2.0	1.2	1.25	3.7	2.0	1.15-1.55	1.8
Cycle efficiency (%)	70–80	60–70	50–80	75–90	75–90	65–75	65–75
Energy density (Wh / kg)	10–50	30–60	60-90	70–160	60–130	10–20	10–30
Power density (W / kg)	50–100	40–80	70-200	130–300	10–90	< 20	< 25
Daily self-discharge (%)	0.1–0.3	0.2–0.6	0.6-1.6	0.1–0.3	~0	Small	Small
Cycle life (cycles)	500–1000	2000–2500	500-2000	1000–10000	2500	>12000	>2000
Lifespan (years)	5–15	10–20	5	5–15	10–15	5–10	5–10
Storage duration	Minutes–hours	Minutes–hours	Minutes–hours	Minutes–hours	Minutes–hours	Hours	Hours
Operating temperature (°C)	-10 to 40	-40 to 50	-30 to 50	-30 to 60	300 to 350	0 to 40	20 to 50
Maturity	Mature	Deployed	Deployed	Deployed	Deployed	Deployed	Deployed
Advantages	Low cost, high discharge rate, reliable	Low maintenance , reliable, good charge retention	High energy density	High energy density, relatively low self-discharge, low maintenance	High efficiency, high energy density, inexpensive materials, high cycle life	Low maintenance , high efficiency, high cycle life	High cycle life, high efficiency
Limitations	Low energy density, low cycle life, contains lead	Low energy density, contains cadmium	Limited cycle life, limited discharge current	Expensive, protection circuit required	Thermal control unit and adequate insulation required	Low energy density, expensive	High self-discharge rate, thermal control unit required

2.2 Grid-scale Lead-acid BESSs

Lead-acid battery technology is the oldest and most mature of all battery technologies that have been used for electrical energy storage, with over 20 years of industry usage, thus, it has seen the most widespread use among grid-scale BESSs [139].

The use of Lead-acid battery technology has been studied since the early 1900s, with the

first grid-scale system (BEWAG AG, Berlin, Germany) installed at the end of the 1970s under a test program in order to collect the necessary operational and technical data. It was successfully put into operation in July 1981 and has demonstrated its longevity and reliability [140].

Since then, Lead-acid battery technology have been used in several grid-scale BESSs such as 20 MW/ 14 MWh PREPA (San Juan, Puerto Rico) [141], 1 MW / 4 MWh Kansai Power Co. (Tatsumi, Japan), 4 MW / 7 MWh Vaal Reefs Exploration and Mining Co. (South Africa), and 10 MW/ 40 MWh SCE Chino (California, US) [142]. Table 2.3 presents the details of location, date of installation, rated capacity, and primary applications for most of the installed grid-scale Lead-acid BESSs since 1980.

Lead-acid BESSs utilising either flooded or valve-regulated cells have ranged from 200 kW with two hours of storage to 20 MW with one and half hour storage to provide grid services including frequency control, spinning reserve, peak shaving, and load levelling [143]. The essential features of Lead-acid BESSs are summarised in Table 2.3. Key manufacturers are Hagen Batterie AG, Exide Technologies (formerly known as GNB Industrial Battery), and Japan Storage Battery Company (GS) (now GS Yuasa).

Table 2.3 Grid-scale Lead-acid BESSs [43] [72] [99] [140] [144-153]

BESS	Manufacturer (battery, PCS)	Primary applications & capacity	Cell size & configuration	Descriptions
Berliner Kraft- und Licht (BEWAG) AG Berlin, Germany 1987-1995	Hagen OCSM cells (battery) AEG Power Solutions (PCS)	Frequency control Spinning reserve 17 MW / 14 MWh	1000 Ah @ C/5 7080 cells in 12 parallel strings with 590 cells each 1416 modules of 5 cells each housed in a container	Batteries are connected to a 30 kV distribution network via 4 parallel-connected converters. Power flow is limited to 8.5 MW when providing frequency control and increased to 17 MW when providing spinning reserve.
Kansai Power Co. Tatsumi, Japan 1986	Japan Storage Battery Company (battery)	Load leveling 1 MW / 4 MWh	7500 Ah 526 tubular-positive cells in a single series string	It is a 2-year trial program that precedes the introduction of other battery technologies (Sodium-sulphur and Zinc-bromine).
Hagen Batterie AG Soest, Germany 1986	Hagen OCSM cells (battery)	Load leveling 0.5 MW / 7 MWh	9000 Ah 2 parallel strings, each with 200 cells	This 400 V BESS is connected to a 380 V bus via 2 parallel-connected converters rated at 250 kW each.
Crescent Electric Membership Cooperative (EMC) (now Energy United) Statesville, NC, US 1987–2002	GNB Industrial Battery, flooded cell (now Exide Battery) (battery)	Peak shaving 0.5 MW / 0.5 MWh	2080 Ah @ C/5 324 cells with 6 cells per module	The 12-pulse, line-commutated converter is rated at 500 kW connected to a 480 V three-phase system.
Southern California Edison (SCE) Chino, CA, US 1988-1997	Exide Batteries GL-35, flooded cell (battery) EPRI & General Electric (PCS)	Demonstrations: Load leveling Transmission line stability Black start VAR control 10 MW / 40 MWh	2600 Ah @ C/4 1376 modules or 8256 cells housed in 2 battery rooms	The PCS converts a 12 kV/60 Hz AC from the grid to 2000 V DC required for battery charging and vice versa for discharging.
Vaal Reefs Exploration and Mining Co. South Africa 1989	Hagen OCSM cells (battery)	Peak shaving Emergency power supply backup to a diesel generator 4 MW / 7 MWh	4 string halves, each with 640 cells arranged in 128 groups of the 5-cell modules	The system operates between a maximum end-of-charge voltage of 3000 V, and a maximum end-of-discharge voltage of 2100 V.

Johnson Controls, WI, US 1989	Johnson Controls, GC6-1500B gel, valve-regulated cells (battery)	Peak shaving Load leveling 0.3 MW / 0.6 MWh	2700 Ah 15 blocks connected in parallel to give 6 V / 2700 Ah, each block consists of 6 V/ 180 Ah 64 modules to provide 384 V	The PCS is of a dual- bridge 6-pulse line- commutated design. The BESS has a nominal 384 V connected to a 480 V three-phase input.
Puerto Rico Electric Power Authority (PREPA) San Juan, Puerto Rico 1994 – 1999	Lorica 29TH95 tubular flooded cell (battery) General Electric (PCS)	Spinning reserve Frequency control Voltage regulation 20 MW / 14 MWh	2088 Ah @ C/3 6048 cells in 6 parallel strings of 1000 cells each	The PCS consists of 2 parallel-connected converters, rated at 10 MVA each. It has 3, 6- pulse gate-turn-off (GTO) bridges (18- pulses) and a capacitor bank as harmonic filter.
GNB Technologies Vernon, CA, US 1996	GNB Industrial Battery, Absolyte IIP, type 100A33, valve- regulated cells. (now Exide Battery) (battery) General Electric (PCS)	Peak shaving Spinning reserve 3.5 MW / 3.5 MWh	5000 Ah 2 parallel strings with 378 modules per string; 3 cells in parallel per module to give a total of 2268, 2 V cells	The PCS consists of 2, 6-pulse converters (12- pulses), and 3 are connected in parallel to achieve the desired power rating.
Metlakatla Power & Light (MP & L) Metlakatla, AK, US 1997-present	GNB Industrial Battery, valve- regulated 378 Absolyte IIP (now Exide Battery) (battery) General Electric (PCS)	Voltage regulation Displacing diesel generation 1.3 MW / 1.3 MWh	3600 Ah @ C/8 1134 cells in total; A single module consists of 3, 2 V cells connected in parallel	The PCS uses GTO thyristor technology. It is rated at 1 MW continuous power and 1.6 MVA peak.
PQ2000 Brockway Standard Lithography Plant Homerville, Georgia, US 1996-2001	Delco, model 1150 (battery)	Power quality Uninterruptible power supply 2 MW / 0.055 MWh	384, 12 V cells are configured in 8, 250 kW battery modules in a PQ2000 module	PQ2000 is a modular BESS consisting of PQ2000 modules, transformer and static switch.

2.3 Grid-scale Li-ion BESSs

Li-ion technology stands as the most promising option for energy storage, and has a near-monopoly in the consumer electronic device market due to its very high energy density, resulting in the production of the order of billions of units per year. It is also seen as the power sources of choice for electric vehicles (again because of high energy density), which accelerates the worldwide market for Li-ion [154]. Several manufacturers have sought to expand their markets beyond consumer electronics, and after applying the technology to electric vehicles, are now beginning to do the same for the electric grid market, recent advances in this technology have translated into several Li-ion BESSs in the 10 MW or greater size range such as 32 MW / 8 MWh Laurel Mountain (Elkins, US) [155], 6 MW / 10 MWh Smarter Network Storage (Leighton Buzzard, Bedfordshire, UK) [156], 6 MW / 36 MWh Zhangbei (Hebei, China) [157], 20 MW / 6.6 MWh AES Angamos (Mejillones, Chile) [158] and 8 MW / 32 MWh Southern California Edison Tehachapi (Tehachapi, US) [159-160]. Table 2.4 presents the details of location, date of installation, rated capacity, and primary applications for the installed grid-scale Li-ion BESSs.

The concept of Li-ion technology was first introduced in the 1970's, however, early attempts were thwarted by the poor cycling characteristics and safety issues associated with metallic lithium. It required nearly 20 years of research and development before being to see a widespread adoption and mass production by Sony in 1991 [161].

The much greater energy density is one of the chief advantages of a Li-ion cell, which is typically twice that of the standard NiCd cell and the energy density is increasing rapidly. Li-ion cells do not suffer from the high self-discharge rate of NiCd and NiMH cells

Table 2.4 Grid-scale Li-ion BESSs [156] [162-165]

BESS	Manufacturer (battery, PCS)	Primary applications & capacity	Cell size & configuration	Descriptions
Laurel Mountain Elkins, WV, US 2011	A123 (battery) SSD Parker (PCS)	Frequency control Ramp rate control Peak shaving 32 MW / 8 MWh	A123 patented Nanophosphate Lithium Iron Phosphate	The BESS is integrated with the 98 MW wind farm. The embedded BMS is used for cell balancing, SoC estimation, voltage and temperature measurements.
Smarter Network Storage , Leighton Buzzard, Bedfordshire, UK 2014	Samsung SDI (battery) S&C Electric (PCS)	Peak shaving, Frequency control 6 MW / 10 MWh	Lithium Manganese Oxide 192 cells are connected in series to make strings 264 trays in racks with 22 racks connected to each 500 kW of storage management system	This single-module, multi-stage system employs a boost DC-DC converter in the PCS to reduce the number of series-connected cells required in the battery packs.
Reese Technology Center Lubbock, TX, US 2013	Samsung SDI (battery) Yunicos (PCS)	Ramp support Demand response Frequency control 1 MW / 1 MWh	Lithium Manganese Oxide 1200 Ah cells stacked in series and parallel with voltage of 1055 V	The project marks the coupling between Samsung SDI's Lithium Manganese Oxide cells with Xtreme Power's Xtreme Active Control Technology™ to provide optimal energy storage control.
Orkney storage park project Kirkwall, Orkney, UK 2013	Mitsubishi Heavy Industries (battery) SSE Generation (PCS)	Emergency power supply backup Renewable energy integration 2 MW / 0.5 MWh	2000 Li-ion cells	A scheme called Active Network Management is designed to manage grid constraints, which aims to increase the capacity of renewable and distributed generation that can connect to the network.

State Grid Corporation of China / Zhangbei National Wind and Solar Energy Storage and Transmission Project Hebei, China 2011	BYD (battery) ABB (PCS)	Frequency control Voltage regulation Renewable energy integration 6 MW / 36 MWh	Lithium Iron Phosphate cells	10 units of the ABB PCS100 ESS equipment are used to monitor the real-time voltage and control the power in order for the battery to release power smoothly by adjusting frequency and voltage.
Southern California Edison / Tehachapi Wind Energy Storage Project Tehachapi, CA, US 2014	LG Chem (battery) ABB (PCS)	Frequency control Ramp management Black start 8 MW / 32 MWh	Li-ion 604 battery racks, 10872 battery modules and 608832 cells	The PCS consists of two converters each rated at 4 MW / 4.5 MVA, designed for connection to 12.47 kV. Each unit is configured to connect to two 2 MW battery strings with a charge-discharge DC voltage range of 750-1050 V.
AES / Angamos Mejillones, Chile 2012	A123 (battery) ABB (PCS)	Frequency control Spinning reserve 20 MW / 6.6 MWh	Li-ion	The BESS continuously monitors the condition of the power system and provides power instantaneously (up to 15 minutes) if there is any significant frequency deviation due to the loss of a generator.
AES / Los Andes Atacama, Chile 2009	A123 (battery) SSD Parker (PCS)	Frequency control Spinning reserve 12 MW / 4 MWh	Li-ion	The BESS operates in either autonomous or dispatch mode. When there is significant frequency deviation, it provides immediate response (up to 20 minutes) to help maintain the grid until the fault is cleared.
Sempra / Auwahi Wind Farm Kula, HI, US 2012	A123 (battery) Dynapower (PCS)	Ramp rate control Voltage regulation 11 MW / 4.4 MWh	Li-ion	The BESS helps to regulate power to Maui Electric Company's grid during variable wind conditions. The BESS also includes BMS for monitoring and safety control to ensure reliable operation.

, the self-discharge is less than half that of NiCd cells. Li-ion cell requires low maintenance, an advantage that most other battery technologies like Lead-acid cannot claim. It does not require periodic cycling to prolong lifespan [70]. Li-ion does not contain toxic heavy metals such as mercury or cadmium as in Lead-acid and NiCd. Other advantages of Li-ion technology include high-energy efficiency, lightweight, high charge and discharge rate capabilities, and a relatively long cycle life [166-167]. Several key features of Li-ion technology can be seen in Table 2.2.

The main hurdle in implementing grid-scale Li-ion BESSs is the high cost (GBP 350/kWh) [168-169]. Li-ion is expensive to manufacture and it is around 50 % more costly than per unit energy of NiMH [170-172]. Another challenge is it requires a protection circuit or BMS built into each pack to maintain safe operation by monitoring the cell voltage, current and temperature during charge and discharge [173]. Due to its closely defined operational limits, the safe operation of the cell requires detailed consideration, the maximum charge and discharge current is typically limited to between 1 C and 2 C to prevent internal heating.

With over a million electric vehicles on the road globally in September 2015, and an increasing number of grid-scale Li-ion BESSs worldwide, battery manufacturers such as SAFT and Mitsubishi are working towards reducing the manufacturing cost of Li-ion cells [174]. In fact, research [175] has found that there was a cost reduction of 14 % per year since 2007 and another research [176] has seen a cost reduction of 6-9 % for every doubling of production volume. Continued cost reduction, safety issues, material availability, and its scalability to large BESSs are the current research focuses on Li-ion technology [177].

2.4 Grid-scale Nickel-based BESSs

The world's largest NiCd BESS has been in operation since September 2003 in Fairbanks, Alaska (US) developed by Golden Valley Electrical Association (GVEA) to provide spinning reserves in an island grid. It can provide 27 MW of power for 15 minutes. In 2015, this BESS responded to 752 events, preventing a total of 320446 member outages [178]. NiCd cells were manufactured since the turn of the century and were widely used in emergency lighting, airline industry, medical equipment, and portable power tool [179]. In addition, NiCd cells are used as sub-station batteries and bulk storage as they offers relatively higher energy density, less maintenance and longer cycle life than Lead-acid cells [180-181].

By the mid-1990s, NiMH has gained importance over NiCd in many portable applications, due to the improved performance such as 25-40 % higher energy density, longer cycle life, less memory effect, good abuse tolerance, and free of environmentally unfriendly cadmium [182-183]. It has emerged as battery of choice for electric vehicles since 1990's [184] and also a feasible alternative to the failed reusable alkaline cells before losing to market share to Li-ion as NiMH suffers from severe self-discharge, which increases greatly with elevated temperature, age and cycling [185-186]. Excluding losses due to PCS and thermal management, the DC-DC energy efficiencies on NiMH range from 65-85 %, while for NiCd batteries, the efficiency is about 60-70 % [187]. Table 2.5 presents the details of location, date of installation, rated capacity, and primary applications for the installed grid-scale Nickel-based BESSs.

Table 2.5 Grid-scale Nickel-based BESSs [188-190]

BESS	Manufacturer (battery, PCS)	Primary applications & capacity	Cell size & configuration	Descriptions
Golden Valley Electric Association Fairbanks, AK, US 2003	Saft (battery) ABB (PCS)	Spinning reserve 27 MW / 6.75 MWh	NiCd 4 parallel strings of 3440 pocket-plate cells, type SBH920, with 10 cells per module	The PCS is capable of operating in all four quadrants (full power circle) utilising ABB's integrated gate commutated thyristor (IGCT) technology.
EcoPower Bonaire BV / Bonaire Wind-Diesel Hybrid Bonaire, Netherlands 2010	Saft (battery) Enercon (PCS)	Frequency control Spinning reserve 3 MW / 0.25 MWh	NiCd Type SMRX connected for a 640 V battery with a nominal capacity of 1320 Ah	Owing to its rapid start-up capability, this BESS serves as back-up during periods of low wind speeds and it meets the peak demand during tropical storms in order to stabilise the system.
Okinawa Electric Power Company / Minami Daito Island Okinawa, Japan 2013	Kawasaki Heavy Industries (battery)	Frequency control 0.3 MW / 0.08 MWh	NiMH 2 banks of 30-K5 Gigacell cells connected to give 12 V / 177Ah, 48 modules to provide 576 V	This BESS is used to control the frequency fluctuation due to the installation of renewable energy facility on the remote island. It also serves as backup power supply (15 minutes start-up time) in case of power failure.

2.5 Remarks on Selected Existing Grid-scale BESSs

The BESSs listed in Tables 2.3-2.5 encompass a wide range of capacities and a multitude of applications. This reflects the maturity of BESS technology. Among all the BESSs, Chino BESS was commissioned for multi-purpose demonstrations with load leveling as the initial intention. It was subsequently tested and demonstrated for several others grid services such as peak shaving, spinning reserve, voltage and frequency control, and black-start operations. Chino BESS was reported to have the following efficiencies:

plant, 72 %, battery pack, 81 %, PCS, 97 % [191-192]. The 10 MW / 40 MWh Chino BESS is the largest Lead-acid BESS to date, consisting of one 12 kV AC switch rack, one common room for PCS and control, and two large parallel buildings to locate the battery pack. It supplies 40 MWh of energy or 10 MW of power in four hours, to meet energy demand of 5000 residents [193].

A full-scale 17 MW / 14 MWh BEWAG BESS was installed in 1986 following a successful 5-year trial on a 24 kW test facility. It was designed to provide spinning reserve and frequency control for the isolated island in Steglitz, West Berlin, Germany.

The 32MW / 8MWh Laurel Mountain BESS was deployed in October 2011 to manage the output fluctuations in the 98 MW wind farm via frequency control. It is the largest Li-ion BESS in the world, where its applications include frequency control, peak shaving, black start, power factor control and ramp rate control [153].

The 27 MW / 6.75 MWh GVEA BESS was motivated by the occasional problem with the power plants required rolling blackout in Fairbanks. The BESS was developed to provide power for a short duration (up to 15 minutes) to a population of around 90000 during outages (about 30 times a year) until back-up supply comes on-line. The BESS is designed to operate in seven modes: VAR support, spinning reserve, power system stabiliser, scheduled load increase, charging, automatic scheduling and automatic generation control [155]. The following sections discuss the battery pack and PCS in the four existing BESSs described above.

2.5.1 Battery Pack

The hierarchy and terminology of the battery pack used in most of the existing BESSs is illustrated in Figure 2.4. A module is defined as the smallest modular unit and it consists of a number of individual cells. A tray contains several modules and several trays form a string.

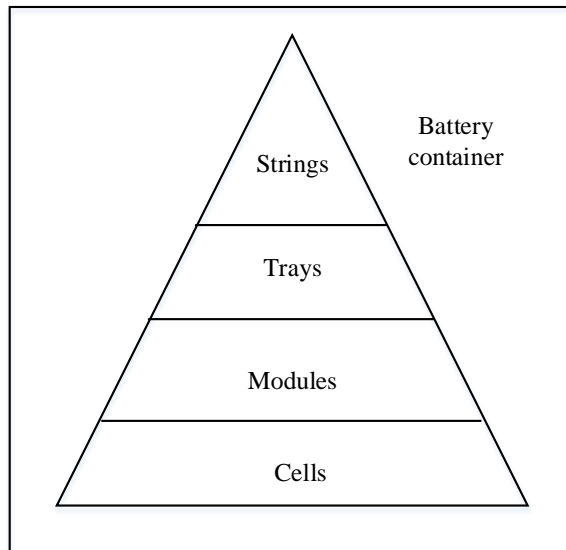


Figure 2.4 The hierarchy of the battery pack used in the existing BESSs

In the 10 MW / 40 MWh Chino BESS, the battery pack consists of 8256 individual Exide GL-35 flooded Lead-acid cells where, six cells are assembled to form a 12 V module, 44 modules form a tray, four trays form a string, five strings are connected in parallel to form 1376 modules [142] [194] as illustrated in Figure 2.5. The 17 MW / 14 MWh BEWAG BESS is composed of 7080 Hagen OCSM flooded Lead-acid cells configured in twelve parallel strings with 590 cells in each string as can be seen in Figure 2.6, which produce a nominal voltage of 1180 V. Five cells are grouped to form a sub-module, with a total of 1416 sub-modules [151]. Both employ series-connected cells in several strings to form a sufficient number of cells, where the cells are specially designed

for deep discharge with a capacity of 2600 Ah at C/4 rate [191] and 1000 Ah at C/5 rate [192] respectively. The cells are specially tailored to have a very low internal resistance and a fast response time. The battery pack in Chino BESS is able to deliver 40 MWh at 10 MW power for four hours, and maximum 52.7 MWh at 10.54 MW power for five hours during daily discharge at 80 % DOD [193] [195]. BEWAG BESS was installed to enhance frequency control and provide a rapid-response (spinning reserve) capacity to the isolated island utility, where it is able to supply a maximum power of 8.5 MW for at least 30 minutes during worst-case operating conditions [152].

The 32MW / 8 MWh Laurel Mountain BESS employs 800000 A123 patented Nanophosphate Lithium Iron Phosphate cells connected in series/parallel to achieve the desired voltage/storage capacity [196]. Cells are grouped to form a sub-module, sub-modules form a tray and eight trays form a string and eighteen trays are placed in a container, which sums up to 800000 cells [197] in the battery pack shown in Figure 2.7. Similarly, the 27 MW / 6.75 MWh GVEA BESS is composed of 13760 Saft SBH 920 pocket plate NiCd cells arranged in four parallel strings illustrated in Figure 2.8, each string has 3440 cells connected in series and each string is split into eight groupings, each with an open circuit voltage (OCV) around 600 V [198].

The cell arrangement employed in all the mentioned systems allows each string of lower voltage to be disconnected from the rest of the system using DC switches for maintenance purposes. Alternately, additional strings can be installed, for instance, additional four strings can be installed to deliver 40 MW for 15 minutes in the GVEA BESS illustrated in Figure 2.8 [199].

It is worth to mention that the A123 patented Nanophosphate Lithium Iron Phosphate cell employed in Laurel BESS has excellent safety performance and exceptional cycle life. It has wider range of SoC and is able to deliver maximum energy [200]. The cell is able to pulse at a discharge rate as high as 100 C (continuously discharged at 35 C) [201-202] and it delivers high power and energy density [203-204].

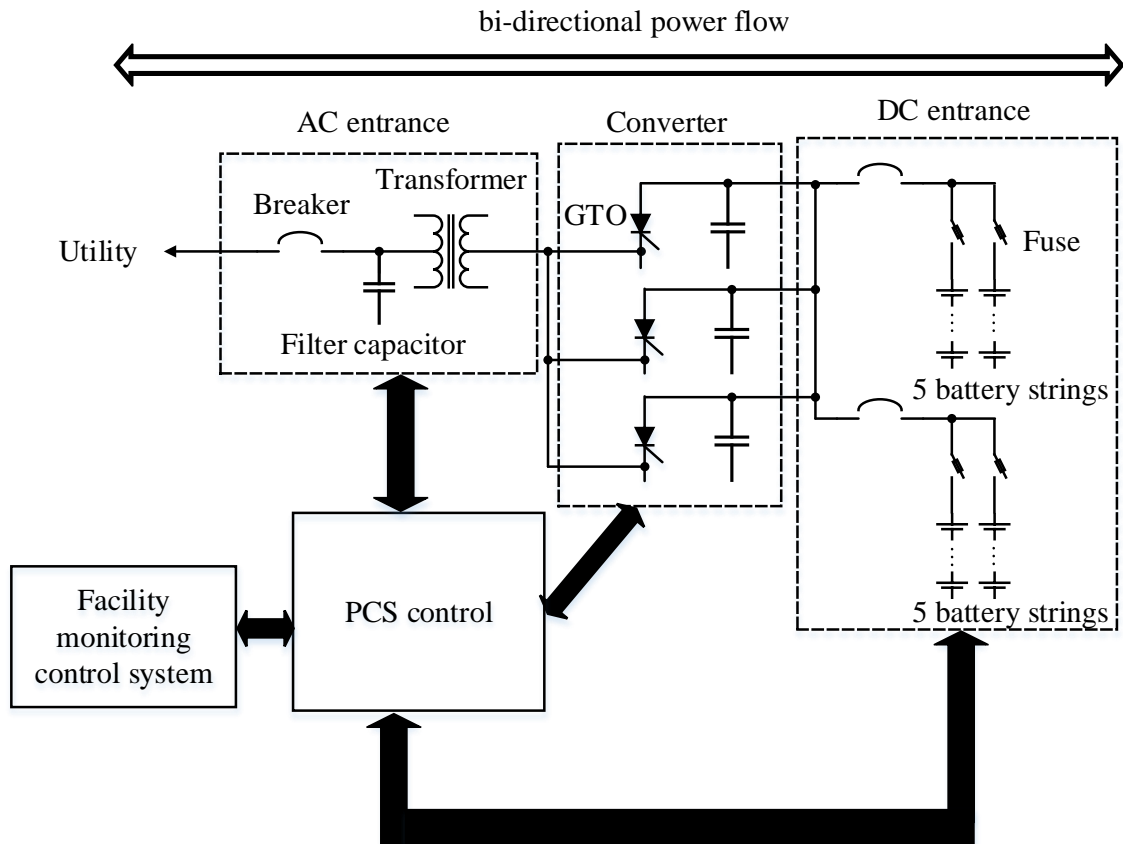


Figure 2.5 Chino : PCS layout (adapted from [195])

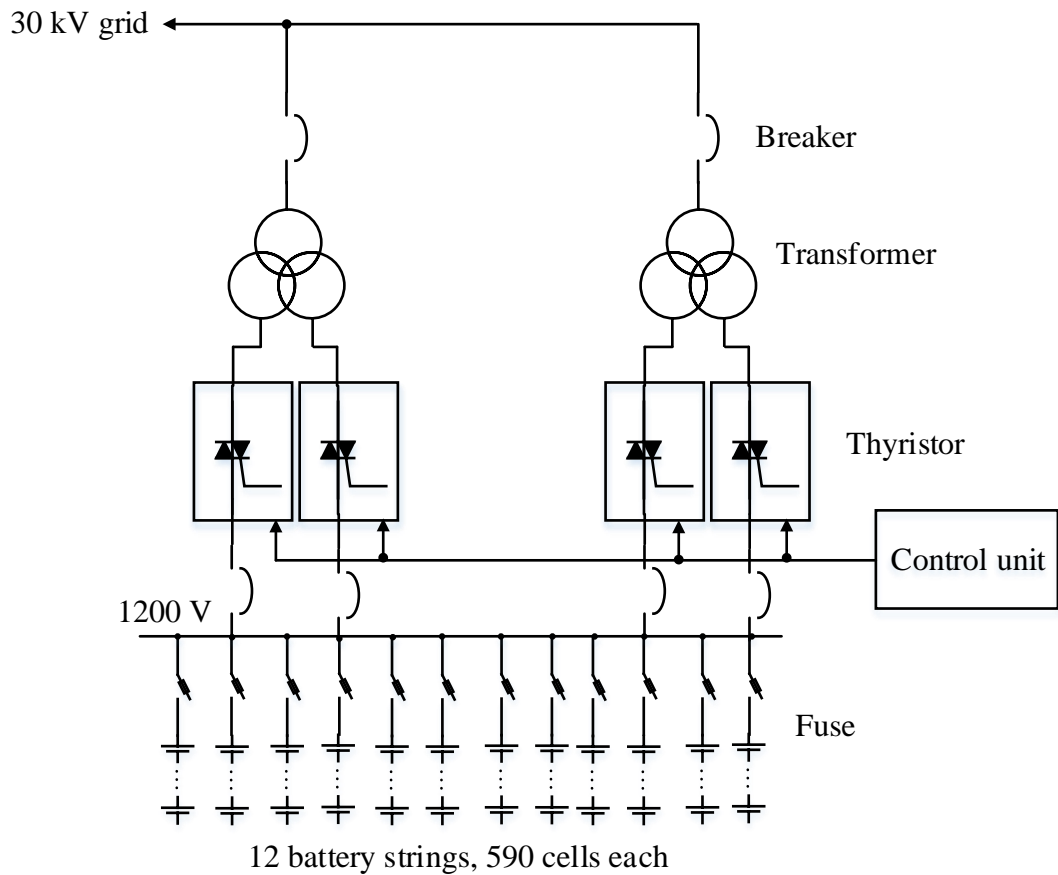


Figure 2.6 Block diagram of 17 MW / 14 MWh BEWAG BESS (adapted from [152])

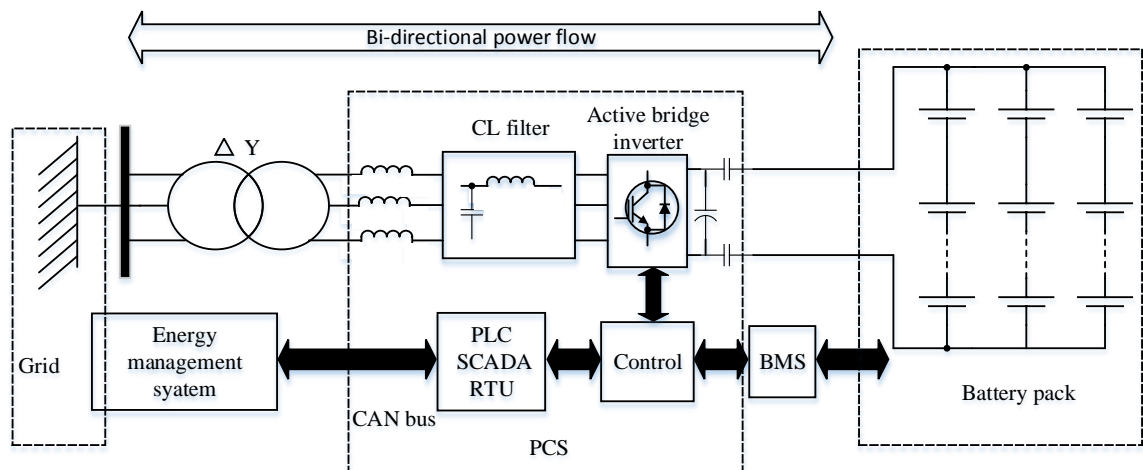


Figure 2.7 Block diagram of 32MW / 8 MWh Laurel Mountain BESS in Elkins, US (adapted from [146])

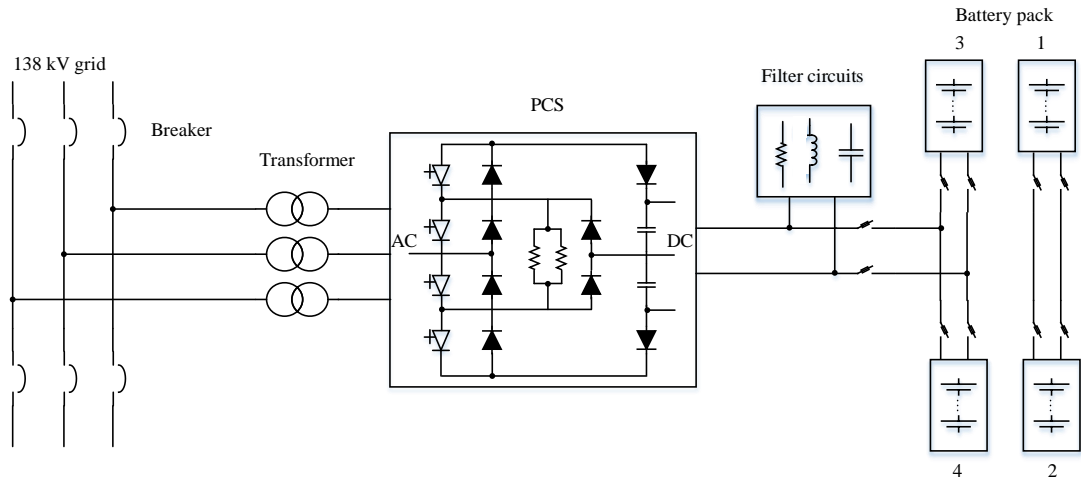


Figure 2.8 Block diagram of 27 MW / 6.75 MWh GVEA BESS in Fairbanks, US (adapted from [205-206])

2.5.2 Power Conversion System (PCS)

Among four BESSs discussed above, the 40 MW / 46 MVA PCS in GVEA BESS in Figure 2.8 interfaces battery pack to AC system using ABB's IGCT technology, an advanced type of GTO controlled by programmable high-speed controller. IGCTs have the advantages of lower conduction and switching losses, with exceptional switch-off characteristic that allows a converter design without snubber [155] [178] [207].

Figure 2.7 illustrates the bi-directional power flow in the PCS provided by SSD Parker in Laurel BESS utilising Parker 890GTB-series PCS [208], a modular inverter design containing an array of insulated gate bipolar transistors (IGBTs). IGBTs are switched on and off by sequenced gate drivers coordinated by a supervisory control system interfacing with a supervisory control and data acquisition (SCADA) system. Harmonic filters (CL filters) are used to eliminate the harmonic distortion in order to deliver pure sine wave power [209]. Similarly, the microprocessor-based monitoring and control system of Chino BESS depicted in Figure 2.5, provides a highly automated supervisory control and

data acquisition. It also acts as a BMS to monitor the cells and protect them from operating outside its safe operation area during charging and discharging operations [210].

The battery pack of BEWAG BESS in Figure 2.6 is interfaced to a 30 kV distribution network via two AEG 12-pulse, line-commutated thyristor-based inverter, each rated at 1200 V, 8.5 MW while the 10 MW PCS in Chino BESS illustrated in Figure 2.5, consists of 3, 6-pulse (18-pulse) self-commutated GTO voltage source converter (VSC), which converts the 12 kV AC grid to 1750-2800 V DC for charging and vice versa for discharging [211]. Both are capable of four-quadrant operation with the latter being able to yield a response time around 16 milliseconds [212].

Overall, PCS is used in the BESS to enable AC power from the grid to be converted to DC to charge the battery pack in a controlled manner, and discharge DC battery power to feed the grid. In certain systems, not all converters are used all the time, for instance, in BEWAG BESS, during its operation as spinning reserve, both converters were used to supply 17 MW, however, only one converter is used to provide 8.5 MW while another converter serves as a standby back-up system during frequency control operation [153]. Some PCSs incorporate BMS to manage charging/discharging and provide notification on the status of the battery pack based on cell voltage, temperature and SoC. PCSs in the existing grid-scale BESSs will be discussed in Section 3.5 in conjunction with the proposed structure of BESS in this work.

2.6 Balancing Control in BESSs

Taking a Lithium cobalt oxide cell as an example, a cell operates over a range of roughly 2.5 V to 4.2 V (fully discharged to fully charged). Different cell chemistries have slightly different ranges as shown in Table 2.6. Cells made today are typically limited to capacities of ~100 Ah due to manufacturing constraints and therefore each cell may be expected to store 250–420 Wh. It can therefore be estimated that a BESS must contain something in the order of 300000 individual cells to provide a 100 MWh energy storage capacity. Although schemes of this size have yet to be implemented, demonstration of BESS schemes (of the order of 1 MW) typically use series connections of 100–200 cells to form battery packs with a terminal voltage of 300–600 V. These battery packs are then interfaced to the AC grid by way of an optional step-up DC–DC converter and two- or three-level pulse-width modulated (PWM) inverter. This design and associated technology is similar to what is implemented in a battery electric vehicle, except that the AC connection is to the grid rather than a synchronous motor.

To achieve greater power and energy capacity, many such units can be connected at the same grid connection point. However, to reach much larger capacities, increasing the terminal voltage of the battery pack is desirable in order to reduce the number of parallel units required. For example, a 100 MWh BESS might use a voltage of ~20 kV at the primary of a grid interface transformer for step-up to transmission voltage (i.e. similar to typical thermal generating units).

Cell mismatch or imbalance is common in the battery pack due to two major sources; internal and external. Internal imbalance refers to the manufacturing difference in

Table 2.6 Typical properties of various Li-ion chemistries [213-214]

Li-ion chemistry	Lithium Cobalt Oxide	Lithium Manganese Oxide	Lithium Nickel Manganese Cobalt Oxide	Lithium Iron Phosphate	Lithium Titanate
Operating voltage range (V)	2.5-4.2	2.5-4.2	2.5-4.2	2.5-3.6	1.5-2.8
Nominal voltage (V)	3.6-3.7	3.7-3.8	3.6-3.7	3.3	2.3-2.4
Discharge rate (continuous)	2-3 C	> 30 C	2-3 C	10-125 C	10 C
Cycle life (100 % DOD to 80 % capacity)	500	500	500	1000	4000
Ambient temperature during charge (°C)	0-45	0-45	0-45	0-45	-20-45
Ambient temperature during discharge (°C)	-20-60	-30-60	-20-60	-30-60	-30-60

charge storage volume and internal resistance as well as the differences in self-discharge rate. External imbalance includes temperature difference across the battery pack, which affects the aging behaviour of each cell [215]. Over the life of the battery pack, some cells may be charged/discharged for more cycles than the others, thus, the individual cells may age differently where some cells may become mismatched with respect to other cells in the battery pack [216].

Cell mismatch is less of a problem with parallel connection where cells tend to be self-balancing since parallel connection holds all cells at equal voltage, while allowing charge to move between cells. Therefore, cell voltages are forced to be equal, leading to automatic cell balancing. Cells from the same manufacturing batch are chosen to form a battery pack to prevent one cell from charging another due to internal resistance difference between cells connected in parallel [217]. A weak cell in a parallel connection will not affect the voltage but will result in a lower runtime due to reduced current handling. However, a weaker cell in series connection is especially critical as the available capacity

of a battery pack is limited by the weakest cell, in which the weakest cell determines when the charging and discharging operation has to be terminated [218].

In a series-connection where all cells are loaded with same current, when cell mismatch is left uncompensated, the weak cells in the battery pack tends to be deep discharged or overcharged during operation which negatively affect the cells' lifespan. Over many charge and discharge cycles, the weak cells tend to go out of balance in the form of unequal voltage and SoC, the difference does not stay the same but grows with time. This subsequently leads to premature cell degradation or deterioration, capacity loss or the failure of the entire battery pack as the available capacity of a battery pack is limited by the weakest cell [219]. Consider a battery pack consisting of three Li-ion cells with different capacities (8.1–8.5 Ah) as illustrated in Figure 2.9, three cells are connected in series. During charging, the weakest cell will reach the maximum charge level before the rest of the cells in the battery pack and during discharging, again, the weakest cell will reach the minimum discharge level first. Therefore, the capacity of the battery pack is determined by the weakest cell, 8.1 Ah.

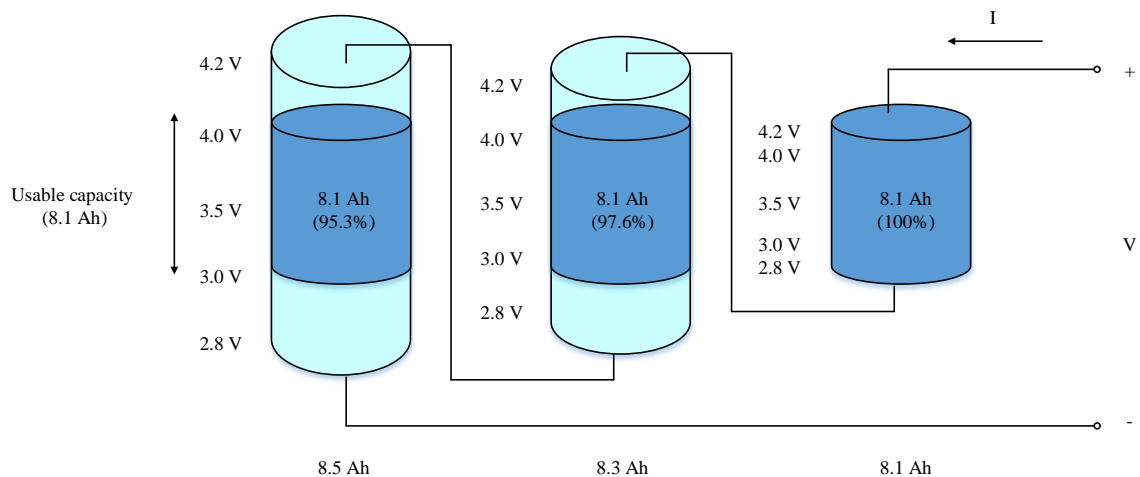


Figure 2.9 Capacity mismatch between three cells

Cell balancing or charge equalisation is, thus, an important task performed by the BMS to reliably monitor the cells in order to minimise the mismatch across the cells, which can significantly improve the overall capacity [220] and lifetime of a battery pack for optimum performance [221]. Cell balancing can be performed using either passive cell balancing or active cell balancing. Passive cell balancing, also known as a dissipative charge equalisation, removes excess charge from fully charged cell(s) through a resistive element until the charge matches those of the lower cells in a battery pack. There are two approaches in passive cell balancing. First, fixed shunt resistor is used in parallel with each individual cell to limit the cell voltage by continuously bypassing the current for all cells. The energy from the cell is transformed into heat. It is important to note that the shunt resistors used across the cells are of the same value. A cell with a higher voltage will have lower charging current because a higher current will flow (i.e. be bypassed) through the shunt resistor, and thus the cells get balanced over time. This configuration is only applicable to Lead-acid and Nickel-based cells because these cells can be exposed to light overcharge conditions without permanent cell damage as they can be trickle charged at a low current until all cells are fully charged. However, this is not the case for Li-ion cells as some cells will still be overcharged and this will lead to catastrophic failure [222].

Second, a switched shunting resistor is used instead to remove energy in a controlled manner using switching devices or relays. Cell voltage is monitored continuously and the shunt resistor is switched on once the cell reaches the maximum allowable voltage. This approach has been applied to Li-ion cells in [223-224]. The implementation of passive cell balancing is straightforward as it requires only one controllable switch and dissipative element per cell. Although it is relatively simple and

low cost, passive cell balancing is not efficient as excess energy from a higher capacity cell is dissipated as heat [225].

Active cell balancing has emerged to deal with the losses associated with passive cell balancing where it employs inductors/transformer, capacitors, or converters to transfer charge from a higher energy cell to a lower energy cell. In this way, energy is not wasted but moved among the cells within a battery pack, thus, cell balancing can be achieved. This approach does not depend on the chemical characteristics of a cell and can be used for all battery technologies. Figure 2.10 demonstrates the fundamental difference between passive cell balancing and active cell balancing. For simplification, assuming there are only three cells in a battery pack, each cell exhibits a distinct level of SoC before balancing takes place (70 %, 60 %, 50 %), where cell 1 has the highest SoC while cell 3 has the lowest SoC. When passive cell balancing is applied, cell 1 and cell 2 are discharged until they reach the same SoC as the worst cell, i.e. cell 3. Excessive energy is dissipated or thrown away while discharging cell 1 and cell 2, thus, this reduces the system efficiency. Active cell balancing enables the charge transfer from cell 1 to cell 3, such that all cells have equal SoC, i.e. 60 % as shown in Figure 2.10. Active cell balancing offers the advantages of high efficiency and high balancing speed compared to passive cell balancing approach. However, such increased efficiency comes at a cost of complexity and consequent cost of manufacturing [226].

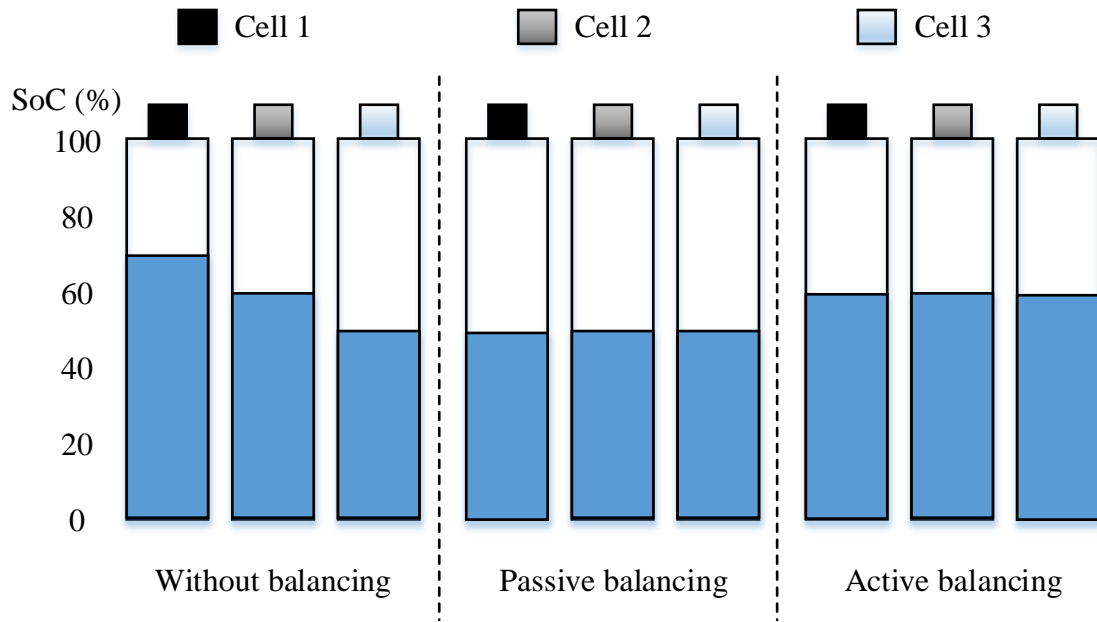


Figure 2.10 Passive cell balancing and active cell balancing

As illustrated in Figure 2.11, there are many methods to perform active cell balancing. They can be grouped into three major categories according to the active element used for storing the energy such as capacitor, inductor or transformer and energy converter. Under each category, there are many different circuit configurations and the details can be found in [208-209]. Recent research proposes using a combination of inductor-capacitor or transformer-capacitor or switched capacitor or switched inductor with controlled switches or converters to perform active cell balancing. Other literatures [227-230] group the balancing circuits into five topologies: cell-to-heat (passive cell balancing), cell-to-cell, cell-to-module, module-to-cell, and cell-to/from-module, according to the way by which energy is transferred between the cells.

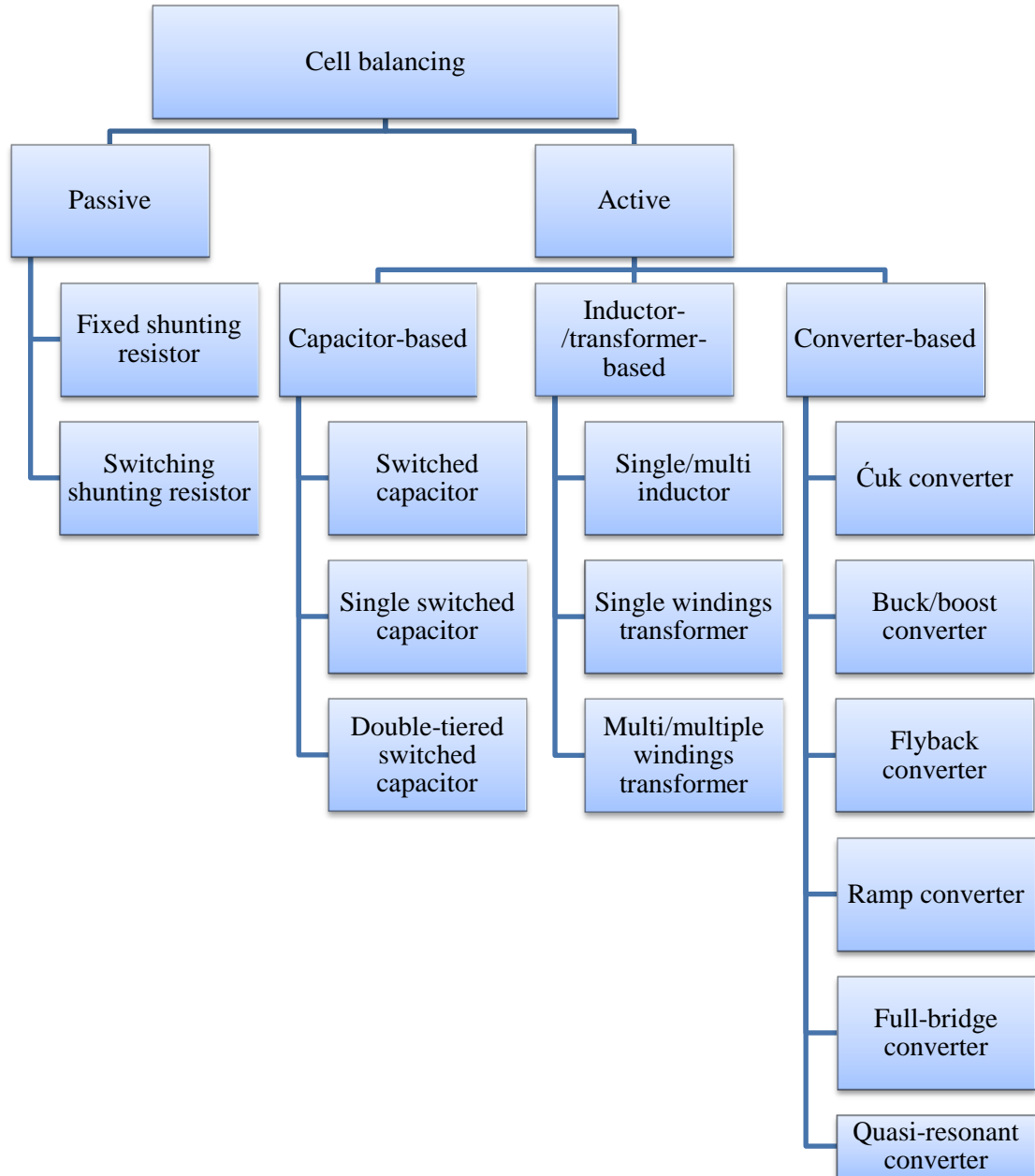


Figure 2.11 Classification of active cell balancing

Generally, capacitor-based active cell balancing is only applicable to system with balancing current within 100 mA as significant energy losses occur during capacitor charging. Due to the fact that a distinct voltage difference between unbalanced cells can only be observed when the capacitor is highly discharged, this method is only efficient near

the end of discharge [231]. Consequently, the balancing speed is low due to limited amount of charge removal in one cycle [232]. Switched capacitor technique, for example, requires a large number of switches, and so a large amount of energy dissipates in the switches.

Inductor-based active cell balancing allows higher balancing current up to several Amperes and it performs balancing independently of cell voltage. Cell balancing based on multiple windings transformer technique is efficient and inexpensive, however, it is challenging to implement multiple windings in a single transformer when there are hundreds of cells in a grid-scale BESS [233]. In recent years, there has been increasing interest on converter-based cell balancing techniques, basically built around standard or modified DC-DC converters [234], forward or flyback converters [233], buck-boost or boost-buck converters [235-237] and others [238-239].

Table 2.7 presents a summary of the key aspects of different cell balancing techniques and compares the performance among them associated with efficiency, balancing speed, size, and major components needed to balance N cells in M modules [240-243]. Combined with an optimal balancing control algorithm, active cell balancing is preferable for efficiency-conscious applications where delivering the maximum available capacity is top priority [244].

Table 2.7 Comparison of cell balancing techniques [227-228] [240-243]

Technique	Components	Efficiency	Balancing speed	Charge / discharge	Applications
Fixed shunting resistor	N resistors	Poor	Satisfactory	Fixed	Low power
Switching shunting resistor	N resistors, N switches	Satisfactory	Good	Bi-directional	Low power
Switched capacitor	N-1 capacitors, 2N switches	Good	Satisfactory	Bi-directional	Medium / high power
Single switched capacitor	1 resistor, 1 capacitor, N+5 switches	Very good	Satisfactory	Bi-directional	Medium / high power
Double tiered switched capacitor	N capacitors, 2N switches	Good	Good	Bi-directional	Medium / high power
Modularised switched capacitor	N-1 capacitors, 2N+2M switches	Satisfactory	Satisfactory	Bi-directional	Medium / high power
Single inductor	2N switches, 2N-2 diodes	Good	Very good	Bi-directional	Medium / high power
Multi inductor	N-1 inductors, 2N-2 diodes	Good	Very good	Charge	Medium / high power
Single winding transformer	2 inductors, N+6 switches, 1 diode, 1 winding transformer	Satisfactory	Good	Charge	Medium / high power
Multi-winding transformer	N+1 inductors, 2 switches, 1 winding transformer	Satisfactory	Good	Charge	Medium / high power
Multiple transformers	2N inductors, 1 switch, N diodes, N winding transformers	Satisfactory	Good	Bi-directional	Medium / high power
Modularised switched transformer	2N+2M inductors, M switches, N diodes, N+M winding transformers	Satisfactory	Satisfactory	Bi-directional	Medium / high power

Cuk converter	N+1 inductors, N-1 capacitors, N+1 switches	Good	Satisfactory	Bi-directional	Medium / high power
Buck-boost converter	N inductors, N capacitors, 2N switches	Good	Good	Bi-directional	Medium / high power
Flyback converter	2N inductors, 2N switches, N winding transformers	Satisfactory	Good	Bi-directional	Medium / high power
Ramp converter	N/2 inductors, N capacitors, N switches, N diodes, 1 winding transformer	Satisfactory	Satisfactory	Bi-directional	Medium / high power
Full-bridge converter	M capacitors, 4M switches	Very good	Very good	Bi-directional	High
Quasi-resonant converter	2N-2 inductors, N-1 capacitors, 2N-2 switches	Good	Satisfactory	Bi-directional	Medium / high power

2.7 Balancing Algorithms

Regardless of the cell balancing techniques described above, be it passive cell balancing or active cell balancing, appropriate balancing control algorithms are required to make decision regarding when to turn on a bypass switch or when to transfer energy among cells. Generally, balancing control can be implemented based on two types of divergence metrics either voltage-based or SoC-based balancing algorithm [245].

Cell voltage difference is the most typical manifestation of cell imbalance. Voltage-based balancing approach is extensively adopted by research and industry in BMS due to its simplicity. It uses direct measurement of terminal cell voltage divergence as the balancing criterion, where cell with the lowest/highest voltage is picked for balancing during charging/discharging. It is important to note that the fundamental causes for cell voltage difference on the level of cell chemistry and discharge kinetics have not been fully

explained [246]. Attempting to balance the cell voltage itself rather than the underlying cause can often do more harm than good. Research [233] has exhibited that voltage-based balancing control might result in a battery pack more unbalanced than without it. Therefore, it is important to understand the underlying causes of voltage imbalance: SoC difference, total capacity difference and impedance difference.

SoC difference is the only cause of voltage imbalance under a no-load condition (no current is flowing) as OCV is in direct correlation with chemical SoC in the function of $OCV = f(SoC, T)$ where T is temperature. In general, SoC difference results in OCV difference [239]. Battery chemistry such as Lead-acid, exhibits almost linear voltage change with SoC, therefore, it is possible to estimate how much SoC difference for a given voltage difference. Other chemistries, such as Li-ion and NiMH, have an almost flat voltage plateau in the mid-range of SoC (20 % to 80 %) where voltage is fairly constant [247]. Even when a SoC difference is as large as 5 % to 10 %, the corresponding voltage difference remains small and this makes voltage-based balancing control impractical to detect a weak cell. Consequently, this might cause protection circuits in the BMS to terminate the charging process before the battery pack is fully charged [248]. It is apparent that voltage-based balancing control is difficult to perform satisfactorily on these chemistries. This method, however, can be used when a Li-ion cell is fully charged or discharged, where the curve is much steeper towards both ends as illustrated in Figure 2.12 [249].

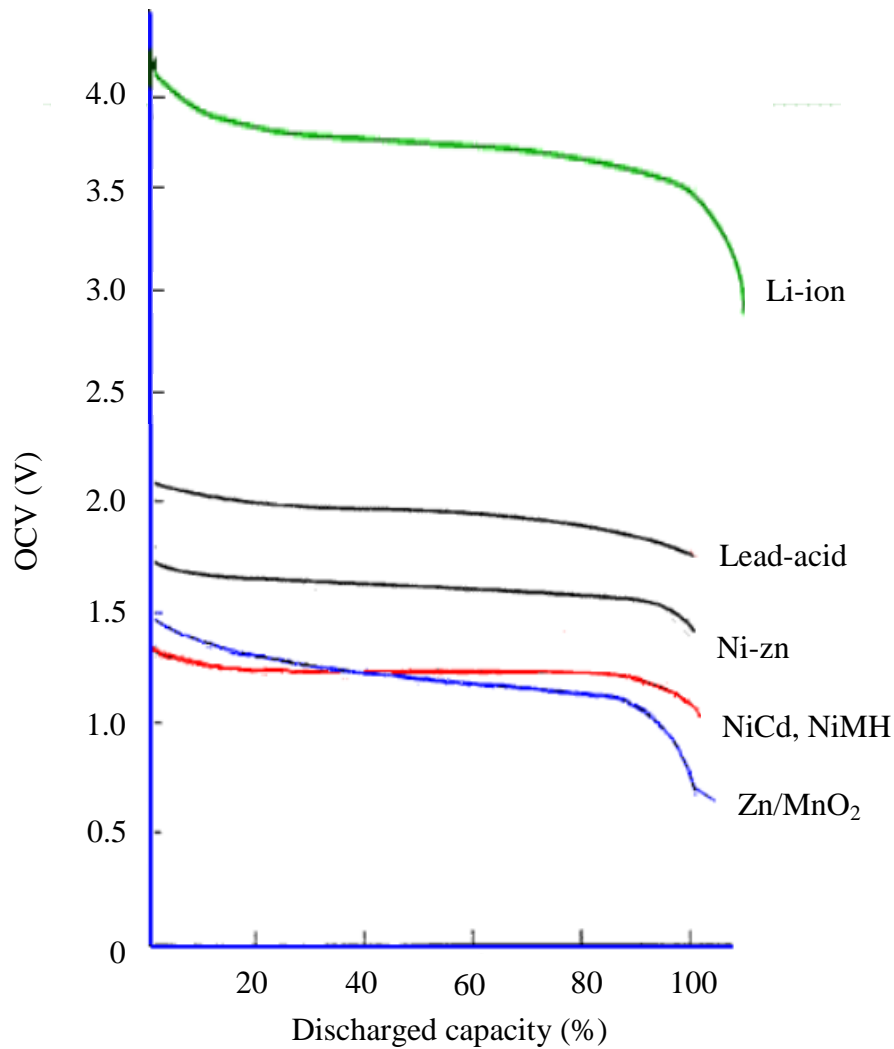


Figure 2.12 OCV-Discharged capacity curves for various cell chemistries [250]

Another cause of voltage difference among cells is the cell impedance difference, which occurs only under a loaded condition (current is flowing). Internal impedance differences among the cells with the same production batch can vary by around 15 %. Consider an IR equivalent circuit model in Figure 2.13(a), cell terminal voltage, V_t can be approximated as indicated in (2.1). During charging process (indicated by a negative current), cell with a higher R_{int} will exhibit a higher voltage; while discharging (indicated by a positive current), cell with a higher R_{int} will show a lower voltage [251].

$$V_t = OCV - IR_{int} \quad (2.1)$$

where I is the charging/discharging current and R_{int} is cell internal resistance.

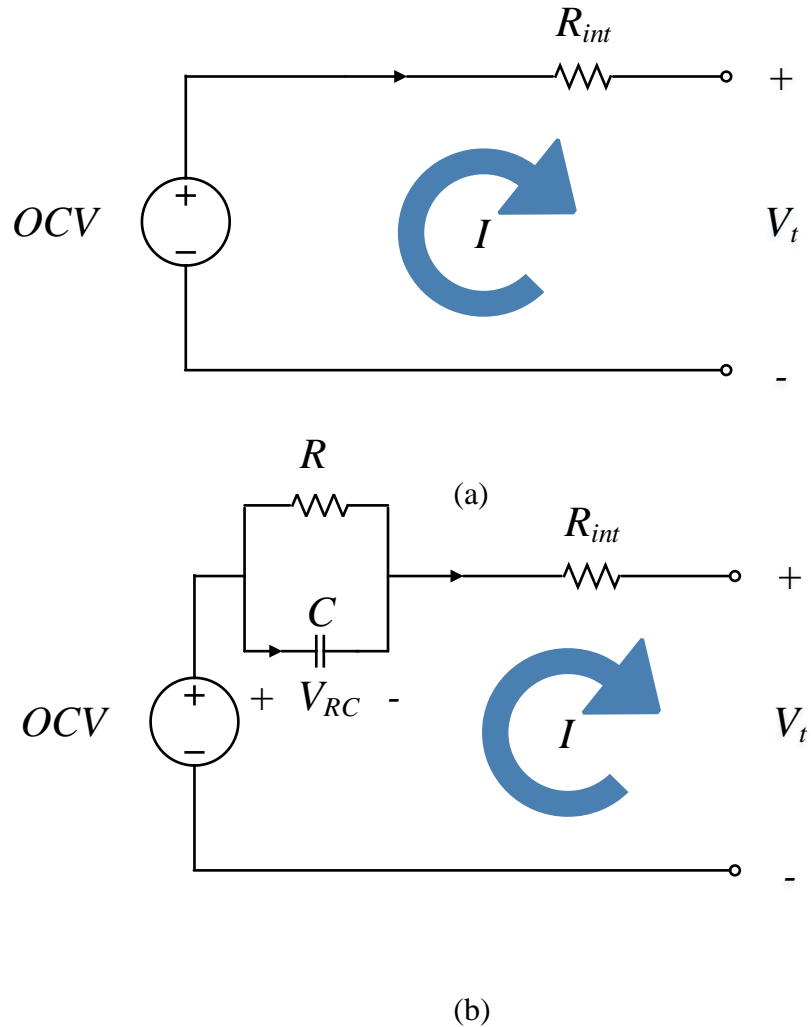


Figure 2.13 Cell equivalent circuit diagram (a) IR model, (b) RC model

Voltage-based balancing control using OCV as divergence criterion is considered a more effective way compared to using V_t [252]. Consider a RC equivalent circuit model in Figure 2.13(b), it consists of three parts including voltage source, OCV , ohmic resistance, R_{int} and R_c, C_c to describe the cell transient response during charging/discharging. Cell terminal voltage, V_t can be approximated as indicated in (2.2).

$$\begin{cases} V_t = OCV - V_{RC} - IR_{int} \\ \frac{dV_{RC}}{dt} + \frac{V_{RC}}{RC} = \frac{I}{R} \end{cases} \quad (2.2)$$

Upon the termination of charging or discharging, a cell takes certain period of time to return to the OCV due to the transient response and ohmic resistance of the cell [253-254]. OCV cannot be measured directly under loaded condition and it has to be estimated instead and this can be very challenging. It is therefore not suitable for a real-time system where cells are continuously charged or discharged [215].

Existing BESSs employ BMS to determine SoC and most commonly, OCV is used as an indicator of SoC as cell's SoC decreases with its OCV. This method is more accurate for some chemistries than for others. However, in all cases, complex non-linear models are required to relate the OCV and SoC. This approach is risky for any cell chemistry as it can lead to potential overcharging or deep discharging of a cell especially when the cell degrades and losses capacity over time [112].

Ideally, battery packs should be balanced on the basis of SoC. SoC-based balancing control requires accurate cell SoC and capacity estimation. Techniques for SoC and capacity estimation have been applied to most of the battery chemistries. SoC estimation will be discussed in detail in Section 2.8. If an accurate SoC is estimated, the balancing processes could be carried out at any time whenever there is a SoC difference among the cells within a battery pack [244] [255]. Therefore, SoC-based balancing control has attracted great attention and many variations of SoC-based balancing control have been proposed [256].

2.8 SoC Estimation

SoC is generally expressed as the ratio of the remaining capacity, $Q(t)$ to the maximum capacity, Q_{max} , indicated in (2.3) where SoC takes a value between 0 and 1.

$$SoC(t) = \frac{Q(t)}{Q_{max}} \quad (2.3)$$

Accurate SoC estimation is of essential importance for BMS as it is an indicator of the operating conditions of a battery pack that reflects the system performance. SoC is used to facilitate charging/discharging decision in order to protect cells from deep discharging or overcharging, ensuring a safe and reliable operation. SoC is more of a mathematical concept to aid in quantifying the energy in each cell but not a physical parameter. There are thirty or more variables affecting SoC of a cell, some of which are much more significant than others. Ideally, SoC estimation has to take into consideration of all of these variables and this results in a highly complex process. These variables include the rate at which cells have been charged and discharged, the chemical composition of the various active chemicals and any doping which has been used, the possibility and effects of contamination, the shape and length of the physical current paths within the cell, the volume of electrolyte, the thickness of the electrolyte and the separator, the resistivity of the components, the rate of mass transfer of the ions through the electrolyte, the ambient temperature, the Joule heating effect, the self-discharge rate of the cells, the time between charges plus several other factors [255].

There have been many attempts to estimate SoC and many methods exist with the primary methods being Ampere-hour/Coulomb counting, voltage measurement, impedance measurement, neural network, fuzzy logic, and Kalman filtering. Table 2.8 lists the strength and weakness of each. SoC estimation remains a challenging task in a grid-scale BESS due

to measurement errors, mapping nonlinearity, large variations of the operating conditions from cycle to cycle, such as temperature, and the high sensitivity of the voltage inverse mapping. Details of each SoC estimation method can be found in [256-260].

Table 2.8 Comparison of SoC estimation methods [256-260]

Methods	Inputs	Advantages	Disadvantages
Coulomb counting	Current, usable capacity, initial SoC	Easy to implement, high accuracy if input parameters are known	Open-loop, needs accurate value of initial SoC, current measurement and usable capacity, not suitable for cells under very dynamic conditions
OCV method	Voltage, idling time	Accurate	Open-loop, sensitive to the voltage sensor precision, requires idling time, unsuitable for cells with flat OCV-SoC relationship
DC resistance	Resistance	Simple	Not accurate, sensitive to disturbances
AC impedance	Resistance	Accurate	Complicated
Discharge test	Capacity, remaining capacity	Simple	Time-consuming, energy loss, only suitable for off-line applications
Neural networks	Current, voltage, initial SoC, cumulative charge etc.	Suitable for all kinds of cells, good nonlinearity mapping approximation	Require large amount of training data, sensitive to the amount and quality of training data
Fuzzy logic based approaches	Current, voltage etc.	Good nonlinearity mapping approximation	Require large amount of training data, sensitive to the amount and quality of training data, low accuracy
Kalman filtering	Current, voltage, capacity, cell model, initial SoC, self-discharge rate	Accurate, closed-loop, on-line, dynamic, insensitive of noise and error of initial SoC value	Complicated, computationally expensive and demanding, highly dependent on the model accuracy

Coulomb counting integrates current over time to estimate SoC based on (2.4). It requires a precise measurement of current going in and out of a cell ($I(t)$), initial SoC (SoC_0), and also knowledge of the present cell capacity (Q_{max}).

$$SoC(t) = SoC_0 + \frac{1}{Q_{max}} \int_0^t I(\tau) d\tau \quad (2.4)$$

It is the most widely used approach due to its simplicity and low-cost, however, this approach is prone to errors due to cumulative integration of current sensor offset, current sensor signal noise, and inaccuracy of on-line assessment of initial SoC and actual cell capacity. When Coulomb counting has been used over a long period of time, cumulative integration errors could lead to significant inaccuracy of SoC estimation unless re-calibration is performed. As this approach relies entirely on current measurement, any signal noise of current sensor will affect the accuracy of the SoC estimation [262]. It requires an accurate initial SoC, any error in this value will affect the subsequent SoC values. The actual cell capacity is not constant; the usable or present capacity is time-variant depending on current profile, temperature etc. [262].

SoC estimation based on voltage can be divided into two categories: V_t methods and OCV methods. V_t methods are based on V_t change due to internal impedance when a load is connected to the cell. These methods are straightforward as voltage can be measured online; however, the estimated SoC is inaccurate as there is voltage fluctuation due to load current variations and/or diffusion dynamics of a cell. OCV methods use a pre-determined OCV-SoC look-up table to estimate SoC [263]. These methods provide a more accurate estimation compared to V_t methods as the cell has been idle (typically a period of at least two hours) to reach equilibrium state before the OCV is measured [256]. The requirement of sufficient relaxation period potentially impedes it from being used in a real-time grid-

scale BESS [264]. OCV methods work especially for a Lead-acid cell due to a linear relationship between SoC and OCV [265]. SoC estimation based on voltage method is the easiest way to implement although it is highly prone to error as voltage varies widely with temperature; OCV of a cell is lower in a low ambient temperature than that in a high ambient temperature, this may lead to SoC estimation error unless appropriately compensated for.

Several artificial intelligence-based methods have been designed such as using neural networks, fuzzy logic, and Kalman filtering. Neural networks estimate the SoC based on a large amount of training data without requiring an accurate cell model or detailed internal structure. The systems typically consist of three layers: input layer, hidden layer and output layer. Careful selection must be made so that only parameters that contribute towards the accuracy should be chosen as candidates for the input layer. These parameters include charging/discharging current, cell terminal voltage, starting voltage, temperature etc.. The output layer of the system produces an estimated value of SoC. Neural networks suffer from high computational requirement, the cost is rather high, thus, it is generally used in small battery packs. The accuracy of SoC estimation in such system is highly dependent on training data and method used to train the data [266].

In fuzzy logic based approaches, an initial cell model is developed and used for measurement of parameters such as cell voltage, current and temperature. These data are compared with actual measurement, the feedback error is used to adjust the fuzzy logic controller and over several corrections, a relatively ideal cell model can be obtained for an accurate SoC estimation [267]. Similar to neural networks, fuzzy logic based approaches have large storage requirements and high computational complexity [268].

In Kalman filtering methods, relationships between SoC and accurate measured state variables such as voltage and current are used to develop a cell model [269]. The cell model can be either a numerical, state-space or an equivalent circuit model [270]. The basic principle is to estimate SoC based on the cell model and this value is compared with output measurements and state estimates are updated accordingly to reduce the difference between the estimated and measured values [271]. An advantage of the Kalman filtering estimation methods is that they can automatically provide an estimated SoC value in the time-varying state of a dynamic system that is prone to noise [272]. However, these methods are subject to model error as they require an accurate cell model that can exactly represent the dynamic state. Also, estimation time increases with an increasing number of parameters in the cell model [273]. Hybrid models benefit from the advantages of each SoC estimation method as integration of several individual approaches gives rise to estimation accuracy. For example, the combination of fuzzy logic based approaches with neural networks forms an integrated system named fuzzy neural network possessing the advantage of both. Research [274] proposes combining both Coulomb counting and OCV approaches to estimate SoC for a Li-ion cell for increased accuracy and robustness. Coulomb counting is used for the mid-range SoC where OCV remains constant. OCV is used at both ends of its SoC range where voltage increases significantly when full, and drops rapidly when it starts getting empty. OCV method also serves as an effective way to calibrate the cumulative error in Coulomb counting method [275].

2.9 Challenges in using BESSs - Managing Cell Failure

Cell design faults such as weak mechanical design, poor quality material or poor production methods may contribute to cell failure and these occur during manufacturing process and thus, are known as internal parameters. The capacity of a cell decreases with the number of cycles. This process is known as aging; it is not reversible and eventually results in cell failure. Cell aging or degradation often encounter various complex and coupled physical–chemical processes during operation, including temperature/thermal effects, dynamic duty cycles, time between operations, and other environmental factors, these are known as external parameters [276].

Cells contribute to the large capital investment needed in a grid-scale BESS, considering the lifetime cost, cell lifetime is substantially shorter than any other components in a BESS. It is important to quantify cell degradation process in order to help understand the mechanism of capacity decrease and power fading, in an attempt to better understand the remaining useful life of a cell, a useful parameter in a grid-scale BESS. However, the quantifying process is rather challenging and complicated due to the inherent complexity of the physical–chemical processes occurring within cells, for example, cell aging can result from a number of various operating conditions and their interactions, thus, cannot be studied independently [277].

Cells must be operated within the pre-defined safe and reliable operating regions, commonly restricted by voltage and temperature windows [278]. As indicated in the Arrhenius equation, the rate of unwanted chemical reactions that cause permanent damage to the cell is exponentially related to temperature, it doubles for each increment of 10 °C [279]. Elevated temperature accelerates the cell degradation, which causes a rapid

attenuation in capacity, thermal runaway and premature cell failure [280]. Thus, temperature change in cells during charging and discharging must be monitored and restricted according to manufacturer's specifications.

Cycle life can be improved by cycling a cell at a reduced DoD as the number of cycles to end-of-life is extended. For example, a Lithium-metal-polymer cell lasts 5000 cycles when it is discharged by 10 % in each cycle, or 500 cycles when the DOD is 90 % [281]. Overcharging or exceeding the upper limit of a cell voltage will result in irreversible structural degradation at the cathode and loss of active materials at both electrodes due to electrolyte oxidation, leading to capacity fade [282]. Also, it causes a significant rise in temperature and pressure, which will cause interruptions in the current path, short circuits within parts, or in the worst case catastrophic failure. Discharging a cell below the lower limit of a cell voltage can result in similar but less dangerous damage, which also contributes to cell aging. For example, research [279] shows that overcharging a NiMH cell by 0.2 V contributes to 40 % capacity fading while deep discharging a Li-ion cell by 0.3 V results in 66 % loss of capacity.

CHAPTER 3 PROPOSED STRUCTURE FOR A GRID-SCALE BESS

This chapter reviews the literature on medium-voltage power converters, and discusses the limitation of existing grid-connected BESS designs. The use of power converters for cell balancing in grid-connected BESSs is proposed.

3.1 Medium-voltage (MV) Power Converters

Figure 3.1 presents a simplified classification of MV power converters. Two major types of power converters are as the voltage source converter (VSC) and the current source converter (CSC). CSCs have been in commercial use since the 1950s and have been used in the majority of existing high voltage DC (HVDC) transmission systems in the world [283-284]. From about 1990 onwards, VSCs become viable due to the availability of high-power self-commutating power semiconductor devices such as gate-turn-off (GTOs) or insulated gate bipolar transistors (IGBTs). VSCs are often favoured over CSCs due to greater controllability and flexibility, e.g. independent control of active and reactive power [285-287]. The features of CSCs and VSCs are compared in Table 3.1.

VSCs operate at high switching frequency utilising Pulse-width Modulation (PWM) technique. Various VSC topologies and corresponding modulation schemes have been developed over the last 10-15 years. Conventional two-level VSCs are commonly used in low- or medium- power applications due to the voltage constraint of power semiconductor devices technology, with blocking voltage up to 6.5 kV [288-290]. The limited number of levels that can be constructed for the voltage waveform, results in high harmonic content in the induced AC current. In order to increase the output voltage, power semiconductor devices are connected in series to act as a single switch, however, due to the difficulties in

ensuring all series-connected devices are switched on at the same instant, the synchronisation of the switching becomes challenging and may result in voltage unbalance between the devices [291].

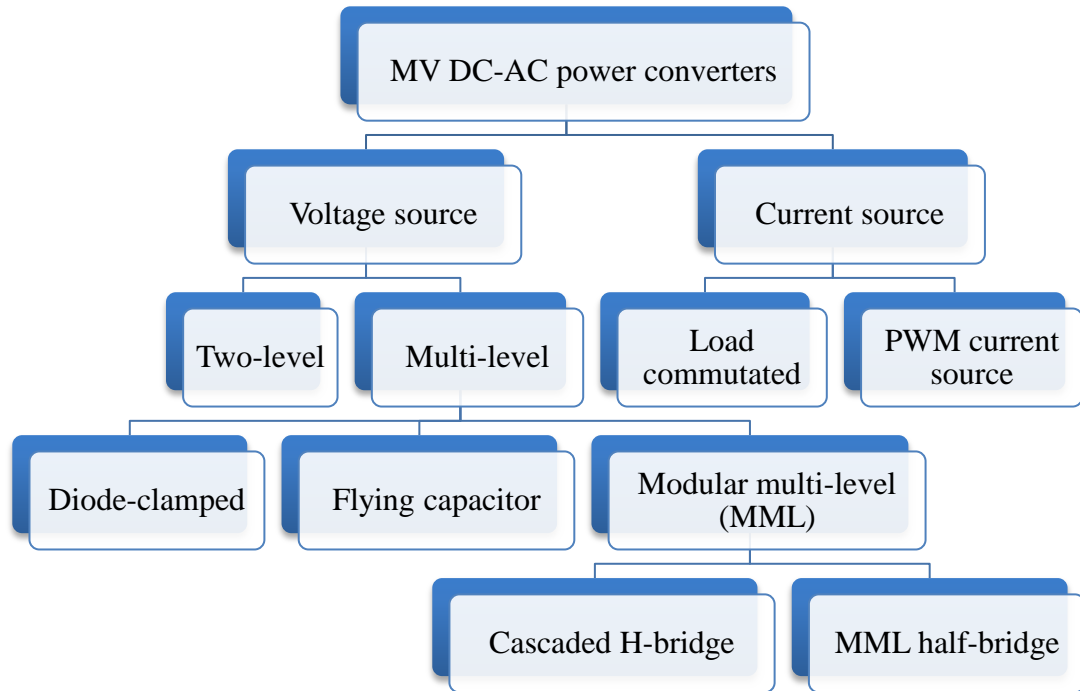


Figure 3.1 Classification of MV power converters (adapted from [268])

Multi-level VSC circuits were emerged to address this issue with the specific aim to overcome the voltage limit capability of power semiconductor devices [292]. Subsequently, it has been receiving considerably increasing attention for high power applications and several topologies and modulation schemes have been introduced and studied in-depth. A multi-level VSC has several advantages over a conventional two-level VSC. Some important attractive features of a multi-level VSC can be briefly summarised as follows [287] [296-297]: improved output voltage quality, low switching losses, high voltage capability and low voltage change rate ($\frac{dV}{dt}$) or voltage stress across switching devices. The diode-clamped [298], flying capacitor [299], cascaded H-bridge [300] and modular multi-

level (MML) half-bridge [301] are the most popular topologies and have been emerged as standard products for industrial MV power converters and commercialised by major manufacturers [302-303].

Table 3.1 Comparison between CSC and VSC technologies (adapted from [293-295])

Features	CSC	VSC
Maturity of technology	Mature	Developing
Valves	Thyristor	IGBT
AC harmonic filters	Large AC filters required	Less filtering required
Reactive compensation	Required	Not required
Reactive power exchange with AC system	50 % of active power transmitted	Independent control of active and reactive power
Reversal of power flow	DC voltage polarity reversal required	Controllable in both directions, no reversal of DC voltage polarity required
System response to changes	Slower	Fast ramp up/down capability
Commutation failure	Can occur	Does not occur
Converter station footprint (relative size)	200 m × 120 m × 22 m (100 %)	120 m × 60 m × 22 m (30 %)
Converter losses (per converter station)	0.5 % to 1 % of transmitted power	1 % to 2 % of transmitted power
DC voltage	Up to 800 kV available	Up to 350 kV available

3.2 Two-level VSCs

Two-level VSCs are widely used in low-voltage applications where the blocking voltage of a single power semiconductor device is sufficient. A series connection of power semiconductor devices is required in order to increase the converter voltage to suit MV systems. A schematic diagram of a three-phase two-level VSC and its output phase voltage relative to the supply mid-point are shown in Figure 3.2, where N is the number of cells and

V_{cell} is the individual cell voltage. A converter leg is formed by two groups of power semiconductor devices; each group consists of two or more devices in series depending on the DC voltage. Such converters can switch each output voltage between two possible voltage levels: $-\frac{1}{2}NV_{cell}$ and $+\frac{1}{2}NV_{cell}$. For example, for phase a , the voltage level of $+\frac{1}{2}NV_{cell}$ is achieved by turning the upper switch S_1 on and lower switch S_2 off, while the voltage level of $-\frac{1}{2}NV_{cell}$ is generated by turning the upper switch S_1 off and lower switch S_2 on. Although two-level VSCs offer advantages such as small volume, light weight, and simple circuitry, there are certain limitations including high levels of harmonic distortion and high $\frac{dV}{dt}$ due to synchronous commutation of series devices [304].

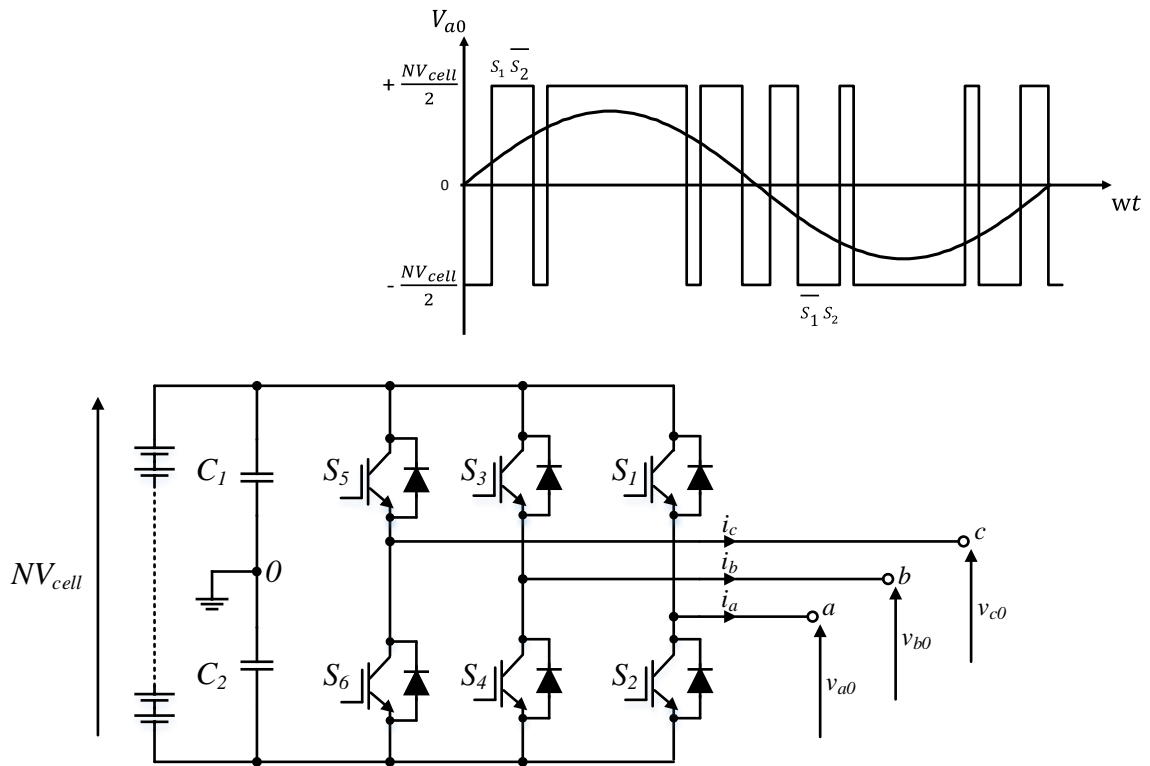


Figure 3.2 A classical two-level VSC

3.3 Multi-level Converters

Multi-level converters enable the realisation of direct interfacing with MV AC grids without requiring step-up transformers due to their ability to attain higher voltage with low harmonic [305-306]. The term ‘multi-level’ begins with three levels. The elementary idea is to synthesise a sinusoidal voltage from several lower voltage DC sources. The DC voltage sources can be capacitors or cells in this context. With increasing number of levels, the AC voltage produced from these DC voltage sources has more steps and so can approach a true sinusoidal voltage, i.e. significantly reduce the undesired harmonic content of the output voltage. Smaller voltage steps reduce the $\frac{dV}{dt}$ stress on the load leading to a higher quality waveform [307-309]. The best known multi-level inverter topologies are: diode clamped, flying capacitor, cascaded H-bridge and MML half-bridge. Operation and structure of these topologies are discussed in the following sections.

3.3.1 Diode-clamped Converter

Figure 3.3 shows the configuration of a three-phase three-level diode-clamped converter. It can generate three voltage levels ($+\frac{1}{2}NV_{cell}$, 0 and $-\frac{1}{2}NV_{cell}$) at the output of each phase (a , b and c) relative to neutral-point ‘0’ or supply mid-point. The diode-clamped converter was also called the neutral-point clamped converter when it was initially proposed as a three-level converter in the early 1980s [298] [310-311]. It is a modification of the two-level VSCs where there are twice as many power semiconductor devices as well as additional diodes. It can be generally configured as three-, four- or five-level topology and especially the three-level topology has found wide acceptance in MV applications due to its high voltage capability and high efficiency [115]. The DC bus capacitor is split into

two to provide a neutral point. Diodes connected to the neutral point are the clamping diodes which enable the generation of the zero voltage level.

Considering phase a as an example, the neutral-point clamped converter in Figure 3.3 generates a voltage level of $+\frac{1}{2}NV_{cell}$ at the output of phase a relative to neutral-point '0' by turning on switches S_{a1} and S_{a2} , while S_{a3} and S_{a4} are turned off. A zero voltage level is achieved by turning switches S_{a2} and S_{a3} on, with switches S_{a1} and S_{a4} off. Voltage level of $-\frac{1}{2}NV_{cell}$ is generated by turning on switches S_{a3} and S_{a4} , with S_{a1} and S_{a2} off. The concept can be extended to any number of levels by increasing the number of capacitors and diodes. Generally, for m number of levels, a diode-clamped converter comprises $(m - 1)$ capacitors on the DC bus. The voltage across each capacitor is $\frac{V_{dc}}{m-1}$. However, increasing the number of levels above three, the diode-clamped converter may experience capacitor voltage unbalance causing distorted output waveforms [312].

The major drawbacks of diode-clamped converter are the lack of modularity, the voltage balancing issue, the requirement of clamping diodes, and the unequal semiconductor-loss distribution [28].

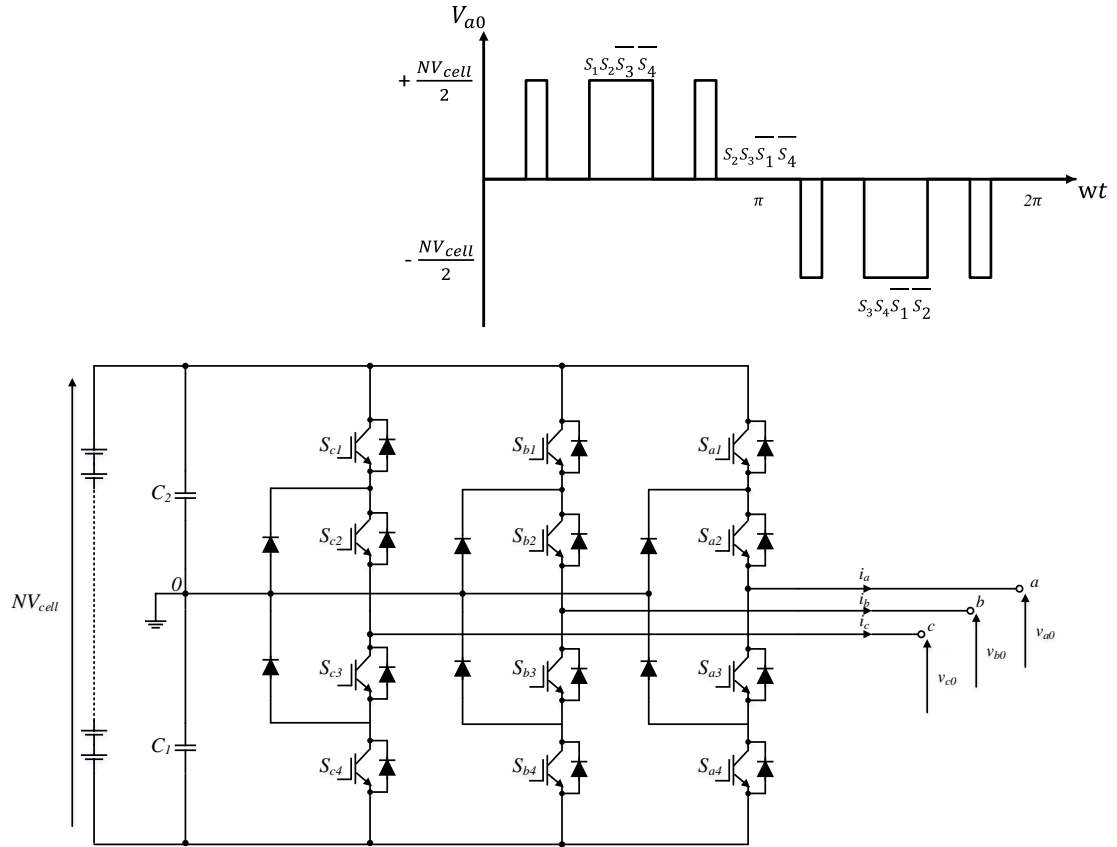


Figure 3.3 A three-phase three-level diode-clamped converter

3.3.2 Flying-capacitor Converter

Figure 3.4 illustrates the fundamental building block of a three-phase three-level flying-capacitor converter. Also known as capacitor-clamped, this configuration is similar to that of the diode-clamped converter except that the voltage across an open switch is constrained by clamping capacitors instead of clamping diodes. With proper selection of capacitor combinations, it is capable of solving the capacitor voltage unbalance issue in diode-clamped converters [287]. Output voltage is obtained by switching combinations of power semiconductor devices to allow adding or subtracting of the capacitor voltages. It can generate three voltage levels ($+\frac{1}{2}NV_{cell}$, 0 and $-\frac{1}{2}NV_{cell}$) at each output phase relative

to supply mid-point. Taking phase a as an example, voltage level $+\frac{1}{2}NV_{cell}$ is obtained by turning on switches S_{a1} and S_{a2} , while turning off S_{a3} and S_{a4} . A zero voltage level can be achieved using two distinct switching combinations: turning on switches S_{a1} and S_{a3} (or S_{a2} and S_{a4}), while turning off switches S_{a2} and S_{a4} (or S_{a1} and S_{a3}). A voltage level of $-\frac{1}{2}NV_{cell}$ can be generated by turning switches S_{a3} and S_{a4} on, with S_{a1} and S_{a2} off.

In a similar manner as in the diode-clamped converter, higher level flying-capacitor topology can be formed by extending the three-level structure. Generally, an m -level flying-capacitor converter requires a total of $\frac{(m-1)\times(m-2)}{2}$ clamping capacitors per phase leg in addition to $(m - 1)$ main DC-bus capacitors provided that all the capacitors are of same size.

The voltage synthesis in the flying-capacitor converter has more flexibility than the diode-clamped converter. The main constraint lies in the fact that it is required to pre-charge the capacitors before the start-up, also known as initialisation [313]. The need to pre-charge the capacitors increases complexity in control and cost [297]. Hence, this topology is mostly seen in large motor drive applications [314].

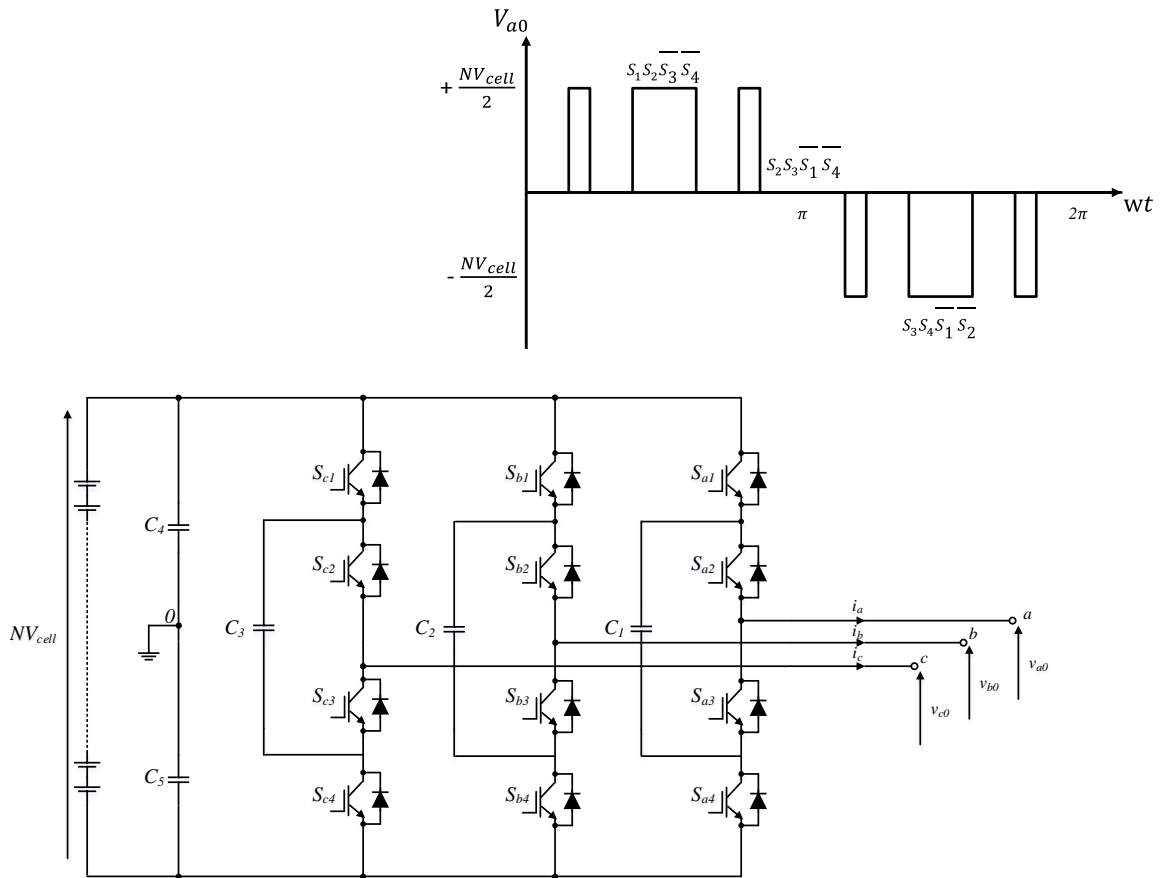


Figure 3.4 A three-phase three-level flying-capacitor converter

3.3.3 Modular Multi-level (MML) Converter

MML topology is based on a series connection of identical elements, called sub-modules (SMs); it was first introduced in 1975 [296] with H-bridge modules, while in 2002, a topology utilising half-bridge modules was introduced [315]. Two patents [316-317] were filed in 1997 which mark the advent of cascaded H-bridge converter for motor drives and grid applications.

Cascaded H-bridge converter consists of N series-connected H-bridge cell-converters² which are identical but individually controllable to synthesise a desired AC voltage. The H-bridge cell-converters are fed from separate DC sources where the DC sources are considered to be identical in that all of them are capacitors, solar cells or cells in this context. Figure 3.5 shows the fundamental building block of a three-phase cascaded H-bridge converter. The number of output voltage levels is $2N + 1$, where N is the number of cell-converter. The output phase voltage is the results of superimposing the voltages generated by all the cells in the phase. Taking phase a as an example, the output voltage is $V_{cell,a1} + V_{cell,a2} \cdots + V_{cell,aN}$. Each H-bridge cell-converter can generate three voltage levels ($+V_{cell,a1}$, 0 and $-V_{cell,a1}$). Voltage level $+V_{cell,a1}$ is obtained by turning on switches S_{a12} and S_{a13} while turning off S_{a11} and S_{a14} . A zero voltage level can be achieved by either turning on two upper switches S_{a11} and S_{a13} , or two lower switches S_{a12} and S_{a14} . A voltage level of $-V_{cell,a1}$ can be generated by turning switches S_{a11} and S_{a14} on.

An m level cascaded H-bridge converter needs $2(m - 1)$ power semiconductor devices. Only odd numbers of levels are possible: indeed the first cell gives three levels whereas the others always add two levels more. To obtain a clearer comprehension of how the voltage levels are produced, Table 3.2 shows the overall switching state as well as the resulting output voltage. Apart from maximum and minimum output voltage levels, several switching combinations can be used to produce similar output voltage level. In case $V_{cell,a1}=V_{cell,a2}=V_{dc}$, output voltage level V_{dc} can be achieved in two different ways; one is

² Consists of an energy storage unit and a DC-AC power converter.

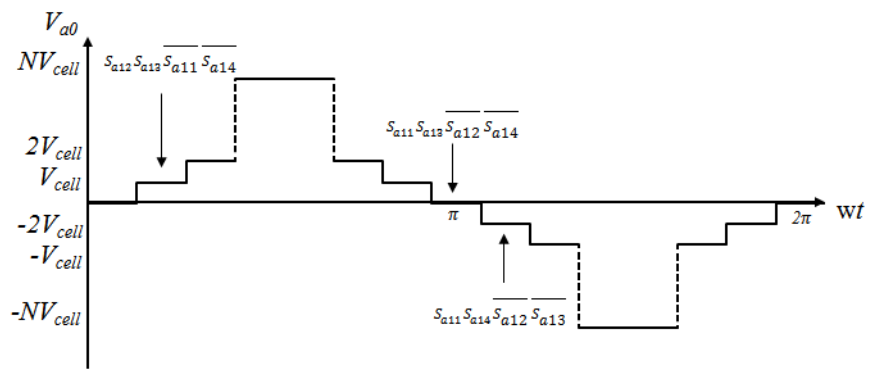
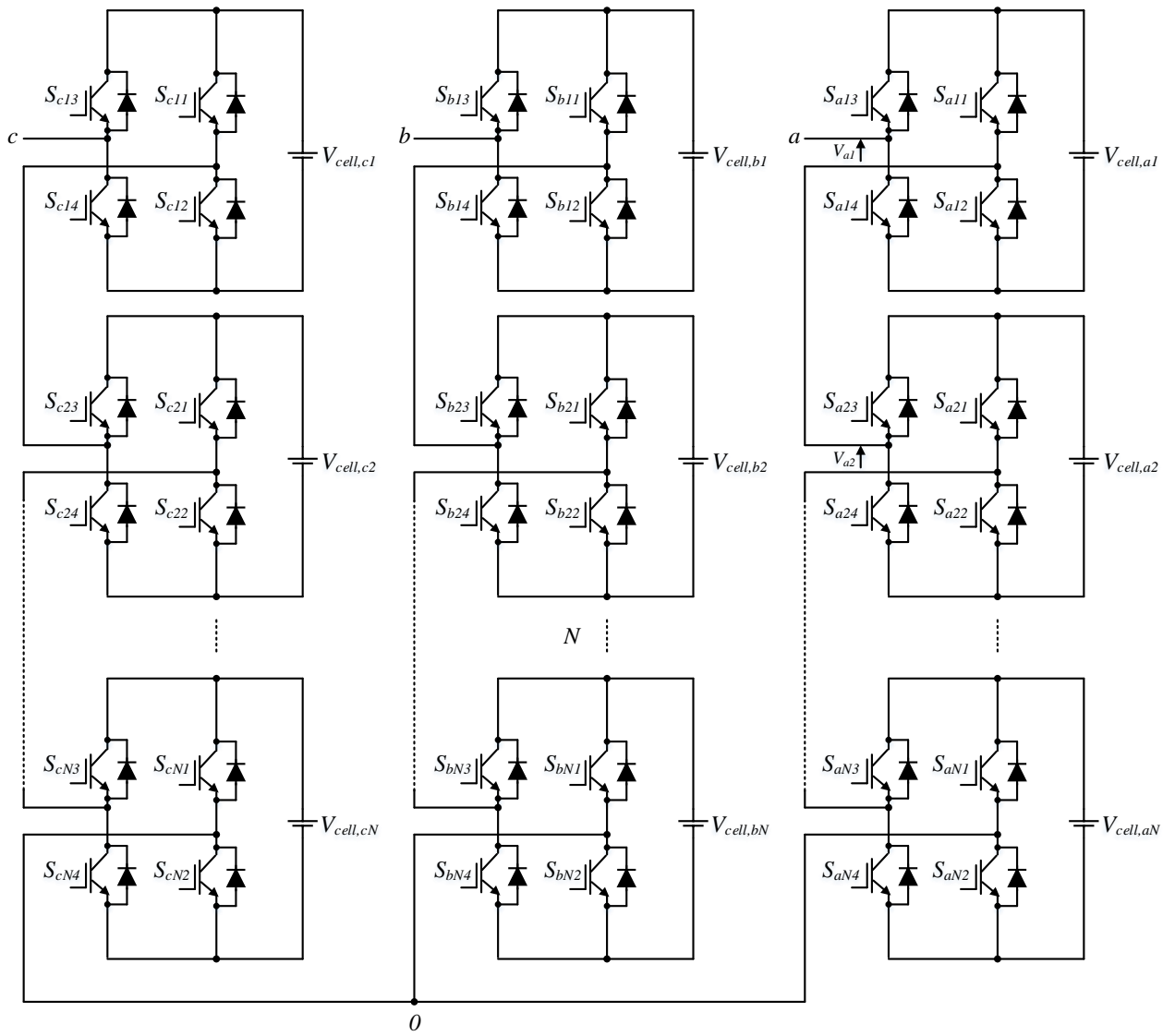


Figure 3.5 A three-phase MML converter with H-bridge topology

Table 3.2 Possible combinations of voltage levels and corresponding switching state of a five-level cascaded H-bridge multi-level converter

Phase voltage V_{a0}	Switching state					
	S_{a11}	S_{a13}	V_{a1}	S_{a21}	S_{a23}	V_{a2}
$2V_{dc}$ (No redundancy)	off	on	V_{dc}	off	on	V_{dc}
V_{dc} (3 redundancies)	off	on	V_{dc}	on	on	0
	off	on	V_{dc}	off	off	0
	on	on	0	off	on	V_{dc}
	off	off	0	off	on	V_{dc}
0 (5 redundancies)	on	on	0	on	on	0
	on	on	0	off	off	0
	off	off	0	on	on	0
	off	off	0	off	off	0
	off	on	V_{dc}	on	off	$-V_{dc}$
	on	off	$-V_{dc}$	off	on	V_{dc}
$-V_{dc}$ (3 redundancies)	on	off	$-V_{dc}$	off	off	0
	on	off	$-V_{dc}$	on	on	0
	on	on	0	on	off	$-V_{dc}$
	off	off	0	on	Off	$-V_{dc}$
$-2V_{dc}$ (No redundancy)	on	off	$-V_{dc}$	on	Off	$-V_{dc}$

to choose $V_{cell,a1} = V_{dc}$ and $V_{cell,a2} = 0$ (or $V_{cell,a1} = 0$ and $V_{cell,a2} = V_{dc}$). With more cell-converters, the converter output redundancy for the intermediate voltage levels is relatively increased. Figure 3.6 compares the harmonic content presents in the voltage waveform of 5-, 13- and 21-level of a cascaded H-bridge converter. It can be observed that a higher number level leads to a lower harmonic content. When the number of levels is high enough, harmonic content will be low enough to avoid the need of filters [318].

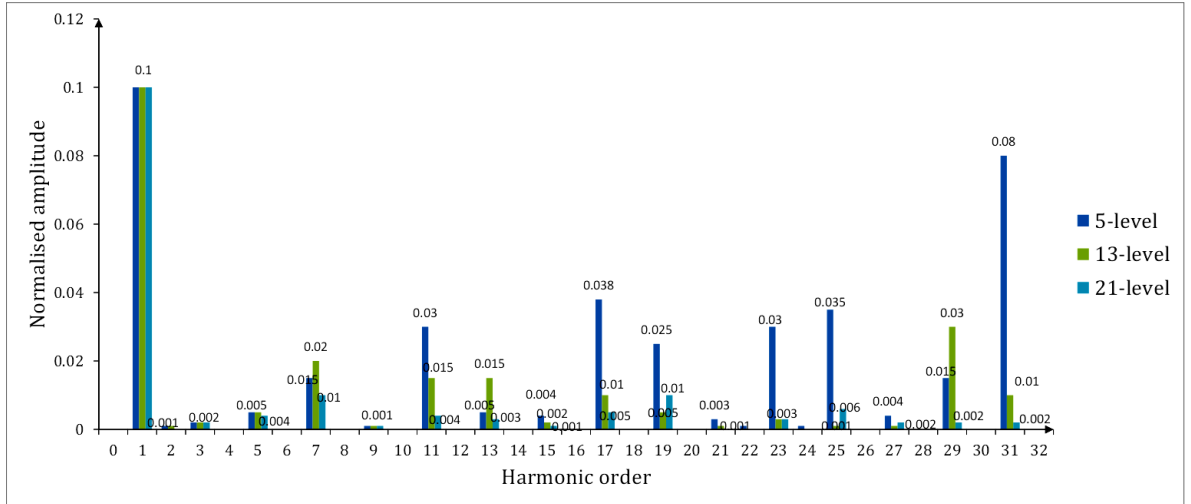


Figure 3.6 Harmonic content in 5-, 13- and 21-level of a cascaded H-bridge multi-level converter (adapted from [319])

In a three-phase MML half-bridge converter topology, each phase-leg is composed of two arms: upper arm and lower arm such that each arm comprises N_{SM} series-connected, nominally identical SMs and a series inductor L_{arm} [320-321]. Figure 3.7 shows the configuration of a three-phase MML half-bridge converter topology. Each SM can generate two voltage levels depending on the switching states of the complimentary switching pairs, i.e. S_1 and S_2 . When S_1 is on and S_2 is off, the SM is inserted into the circuit, thus, the voltage between the terminals, V_{SM} is equal to V_{cell} . When S_1 is off and S_2 is on, the SM is bypassed and the terminal voltage is zero [322].

By controlling the number of the SMs inserted and bypassed via switching states, a staircase voltage waveform can be synthesised at the AC terminals of the converter. The half-bridge circuit or chopper cell is favourable over the others due to the presence of only two power semiconductor devices in each SM which results in fewer components and lower power losses [323]. The MML converter was a major step forward in VSC technology for HVDC transmission with several advantages reported in [324-326].

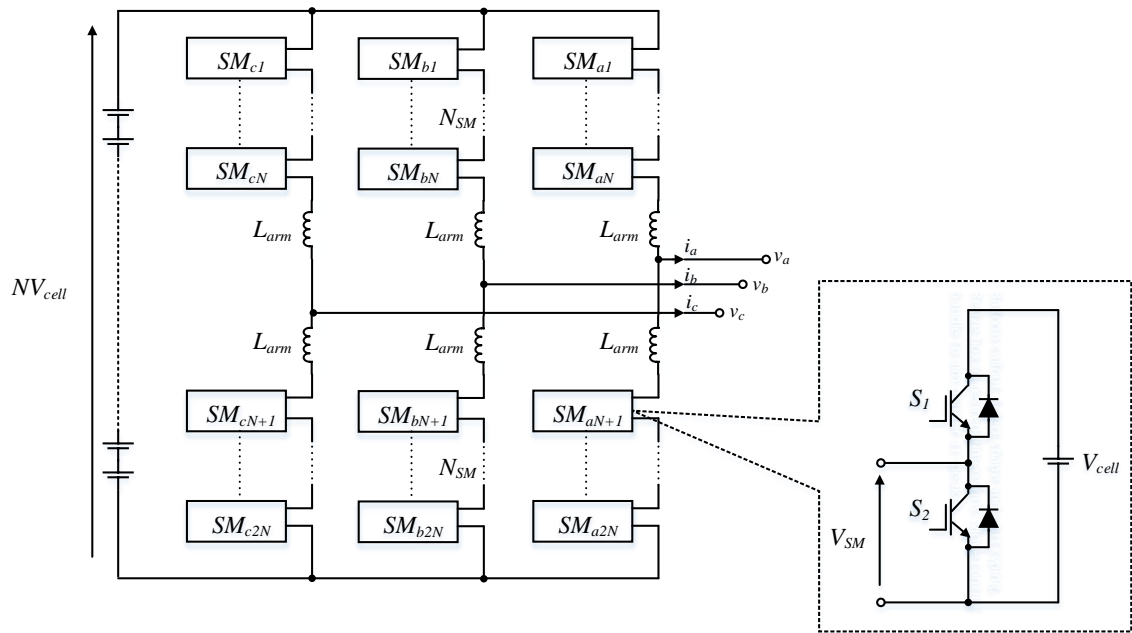


Figure 3.7 A three-phase MML converter with half-bridge topology

3.3.4 Comparison of Multi-level Converters

Table 3.3 compares the components needed by the four multi-level converters discussed above to achieve the same number of voltage levels. The comparison assumes the same voltage rating for all devices, but not necessarily the same current rating.

The diode-clamped converters, particularly the neutral-point clamped converter, have been extensively used in motor drive applications compared to the other two topologies. However, when the level exceeds three, excessive clamping diodes are required which increases the control complexity. The flying-capacitor converter uses floating capacitors to clamp the output voltage instead of diodes. Just like diode-clamped converters, the control becomes more complex for flying-capacitor converters with a higher number of voltage levels, as different triangular functions for individual power semiconductor device have to be arranged at different voltage levels [327].

The main advantage of a cascaded H-bridge converter over the diode-clamped converter and flying-capacitor converter is its modular structure; it is scalable up to a higher voltage and the voltage level determines the number of cell-converter needed. It needs less number of components compared to diode-clamped converter and flying-capacitor converter, thus, the weight and cost are less than those of the two converters. Since the total output phase voltage of a cascaded H-bridge converter is the summation of voltages produced by each H-bridge cell-converter, switching redundancy exists as described in Section 3.3.3. The main disadvantage of a cascaded H-bridge converter is that each H-bridge cell-converter requires an isolated DC source for real power conversions, thus, its application is limited [316]. Although it has an inherent self-balancing characteristic, a slight voltage imbalance can occur due to the circuit component losses and limited controller resolution. The second harmonic that presents on the cell current is potentially a threat to the health of a cell and may lead to higher losses at cell level [307].

The comparison between cascaded H-bridge and MML half-bridge topologies are discussed in [328-329]. It can be seen that the cascaded H-bridge converter requires the least number of components for a given number of levels as no extra clamping diodes or voltage balancing capacitor are needed. It is the most promising topology for utility interface such as grid-scale BESSs due to its modularity and flexibility of manufacturing. The number of voltage levels can be easily increased by inserting additional cell-converters [330-331].

Table 3.3 Comparison of components requirements per phase leg among three m -level converters (adapted from [318])

Topology	Diode-clamped	Flying-capacitor	Cascaded H-bridge	MML half-bridge
Main switching devices	$2(m - 1)$	$2(m - 1)$	$2(m - 1)$	$4(m - 1)$
Main anti-parallel diodes	$2(m - 1)$	$2(m - 1)$	$2(m - 1)$	$4(m - 1)$
Clamping diodes	$(m - 1)(m - 2)$	0	0	0
DC capacitors	$(m - 1)$	$(m - 1)$	$\frac{1}{2}(m - 1)$	$2(m - 1)$
Balancing capacitors	0	$\frac{1}{2}(m - 1)(m - 2)$	0	0
Smoothing inductors	0	0	0	2
Maximum number of levels	Any	Any	Odd only	Any
Modularity	Low	High	High	High
Design complexity	Low	Medium	High	High
Specific requirement	Clamping diodes	Additional capacitors	Isolated dc sources	Upper and lower arms

3.4 Emerging Multi-level Converters

Apart from the four basic topologies discussed earlier, combination or modification between them brings forth new converters in large variety. Emerging topologies like mixed-level multi-level converter, asymmetrical multi-level converter, and alternative arm modular multilevel converter are discussed.

Mixed-level multi-level converter first emerged to reduce the number of isolated DC sources required in high-voltage high-power applications. To synthesise a nine-level voltage waveform, it adopts a three-level diode-clamped or flying-capacitor converter to replace the H-bridge cell-converter in a cascaded H-bridge converter, the voltage level is

potentially doubled for each cell, thus, only two isolated DC sources are needed instead of four [332].

Instead of using an identical voltage level for every H-bridge cell-converter, the asymmetric multilevel converter employs a binary system to generate unique voltage levels among the H-bridge cell-converters by addition and subtraction of the H-bridge cell-converter voltages. This topology allows more levels to be generated in the output voltage, and thus reduces the harmonic content with less H-bridge cell-converters [333-335]. However, this topology loses modularity and it requires non-uniform cell design [336].

The alternate arm converter is a hybrid topology between the two-level converter, in the form of director switches in each arm, and the MML converter, because of the presence of H-bridge cell-converters. This converter is claimed to generate a multi-level AC voltage which is higher than the DC terminal voltage. Several advantages have been reported including the reduced number of cells per arm like in the two-level converter, and its capability to generate almost harmonic-free AC current, as does the MML topology. This topology has been validated in a component-level simulation of a 20 MW converter [337].

3.5 Power Conversion Systems (PCSs) in Grid-scale BESSs

The energy storage component of a BESS is essentially DC in nature. To effectively utilise the energy storage capacity on the utility grid, the energy must be converted to a standard AC level and regulated through a converter [184]. Generally, a BESS installation is composed of two main components: an energy storage unit and a PCS (or grid interface) [303] [338-339]. The focus of this work is on the PCS of a three-phase BESS, utilising a mature battery technology such as Li-ion or NiMh [340-342]. The PCS used in the modern

BESSs typically in the MW range, can be categorised into single-stage, multi-stage [343-344], and direct DC-AC conversion configurations as illustrated in Figure 3.8. Assuming that third harmonic injection is not used, the number of cells (N_s, N_m) or cell-converters (N) required for each topology is shown in Figure 3.9.

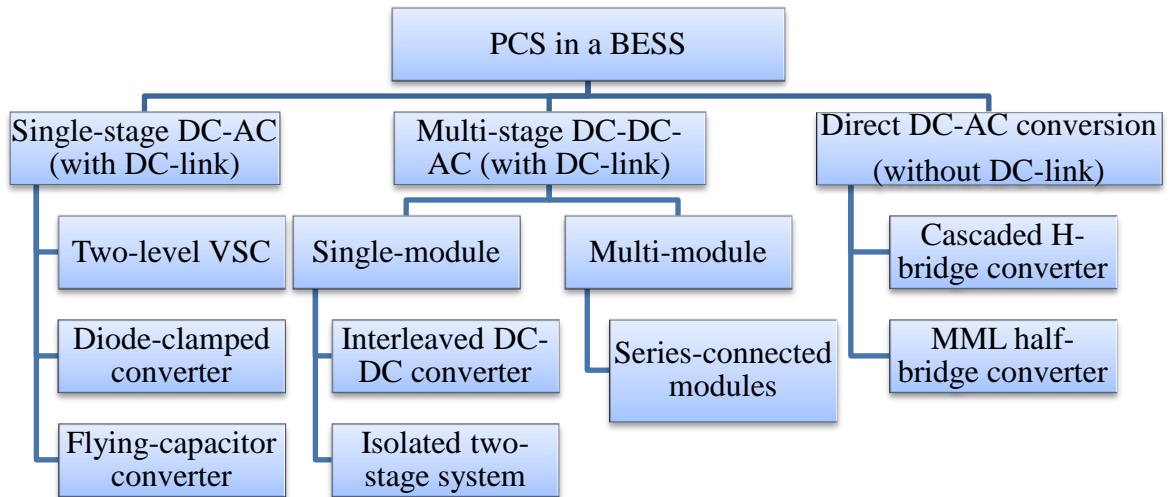
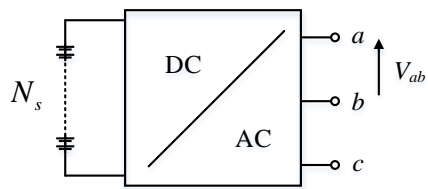
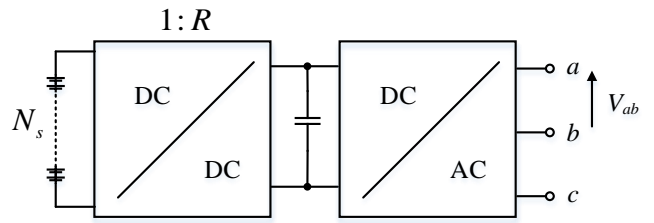


Figure 3.8 PCS in a BESS



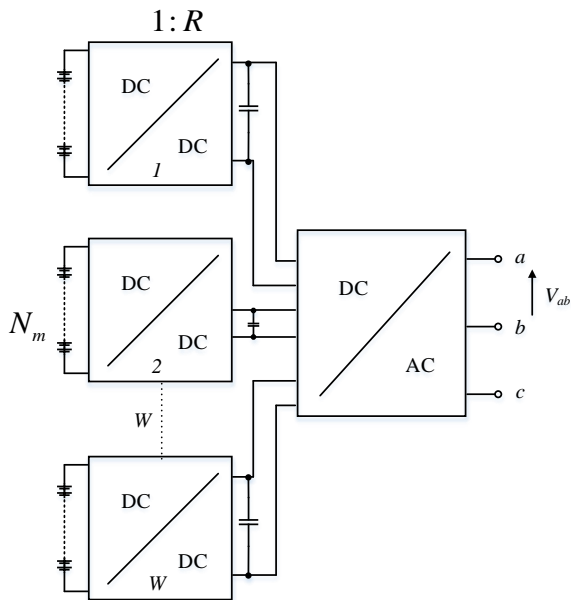
$$N_s \geq \frac{\sqrt{2}V_{ab}}{V_{cell}}$$

(a)



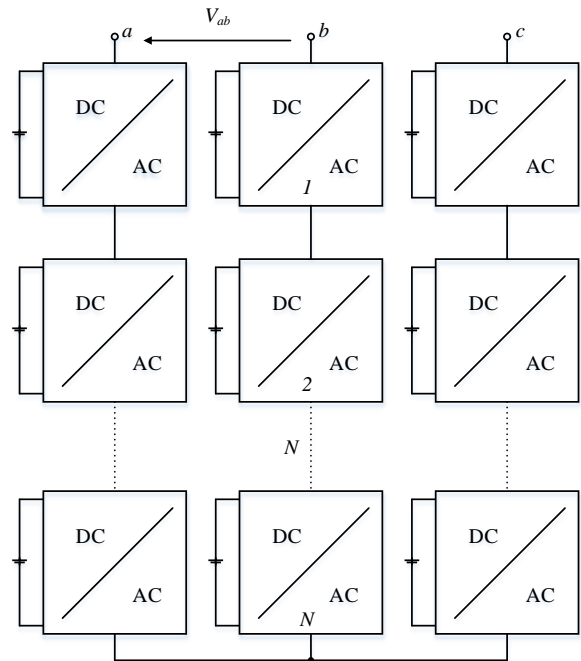
$$N_s \geq \frac{\sqrt{2}V_{ab}}{RV_{cell}}$$

(b)



$$N_m \geq \frac{\sqrt{2}V_{ab}}{WRV_{cell}}$$

(c)



$$N \geq \frac{\sqrt{2}V_{ab}}{\sqrt{3}V_{cell}}$$

(d)

Figure 3.9 Generalised BESS structure: (a) single-stage, (b) single-module, multi-stage, (c) multi-module, multi-stage and (d) direct DC-AC conversion

Single-stage systems are the most commonly used configuration where battery packs are integrated directly to the DC bus of an inverter [345], as illustrated in Figure 3.9(a). Though single-stage systems are simple, integrating a BESS directly on the inverter DC-link can negatively impact system efficiency, reliability, and cost [322]. Large amounts of energy delivery and repeated charging and discharging processes over time cause significant voltage variations within the battery pack. For instance, the charging voltage of a battery pack is approximately 50 % higher than the final discharging voltage [346]. The voltage stress on the VSC components can be very high. For a VSC to deliver power to the grid, the final discharging voltage should be no lower than the minimum DC-link voltage [347]. Hence, the VSC needs to be oversized to enable the required grid power transfer, i.e. the voltage rating is chosen based on the charging voltage of the BESS, which is considerably higher than the minimum required voltage, and thus increases the cost [348]. Examples of companies using this configuration are ABB and Parker SSD. The ABB DynaPeaQ employs a neutral-point clamped converter [349-352] as illustrated in Figure 3.10 whereas the Parker SSD employs a two-level VSC [353-354]. The DC bus in a neutral-point clamped converter, shown in Figure 3.10, is composed of a string of cells to achieve higher voltage level with clamping diodes connected at regular intervals [355-356]. Over 36000 individual cells, arranged in two parallel strings, are placed on the DC-link to provide an energy storage capacity of 5.36 MWh in the ABB DynaPeaQ [350]. The DC switches are included for isolating the battery packs from the DC side capacitors but still keeping neutral-point clamped converter in operation [357-361].

A multi-stage system can be divided into two categories: single-module (Figure 3.9(b)) and multi-module (Figure 3.9(c)). A single-module, multi-stage system consists of a

bi-directional DC-DC converter that feeds a grid-tied inverter stage. The DC-DC converter, shown in Figure 3.9(b) and Figure 3.9(c), decouples the battery packs from the DC-AC conversion, thus, maintaining a constant voltage independently from the battery packs' SoC to overcome the voltage variation issue in a single-stage system.

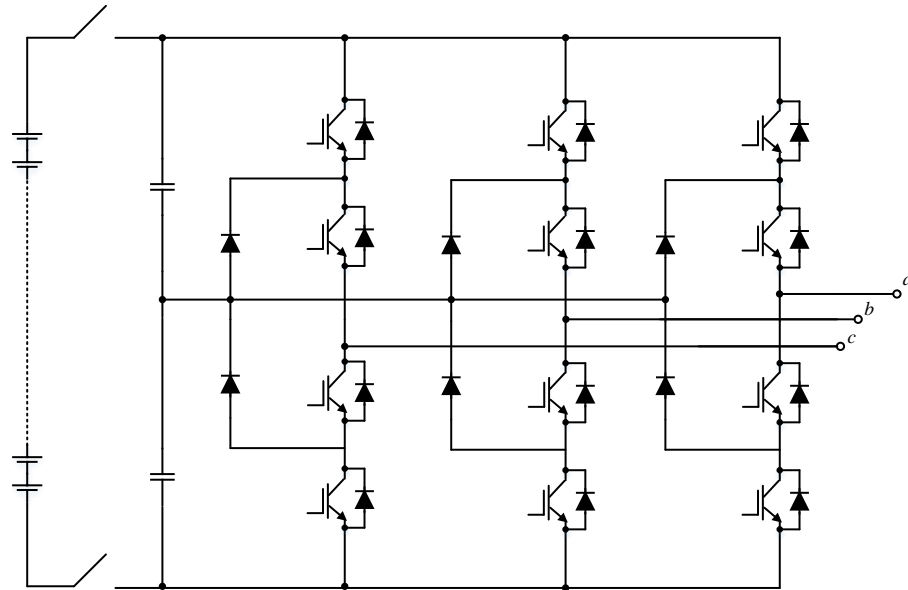
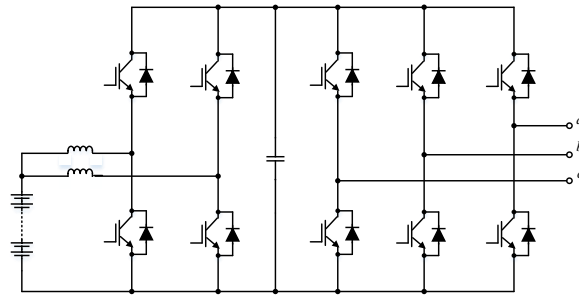


Figure 3.10 Single-stage: neutral-point clamped multi-level converter in ABB's DynaPeaQ [330]

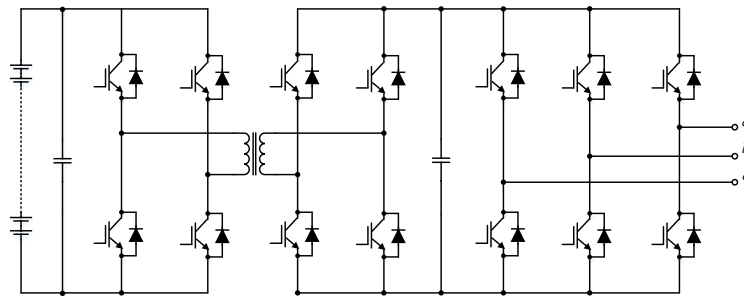
An example of single-module, multi-stage system is shown in Figure 3.11(a) from [147]. A boost DC-DC converter can be used to reduce the number of series-connected cells required in the battery packs. This topology has been applied by S&C Electric Company in several grid-scale BESSs [362-364]. A bidirectional DC-DC converter can be used instead to provide galvanic isolation, such a topology is studied in [365] and is shown in Figure 3.11(b). It serves the additional purpose to step the voltage up to a desired level. A multi-module, multi-stage system consists of W bi-directional DC-DC converter that feeds a grid-tied inverter stage. Figure 3.12 illustrates this topology where DC-DC converters are modularised into series-connected modules, each with its own battery packs

[366-367]. Compared to single-stage system, the conversion efficiency is reduced due to the losses in the DC-DC converter.

In a direct DC-AC conversion system shown in Figure 3.9 (d), it introduces a high degree of modularity to interface a BESS to medium or high voltage grid. It is well scalable and flexible to a wide range of operating voltage, energy storage capacity, and output power [368-371]. With modular construction and controllable SMs, a direct DC-AC conversion system allows the shift of centralised stored energy from the conventional main DC-link to several distributed DC-links, each with a lower voltage rating [372-373]. It has high efficiency conversion due to direct coupling to the grid. Nonetheless, since each H-bridge cell-converter is controlled independently, there is an inherent power imbalance between the cells, which poses a hazard for the converter if the voltage limits of the cells are exceeded [374-375]. To reach higher capacity for grid-scale BESSs, a three-phase configuration is required. However, this configuration leads to another issue, which is the inherent imbalance between the three phases.



(a)



(b)

Figure 3.11 Single-module, multi-stage (a) interleaved DC-DC converter: simplified diagram of S & C’s PureWave storage management system [376], (b) isolated system

In a standard MML converter, each SM consists of a half-bridge and a long string of cells [377-379]. To demonstrate the modularity of the converter, cells can be connected to each SM as illustrated in Figure 3.13(a). DC-DC converter decouples the battery packs from the DC-link, it also enables the control of DC cell current and thus reduces the power losses at cell level. Depending on the control scheme, the DC current provided by DC-DC converter varies from a smooth DC current to a stepped DC current.

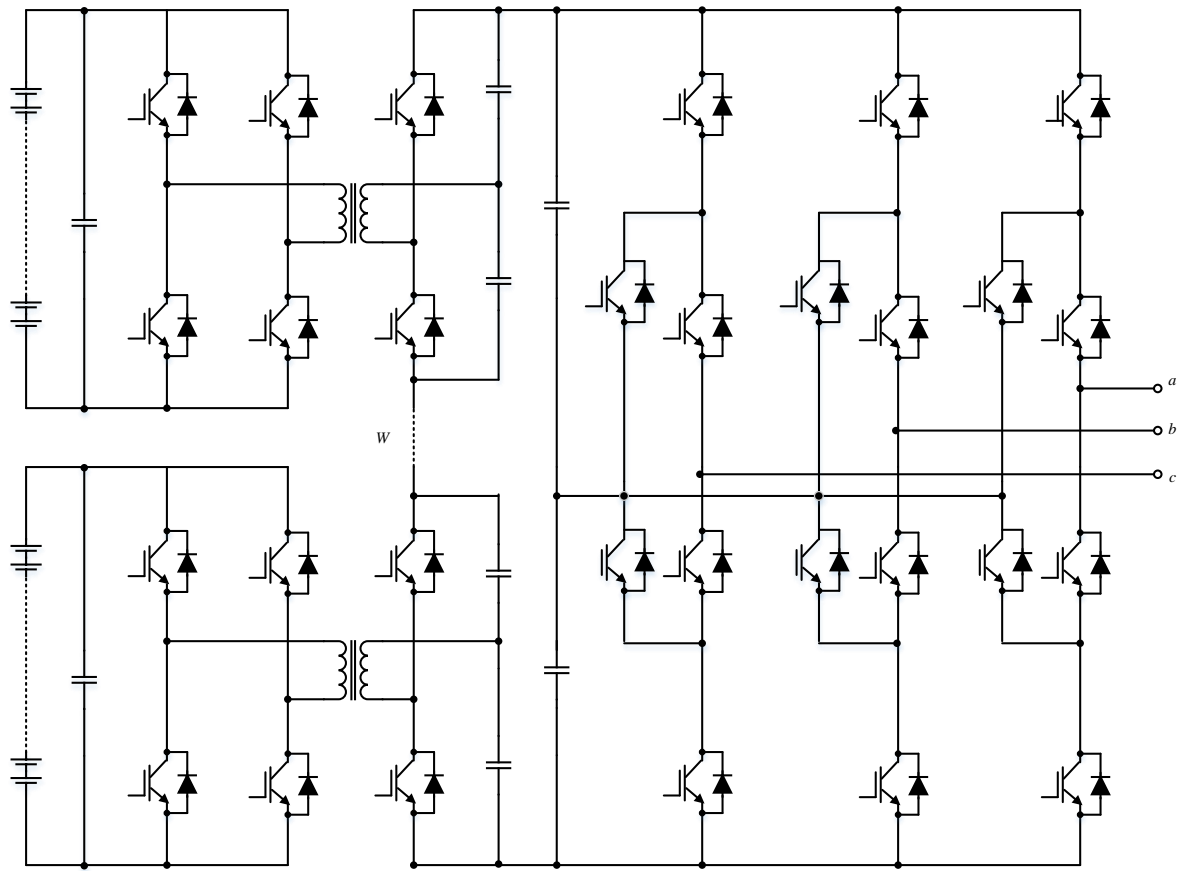


Figure 3.12 Multi-module, multi-stage: series-connected modules of isolated system

Figure 3.13(b) shows two ways to integrate battery packs using a cascaded H-bridge converter; by either connecting battery packs directly to the H-bridge or interfaced through a DC–DC converter [378]. The former appears preferable and has gained the most interest for BESSs [380-381] and electric drives [297]. Altair Nanotechnologies has published a white paper demonstrating an experimental cascaded H-bridge converter for use in a BESS [382].

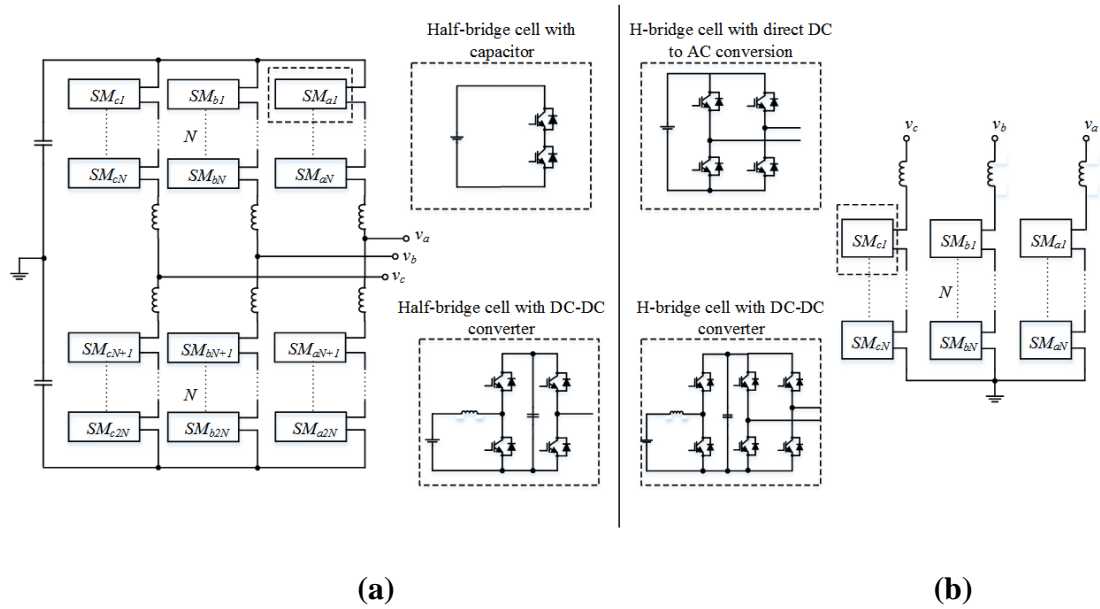


Figure 3.13 Multi-level stage (a) MML half-bridge converter, (b) Cascaded H-bridge converter

Use of single-stage or multi-stage converters described in this section for battery integration is simple as it integrates BESS directly on the DC-link of an inverter, yet it presents challenges in performance, safety, cost and reliability. A key problem with such configuration in BESSs is the potential for poor utilisation of mismatched cells and reliability issues resulting from the use of large series strings of cells as well as limited efficiency of two-level converter systems. Taking, for example, the existing BESS in [349-350], large strings of cells are composed of modularised battery packs with each module consists of a short string of cells. However, the PCS is not modularised. Therefore, this system configuration is susceptible to reliability issues as no mechanism exists to address the failure of individual cell. If a single cell fails or exceeds its operating limits (overcharging or deep discharging), an entire string must be disconnected for service, thus, half the energy storage capacity is lost.

Moreover, it is not clear that the battery packs in the existing BESSs can be viably scaled by the necessary one or two orders of magnitude due to the increasing challenges associated with cell balancing. In addition, simple two- or three-level PWM inverters become increasingly challenging to implement as connection voltage is increased due to the requirement to connect many semiconductor switching devices in series. These deficiencies potentially impede Li-ion technology from being used extensively in a large BESS. The cascaded H-bridge converter is an ideal candidate for BESSs due to several advantages [296]. To reduce the nominal voltage of the cell, the number of series-connected cells can be distributed in a number of cell-converters making use of the cascaded H-bridge multi-level converter. This will keep the possibility of MV converter output, while using low voltage cells. In study [367], this topology has proven to achieve the highest power electronic efficiencies in combination with low costs of the power electronic converter. In the event of cell failure, additional modules can be inserted, and only a single module is taken out for service rather than a string of cells connected to the DC-link. For this reason, it is suggested that a MML converter composed of series-connected H-bridge units that address the limitation of power semiconductor devices voltages whilst also providing opportunities for cell balancing holds great promise [318].

CHAPTER 4 BALANCING CONTROL USING A HIERARCHICAL STRUCTURE

This chapter describes the balancing control for a grid-scale BESS; cells are organised in a hierarchical structure consisting of modules, sub-banks, banks and phases. The control strategy includes five levels of balancing: balancing of cells within a module, balancing of modules within a sub-bank, sub-banks within a bank, banks in a phase and balancing between phases. The system is validated in simulation for a 380 kWh BESS using 2835 Li-ion cells.

4.1 Cell Organisation in a Hierarchical Arrangement

In a 100 MWh grid-scale BESS described in Section 2.6, it can be estimated that around 300000 cells are required and this involves a huge number of sensing and control signals. An attempt to implement a practical BESS using cascaded-H-bridge multi-level converter circuit which are all directly operated by a centralised control system structure will rapidly become cumbersome. Thus, a hierarchical arrangement of cells and control functions becomes a necessity.

In this work, cells are sub-divided into a hierarchy consisting of modules, sub-banks, banks and phase ‘layers’ as illustrated in Figure 4.1. Control and sensing is mostly contained within each layer and only limited information is transferred between layers. The hierarchical design allows conceptually simple scale-up of the overall BESS and greatly simplifies the control challenge when compared to a flat (non-hierarchical) structure. Figure 4.1 demonstrates the underlying electrical circuit and hierarchical arrangement employed in this work: $N = 35$ cells are grouped in a module; $M = 3$ modules in a sub-bank; $K = 3$ sub-banks in a bank and $J = 3$ banks in a single phase. The system studied here therefore

contains $3NMKJ = 2835$ cells. This structure is intended to allow scale-up to even larger number of cells by increasing N, M, K and J and/or by adding additional layers in the hierarchy (e.g. by introducing a sub-sub-bank layer).

4.2 Circuit Configuration

In Figure 4.1, each H-bridge block of the cascaded-H-bridge multi-level converter contains a single Li-ion cell and four metal-oxide-semiconductor field-effect transistors (MOSFETs) which enable full control of cell connection, independent of every other cell within the system. Each H-bridge block is capable of producing three output voltage levels: 0 if Q1A and Q1B are on, $+V_{cell}$ if Q1A and Q1B' are on, and $-V_{cell}$ if Q1A' and Q1B are on (remaining MOSFETs are off in each case). The output voltage of the cascaded-H-bridge multi-level converter is the sum of the voltages that are generated by each cell. The number of output voltage levels is $2N + 1$, where N is the number of cells and a y level cascaded-H-bridge multi-level converter needs $2(y - 1)$ switching devices (MOSFETs). Cells are dynamically configured in series during operation to achieve the desired output voltage level. As there are over 900 cells in each phase, the system is capable of producing an output voltage very close to a smooth sinusoidal voltage at the grid connection point. Additional monitoring, control, over/under voltage and current protection, as well as thermal monitoring and fault detection can be added to each H-bridge block to produce an overall control and monitoring system for the BESS.

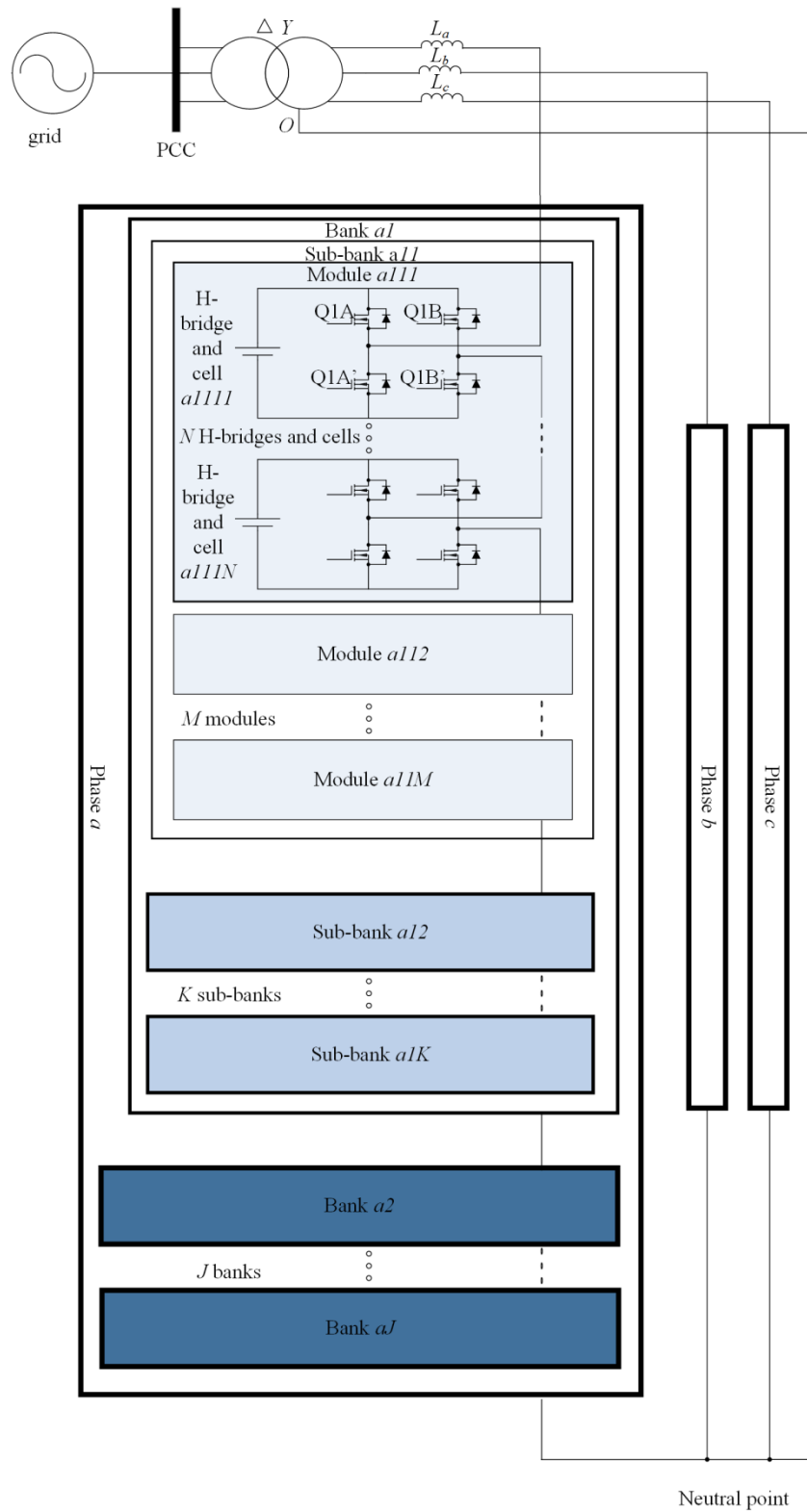


Figure 4.1 Electrical hierarchical arrangement of the proposed BESS: cells, modules, sub-banks, banks and three phases

4.3 System Overview

Figure 4.2 gives a high-level overview of the BESS control system and its connection to the grid. Li-ion cells are electrically interfaced to the grid by the cascaded-H-bridge multi-level converter power electronic circuit. The switching signals for the MOSFETs in each cascaded-H-bridge multi-level converter are generated by a balancing controller, which receives a reference voltage from a power controller and a zero-sequence voltage injection block. The balancing controller uses cell SoC and cell voltage to choose which cells are active at any particular instant in time.

In this work, the balancing controller implements four ‘levels’ of balancing: between cells within a module, between modules within a sub-bank, between sub-banks within a bank, and between banks in a phase. The power controller is a conventional closed-loop VSC control scheme implemented in the direct-quadrature (dq) reference frame that separately controls the active power and reactive power exchanged with the grid [383]. The dq reference frame will be discussed in Section 4.4. To achieve power balancing between phases, a zero-sequence voltage component is added to the reference voltage signal generated by the power controller. This enables active power exchange between phases which implements the fifth level of balancing (phases within the BESS) whilst maintaining a balanced three-phase voltage at the grid interface. Together these three sub-systems (balancing controller, power controller and zero-sequence injection block) form the complete control system for the proposed BESS. The simulation model implemented in MATLAB Simulink can be found in Appendix A.

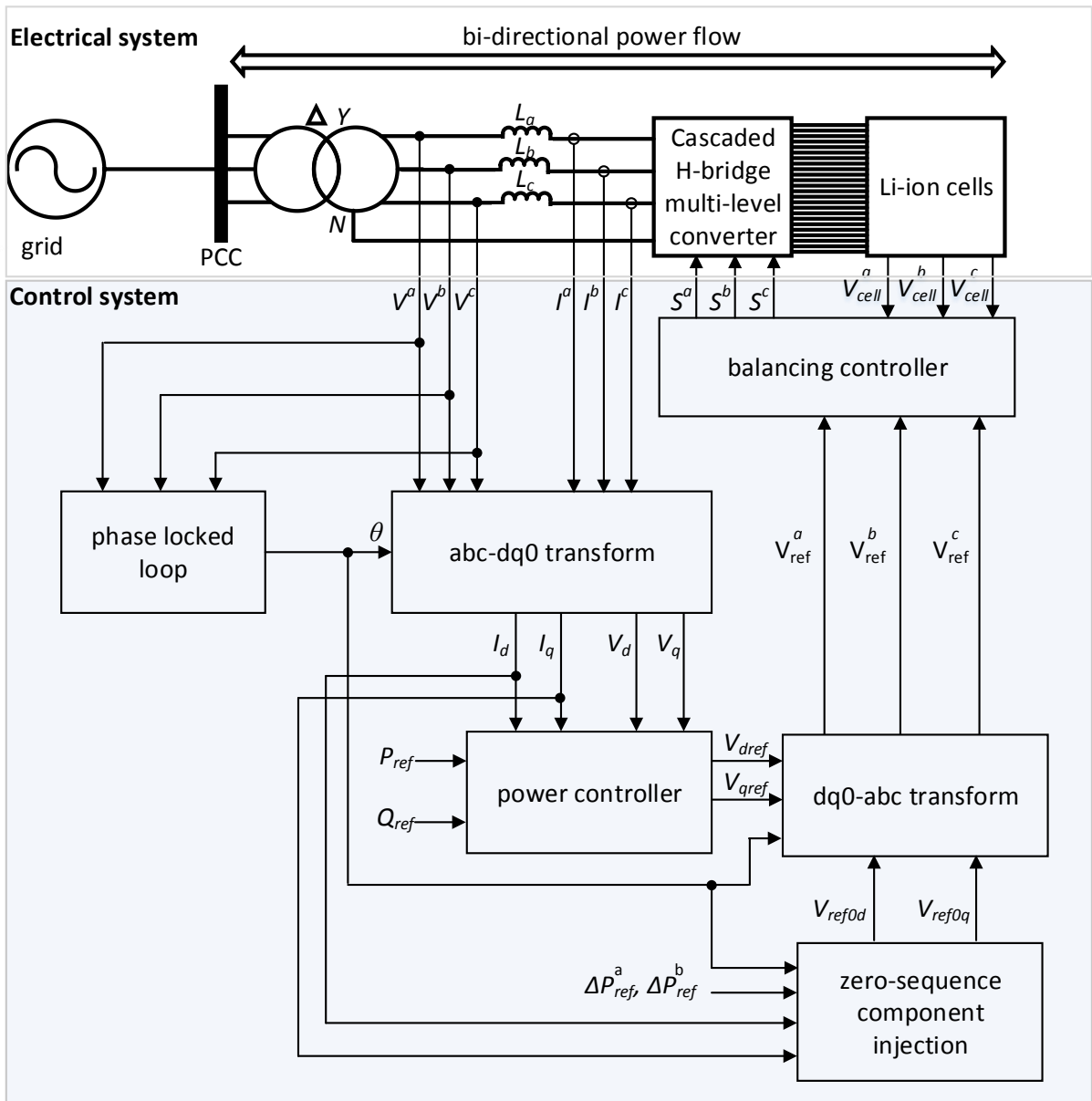


Figure 4.2 System overview showing electrical and control system interconnections

4.4 Control System of VSC

Synchronous reference frame control, also known as direct-quadrature (*dq*), uses reference frame transformation *abc* to *dq* to transform grid voltage and current into a reference frame that rotates synchronously with the grid voltage (see Appendix B). The

frame is synchronised with the electrical angular velocity ω , thus, the resulting d and q components are coupled in the VSCs [384-390]. By means of this, grid voltage and current become DC quantities as the number of required control loops is reduced from three to two and all the control variables are DC quantities under steady-state conditions, thus, no tracking error exists when using a proportional-integral (PI) controller to regulate the AC input current, thereby, control and filtering can be achieved relatively easily [391]. It is widely used in the control of electrical machines and grid-connected converters [385-386].

In this work, the grid voltages and currents are first transformed to the dq frame for active and reactive power control using PI controllers, which provides the reference voltages in the dq frame. The reference voltages are transformed back to abc frame to be fed to the VSC. The control system relies on an accurate estimation of grid phase angle, thus, phase-locked-loop (PLL) is employed to extract phase angle of the grid voltage for grid synchronisation where the controlled current must be in phase with the grid voltage [392-393].

The control system of VSC consists of a fast inner current control loop and an outer control loop. Active and reactive power are regulated in the outer control loop using the phase and amplitude of the VSC line currents with respect to the point of common coupling (PCC) voltage. The outer control loop regulates the bi-directional power transfer between the AC grid and DC system. The inner current control loop is employed for fast tracking of reference signals provided by the outer control loop [394].

4.4.1 Phase-locked-loop (PLL)

An accurate detection of grid angle and frequency is essential to ensure a proper generation of reference signal in a grid-tied VSC, and to be able to inject/draw desired currents. Thus, a PLL is required to track the grid angle, θ and the electrical angular velocity, ω for synchronisation, where θ is needed for abc to dq transformation module in Park transformation (see Appendix B) while ω is used to monitor grid condition to ensure its compliance with the control requirements [395].

PLL is a closed-loop frequency-control system based on the phase difference between an actual input signal and an internal generated signal. The phase difference is filtered by a PI controller and is used to reconstruct the signal. The fundamental idea is to automatically adjust the phase of the generated signal to match the phase of the actual input signal. For example, ω is decreased if current lags grid voltage until the current is in phase with the grid voltage; ω is increased if the current leads the grid voltage until they are in phase [396].

Figure 4.3 depicts a basic PLL configuration. Grid voltages, V^{ga} , V^{gb} and V^{gc} are transformed into vectors in the dq frame by means of Park transformation and so, V_{gqref} serves as input to the PLL. The feed-forward controller includes a PI controller and an integrator. With V_{gqref} set as zero, a PI controller is used to adjust θ so that the phase angle error is reduced to zero, resulting in V_{gq} equal to zero in steady state. Thus, V_{gd} denotes the amplitude of a balanced three-phase voltage. The output of the controller corresponds to ω , in which it is integrated to yield θ . θ is fed back into the abc to dq transformation module for both voltage and current and are used in the control loops as part of the decoupling terms. It is used in PI controller for adaptive tuning in respect to the grid frequency where it

is designed to have minimum overshoot [397]. Loop filter controls the oscillation frequency of a voltage-controlled oscillator (VCO) based on the voltages proportional to the error signal and time integral of the error signal respectively. Parameters are chosen to trade off a fast dynamic response providing quick synchronisation against a slow system providing filtered output. Careful selection of parameters in the PI controller is important as they have significant effects on the PLL dynamic performance and lock quality [398-399].

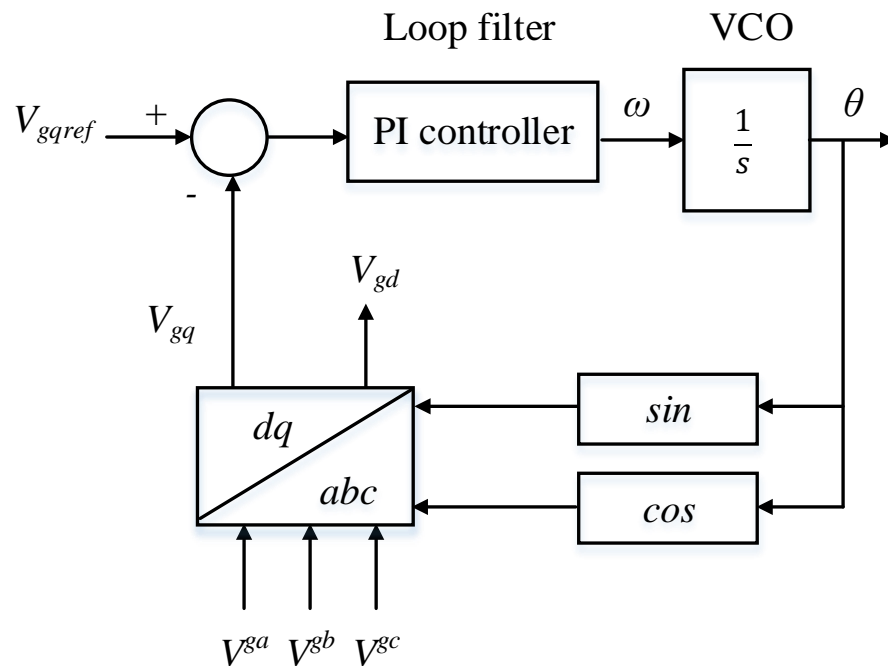


Figure 4.3 PLL block diagram

4.4.2 Inner Current Control Loop

Current control is achieved using an inner current control loop that determines the necessary voltage drop over the series reactance (the total resistance and inductance between the VSC and the PCC with the AC grid) to generate the required AC current without exceeding the VSC rating. Phase current is measured and the voltage drop across

inductor is controlled to force the phase current to track its reference value, in which the reference value is provided by outer control loop described later.

All system parameters such as three-phase voltage and converter currents are transformed into the dq frame, which will be synchronised with the AC grid through PLL. The control system will determine the reference voltage in dq frame, V_{dref} and V_{qref} , which are then be transformed back to the three-phase abc frame before being fed to the balancing controller shown in Figure 4.2. The reference currents, I_{dref} and I_{qref} that are required to generate the desired V_{dref} and V_{qref} , can be obtained from outer control loop. Considering a grid-tied VSC equivalent circuit illustrated in Figure 4.4, the following equations describe the dynamics of the AC side of the VSC:

$$\begin{cases} L \frac{dI}{dt} = -RI + V - V^g \\ V^a = L \frac{dI^a}{dt} + RI^a + V^{ga} \\ V^b = L \frac{dI^b}{dt} + RI^b + V^{gb} \\ V^c = L \frac{dI^c}{dt} + RI^c + V^{gc} \end{cases} \quad (4.1)$$

or in matrix form,

$$\frac{d}{dt} \begin{bmatrix} I^a \\ I^b \\ I^c \end{bmatrix} = \frac{1}{L} \begin{bmatrix} V^a \\ V^b \\ V^c \end{bmatrix} - \frac{R}{L} \begin{bmatrix} I^a \\ I^b \\ I^c \end{bmatrix} - \frac{1}{L} \begin{bmatrix} V^{ga} \\ V^{gb} \\ V^{gc} \end{bmatrix} \quad (4.2)$$

where R and L are, respectively, the total resistance and inductance between VSC and PCC with the AC grid, V^{ga} , V^{gb} and V^{gc} are three-phase instantaneous grid voltages in abc frame, V^a , V^b and V^c are the three-phase instantaneous VSC voltages in abc frame, I^a , I^b and I^c are the three-phase instantaneous currents in abc frame.

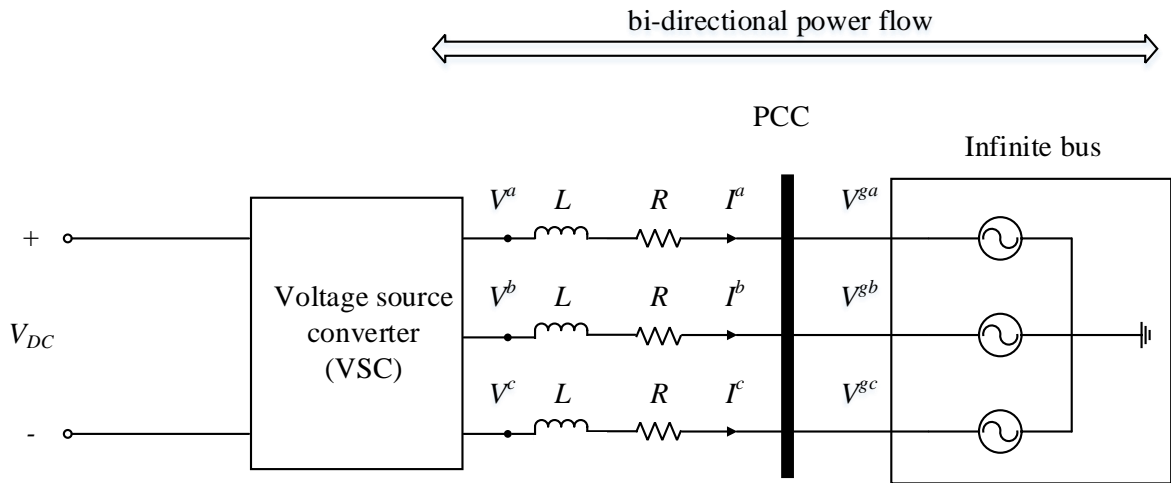


Figure 4.4 Grid-tied VSC equivalent circuit

Applying Park transformation, the space vectors that represent the electrical quantities in the VSC are projected on d and q axes. For a space vector rotating at the same speed as the synchronous dq frame, d and q components will remain constant, otherwise, the components will have a time-variable magnitude. There exists a cross-coupling between d and q components of voltages and currents, which can affect dynamics performance of the PI controller and should be decoupled and controlled independently [400-401].

Figure 4.5 illustrates the implementation of inner current control loop according to (4.3), consisting of three terms: filter dynamics, decoupling and feed-forward term. PI controller is used where the tracking signals are DC quantities; filter dynamics are represented by proportional gain, $K_{p,i}$ and integral gain, $K_{i,i}$. The current decoupling and voltage feed-forward terms are introduced to improve system performance by eliminating the effect of steady-state voltage across L [402]. The tuning of PI controllers can be performed in one loop since both d and q have same dynamics. The inner current control loop is designed to have fast reference tracking.

$$\begin{cases} \frac{d}{dt} \begin{bmatrix} I_d \\ I_q \end{bmatrix} = \frac{1}{L} \begin{bmatrix} V_d \\ V_q \end{bmatrix} - \frac{R}{L} \begin{bmatrix} I_d \\ I_q \end{bmatrix} - \frac{1}{L} \begin{bmatrix} V_{gd} \\ V_{gq} \end{bmatrix} + \omega \begin{bmatrix} I_q \\ -I_d \end{bmatrix} \\ \begin{bmatrix} V_d \\ V_q \end{bmatrix} = \underbrace{R \begin{bmatrix} I_d \\ I_q \end{bmatrix}}_{\text{filter dynamics}} + L \frac{d}{dt} \begin{bmatrix} I_d \\ I_q \end{bmatrix} + \underbrace{\omega L \begin{bmatrix} I_q \\ -I_d \end{bmatrix}}_{\text{decoupling}} + \underbrace{\begin{bmatrix} V_{gd} \\ V_{gq} \end{bmatrix}}_{\text{feed-forward term}} \end{cases} \quad (4.3)$$

By controlling I_d and I_q independently, the desired converter voltage, V_{dref} and V_{qref} can be generated to regulate the active and reactive power flow in the system. The reference values of the AC-side voltages can therefore be described by the following equation:

$$\begin{bmatrix} V_{dref} \\ V_{qref} \end{bmatrix} = R \begin{bmatrix} I_d \\ I_q \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} I_d \\ I_q \end{bmatrix} + \omega L \begin{bmatrix} I_q \\ -I_d \end{bmatrix} + \begin{bmatrix} V_{gd} \\ V_{gq} \end{bmatrix} \quad (4.4)$$

The total output of the inner current control loop, $V_{dref} + jV_{qref}$ represents the voltage across the AC grid and AC inductor, which is equivalent to the AC terminal voltage of the VSC [403]. The total output of V_{dref} and V_{qref} are transformed to the three-phase reference voltage, V_{ref}^a , V_{ref}^b and V_{ref}^c shown in Figure 4.1 by applying the dq to abc transformation.

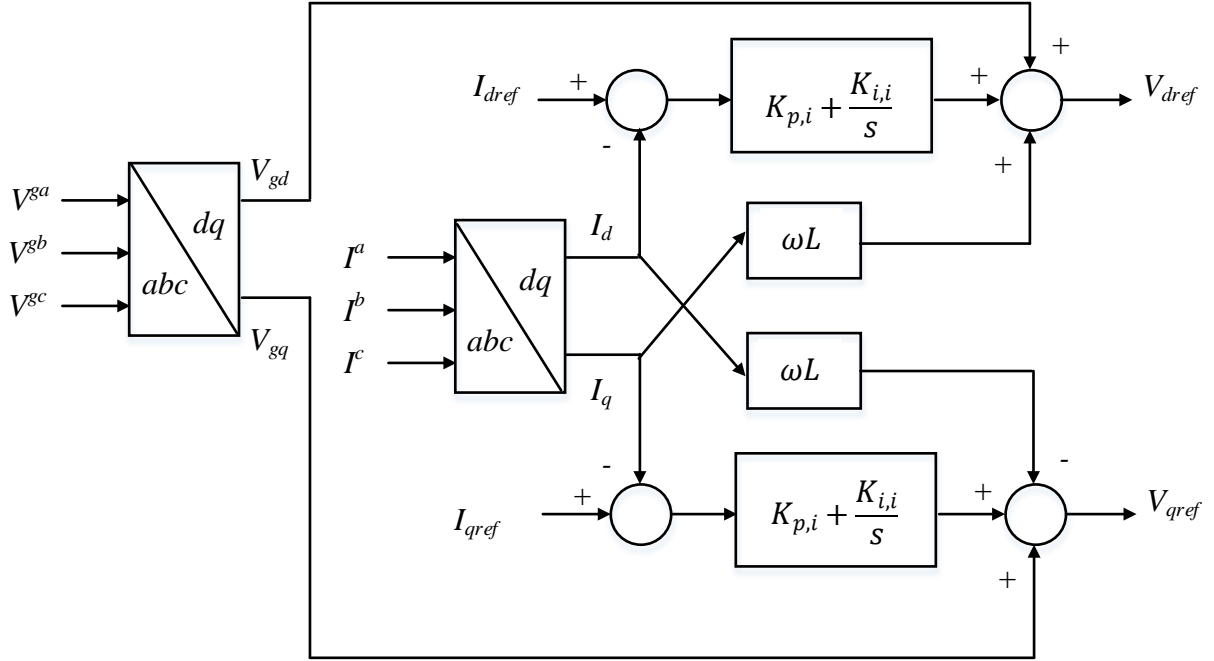


Figure 4.5 Block diagram of inner current control loop

4.4.3 Outer Control Loop

The outer control loop generates reference currents, I_{dref} and I_{qref} which serve as inputs to the inner current control loop. Two controllers are required: the active power controller provides I_{dref} while the reactive power controller provides I_{qref} . In each controller, a PI controller is employed to eliminate steady state errors. The active and reactive power can be calculated based on instantaneous power theory [389]:

$$Re\{\mathbf{V}_s(\mathbf{I}_s)^*\} = Re\{\mathbf{V}_{gdq}(\mathbf{I}_{dq})^*\} \quad (4.5)$$

From the space vector defined in (B.2) (see Appendix B), the power at the PCC in the abc frame can be calculated as follows:

$$\left\{ \begin{array}{l} \mathbf{V}_s(\mathbf{I}_s)^* = \left(\frac{2}{3}K\right)^2 \left(V^{ga} + V^{gb}e^{j\frac{2\pi}{3}} + V^{gc}e^{j\frac{4\pi}{3}}\right) \left(I^a + I^be^{j\frac{2\pi}{3}} + I^ce^{j\frac{4\pi}{3}}\right)^* \\ \mathbf{V}_s(\mathbf{I}_s)^* = \left(\frac{2}{3}K\right)^2 \left(V^{ga}I^a + V^{gb}I^b + V^{gc}I^c + j\frac{1}{\sqrt{3}}[V^{ga}(I^c - I^b) + V^{gb}(I^a - I^c) + V^{gc}(I^b - I^a)]\right) \end{array} \right. \quad (4.6)$$

Assuming a balanced three-phase system, Park transformation is applied to conserve power from the abc to dq frame, the real part indicates the active power while the imaginary part indicates the reactive power:

$$\left\{ \begin{array}{l} P = \frac{3}{2K^2} \operatorname{Re}\{\mathbf{V}_s(\mathbf{I}_s)^*\} = \frac{3}{2K^2} \operatorname{Re}\{\mathbf{V}_{gdq}(\mathbf{I}_{dq})^*\} = V^{ga}I^a + V^{gb}I^b + V^{gc}I^c \\ P = \frac{3}{2}[V_{gd}I_d + V_{gq}I_q] \\ Q = \frac{3}{2K^2} \operatorname{Im}\{\mathbf{V}_s(\mathbf{I}_s)^*\} = \frac{3}{2K^2} \operatorname{Im}\{\mathbf{V}_{gdq}(\mathbf{I}_{dq})^*\} = \frac{1}{\sqrt{3}}[V^{ga}(I^c - I^b) + V^{gb}(I^a - I^c) + V^{gc}(I^b - I^a)] \\ Q = \frac{3}{2}[V_{gq}I_d - V_{gd}I_q] \end{array} \right. \quad (4.7)$$

The amplitude of the transformed grid voltage can be obtained from (4.8), with an arbitrary phase shift, γ obtained from (4.9).

$$|V_g| = \sqrt{V_{gd}^2 + V_{gq}^2} \quad (4.8)$$

$$\gamma = \tan^{-1} \frac{V_{gd}}{V_{gq}} \quad (4.9)$$

Any arbitrarily rotating frame can be chosen as the reference frame. PLL synchronisation described in Section 4.4.1 ensures that the d component, V_{gd} is aligned with the AC grid voltage vector where it represents the magnitude of the grid voltage at the PCC. Consequently, the q component, V_{gq} is always equal to zero. Thus, the instantaneous power flow can be simplified in (4.10).

$$\begin{cases} P = \frac{3}{2}V_{gd}I_d \\ Q = -\frac{3}{2}V_{gd}I_q \end{cases} \quad (4.10)$$

As described in Section 4.4.2, I_d and I_q can be controlled independently in order to regulate the amount of active and reactive power flow in the system. The d component and q component of reference current, I_{dref} and I_{qref} are given by (4.11). The block diagram of the outer control loop is illustrated in Figure 4.6. The outer control loop is implemented in a close-loop manner to allow precise tracking of power references. Active power reference, P_{ref} is set to charge or discharge the battery pack depending on the system requirement. The generated I_{dref} and I_{qref} have to be limited to VSC ratings.

$$\begin{cases} I_{dref} = \frac{2P_{ref}}{3V_{gd}} \\ I_{qref} = -\frac{2Q_{ref}}{3V_{gq}} \end{cases} \quad (4.11)$$

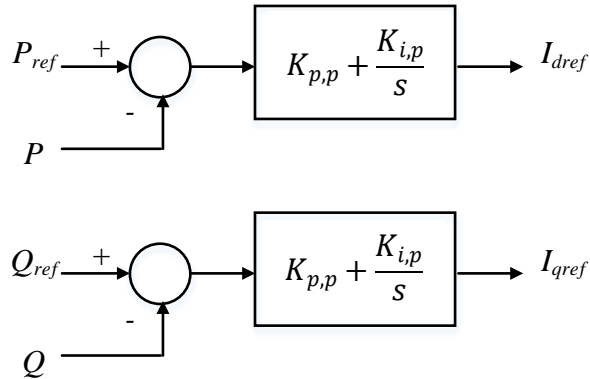


Figure 4.6 Block diagram of outer control loop

The performance of the VSC control system (i.e. inner current controller and outer controllers) is evaluated. Figure 4.7 indicates a fast response system where the bi-directional power flow is achieved by controlling the active and reactive power independently: from the AC grid to the battery pack, and vice versa. In order to test the

dynamic response of the VSC control system, changes in active and reactive power reference are made as shown in Figure 4.8. Active and reactive power are controlled at -60 kW and $+51$ kVar respectively before $t = 3$ s, and are changed to $+60$ kW and -51 kVar respectively at $t = 3$ s. Both the measured active and reactive power (P and Q) reach the new references after the transient.

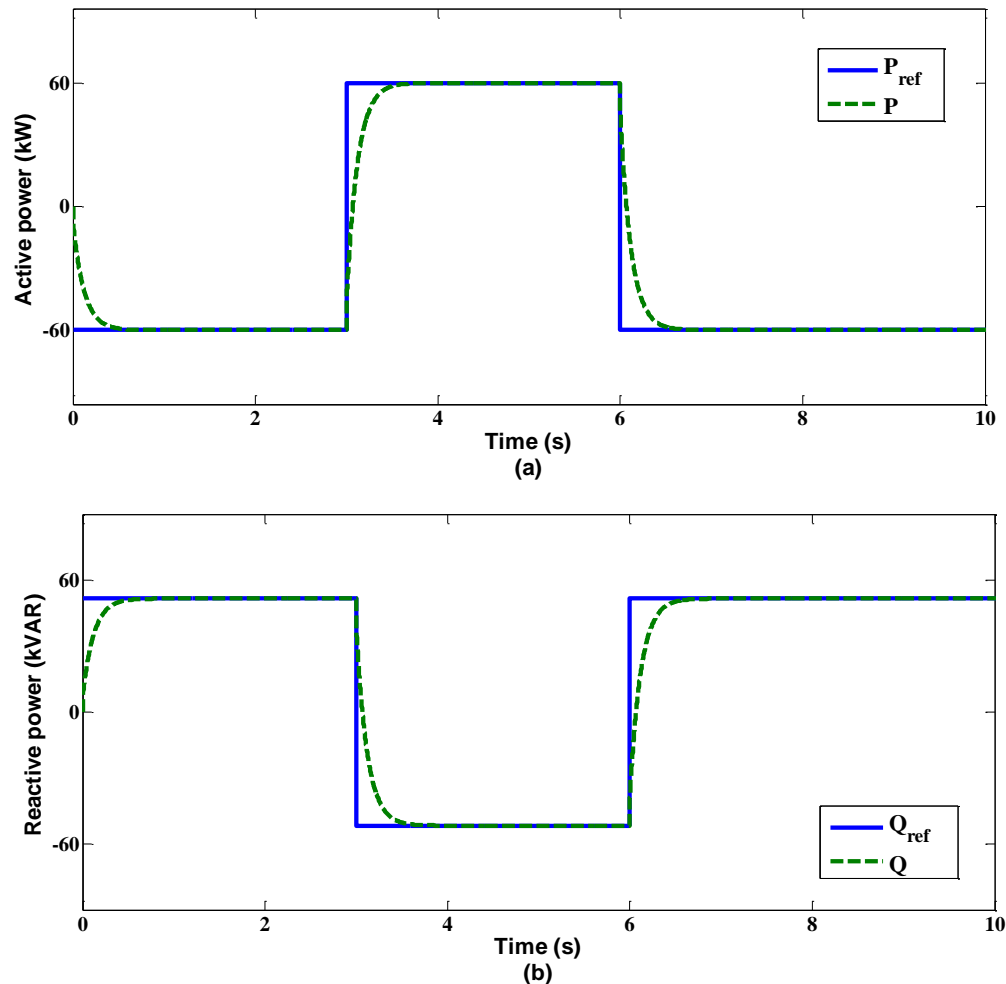


Figure 4.7 (a) Reference and measured active power, (b) reference and measured reactive power, injected to the grid

The reference and measured currents in the dq frame are plotted in Figure 4.8. The current control loop performance is validated where the measured signals, I_d and I_q track their references, I_{dref} and I_{qref} very closely. The controller is able to give a fast response that both

the I_d and I_q reach the references in a very short period. It can be observed that I_d and I_q respond to the step change in active power and reactive power respectively. Grid current waveforms, I^a , I^b and I^c are shown in Figure 4.9 where the grid currents respond with active power variation.

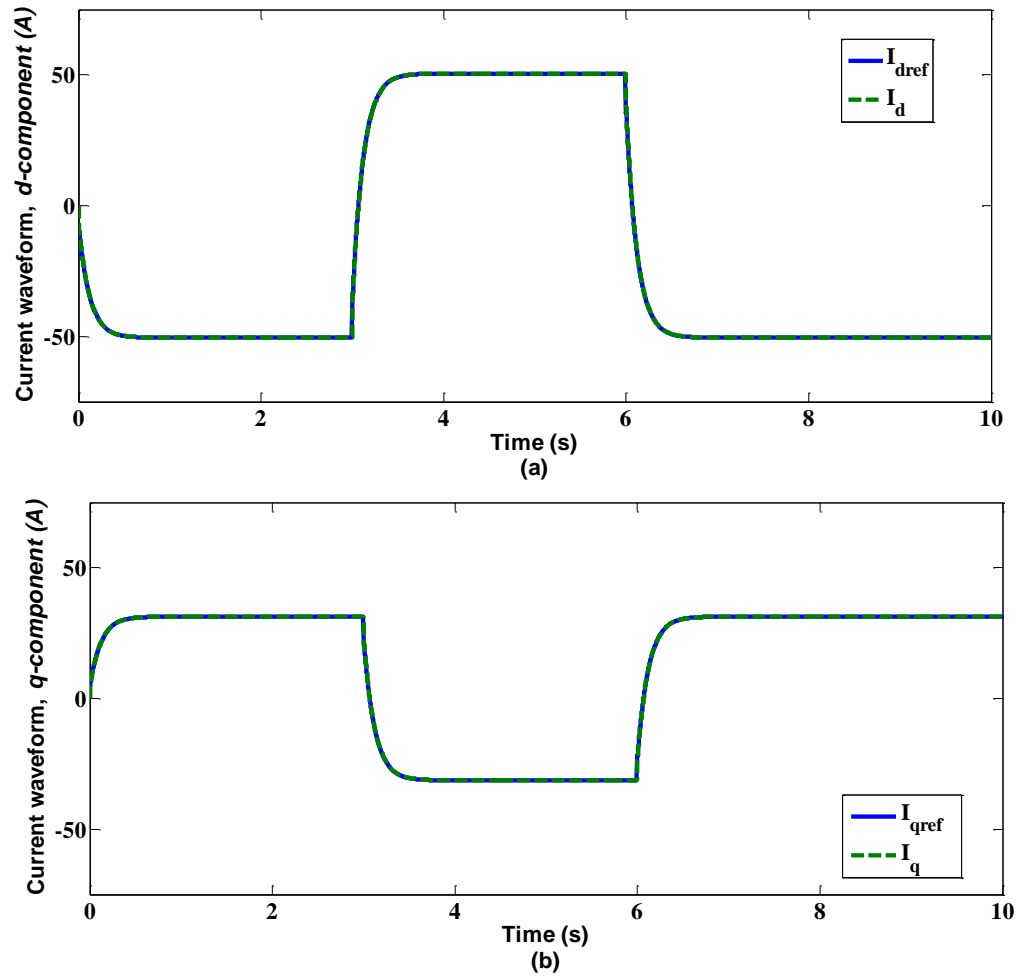


Figure 4.8 Reference and measured currents in dq frame (a) d component, (b) q component

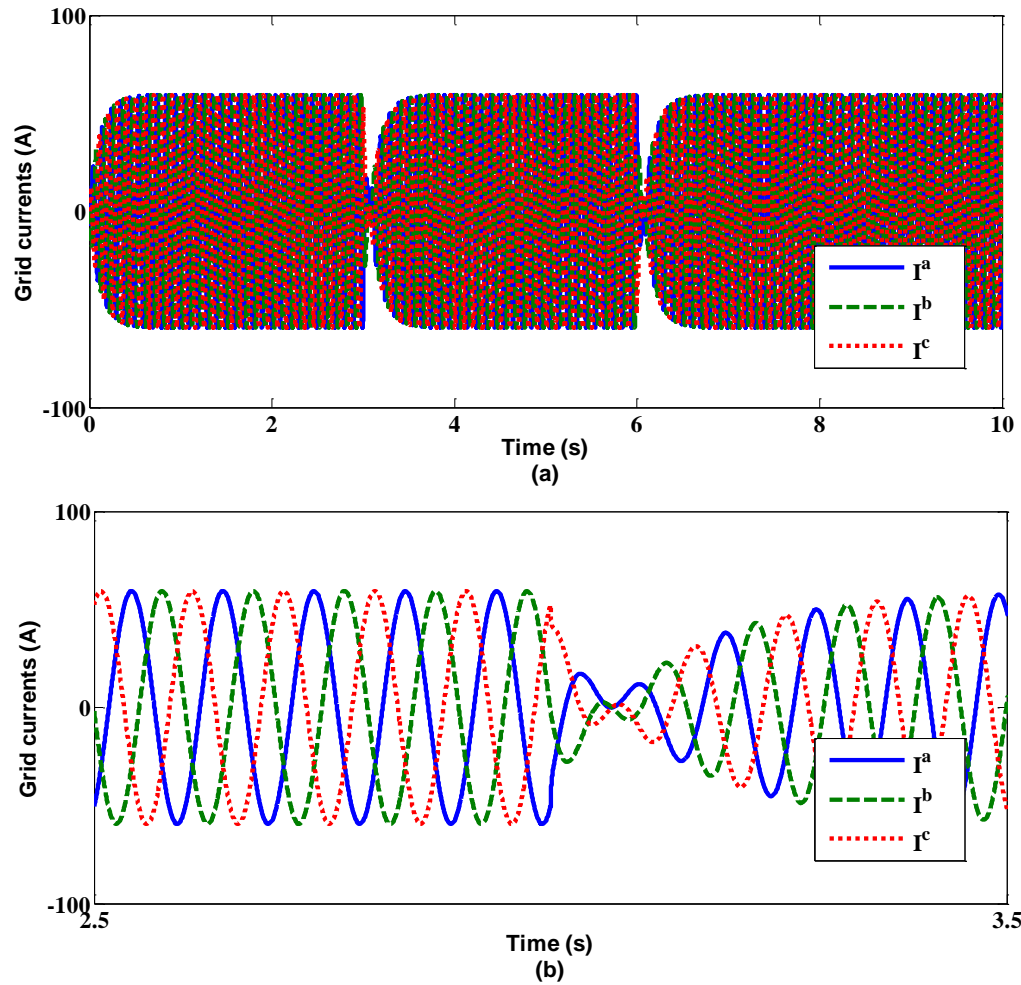


Figure 4.9 Grid currents for the duration of: (a) $0 < t < 10$ s, (b) $2.5 < t < 3.5$ s

4.5 Simulation of Large Numbers of Cells

It is well known that simulation of large systems tend to be slow as it requires huge computational resources that only high-performance multi-processors can meet. In this work, an integrated approach, including vectorisation and variable simulation time steps, is adopted to combine real-time simulation of communication systems and power-electronic-based systems together, which provides an efficient way to examine communication and control related issues in a BESS.

4.5.1 Cell Model

The fundamental concept of the cell modelling used in this work is to model a cell based on internal cell voltage and internal resistance, it is an IR model where it does not represent the transient behaviour of a cell. Internal cell voltage, V_{cell} is a non-linear function of SoC as depicted in (4.12). Using (4.13), SoC is obtained based on Coulomb Counting method by integrating cell current, I_{cell} .

$$V_{cell} = f(SoC) \quad (4.12)$$

$$SoC = \int_0^t I_{cell} dt \quad (4.13)$$

Figure 4.10 plots V_{cell} in the function of charge, Q based on a 3.6 V 2150 mAh Li-ion cell at 20 °C at 1 C charging rate.

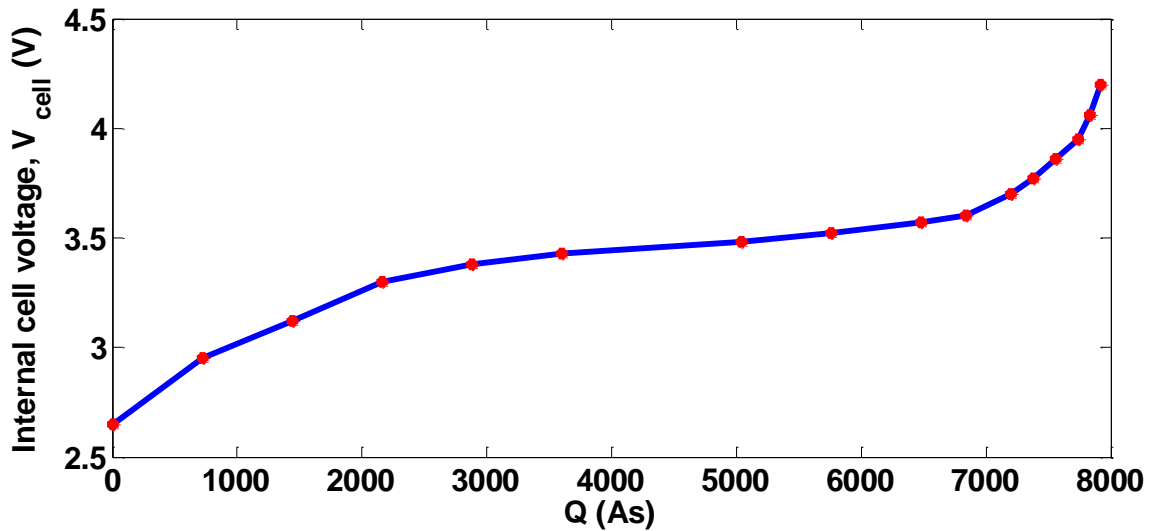


Figure 4.10 Recorded data points for modelling V_{cell} in a function of charge at $T = 20$ °C and $I_{cell} = 2.15$ A

Using Kirchhoff's Voltage Law, cell output voltage, V_{out} can be calculated by taking into account the voltage drop due to internal resistance in a cell, R_{int} as indicated in (4.14).

$$V_{out} = V_{cell} + I_{cell}R_{int} \quad (4.14)$$

where $I_{cell} > 0$ indicates the cell is charging and $I_{cell} < 0$ indicates the cell is discharging

In Figure 4.11, a cell consists of an ideal internal cell voltage, V_{cell} connecting in series with a resistor which represents the R_{int} . The R_{int} can be calculated using (4.15) based on the parameters extracted from manufacturer's datasheet in Appendix C. The R_{int} plot in a function of Q is illustrated in Figure 4.12. In some instances, R_{int} appears to be constant and the actual value is smaller than the effective load resistance [404].

$$R_{int} = \frac{\Delta V}{I_{1C} - I_{0.2C}} \quad (4.15)$$

where ΔV is the voltage difference at $Q = 7740$ As during $I_{1C} = 2.15$ A and $I_{0.2C} = 0.43$ A for a 3.6 V 2150 mAh Li-ion cell at 20 °C.

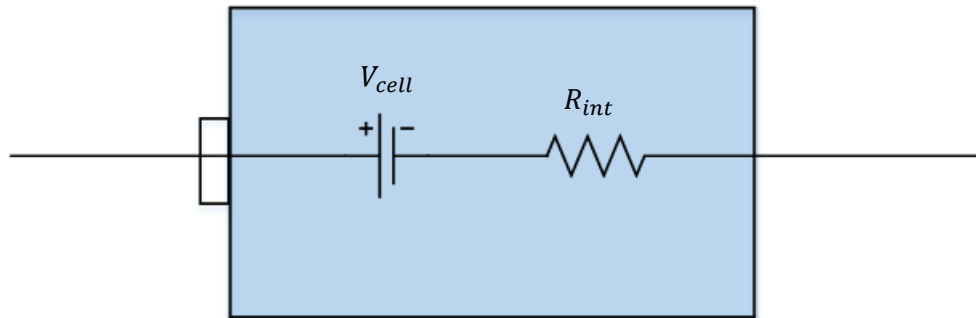


Figure 4.11 R_{int} of a cell

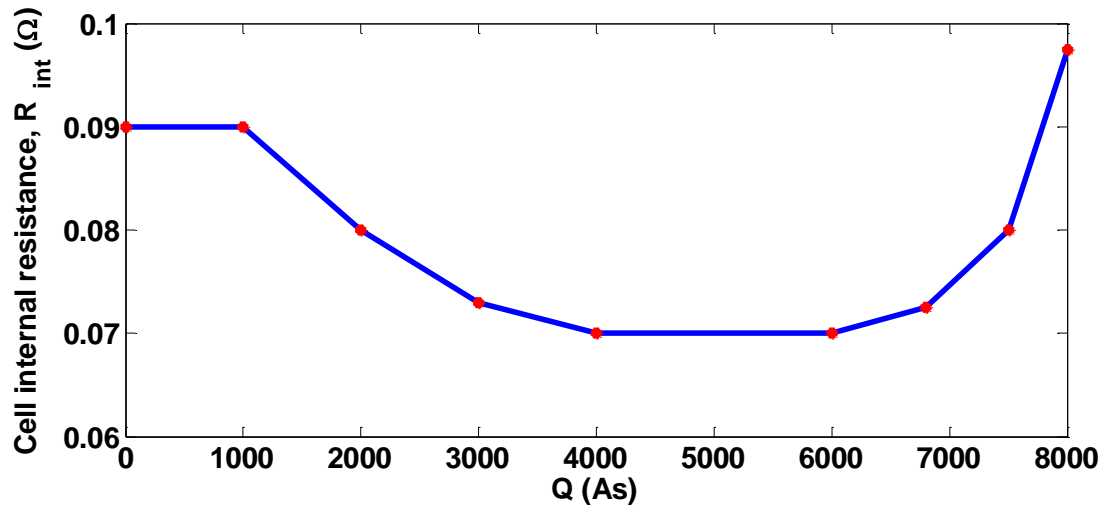


Figure 4.12 Recorded data points for modelling R_{int} in a function of SoC at $T = 20^\circ\text{C}$

Both V_{cell} and R_{int} are non-linear functions of SoC and can be modelled as a one-dimensional look-up table respectively, where the functions use linear interpolation to calculate the values between the recorded data points. Based on the parameters mentioned above, a simple Li-Ion cell model in Figure 4.13 can be implemented using look-up tables in MATLAB Simulink. The cell model allows independent setting of important parameters such as initial SoC, α_0 , cell Ampere-hour capacity, Q_{max} , and cell internal resistance, R_{int} . Multiple cells can be instantiated efficiently using vectorisation discussed in the following section.

4.5.2 Vectorisation

The fundamental idea behind vectorisation in a programming language such as MATLAB is that the operations are applied at once to the entire set of array instead of individual elements [405]. Vectorisation also enables multiple components to be created from a single component by entering the parameter in array format. Also known as array programming, it allows single-line representation of multiple signals. This is particularly

useful in this work as it involves the modelling of a large number of cells in the simulation model [406-407]. In addition to that, vectorisation improves the visual appearance as it avoids duplication of blocks of code or visual elements.

Consider a simple Li-Ion cell model in Figure 4.13 implemented using look-up tables in MATLAB Simulink, at the start of simulation, cell parameters are chosen randomly with a uniform distribution in the ranges given in Table 4.1. As it is needed to run the models for different values of α_0 , constant α_0 is made a vector, in which case all α_0 values would get added to the relative charge in and out of each cell, α_i and the result would be a vector of signals $[\alpha_0(1) \pm \alpha_i(1), \alpha_0(2) \pm \alpha_i(2), \dots, \alpha_0(N) \pm \alpha_i(N)]$.

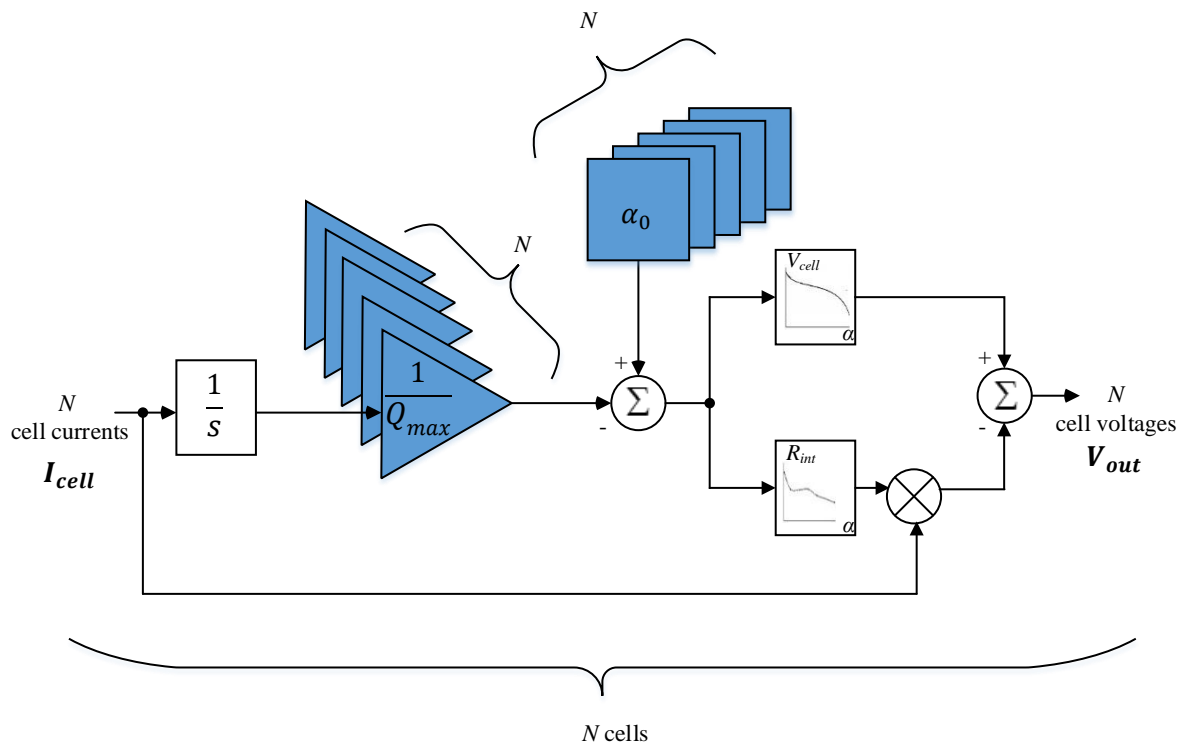


Figure 4.13 Single MATLAB Simulink block of Li-ion cell model for N cells

Table 4.1 Pre-defined range of cell parameters

No. of cells	N	35
Initial SoC	α_0	10-90 %
Capacity	Q_{max}	40-100 Ah
Internal resistance	R_{int}	0.07-0.15 Ω

4.5.3 Simulation Time Step Selection

Figure 4.14 shows the effect of small and large simulation time steps on the output voltage of a cascaded H-bridge multi-level converter. Each cell generates one voltage level, so each voltage step is V_{cell} . As indicated in Figure 4.14 (b), if the chosen simulation time step is too large, the voltage step will increase where a single voltage step is $2V_{cell}$ instead of V_{cell} .

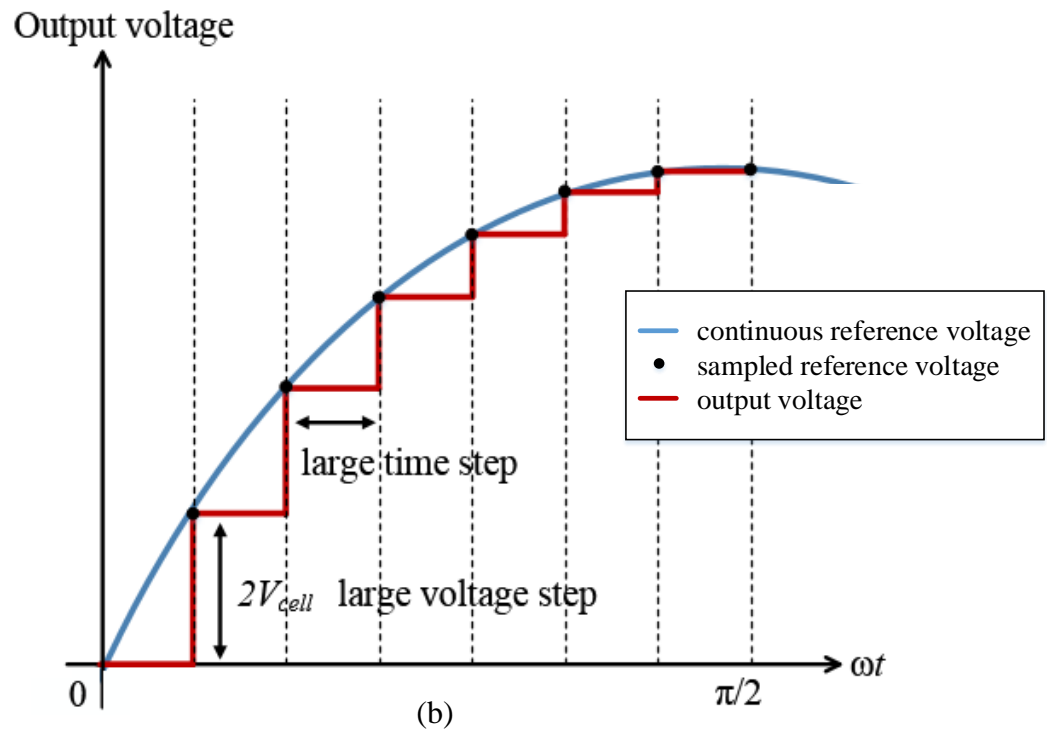
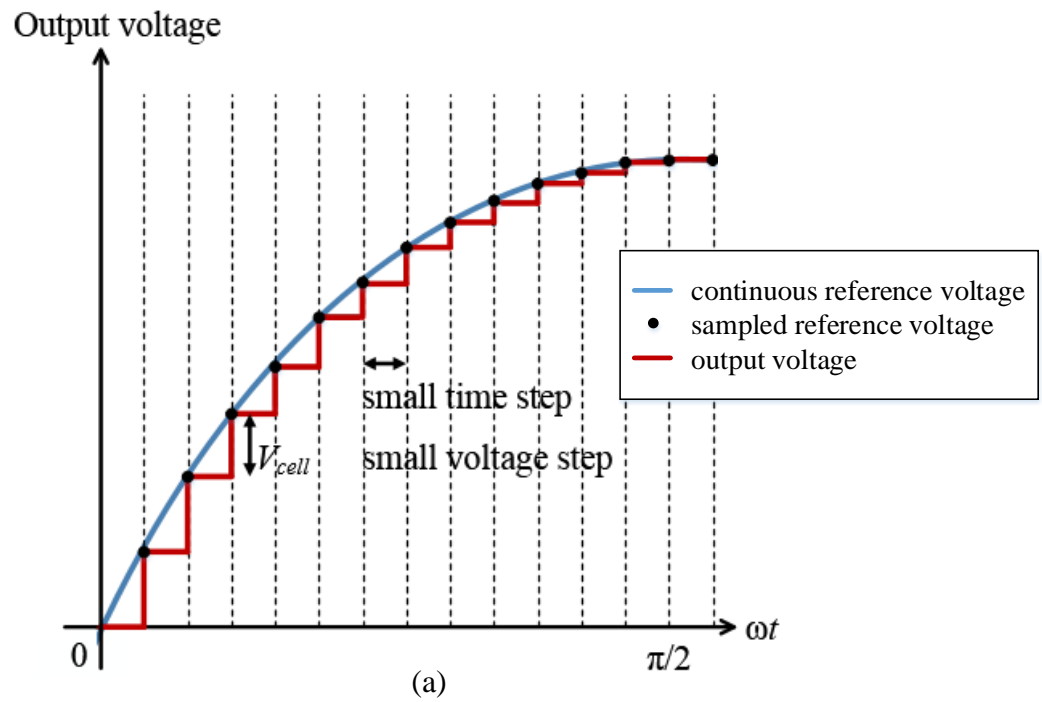


Figure 4.14 Output voltage of a cascaded H-bridge multi-level converter with different simulation time steps: (a) small simulation time step, (b) large simulation time step

Simulation of a large number of cells is time consuming and a proper way to select simulation time step is therefore necessary. In (4.16), a typical sinusoidal waveform is considered as reference voltage, V_{ref} with V_0 as peak voltage and ω_0 as fundamental frequency.

$$V_{ref} = V_0 \sin \omega_0 t \quad (4.16)$$

The maximum rate of voltage change occurs at the steepest point of a sinusoidal waveform which is when $\omega_0 t = 0$, as indicated in (4.17). Thus, this point is referred to as the critical point in order to appropriately select a simulation time step.

$$\max\left(\frac{dV_{ref}}{dt}\right) = \frac{\Delta V_{ref}}{T_s} = \omega_0 V_0 \quad (4.17)$$

The voltage change during one simulation time step, T_s is equal to a single cell voltage, thus ΔV_{ref} can be replaced by V_{cell} as shown in (4.18).

$$T_s < \frac{V_{cell}}{\omega_0 V_0} \quad (4.18)$$

4.5.4 Multiple Simulation Time Steps

Simulating a power-electronic-based system involves a wide range of time scales. In the proposed BESS, the time constants associated with the power semiconductor devices are on the order of microseconds while the time constants of the battery dynamics may extend over several seconds or hours. Therefore, a time-scale separation technique is used to decouple the overall system into fast and slow sub-systems. When advancing the fast sub-system, the slow state variables are used based on their derivatives evaluated at the previous time step, whereas the updated fast variables are used when advancing the slow

sub-system [408-410]. Its purpose is to increase simulation speed while preserving accuracy [411-412].

Multiple simulation time steps allow a certain time step to be chosen consistent with the system parameters. For example, it is necessary to update the grid voltage, converter voltage, cell voltage and switching signals in the order of microsecond. However, there is no noticeable change in the cell's SoC in a short interval of microseconds. Therefore, it is not necessary to update SoC as often as voltage and switching signals. The implementation of multiple simulation time steps reduces computational effort and therefore offers a significant improvement in the simulation speed.

4.6 Balancing of Cells in a Module

The cascaded-H-bridge multi-level converter circuit is formed by the series connection of a number of H-bridge circuits as shown in Figure 4.1. This topology allows independent control of each cell which naturally facilitates battery management. The output voltage of a 71-level (35 cells) cascaded-H-bridge multi-level converter can range from $-35V_{cell}$ to $+35V_{cell}$. Intermediate voltages of, for example, $+30V_{cell}$ can be obtained by switching any 30 H-bridges of the cascaded-H-bridge multi-level converter to provide $+V_{cell}$, whilst the remaining H-bridges produce 0 V. For all output levels apart from the maximum and minimum, many different cell combinations will provide similar output levels as demonstrated in Section 3.3.3. It is this state redundancy that provides scope for preferentially charging or discharging some cells over others, allowing the SoC of each cell to be adjusted independently over time.

In any practical BESS, there will be some degree of cell-to-cell variation described in Chapter 2 where even nominally identical cells within the battery pack will develop different capacities and SoC over time due to self-discharge, aging and a variety of temperature-related effects [413]. In order to fully utilise the capacity of every cell in a BESS, the control system must accommodate variations between cells such that every cell is fully discharged at the end of a discharge cycle (i.e. every cell should reach an SoC of 0 % simultaneously) and every cell is fully charged at the end of a charge cycle (i.e. every cell should reach an SoC of 100 % simultaneously) [414-416]. In this work, this is achieved by the balancing controller which attempts to maintain equal SoC across all cells in the BESS at all times.

The fundamental balancing principle is simple: At any particular instant of time, the balancing controller chooses a cell combination in order to get as close as possible to the value of the reference voltage, V_{ref} generated by the power controller. Assuming N cells in module m of sub-bank k , bank j and phase x , the balancing controller aims to keep SoC of each cell ($\alpha^{xjkm1} \dots \alpha^{xjkmN}$) in a module equal to the average SoC of the module, α^{xjkm} as indicated by (4.19). During discharge, cells with the highest SoC are prioritised for active use, and during charge, cells with the lowest SoC are prioritised instead. This tends to equalise the SoC as the charge or discharge cycle progresses by minimising the SoC difference ($\Delta\alpha^{xjkmn}$) shown in (4.19), eventually leading to an equal SoC across all cells in the module.

$$\begin{bmatrix} \Delta\alpha^{xjkm1} \\ \vdots \\ \Delta\alpha^{xjkmN} \end{bmatrix} = \begin{bmatrix} |\alpha^{xjkm1} - \alpha^{xjkm}| \\ \vdots \\ |\alpha^{xjkmN} - \alpha^{xjkm}| \end{bmatrix} \approx 0 \quad (4.19)$$

where $\Delta\alpha^{xjkmn}$ is the SoC difference between cell n and average SoC of module m , α^{xjkmn} is the SoC of cell n , and N is the number of cells in a module, α^{xjkm} is the average SoC of module m .

Figure 4.15 shows a pseudocode to demonstrate the control strategy of balancing of cells in a module: First, the power flow direction is checked. If it is positive, the system is discharging; therefore, cells are sorted in descending order so that the cells with highest SoC are used first. Otherwise, the system is charging and cells are sorted in ascending order so that the cells with lowest SoC are used first. The algorithm now works from the start of the sorted cell list: cells are ‘used’ (switched in by the H-bridge) to build a module output voltage (V_{out}^{xjkm}) closer to the reference voltage (V_{ref}^{xjkm}) until the use of the next cell on the list would take V_{out}^{xjkm} further away from V_{ref}^{xjkm} , at which point the algorithm terminates.

The algorithm builds an n -vector S^{xjkm} corresponding to the desired state of each H-bridge in the module. Referring to Table 4.2, each element of S^{xjkm} is +1, 0 or -1 to indicate cell insertion direction. When the algorithm terminates, the gate signals to the MOSFETs in the module are updated accordingly. Figure 4.16 shows the switching signals of cells in a module using a grid frequency of 1 Hz instead of 50 Hz for the sake of simplicity. As illustrated in Figure 4.16, only positive cell directions are used when V_{ref}^{xjkm} is positive, and only negative cell directions are used when V_{ref}^{xjkm} is negative.

```

begin Cell sorting
if  $P_{ref} > 0$  then sort cells in descending order of SoC
else sort cells in ascending order of SoC
endif
end Cell sorting

begin Nearest voltage matching
initialize  $S_{acc}^{xjkmn} \leftarrow 0; V_{acc} \leftarrow 0; S^{xjkmn} \leftarrow 0$ 
for  $n \leftarrow 1$  to  $N$  do
  if enabling the cell would make the  $V_{out}^{xjkm}$  closer to  $V_{ref}^{xjkm}$ 
  then cell is enabled
    if  $V_{ref}^{xjkm} > 0$  then  $S_{acc}^{xjkm} \leftarrow 1; V_{acc} \leftarrow V_{acc} + V_{cell}^{xjkmn}$ 
    else, if  $V_{ref}^{xjkm} < 0$  then  $S_{acc}^{xjkmn} \leftarrow -1; V_{acc} \leftarrow V_{acc} - V_{cell}^{xjkmn}$ 
    endif
     $V_{acc} \leftarrow V_{acc} + V_{cell}^{xjkmn}$ 
  endif
endfor
 $S^{xjkmn} \leftarrow S_{acc}^{xjkmn}; V_{out}^{xjkm} \leftarrow V_{acc}$ 
end Nearest voltage matching

```

Figure 4.15 Pseudocode: balancing of cells in a module

Table 4.2 Signals in the balancing controller

Level	I/O	Signals	Description
H-bridge and cell	output	α^{xjkmn} V_{cell}^{xjkmn}	SoC and output voltage of cell n in module m in sub-bank k in bank j in phase x .
	input	S^{xjkmn} ($S^{xjkmn} = -1,0,1$ for cell inserted in negative direction, bypassed, inserted in positive direction)	Switching signal for H-bridge n in module m in sub-bank k in bank j in phase x .
Module	output	$\alpha^{xjkm} = \frac{1}{N} \sum_{n=1}^N \alpha^{xjkmn}$ $V_{max}^{xjkm} = \sum_{n=1}^N V_{cell}^{xjkmn}$	Average SoC and maximum output voltage of module m in sub-bank k in bank j in phase x .
	input	$\Delta\alpha^{xjkm} = \alpha^{xjkm} - \alpha^{xjk}$ $V_{ref}^{xjkm} =$ $\frac{1}{M} V_{ref}^{xjk} (1 \pm \beta \Delta\alpha^{xjkm}) \begin{cases} + \text{ if } P_{ref} > 0 \\ - \text{ if } P_{ref} \leq 0 \end{cases}$	Reference voltage for module m in sub-bank k in bank j in phase x .
Sub-bank	output	$\alpha^{xjk} = \frac{1}{M} \sum_{m=1}^M \alpha^{xjkm}$ $V_{max}^{xjk} = \sum_{m=1}^M V_{max}^{xjkm}$	Average SoC and maximum output voltage of sub-bank k in bank j in phase x .
	input	$\Delta\alpha^{xjk} = \alpha^{xjk} - \alpha^{xj}$ $V_{ref}^{xjk} = \frac{1}{K} V_{ref}^{xj} (1 \pm \beta \Delta\alpha^{xjk})$	Reference voltage for sub-bank k in bank j in phase x .
Bank	output	$\alpha^{xj} = \frac{1}{K} \sum_{k=1}^K \alpha^{xjk}$ $V_{max}^{xj} = \sum_{k=1}^K V_{max}^{xjk}$	Average SoC and maximum output voltage of bank j in phase x .
	input	$\Delta\alpha^{xj} = \alpha^{xj} - \alpha^x$ $V_{ref}^{xj} = \frac{1}{J} V_{ref}^x (1 \pm \beta \Delta\alpha^{xj})$	Reference voltage for bank j in phase x .
Phase	output	$\alpha^x = \frac{1}{J} \sum_{j=1}^J \alpha^{xj}$ $V_{max}^x = \sum_{j=1}^J V_{max}^{xj}$	Average SoC and maximum output voltage of phase x .
	input	V_{ref}^x	Reference voltage for phase x (produced by zero-sequence injection block).
Zero-sequence injection	output	$\alpha = \frac{1}{3} (\alpha^a + \alpha^b + \alpha^c)$	Average SoC of whole system.
	internal	$\Delta\alpha^x = \alpha^x - \alpha$ $P_{ref}^x = \frac{1}{3} P_{ref} (1 \pm \beta \Delta\alpha^x)$	Reference power calculated internally (used to produce zero-sequence component of V_{ref}^x).

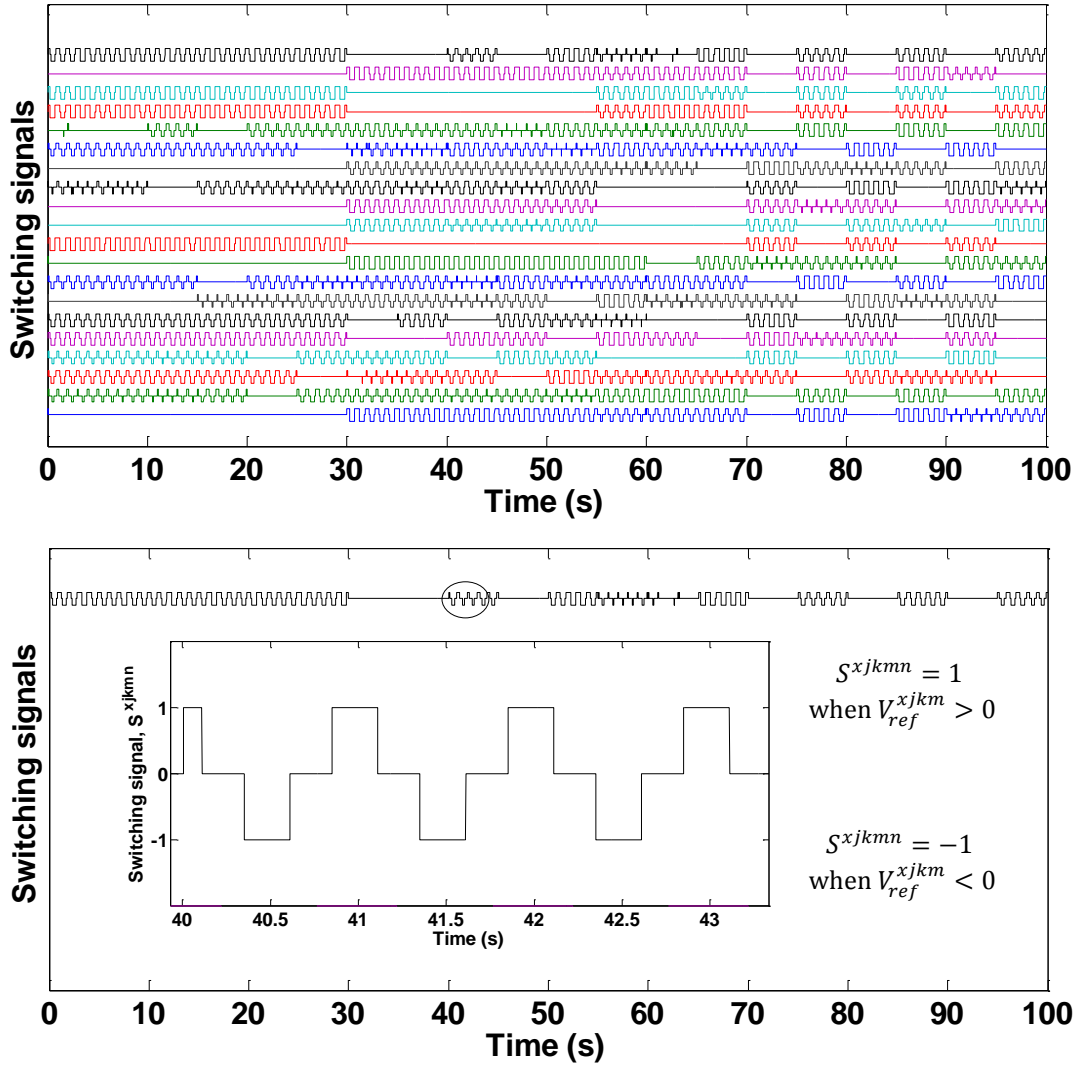


Figure 4.16 Switching signals: turning on and off a cell

The switching signal, S^{xjkmn} and phase current, I^x are inputs to the cell model as shown in Figure 4.17. Table 4.3 demonstrates that by controlling S^{xjkmn} and I^x , I_{cell} can be either positive, negative or zero, thus, a cell can be charged or discharged. Figure 4.18 presents cell current waveforms where a dashed line is drawn as a reference to indicate that a cell is not in used ($I_{cell} = 0$). It can be observed that system was charging initially and was switched to discharging at $t = 30$ s and was swapped back to charging again at $t = 60$ s.

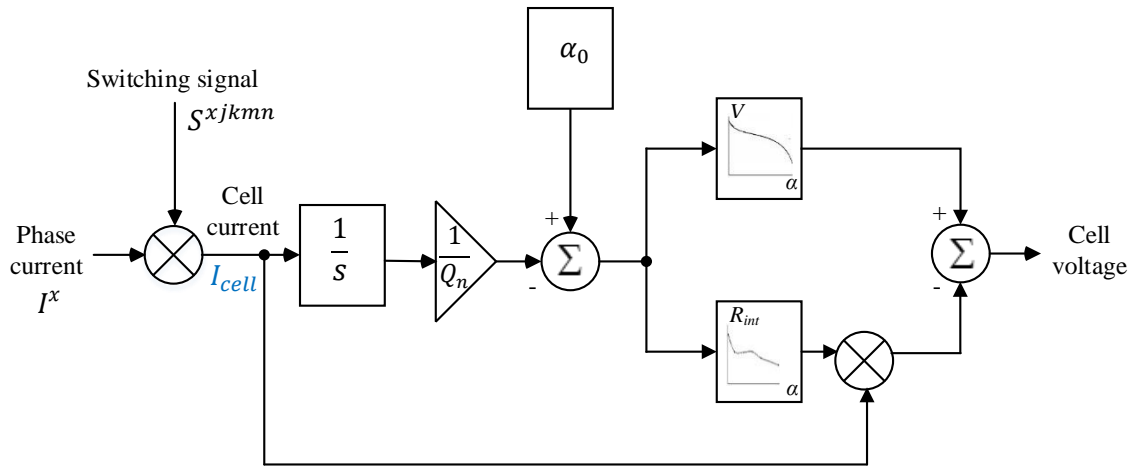


Figure 4.17 Inputs to cell model: S^{xjkmn} and I^x

Table 4.3 Charging and discharging control of a cell

Switching signal, S^{xjkmn}	Phase current, I^x	Cell current, I_{cell}	Cell status
+1	+I	+I	on - discharging
+1	-I	-I	on - charging
-1	+I	-I	on - charging
-1	-I	+I	on - discharging
0	X	X	off

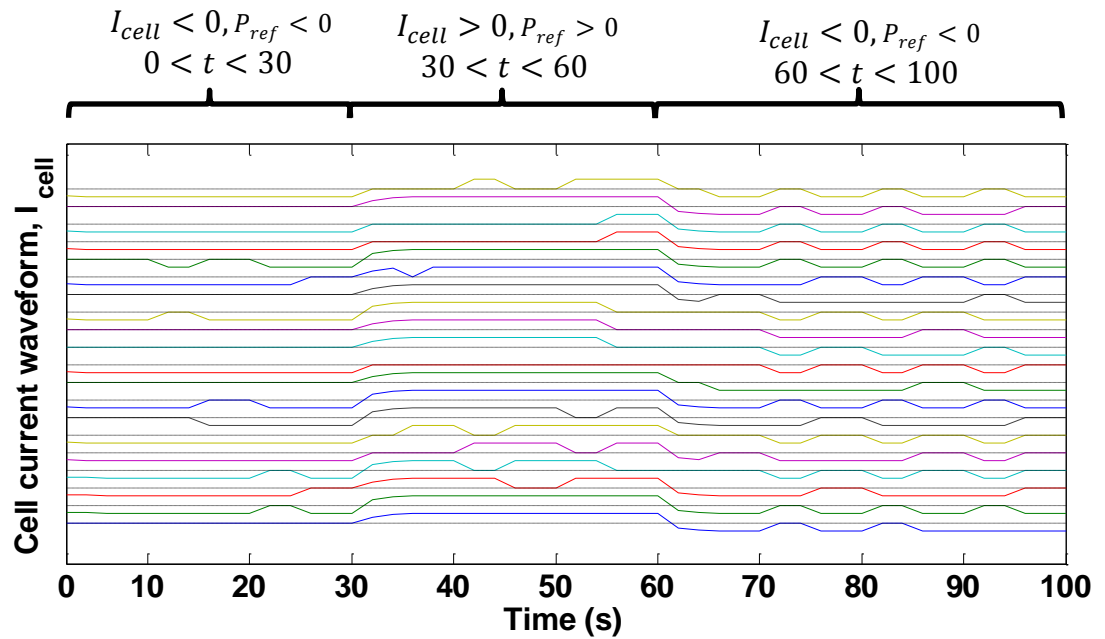


Figure 4.18 Cell current

By repeating this process many times during a fundamental cycle of the grid waveform, V_{out}^{xjkm} can be made to follow a sinusoidal reference voltage, and, as long as the number of cells is relatively large, it will tend to provide a good approximation of the reference as shown in Figure 4.19. The key property of the algorithm is that it tends to push the SoC of the cells in the module together over time, i.e. to provide cell balancing internal to the module. The number of times the algorithm is executed per fundamental cycle is the effective sampling rate, f_s of the system. As explained in Section 4.5.4, this rate should be set high enough so that, under steady state conditions, the reference voltage increases or decreases by a maximum of a single cell voltage, V_{cell} at each step, in this case the algorithm will produce the smoothest possible waveform as it will insert (or remove) one cell per sample step. The sampling rate should therefore be scaled proportionally with the number of cells in a module as indicated in (4.18).

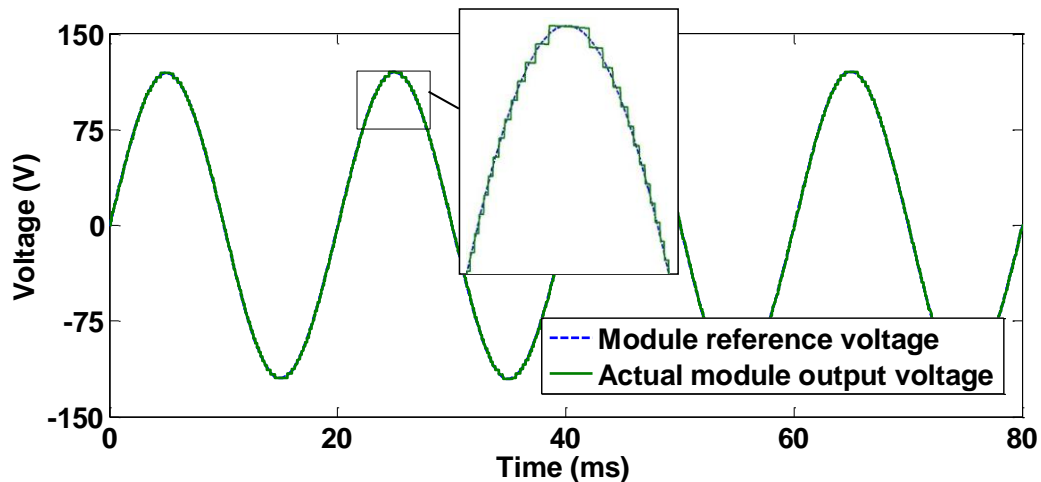


Figure 4.19 Output voltage of a 71-level cascaded H-bridge multi-level converter

4.7 Balancing of Modules within a Sub-bank, Sub-banks within a Module and Banks in a Phase

Figure 4.20 shows the hierarchical nature of and the signal flow within the balancing controller. Table 4.2 details how each signal is calculated at each level within the hierarchy. For all V_{ref} and P_{ref}^x calculations, positive sign is used if active power flow is positive ($P_{ref} > 0$ indicates the system is discharging); and the negative sign is used if active power flow is negative ($P_{ref} < 0$ indicates the system is charging). This is achieved by distributing the reference voltage for each member of a level in proportion (or in negative proportion) to that members' SoC deviation from the average SoC of all members, depending on whether the system is discharging (or charging). Taking modules within a sub-bank as an example, the balancing controller aims to keep SoC of each module ($\alpha^{xjk1} \dots \alpha^{xjkM}$) within a sub-bank equal to the average SoC of the sub-bank, α^{xjk} as shown in (4.20).

$$\begin{bmatrix} \Delta\alpha^{xjk1} \\ \vdots \\ \Delta\alpha^{xjkM} \end{bmatrix} = \begin{bmatrix} |\alpha^{xjk1} - \alpha^{xjk}| \\ \vdots \\ |\alpha^{xjkM} - \alpha^{xjk}| \end{bmatrix} \approx 0 \quad (4.20)$$

where $\Delta\alpha^{xjkm}$ is the SoC difference between module m and average SoC of sub-bank k , α^{xjkm} is the average SoC of module m , and M is the number of modules in a sub-bank, α^{xjk} is the average SoC of sub-bank k .

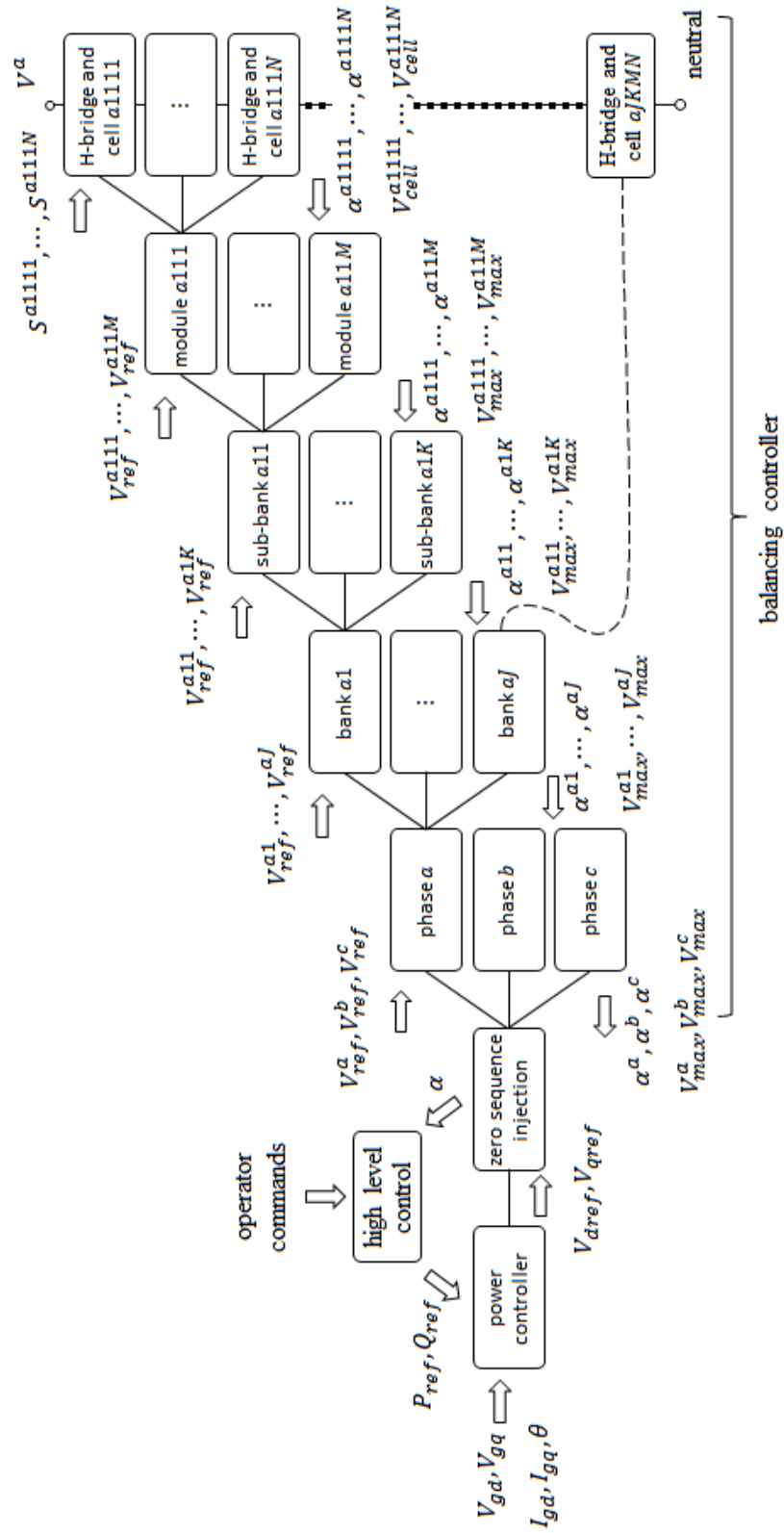


Figure 4.20 Balancing controller hierarchy and internal signal flow

The principle is demonstrated by taking modules within a sub-bank during discharge as example: the reference voltage (V_{ref}^{xjkm}) supplied to each module is dependent on that modules' SoC difference from the average SoC of all modules in the sub-bank ($\Delta\alpha^{xjkm}$). The reference voltage for the sub-bank is shared equally across all modules in the sub-bank but with the addition (or subtraction) of extra voltage which is proportional to $\Delta\alpha^{xjkm}$. β is the constant of proportionality and sets the strength of charge balancing (higher β increases sensitivity to small SoC differences). The sum of the reference voltages for all modules in a sub-bank is always equal to the reference voltage for that sub-bank as indicated in (4.21). The control strategy is illustrated in a pseudocode shown in Figure 4.21.

$$\begin{cases} V_{ref}^{xjk} = V_{ref}^{xjk1} + V_{ref}^{xjk2} + \dots + V_{ref}^{xjkM} \\ V_{ref}^{xjk} = \sum_{m=1}^M V_{ref}^{xjkm} \end{cases} \quad (4.21)$$

where V_{ref}^{xjk} is the reference voltage assigned to sub-bank k , V_{ref}^{xjkm} is the reference voltage assigned to module m , and M is the number of modules in a sub-bank.

```

begin Calculate SoC difference
for  $m \leftarrow 1$  to  $M$  do
     $\Delta\alpha^{xjkm} \leftarrow \alpha^{xjkm} - \alpha^{xjk}$ 
endfor
end Calculate SoC difference

begin Set reference voltage
if  $P_{ref} > 0$ 
    for  $m \leftarrow 1$  to  $M$  do
         $V_{ref}^{xjkm} = \frac{1}{M} V_{ref}^{xjk} (1 + \beta \Delta\alpha^{xjkm})$ 
    endfor
else
    for  $m \leftarrow 1$  to  $M$  do
         $V_{ref}^{xjkm} = \frac{1}{M} V_{ref}^{xjk} (1 - \beta \Delta\alpha^{xjkm})$ 
    endfor
endif
end Set reference voltage

```

Figure 4.21 Pseudocode: Balancing of modules within a sub-bank

Figure 4.22 shows how the selection of β value affects the SoC convergence with $\beta=1$, $\beta=10$ and $\beta=100$ respectively. It can be seen that higher β accelerates the convergence of module SoC.

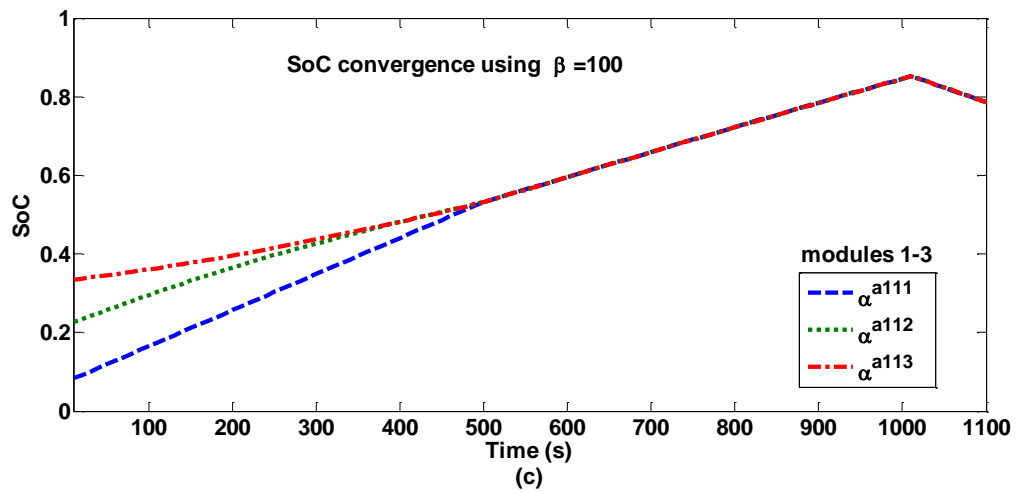
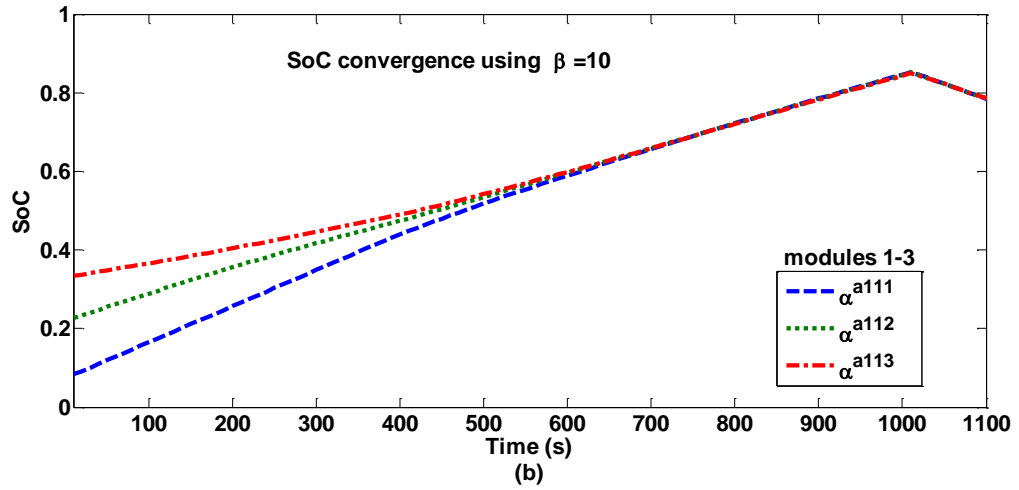
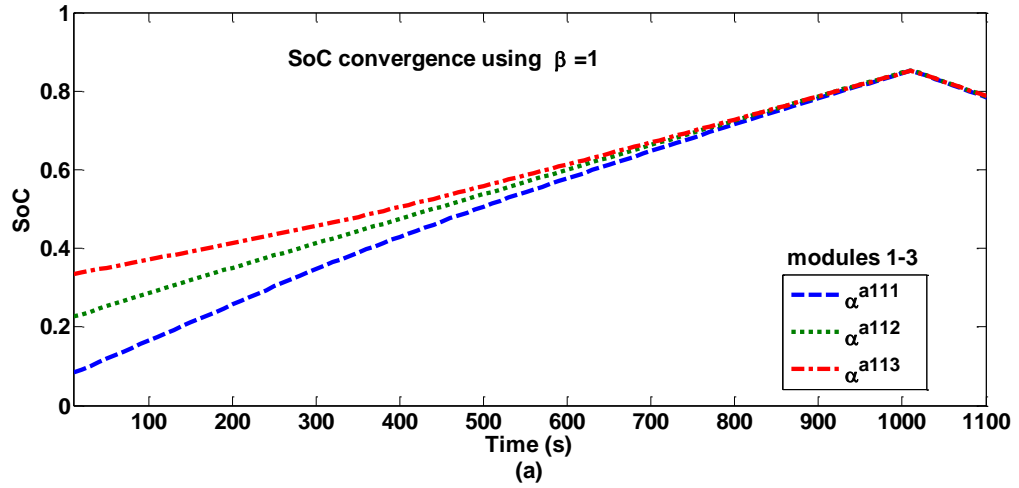


Figure 4.22 Effect of β value selection on SoC convergence (a) $\beta=1$, (b) $\beta=10$ and (c) $\beta=100$

The reference voltage is greater for the modules with the higher average SoC and so these modules will tend to be discharged more rapidly because more cells from these modules will be used to construct the output voltage of the overall cascaded H-bridge multi-level converter circuit. Conversely, during charge, the reference voltage is made greater for the modules with lower average SoC so that they will tend to be preferentially charged.

The hierarchical nature of the balancing controller can now be seen: the balancing control occurring at the sub-bank level causes cell SoCs to be equalised across modules in the sub-bank because the average SoC of each module is made equal and the cell balancing algorithm from Section 4.6 ensures that the SoC of cells within a module are equal. This is achieved without the requirement for the sub-bank balancing controller to receive and process the individual SoC for each cell in all modules (MN values), or to provide switching signals to each H-bridge cell ($4MN$ signals). Only the average module SoCs are required (M values) and only a set of module reference voltages need to be generated (M values).

As illustrated in Table 4.2, balancing of sub-banks within a bank and then balancing of banks within a phase proceeds in an identical manner to that of modules within sub-banks. Critically, communication between layers is limited to three values (SoC, V_{ref} and V_{max}) for each member of the next-lowest level only (the role of the parameter V_{max} is described in Chapter 5). It is not necessary to propagate e.g. values for individual cell SoC from the cell level all the way up the hierarchy to the phase level: This would present major challenges to scaling to very large numbers of cells due to the exponential growth of cell number with number of levels in the hierarchy. The balancing controller could theoretically

be extended to any number of hierarchical levels by continuing the pattern in Table 4.2, however it may become progressively more challenging to calculate and propagate signals rapidly enough to allow the system to follow the reference voltage accurately.

4.8 Balancing between Phases

A fundamental-frequency zero-sequence voltage, V_{ref0} is injected into each phase reference voltage (V_{ref}^a , V_{ref}^b and V_{ref}^c) to provide independent control of the power delivered by each phase as indicated in (4.22). This allows each of the three phases to inject or absorb an unequal active power without drawing negative-sequence voltage. Thus, SoC balancing control between phases can be performed in a similar manner as that provided within each phase. The block diagram demonstrating the zero-sequence voltage injection used for SoC balancing control between phases is shown in Figure 4.1.

$$\begin{bmatrix} V_{ref}^a \\ V_{ref}^b \\ V_{ref}^c \end{bmatrix} = \begin{bmatrix} V_{ref+}^a \\ V_{ref+}^b \\ V_{ref+}^c \end{bmatrix} + \begin{bmatrix} V_{ref0} \\ V_{ref0} \\ V_{ref0} \end{bmatrix} \quad (4.22)$$

where V_{ref+}^a , V_{ref+}^b and V_{ref+}^c represents positive-sequence voltage of the reference voltages.

Figure 4.23 illustrates the vector diagram of V_{ref0} injection in a three-phase system. Point ‘o’ represents the neutral point of the grid while point ‘v’ represents the neutral point of the VSC. The three-phase output voltages of the VSC are ‘oa’, ‘ob’ and ‘oc’. V_{ref0} is indicated by ‘vo’ and a proper V_{ref0} injection is required to ensure an equal amplitude of phase voltage among ‘oa’, ‘ob’ and ‘oc’ in order not to affect the grid-side three-phase line voltages whilst providing SoC balancing between phases.

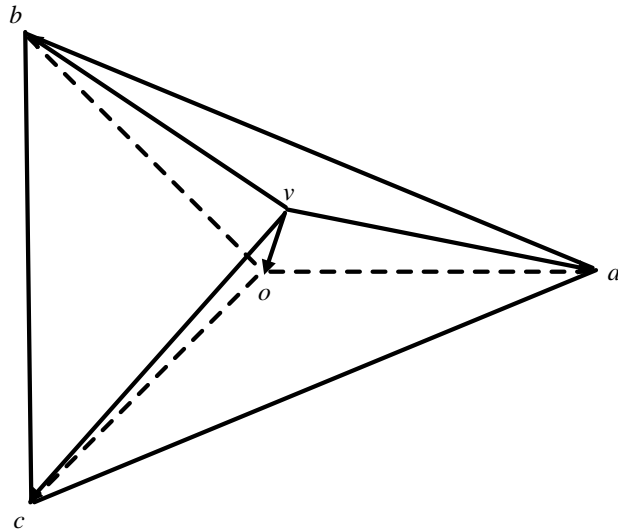
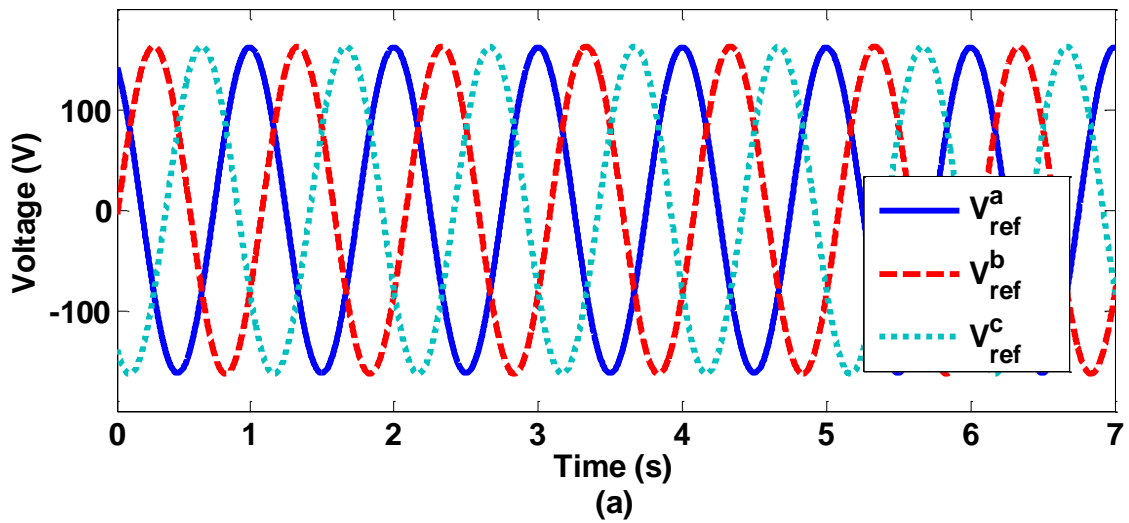
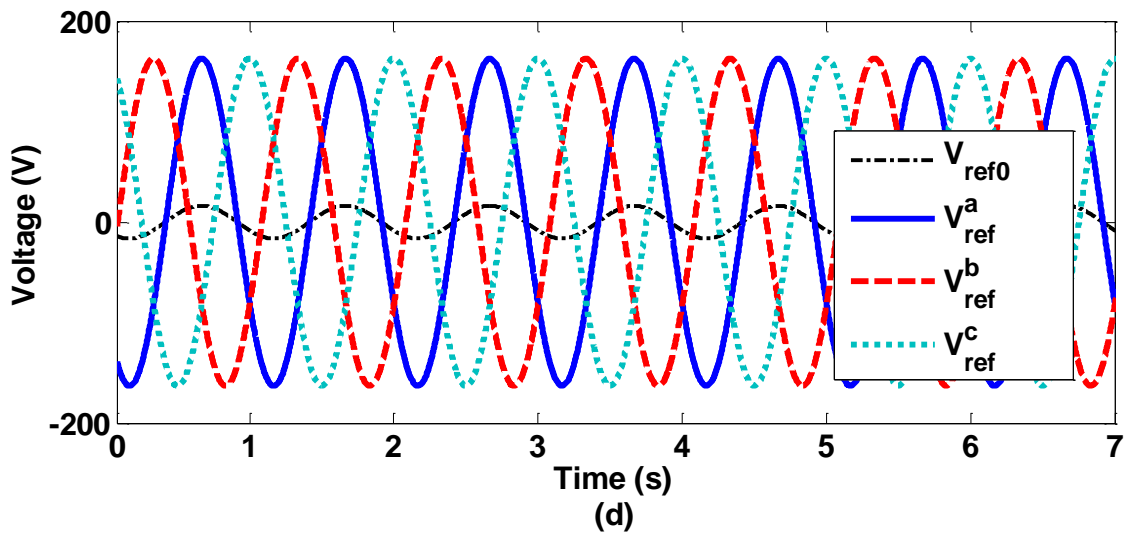
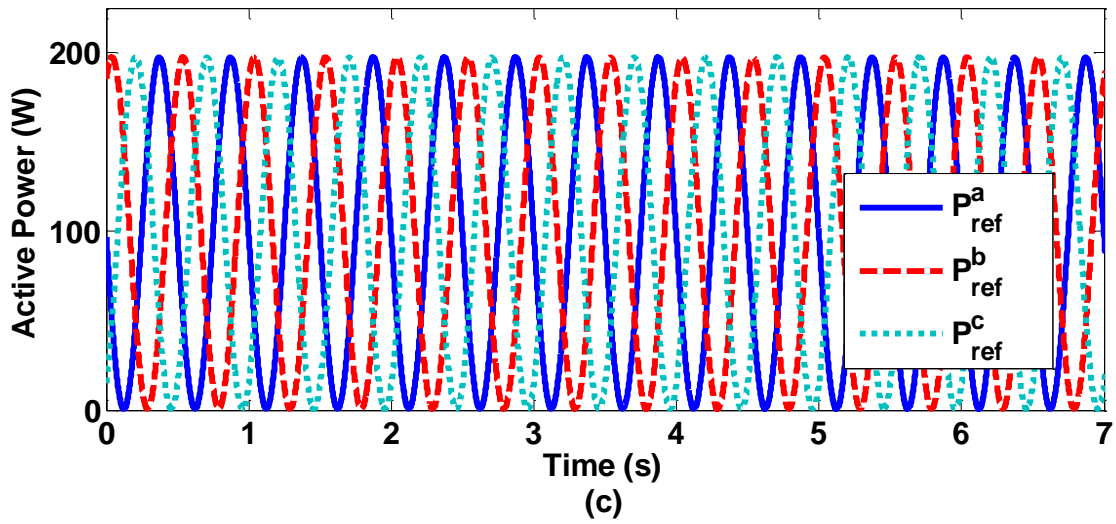
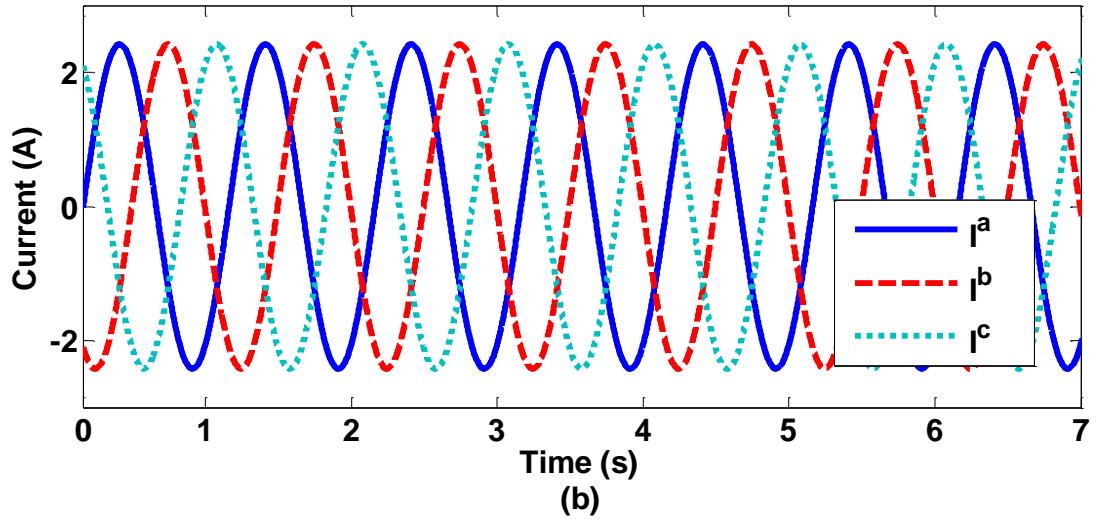


Figure 4.23 Vector diagram of V_{ref0} injection to a three-phase system

Figure 4.24 shows the effect of V_{ref0} injection on three-phase electrical power. Figure 4.24(a)-(c) presents the voltage, current and power waveforms under normal condition while Figure 4.24(d)-(f) depicts the corresponding waveforms under condition where the V_{ref0} is injected. The dash-dot line in Figure 4.24(d) is the injected V_{ref0} waveform.





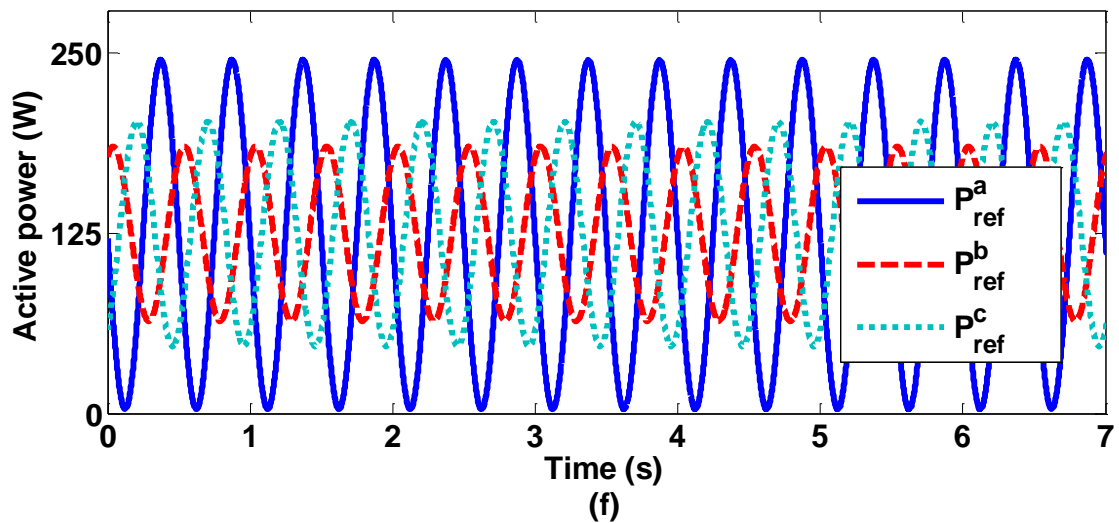
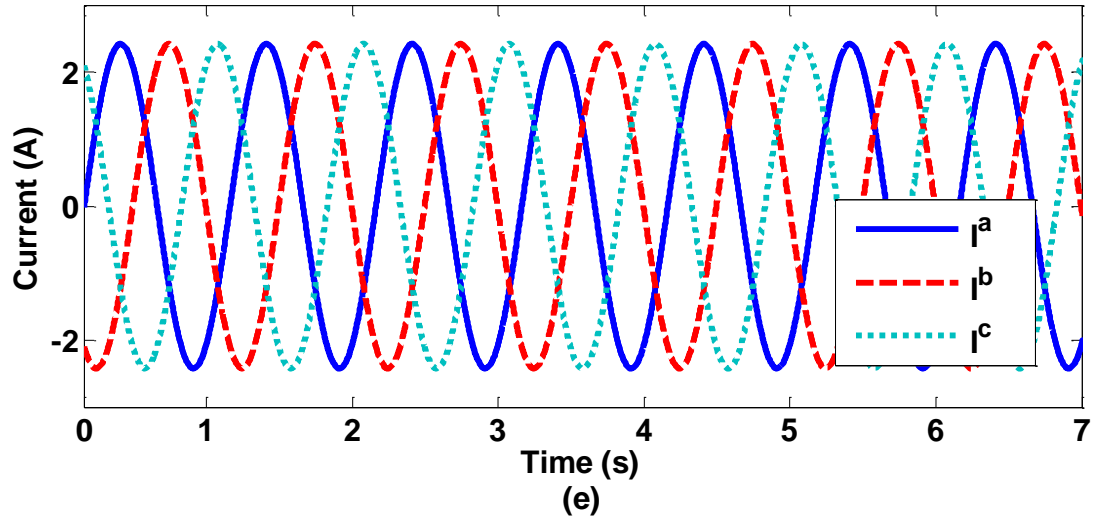


Figure 4.24 The effect of V_{ref0} injection on three-phase electrical power: (a) voltage, (b) current, (c) power under normal condition; (d) voltage, (e) current, (f) power during V_{ref0} injection

The active power absorbed or released by each phase consists of two components: the power due to the positive-sequence voltage from the power controller and the power attributed to the V_{ref0} injection. The required zero-sequence power (ΔP_{ref}^x) can be calculated from the overall system power reference (P_{ref}) and the power references from the balancing controller (P_{ref}^x , see Table 4.2) as shown in (4.23).

$$\begin{bmatrix} \Delta P_{ref}^a \\ \Delta P_{ref}^b \\ \Delta P_{ref}^c \end{bmatrix} = \begin{bmatrix} P_{ref}^a \\ P_{ref}^b \\ P_{ref}^c \end{bmatrix} - \frac{P_{ref}}{3} \quad (4.23)$$

The zero-sequence power components sum to zero ($\Delta P_{ref}^a + \Delta P_{ref}^b + \Delta P_{ref}^c = 0$), thus, V_{ref0} injection produces no effect on the overall three-phase power flow. In (4.24), the V_{ref0} is calculated from the phase balancing power references (ΔP_{ref}^a and ΔP_{ref}^b) and the measured grid currents (represented by I_d and I_q). See Appendix D for detailed calculation of V_{ref0} .

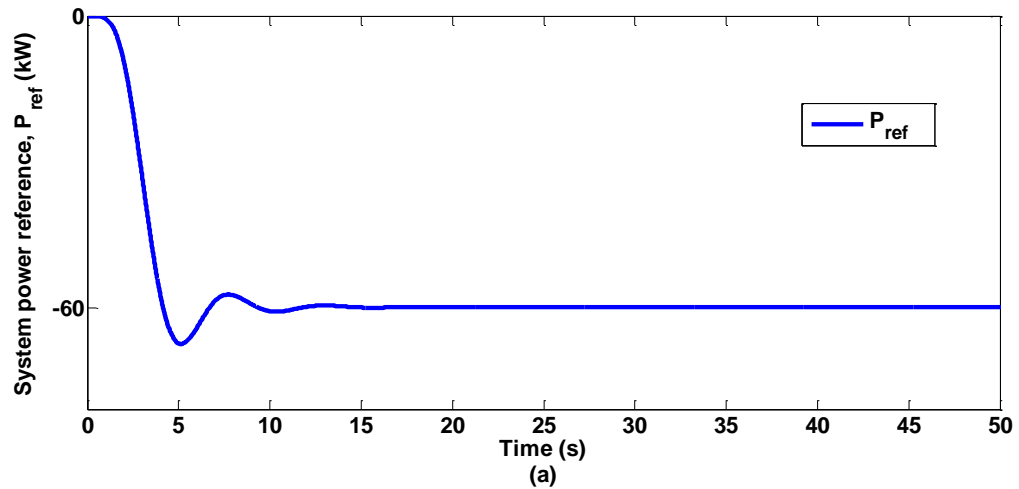
$$V_{ref0} = \frac{2\Delta P_{ref}^a(\sqrt{3}I_d + I_q) + 4\Delta P_{ref}^b I_q}{\sqrt{3}(I_d^2 + I_q^2)} \cos \theta + \frac{2\Delta P_{ref}^a(\sqrt{3}I_d - I_q) - 4\Delta P_{ref}^b I_d}{\sqrt{3}(I_d^2 + I_q^2)} \sin \theta \quad (4.24)$$

The final phase reference voltages supplied to the balancing controller are calculated using the $dq0$ to abc transformation [385] (see Appendix B) as shown in (4.25).

$$\begin{bmatrix} V_{ref}^a \\ V_{ref}^b \\ V_{ref}^c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \begin{bmatrix} V_{refd} \\ V_{refq} \\ V_{ref0} \end{bmatrix} \quad (4.25)$$

Since the V_{ref0} injection does not cause any change in the line-to-line voltage on the delta side of the transformer, the phase balancing control does not affect the grid-side three-phase line voltages, and so power flow at the grid interface remains balanced across all phases. Without phase balancing control ($\Delta P_{ref}^a = \Delta P_{ref}^b = \Delta P_{ref}^c = 0$), the power references from the balancing controller in Figure 4.1 provides an equal power reference for each phase, i.e. $P_{ref}^a = P_{ref}^b = P_{ref}^c = \pm 20$ kW with P_{ref} set at ± 60 kW. Figure 4.25

demonstrates the effectiveness of phase balancing control where each phase absorbs or injects an unequal amount of active power. Taking $P_{ref} < 0$ as an example (system is charging), the power handling capability of each phase varies due to SoC variation among the cells. Assuming $\alpha^a < \alpha^b < \alpha^c$ at $t = 0$ s, phase a absorbs the highest amount of active power compared to phase b and phase c , which yields $P_{ref}^a = -36.65$ kW, $P_{ref}^b = -12.59$ kW, $P_{ref}^c = -10.6$ kW as demonstrated in Figure 4.25(b). The total active power remains unaffected where $P_{ref}^a + P_{ref}^b + P_{ref}^c = -60$ kW is observed. In Figure 4.25(c), each of the zero-sequence power component is no longer zero but have the following values: $\Delta P_{ref}^a = -16.71$ kW, $\Delta P_{ref}^b = 7.36$ kW, $\Delta P_{ref}^c = 9.36$ kW, with the zero-sequence power components sum to zero ($\Delta P_{ref}^a + \Delta P_{ref}^b + \Delta P_{ref}^c = 0$).



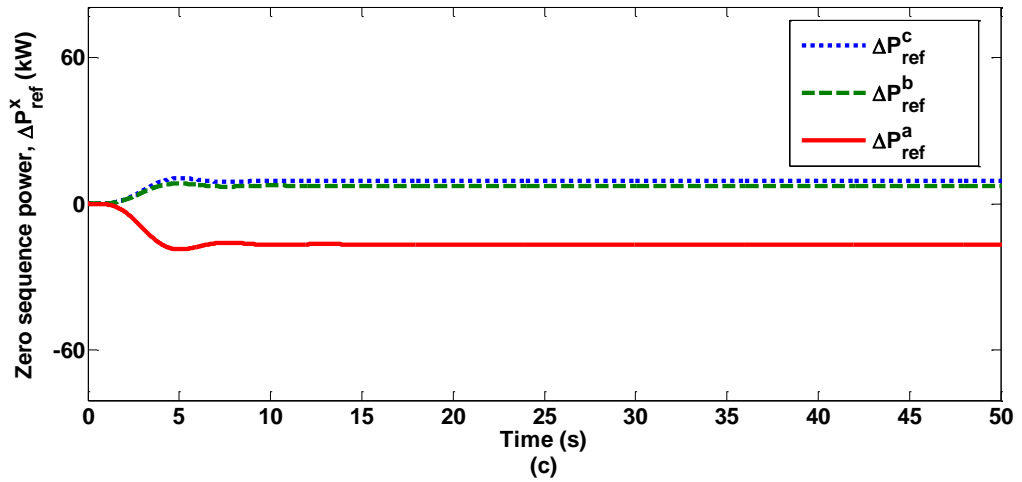
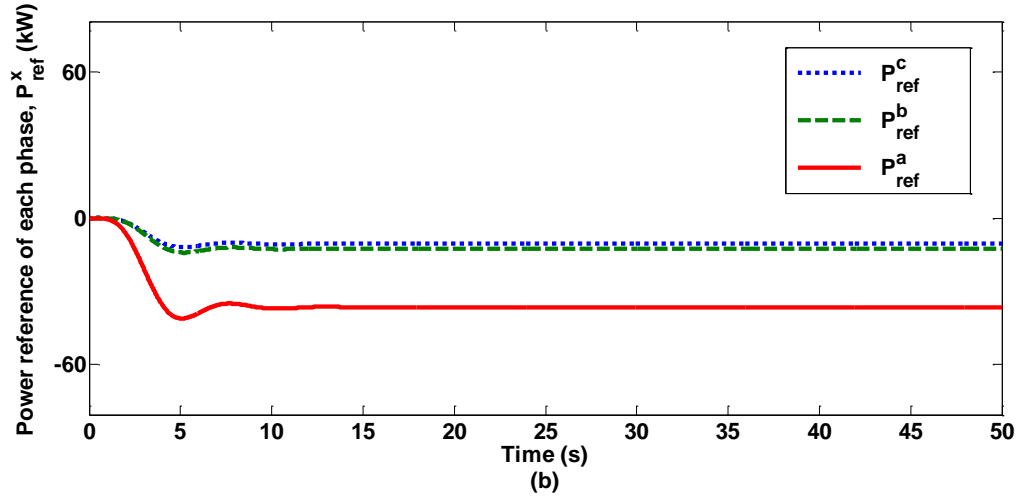


Figure 4.25 (a) System power reference, P_{ref} , (b) power references from the balancing controller, P_{ref}^x , (c) zero-sequence power, ΔP_{ref}^x

4.9 Simulation Results and Discussion

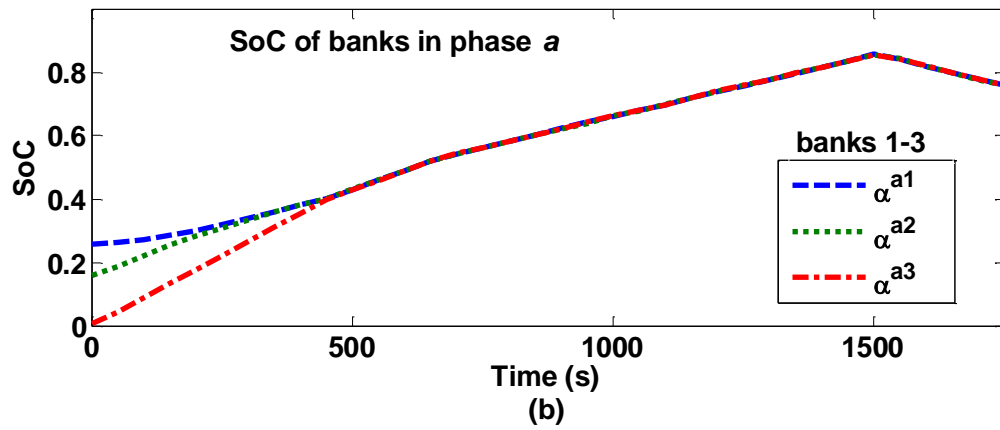
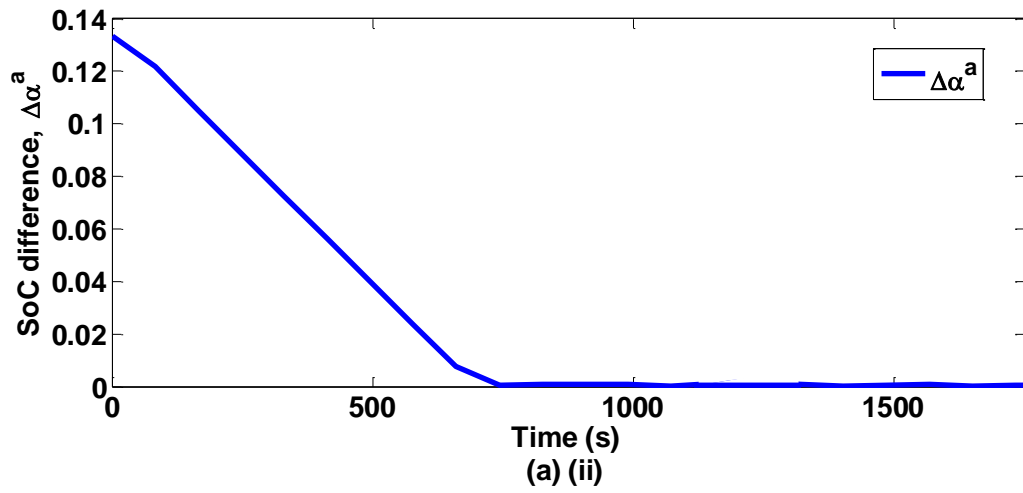
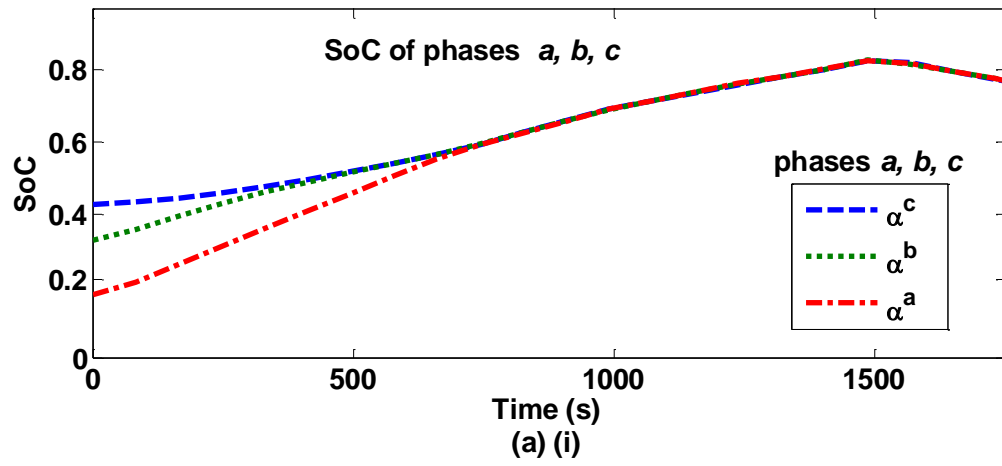
A simulation model with circuit parameters summarised in Table 4.4 was built in MATLAB Simulink to validate the proposed balancing control. In this work, a simple Li-ion cell model shown in Figure 4.13 is used. Multiple cells can be instantiated efficiently using vector implementation where it allows independent setting of important parameters:

α_0 , Q_n and R_{int} . At the start of a simulation, cell parameters are chosen randomly with a uniform distribution in the ranges given in Table 4.4.

The balancing controller is implemented to make SoC equal for maximum utilisation of the proposed BESS. Charge balancing is demonstrated for mismatched cells and the detailed results are demonstrated in Figure 4.26. Before the balancing control takes place, a maximal SoC imbalance of 24 % exists between the highest and lowest cells. When the balancing controller is started at $t = 0$, the SoCs gradually converge. Figure 4.26(a)-(b) presents the SoC of phases a , b and c ($\alpha^a, \alpha^b, \alpha^c$) and SoC of banks (α^{xj} where $x = a; j = 1,2,3$). Figure 4.26(c)-(e) show SoC of sub-banks (α^{xjk} where $x = a; j = 1; k = 1,2,3$), SoC of modules (α^{xjkm} where $x = a; j = 1; k = 1; m = 1,2,3$) and SoC of cells (α^{xjkmn} where $x = a; j = 1; k = 1; m = 1; n = 1,2,3$) respectively. Taking Figure 4.26(a) as an example, the variation of SoC due to the random initial conditions is observed where $\alpha^a < \alpha^b < \alpha^c$ during charging, thus α^a will tend to be charged more rapidly compared to α^b and α^c and this eventually brings SoC convergence at around $t = 750$ s, where all SoCs are effectively balanced. The SoC difference, $\Delta\alpha^a$ was reduced to half of its initial value in 330 s as illustrated in Figure 4.26(a)(ii). When SoC becomes equal, the algorithm causes the demand to be shared among cells proportional to their capacity, ensuring that their SoC decreases/increases at similar rates. It should be noted that the initial SoC distribution illustrated in Figure 4.26 is extreme in the sense that it is highly unlikely cells in a practical BESS would ever exhibit such a wide spread in cell SoC. These values were chosen explicitly to demonstrate the effectiveness of the algorithm at equalising very widely varying SoCs.

Table 4.4 System parameters in MATLAB Simulink

Phase voltage	V_{phase}	2.6 kV
Line current	I	50 A
Power rating	P_{ref}	60 kW
Power factor	pf	0.85
Line inductor	L	2 mH
Sampling frequency	f_s	11 kHz
No. of cells	N	35
No. of modules	M	3
No. of sub-banks	K	3
No. of banks	J	3
Balancing 'strength'	β	30
Total cells	$3NMKJ$	2835
Initial SoC for cells in module $a112$	α_0^{a112}	0.1-0.9
Initial SoC for cells in module $a113$	α_0^{a113}	0.1-0.3
Initial SoC for cells in sub-bank $a12$	α_0^{a12}	0.1-0.3
Initial SoC for cells in sub-bank $a13$	α_0^{a13}	0.2-0.8
Initial SoC for cells in bank $a2$	α_0^{a2}	0.1-0.3
Initial SoC for cells in bank $a3$	α_0^{a3}	0.01-0.03
Initial SoC for cells in phase b	α_0^b	0.2-0.4
Initial SoC for cells in phase c	α_0^c	0.2-0.7
Capacity of cells	Q_n	40-100 Ah
Internal resistance of cells	R_{int}	0.07-0.15 Ω



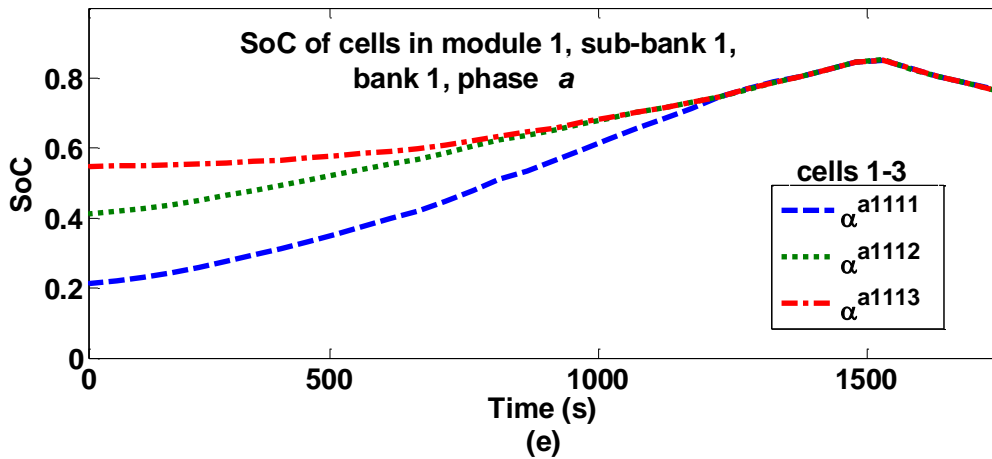
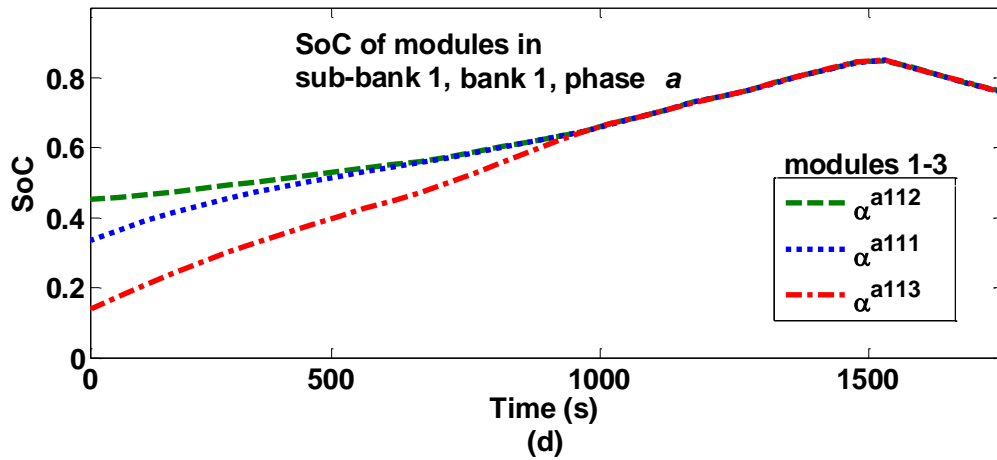
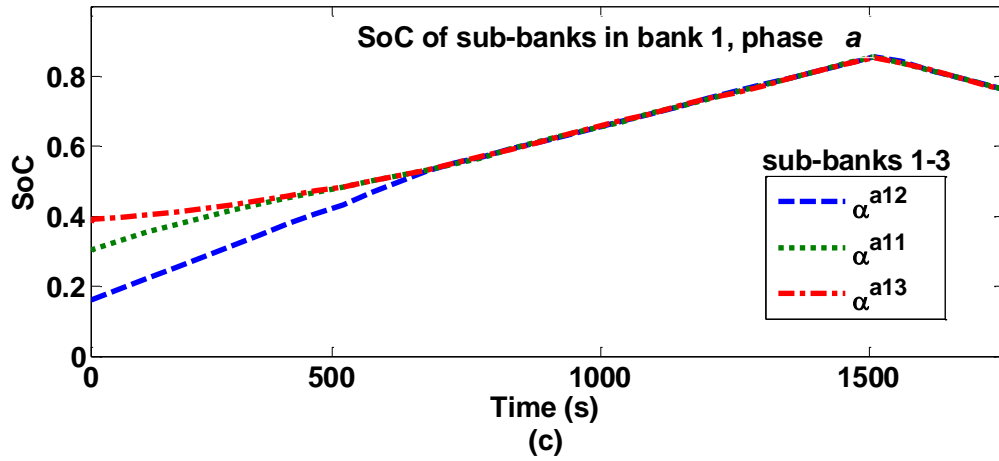


Figure 4.26 (a) (i) Balancing control between phases, (a) (ii) SoC difference between phase *a* and average SoC of three phases, (b) balancing control between banks within phase *a*, (c) balancing control between sub-banks within a bank, (d) balancing control between modules within a sub-bank, and (e) balancing control between cells within a module

CHAPTER 5 MANAGING VOLTAGE CONSTRAINTS USING PEAK SHARING

This chapter introduces an additional step referred to as *peak sharing*, which must be incorporated into the balancing controller described in Chapter 4 so that alternative modules assume a portion of the load when certain modules are not capable of meeting the demand. This is necessary to avoid severely limiting the performance of the system under certain conditions. Using three different scenarios, this chapter demonstrates the effectiveness of peak sharing by exhibiting how it manages voltage constraints.

5.1 Overview of the Control System

The balancing controller as so-far described assumes that all cells possess similar terminal voltages, that all modules can therefore produce similar maximum output voltages, all sub-banks can produce similar maximum output voltages and so forth. However, this assumption is problematic for two main reasons: first, a cell with significantly lower SoC than another will have significantly lower terminal voltage. If one module has many highly discharged cells, it will be unable to produce as high a terminal voltage as a module with mostly fully charged cells. Second, should a cell fail in a particular module (or a module fail within a sub-bank etc.) then the containing module (or sub-bank etc.) would be permanently limited in the output voltage it could provide.

Assuming that system is charging, there are three modules within a sub-bank, module 1 has the lowest average SoC while module 3 has the highest average SoC, i.e. $\alpha^{a111} < \alpha^{a112} < \alpha^{a113}$. When a low β value is used for the balancing controller described in Chapter 4, the reference voltage assigned to the modules is shared more evenly between three modules, thus, each module is less likely to have a reference voltage that is higher

than the maximum voltage available in that module as long as a reasonable system reference voltage is set. For instance, in a scenario where $V_{ref}^{a111} \leq V_{max}^{a111}$, $V_{ref}^{a112} \leq V_{max}^{a112}$ and $V_{ref}^{a113} \leq V_{max}^{a113}$, all cells in the modules are used to form a 49-level output voltage depicted in Figure 5.1(b), which is a close approximation of sinusoidal waveform that can be achieved without peak sharing. The system reference voltage is shown in Figure 5.1(a).

As a high β value tends to assign an extreme amount of reference voltage, module 3 is assigned a reference voltage that is much lower than the maximum voltage available while module 1 is assigned a reference voltage that is much higher than the maximum voltage available, which yields $V_{ref}^{a113} \ll V_{max}^{a113}$ and $V_{ref}^{a111} \gg V_{max}^{a111}$ when system is charging. Thus, only one or two cells (not all cells) in module 3 are required to switch on as the V_{ref}^{a113} is much lower than the maximum voltage available in module 3. On the contrary, all cells in module 1 are switched on to produce an output voltage that is still lower than the requested V_{ref}^{a111} . Consequently, fewer cells (instead of all 24 cells in the low β value setting in Figure 5.1(b)) are used to form the total output voltage as illustrated in Figure 5.1(c). The number of steps is not enough to follow the sine wave reference voltage, and so the output voltage is distorted (the peaks are ‘clipped’).

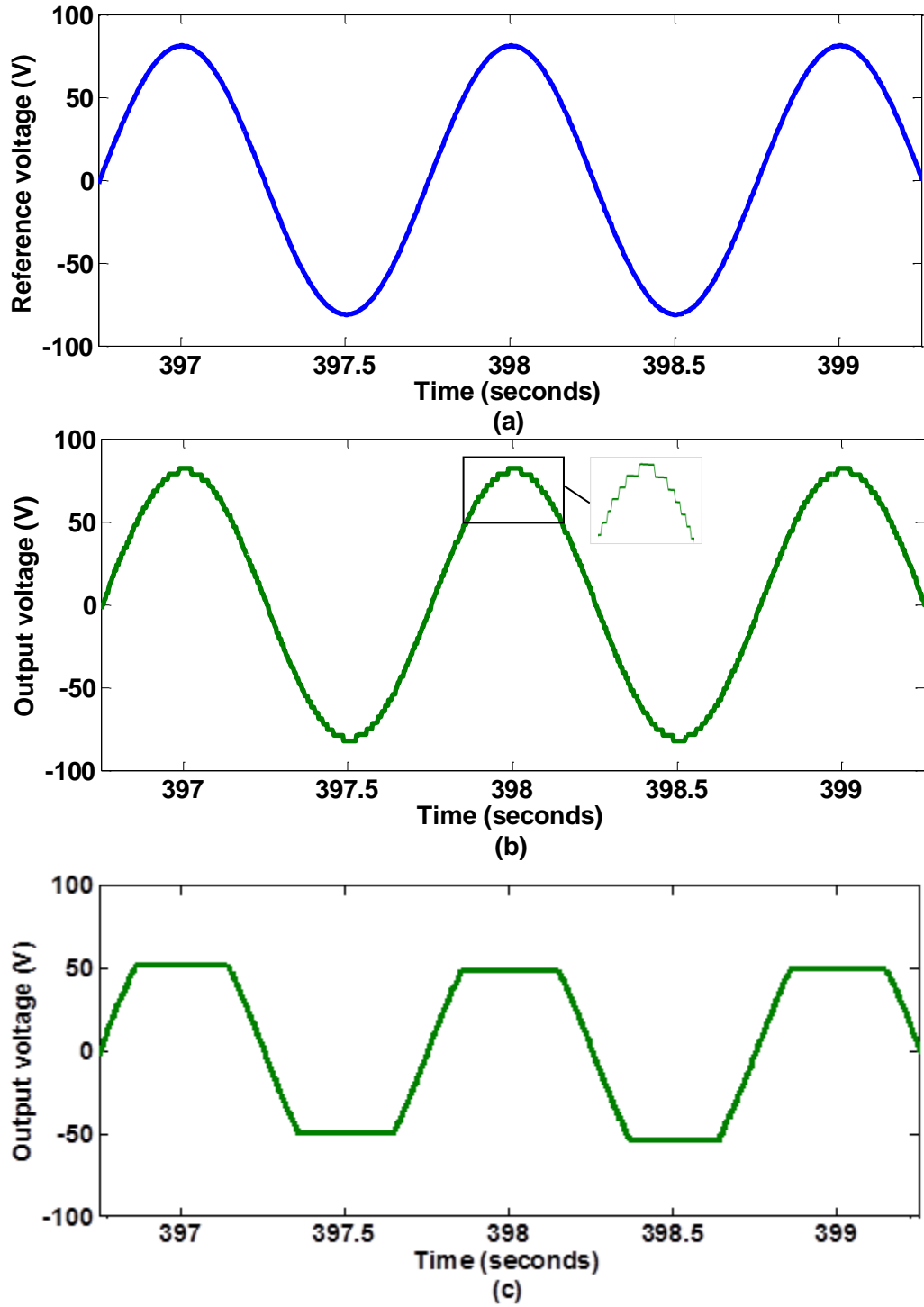


Figure 5.1 (a) System reference voltage, (b) output voltage when a low β value is used without peak sharing, (c) output voltage when a high β value is used without peak sharing

To avoid severely limiting the performance of the proposed system described in Chapter 4 under the conditions described above, an additional step referred to as peak sharing must be incorporated into the balancing controller algorithm. Peak sharing ensures the reference voltage requested from each module (or sub-bank etc.) is limited by the maximum available voltage at all times.

Taking, for example, sub-banks within a bank, the control algorithm is expressed as a pseudocode in Figure 5.2. and functions as follows: let ΔV^{xjk} be the voltage difference between the maximum voltage available of sub-bank k in bank j and phase x , V_{max}^{xjk} and the requested reference voltage, V_{ref}^{xjk} obtained from Chapter 4. ΔV^{xjk} can take a negative, zero or positive value. The negative differences are summed to give a total excessive voltage, v_- that cannot be met by the system without intervention. This voltage must be shared between the sub-banks that have a positive difference since these sub-banks have the voltage ‘available’ because their reference voltages are less than their maximum output voltages.

The negative difference sum, v_- is shared between all sub-banks with positive ΔV^{xjk} . The positive differences are summed to give a total voltage, v_+ . Each sub-bank is allocated a portion of v_- which is proportional to its ΔV^{xjk} compared with v_+ . This additional voltage is added to the existing reference voltage, V_{ref}^{xjk} , to give a new reference voltage, $V_{ref,new}^{xjk}$. If the $V_{ref,new}^{xjk}$ is now higher than V_{max}^{xjk} , the requested reference voltage should be limited to V_{max}^{xjk} . For all the sub-banks with negative or zero ΔV^{xjk} , the requested reference voltage ($V_{ref,new}^{xjk}$) is now set to V_{max}^{xjk} . This procedure ensures no sub-bank is required to supply more than its maximum voltage as long as the bank reference voltage is less than or equal to the sum of all sub-bank maximum voltages.

```

begin Calculate excessive voltage and total voltage difference of sub-banks
with voltage available
initialize  $v_- \leftarrow 0$ ;  $v_+ \leftarrow 0$ 
for  $k \leftarrow 1$  to  $K$  do
     $\Delta V^{xjk} \leftarrow V_{max}^{xjk} - V_{ref}^{xjk}$ 
    if  $\Delta V^{xjk} < 0$  then  $v_- \leftarrow v_- + \Delta V^{xjk}$ 
    endif
    if  $\Delta V^{xjk} > 0$  then  $v_+ \leftarrow v_+ + \Delta V^{xjk}$ 
    endif
endfor
end Calculate excessive voltage and total voltage difference of sub-banks with
voltage available

begin Redistribute reference voltages
for  $k \leftarrow 1$  to  $K$  do
    if  $\Delta V^{xjk} > 0$  then  $V_{ref,new}^{xjk} \leftarrow V_{ref}^{xjk} + \frac{\Delta V^{xjk}}{v_+} |v_-|$ 
        if  $V_{ref,new}^{xjk} > V_{max}^{xjk}$  then  $V_{ref,new}^{xjk} \leftarrow V_{max}^{xjk}$ 
        endif
    else  $V_{ref,new}^{xjk} \leftarrow V_{max}^{xjk}$ 
    endif
endfor
end Redistribute reference voltages

```

Figure 5.2 Pseudocode: Peak sharing algorithm

5.2 Scenario I: Two Modules with a Negative Voltage Difference and One Module with a Positive Voltage Difference

Taking, for example, three modules within a sub-bank; modules 1 and 2 have a negative voltage difference while module 3 has a positive voltage difference. In Figure 5.3(a) and Figure 5.4(a), it can be observed that module 1 and module 2 are assigned a reference voltage that is higher than the maximum voltage available in the module, i.e. $V_{ref}^{a111} > V_{max}^{a111}$ and $V_{ref}^{a112} > V_{max}^{a112}$, where existing reference voltage is represented by a dash-dot line and maximum voltage is indicated with a dash line. These reference voltages are obtained from the balancing controller demonstrated in Chapter 4. Peak sharing works to distribute the additional voltage from these modules (modules 1 and 2) to module 3 that is able to assume the additional load since $V_{ref}^{a113} < V_{max}^{a113}$, which can be observed in Figure 5.5(a).

First, the voltage difference between the existing reference voltage and maximum voltage available is obtained for all modules using (5.1).

$$\begin{cases} \Delta V^{a111} = V_{max}^{a111} - V_{ref}^{a111} \\ \Delta V^{a112} = V_{max}^{a112} - V_{ref}^{a112} \\ \Delta V^{a113} = V_{max}^{a113} - V_{ref}^{a113} \end{cases} \quad (5.1)$$

The additional voltage needed to be distributed is the sum of the negative voltage difference from modules 1 and 2 indicated in (5.2). The positive voltage difference is only contributed by module 3 in this scenario.

$$\begin{cases} v_- = \Delta V^{a111} + \Delta V^{a112} \\ v_+ = \Delta V^{a113} \end{cases} \quad (5.2)$$

Modules 1 and 2 are not able to meet the existing reference voltage assigned to them, so they are assigned a new reference voltage that is equal to the maximum voltage

available in each of the modules indicated in (5.3). Module 3 now would have to assume an additional load of v_- in order for all three modules to meet the total system reference voltage.

$$\begin{cases} V_{ref,new}^{a111} = V_{max}^{a111} \\ V_{ref,new}^{a112} = V_{max}^{a112} \\ V_{ref,new}^{a113} = V_{ref}^{a113} + |v_-| \end{cases} \quad (5.3)$$

It is important to note that, if the $V_{ref,new}^{a113}$ is now higher than V_{max}^{a113} , the requested reference voltage should be limited to V_{max}^{a113} . The output voltage of each module (V_{out}^{a111} , V_{out}^{a112} , V_{out}^{a113}) now can be made to follow the newly assigned sinusoidal reference voltage as can be seen in Figure 5.3(b), Figure 5.4(b) and Figure 5.5(b). The additional load assumed by module 3 results in module 3 having $V_{ref,new}^{a113}$ that is higher than the existing reference voltage V_{ref}^{a113} but less than or equal to its maximum available voltage. Peak sharing also ensures that the total new reference voltage always matches the total value of the existing reference voltage.

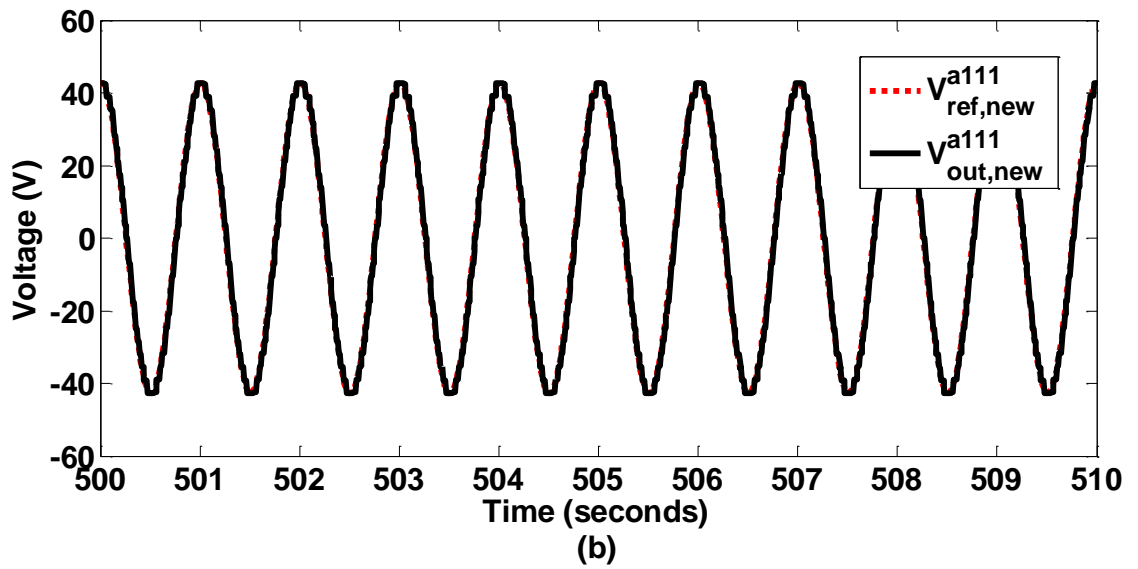
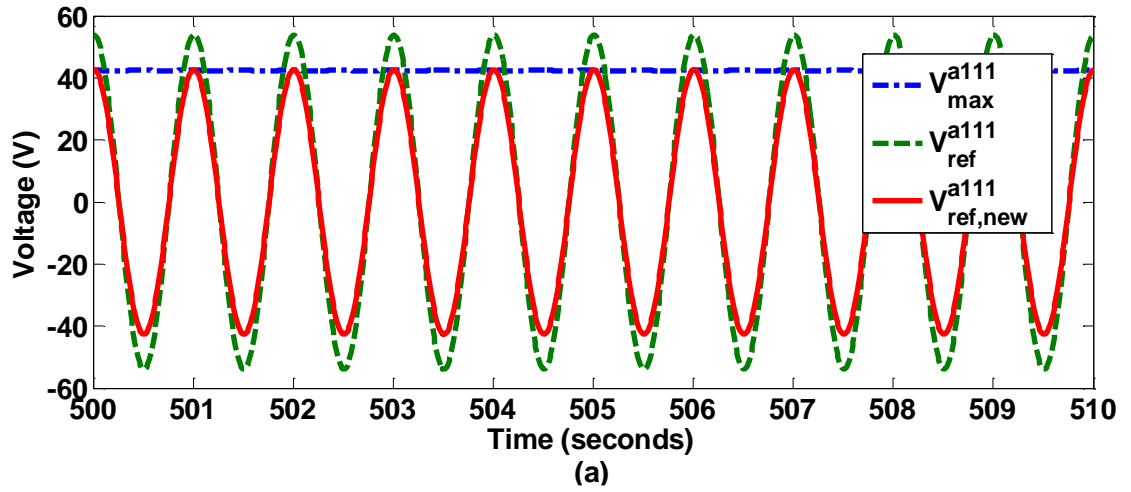


Figure 5.3 Module 1 with negative voltage difference: (a) maximum available voltage, existing reference voltage and new reference voltage, (b) output voltage

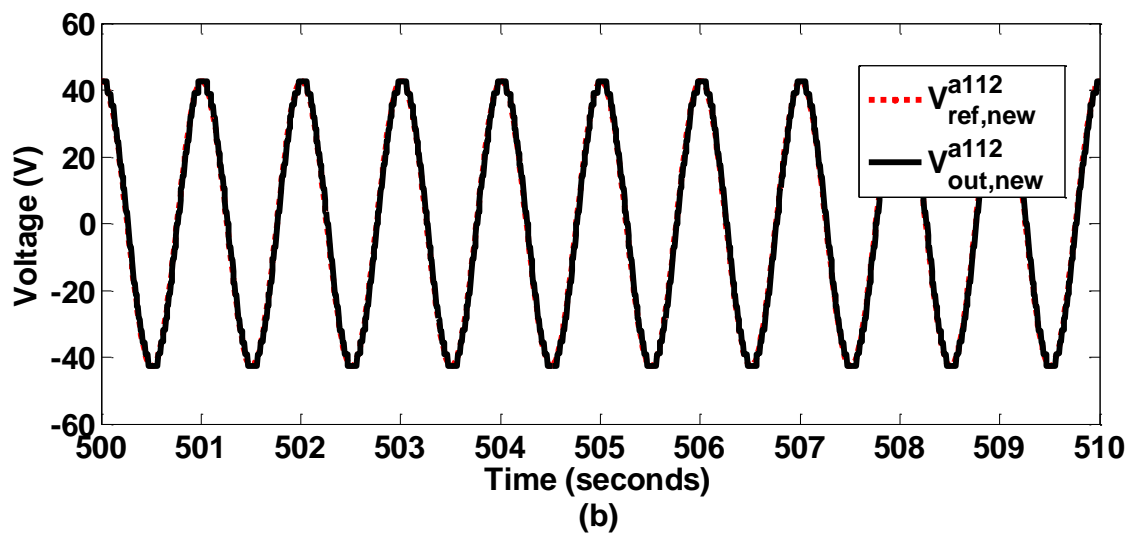
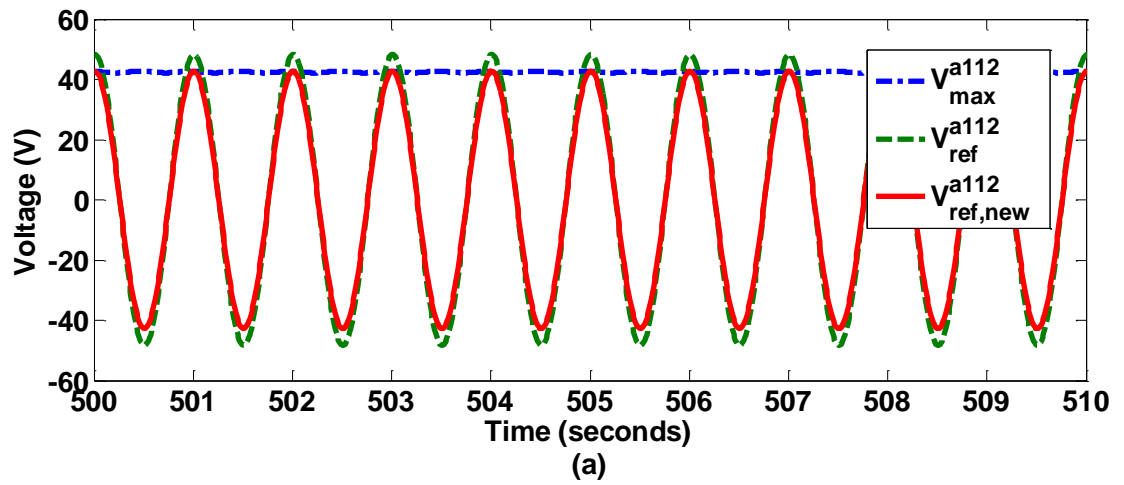


Figure 5.4 Module 2 with negative voltage difference: (a) maximum available voltage, existing reference voltage and new reference voltage, (b) output voltage

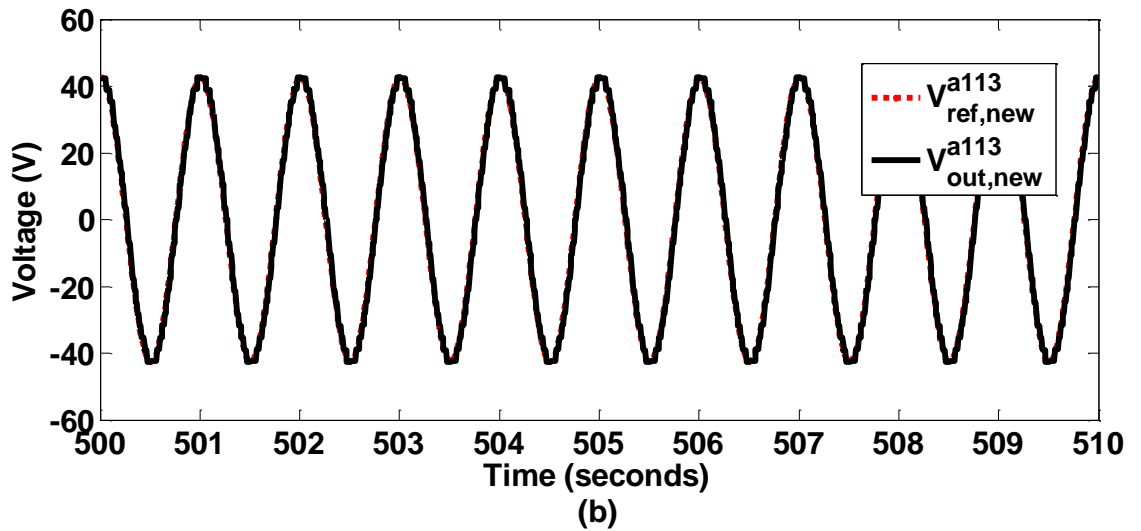
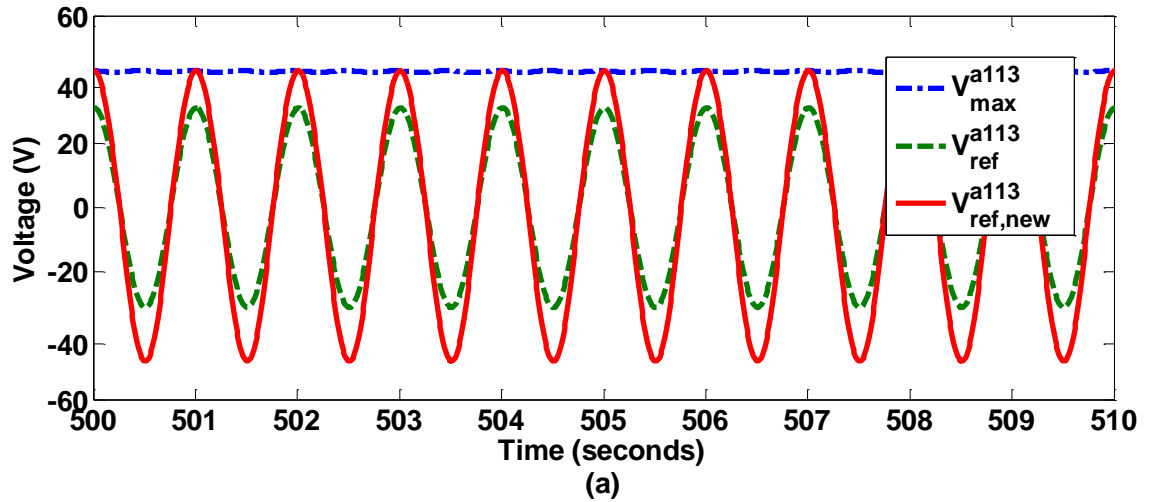


Figure 5.5 Module 3 with positive voltage difference: (a) maximum available voltage, and existing and new reference voltage, (b) output voltage

The presence of a ripple component of V_{max}^{a111} shown in Figure 5.6 can be explained via a simplified cell model illustrated in Figure 5.7, the detailed cell model has been presented in Chapter 4. The system is charging during $500 < t < 510$ s (current flows into the cell as indicated by arrows in Figure 5.6) which causes increase in cell voltage equal to IR as indicated in (5.4). This increase occurs across all cells in the load current path and produces a maximum value of V_{max}^{a111} corresponding to peaks in the load.

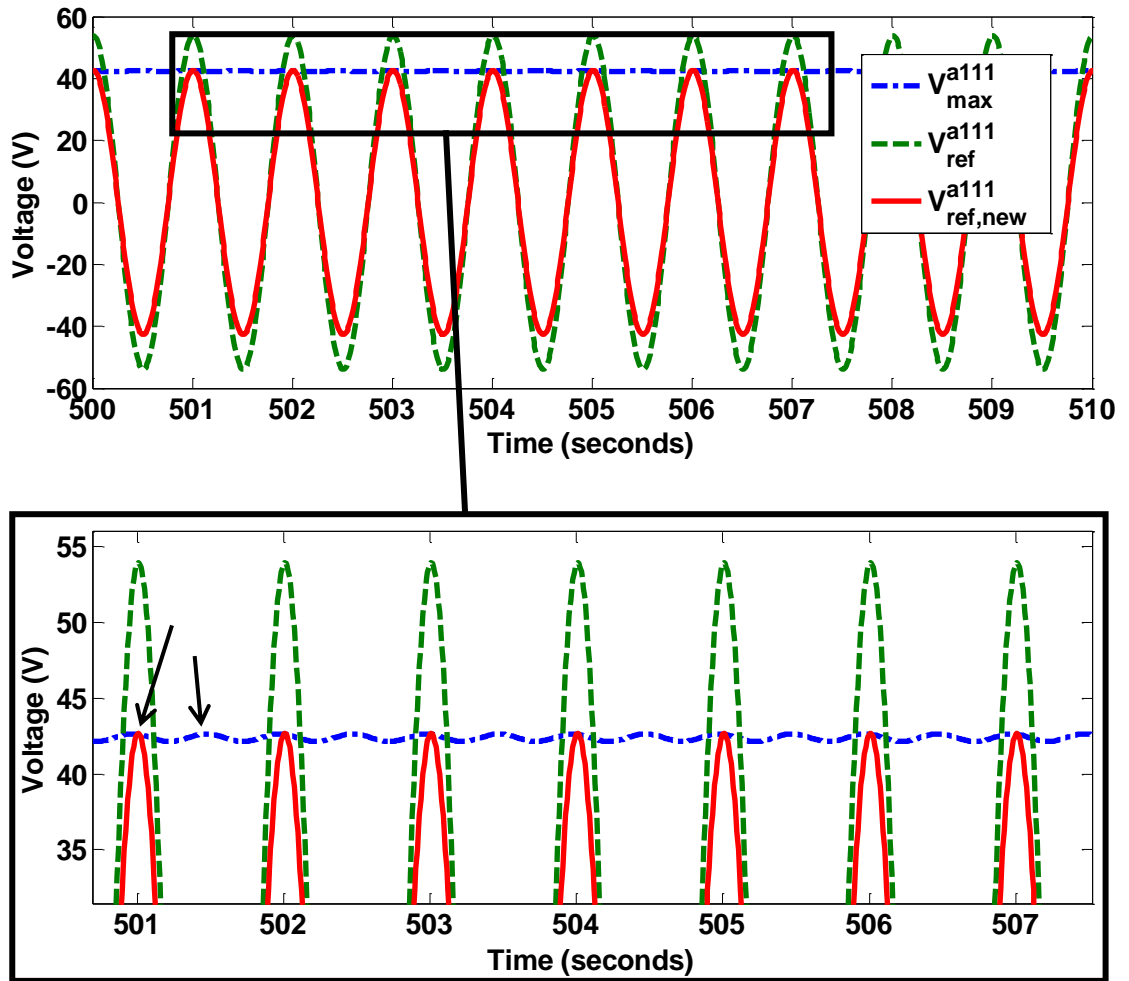


Figure 5.6 V_{max}^{a111} oscillation during charging

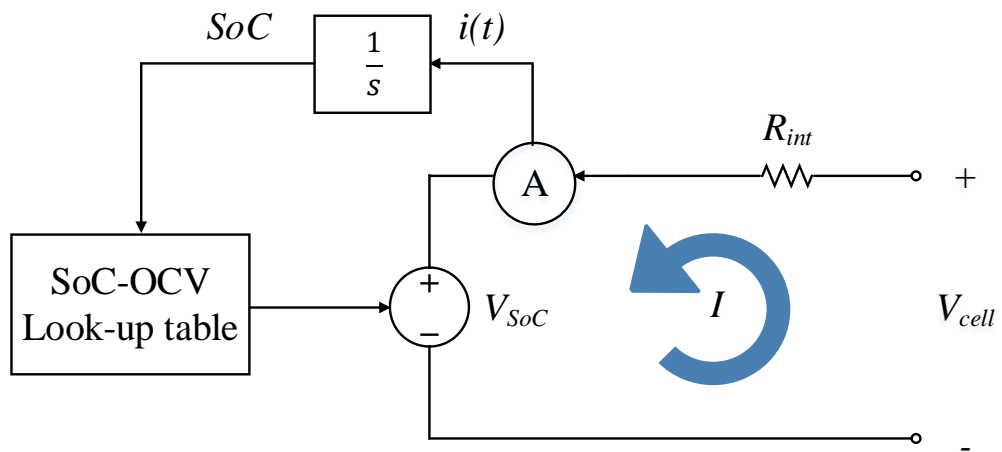


Figure 5.7 Simplified cell model during charging

$$V_{cell} = V_{SoC} + IR \quad (5.4)$$

5.3 Scenario II: One Module with a Negative Voltage Difference and Two Modules with a Positive Voltage Difference

Taking, for example, three modules within a sub-bank, modules 1 and 2 have a positive voltage difference while module 3 has a negative voltage difference. In Figure 5.8(c), it can be observed that module 3 is assigned a reference voltage that is higher than the maximum voltage available in the module, i.e. $V_{ref}^{a113} > V_{max}^{a113}$. Therefore, as illustrated in Figure 5.8(a) and Figure 5.8(b), peak sharing is necessary to distribute the additional voltage from module 3 to modules 1 and 2 (instead of just one module as in scenario I) that are able to assume the additional load since $V_{ref}^{a111} < V_{max}^{a111}$ and $V_{ref}^{a112} < V_{max}^{a112}$.

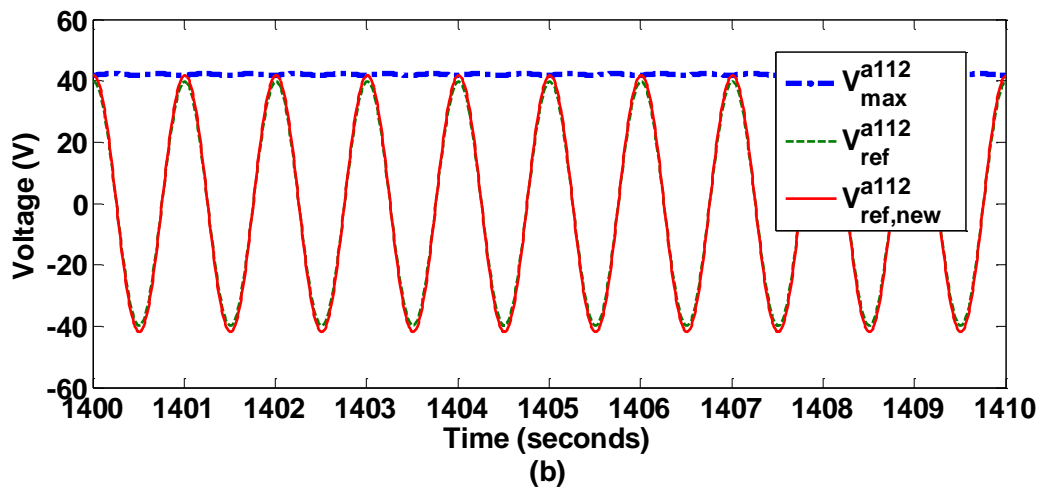
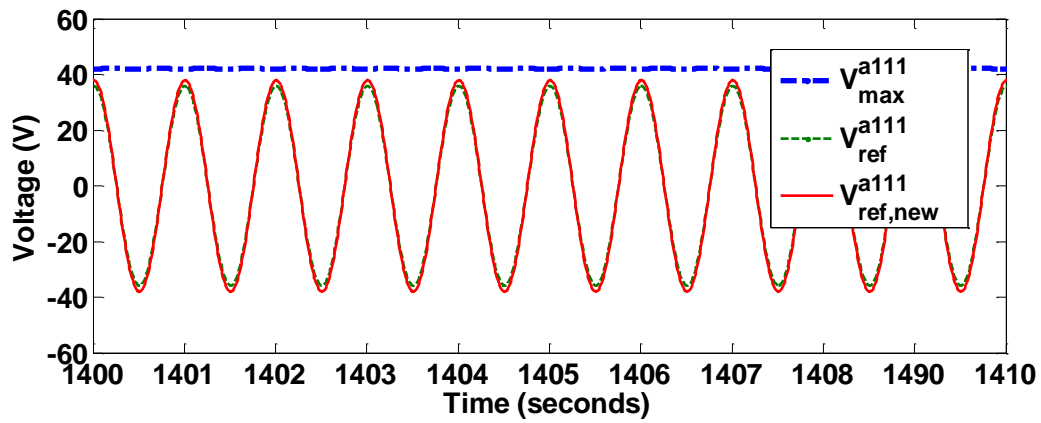
The voltage difference between the existing reference voltage and the maximum voltage available can be obtained using (5.1). The amount of voltage that must be distributed is just the negative voltage difference from module 3 indicated in (5.5), which is to be shared between modules 1 and 2.

$$\begin{cases} v_- = \Delta V^{a113} \\ v_+ = \Delta V^{a111} + \Delta V^{a112} \end{cases} \quad (5.5)$$

In (5.6), modules 1 and 2 assume an additional load which is a portion of v_- that is proportional to ΔV^{a111} and ΔV^{a112} respectively compared with v_+ , where v_+ is the total positive voltage difference from modules 1 and 2. This additional voltage is added to the existing reference voltages, V_{ref}^{a111} and V_{ref}^{a112} , to yield new reference voltages to both modules, $V_{ref,new}^{a111}$ and $V_{ref,new}^{a112}$. The system proceeds to check and ensure that the requested reference voltages, $V_{ref,new}^{a111}$ and $V_{ref,new}^{a112}$ does not exceed V_{max}^{a111} and V_{max}^{a112} respectively.

Meanwhile, in (5.6), module 3 is assigned an updated reference voltage that is equal to the maximum available voltage.

$$\begin{cases} V_{ref,new}^{a111} = V_{ref}^{a111} + \frac{\Delta V^{a111}}{v_+} |v_-| \\ V_{ref,new}^{a112} = V_{ref}^{a112} + \frac{\Delta V^{a112}}{v_+} |v_-| \\ V_{ref,new}^{a113} = V_{max}^{a113} \end{cases} \quad (5.6)$$



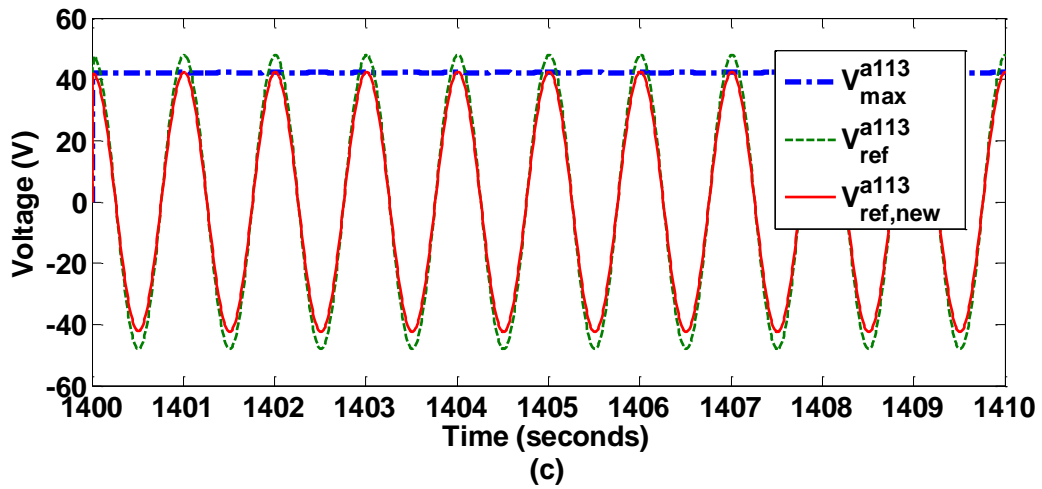


Figure 5.8 (a) Module 1 with positive voltage difference, (b) module 2 with positive voltage difference, and (c) module 3 with negative voltage difference

A simplified cell model when a cell is discharging is illustrated in Figure 5.9. System is discharging during $1400 < t < 1410$ s in Figure 5.10. A maximum increase of IR occurs when a cell is conducting the peak current, resulting in a minimum value of V_{cell} in (5.7), which then contributes to the minimum value of V_{max}^{a111} during peak current indicated by arrows in Figure 5.10.

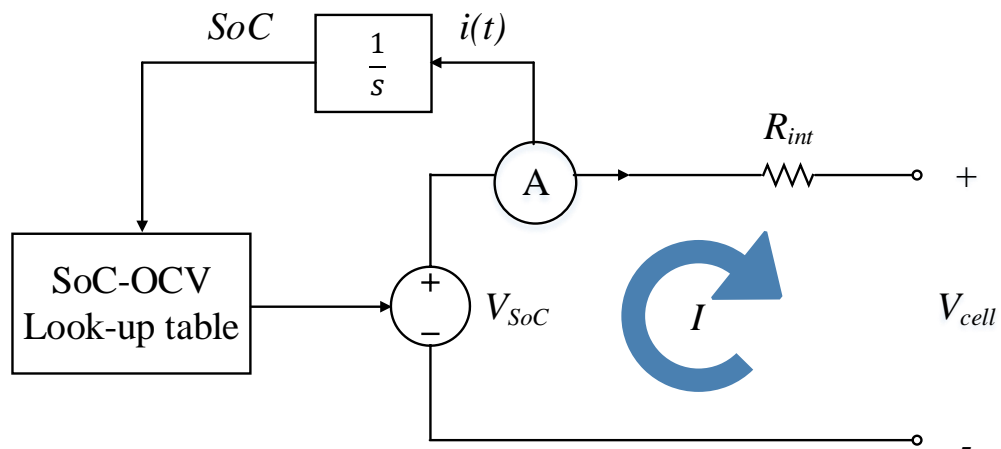


Figure 5.9 Simplified cell model during discharging

$$V_{cell} = V_{SoC} - IR \quad (5.7)$$

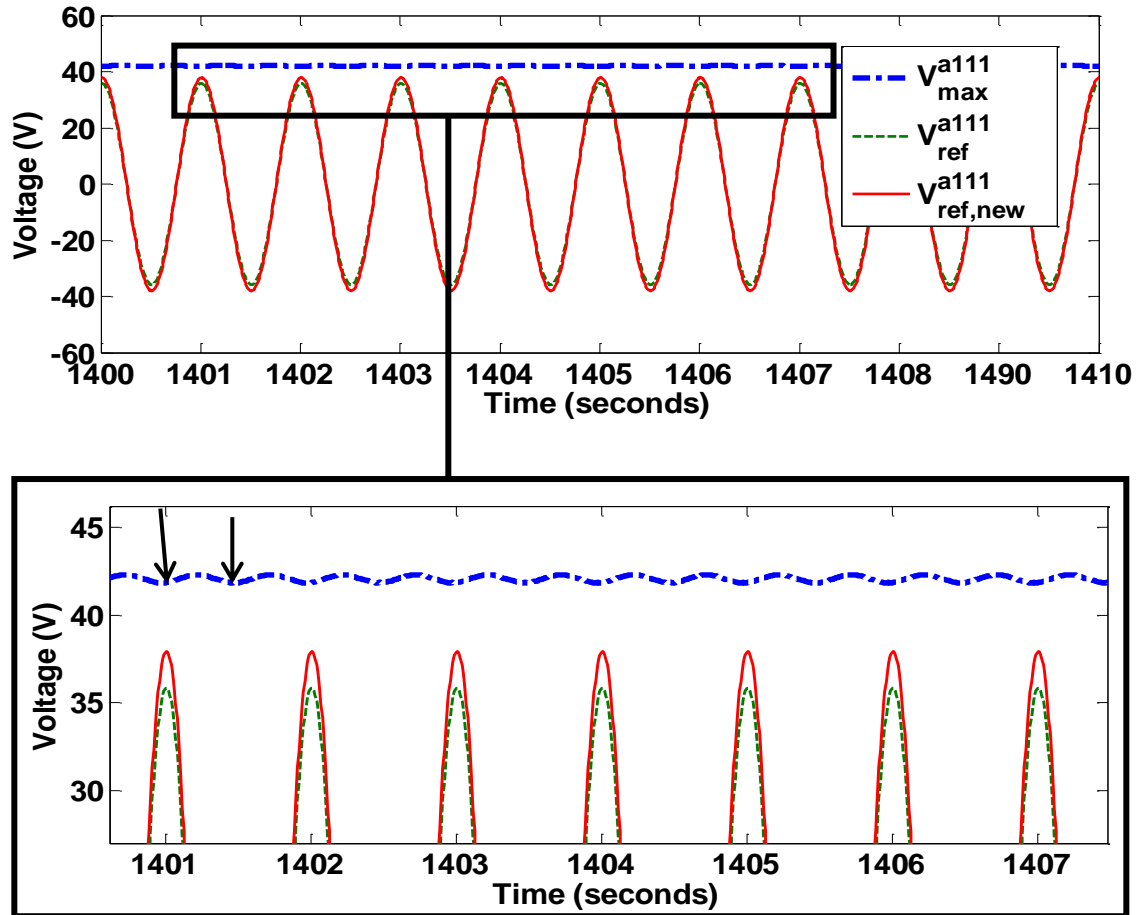


Figure 5.10 V_{max}^{a111} oscillation during discharging

5.4 Scenario III: One Module with a Negative Voltage Difference, One Module with a Zero Voltage Difference, and One Module with a Positive Voltage Difference

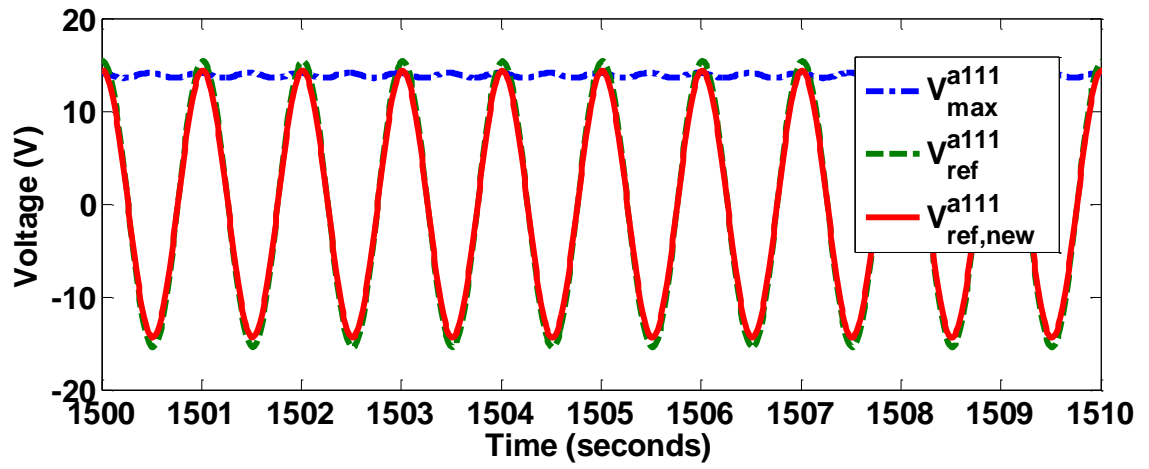
In this scenario, module 1 was assigned a reference voltage that is higher than the maximum voltage available in the modules, i.e. $V_{ref}^{a111} > V_{max}^{a111}$, thus, it has a negative voltage difference. The existing reference voltage for module 2 meets the maximum available voltage, i.e. $V_{ref}^{a112} = V_{max}^{a112}$, which yields a zero voltage difference shown in (5.8).

$$\begin{cases} v_- = \Delta V^{a111} \\ v_+ = \Delta V^{a113} \\ \Delta V^{a112} = 0 \end{cases} \quad (5.8)$$

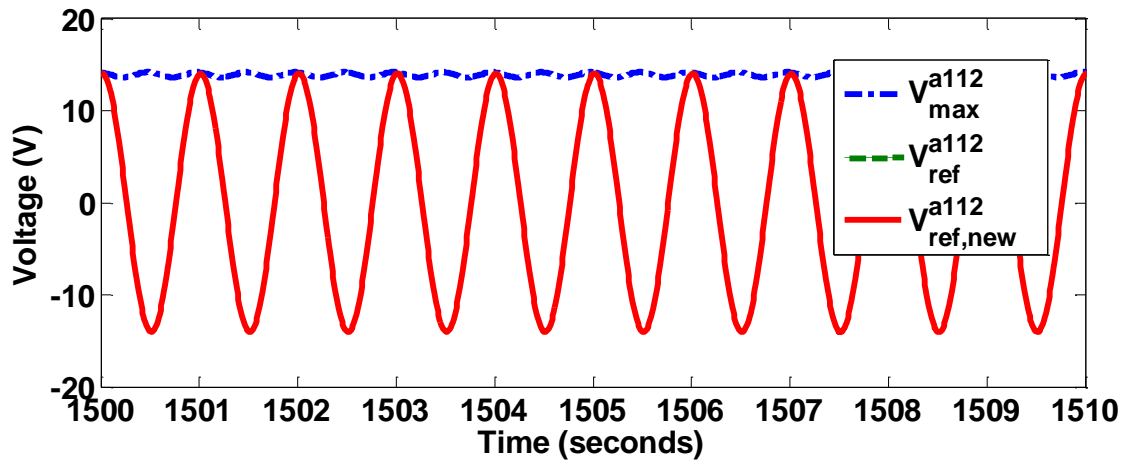
Therefore, peak sharing algorithm works to distribute the additional voltage, v_- from module 1 to module 3 while maintaining the existing reference voltage for module 2. Module 1 is now assigned a new reference voltage that is equal to the maximum available voltage. As long as the new reference voltage assigned to module 3 does not exceed V_{max}^{a113} , $V_{ref,new}^{a113}$ obtained from (5.9) is used. The corresponding voltage waveforms for all three modules are demonstrated in Figure 5.11.

$$\begin{cases} V_{ref,new}^{a111} = V_{max}^{a111} \\ V_{ref,new}^{a112} = V_{ref}^{a112} = V_{max}^{a112} \\ V_{ref,new}^{a113} = V_{ref}^{a112} + |v_-| \end{cases} \quad (5.9)$$

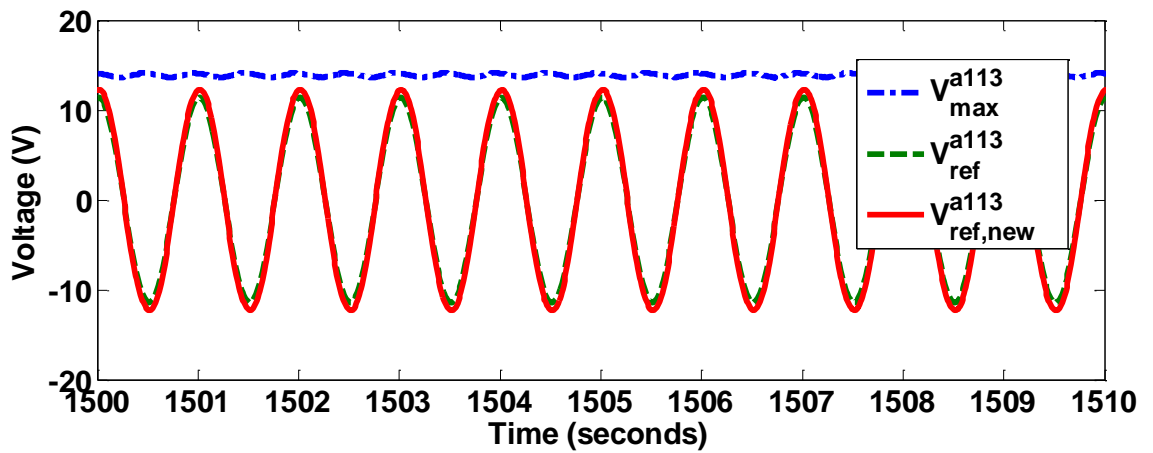
Although the peak sharing concept is demonstrated using only three modules, it is conceptually straightforward to be applied to any number of modules using the control algorithm illustrated in Figure 5.2.



(a)



(b)



(c)

Figure 5.11 a) Module 1 with negative voltage difference, (b) module 2 with zero voltage difference, and (c) module 3 with positive voltage difference

CHAPTER 6 EXPERIMENTAL SYSTEM

This chapter presents a down-scaled experimental BESS to validate the hierarchical balancing control and peak sharing algorithm in the simulation work demonstrated in Chapter 4 and Chapter 5. Experimental set-up, system configuration and key results of the experimental system will be presented and discussed.

6.1 Experimental Set-up

An experimental battery test bench shown in Figure 6.1 has been established to validate the performance of the SoC balancing control, for mainly three ideas: balancing of cells within a module, balancing of modules and peak sharing. Figure 6.2 gives a high-level overview of the experimental BESS control system and its connection to the grid. NiMH cells are electrically interfaced to the grid by the cascaded H-bridge multi-level converter. In this first prototype system, NiMH is chosen as it has good abuse tolerance where it can be exposed to light overcharge conditions without permanent cell damage [222].

The experimental system consists of a master board and two module boards as slaves. The master board is connected to two battery modules, consisting of twelve Ansmann NiMH cells connected in series in each module. Each H-bridge is connected to a single NiMH cell. Each NiMH cell has a nominal voltage of 1.2 V and nominal capacity of 8500 mAh (see Appendix E for details). The main specifications of the NiMH cell are listed in Table 6.1. The nominal voltage of the BESS is $(1.2\text{ V} \times 12\text{ cells} \times 2\text{ modules} = 28.8\text{ V})$. The operating voltage of the BESS may range from 21.6 V to 36 V.

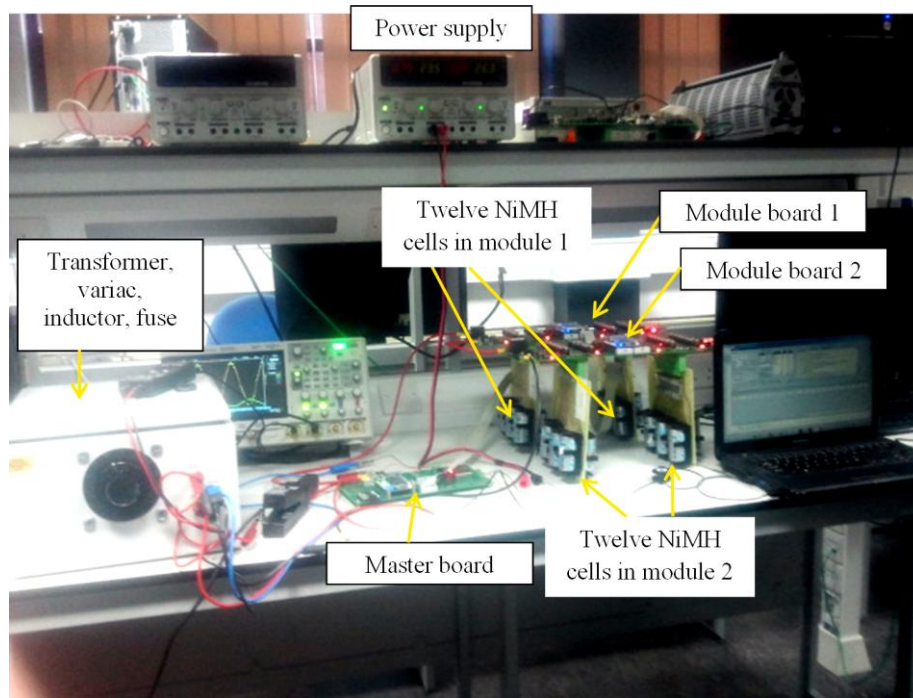


Figure 6.1 Experimental set-up showing main components

Table 6.1 Main specifications of each NiMH cell

Nominal voltage	Nominal capacity	Maximum charged voltage	Cut-off voltage	Internal resistance
1.2 V	8500 mAh	1.5 V	0.9 V	15 mΩ

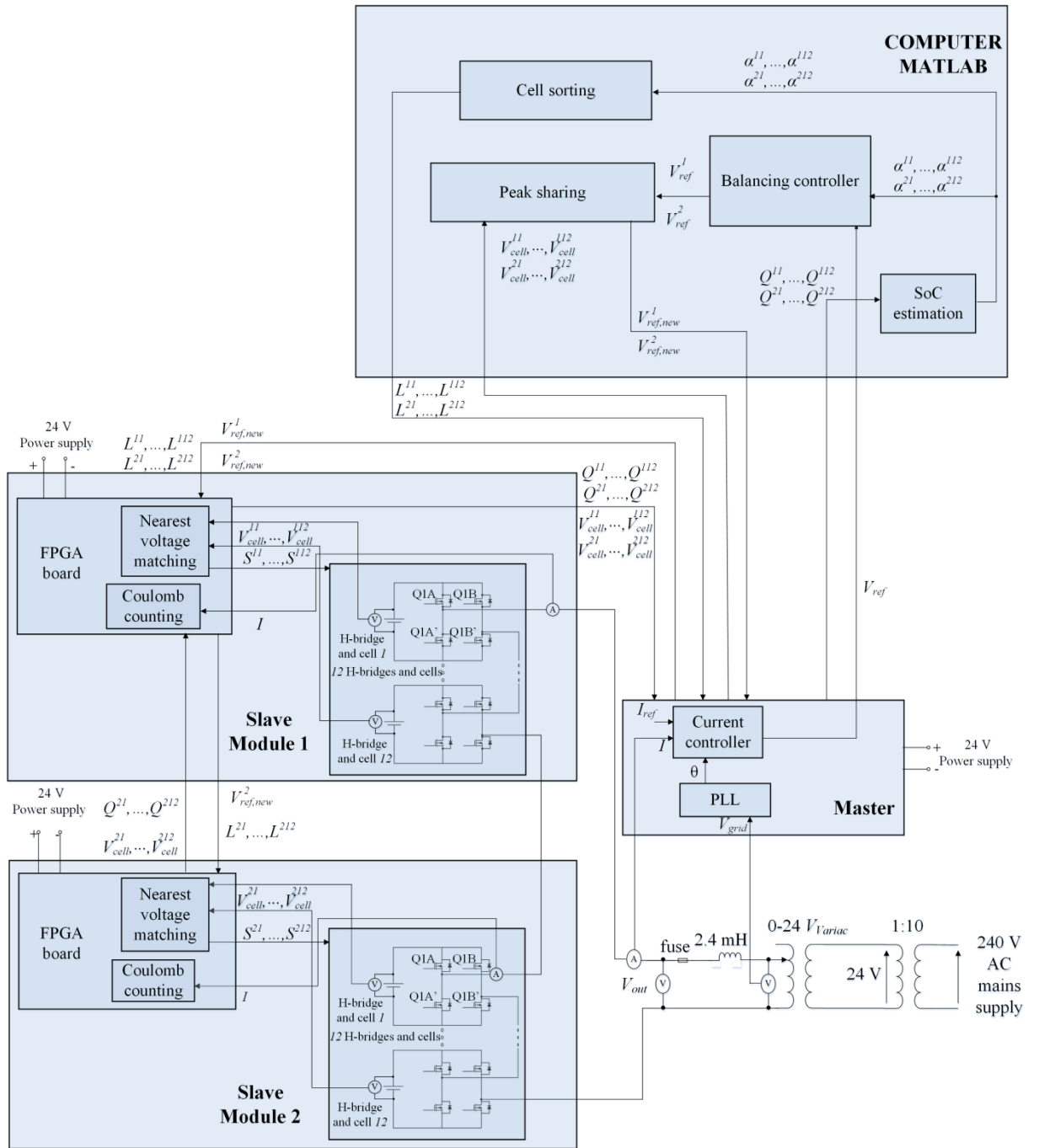


Figure 6.2 System overview showing electrical and control system interconnections

The master controller implements closed-loop control of the AC current to produce the desired AC power. It performs SoC balancing control by adjusting the duty cycle of each slave based on the SoC estimation from each slave. The communication channels to each slave are isolated from each other as the slaves are cascaded. This two-module BESS can charge from and discharge to the mains supply, where it is connected to a single-phase 240-V, 50 Hz line through a 10:1 step-down transformer to achieve the desired voltage. The inverter stages are connected in series where two slaves share the same current, thus, AC voltage of each stage determines the power drawn from each slave. Several tools are used to set up this experiment. VHSIC (Very High Speed Integrated Circuit) Hardware Description Language (VHDL) is used as the hardware description language in the Altera Quartus II system and Terasic Cyclone IV E on Altera DE0-Nano development board is chosen as the field-programmable gate array (FPGA) device. Balancing control algorithm is developed in MATLAB to read, write, analyse and visualise data collected from the hardware system which is connected to a computer running MATLAB. The balancing control algorithm can be found in Appendix F.

The complete control of the experimental system is illustrated in Figure 6.2. In the master controller, PLL is used to synchronise with the angle of the grid voltage, θ . The current controller consists of two PI controllers to control the d and q components of cell current. The d component is set to the desired charging/discharging current while the q component is set to zero to yield output with unity power factor. The output of the PI controllers corresponds to the d and q components of the reference voltage. Applying reverse Park transformation, V_{ref} is obtained which serves as the input to the balancing controller developed in MATLAB. The balancing controller attempts to equalise SoC of

two modules by distributing the reference voltage for each module in proportion (or in negative proportion) to each module's SoC deviation from the average SoC of both modules, depending on whether the system is discharging (or charging). The module's reference voltage is indicated by V_{ref}^m in Figure 6.2, m represents module, where $m = 1, 2$. The SoC of each cell in module m ($\alpha^{m1}, \dots, \alpha^{m12}$) is estimated in MATLAB using Coulomb counting where charge transferred in or out of each cell (Q^{m1}, \dots, Q^{m12}) is sent from each slave to master controller. These SoCs are used to sort cells within the module in descending (or ascending) depending on whether the system is discharging (or charging).

Twelve 12-bit analog-to-digital converters are mounted on each slave to provide voltage measurement of the cells ($V_{cell}^{m1}, \dots, V_{cell}^{m12}$). These measurements are fed to the FPGA board on the slave where the nearest voltage matching algorithm is implemented. The cell voltages together with the reference voltage of each slave obtained from balancing controller (V_{ref}^m) are needed in implementing peak sharing. The updated reference voltages obtained in peak sharing ($V_{ref,new}^1, V_{ref,new}^2$) are sent to master controller where these voltages are required by the nearest voltage matching algorithm in each slave to generate the gate driving signals of the MOSFET switching devices (S^{m1}, \dots, S^{m12}) based on the sorting list obtained from the master controller (L^{m1}, \dots, L^{m12}). The authors in [418-419] have contributed to the hardware development.

Figure 6.3(a) depicts the reference voltage waveform obtained from the current controller (V_{ref} in Figure 6.2). Figure 6.3(b) shows the output voltage waveform measured at the cascaded H-bridge multi-level converter terminals (V_{out} in Figure 6.2) while Figure 6.3(c) illustrates the current waveform (I in Figure 6.2). A 49-level output phase voltage

waveform can be obtained, thus, producing a near sinusoidal output, and resulting in very low voltage total harmonic distortion.

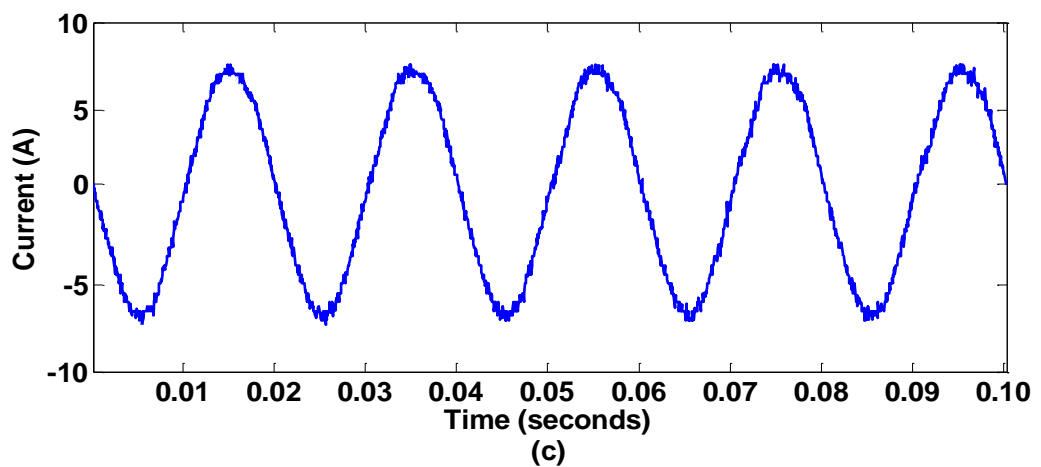
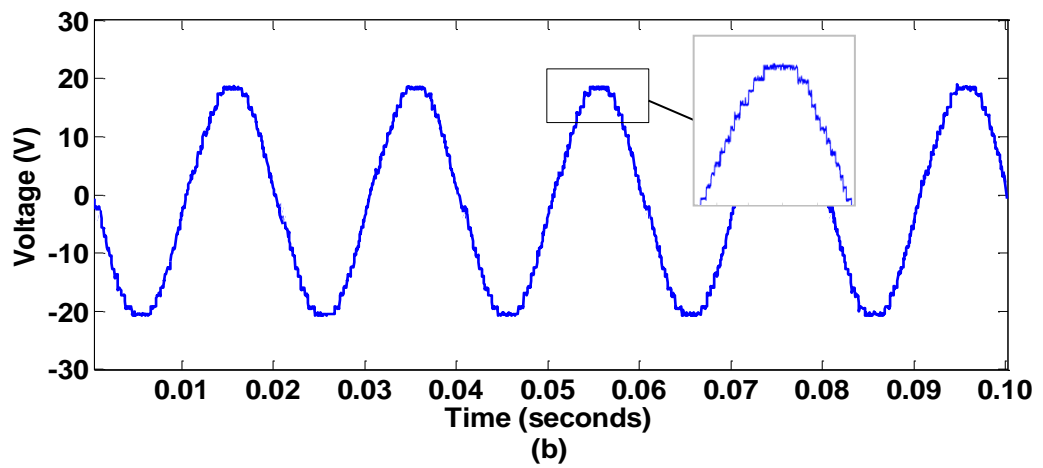
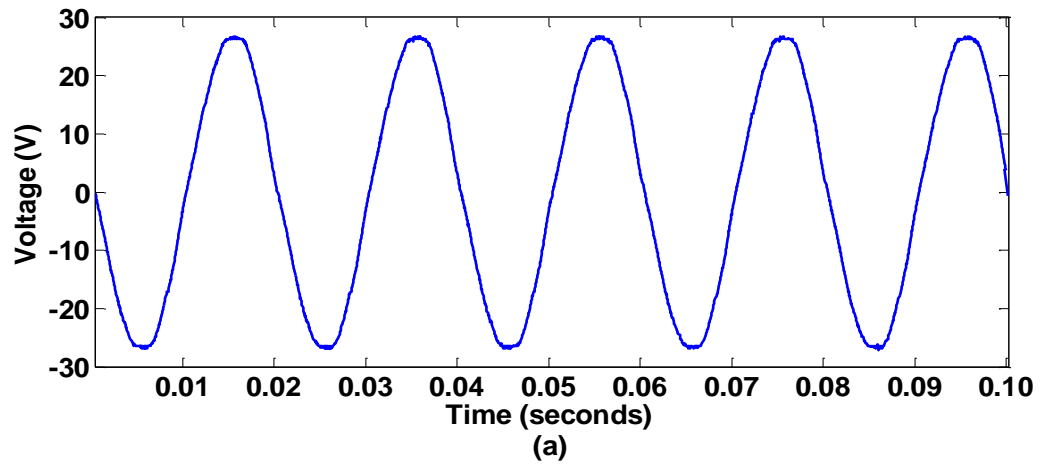


Figure 6.3 (a) Reference voltage, (b) output voltage, (c) current

6.1.1 Hierarchical Balancing Control

In this experiment system, SoC of each cell is estimated using Coulomb counting based on (6.1). This method has been described in detail in Section 2.5.

$$SoC(t) = SoC_0 + \frac{1}{Q_{max}} \int_0^t I(\tau) d\tau \quad (6.1)$$

where SoC_0 is the initial SoC and Q_{max} is the maximum Ampere-hour of the cell. SoC_0 is set to 1 when a cell is fully charged.

As illustrated in Figure 6.4, this experimental work includes two levels of balancing: balancing of cells within a module and balancing of modules. For balancing of cells within a module, at any particular instant of time, the balancing controller chooses an active cell combination in order to get as close as possible to the value of the reference voltage, V_{ref}^m , where $m = 1, 2$. It aims to keep SoC of each cell ($\alpha^{m1}, \alpha^{m2} \dots \alpha^{m12}$) in a module equal to the average SoC of the module, α^m . Balancing of modules is achieved by distributing the reference voltage for each module in proportion (or in negative proportion) to that module's SoC deviation from the average SoC of two modules, depending on whether the system is discharging (or charging). V_{max}^m is needed for peak sharing algorithm which will be discussed in Section 6.3.

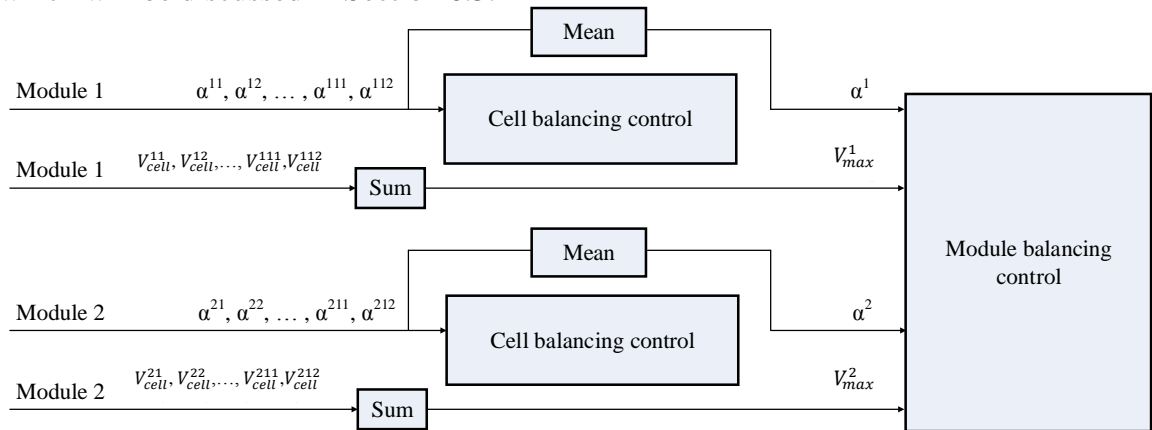


Figure 6.4 Block diagram of SoC balancing control

6.1.2 Obtaining Maximum Capacity of Individual Cell

There is cell variation due to manufacturing tolerances across a set of cells; not all cells are created equal. Even for cells that are the same model from the same manufacturer or same production batch, the variation in cell capacity of up to 15 % is common [417]. For those cells with slightly less capacity than the others, their SoCs will gradually deviate over multiple charge and discharge cycles. Therefore, instead of assuming all cells have equal capacity, a series of experiments illustrated in Figure 6.5 has been carried out to obtain the maximum capacity of each cell for all 24 cells in both modules.

All cells are fully charged initially and maintained in an open state for 24 hours. A discharge test is performed with a constant current of 0.2 C rate to discharge each cell from fully charged state (upper voltage limit, 1.5 V) to fully discharged state (lower voltage limit, 0.9 V). A cell may reach its cut-off voltage before the others in the chain due to having a higher internal resistance than the other cells, which means that each cell reaches cut-off voltage at a different time point. When a cell reaches cut-off voltage, the system stops discharging the cell, and the cell capacity is obtained based on Coulomb counting in (6.1). The system continues discharging the remaining cells until each of them reaches cut-off voltage.

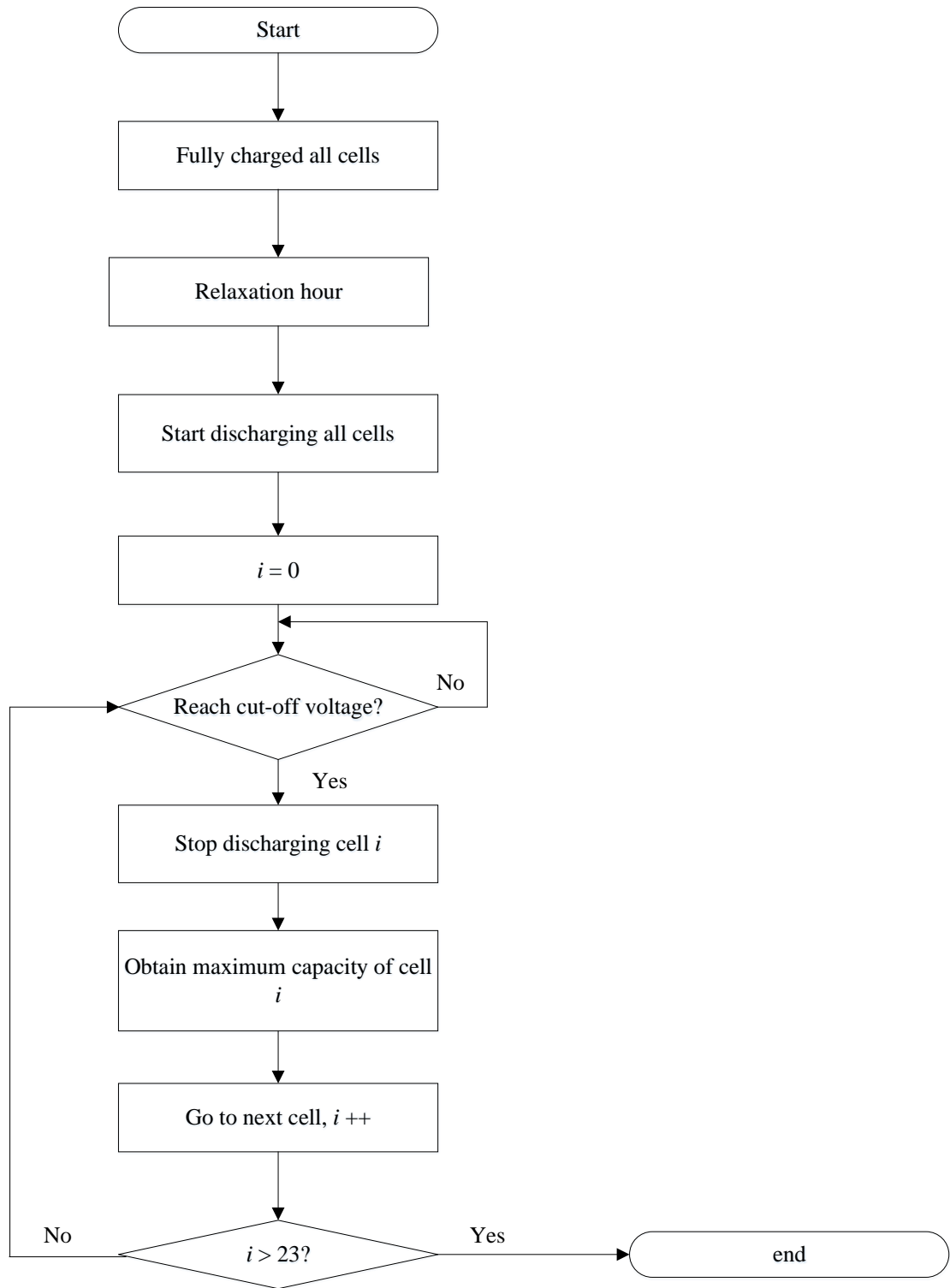


Figure 6.5 Flowchart: obtaining maximum cell capacity

Figure 6.6 illustrates the maximum capacities obtained for all twelve cells in module 1 where the capacities range from 7866 mAh to 8430 mAh. Cell 9 reaches the cut-off voltage at $t = 276$ min, which yields a maximum capacity of 7866 mAh. The other cells continue discharging until at $t = 295$ min, cell 12 reaches the cut-off voltage and thus obtaining a maximum capacity of 8430 mAh, it has the highest capacity among twelve cells in module 1. It can be observed that each cell exhibits a different maximum capacity even though cells of same model are used in this work.

By repeating the same experimental procedures above, the maximum capacities obtained for twelve cells in module 2 range from 7555 mAh to 8151 mAh as demonstrated in Figure 6.7. Cell 10 has the lowest capacity where it reaches the cut-off voltage at $t = 276$ min with a maximum capacity of 7555 mAh. The system continues to discharge the remaining cells until cell 11 reaches the cut-off voltage at $t = 296$ min and thus obtaining a maximum capacity of 8151 mAh, which is the highest capacity among twelve cells in module 2.

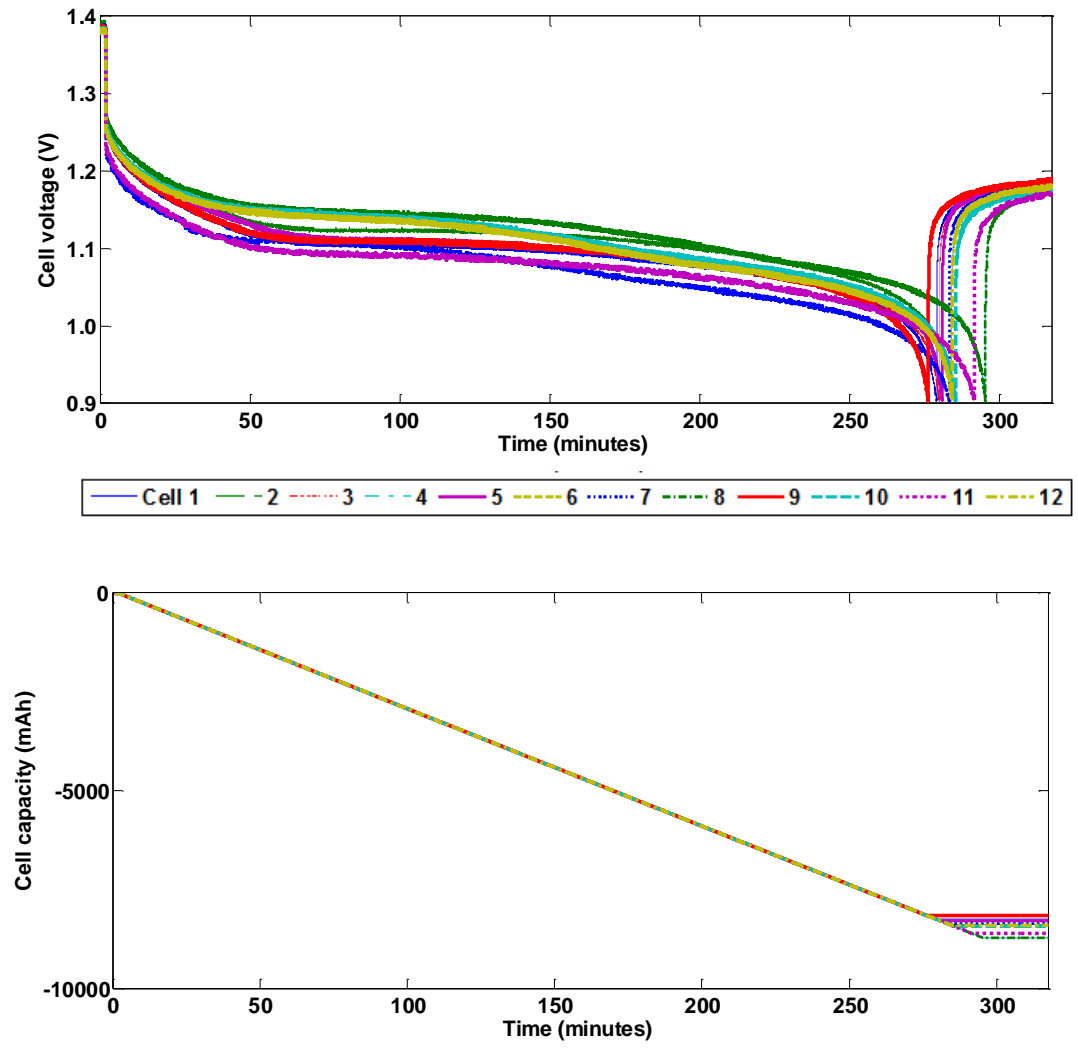


Figure 6.6 Obtaining maximum capacity for all cells in module 1

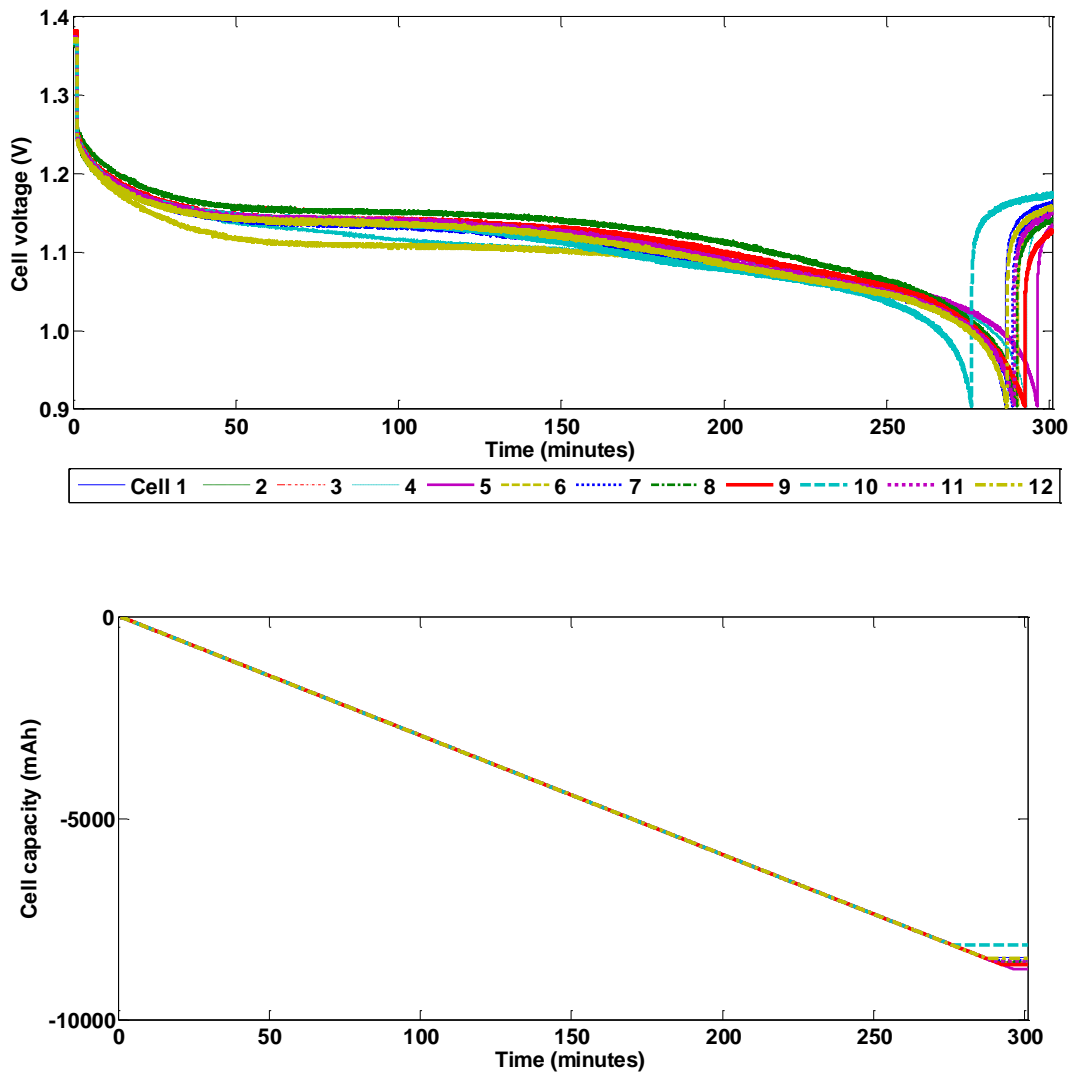


Figure 6.7 Obtaining maximum capacity for all cells in module 2

6.2 Experimental Results and Discussion

Two sets of experiments are carried out using different β values: $\beta = 3$ and $\beta = 6$ respectively. Table 6.2 summarises the circuit parameters. Each experiment consists of two modules, each module comprises of twelve Ansmann 8500 mAh NiMH. The modules initial SoC are set as: $\alpha_0^1 = 0.736$ and $\alpha_0^2 = 0.436$ where α_0^1 and α_0^2 represent the initial

average SoC of module 1 and module 2 respectively. The initial SoC of cells in module 1 ($\alpha_0^{11}, \alpha_0^{12} \dots \alpha_0^{112}$) range from 0.6 to 0.855. The initial SoC of cells in module 2 ($\alpha_0^{21}, \alpha_0^{22} \dots \alpha_0^{212}$) range from 0.3 to 0.555.

Table 6.2 System parameters

Reference voltage	V_{ref}	24 V
Current	I	10 A
Inductor	L	2.4 mH
Sampling rate	f_s	50 kHz
No. of modules	M	2
Nominal maximum voltage of each module	V_{DC}	28.8 V
No. of cells in each module	N	12
Average initial SoC of module 1	α_0^1	0.736
Initial SoC for cells in module 1	$\alpha_0^{11}, \alpha_0^{12} \dots \alpha_0^{112}$	0.855, 0.85, 0.825, 0.80, 0.775, 0.75, 0.725, 0.70, 0.675, 0.65, 0.625, 0.60
Average initial SoC for cells in module 2	α_0^2	0.436
Initial SoC for cells in module 2	$\alpha_0^{21}, \alpha_0^{22} \dots \alpha_0^{212}$	0.555, 0.55, 0.525, 0.50, 0.475, 0.45, 0.425, 0.40, 0.375, 0.35, 0.325, 0.30

Each cell can be set to the pre-defined initial SoC through a series of experiments illustrated in a flowchart in Figure 6.8. All cells are fully charged initially and maintained in a long relaxation period of 24 hours. A discharge test is performed to discharge all the cells in the system. Prior to the discharge test, all cells have a SoC of 1 since they are all fully charged. The system stops discharging a cell when the cell's SoC is equal to the pre-defined SoC listed in Table 6.2. The system continues discharging the remaining cells until each of them reaches the pre-defined SoC value.

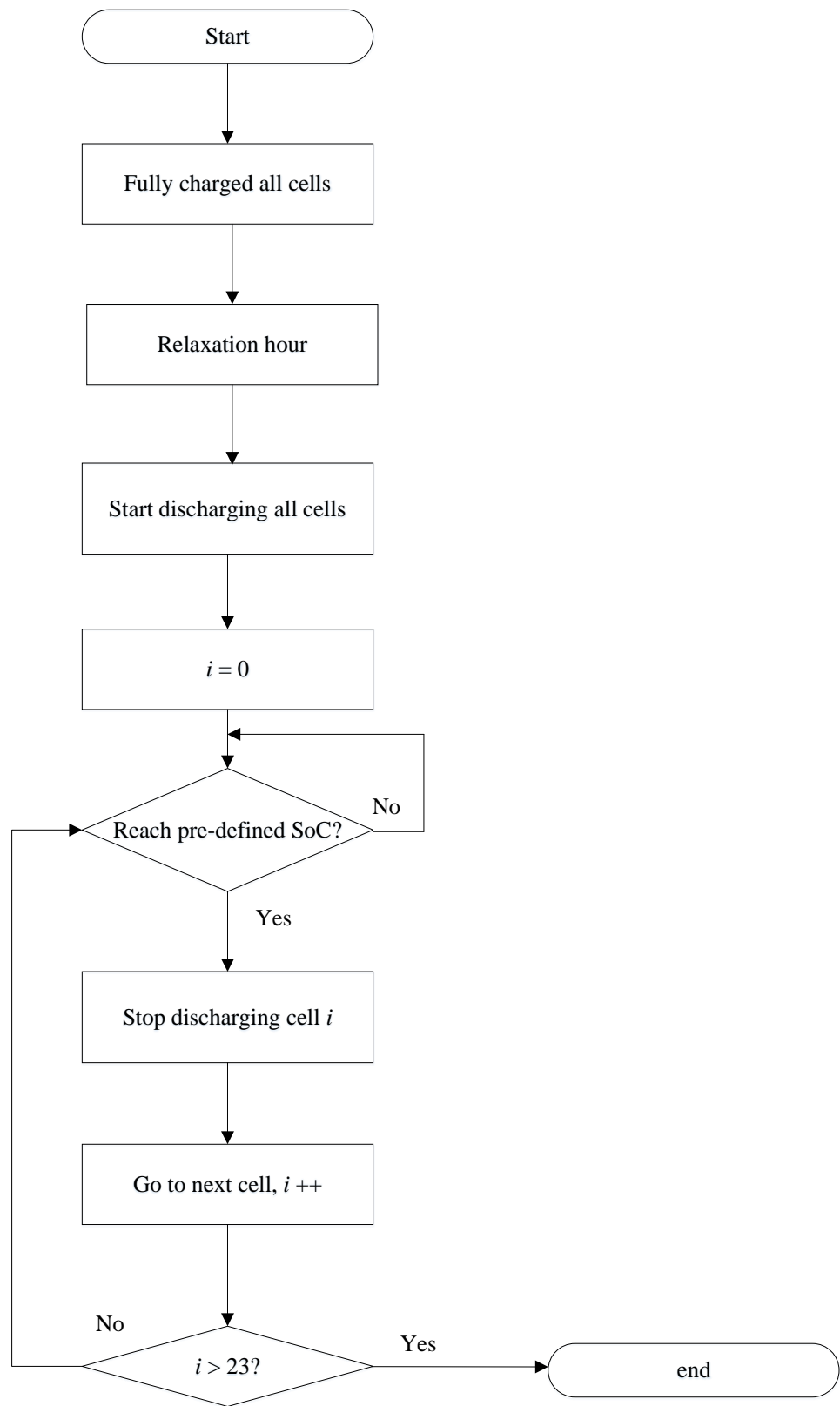


Figure 6.8 Flowchart: setting initial SoC for each individual cell

The result of the experiments applying SoC balancing control to two modules with mismatched SoC is shown in Figure 6.9 and Figure 6.10 for high and low β values respectively. In Figure 6.9, before the balancing control takes place, a maximal SoC imbalance of 25.5 % exists between the highest and lowest cells in module 1 and module 2, while a SoC mismatch of 30 % exists between module 1 and module 2. When the balancing control is started at $t = 0$, the SoCs gradually converge. In module 1, the variation of SoC due to the random initial conditions is observed where $\alpha^{11} > \alpha^{12} > \alpha^{13} \dots > \alpha^{112}$ during charging, thus α^{112} will tend to be charged more rapidly compared to the remaining eleven cells within the module and this eventually brings SoC convergence within module 1 at around $t = 2990$ s, where all SoCs are effectively balanced. In module 2, the variation of SoC due to the random initial conditions is observed where $\alpha^{21} > \alpha^{22} > \alpha^{23} \dots > \alpha^{212}$ during charging, thus α^{212} will tend to be charged more rapidly compared to the remaining eleven cells within the module and this eventually brings SoC convergence within module 2 at around $t = 3220$ s, where all SoCs are effectively balanced.

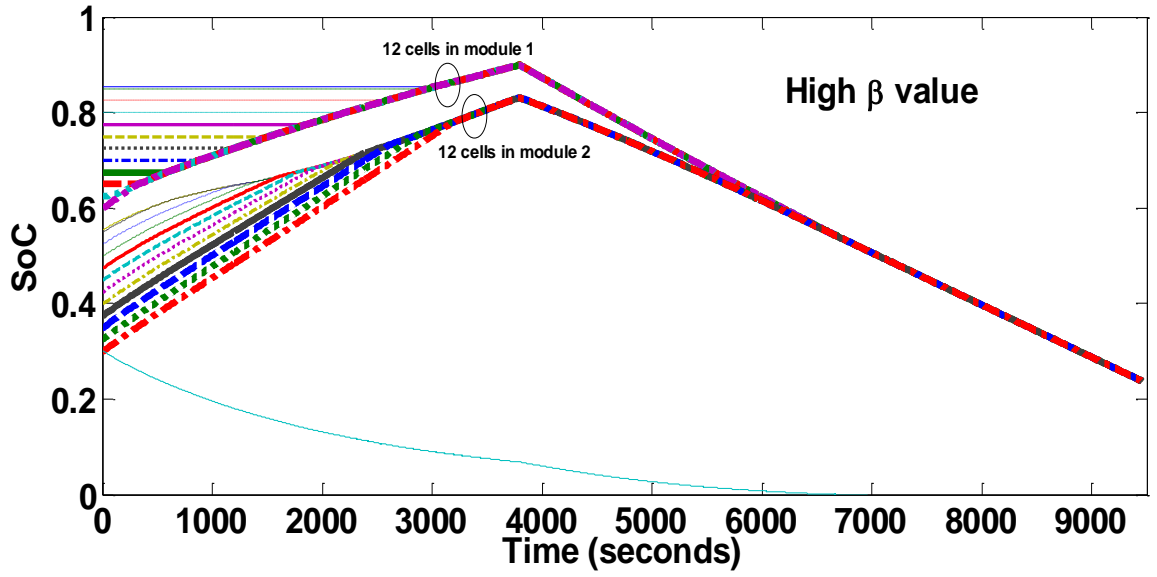
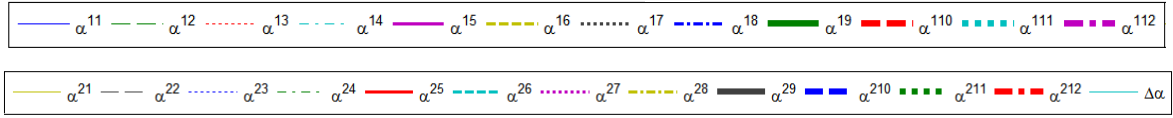
Module 2 has a lower initial average SoC compared to module 1 at the beginning of the balancing test, thus module 2 is assigned a higher reference voltage and it tends to be charged more rapidly than module 1. This eventually brings SoC convergence between the two modules at around $t = 6200$ s. The duration needed for module 1 and module 2 to reach convergence varies where it is dependent on the reference voltage assigned to each module. It can be observed that module 1 takes a shorter time to reach convergence within the module compared to module 2 as not all twelve cells in module 1 are being charged. Module 2 took around 230 s longer to reach convergence where all twelve cells are being

used. The SoC difference between two modules, $\Delta\alpha$ is reduced to half of its initial value (0.3 to 0.15) in 1650 s as illustrated in Figure 6.9.

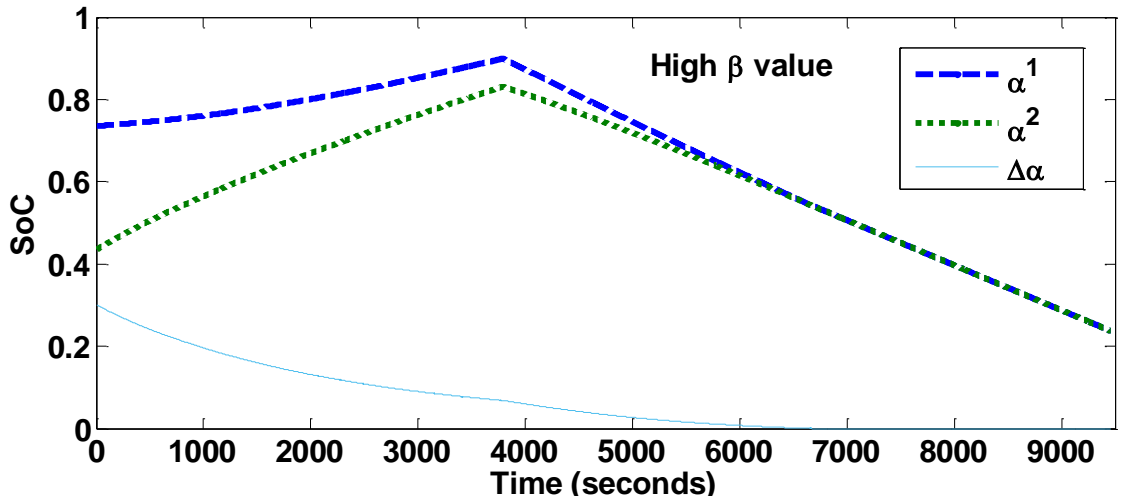
Another experiment is carried out using a low β value with the same initial SoC setting described above. In Figure 6.10, the variation of SoC in module 1 due to the random initial conditions is observed where $\alpha^{11} > \alpha^{12} > \alpha^{13} \dots > \alpha^{112}$ during charging, thus α^{112} will tend to be charged more rapidly compared to the remaining eleven cells within the module and this eventually brings SoC convergence within module 1 at around $t = 2300$ s, where all SoCs are effectively balanced. In module 2, the variation of SoC due to the random initial conditions is observed where $\alpha^{21} > \alpha^{22} > \alpha^{23} \dots > \alpha^{212}$ during charging, thus α^{212} will tend to be charged more rapidly compared to the remaining eleven cells within the module and this eventually brings SoC convergence within module 2 at around $t = 2590$ s, where all SoCs are effectively balanced. Similarly to the high β value setting, module 2 has a lower initial average SoC compared to module 1 at the beginning of the balancing test, thus module 2 is assigned a higher reference voltage and it therefore tends to be charged more rapidly than module 1. However, the reference voltage assigned to module 2 is lower than the voltage assigned to it in the high β value test. The amount of reference voltage assigned to each module can be calculated from Table 4.2 and has been described in Chapter 4. This eventually brings SoC convergence between the two modules at around $t = 9240$ s. The cells in module 1 take a shorter time to reach convergence because more cells (four cells) are being used instead of just one cell in the experiment using high β value as the reference voltage assigned to module 1 is now higher. The cells in module 2 reach convergence about 630 s faster than in the experiment using high β value. Cell 1 and cell 2 in module 2 are now lightly utilised, this is different from the experiment using high β

value where all twelve cells are being charged aggressively. This is due to the fact that a lower reference voltage is now assigned to module 2 with a low β value, therefore not all twelve cells in module 2 are needed to meet the assigned reference voltage. The SoC difference between two modules, $\Delta\alpha$ is reduced to half of its initial value (0.3 to 0.15) in 3520 s which is more than double the duration needed when a high β value is used. It can be concluded that higher β value accelerates the module SoC convergence rate. In contrast, with a lower β value, the reference voltage assigned to the modules is shared more evenly but module SoC convergence rate is decreased.

It is important to note that a higher β value tends to assign an extreme amount of reference voltage that might exceed the maximum voltage available in a module. For example, during discharging (charging), the assigned reference voltage could be much higher than the maximum voltage available in the module with a higher (lower) average SoC. Therefore, an additional feature, ‘peak sharing’ is implemented to address this issue where alternative modules assume a portion of the load when certain modules are not capable of meeting the demand. The experimental work of peak sharing is demonstrated in Section 6.3.



(a)



(b)

Figure 6.9 High β value: (a) SoC balancing of cells in module 1 and module 2 respectively, (b) SoC balancing of modules within a sub-bank

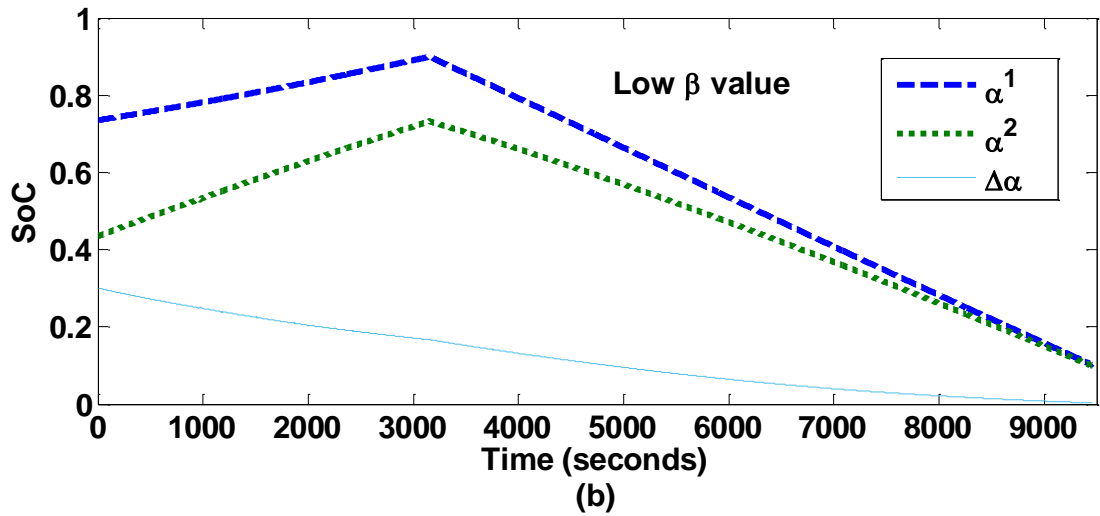
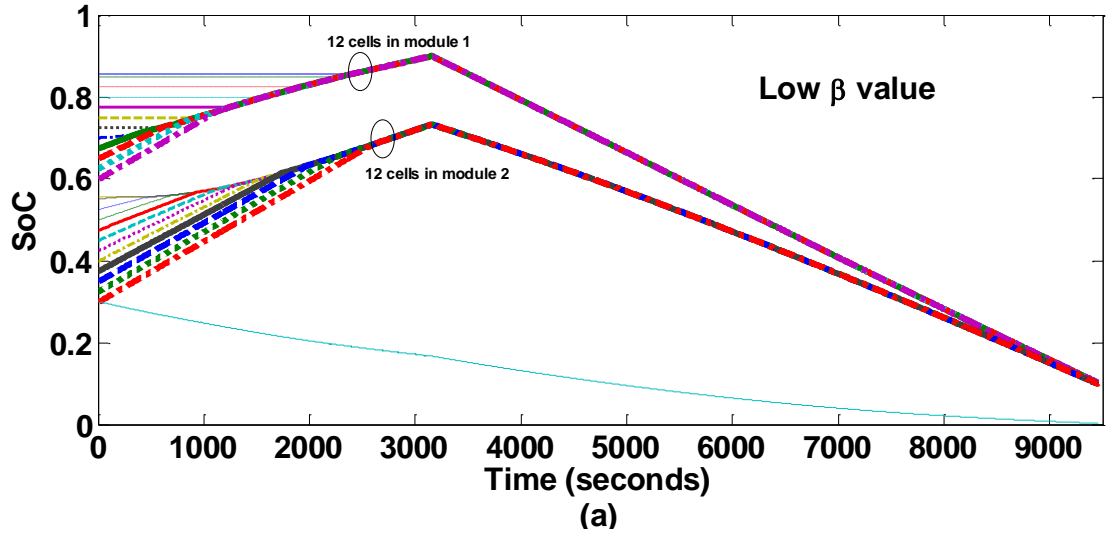
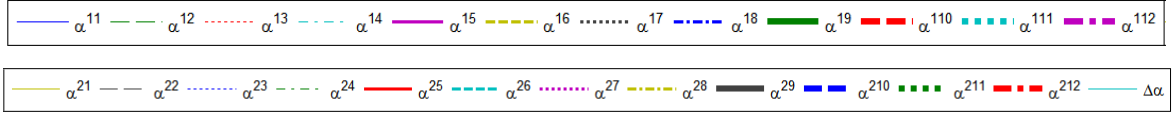


Figure 6.10 Low β value: (a) SoC balancing of cells in module 1 and module 2 respectively, (b) SoC balancing of modules within a sub-bank

Once the balancing test is terminated, all cells are left to recover for 24 hours and cell voltages are measured and tabulated in Table 6.3. There is a maximal voltage difference of 56 mV before the balancing test, and the difference dropped to 19 mV after 24 hours of recovery period. In this work, SoC is estimated using Coulomb counting method. Although this method is highly accurate theoretically, current sensor inaccuracies due to noise, resolution and rounding can introduce errors that accumulated over time, which might result in the OCV difference among the cells.

A SoC difference is the only cause for cell voltage differences if no current is flowing. Although OCV has a direct correlation with SoC, the relationship between the OCV and SoC cannot be exactly the same. Even for cells with same chemistry, the same SoC imbalance of 1 % has different voltage for different SoCs [246] [274] [416-417], as can be seen in Figure 6.12. In this work, the balancing test is terminated when the average SoC of all cells is around 10.225 % (see Figure 6.10(a)) which yields a maximal OCV difference of 19 mV between cells with highest and lowest OCV. Referring to Figure 6.11, the OCV difference between two cells at $SoC = 10\%$ can be as high as 70 mV for a SoC imbalance of 1 %. In this work, the maximal SoC difference, when the balancing test is terminated, is 0.46 %. It can be concluded that all cells stay close within acceptable margin (19 mV) after the recovery period, thus indicating the success of the balancing control.

Table 6.3 Cell voltage of all cells before and 24 hours after the balancing test (in Volts)

Module 1	Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8	Cell 9	Cell 10	Cell 11	Cell 12
Before balancing	1.369	1.365	1.362	1.361	1.355	1.355	1.349	1.361	1.346	1.355	1.342	1.338
24hours after balancing	1.313	1.311	1.306	1.311	1.313	1.305	1.301	1.320	1.306	1.317	1.304	1.307

Module 2	Cell 1	Cell 2	Cell 3	Cell 4	Cell 5	Cell 6	Cell 7	Cell 8	Cell 9	Cell 10	Cell 11	Cell 12
Before balancing	1.335	1.331	1.327	1.322	1.332	1.331	1.326	1.324	1.33	1.321	1.319	1.313
24hours after balancing	1.311	1.306	1.304	1.304	1.308	1.314	1.314	1.311	1.315	1.307	1.310	1.307

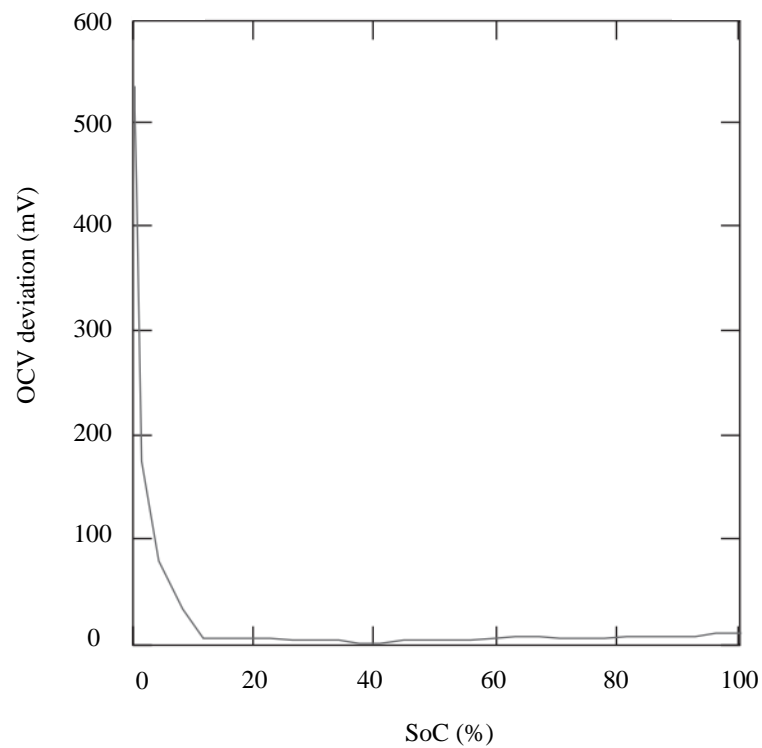


Figure 6.11 OCV differences at different SoCs between two cells with SoC imbalance of 1 % [246] [417]

Figure 6.12 shows the current waveforms for cell 1 and cell 12 in module 2 at $t = 0 - 0.01$ s. Referring to Figure 6.9, cell 12 has the lowest initial SoC compared to other cells, therefore, it is used to form the output voltage for the entire half cycle of the sinusoidal waveform when system is charging. However, cell 1 is only active and used to form the output voltage during peak voltage when the requested reference voltage cannot be achieved by the first eleven cells in the sorting list. Cell 1 is sorted as the last cell to be used as it has the highest initial SoC.

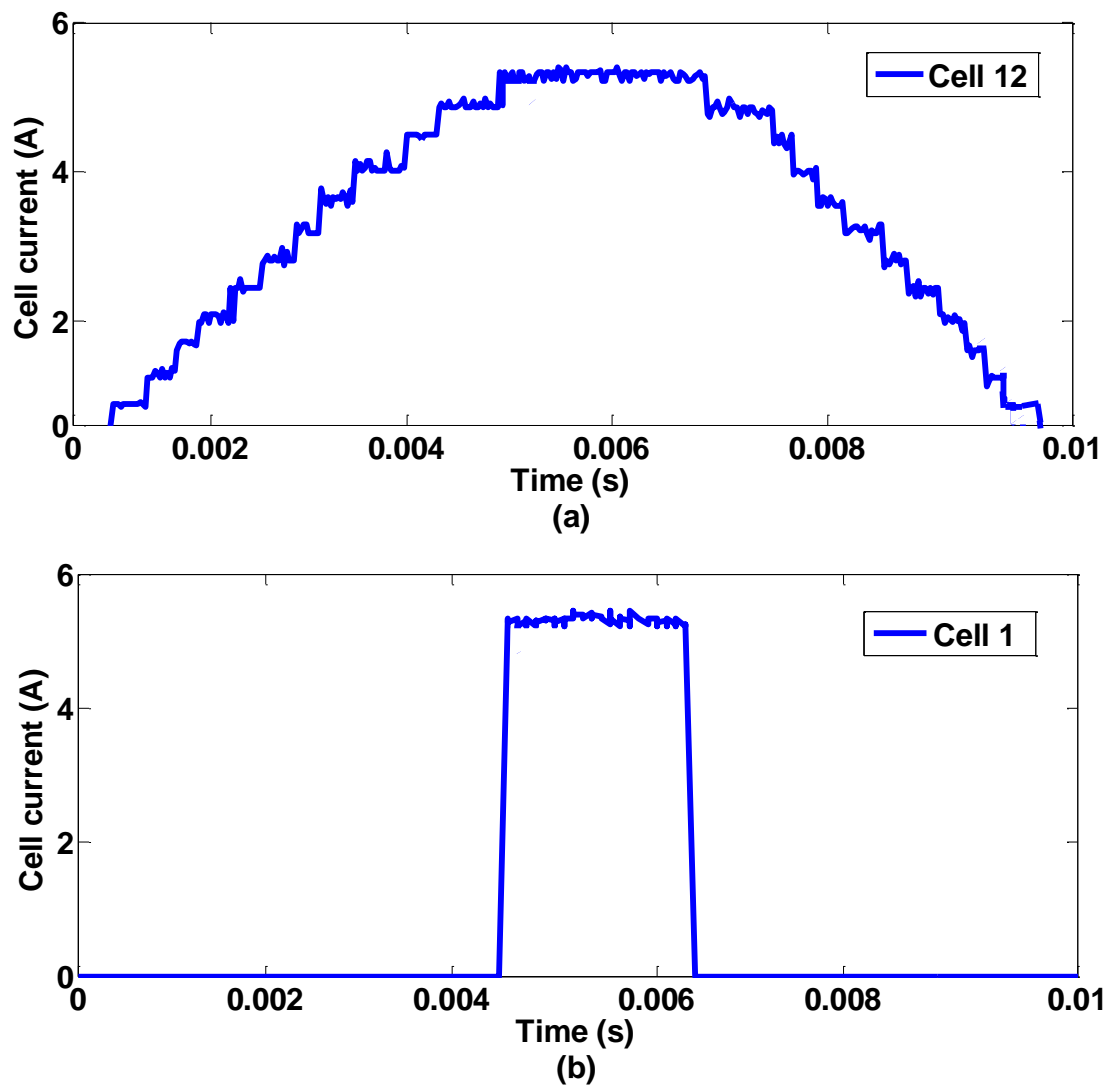


Figure 6.12 Current waveform: (a) cell 12, (b) cell 1 in module 2

6.3 Peak Sharing

This experimental work aims to validate the effectiveness of peak sharing concept demonstrated in simulation model in Chapter 5. When a low β value is used, the reference voltage assigned to the modules is shared more evenly between two modules, thus, each module is less likely to have a reference voltage that is higher than the maximum voltage available in that module as long as a reasonable system reference voltage is set. For instance, in a scenario where $V_{ref}^{a111} \leq V_{max}^{a111}$ and $V_{ref}^{a112} \leq V_{max}^{a112}$, all cells in both modules are used to form a 49-level output voltage depicted in Figure 6.13, which is a close approximation of sinusoidal waveform that can be achieved without peak sharing.

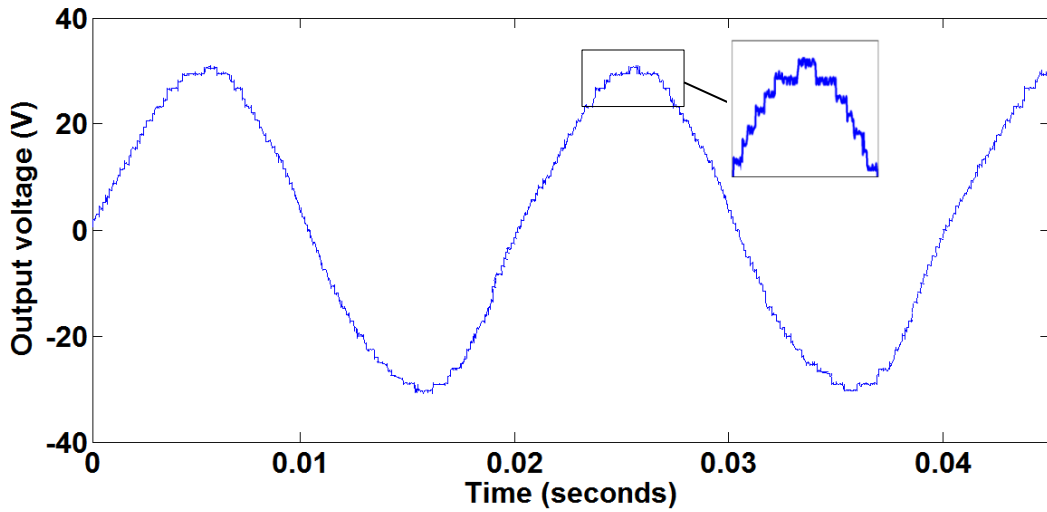


Figure 6.13 Low β value without peak sharing: output voltage of a 49-level cascaded H-bridge multi-level converter

In this work, module 2 has a lower average SoC compared to module 1 prior to convergence ($\alpha^2 < \alpha^1$), thus, module 2 is assigned a higher reference voltage and it tends to be charged more rapidly than module 1. As a high β value tends to assign an extreme amount of reference voltage, module 1 is assigned a reference voltage that is much lower than the maximum voltage available while module 2 is assigned a reference voltage that is

much higher than maximum voltage available, which yields $V_{ref}^{a111} \ll V_{max}^{a111}$ and $V_{ref}^{a112} \gg V_{max}^{a112}$ when system is charging. Only one cell in module 1 is switched on as the V_{ref}^{a111} is much lower than the maximum voltage available in module 1. All cells in module 2 are switched on, which yields an output voltage that is still lower than the requested V_{ref}^{a112} . Consequently, there are only thirteen cells (instead of 24 cells in the experiment using low β value in Figure 6.13) that form the output voltage illustrated in Figure 6.14(a). The number of steps is not enough to follow the sinusoidal reference voltage, and so the output voltage is distorted (the peaks are ‘clipped’). In a practical BESS, this will result in highly distorted line currents and is unacceptable. Peak sharing is essential when a high β value is used to accelerate the convergence of module SoC. Figure 6.14(b) demonstrates the implementation of peak sharing to the system in Figure 6.14(a) when a high β value is used. With peak sharing, module 2 is now assigned a new reference voltage that is limited to the maximum voltage available within the module, the additional voltage is now distributed to module 1 that can assume additional load. Thus, module 1 now requires more cells (instead of one cell in Figure 6.14(a)) to meet the new reference voltage. A total of 24 cells is used to form the output voltage which is a close resemblance to a perfect sinusoidal waveform. This output voltage (Figure 6.14(b)) is 150 % higher than the output voltage obtained in the experiment without peak sharing (Figure 6.14(a)).

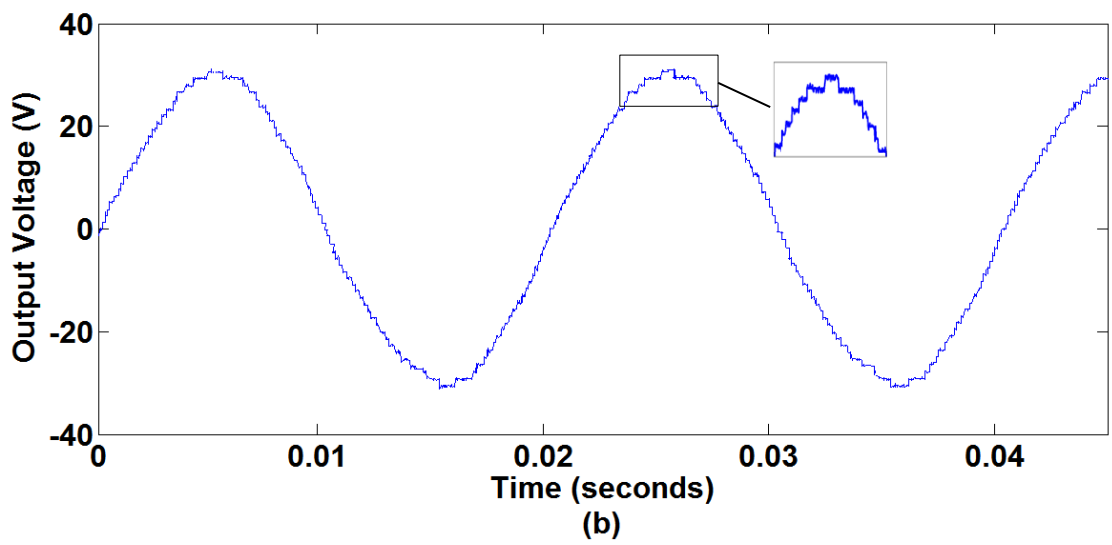
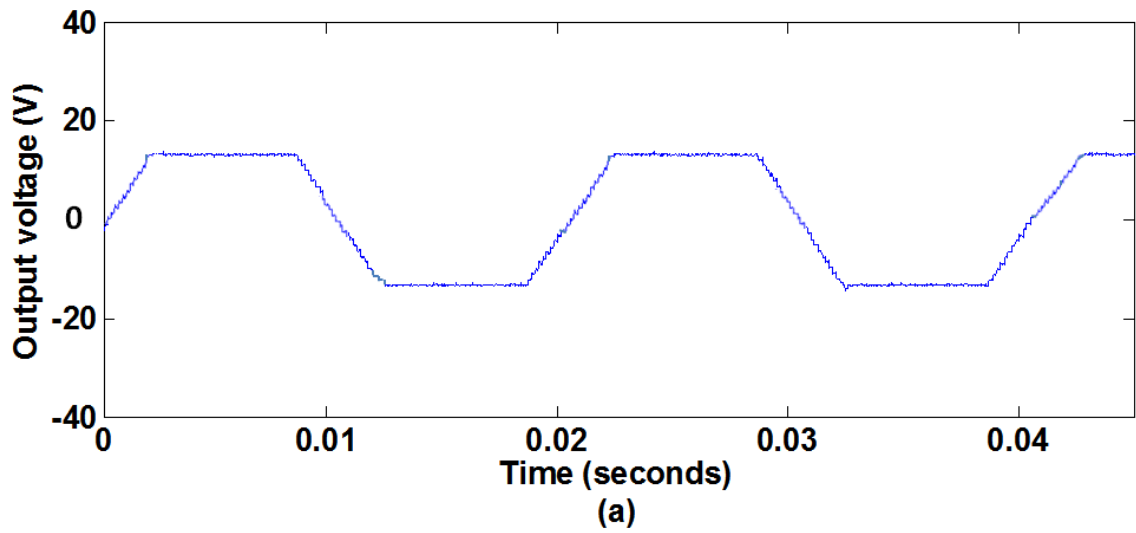


Figure 6.14 Output voltage in the experiment using a high β value: (a) without peak sharing, (b) with peak sharing

CHAPTER 7 CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE RESEARCH

7.1 Conclusions

The thesis has presented a circuit and control topology for a grid-scale BESS. The thesis has addressed three important issues: direct DC-AC power conversion system, SoC balancing control using a hierarchical structure and voltage constraints management using peak sharing, which are essential for a practical BESS. An experimental validation has been performed to demonstrate the effectiveness of the proposed balancing control. This work is intended to address the challenges of eventual scaling towards a 100 MWh+ BESS, which may be composed of hundreds of thousands of individual cells which must be managed in a cost-effective, scalable and efficient manner.

7.1.1 Direct DC-AC Power Conversion System

The thesis proposes the close integration of a cascaded H-bridge multi-level converter and a large number of Li-ion cells interfacing with an AC electrical grid. The direct DC-AC conversion distributes the number of series-connected cells required in a number of cell-converters, while keeping the possibility of MV converter output using low voltage cells. Additional modules can be inserted in the event of cell failure, and only a single module is taken out for service rather than a string of cells connected to the DC-link. The switching state redundancy of this topology demonstrated in Chapter 3 provides scope for cell balancing without using additional circuits. However, this topology uses a high number of devices resulting in higher number of gate drivers, higher conduction losses (as they are proportional to the number of cells), and increased failure rate.

7.1.2 SoC Balancing Control using a Hierarchical Structure

Cells are organised in a hierarchical structure consisting of modules, sub-banks, banks and phases. This hierarchical system arrangement is used to scale the system to the very large number of cells required for a practical grid-scale BESS. The control strategy presented in Chapter 4 includes five levels of balancing: balancing of cells within a module, balancing of modules within a sub-bank, sub-banks within banks, banks within phases and balancing between phases. Critically, communication between layers is limited to three values (SoC , V_{ref} and V_{max}) for each member of the next lowest level only. It is not necessary to propagate, for example, values for individual cell SoC from the cell level all the way up the hierarchy to the phase level. This would present major challenges to scaling to very large numbers of cells due to the exponential growth of cell number with the number of levels in the hierarchy. The system is validated in simulation for a 380 kWh BESS using 2835 Li-ion cells.

The underlying balancing controller and circuit operation was verified by simulation, demonstrating that SoC is equalised during the charge/discharge process and voltage limits internal to the system are respected at all times. The system has been shown to work for levels of SoC imbalance that are much greater than would be expected in practice. The proposed system maximises the accessible SoC range of each individual cell by ensuring that weak cells do not limit the capacity of the system. This is in contrast to the situation where cells are connected in a simple series battery pack arrangement. Although the hierarchical organisation is restricted to four layers (cells, modules, sub-banks and banks), it is conceptually straightforward to insert further hierarchical layers into this structure by continuing the pattern in Table 4.2 to increase further the number of cells in the

BESS. However, it may become progressively more challenging to calculate and propagate signals rapidly enough to allow the system to follow the reference voltage accurately.

7.1.3 Managing Voltage Constraints using Peak Sharing

To avoid severely limiting the performance of the proposed system described in Chapter 4 especially when a high β value is used, an additional step referred to as peak sharing is incorporated into the balancing controller algorithm. Peak sharing, discussed in detail in Chapter 5, allows alternative modules to assume a portion of the load when certain modules are not capable of meeting the demand. It ensures that the reference voltage requested from each module (or sub-bank etc.) is limited by the maximum available voltage at all times. It also ensures that no module is required to supply more than its maximum voltage as long as the sub-bank (or bank etc.) reference voltage is less than or equal to the sum of all module maximum voltages. The limitation of this approach is that the sub-bank (or bank etc.) reference voltage must be less than or equal to the sum of all modules (or sub-banks etc.) maximum voltages.

7.1.4 Experimental BESS

The experimental BESS presented in Chapter 6 has been established to validate the performance of the SoC balancing control, for mainly three ideas: balancing of cells within a module, balancing of modules and peak sharing. NiMH cells are electrically interfaced to the grid by the cascaded H-bridge multi-level converter. Two sets of experiments using different β values have demonstrated the effectiveness of the proposed balancing control where higher β value accelerates the module SoC convergence rate. The experimental work also verifies the effectiveness of peak sharing in managing voltage constraints to

avoid severely limiting the system performance. Note that although the experimental BESS consists of only two modules which serves as a basic design concept for a practical BESS, it can easily be expanded to a larger system by increasing the number of module and hierarchical level.

7.2 Recommendations for Future Research

7.2.1 Improvement on SoC Estimation

In this thesis, the underlying balancing controller relies on Coulomb counting to estimate SoC. Precise SoC estimation is critical for practical BESSs to prevent overcharging and deep discharging of each individual cell, which may cause major failure and serious deterioration in system performance. Improvement could be made to the proposed system by integrating hybrid or model-based SoC estimation methods into the balancing controller to improve the accuracy and the robustness of the SoC estimation.

Another useful direction for this work in future is to include an additional parameter in the balancing controller, which is the state-of-health (SoH) of each cell. The accuracy of SoC estimation is greatly affected by cell degradation [258]. SoH prediction can be performed by monitoring the number of charge/discharge cycles, capacity and/or internal resistance, etc.. The knowledge of the SoH, which can be incorporated into the proposed balancing controller, is required to predict cell degradation in order to prevent a possible failure and to plan replacement.

The balancing controller chooses a cell combination in order to get as close as possible to the value of the reference voltage by monitoring both the SoC and SoH of each cell. For instance, a cell with higher SoC will not be used when system is discharging if its

SoH shows that the cell will fail. Early detection of cell degradation allows the BESS to take remedial action, preventing serious damage to the system. SoC estimation can also be improved by taking into account the temperature effect as cells might experience severe loss of capacity in case of temperature variation [121-122]. The effect of temperature changes can be modelled by including a temperature-dependent rate factor in the Li-ion cell model illustrated in Figure 4.13. The temperature-dependent rate factor, k is obtained using (7.1). Equation (7.2) shows the SoC estimation using Coulomb counting replacing (4.13) as the temperature effect is now included in the cell model.

$$k(T_n) = \frac{SoC(T_{ref})}{SoC(T_n)} \quad (7.1)$$

where $SoC(T_{ref})$ is the SoC of cell at T_{ref} , T_{ref} is 20 °C, $SoC(T_n)$ is the SoC of cell at various temperatures such as -10 °C, 0 °C, 10 °C or 45 °C for the Li-ion cell used in this work (see Appendix C for details).

$$SoC = \int_0^t k I_{cell} dt \quad (7.2)$$

Since k is not constant but is dependent on the temperature, an additional look-up table implementation is required in the cell model as depicted in Figure 7.1.

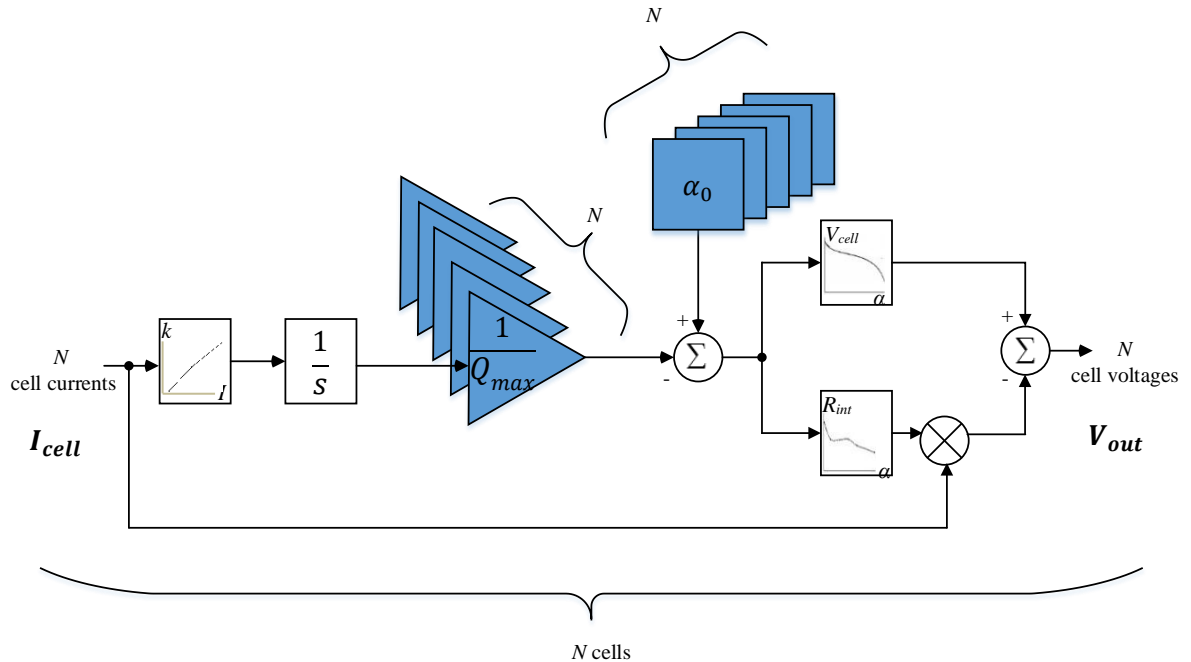


Figure 7.1 Incorporation of temperature effect into a single MATLAB Simulink block of Li-ion cell model for N cells

7.2.2 Reliability Evaluation of Grid-scale BESSs

A direction for future development of this work could be to evaluate the reliability of a grid-scale BESS. The reliability performance of a BESS is not only affected by the battery pack but also the PCS, thus, developing a reliability model for both battery pack and PCS is essential. In order to assess the reliability of the battery pack, a capacity fade model based on SoH can be developed and used to recognise ongoing or abrupt degradation of each cell to prevent possible failure. The reliability evaluation can be performed under different operating conditions such as varying the number of cells (modules etc.) connected in series within a module (sub-bank etc.), capacity, battery module power, and the number of cycles [420].

The failure rate of the power semiconductor devices in a PCS is dependent on the power losses (conduction losses and switching losses), which is determined by the

charging/discharging current and operating temperature. A correlation between the charging/discharging current versus the failure rate can be obtained. A reliability model based on current and junction temperature can be developed to assess the reliability of a PCS, other factors that significantly affect the PCS reliability can also be included in the model [421]. The reliability model can be used to evaluate the performance of other circuit topologies such as MML half-bridge and mixed-level multi-level converters.

7.2.3 Efficiency Comparison of Direct DC-AC Power Conversion System and Conventional Power Conversion Systems

In a BESS, energy must be transferred in and out of the battery pack. Thus, the overall efficiency of the BESS, or round-trip efficiency, is greatly affected by the power conversion system (PCS) efficiency. An efficiency study can be performed to compare the conduction and switching losses between direct DC-AC PCS and conventional PCSs, where these are the primary sources of loss. Conduction loss can be modelled as a fixed voltage source that accounts for the voltage drop on each conducting device, connected in series with a resistor. The energy loss each time a switch is turned on and off depends on the driving circuit and can be considered proportional to the DC voltage and the instantaneous value of AC current [322].

7.2.4 Evaluation of Cell Utilisation Improvement with SoC Balancing Control

The existing system employs SoC balancing control that ensures each cell goes through all possible operational conditions as the balancing control equally distributes the cells through the available operational conditions in order to keep them balanced. A direction for future development of this work is to evaluate the cell utilisation improvement

under the proposed balancing control. The maximum available capacity of the battery pack in the current state and the maximum available capacity of the battery pack after balancing are deduced, where this ratio is defined as the capacity utilisation of the battery pack. The difference between these two capacities indicates the increase in the capacity after balancing.

Assuming there is SoC mismatch between cells before the balancing control takes place, the SoC balancing control is to keep all cells in a module equal to the mean SOC value of the corresponding module. Two tests are required in order to study the effectiveness of the balancing control on the cell utilisation. For the test without SoC balancing control using 1 C discharging (or charging) rate, the total time required for discharging (or charging) the module from 100 % (or 0 %) SoC to 0 % (or 100 %) SoC is recorded as t_{nbal} . Another test is performed by applying the proposed SoC balancing control in this work, where the duration taken for the system to fully discharged (or charged) is recorded as t_{bal} . Therefore, the percentage of capacity improvement, A can be calculated as:

$$A = \frac{100(t_{bal} - t_{nbal})}{t_{nbal}} \% \quad (7.3)$$

A SoC window between 30 % and 70 % (rather than 0 % and 100 %) can be chosen to improve the lifetime of a battery pack [163].

7.2.5 Three-phase Experimental BESS with Fault-tolerant Control

MV multi-level converters require a large number of power semiconductor devices. Each of these devices is a potential failure point, which can lead to expensive downtime. Fault-tolerant control allows the system to continue operation under fault conditions either

by providing a redundant cell-converter in each phase and bypassing the faulty cell-converter as well as the healthy cell-converter in the other two phases, or by bypassing the faulty cell-converter without redundant cell-converters. Fault-tolerant design has been investigated in literatures [422-424], however, most have been limited to theoretical analysis and/or simulation work.

The experimental BESS presented in this thesis is a single-phase system, a three-phase experimental system can be implemented to allow each of the three phases to inject or absorb an unequal active power in order to achieve balancing between phases as demonstrated in the simulation work in Chapter 4. A fault-tolerant control based on a combination of cell-converter bypass and zero-sequence voltage injection can be implemented to maintain continuous operation of the system by producing a three-phase balanced line-to-line voltage and achieving SoC balancing among the remaining healthy cells. This will enhance the reliability of a BESS. Reactive power control can be added to the existing experimental BESS for reactive power compensation and improvement in voltage regulation [394].

7.2.6 Experimental BESS using Li-ion cells

The experimental BESS presented in Chapter 6 is based on NiMH cells. NiMH cells have energy densities in the range of 140-300 Wh/kg while Li-ion cells in the range of 200-500 Wh/kg. Li-ion cells are becoming increasingly attractive for use in grid-scale BESSs. Experimental validation of Li-ion cells in the proposed balancing control is therefore necessary.

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APPENDIX A. SIMULATION MODEL IN MATLAB SIMULINK

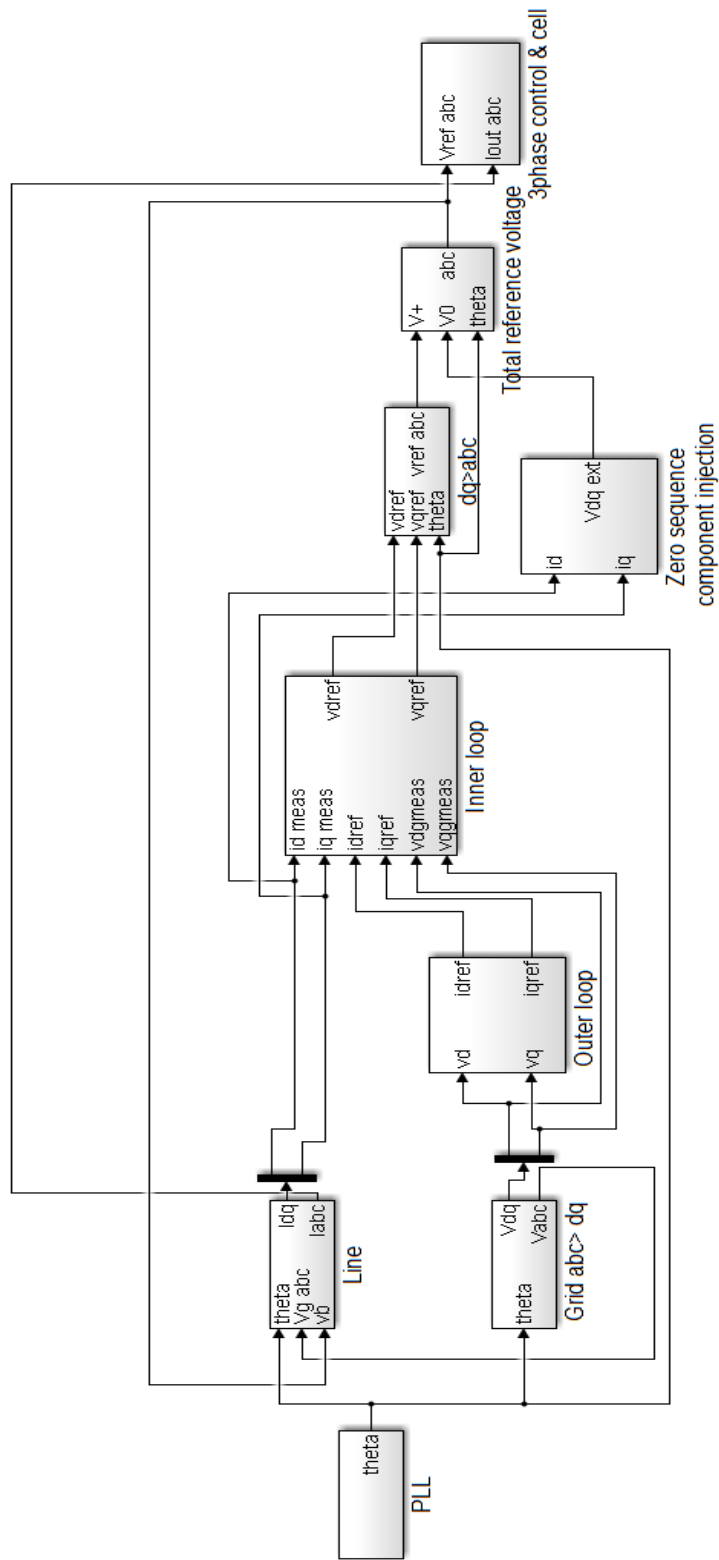


Figure A.1 High-level simulation model in MATLAB Simulink

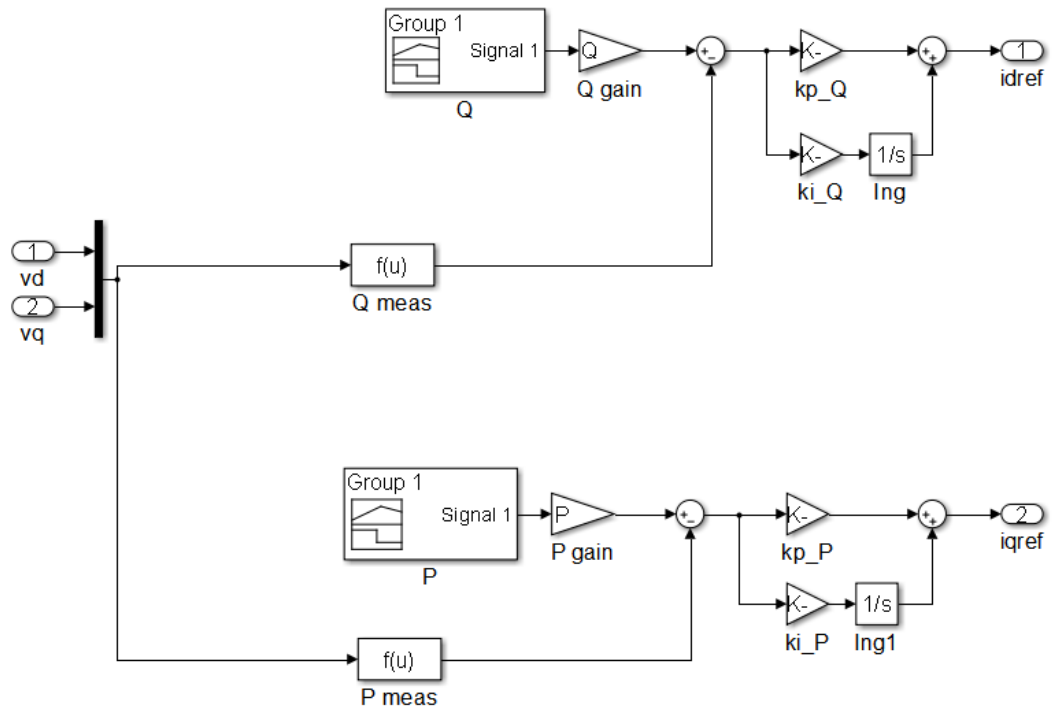


Figure A.2 Outer loop

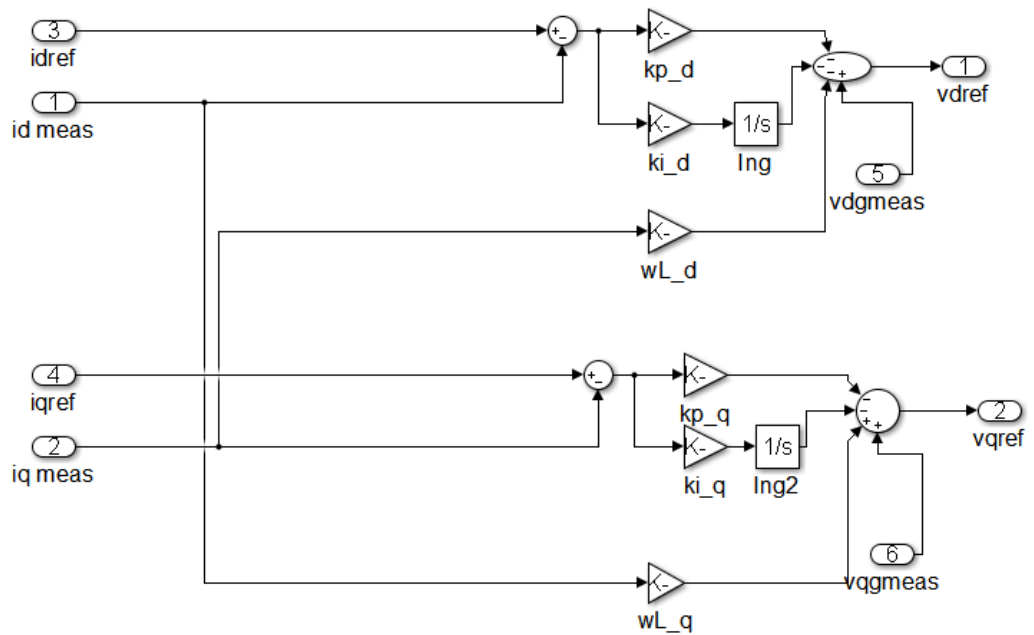


Figure A.3 Inner loop

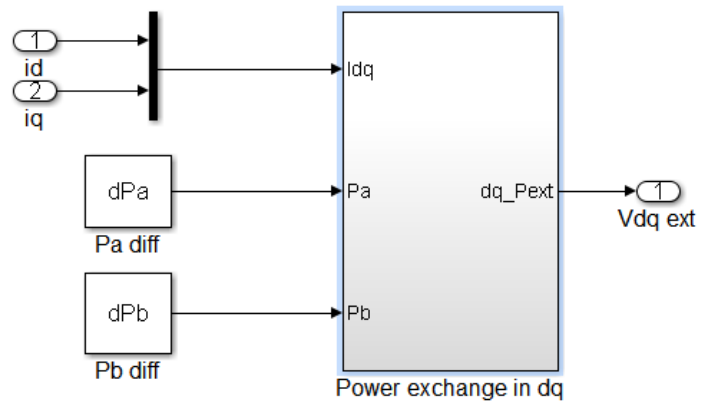


Figure A.4 Zero-sequence component injection

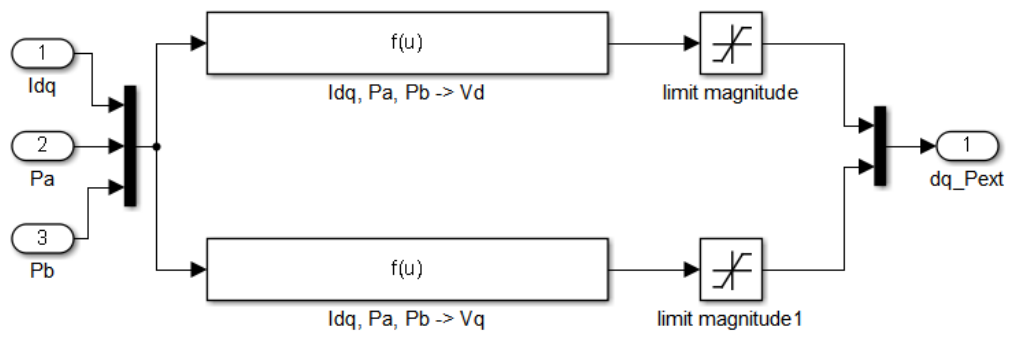


Figure A.5 Power exchange in dq

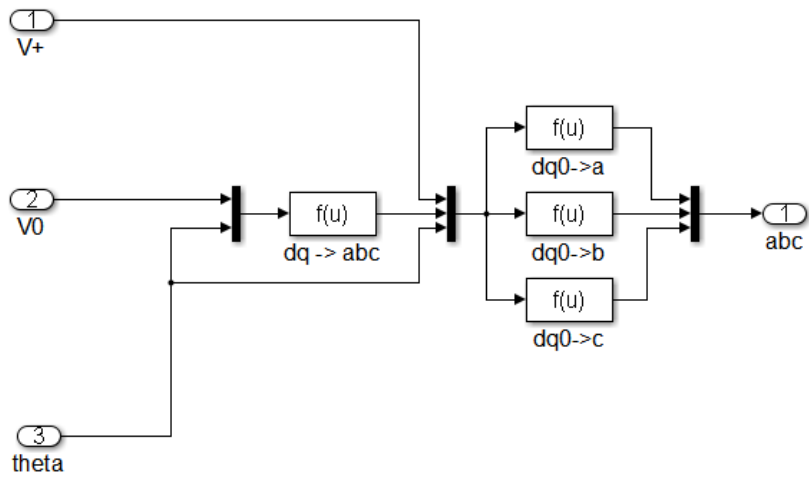


Figure A.6 Total reference voltage

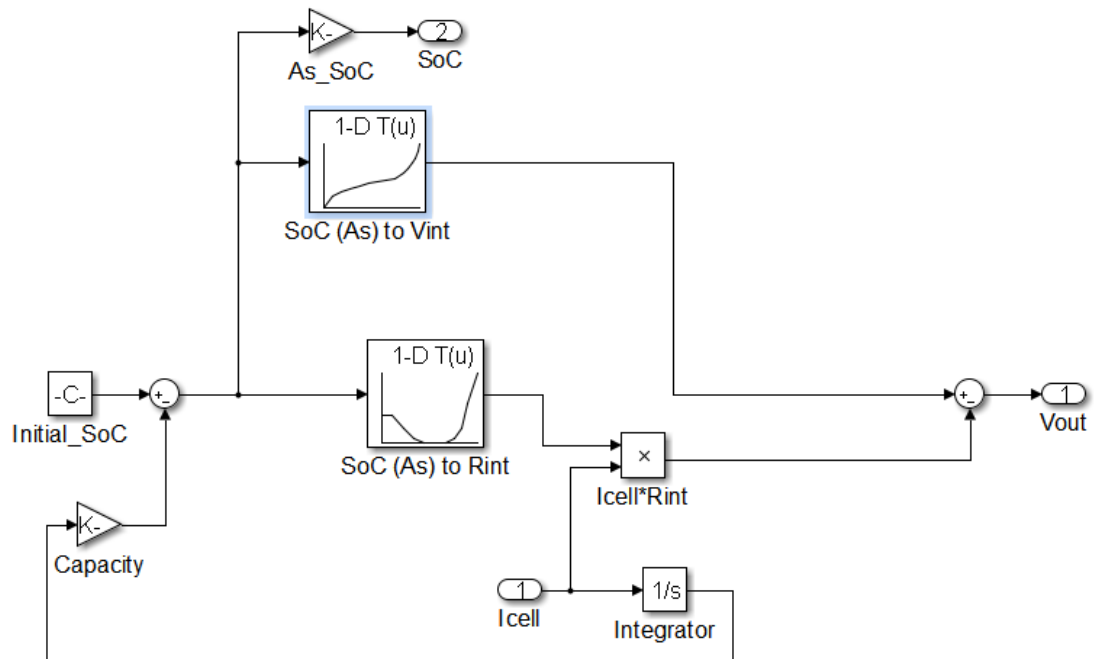


Figure A.7 Cell model

Parameter Setting

N = 35; %number of cells in a module

R= 0.0001; %line resistor

L= 0.1; %line inductor

Tsamp=0.0001; %sampling time

Tfast=0.0001; %fast time step

Tslow=10; %slow time step

kp_Q = 0.0003; %proportional gain for outer loop

kp_P = 0.0003; %proportional gain for outer loop

ki_Q=0.002; %integral gain for outer loop

ki_P= 0.002; %integral gain for outer loop

kp_d= 1; %proportional gain for inner loop

ki_d=0.01; %integral gain for inner loop

kp_q=1; %proportional gain for inner loop

ki_q=0.01; %integral gain for inner loop

a = 0.98;

b = 1;

Initial_SoC = (b-a).*rand(1,N) + a; %set initial SoC for all cells

c = 40; %minimum capacity in Ah

d = 100; %maximum capacity in Ah

Capacity= (d-c).*rand(1,N) + c; %set maximum capacity for all cells

APPENDIX B. REFERENCE FRAME TRANSFORMATION

Stationary Reference Frame $\alpha\beta$

The behaviour of a three-phase system, generally described by mathematical modelling involving voltage and current equations, tends to be complex as the coefficients of the differential equations are time varying; induced voltages, flux linkages, and currents change continuously. Consequently, a mathematical transformation is often used to transform a three-phase system to a two-phase system to decouple AC variables such as voltages and currents, and to solve equations involving time varying quantities by referring all variables to a common reference frame, where the frame is the axes of the transformed system. The instantaneous voltages and currents of a balanced three-phase system can be expressed as:

$$\left\{ \begin{array}{l} \left\{ \begin{array}{l} V^a = V^m \cos \theta \\ V^b = V^m \cos \left(\theta - \frac{2\pi}{3} \right) \\ V^c = V^m \cos \left(\theta + \frac{2\pi}{3} \right) \end{array} \right. \\ \left\{ \begin{array}{l} I^a = I^m \cos(\theta + \varphi) \\ I^b = I^m \cos \left(\theta - \frac{2\pi}{3} + \varphi \right) \\ I^c = I^m \cos \left(\theta + \frac{2\pi}{3} + \varphi \right) \end{array} \right. \end{array} \right. \quad (\text{B.1})$$

where V^m is the peak value of line-to-neutral voltage, I^m is the peak value of line-to-neutral current, θ is the instantaneous phase angle and φ is the phase angle between voltage and current.

Applying the concept of stationary reference frame [425], a three-phase system is transformed into a two-phase system, and this is often called abc to $\alpha\beta$ transform. Both systems are said to be stationary as the axes is locked in a common position [426]. The

transformation can be seen as a change of coordinate system from a three-axis system to a two-axis system as illustrated in Figure B.1.

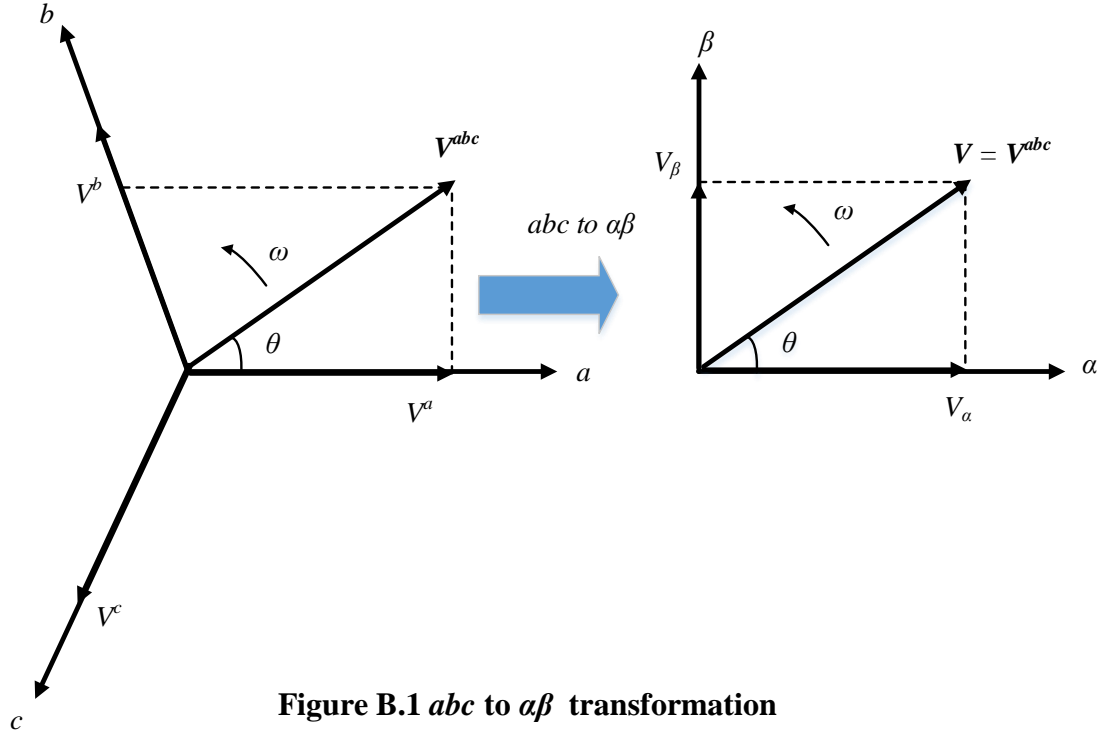


Figure B.1 abc to $\alpha\beta$ transformation

The three-phase voltages and currents can be split into only two components, α and β (real and imaginary parts). Using Clarke transformation, voltages and currents can be transformed from abc frame to $\alpha\beta$ frame as in (B.2), where X denotes voltage or current.

$$\left\{ \begin{array}{l} \mathbf{X}_s = X_\alpha(t) + jX_\beta(t) = \frac{2}{3}K(X^a(t) + X^b(t)e^{j\frac{2\pi}{3}} + X^c(t)e^{j\frac{4\pi}{3}}) \\ \begin{bmatrix} X_\alpha \\ X_\beta \\ X_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} X^a \\ X^b \\ X^c \end{bmatrix} \end{array} \right. \quad (\text{B.2})$$

where K is a scaling constant ($K = 1$ for amplitude invariant, $K = \frac{1}{\sqrt{2}}$ for rms-invariant, and

$K = \sqrt{\frac{2}{3}}$ for power invariant)

Equation (B.3) is obtained by performing matrix multiplication on (B.2).

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} \mathbf{V}^{abc} \sin \theta \\ -\mathbf{V}^{abc} \cos \theta \end{bmatrix} \quad (\text{B.3})$$

Synchronous Rotating Frame dq

The stationary reference frame is useful, however, the quantities in $\alpha\beta$ frame also suffer from the oscillation as in the abc frame as α and β components are still sinusoidal signals rotating physically with the angular velocity of the electrical system ω . For many applications, it is useful to work with slowly varying DC quantities instead. In this system, the axis is no longer locked, but rotates following an arbitrary vector, hence it is called synchronous reference frames, or more commonly known as dq frame [385-386]. The $\alpha\beta$ axis system is displaced by angle θ using (B.4).

$$\mathbf{V}_{dq} = \mathbf{V}_s e^{-j\theta} \quad (\text{B.4})$$

This transformation has gained popularity in motor drives application where the axis system follows the rotor position or rotor flux. In a grid-tied VSC system, it is a common practice to lock the axis to grid voltage or current (usually the grid voltage). Figure B.2 demonstrates the $\alpha\beta$ to dq transformation where d -axis is locked to $\mathbf{V}_{\alpha\beta}$, and thus $V_d = \mathbf{V}_{\alpha\beta}$ and $V_q = 0$. The transformation depends on the dq frame alignment at $t = 0$ where its position is given by ωt (where ω represents the frame rotation speed).

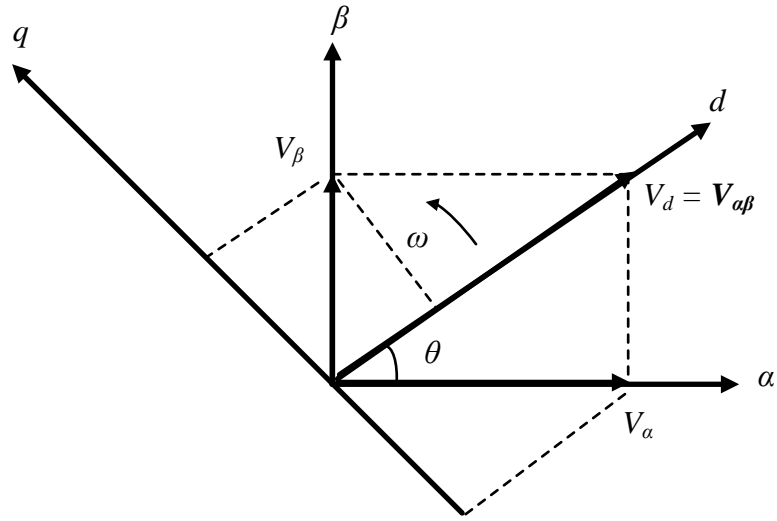


Figure B.2 $\alpha\beta$ to dq transformation

Using Park transformation shown in (B.5), synchronous quantities can be expressed as a function of the stationary quantities. Both grid voltage and current are transformed into dq system using same reference frame. With the dq system locked to grid voltage, the axes rotate following ω and the dq values appear as DC quantities. By choosing the correct θ , constant quantities are obtained. The d -axis current is in phase with the grid voltage, and thus, it represents the active power in the system while the q -axis current is out of phase with the voltage, and thus it represents the reactive power in the system. It is possible to have active power controlled by q -axis with a modification to the orientation of dq -axis on $V_{\alpha\beta}$ vector.

$$\begin{bmatrix} V_d \\ V_q \\ V_0 \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta & 0 \\ -\sin \theta & \cos \theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} \quad (\text{B.5})$$

The summary of transformation is presented as follows:

Table B.1 Transformation of axes

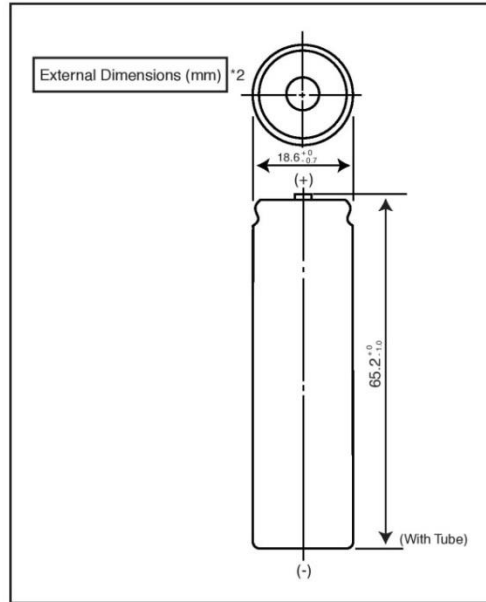
Transformation	Input	Output	Transformation matrix
Clark transformation	abc	$\alpha\beta$	$\frac{2}{3} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix}$
Inverse Clark transformation	$\alpha\beta$	abc	$\begin{pmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix}$
Park transformation	$\alpha\beta$	dq	$\begin{pmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{pmatrix}$
Inverse Park transformation	dq	$\alpha\beta$	$\begin{pmatrix} \cos \theta & -\sin \theta \\ \sin \theta & \cos \theta \end{pmatrix}$

APPENDIX C. PANASONIC CGR18650CG LI-ION CELL DATA SHEET

LITHIUM ION BATTERIES: INDIVIDUAL DATA SHEET

CGR18650CG

CGR18650CG: Cylindrical Model



To ensure safety, the referenced Li-ion cell is not sold as a bare cell. Li-ion cells must be integrated with the appropriate safety circuitry via an authorized Panasonic Li-ion pack assembler.

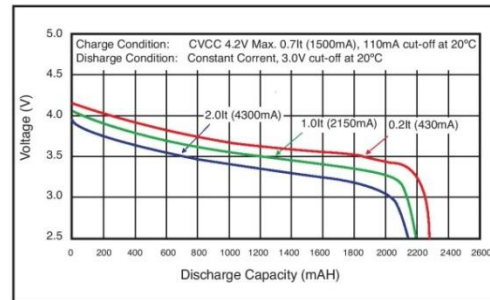
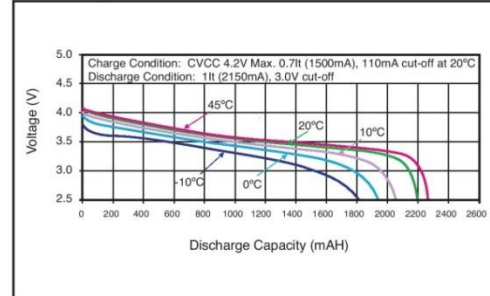
Specifications

Nominal Voltage		3.6 V
Standard Capacity^{*1}		2250mAh
Dimensions^{*2}	Diameter	18.6 + 0/-0.7mm
	Height	65.2 + 0/-1.0mm
	Weight	Approx. 45g

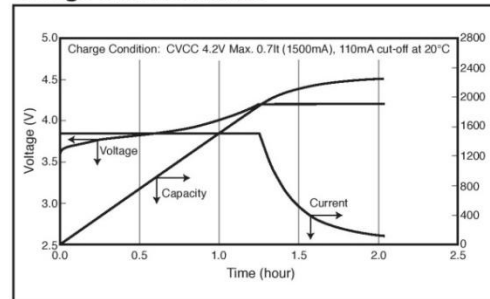
*1 After a fresh battery has been charged at constant voltage/constant current (4.2 V, 1500mA (max), 2 hours, 20°C), the average of the capacity (ending voltage of 3 V at 20°C) that is discharged at a standard current (430mA).

*2 Dimensions of a fresh battery

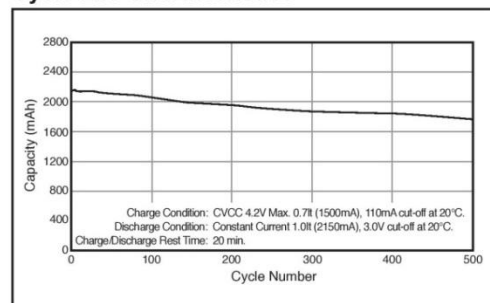
Discharge Characteristics



Charge Characteristics



Cycle Life Characteristics



Panasonic

LITHIUM ION

DECEMBER 2008

This information is generally descriptive and is not intended to make or imply any representation, guarantee or warranty with respect to any cells and batteries. Cell and battery design specifications are subject to modification without notice. Contact Panasonic for the latest information.

APPENDIX D. CALCULATION OF ZERO-SEQUENCE VOLTAGE

From (B.1), the instantaneous current for phase a and phase b in a balanced three-phase system can be expressed as follow:

$$\begin{cases} I^a = I^m \cos(\omega t + \varphi) = I_d \cos(\omega t + \varphi) - I_q \sin(\omega t + \varphi) \\ I^b = I^m \cos(\omega t + \varphi - \frac{2\pi}{3}) = I_d \cos(\omega t + \varphi - \frac{2\pi}{3}) - I_q \sin(\omega t + \varphi - \frac{2\pi}{3}) \end{cases} \quad (\text{D.1})$$

The average power on each phase in dq frame is derived as:

$$\begin{cases} P_{avg} = \frac{1}{2} (V_d I_d + V_q I_q) \\ 2P^a = V_d I_d + V_q I_q \end{cases} \quad (\text{D.2})$$

The required trigonometric identities are listed below:

$$\begin{cases} \cos(\omega t + \varphi - \frac{2\pi}{3}) = -\frac{1}{2} \cos(\omega t + \varphi) + \frac{\sqrt{3}}{2} \sin(\omega t + \varphi) \\ \sin(\omega t + \varphi - \frac{2\pi}{3}) = -\frac{1}{2} \sin(\omega t + \varphi) - \frac{\sqrt{3}}{2} \cos(\omega t + \varphi) \end{cases} \quad (\text{D.3})$$

Substituting for I^b in (D.1) using (D.3), I^b can be described as:

$$I^b = \frac{1}{2} (-I_d + \sqrt{3} I_q) \cos(\omega t + \varphi) - \frac{1}{2} (-\sqrt{3} I_d - I_q) \sin(\omega t + \varphi) \quad (\text{D.4})$$

From (D.2), P^b can be expressed as follows:

$$2P^b = \frac{1}{2} [(-I_d + \sqrt{3} I_q) V_d + (-\sqrt{3} I_d - I_q) V_q] \quad (\text{D.5})$$

From (D.5), V_q is obtained as:

$$V_q = \frac{-4P^b + (-I_d + \sqrt{3} I_q) V_d}{(\sqrt{3} I_d + I_q)} \quad (\text{D.6})$$

Substituting (D.6) to (D.2), V_d is obtained as:

$$V_d = \frac{2P^a(\sqrt{3}I_d + I_q) + 4P^bI_q}{\sqrt{3}(I_d^2 + I_q^2)} \quad (\text{D.7})$$

From (D.6), V_d is obtained as:

$$V_d = \frac{(\sqrt{3}I_d + I_q)V_q + 4P^b}{(\sqrt{3}I_q - I_d)} \quad (\text{D.8})$$

Substituting (D.8) to (D.2), V_q can be expressed as:

$$V_q = \frac{2P^a(\sqrt{3}I_q - I_d) - 4P^bI_d}{\sqrt{3}(I_d^2 + I_q^2)} \quad (\text{D.9})$$

A voltage waveform can be expressed in dq frame as:

$$V = V_d \cos \theta + V_q \sin \theta \quad (\text{D.10})$$

Substituting (D.7) and (D.9) into (D.10), the zero-sequence injected voltage, V_{ref0}

is calculated as:

$$V_{ref0} = \frac{2\Delta P_{ref}^a(\sqrt{3}I_d + I_q) + 4\Delta P_{ref}^bI_q}{\sqrt{3}(I_d^2 + I_q^2)} \cos \theta + \frac{2\Delta P_{ref}^a(\sqrt{3}I_d - I_q) - 4\Delta P_{ref}^bI_d}{\sqrt{3}(I_d^2 + I_q^2)} \sin \theta \quad (\text{D.11})$$

APPENDIX E. ANSMANN D SIZE NIMH 8500 MAH CELL DATA SHEET

		Conditions	Diagrams
cell type:	NiMH		standard charge
cell size:	D		
nominal voltage:	1.2 V	at standard charge (0.1C / 20 °C)	fast charge
max. charge voltage:	1.5 V		
capacity			low rate discharge
nominal:	8500 mAh	discharge at 0.2C	
minimum:	8500 mAh 8000 mAh	discharge at 0.2C discharge at 1C	
		1.0V end discharge voltage ta: 20 °C	high rate discharge
max. continuous discharge current:	8500 mA	ta: 0...45 °C	
charge	current	time	
standard charge:	850 mA	14...16hrs	
quick charge:	2550 mA	4hrs	
fast charge:	4250 mA	2.3hrs	
recommended charge termination control parameters:	0...5 mV 0.8...1 °C 45...50 °C	- ΔV (-deltaV) temperature rise per minute TCO (temperature cut off)	
trickle charge current:	50...250 mA	(recommended)	
continuous overcharge: (less than 1 year)	≤ 850 mA	no conspicuous deformation no leakage	
internal resistance: (impedance)	≤ 15 mΩ	at 1KHz battery fully charged	
life expectancy:	≥ 500 cycles	acc. IEC standard	
self discharge			
charge retention:	≥ 80 %	after 12 months storage at 20 °C	
initial capacity:	≥ 6000 mAh	within 30 days after delivery discharge at 0.2C	
ambient temperature range:	0...45 °C 10...40 °C 0...45 °C - 20...65 °C - 20...50 °C - 20...40 °C - 20...30 °C	standard charge fast charge discharge (≥1C) discharge (<1C) storage (≤3months) storage (≤6months) storage (≤24months)	
QCT1:	20/8000/15		
QCT2:	30/7800/15		
mechanical specifications			
cell dimensions			
diameter d1:	32.8 - 1.0 mm		
diameter d2:	max. 9.5 mm		
height h1:	61.5 - 2.0 mm		
height h2:	min. 1.5 mm		
weight:	155 ± 8 g		
blister card dimensions:	123 x 85 mm		
blister card weight (incl. batteries):	320 g		

Manufacturer reserves the right to alter or amend the design, model and specification without prior notice

APPENDIX F. BALANCING CONTROL ALGORITHM IN MATLAB FOR EXPERIMENTAL SYSTEM

```
function mmc_heartbeat(heartbeat_timer,~,~) %need to take (obj, event,
string_arg)
global module_list;
global powerflow_direction;
global guiHandles
global heartbeat_vars; %contains all the parameters used from beat to
beat

timer = tic;
code = update_estop_status('raw');
heartbeat_vars.estop_code = code;

if ~strcmp(code, 'No fault')
    msg = sprintf('Heartbeat %i: emergency stop active with code:
%s',heartbeat_vars.count,code);
    stop(heartbeat_timer); %stop the timer which will cause StopFcn to
execute and show the estop in the GUI
else
    if heartbeat_vars.count == 0
        heartbeat_vars.count = 1;
        heartbeat_vars.pocv = get_all_cell_voltages('raw'); %get cell
voltage directly
        heartbeat_vars.q = get_all_cell_charges('raw'); %get cell charges
directly
    else
        heartbeat_vars.count = heartbeat_vars.count + 1; %read in
previous values
        for i = 1:length(module_list)
            heartbeat_vars.q(i) = get_cell_charge(module_list(i)); %get
all cell charges
        end
    end

    if get(guiHandles.operationTogglebutton,'Value') == 1
        %if we are running then update table with cell charges
        cell_charges = heartbeat_vars.q;
    else
        %if not then we have to get them from the mmc ourselves, but we
can get them in raw mode (faster)
        cell_charges = get_all_cell_charges('raw');
    end

    heartbeat_vars.soc =zeros(2,12); %allocate memory for all 24 cells
    Q12=zeros(2,12);
    S12=zeros(2,12);
    %set pre-defined initial SoC for all cells
    Si=[0.855 0.85 0.825 0.8 0.775 0.75 0.725 0.7 0.675 0.65 0.625 0.6;
0.555 0.55 0.525 0.5 0.475 0.45 0.425 0.4 0.375 0.35 0.325 0.3];
```

```

%set present cell capacity in mAh
Qm=[8246 8390 8274 8166 8301 8370 8730 8166 8433 8619 8400 8370; 8460
8155 8565 8654 8751 8576 8529 8565 8641 8155 8541 8475];
gq=(2^16/50e3) * ((2.5/4095)/0.08);%coulomb counter gain to give
result in Coulombs (As) (2.5V vref is 4095, sensitivity is 80mV/A)
(sample rate is 50kHz and we take top 24 bits from a 40 bits
accumulator)
C2mAh=1/3.6; %1 Coulomb is 1/3600 Ah

%module 1
for i = 1:12 %12 cells in a module
    Q12(1,i)= cell_charges(1,i);
    S12(1,i)= Si(1,i)+Q12(1,i)*gq*C2mAh/Qm(1,i); %calculate SoC from
    cell charge
    heartbeat_vars.soc (1,i) = S12(1,i);
end

%module 2
for i = 1:12
    Q12(2,i)= cell_charges(2,i);
    S12(2,i)= Si(2,i)+Q12(2,i)*gq*C2mAh/Qm(2,i);
    heartbeat_vars.soc (2,i) = S12(2,i);
end

%module 1
%sort the cells and send out new cell list to each module
i = 1; %sort cells by SoC
if strcmp(powerflow_direction,'charging')
    [~, cell_list_i] = sort(S12(i,:), 'ascend'); %lowest SoC cells
    have priority when charging
elseif strcmp(powerflow_direction,'discharging')
    [~, cell_list_i] = sort(S12(i,:), 'descend'); %highest SoC cells
    have priority when discharging
else
    error('illegal powerflow_direction');
end;

send_cell_list(module_list(i),cell_list_i); %send new cell list to
mmc
heartbeat_vars.cell_list(i,:) = cell_list_i; %update cell list

%module 2
i = 2; %sort cells by SoC
if strcmp(powerflow_direction,'charging')
    [~, cell_list_i] = sort(S12(i,:), 'ascend'); %lowest SoC cells
    have priority when charging
elseif strcmp(powerflow_direction,'discharging')
    [~, cell_list_i] = sort(S12(i,:), 'descend'); %highest SoC cells
    have priority when discharging
else
    error('illegal powerflow_direction');
end;

send_cell_list(module_list(i),cell_list_i); %send new cell list to
mmc

```

```

heartbeat_vars.cell_list(i,:) = cell_list_i;
%save data in csv
dlmwrite('cell_list1.csv', heartbeat_vars.cell_list(1,:), '-append');
dlmwrite('cell_list2.csv', heartbeat_vars.cell_list(2,:), '-append');
dlmwrite('soc_mm1.csv', heartbeat_vars.soc(1,:), '-append');
update_cell_table;
update_pll_text('raw');

%beta method
b=6; %set high or low beta value
S1avg=sum(S12(1,:))/12; %average SoC of module 1
S2avg=sum(S12(2,:))/12; %average SoC of module 2
Savg= (S1avg+S2avg)/2; %average SoC of all modules
S1d= S1avg-Savg; %SoC difference calculation
S2d= S2avg-Savg;
    if strcmp(powerflow_direction,'charging')
        akk(1)= 0.5*(1-b*S1d); %set reference voltage for module 1
        during charging
        akk(2)= 0.5*(1-b*S2d); %set reference voltage for module 2
        during charging
    elseif strcmp(powerflow_direction,'discharging')
        akk(1)= 0.5*(1+b*S1d); %set reference voltage for module 1
        during discharging
        akk(2)= 0.5*(1+b*S2d); %set reference voltage for module 2
        during discharging
    else
        error('illegal powerflow_direction');
    end;

q=0;
persistent d11;
if isempty(d11)
d11 = -0.5; %set charging or discharging current
end

%switch to charging when reaching lower SoC limit
for j=1:12
    if S12(1,j)<=0.1
        d11=-0.5;
    end
end

for j=1:12
    if S12(2,j)<=0.1
        d11=-0.5;
    end
end

%switch to discharging when reaching upper SoC limit
for j=1:12
    if S12(1,j)>=0.9
        d11=0.5;
    end
end
for j=1:12

```



```

        if S12(2,j)>=0.9
            d11=0.5;
        end
    end
end

set_master_iref2(d11,q); %set charging or discharging current

%peak sharing
Vps1=zeros(1,12);%memory allocation
Vps2=zeros(1,12);
vneg=0;
vpos=0;
%get cell voltages
for g = 1:12
    Vps1(g)= heartbeat_vars.pocv(1,g);
end
for g = 1:12
    Vps2(g)= heartbeat_vars.pocv(2,g);
end
%calculate the maximum voltage available in each module
vt1=sum(Vps1);
vt2=sum(Vps2);
vref_t = read_vref_t();%get system reference voltage
dlmwrite('vreftotal.csv', vref_t,'-append'); %save data for system
reference voltage
vref_t_abs = abs(vref_t); %absolute reference voltage
%calculate the voltage difference
vd1= vt1- akk(1)*vref_t_abs;
vd2= vt2- akk(2)*vref_t_abs;

%save data in csv
dlmwrite('vref1.csv', akk(1)*vref_t_abs,'-append');
dlmwrite('vref2.csv', akk(2)*vref_t_abs,'-append');
dlmwrite('vt1.csv', vt1,'-append');
dlmwrite('vt2.csv', vt2,'-append');
dlmwrite('vd1.csv', vd1,'-append');
dlmwrite('vd2.csv', vd2,'-append');

if (vd1 < 0) %negative voltage difference
    vneg = abs(vd1);
else
    vpos = vd1; %positive voltage difference
end

if (vd2 < 0)
    vneg = abs(vd2);
else
    vpos = vd2;
end

if (vd1 < 0) %if module 1 has negative voltage difference
    vrefnew1 = akk(1)*vref_t_abs - vneg; % assigned new reference
    voltage
    vrefnew2 = akk(2)*vref_t_abs + vneg;
else %if module 2 has negative voltage difference

```

```

        vrefnew1 = akk(1)*vref_t_abs + vneg;
        vrefnew2 = akk(2)*vref_t_abs - vneg;
    end

    %save data in csv
    dlmwrite('vpos.csv',  vpos, '-append');
    dlmwrite('vneg.csv',  vneg, '-append');
    dlmwrite('vrefnew1.csv',  vrefnew1, '-append');
    dlmwrite('vrefnew2.csv',  vrefnew2, '-append');

    mult_new1= vrefnew1/vref_t_abs;
    mult_new2= vrefnew2/vref_t_abs;
    mult_new = [mult_new1 mult_new2];
    set_modules_vmuilt2(mult_new); %update reference voltages for both
    modules

    %save data in csv
    dlmwrite('multnew1.csv',  mult_new1, '-append');
    dlmwrite('multnew2.csv',  mult_new2, '-append');

end

execution_time = toc(timer);
if get(guiHandles.logHeartbeatsCheckbox, 'Value') == 1
    write_message_line(sprintf([msg ' (%1.0f ms)\n'],
    1000*execution_time));
end

%get cell voltages
function pocv = get_cell_pocv(module, cell)
global gv;
frame.scope = 'cell';
frame.wrrd = 'read';
frame.command = 'balancing';
frame.module = module;
frame.cell = cell;
[~, value] = send_frame_wrapper(frame, 'raw');
pocv = gv*double(value);

%get system reference voltage
function vref_total = read_vref_t()
frame.scope = 'master';
frame.wrrd = 'read';
frame.command = 'control';
frame.cell = 'r_pll_vacmag';
[status3, v] = send_frame_wrapper(frame, 'raw');
v = double(v);
vref_total = v/2^7;

%set reference voltage for both modules
function set_modules_vmuilt2(mult)
global module_list
frame.scope = 'module';
frame.wrrd = 'write';
frame.command = 'voltage';

```

```

frame.cell = 'w_vmult';

for i = 1:length(module_list)
    frame.value = mult(i)*8192; %8192 is the unity multiplier
    frame.module = module_list(i);
    send_frame_wrapper(frame,'raw');
end

%get cell charges
function q = get_cell_charge(module,cell)
global gq
frame.scope = 'cell';
frame.wrrd = 'read';
frame.command = 'charge';
frame.module = module;
frame.cell = cell;
[~,value] = send_frame_wrapper(frame,'raw');
q = gq*double(value);

%set charging or discharging current
function set_master_iref2(id,iq)
%id and iq are in RMS quantities
global powerflow_direction
girx = 0.01; %MMC master interprets rx_value as 10mA per LSB
frame.scope = 'master';
frame.wrrd = 'write';
frame.command = 'control';
frame.module = 0;
frame.cell = 'w_idref';
frame.value = sqrt(2)*id/girx;
send_frame_wrapper(frame,'raw');
frame.cell = 'w_iqref';
frame.value = sqrt(2)*iq/girx;
send_frame_wrapper(frame,'raw');

if id >= 0
    powerflow_direction = 'discharging';
else
    powerflow_direction = 'charging';
end

%update cell sorting list
function send_cell_list(module,cell_list)
%we send a new cell list in two commands (list needs 48 bits altogether)
frame.scope = 'module';
frame.wrrd = 'write';
frame.command = 'balancing';
frame.module = module;
frame.cell = 'w_cell_list_first'; %first part of list
frame.value = make_value_from_list(cell_list(1:6));
send_frame_wrapper(frame,'raw');
frame.cell = 'w_cell_list_last'; %last part of list
frame.value = make_value_from_list(cell_list(7:12));
send_frame_wrapper(frame,'raw');

```

```

function value = make_value_from_list(list)
% cell_list is transferred as a 24 bit number grouped into 4 bits
% [23-20 19-16 ... 3-0]
% [ a      b      ... f ] where a is the first cell in the list
value = list(1)*2^20 + list(2)*2^16 + list(3)*2^12 + list(4)*2^8 +
list(5)*2^4 + list(6);
%the sending routine expects to get a signed 24 bit number, so if we want
to set the MSB then we need to send a negative number
if value > 2^23-1
    value = value-2^24;
end

```